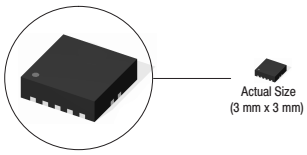


DUAL, 250-mA OUTPUT, ULTRA-LOW NOISE, HIGH PSRR, LOW-DROPOUT LINEAR REGULATOR

Check for Samples: TPS71202-EP

FEATURES

- **Dual 250-mA High-Performance RF LDOs**
- **Adjustable Output Voltage (1.2 V to 5.5 V)**
- **High PSRR: 65 dB at 10 kHz**
- **Ultra-Low Noise: 32 μVrms**
- **Fast Start-Up Time: 60 μs**
- **Stable with 2.2-μF Ceramic Capacitor**
- **Excellent Load/Line Transient Response**
- **Very Low Dropout Voltage: 125 mV at 250 mA**
- **Independent Enable Pins**
- **Thermal Shutdown and Independent Current Limit**
- **Available in Thermally-Enhanced SON Package: 3 mm × 3 mm × 1 mm**

APPLICATIONS

- **Cellular and Cordless Phones**
- **Wireless PDA/Handheld Products**
- **PCMCIA/Wireless LAN Applications**
- **Digital Camera/Camcorder/Internet Audio**
- **DSP/FPGA/ASIC/Controllers and Processors**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

DESCRIPTION

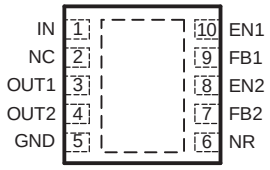
The TPS71202 low-dropout (LDO) voltage regulator is tailored to noise-sensitive and RF applications. It features dual 250-mA LDOs with ultra-low noise, high power-supply rejection ratio (PSRR), and fast transient and start-up response. Each regulator output is stable with low-cost 2.2-μF ceramic output capacitors and features very low dropout voltages (125 mV typical at 250 mA). The regulator achieves fast start-up times (approximately 60 μs with a 0.001-μF bypass capacitor) while consuming very low quiescent current (300 μA typical with both outputs enabled). When the device is placed in standby mode, the supply current is reduced to less than 0.3 μA typical. The regulator exhibits approximately 32 μVrms of output voltage noise with V_{OUT} = 2.8 V and a 0.01-μF noise reduction (NR) capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from high PSRR, low noise, and fast line and load transient features. The TPS71202 is offered in a thin 3-mm × 3-mm SON package and is fully specified from –55°C to 125°C (T_J).

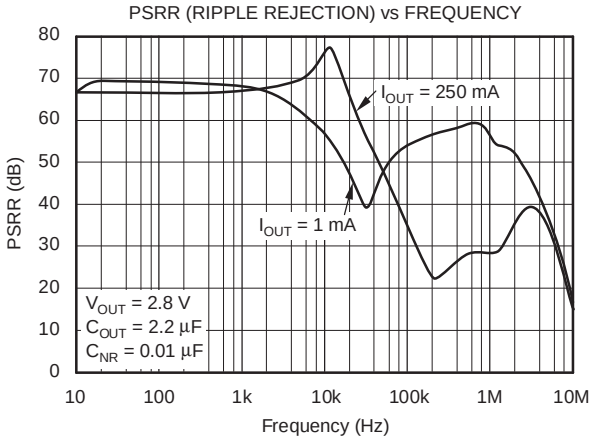
(1) Custom temperature ranges available

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DRC PACKAGE
3-mm × 3-mm SON
(TOP VIEW)





ORDERING INFORMATION(1)

T_J	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SON-10 – DRC	Reel of 250	TPS71202MDRCTEP	CVQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range unless otherwise noted(1)

V_{IN}	Input voltage range	IN	–0.3 V to 6 V
V_{EN1}, V_{EN2}	Input voltage range	EN1, EN2	–0.3 V to V_{IN} + 0.3 V
V_{OUT}	Output voltage range	OUT	–0.3 V to 6 V
	Peak output current		Internally limited
	Output short-circuit duration		Indefinite
	Continuous total power dissipation		See Thermal Information table
T_J	Junction temperature range		–55°C to 150°C
	Storage temperature range		–65°C to 150°C
ESD	Electrostatic discharge rating	Human-Body Model (HBM)	2000 V
		Charged-Device Model (CDM)	500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS71202-EP DRC (10 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	49.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	70.0	
θ_{JB}	Junction-to-board thermal resistance	17.8	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	15.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	5.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

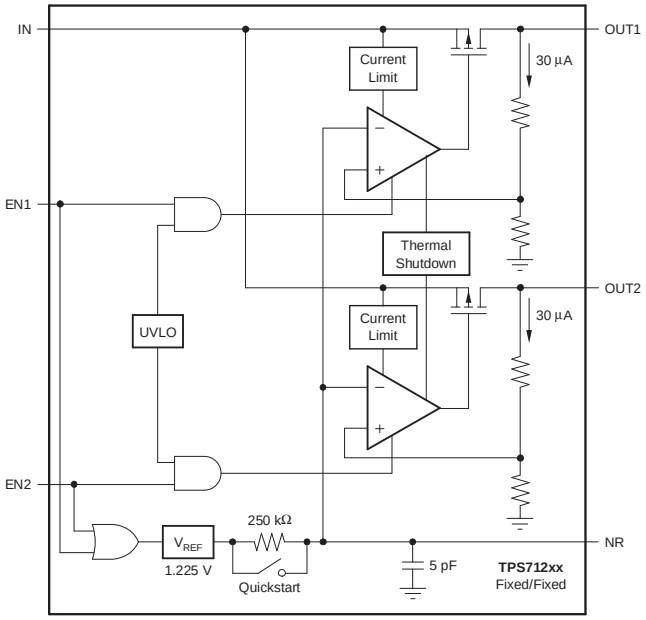
ELECTRICAL CHARACTERISTICS

over operating temperature range (T_J = –55°C to +125°C), V_{IN} = highest ($V_{OUT(nom)}$ + 1 V) or 2.7 V (whichever is greater), I_{OUT} = 1 mA, $V_{EN1,\ 2}$ = 1.2 V, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, and adjustable LDOs are tested at V_{OUT} = 3.0 V (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.7		5.5	V
V_{FB}	Internal reference (adjustable LDOs)			1.200	1.225	1.250	V
V_{OUT}	Output voltage range (adjustable LDOs)			V_{FB}		5.5 – V_{DO}	V
	Accuracy(1)	Nominal	T_J = +25°C, I_{OUT} = 0 mA	–1.5		+1.5	%
		Over V_{IN}, I_{OUT}, and temperature	V_{OUT} + 1.0 V ≤ V_{IN} ≤ 5.5 V, 0 µA ≤ I_{OUT} ≤ 250 mA	–3	1	+3	
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation(1)		V_{OUT} + 1.0 V ≤ V_{IN} ≤ 5.5 V		0.05		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation		0 µA ≤ I_{OUT} ≤ 250 mA		0.8		%/mA
V_{DO}	Dropout voltage (V_{IN} = $V_{OUT(nom)}$ – 0.1V)		I_{OUT1} = I_{OUT2} = 250 mA		125	315	mV
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	400	600	800	mA
I_{GND}	Ground pin current	One LDO enabled	I_{OUT} = 1 mA (enabled channel)		190	250	µA
		Both LDOs enabled	I_{OUT1} = I_{OUT2} = 1 mA to 250 mA		300	600	
I_{SHDN}	Shutdown current(2)		V_{EN} ≤ 0.4 V, 0 V ≤ V_{IN} ≤ 5.5 V		0.3	2.0	µA
I_{FB}	FB pin current				0.1	1.50	µA
V_n	Output noise voltage, BW = 10 Hz to 100 kHz		No C_{NR}, I_{OUT} = 250 mA		80.0 × V_{OUT}		µVrms
			C_{NR} = 0.01 µF, I_{OUT} = 250 mA		11.8 × V_{OUT}		
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100 Hz, I_{OUT} = 250 mA		65		dB
			f = 10 kHz, I_{OUT} = 250 mA		65		
t_{STR}	Startup time		V_{OUT} = 2.85 V, R_L = 30Ω, C_{NR} = 0.001 µF		60		µs
V_{IH}	Enable threshold high (EN1, EN2)			1.2		V_{IN}	V
V_{IL}	Enable threshold low (EN1, EN2)			0		0.4	V
I_{EN}	Enable pin current (EN1, EN2)		V_{IN} = V_{EN} = 5.5 V	–1		1	µA
T_{SD}	Thermal shutdown temperature		Shutdown Temp increasing		+160		°C
			Reset Temp decreasing		+140		
UVLO	Undervoltage lockout threshold		V_{IN} rising	2.25		2.65	V
	Undervoltage lockout hysteresis		V_{IN} falling		100		mV

(1) Minimum V_{IN} = (V_{OUT} + V_{DO}) or 2.7 V, whichever is greater.
(2) For the adjustable version, this applies only after V_{IN} is applied; then V_{EN} transitions from high to low.

FUNCTIONAL BLOCK DIAGRAM — FIXED VERSION



FUNCTIONAL BLOCK DIAGRAM — ADJUSTABLE VERSION

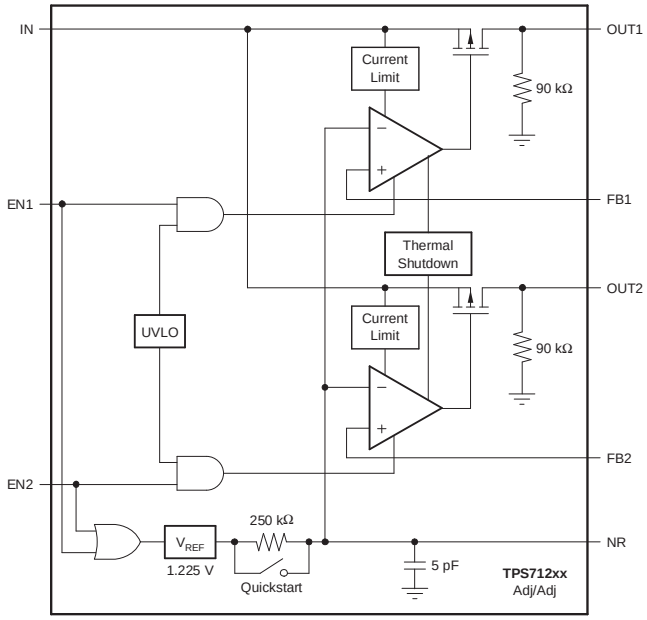


Table 1. TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	DRC	
IN	1	Unregulated input supply. A small 0.1-µF capacitor should be connected from IN to GND.
GND	5, Pad	Ground
OUT1	3	Output of the regulator. A small 2.2-µF ceramic capacitor is required from this pin to ground to assure stability.
OUT2	4	Same as OUT1 but for LDO2.
EN1	10	Driving the enable pin (EN) high turns on LDO1. Driving this pin low puts LDO1 into shutdown mode, reducing operating current. The enable pin should be connected to IN if not used.
EN2	8	Same as EN1 but controls LDO2.
FB1	9	Feedback for channel 1
FB2	7	Feedback for channel 2
NR	6	Noise reduction pin; connect an external bypass capacitor to reduce LDO output noise.
NC	2	No connection.

TYPICAL CHARACTERISTICS

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, V_{EN} = 1.2 V, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted)

OUTPUT VOLTAGE vs INPUT VOLTAGE

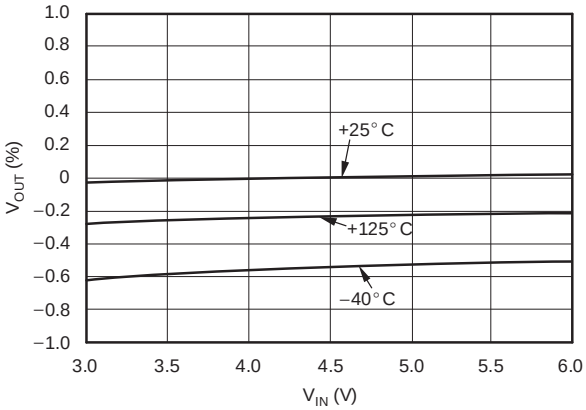


Figure 1.

OUTPUT VOLTAGE vs OUTPUT CURRENT

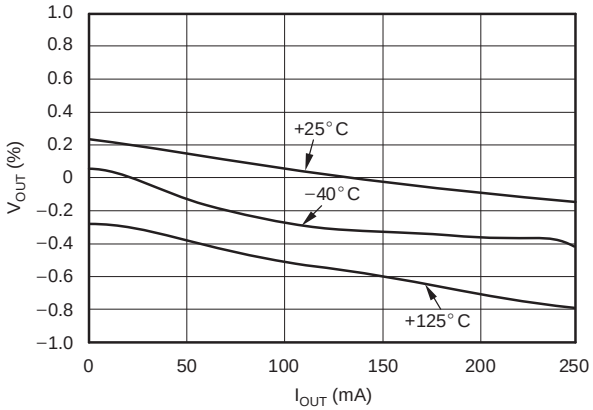


Figure 2.

OUTPUT VOLTAGE vs TEMPERATURE

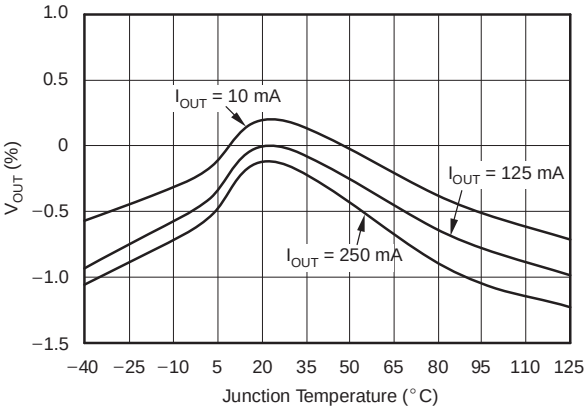


Figure 3.

DROPOUT VOLTAGE vs INPUT VOLTAGE (ADJUSTABLE VERSION)

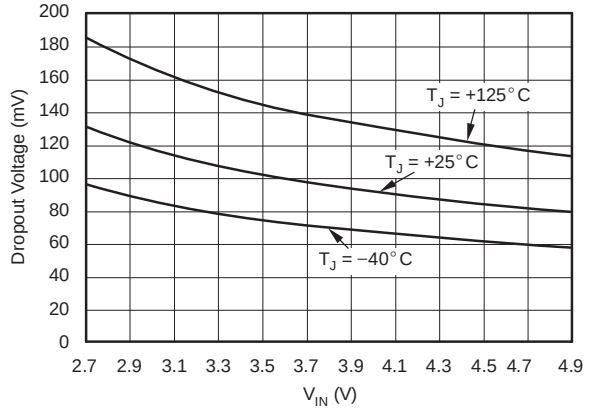


Figure 4.

TPS71256
DROPOUT VOLTAGE vs OUTPUT CURRENT

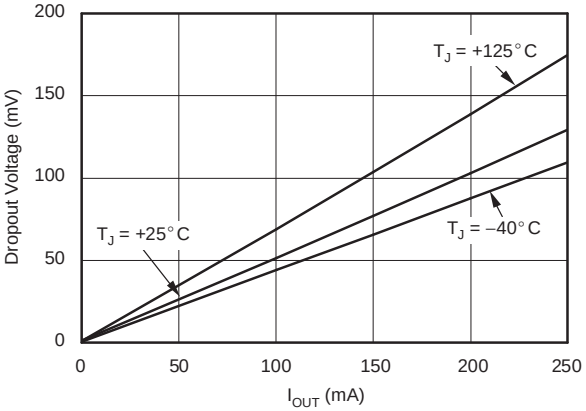


Figure 5.

TPS71256
DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

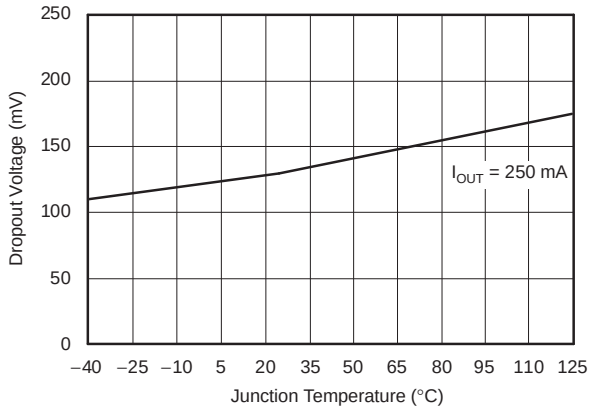


Figure 6.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, V_{EN} = 1.2 V, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted)

GROUND PIN CURRENT vs INPUT VOLTAGE

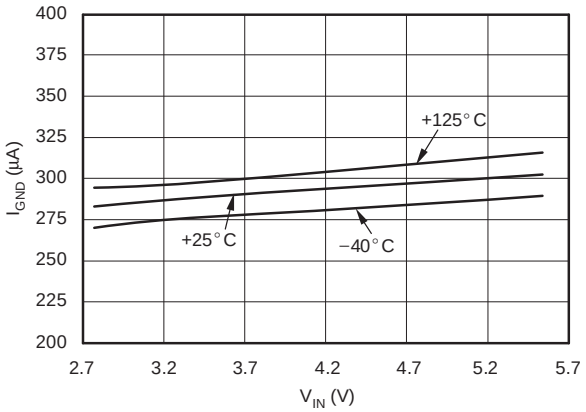


Figure 7.

GROUND PIN CURRENT vs I_{OUT}

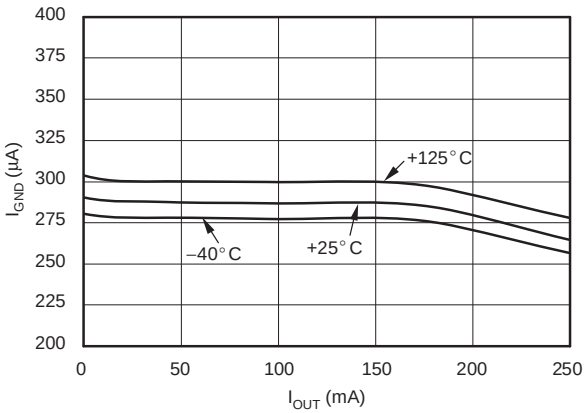


Figure 8.

GROUND PIN CURRENT vs JUNCTION TEMPERATURE

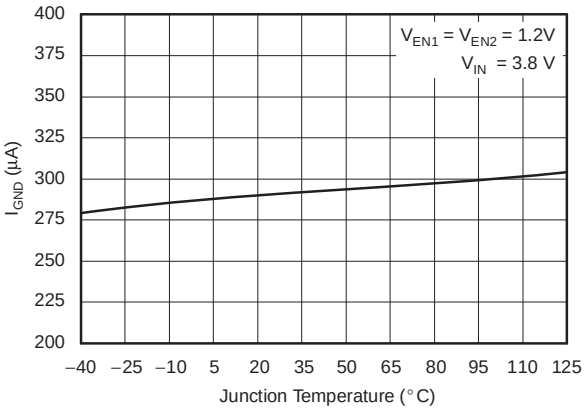


Figure 9.

GROUND PIN CURRENT vs JUNCTION TEMPERATURE (DISABLED)

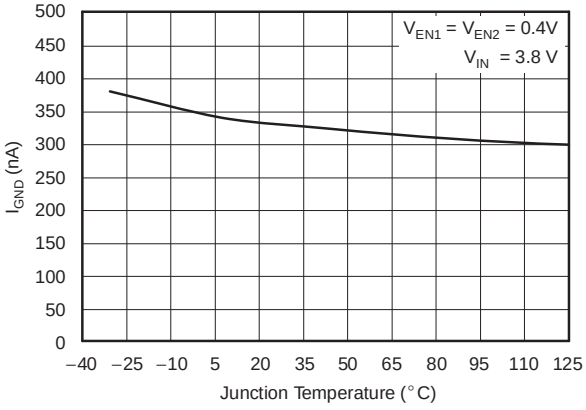


Figure 10.

CURRENT LIMIT vs JUNCTION TEMPERATURE

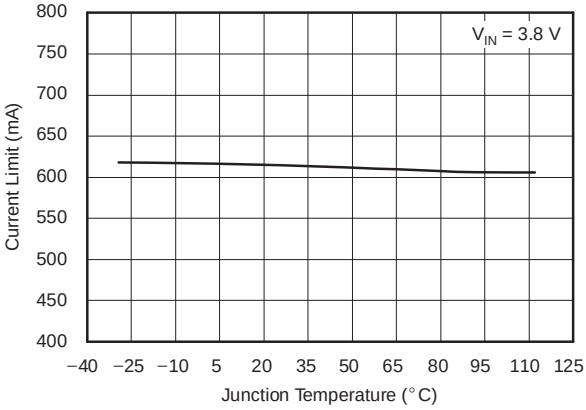


Figure 11.

TPS71256 LINE TRANSIENT RESPONSE

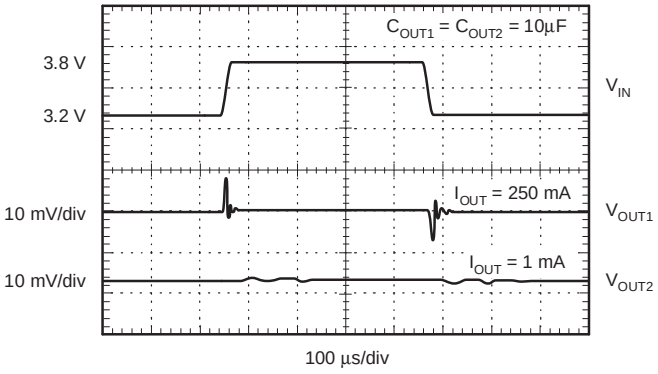


Figure 12.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, V_{EN} = 1.2 V, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted)

TPS71256
LOAD TRANSIENT RESPONSE AND V_{OUT2} CROSSTALK

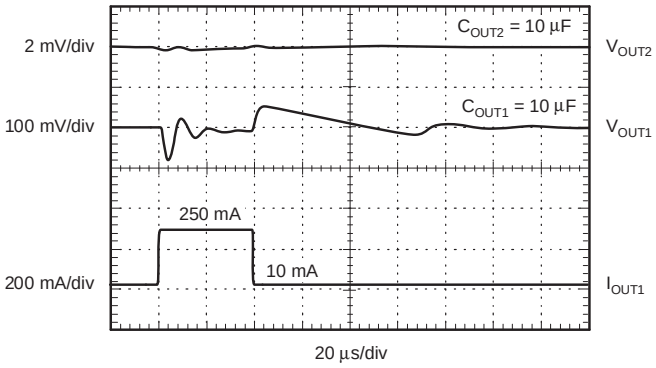


Figure 13.

TPS71256
CHANNEL-TO-CHANNEL ISOLATION vs FREQUENCY

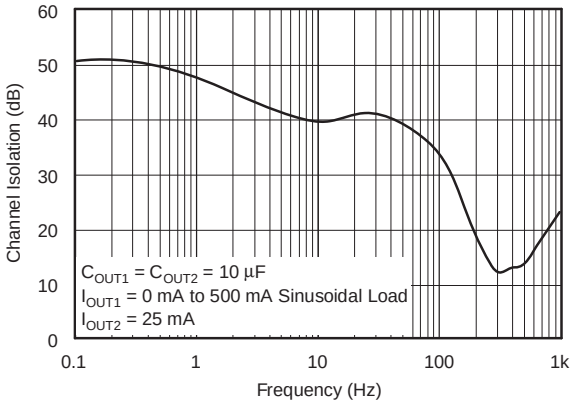


Figure 14.

TPS71256
TURN-ON/TURN-OFF RESPONSE AND V_{OUT2} CROSSTALK

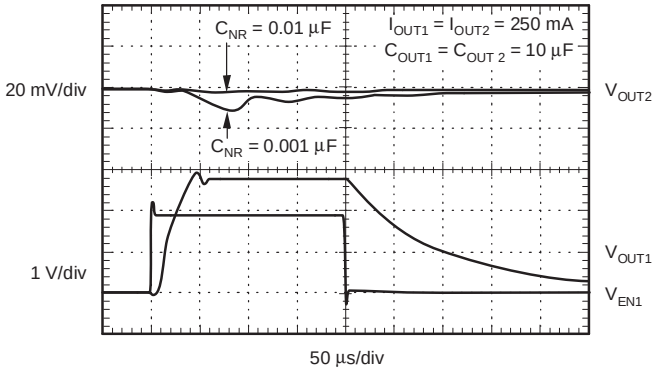


Figure 15.

TPS71229
POWER-UP/POWER-DOWN

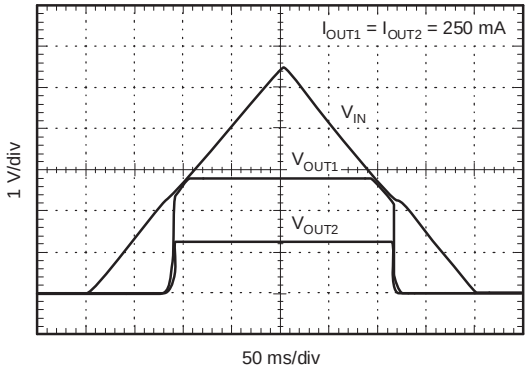


Figure 16.

TOTAL NOISE vs C_{NR}

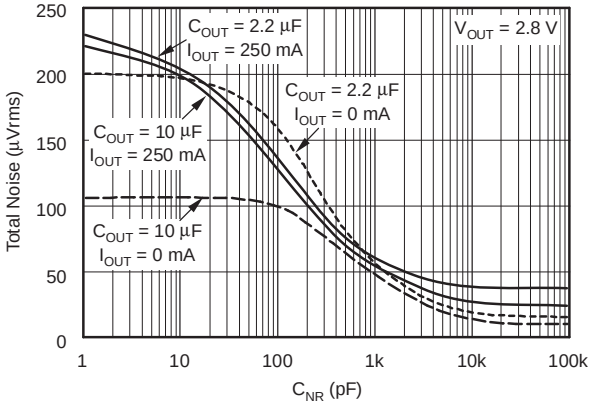


Figure 17.

NOISE SPECTRAL DENSITY
C_{OUT} = 2.2 µF

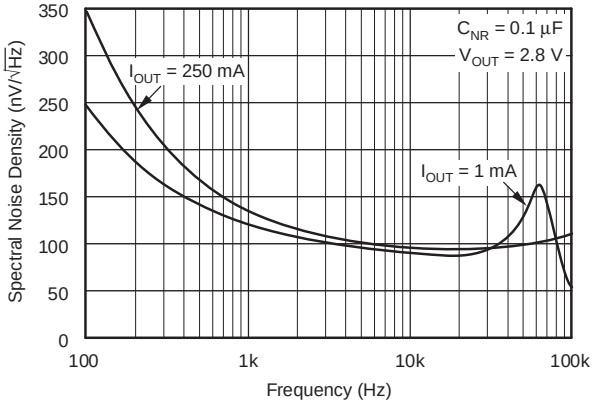


Figure 18.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, V_{EN} = 1.2 V, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted)

NOISE SPECTRAL DENSITY
C_{OUT} = 10 µF

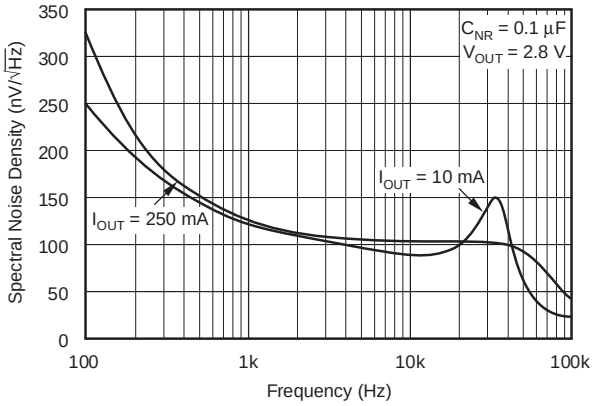


Figure 19.

NOISE SPECTRAL DENSITY vs C_{NR}

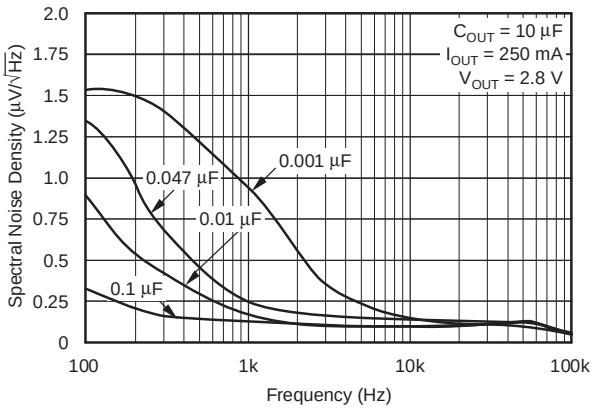


Figure 20.

PSRR (RIPPLE REJECTION) vs FREQUENCY

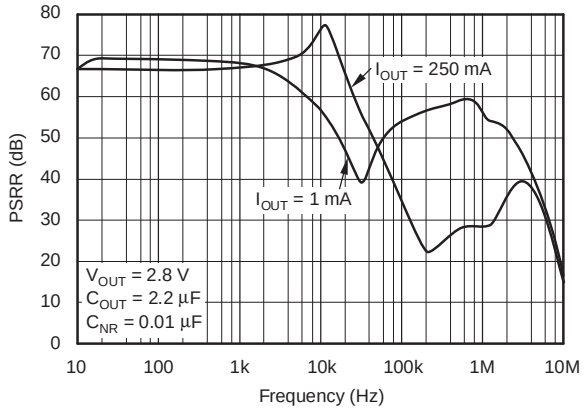


Figure 21.

PSRR (RIPPLE REJECTION) vs FREQUENCY

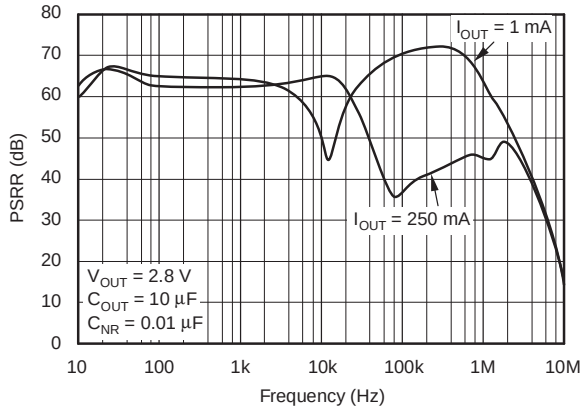


Figure 22.

PSRR (RIPPLE REJECTION) vs V_{IN} − V_{OUT}

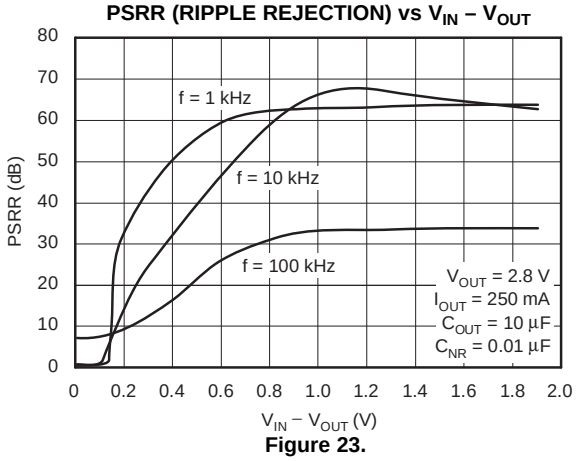


Figure 23.

APPLICATION INFORMATION

The TPS71202 dual low-dropout (LDO) regulator has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout, high PSRR, ultra-low output noise, and low quiescent current (190 μA typical per channel). When both outputs are disabled, the supply currents are reduced to less than 2 μA.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

A 0.1-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS71202, is required for stability. It improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast rise-time load transients are anticipated and the device is located several inches from the power source.

The TPS71202 requires an output capacitor connected between the outputs and GND to stabilize the internal control loops. The minimum recommended output capacitor is 2.2 μF. If an output voltage of 1.8 V or less is chosen, the minimum recommended output capacitor is 4.7 μF. Any ceramic capacitor that meets the minimum output capacitor requirements is suitable. Capacitors with higher ESR may be used, provided the ESR is less than 1 Ω.

OUTPUT NOISE

The internal voltage reference is a key source of noise in an LDO regulator. The TPS71202 has an NR pin that is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external ceramic bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. To achieve a fast startup, the 250-kΩ internal resistor is shorted for 400 μs after the device is enabled.

Because the primary noise source is the internal voltage reference, the output noise is greater for higher output voltage versions. For the case where no noise reduction capacitor is used, the typical noise (μVrms) over 10 Hz to 100 kHz is 80 times the output voltage. If a 0.01-μF capacitor is used from the NR pin to ground, the noise (μVrms) drops to 11.8 times the output voltage.

STARTUP CHARACTERISITCS

To minimize startup overshoot, the TPS71202 initially targets an output voltage that is approximately 80% of the final value. To avoid a delayed startup time, noise reduction capacitors of 0.01 μF or less are recommended. Larger noise reduction capacitors cause the output to hold at 80% until the voltage on the noise reduction capacitor exceeds 80% of the bandgap voltage. The typical startup time with a 0.001-μF noise reduction capacitor is 60 μs. Once one of the output voltages is present, the startup time of the other output is not affected by the noise reduction capacitor.

PROGRAMMING THE TPS71202 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS71202 dual adjustable regulator is programmed using an external resistor divider, as shown in Figure 24. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where V_{REF} = 1.225 V (the internal reference voltage).

Resistors R2 and R4 should be chosen for approximately a 40-μA divider current. Lower value resistors can be used for improved noise performance but consume more power. Higher values should be avoided because leakage current at FB increases the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 40 μA, and then calculate R1 using Equation 2:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (2)$$

To improve the stability and noise performance of the adjustable version, a small compensation capacitor can be placed between OUT and FB.

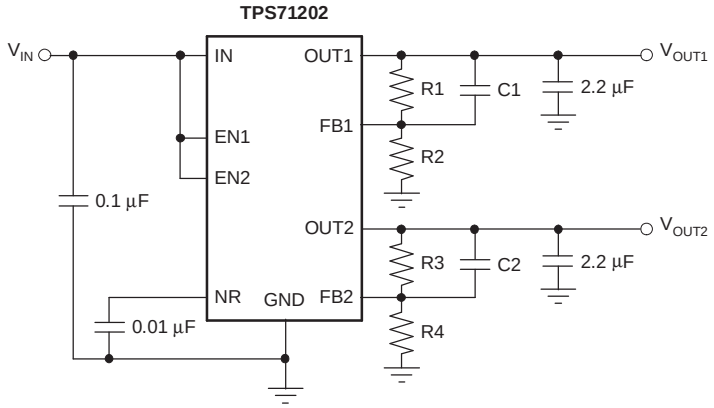
For voltages ≤ 1.8 V, the value of this capacitor should be 100 pF. For voltages > 1.8 V, the approximate value of this capacitor can be calculated as Equation 3:

$$C1 = \frac{(3 \times 10^5) \times (R1 + R2)}{(R1 \times R2)} \quad (pF) \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in Figure 24. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage ≤ 1.8 V is chosen, then the minimum recommended output capacitor is 4.7 μF instead of 2.2 μF.

DROPOUT VOLTAGE

The TPS712xx uses a PMOS pass transistor to achieve extremely low dropout. When (V_{IN} - V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS,\ ON}$ of the PMOS pass element. Dropout voltages at lower currents can be approximated by calculating the effective $R_{DS,\ ON}$ of the pass element and multiplying that resistance by the load current. $R_{DS,\ ON}$ of the pass element can be obtained by dividing the dropout voltage by the rated output current.



Output Voltage Programming Guide

V_{OUT}	R1/R3	R2/R4	C1/C2
1.225 V	Short	Open	Open
1.5 V	7.15 kΩ	30.1 kΩ	100 pF
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.0 V	43.2 kΩ	30.1 kΩ	15 pF
3.3 V	49.9 kΩ	30.1 kΩ	15 pF
4.75 V	86.6 kΩ	30.1 kΩ	15 pF

Figure 24. Adjustable LDO Regulator Programming

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces overshoot/undershoot magnitude but increase duration of the transient response. In the adjustable version, the addition of a capacitor, C_{FB}, from the output to the feedback pin also improves stability and transient response. The transient response of the TPS71202 is enhanced with an active pulldown that engages when the output is overvoltaged. The active pulldown decreases the output recovery time when the load is removed. Figure 13 in the *Typical Characteristics* section shows the output transient response.

SHUTDOWN

Both enable pins are active high and are compatible with standard TTL-CMOS levels. The device is only completely disabled when both EN1 and EN2 are logic low. In this state, the LDO is completely off and the ground pin current drops to approximately 100 nA. With one output disabled, the ground pin current is slightly greater than half the nominal value. When shutdown capability is not required, the enable pins should be connected to the input supply.

INTERNAL CURRENT LIMIT

The TPS71202 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage.

The TPS71202 PMOS-pass transistors have a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (that is, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting may be appropriate.

THERMAL PROTECTION

Thermal protection disables both outputs when the junction temperature of either channel rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS71202 is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS71202 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for a JEDEC high-K board is shown in the *Dissipation Ratings* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to ensure the required output voltage.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS71202MDRCTEP	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	CVQ
TPS71202MDRCTEP.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	CVQ
V62/08621-01XE	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	CVQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

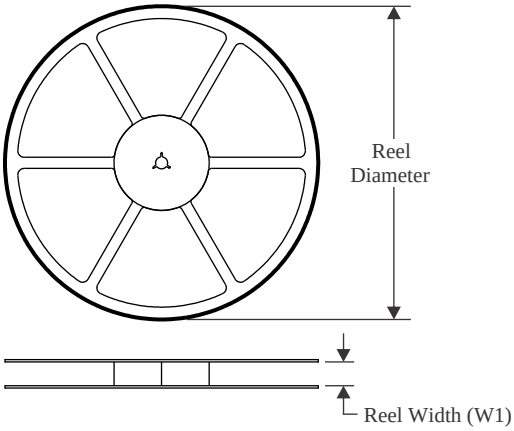
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

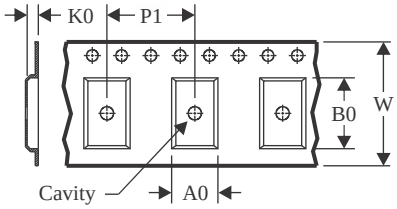
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

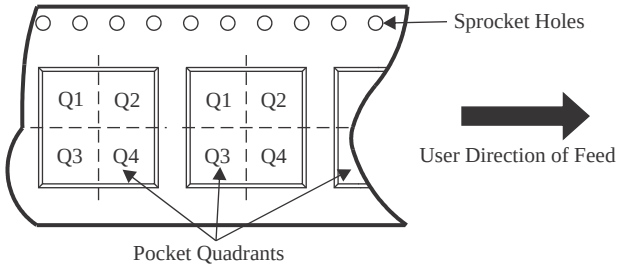


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

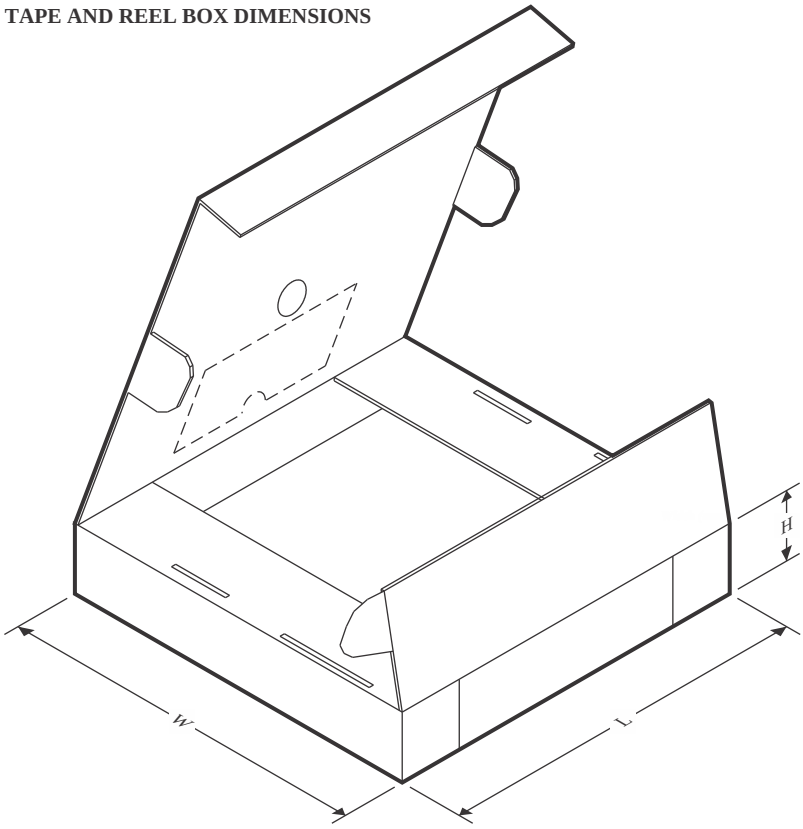
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71202MDRCTEP	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS71202MDRCTEP	VSON	DRC	10	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

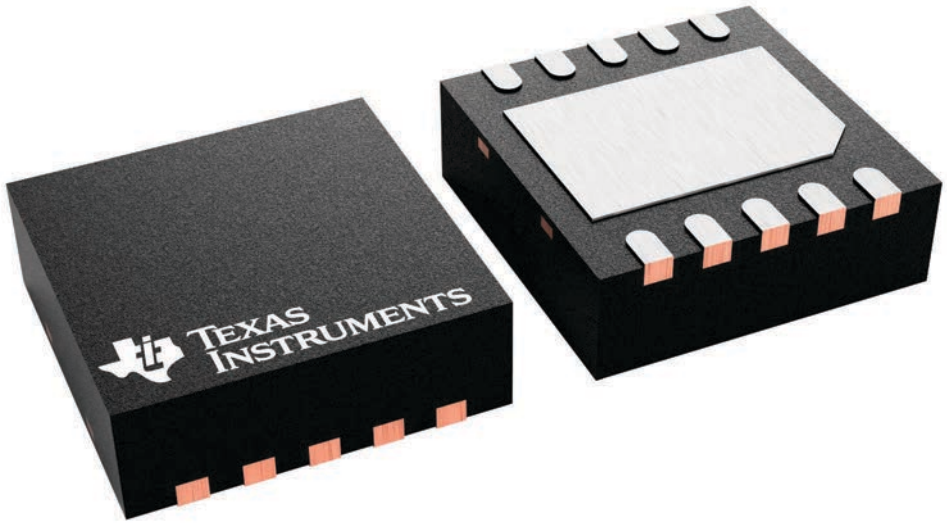
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



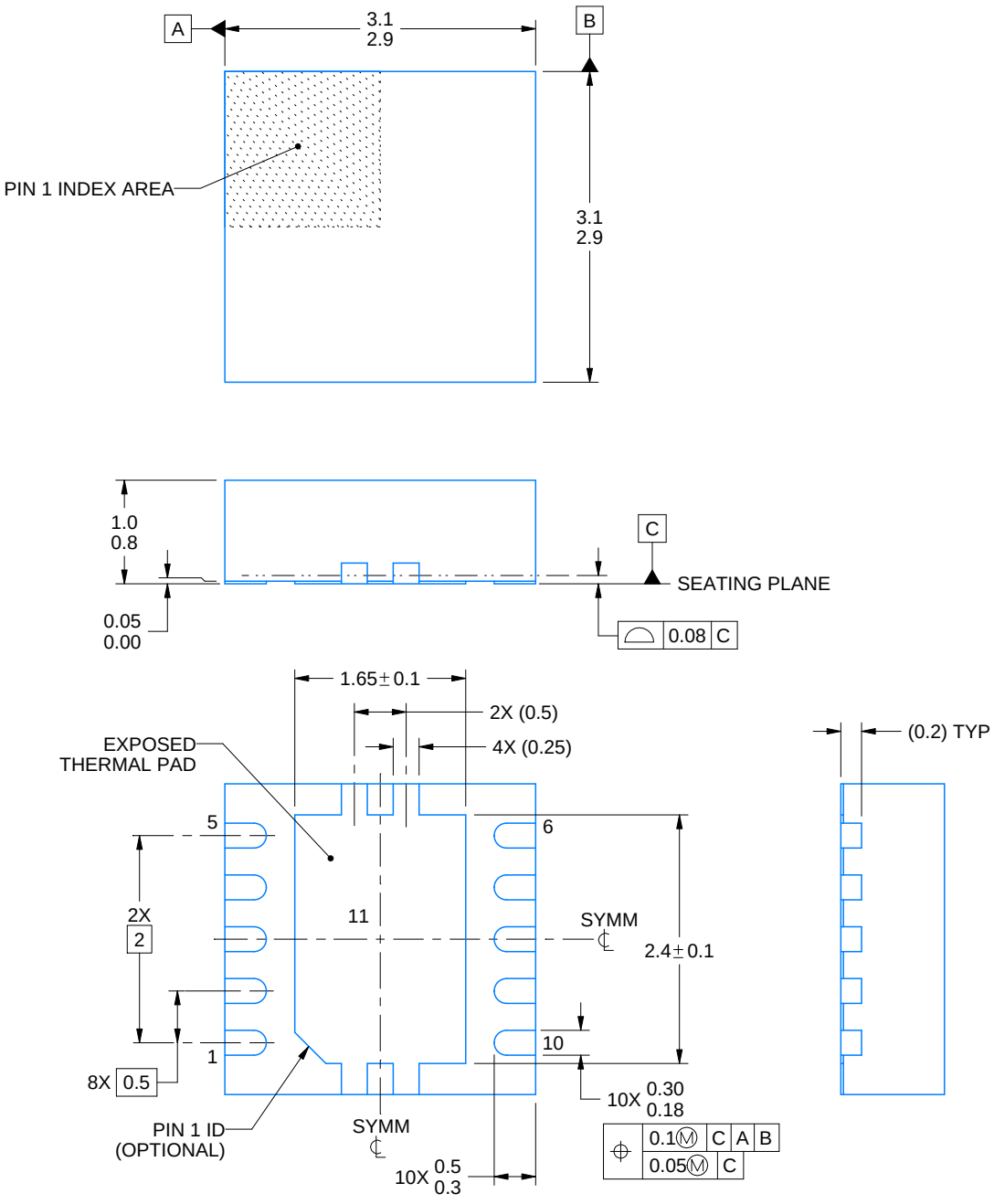
4226193/A

DRC0010J

PACKAGE OUTLINE

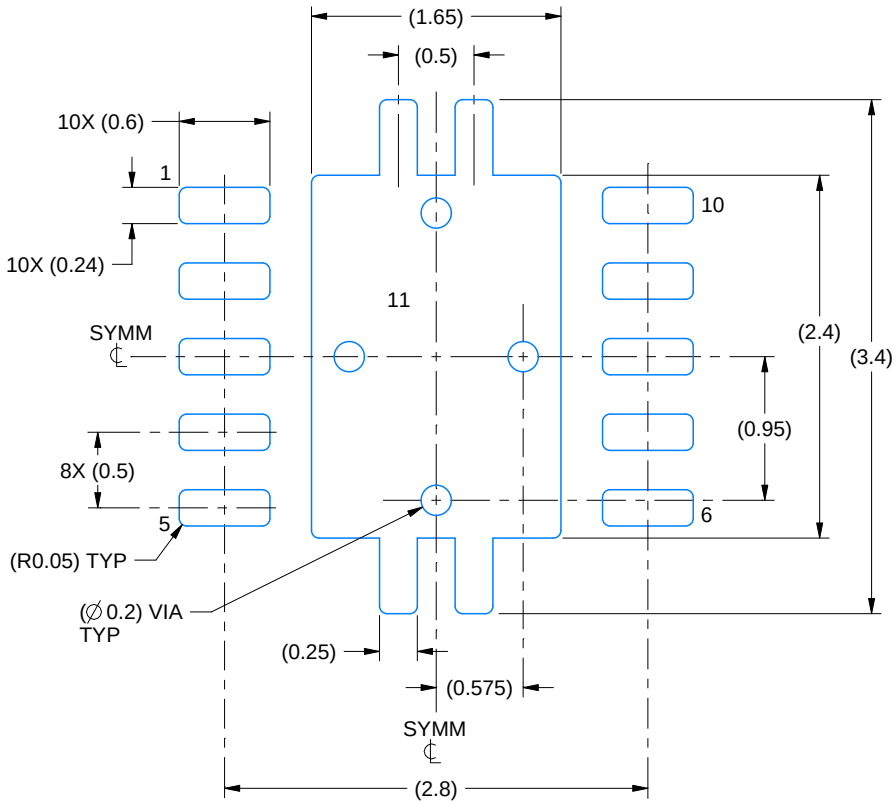
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

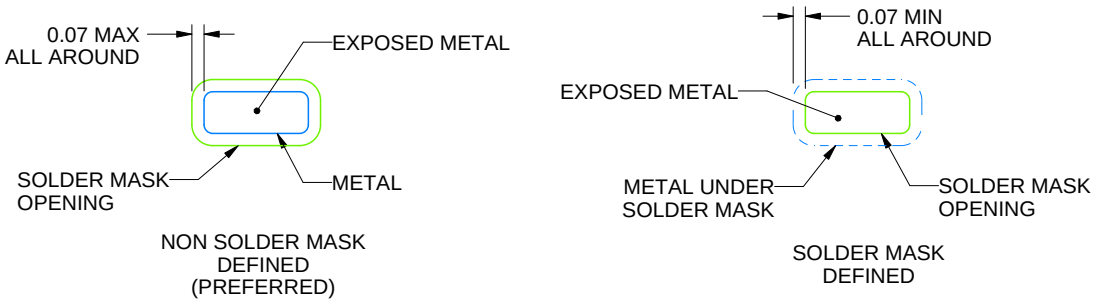


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

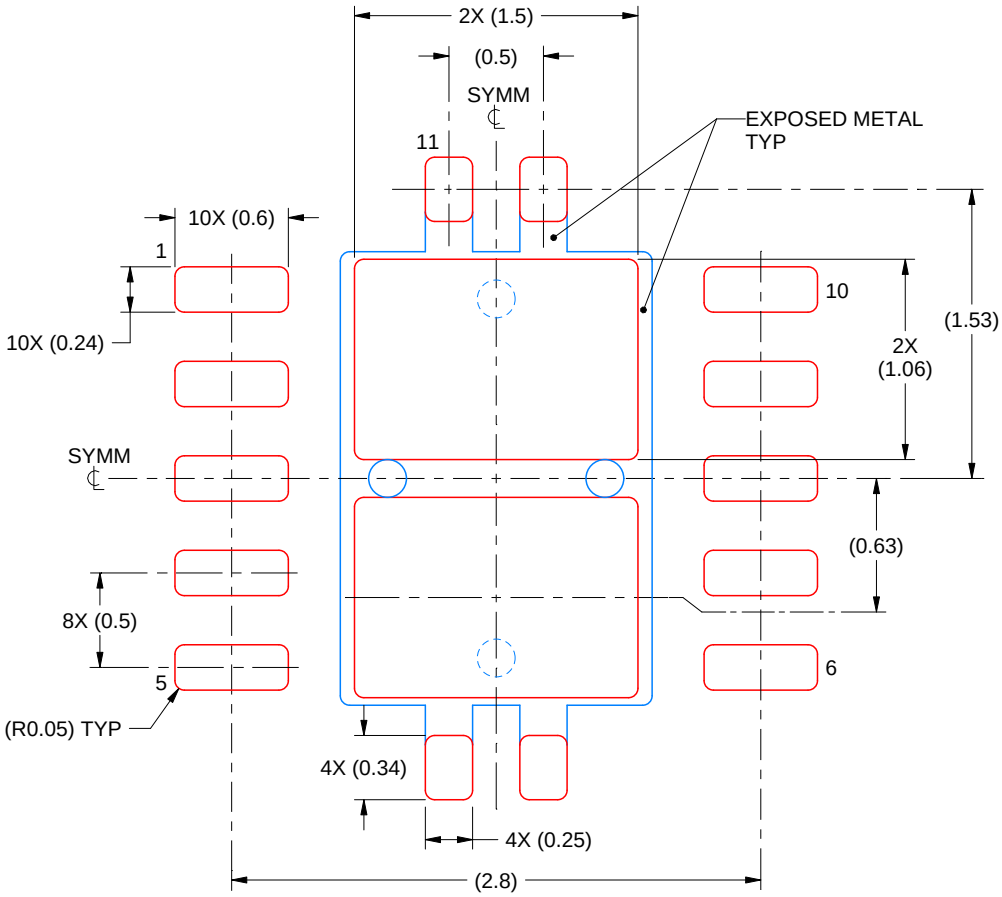
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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