

# DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATOR WITH POWER-UP SEQUENCING FOR SPLIT-VOLTAGE DSP SYSTEMS

Check for Samples: [TPS70175-Q1](#)

## FEATURES

- Qualified for Automotive Applications
- Dual Output Voltages for Split-Supply Applications
- Selectable Power-Up Sequencing for DSP Applications
- Output Current Range of 500 mA on Regulator 1 and 250 mA on Regulator 2
- Fast Transient Response
- Voltage Options: 5 V/2.5 V
- Open Drain Power-On Reset With 30-ms Delay
- Open Drain Power Good for Regulator 1
- Ultra Low 190- $\mu$ A (Typ) Quiescent Current
- 1- $\mu$ A Input Current During Standby
- Low Noise = 65  $\mu$ V<sub>RMS</sub> Without a Bypass Capacitor
- Quick Output Capacitor Discharge Feature
- Two Manual Reset Inputs
- 2% Accuracy Over Load and Temperature
- Undervoltage Lockout (UVLO) Feature
- 20-Pin PowerPAD™ TSSOP Package
- Thermal Shutdown Protection

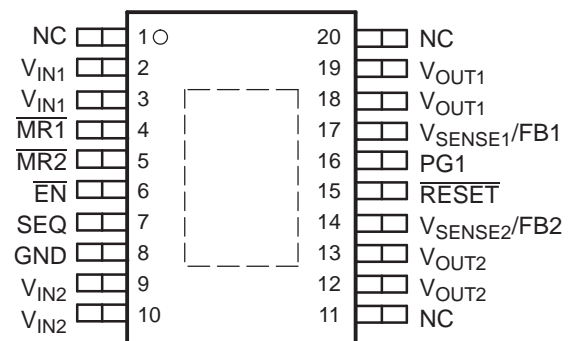
## DESCRIPTION

The TPS70175 is designed to provide a complete power management solution for the TMS320™ DSP family, processor power, ASIC, FPGA, and digital applications where dual output voltage regulators are required. Easy programmability of the sequencing function makes the TPS70175 ideal for any TMS320 DSP applications with power sequencing requirements. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit, manual reset inputs, and an enable function, provide a complete system solution.

The TPS70175 voltage regulator offers low dropout voltage and dual outputs with power-up sequence control, which is designed primarily for DSP applications. These devices have extremely low noise output performance without using any added filter bypass capacitors and are designed to have a fast transient response and be stable with 10- $\mu$ F low ESR capacitors.

This device has a fixed 5 V/2.5 V voltage option. Regulator 1 can support up to 500 mA and regulator 2 can support up to 250 mA. Separate voltage inputs allow the designer to configure the source power.

**PWP PACKAGE  
(TOP VIEW)**

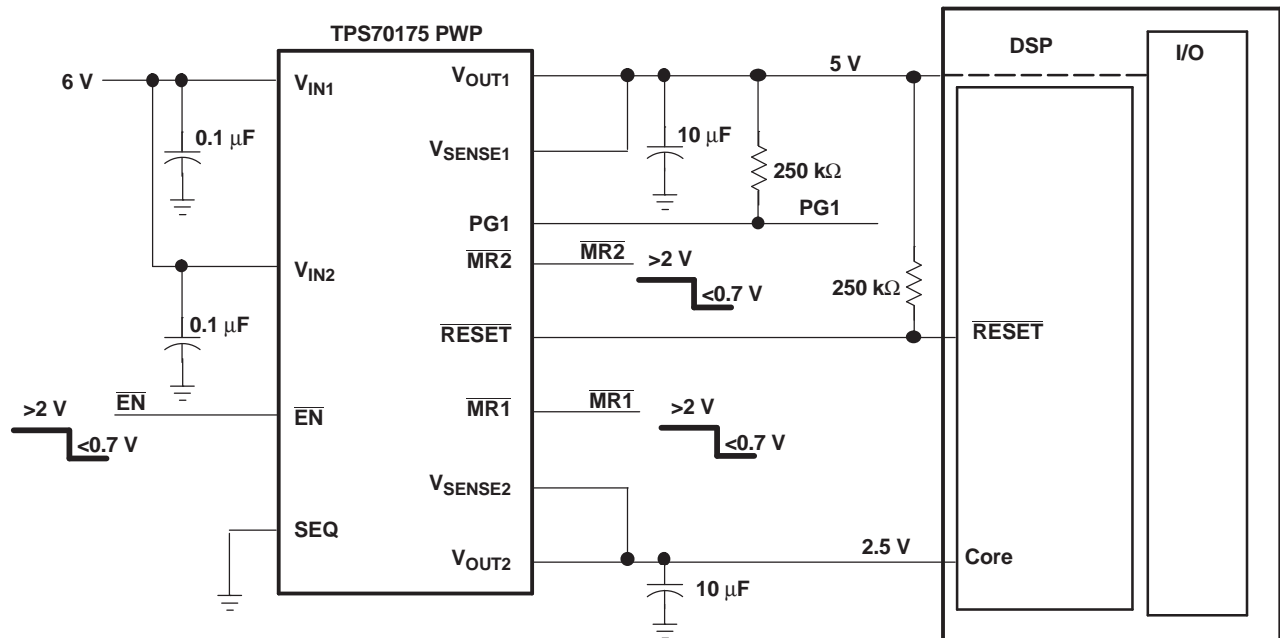


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Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 170 mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (maximum of 280  $\mu$ A over the full range of output current). This LDO family also features a sleep mode; applying a high signal to  $\overline{\text{EN}}$  (enable) shuts down both regulators, reducing the input current to 1  $\mu$ A at  $T_J = 25^\circ\text{C}$ .

The device is enabled when the  $\overline{\text{EN}}$  pin is connected to a low-level input voltage. The output voltages of the two regulators are sensed at the  $V_{\text{SENSE1}}$  and  $V_{\text{SENSE2}}$  pins, respectively.

The input signal at the SEQ pin controls the power-up sequence of the two regulators. When the device is enabled and the SEQ terminal is pulled high or left open,  $V_{\text{OUT2}}$  turns on first and  $V_{\text{OUT1}}$  remains off until  $V_{\text{OUT2}}$  reaches approximately 83% of its regulated output voltage. At that time  $V_{\text{OUT1}}$  is turned on. If  $V_{\text{OUT2}}$  is pulled below 83% (for example, an overload condition),  $V_{\text{OUT1}}$  is turned off. Pulling the SEQ terminal low reverses the power-up order and  $V_{\text{OUT1}}$  is turned on first. The SEQ pin is connected to an internal pullup current source.

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off (disabled).

The PG1 pin reports the voltage conditions at  $V_{\text{OUT1}}$ , which can be used to implement an SVS for the circuitry supplied by regulator 1.

The TPS70175 features a  $\overline{\text{RESET}}$  (SVS, POR, or Power-On Reset).  $\overline{\text{RESET}}$  output initiates a reset in DSP systems and related digital applications in the event of an undervoltage condition.  $\overline{\text{RESET}}$  indicates the status of  $V_{\text{OUT2}}$  and both manual reset pins (MR1 and MR2). When  $V_{\text{OUT2}}$  reaches 95% of its regulated voltage and MR1 and MR2 are in the logic high state,  $\overline{\text{RESET}}$  goes to a high impedance state after a 30-ms delay.  $\overline{\text{RESET}}$  goes to the logic low state when the  $V_{\text{OUT2}}$  regulated output voltage is pulled below 95% (for example, an overload condition) of its regulated voltage. To monitor  $V_{\text{OUT1}}$ , the PG1 output pin can be connected to MR1 or MR2.

The device has an undervoltage lockout (UVLO) circuit which prevents the internal regulators from turning on until  $V_{\text{IN1}}$  reaches 2.5 V.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

T <sub>J</sub>	REGULATOR 1 V <sub>O</sub> (V)	REGULATOR 2 V <sub>O</sub> (V)	TSSOP (PWP) <sup>(2)</sup>
–40°C to 125°C	5 V	2.5 V	TPS70175QPWPRQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		UNIT
Input voltage range: V <sub>IN1</sub> , V <sub>IN2</sub> <sup>(2)</sup>	–0.3 to +7	V
Voltage range at $\overline{\text{EN}}$	–0.3 to +7	V
Output voltage range (V <sub>OUT1</sub> , V <sub>SENSE1</sub> )	5.5	V
Output voltage range (V <sub>OUT2</sub> , V <sub>SENSE2</sub> )	5.5	V
Maximum $\overline{\text{RESET}}$ , PG1 voltage	7	V
Maximum $\overline{\text{MR1}}$ , $\overline{\text{MR2}}$ , and SEQ voltage	V <sub>IN1</sub>	V
Peak output current	Internally limited	
Junction temperature range, T <sub>J</sub>	–40 to +150	°C
Storage temperature range, T <sub>stg</sub>	–65 to +150	°C
ESD rating, HBM <sup>(3)</sup>	3 (H2)	kV
ESD rating, CDM <sup>(3)</sup>	1.5 (C5)	kV
ESD rating, MM <sup>(3)</sup>	150 (M2)	V
θ <sub>JA</sub> <sup>(4)</sup>	32.63	°C / W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are tied to network ground.

(3) ESD Protection Level per AEC Q100 Classification

(4) This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1-oz copper on a 4-in by 4-in ground layer. For more information, see Texas Instruments technical brief SLMA002.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)(2)</sup>		TPS70175-Q1	UNITS
		PWP (20 PINS)	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	74.1	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	43.1	
θ <sub>JB</sub>	Junction-to-board thermal resistance	19.7	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.9	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	17.3	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	1.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/spr953).

(2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](http://www.ti.com/lit/pdf/sla666).

## RECOMMENDED OPERATING CONDITIONS

Over operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage, $V_I$ <sup>(1)</sup>	2.7	6	V
Output current, $I_O$ (regulator 1)	0	500	mA
Output current, $I_O$ (regulator 2)	0	250	mA
Operating junction temperature, $T_J$	–40	125	°C

(1) To calculate the minimum input voltage for maximum output current, use the following equation:  $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$ .

## ELECTRICAL CHARACTERISTICS

Over recommended operating junction temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{IN1}$  or  $V_{IN2} = V_{OUT(nom)} + 1\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $\overline{EN} = 0$ ,  $C_O = 33\text{ }\mu\text{F}$ , (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>O</sub>	Output voltage <sup>(1), (2)</sup>	2.5-V output	2.7 V < V <sub>I</sub> < 6 V,	T <sub>J</sub> = 25°C		2.5		V
			2.7 V < V <sub>I</sub> < 6 V,		2.45	2.55		
		5-V output	2.7 V < V <sub>I</sub> < 6 V,	T <sub>J</sub> = 25°C		5		
			2.7 V < V <sub>I</sub> < 6 V,		4.9	5.1		
Quiescent current (GND current) for regulator 1 and regulator 2, $\overline{\text{EN}} = 0\text{ V}^{(1)}$			See <sup>(2)</sup>	T <sub>J</sub> = 25°C		190		μA
			See <sup>(2)</sup>			280		
Output voltage line regulation for regulator 1 and regulator 2			5.3 V < V <sub>IN</sub> < 6 V	V <sub>OUT1</sub>		4.95	5.05	V
			3.5 V < V <sub>IN</sub> < 6 V	V <sub>OUT2</sub>		2.475	2.525	
V <sub>n</sub>	Output noise voltage	Regulator 1	BW 300 Hz to 50 kHz,	C <sub>O</sub> = 33 μF, T <sub>J</sub> = 25°C		65		μV <sub>RMS</sub>
		Regulator 2				65		
Output current limit		Regulator 1	V <sub>OUT</sub> = 0 V			1.6	2	A
		Regulator 2				0.75	1.1	
Thermal shutdown junction temperature						150		°C
I <sub>I(standby)</sub>	Standby current	Regulator 1	$\overline{\text{EN}} = V_I$ ,	T <sub>J</sub> = 25°C			1	μA
			$\overline{\text{EN}} = V_I$				3	
		Regulator 2	$\overline{\text{EN}} = V_I$ ,	T <sub>J</sub> = 25°C			1	μA
			$\overline{\text{EN}} = V_I$				3	
PSRR	Power-supply ripple rejection		f = 1 kHz, C <sub>O</sub> = 33 μF,	T <sub>J</sub> = 25°C <sup>(1)</sup>		60		dB
RESET Terminal								
Minimum input voltage for valid $\overline{\text{RESET}}$			I <sub>RESET</sub> = 300 μA,	V <sub>(RESET)</sub> ≤ 0.8 V		1	1.3	V
Trip threshold voltage			V <sub>O</sub> decreasing		92%	95%	98%	V <sub>OUT</sub>
Hysteresis voltage			Measured at V <sub>O</sub>			0.5%		V <sub>OUT</sub>
$t_{(\overline{\text{RESET}})}$			RESET pulse duration			30	70	ms
$t_r(\overline{\text{RESET}})$			Rising edge deglitch			30		μs
Output low voltage			V <sub>I</sub> = 3.5 V,	I <sub>O(RESET)</sub> = 1 mA		0.15	0.4	V
Leakage current			V <sub>(RESET)</sub> = 6 V				1	μA

(1) Minimum input operating voltage is 2.7 V or  $V_{O(\text{typ})} + 1\text{ V}$ , whichever is greater. Maximum input voltage = 6 V, minimum output current = 1 mA.

(2)  $I_O = 1\text{ mA}$  to 500 mA for Regulator 1 and 1 mA to 250 mA for Regulator 2.

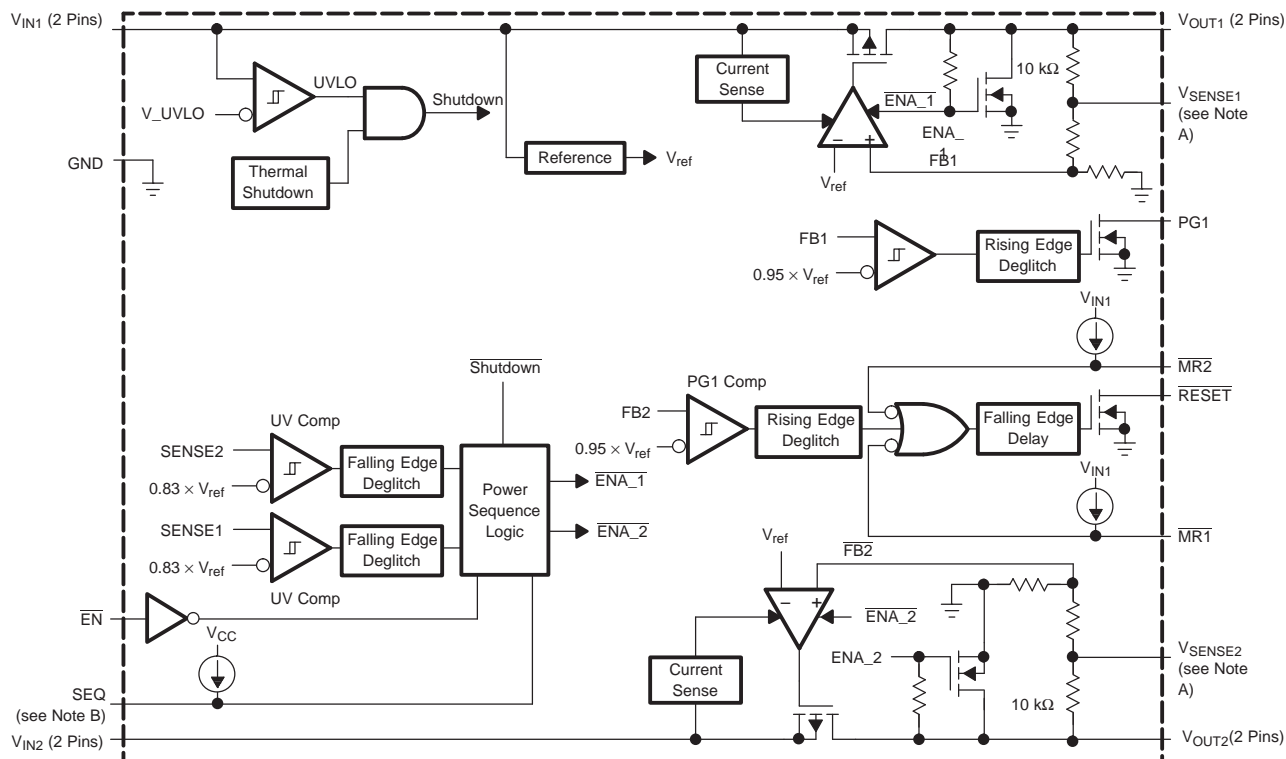
## ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating junction temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN1}$  or  $V_{IN2} = V_{OUT(nom)} + 1\text{ V}$ ,  $I_O = 1\text{ mA}$ ,  $\overline{\text{EN}} = 0$ ,  $C_O = 33\text{ }\mu\text{F}$ , (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>PG1 Terminal</b>					
Minimum input voltage for valid PG1	$I_{(PG1)} = 300\text{ }\mu\text{A}$ , $V_{(PG1)} \leq 0.8\text{ V}$		1	1.3	V
Trip threshold voltage	$V_O$ decreasing	92%	95%	98%	$V_{OUT}$
Hysteresis voltage	Measured at $V_O$		0.5%		$V_{OUT}$
$t_{r(PG1)}$	Rising edge deglitch		30		$\mu\text{s}$
Output low voltage	$V_I = 2.7\text{ V}$ , $I_{O(PG1)} = 1\text{ mA}$		0.15	0.4	V
Leakage current	$V_{(PG1)} = 6\text{ V}$			1	$\mu\text{A}$
<b>EN Terminal</b>					
High level $\overline{\text{EN}}$ input voltage		2			V
Low level $\overline{\text{EN}}$ input voltage				0.7	V
Input current ( $\overline{\text{EN}}$ )		-1		1	$\mu\text{A}$
Falling edge deglitch	Measured at $V_O$		140		$\mu\text{s}$
<b>SEQ Terminal</b>					
High level SEQ input voltage		2			V
Low level SEQ input voltage				0.7	V
Falling edge deglitch	Measured at $V_O$		140		$\mu\text{s}$
SEQ pullup current source			6		$\mu\text{A}$
<b>MR1 / MR2 Terminals</b>					
High level input voltage		2			V
Low level input voltage				0.7	V
Falling edge deglitch	Measured at $V_O$		140		$\mu\text{s}$
Pullup current source			6		$\mu\text{A}$
<b>V<sub>OUT2</sub> Terminal</b>					
$V_{OUT2}$ UV comparator: Positive-going input threshold voltage of $V_{OUT2}$ UV comparator		80% $V_O$	83% $V_O$	86% $V_O$	V
$V_{OUT2}$ UV comparator: Hysteresis			0.5% $V_O$		mV
$V_{OUT2}$ UV comparator: Falling edge deglitch	$V_{SENSE\_2}$ decreasing below threshold		140		$\mu\text{s}$
Peak output current	2-ms pulse width		375		mA
Discharge transistor current	$V_{OUT2} = 1.5\text{ V}$		7.5		mA
<b>V<sub>OUT1</sub> Terminal</b>					
$V_{OUT1}$ UV comparator: Positive-going input threshold voltage of $V_{OUT1}$ UV comparator		80% $V_O$	83% $V_O$	86% $V_O$	V
$V_{OUT1}$ UV comparator: Hysteresis			0.5% $V_O$		mV
$V_{OUT1}$ UV comparator: Falling edge deglitch	$V_{SENSE\_1}$ decreasing below threshold		140		$\mu\text{s}$
Dropout voltage <sup>(3)</sup>	$I_O = 500\text{ mA}$ , $T_J = 25^{\circ}\text{C}$		170		mV
Dropout voltage <sup>(3)</sup>	$I_O = 500\text{ mA}$			275	mV
Peak output current <sup>(3)</sup>	2-ms pulse width		750		mA
Discharge transistor current	$V_{OUT1} = 1.5\text{ V}$		7.5		mA
UVLO threshold		2.4		2.65	V

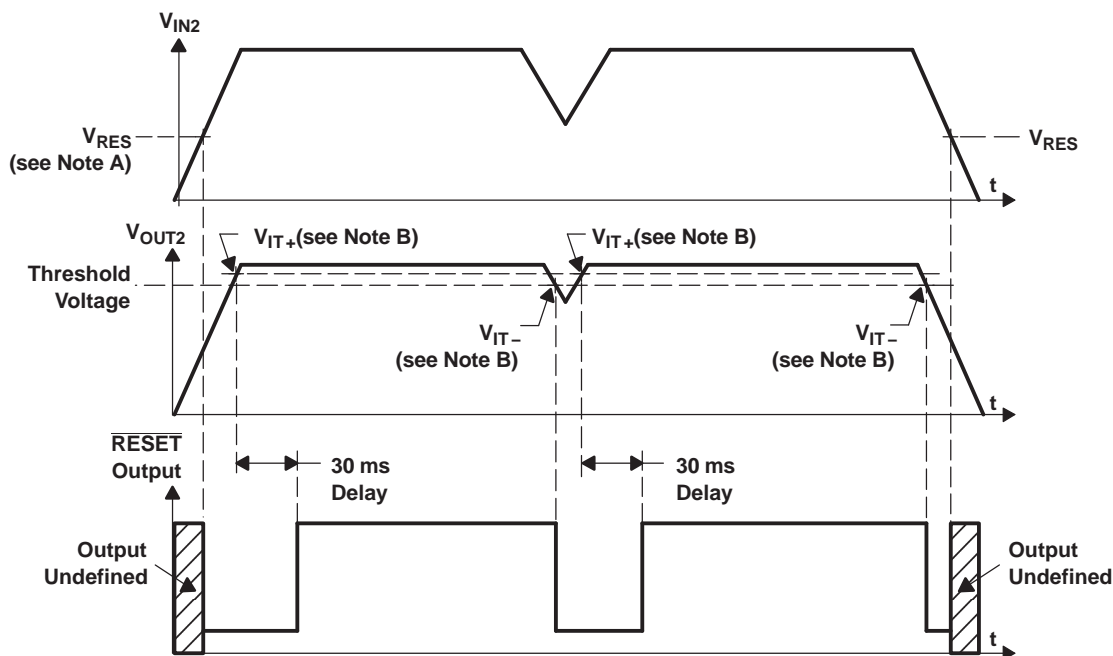
(3) Input voltage ( $V_{IN1}$  or  $V_{IN2}$ ) =  $V_{O(typ)} - 100\text{ mV}$ . For 2.5-V regulators, the dropout voltage is limited by input voltage range.

## DEVICE INFORMATION



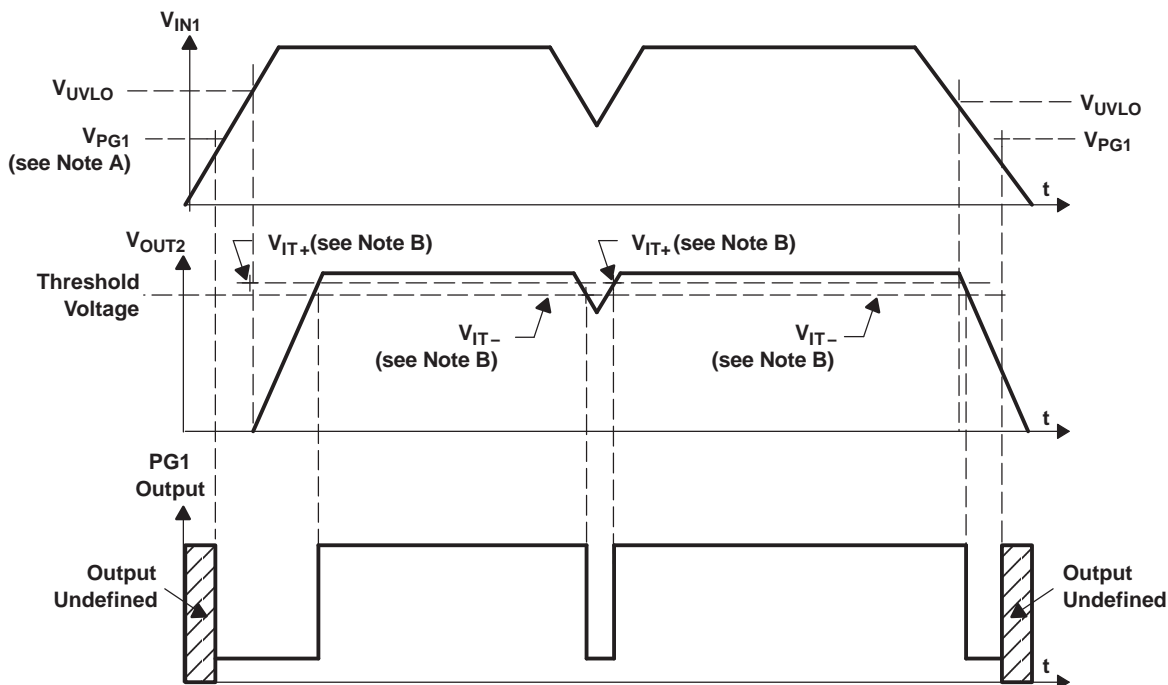
- A. For most applications,  $V_{SENSE1}$  and  $V_{SENSE2}$  should be externally connected to  $V_{OUT}$  as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the *Application Information* section.
- B. If the SEQ terminal is floating at the input,  $V_{OUT2}$  powers up first.

### **$\overline{\text{RESET}}$ Timing Diagram (With $V_{\text{IN1}}$ Powered Up)**



- NOTES: A.  $V_{\text{RES}}$  is the minimum input voltage for a valid  $\overline{\text{RESET}}$ . The symbol  $V_{\text{RES}}$  is not currently listed within EIA or JEDEC standards for semiconductor symbology.
- B.  $V_{\text{IT-}}$  – Trip voltage is typically 5% lower than the output voltage ( $95\%V_{\text{O}}$ )  $V_{\text{IT-}}$  to  $V_{\text{IT+}}$  is the hysteresis voltage.

### **PG1 Timing Diagram**



- NOTES: A.  $V_{\text{PG1}}$  is the minimum input voltage for a valid PG1. The symbol  $V_{\text{PG1}}$  is not currently listed within EIA or JEDEC standards for semiconductor symbology.
- B.  $V_{\text{IT-}}$  – Trip voltage is typically 5% lower than the output voltage ( $95\%V_{\text{O}}$ )  $V_{\text{IT-}}$  to  $V_{\text{IT+}}$  is the hysteresis voltage.

**Table 2. TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{EN}}$	6	I	Active low enable
GND	8	—	Ground
MR1	4	I	Manual reset input 1, active low, pulled up internally
$\overline{\text{MR2}}$	5	I	Manual reset input 2, active low, pulled up internally
NC	1, 11, 20	—	No connection
PG1	16	O	Open drain output, low when $V_{\text{OUT1}}$ voltage is less than 95% of the nominal regulated voltage
RESET	15	O	Open drain output, SVS (power-on reset) signal, active low
SEQ	7	I	Power-up sequence control: SEQ = High, $V_{\text{OUT2}}$ powers up first; SEQ = Low, $V_{\text{OUT1}}$ powers up first, SEQ terminal pulled up internally.
$V_{\text{IN1}}$	2, 3	I	Input voltage of regulator 1
$V_{\text{IN2}}$	9, 10	I	Input voltage of regulator 2
$V_{\text{OUT1}}$	18, 19	O	Output voltage of regulator 1
$V_{\text{OUT2}}$	12, 13	O	Output voltage of regulator 2
$V_{\text{SENSE2}}/\text{FB2}$	14	I	Regulator 2 output voltage sense
$V_{\text{SENSE1}}/\text{FB1}$	17	I	Regulator 1 output voltage sense

## Detailed Description

The TPS70175 low dropout regulator provides dual regulated output voltages for DSP applications which require high performance power management solutions. These devices provide fast transient response and high accuracy with small output capacitors, while drawing low quiescent current. Programmable sequencing provides a power solution for DSPs without any external component requirements. This reduces the component cost and board space while increasing total system reliability. The TPS70175 has an enable feature which puts the device in sleep mode reducing the input currents to less than 3  $\mu\text{A}$ . Other features are integrated SVS (power-on reset, RESET) and power good (PG1) that monitor output voltages and provide logic output to the system. These differentiated features provide a complete DSP power solution.

The TPS70175, unlike many other LDOs, feature low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ( $I_B = I_C/\beta$ ). The TPS70175 uses a PMOS transistor to pass current; because the gate of the PMOS is voltage = driven, operating current is low and stable over the full load range.

## Pin Functions

### Enable

The  $\overline{\text{EN}}$  terminal is an input which enables or shuts down the device. If  $\overline{\text{EN}}$  is at a voltage high signal, the device is in shutdown mode. When  $\overline{\text{EN}}$  goes to voltage low, the device is enabled.

### Sequence

The SEQ terminal is an input that programs which output voltage ( $V_{\text{OUT1}}$  or  $V_{\text{OUT2}}$ ) is turned on first. When the device is enabled and the SEQ terminal is pulled high or left open,  $V_{\text{OUT2}}$  turns on first and  $V_{\text{OUT1}}$  remains off until  $V_{\text{OUT2}}$  reaches approximately 83% of its regulated output voltage. At that time,  $V_{\text{OUT1}}$  is turned on. If  $V_{\text{OUT2}}$  is pulled below 83% (for example, an overload condition)  $V_{\text{OUT1}}$  is turned off. These terminals have a 6- $\mu\text{A}$  pullup current to  $V_{\text{IN1}}$ .

Pulling the SEQ terminal low reverses the power-up order and  $V_{\text{OUT1}}$  is turned on first. For detailed timing diagrams, see [Figure 26](#) through [Figure 30](#).

## Power-Good

The PG1 is an open drain, active high output terminal which indicates the status of the  $V_{OUT1}$  regulator. When the  $V_{OUT1}$  reaches 95% of its regulated voltage, PG1 goes to a high impedance state. It goes to a low impedance state when it is pulled below 95% (for example, an overload condition) of its regulated voltage. The open drain output of the PG1 terminal requires a pullup resistor.

## Manual Reset Pins ( $\overline{MR1}$ and $\overline{MR2}$ )

$\overline{MR1}$  and  $\overline{MR2}$  are active low input terminals used to trigger a reset condition. When either  $\overline{MR1}$  or  $\overline{MR2}$  is pulled to logic low, a POR (RESET) occurs. These terminals have a 6- $\mu$ A pullup current to  $V_{IN1}$ .

## Sense ( $V_{SENSE1}$ , $V_{SENSE2}$ )

The sense terminals of fixed-output options must be connected to the regulator output and the connection should be as short as possible. Internally, sense connects to high-impedance wide-bandwidth amplifiers through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the sense connection in such a way to minimize/avoid noise pickup. Adding RC networks between the  $V_{SENSE}$  terminals and  $V_{OUT}$  terminals to filter noise is not recommended because it can cause the regulators to oscillate.

## RESET Indicator

The TPS70175 features a  $\overline{RESET}$  (SVS, POR, or power-on reset).  $\overline{RESET}$  can be used to drive power-on reset circuitry or a low-battery indicator.  $\overline{RESET}$  is an active low, open drain output which indicates the status of the  $V_{OUT2}$  regulator and both manual reset pins ( $\overline{MR1}$  and  $\overline{MR2}$ ). When  $V_{OUT2}$  exceeds 95% of its regulated voltage and  $\overline{MR1}$  and  $\overline{MR2}$  are in the high impedance state,  $\overline{RESET}$  will go to a high-impedance state after 30-ms delay.  $\overline{RESET}$  will go to a low-impedance state when  $V_{OUT2}$  is pulled below 95% (for example, an overload condition) of its regulated voltage. To monitor  $V_{OUT1}$ , the PG1 output pin can be connected to  $\overline{MR1}$  or  $\overline{MR2}$ . The open drain output of the  $\overline{RESET}$  terminal requires a pullup resistor. If  $\overline{RESET}$  is not used, it can be left floating.

## $V_{IN1}$ and $V_{IN2}$

$V_{IN1}$  and  $V_{IN2}$  are input to the regulators. Internal bias voltages are powered by  $V_{IN1}$ .

## $V_{OUT1}$ and $V_{OUT2}$

$V_{OUT1}$  and  $V_{OUT2}$  are output terminals of the LDO.

## TYPICAL CHARACTERISTICS

**Table 3. Table of Graphs**

			FIGURE
$V_O$	Output voltage	vs Output current	1, 2
		vs Temperature	3, 4
	Ground current	vs Junction temperature	5
PSSR	Power-supply rejection ratio	vs Frequency	6–9
$Z_O$	Output impedance	vs Frequency	10–13
	Dropout voltage	vs Temperature	14
	Load transient response		15, 16
	Equivalent series resistance	vs Output current	17–24
	Test circuit for typical regions of stability performance		25

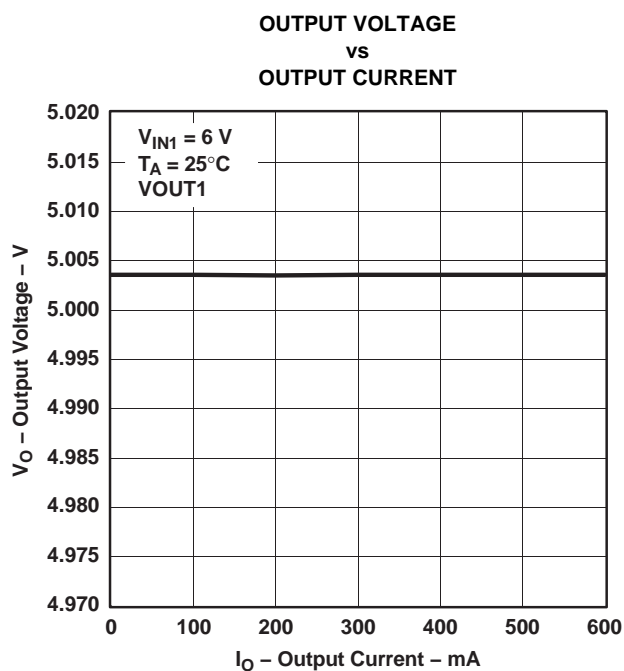


Figure 1.

G001

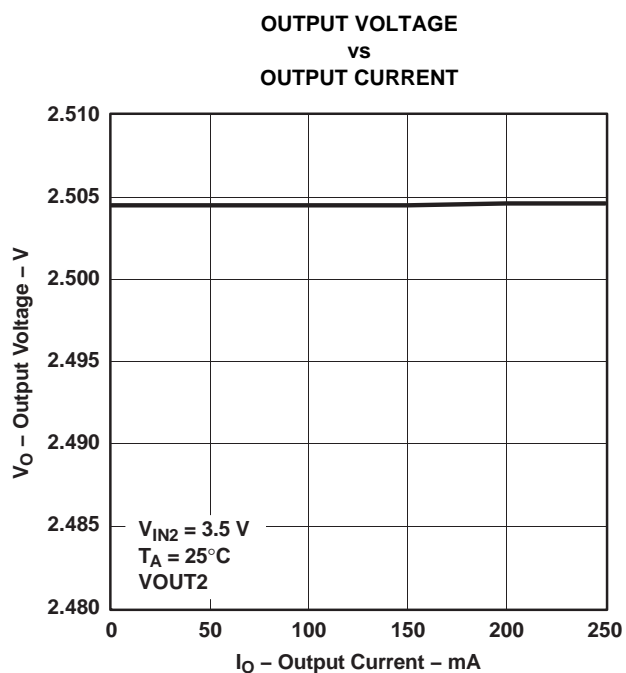


Figure 2.

G002

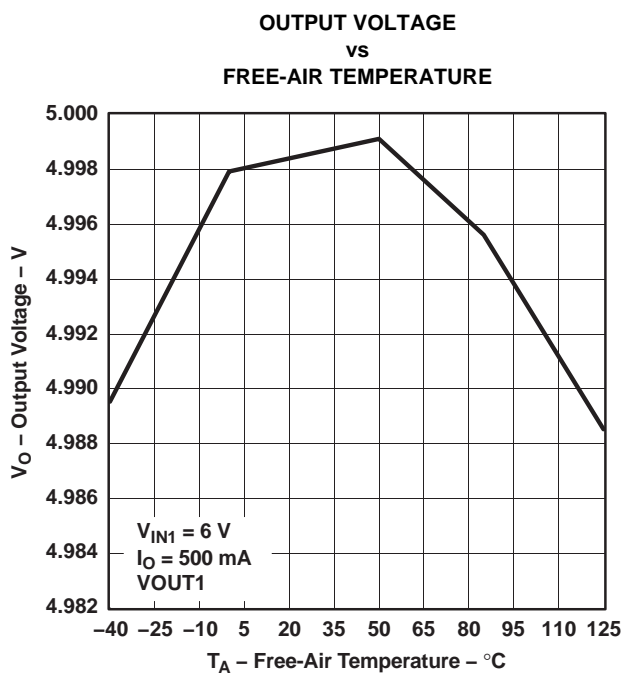


Figure 3.

G003

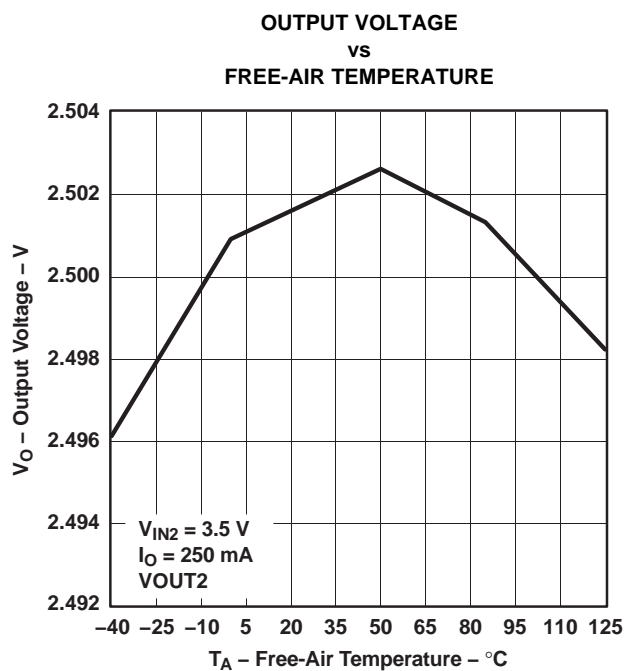


Figure 4.

G004

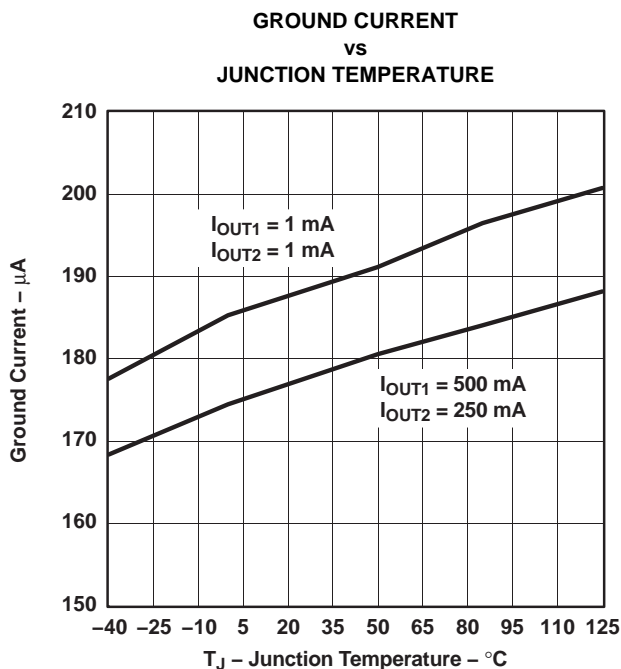


Figure 5.

G005

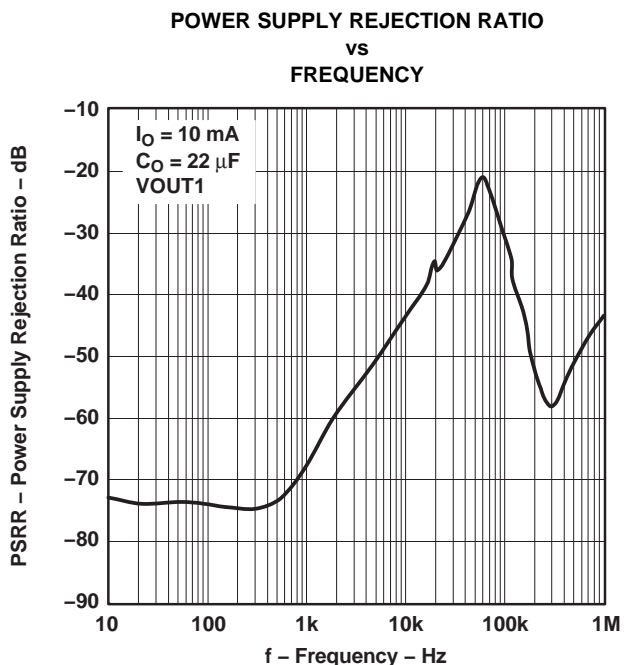


Figure 6.

G006

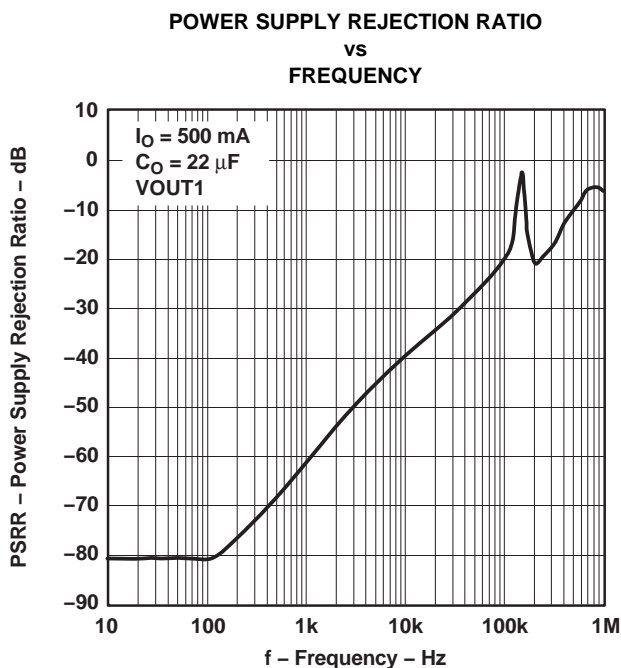


Figure 7.

G007

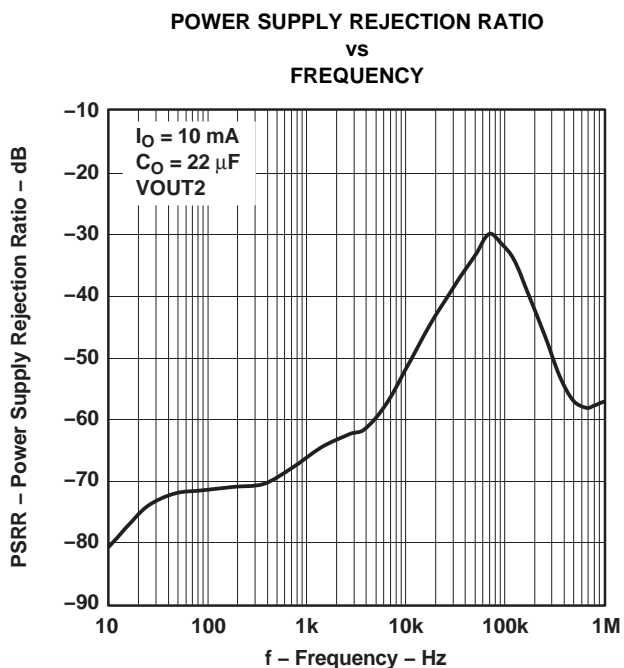


Figure 8.

G008

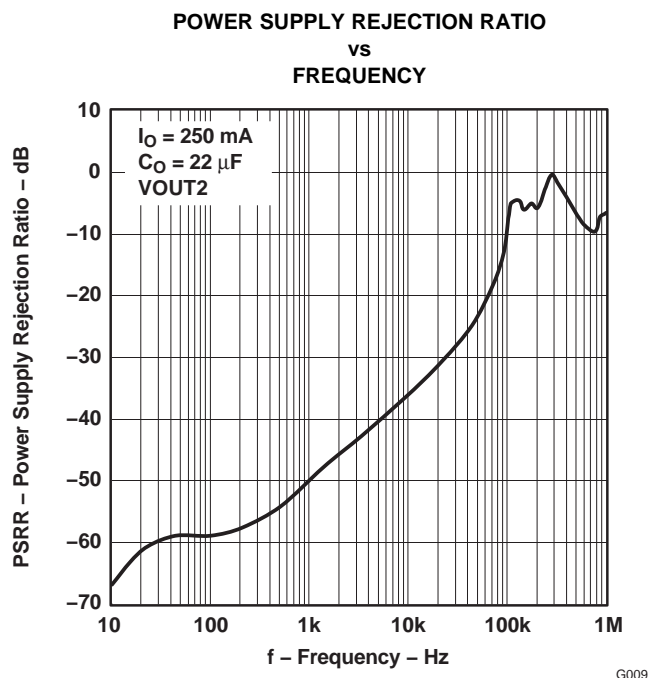


Figure 9.

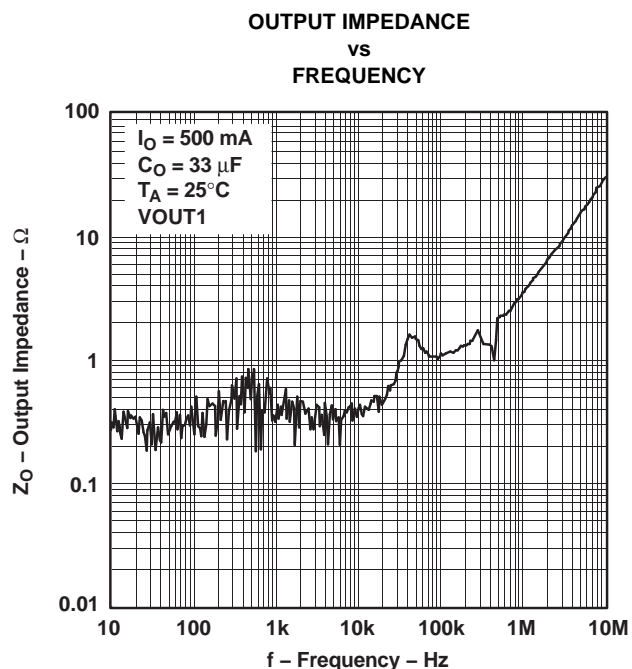


Figure 10.

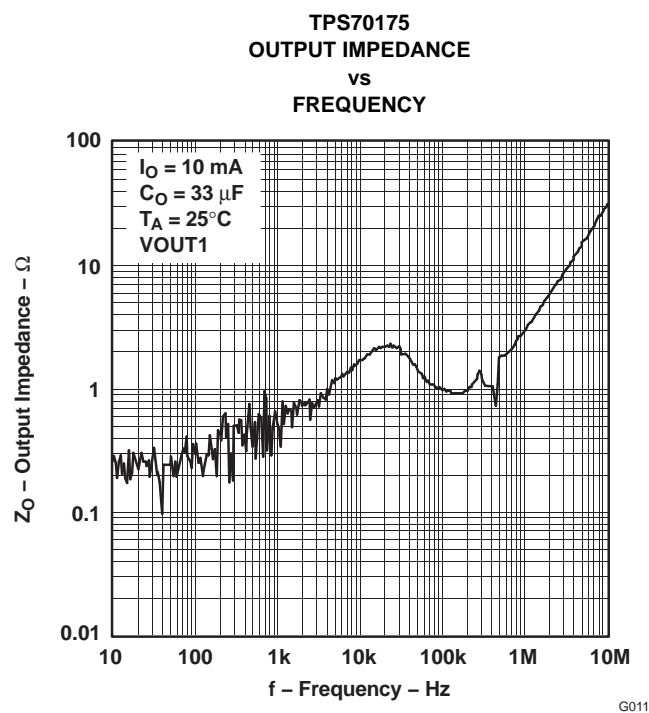


Figure 11.

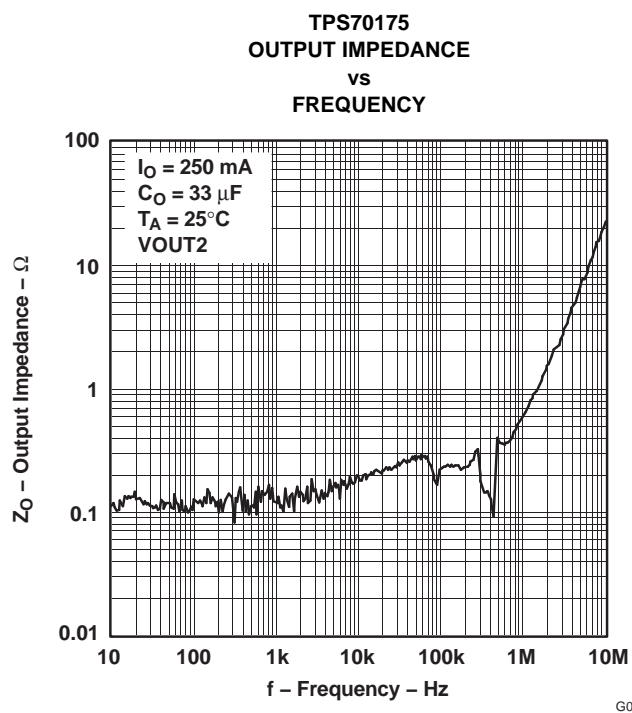


Figure 12.

TPS70175  
OUTPUT IMPEDANCE  
VS  
FREQUENCY

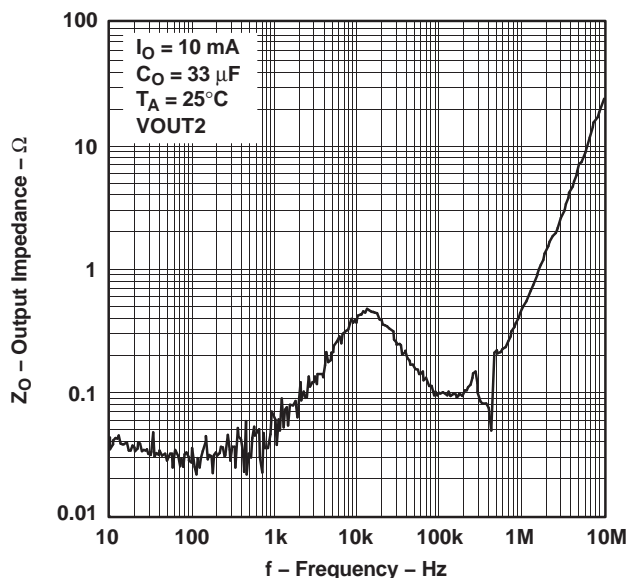


Figure 13.

G013

DROPOUT VOLTAGE  
VS  
FREE-AIR TEMPERATURE

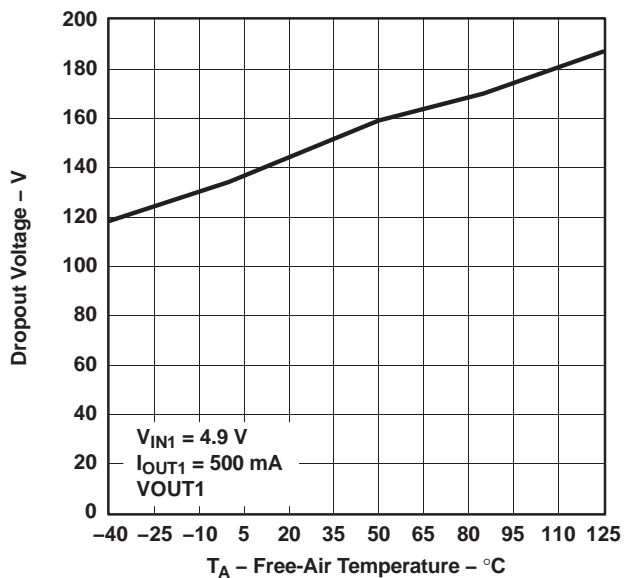


Figure 14.

G014

LOAD TRANSIENT RESPONSE

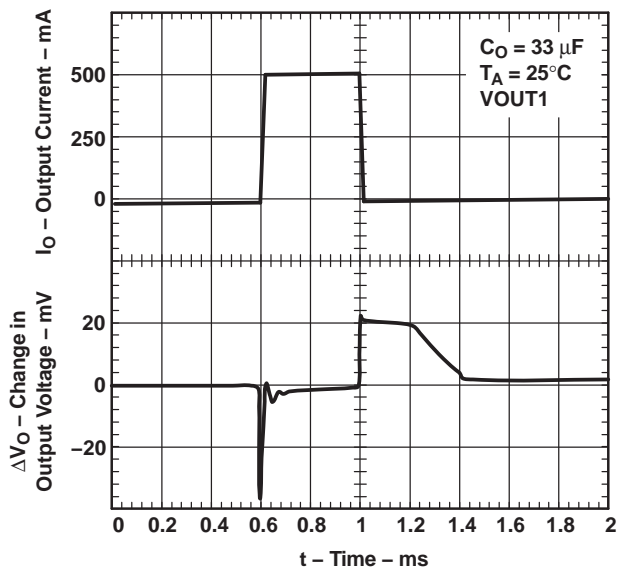


Figure 15.

G015

LOAD TRANSIENT RESPONSE

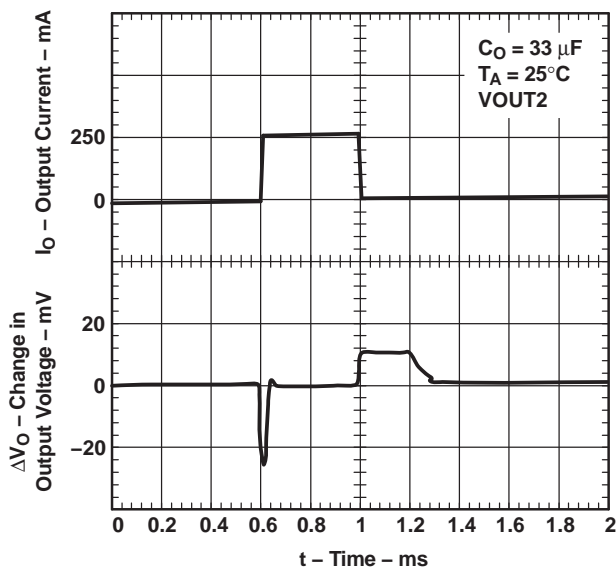


Figure 16.

G016

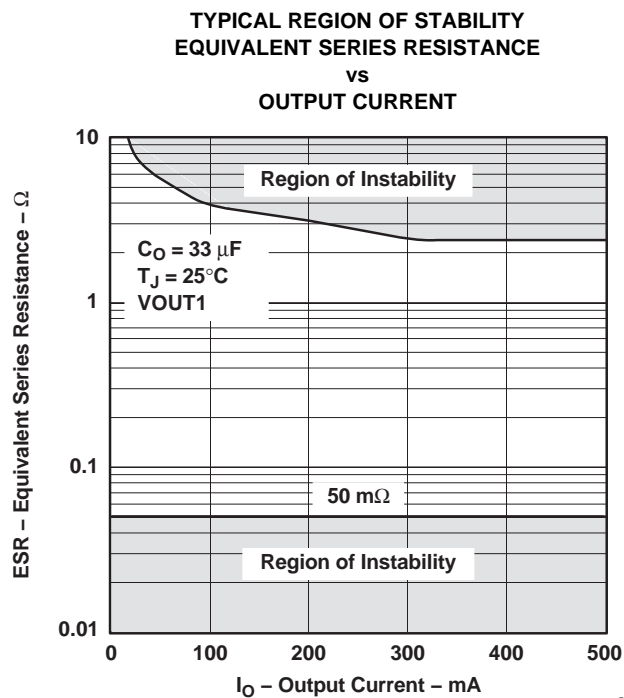


Figure 17.

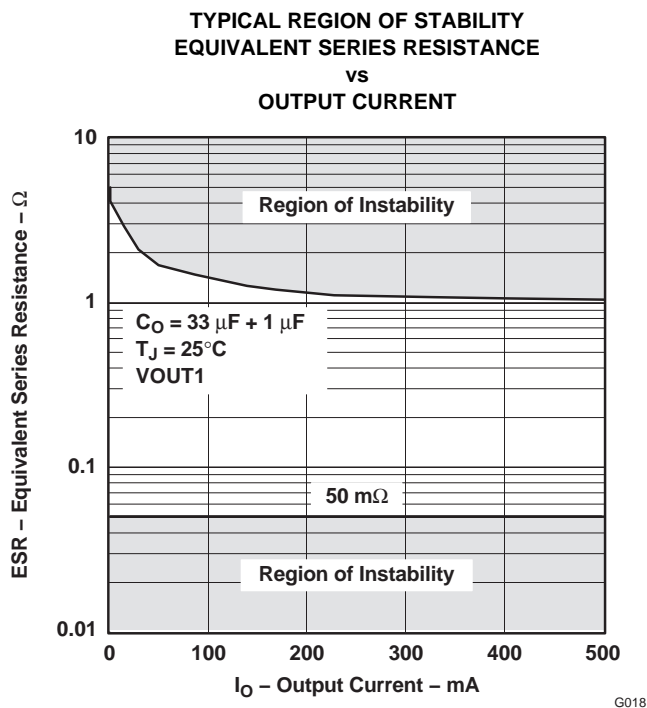


Figure 18.

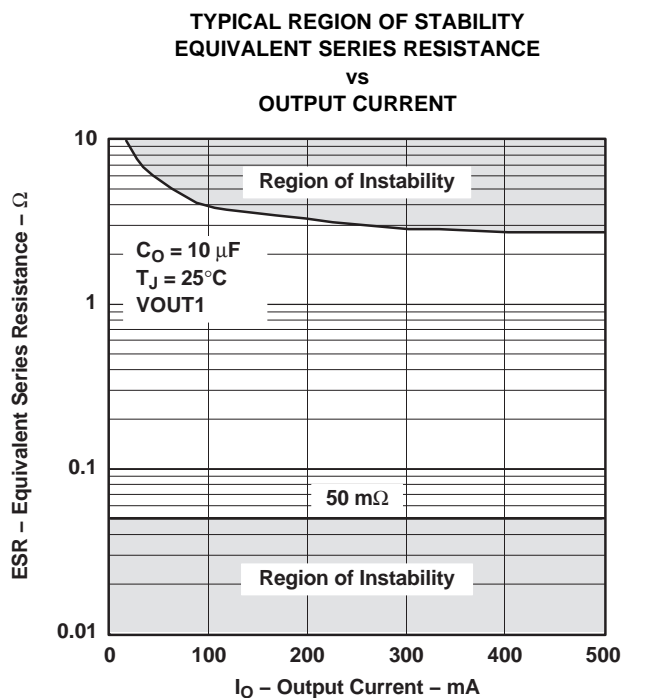


Figure 19.

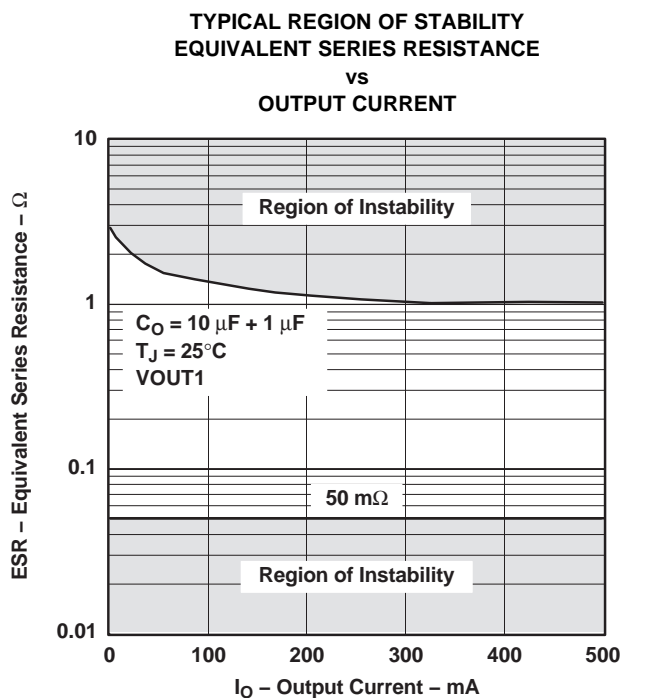


Figure 20.

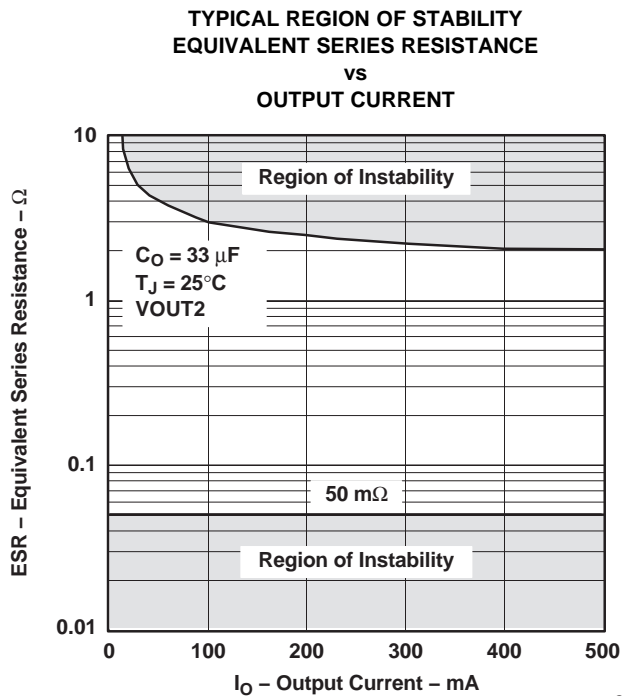


Figure 21.

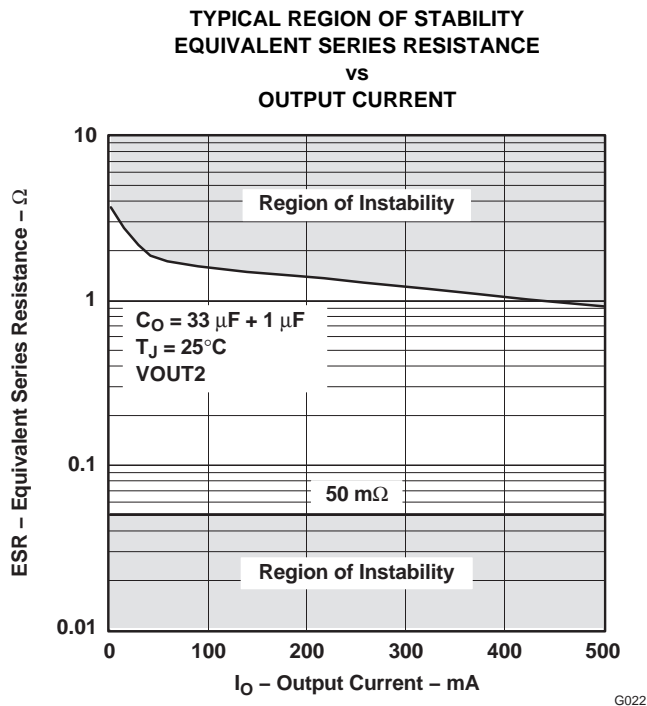


Figure 22.

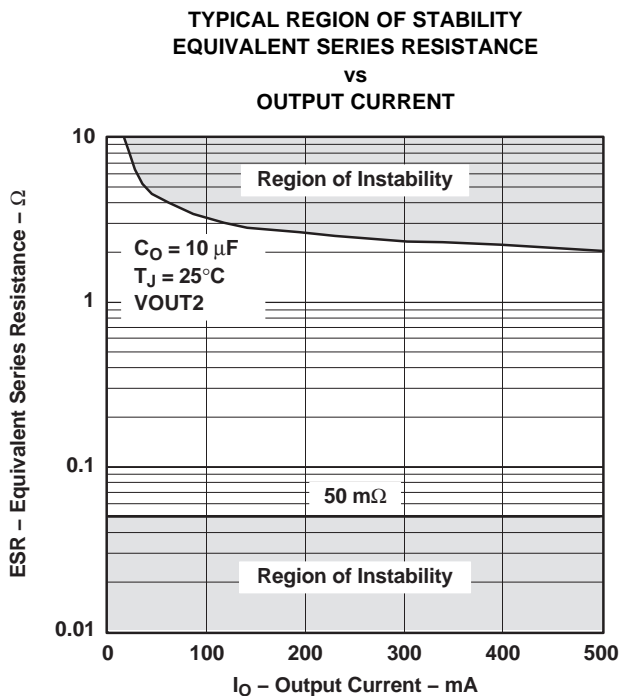


Figure 23.

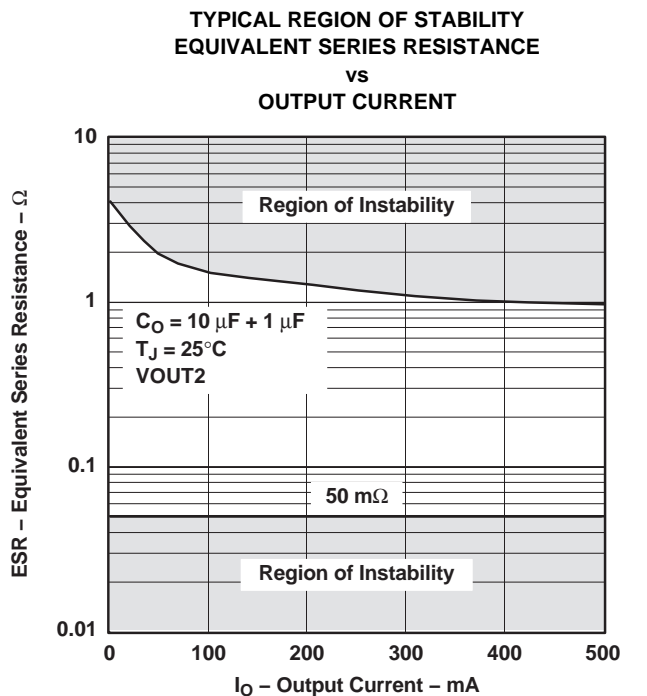


Figure 24.

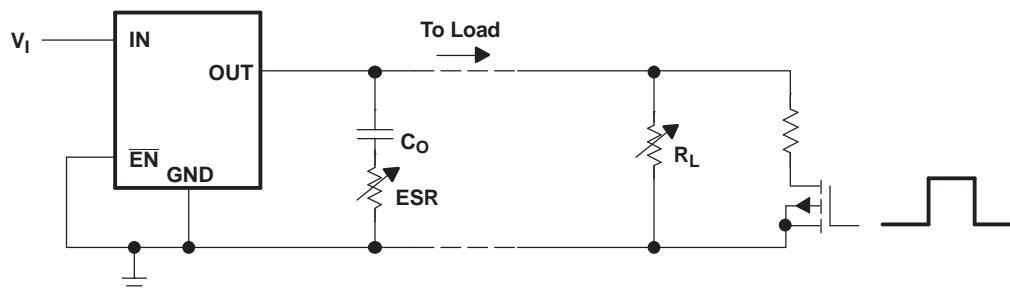


Figure 25. Test Circuit for Typical Regions of Stability

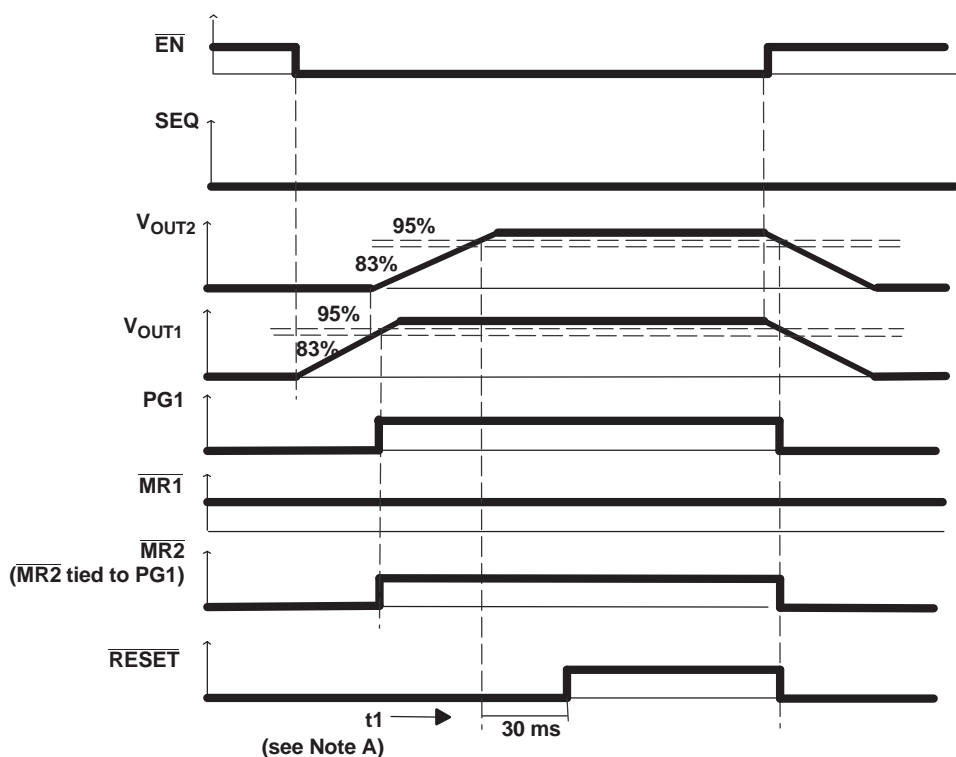
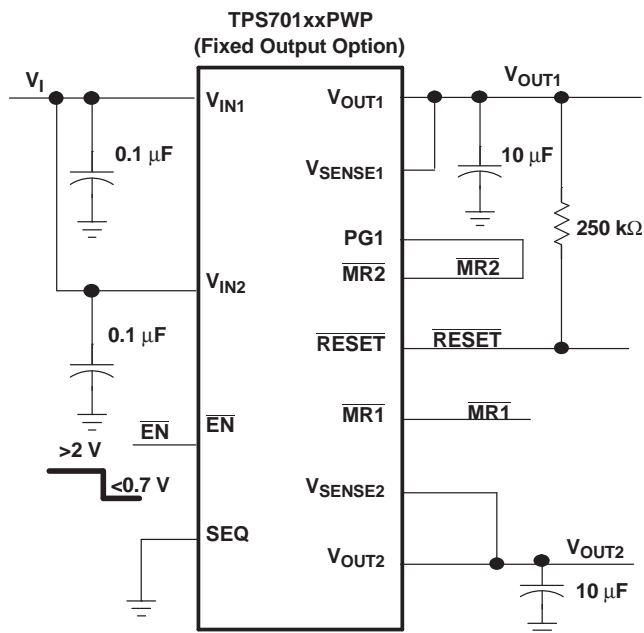
## APPLICATION INFORMATION

### Sequencing Timing Diagrams

This section provides a number of timing diagrams showing how this device functions in different configurations.

Application condition:  $\overline{\text{MR2}}$  is tied to PG1,  $V_{\text{IN1}}$  and  $V_{\text{IN2}}$  are tied to the same input voltage, the SEQ pin is tied to logic low and the device is toggled with the enable ( $\overline{\text{EN}}$ ) function.

When the device is enabled ( $\overline{\text{EN}}$  is pulled low),  $V_{\text{OUT1}}$  turns on first and  $V_{\text{OUT2}}$  remains off until  $V_{\text{OUT1}}$  reaches approximately 83% of its regulated output voltage. At that time,  $V_{\text{OUT2}}$  is turned on. When  $V_{\text{OUT1}}$  reaches 95% of its regulated output, PG1 turns on (active high). Since  $\overline{\text{MR2}}$  is connected to PG1 for this application, it follows PG1. When  $V_{\text{OUT2}}$  reaches 95% of its regulated voltage,  $\overline{\text{RESET}}$  switches to high voltage level after a 30-ms delay (see Figure 26).

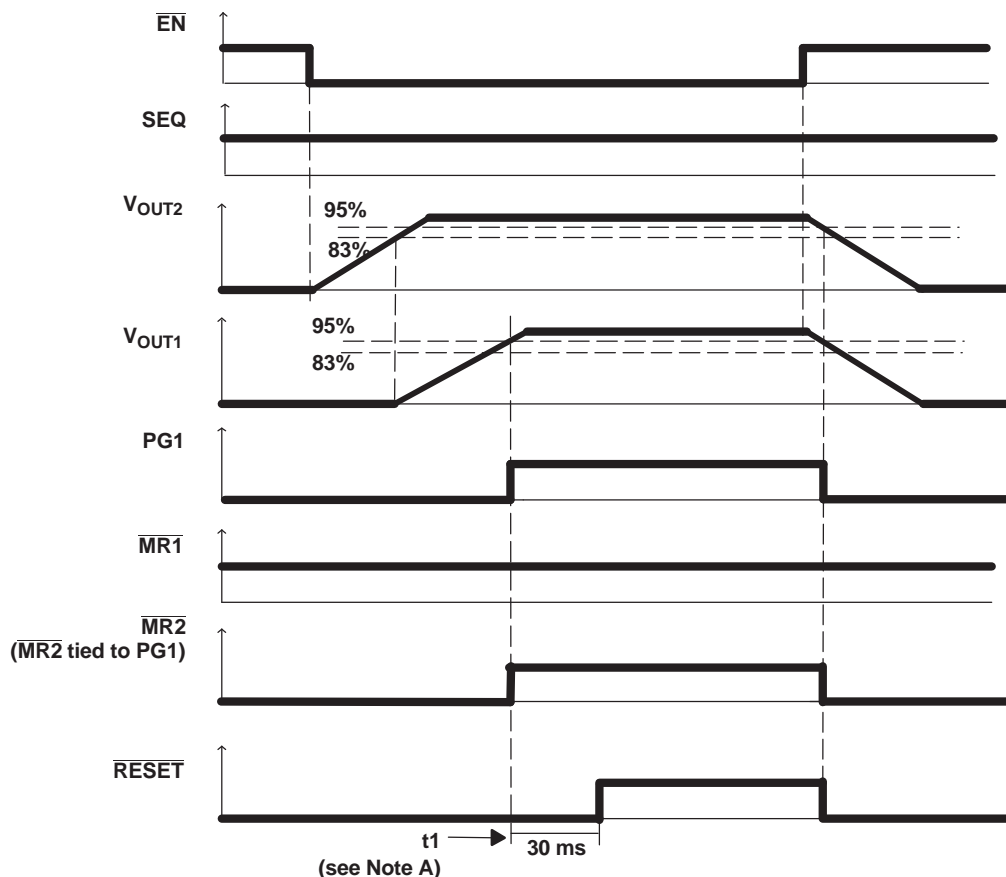
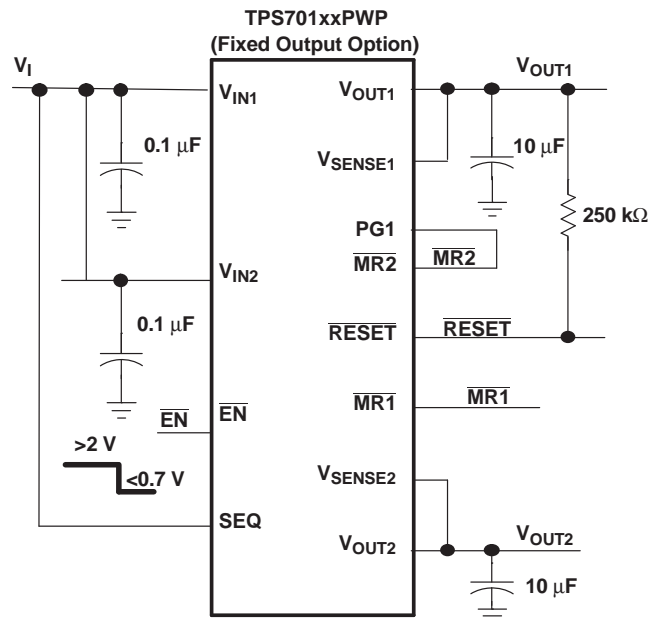


NOTE A:  $t_1$  – Time at which both  $V_{\text{OUT1}}$  and  $V_{\text{OUT2}}$  are greater than the PG1 thresholds and  $\overline{\text{MR1}}$  is logic high.

Figure 26. Timing When  $\text{SEQ} = \text{Low}$

Application condition:  $\overline{\text{MR2}}$  is tied to PG1,  $V_{\text{IN1}}$  and  $V_{\text{IN2}}$  are tied to the same input voltage, the SEQ pin is tied to logic high and the device is toggled with the enable ( $\overline{\text{EN}}$ ) function.

When the device is enabled ( $\overline{\text{EN}}$  is pulled low),  $V_{\text{OUT2}}$  begins to power up. When it reaches 83% of its regulated voltage,  $V_{\text{OUT1}}$  begins to power up. PG1 turns on when  $V_{\text{OUT1}}$  reaches 95% of its regulated voltage and since  $\overline{\text{MR2}}$  and PG1 are tied together,  $\overline{\text{MR2}}$  follows PG1. When  $V_{\text{OUT1}}$  reaches 95% of its regulated voltage, RESET switches to high voltage level after a 30-ms delay (see Figure 27).

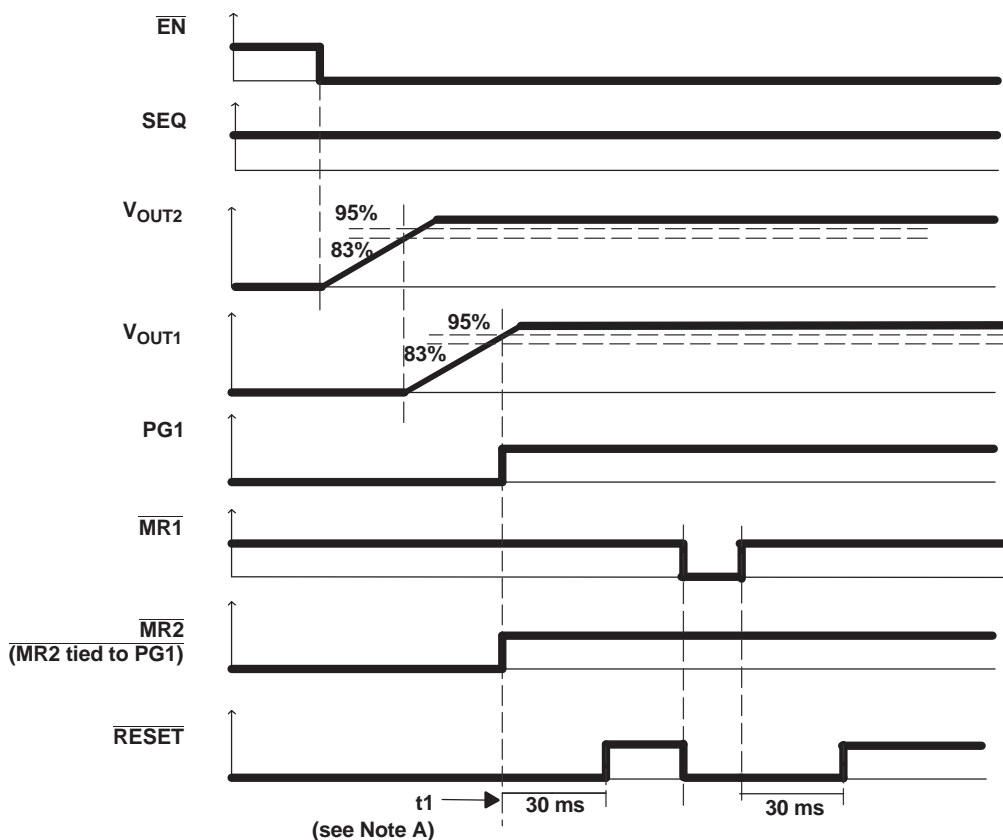
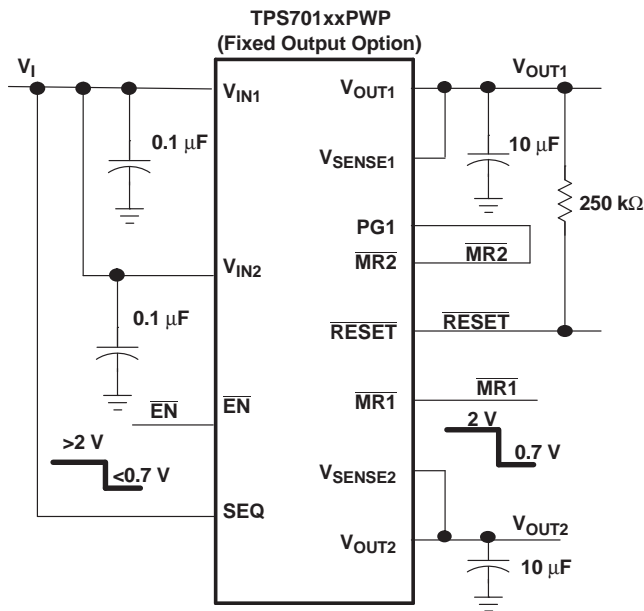


NOTE A:  $t_1$  – Time at which both  $V_{\text{OUT1}}$  and  $V_{\text{OUT2}}$  are greater than the PG1 thresholds and  $\overline{\text{MR1}}$  is logic high.

**Figure 27. Timing When SEQ = High**

Application condition:  $\overline{\text{MR2}}$  is tied to PG1,  $V_{\text{IN1}}$  and  $V_{\text{IN2}}$  are tied to the same input voltage, the SEQ pin is tied to logic high and MR1 is toggled.

When the device is enabled ( $\overline{\text{EN}}$  is pulled low),  $V_{\text{OUT2}}$  begins to power up. When it reaches 83% of its regulated voltage,  $V_{\text{OUT1}}$  begins to power up. PG1 turns on when  $V_{\text{OUT1}}$  reaches to 95% of its regulated voltage and since MR2 and PG1 are tied together, MR2 follows PG1. When  $V_{\text{OUT1}}$  reaches 95% of its regulated voltage, the RESET switches to high a voltage level after a 30-ms delay. When MR1 is pulled low, it causes RESET to go low, but the regulators remains in regulation (see Figure 28).

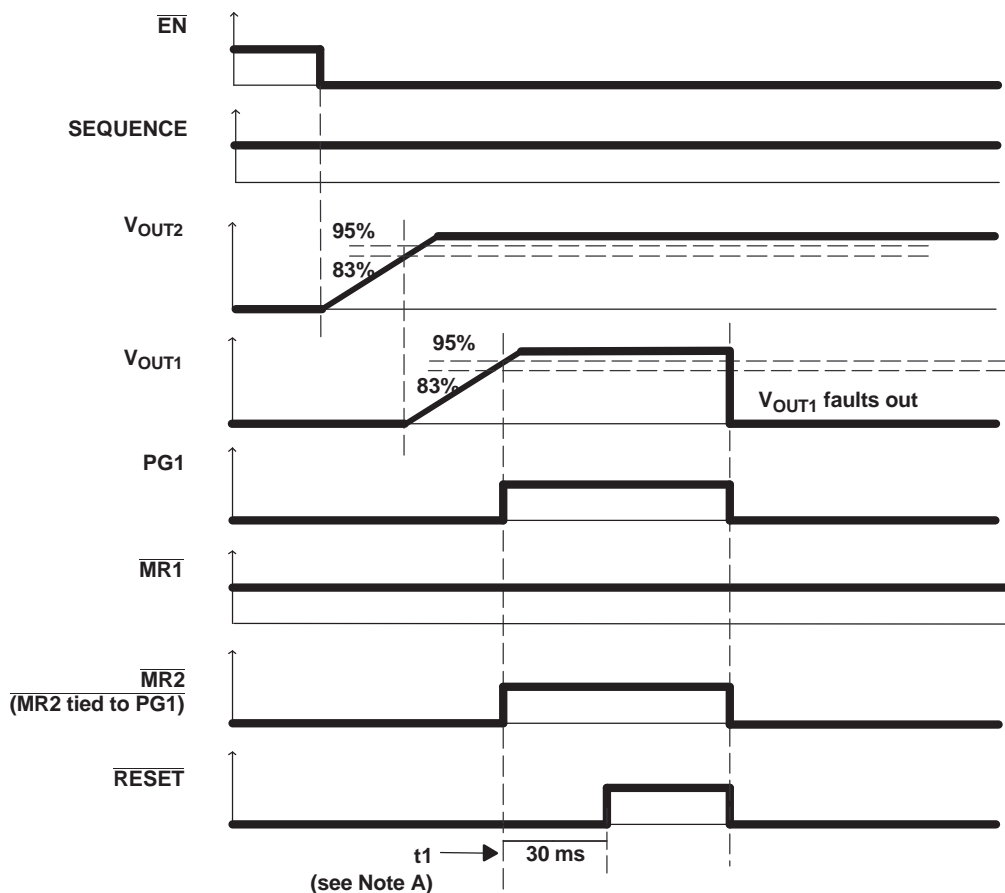
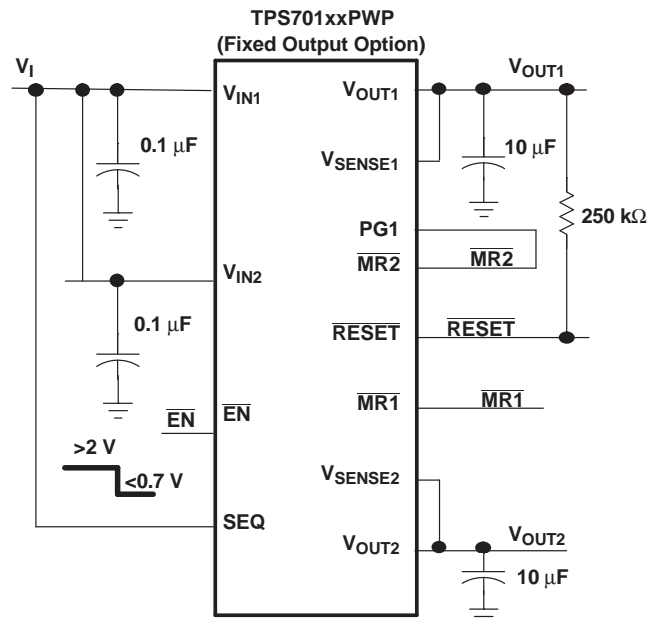


NOTE A:  $t_1$  – Time at which both  $V_{\text{OUT1}}$  and  $V_{\text{OUT2}}$  are greater than the PG1 thresholds and  $\overline{\text{MR1}}$  is logic high.

Figure 28. Timing When  $\overline{\text{MR1}}$  is Toggled

Application condition:  $\overline{\text{MR2}}$  is tied to PG1,  $V_{\text{IN1}}$  and  $V_{\text{IN2}}$  are tied to the same input voltage, the SEQ pin is tied to logic high and  $V_{\text{OUT1}}$  faults out.

$V_{\text{OUT2}}$  begins to power up when the device is enabled ( $\overline{\text{EN}}$  is pulled low). When  $V_{\text{OUT2}}$  reaches 83% of its regulated voltage, then  $V_{\text{OUT1}}$  begins to power up. When  $V_{\text{OUT1}}$  reaches 95% of its regulated voltage, PG1 turns on and  $\overline{\text{RESET}}$  switches to high voltage level after a 30-ms delay. When  $V_{\text{OUT1}}$  faults out,  $V_{\text{OUT2}}$  remains powered on because the SEQ pin is high. PG1 is tied to  $\overline{\text{MR2}}$  and both change state to logic low.  $\overline{\text{RESET}}$  is driven by  $\overline{\text{MR2}}$  and goes to logic low when  $V_{\text{OUT1}}$  faults out (see Figure 29).

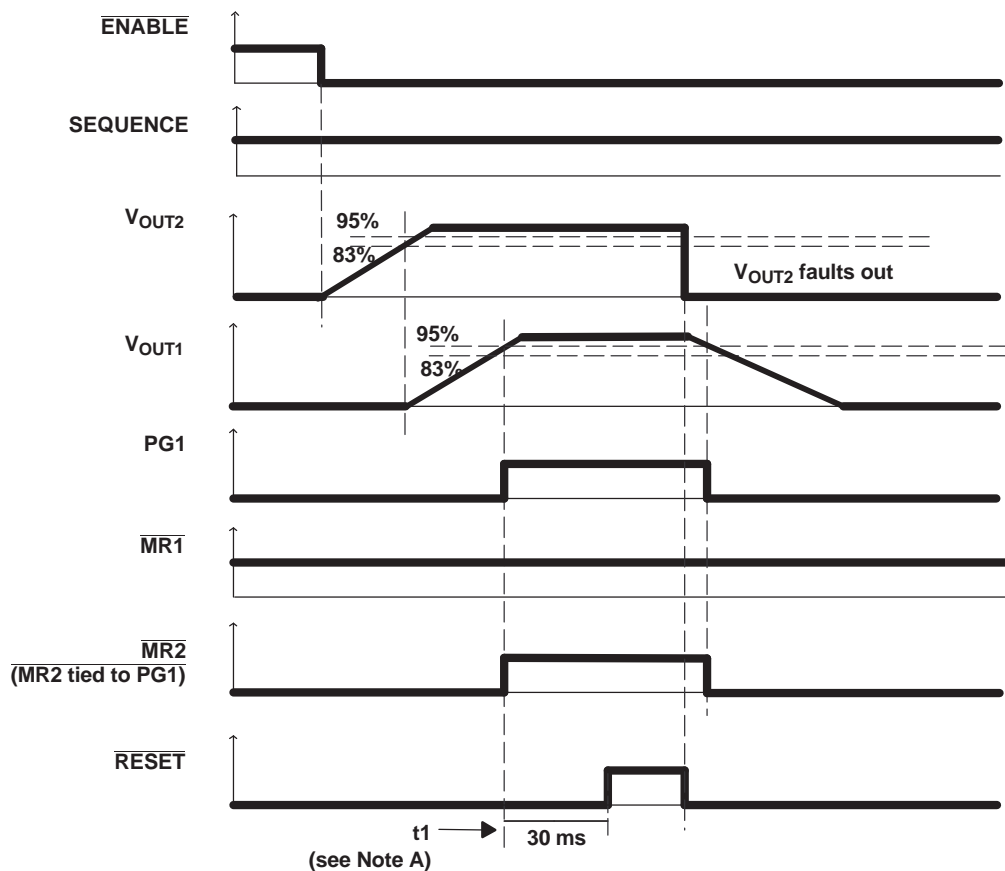
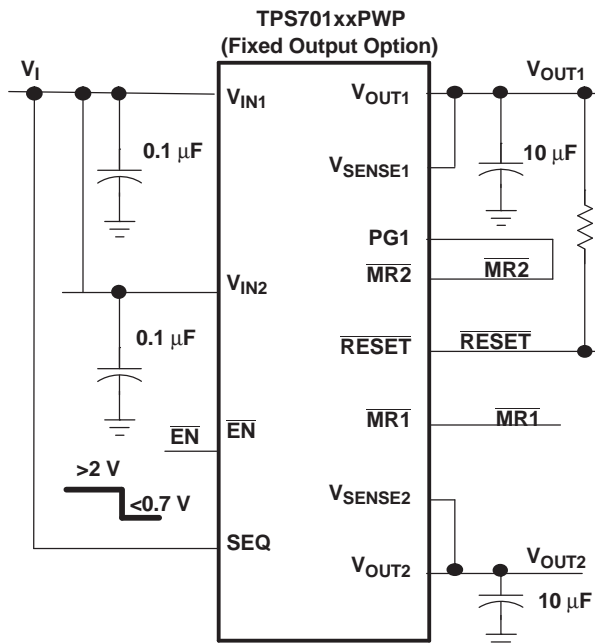


NOTE A:  $t_1$  – Time at which both  $V_{\text{OUT1}}$  and  $V_{\text{OUT2}}$  are greater than the PG1 thresholds and  $\overline{\text{MR1}}$  is logic high.

**Figure 29. Timing When  $V_{\text{OUT1}}$  Faults Out**

Application condition:  $\overline{\text{MR2}}$  is tied to PG1,  $V_{\text{IN1}}$  and  $V_{\text{IN2}}$  are tied to same input voltage, the SEQ is tied to logic high, the device is enabled, and  $V_{\text{OUT2}}$  faults out.

$V_{\text{OUT2}}$  begins to power up when the device is enabled (EN is pulled low). When  $V_{\text{OUT2}}$  reaches 83% of its regulated voltage,  $V_{\text{OUT1}}$  begins to power up. When  $V_{\text{OUT1}}$  reaches 95% of its regulated voltage, PG1 turns on and RESET switches to high voltage level after a 30-ms delay. When  $V_{\text{OUT2}}$  faults out,  $V_{\text{OUT1}}$  is powered down because SEQ is high. PG1 is tied to  $\overline{\text{MR2}}$  and both change state to logic low. RESET goes low when  $V_{\text{OUT2}}$  faults out (see Figure 30).

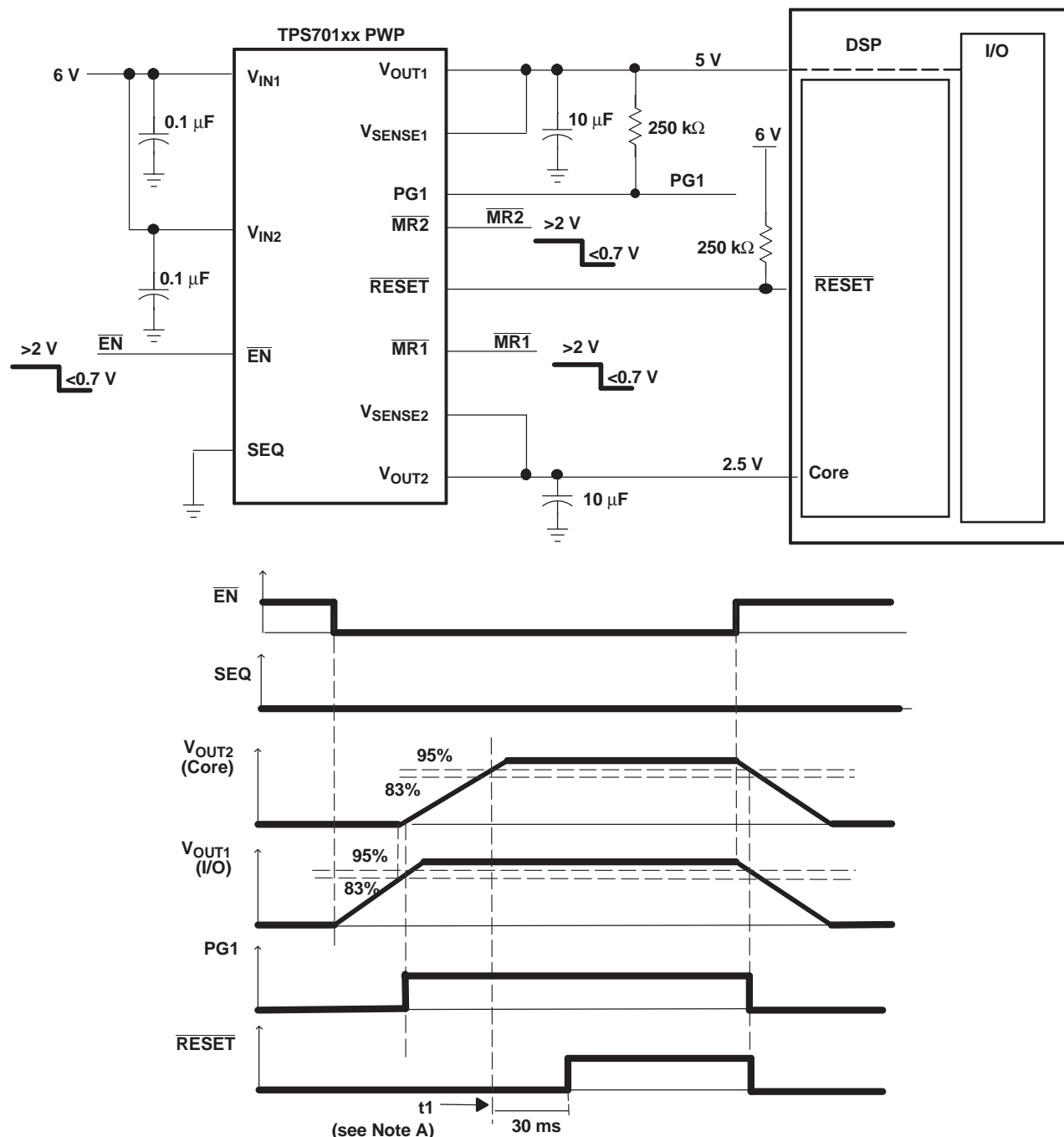


NOTE A:  $t_1$  – Time at which both  $V_{\text{OUT1}}$  and  $V_{\text{OUT2}}$  are greater than the PG1 thresholds and  $\overline{\text{MR1}}$  is logic high.

Figure 30. Timing When  $V_{\text{OUT2}}$  Faults Out

## Split Voltage DSP Application

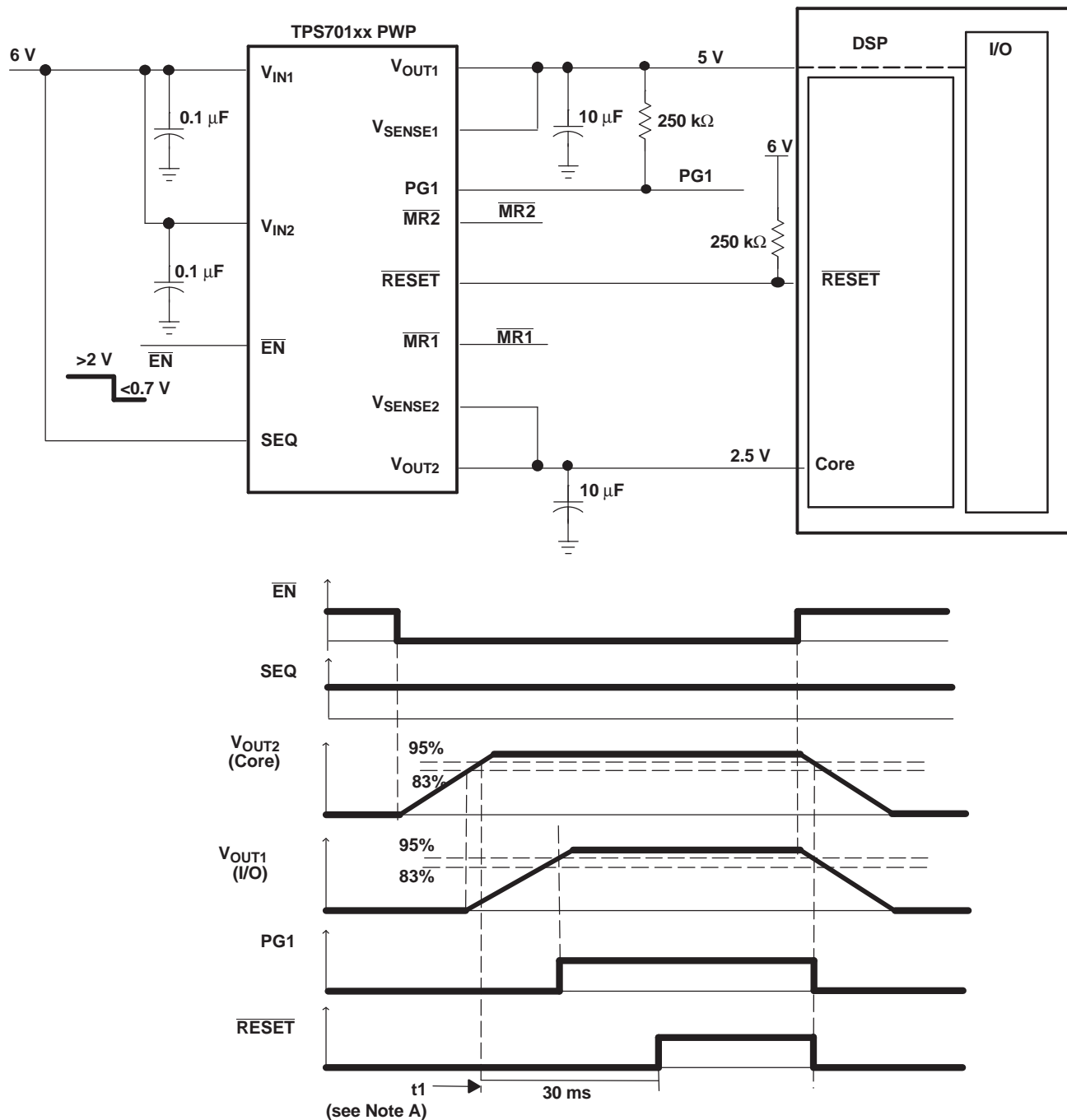
Figure 31 shows a typical application where the TPS701xx is powering up a DSP. In this application, by grounding the SEQ pin,  $V_{OUT1}$  (I/O) is powered up first and then  $V_{OUT2}$  (core).



NOTE A:  $t_1$  – Time at which both  $V_{OUT1}$  and  $V_{OUT2}$  are greater than the PG1 thresholds and  $\overline{MR1}$  is logic high.

**Figure 31. Application Timing Diagram (SEQ = Low)**

Figure 32 shows a typical application where the TPS701xx is powering up a DSP. In this application, by pulling up the SEQ pin,  $V_{OUT2}$  (core) is powered up first and then  $V_{OUT1}$  (I/O).



NOTE A:  $t_1$  – Time at which both  $V_{OUT1}$  and  $V_{OUT2}$  are greater than the PG1 thresholds and  $\overline{MR1}$  is logic high.

Figure 32. Application Timing Diagram (SEQ = High)

### Input Capacitor

For a typical application, an input bypass capacitor (0.1  $\mu\text{F}$  – 1  $\mu\text{F}$ ) is recommended. This capacitor filters any high frequency noise generated in the line. For fast transient condition where droop at the input of the LDO may occur due to high inrush current, it is recommended to place a larger capacitor at the input as well. The size of this capacitor is dependent on the output current and response time of the main power supply, as well as the distance to the  $V_I$  pins of the LDO.

## Output Capacitor

As with most LDO regulators, the TPS70175 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10  $\mu\text{F}$  and the ESR (equivalent series resistance) must be between 50 m $\Omega$  and 2.5  $\Omega$ . Capacitor values 10  $\mu\text{F}$  or larger are acceptable, provided the ESR is less than 2.5  $\Omega$ . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Larger capacitors provide a wider range of stability and better load transient response. [Table 4](#) provides a partial listing of surface-mount capacitors usable with the TPS70175 for fast transient response application.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

**Table 4. Partial Listing of TPS70175-Compatible Surface-Mount Capacitors**

VALUE	MANUFACTURER	MAXIMUM ESR	MFR PART NO.
22 $\mu\text{F}$	Kemet	345m $\Omega$	7495C226K0010AS
33 $\mu\text{F}$	Sanyo	100m $\Omega$	10TPA33M
47 $\mu\text{F}$	Sanyo	100m $\Omega$	6TPA47M
68 $\mu\text{F}$	Sanyo	45m $\Omega$	10TPC68M

## ESR and Transient Response

LDOs typically require an external output capacitor for stability. In fast transient response applications, capacitors are used to support the load current while the LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

Besides its capacitance, every capacitor also contains parasitic impedances. These parasitic impedances are resistive as well as inductive. The resistive impedance is called *equivalent series resistance* (ESR) and the inductive impedance is called *equivalent series inductance* (ESL). The equivalent schematic diagram of any capacitor can therefore be drawn as shown in [Figure 33](#).



**Figure 33. ESR and ESL**

In most cases one can neglect the effect of inductive impedance ESL. Therefore, the following application focuses mainly on the parasitic resistance ESR.

[Figure 34](#) shows the output capacitor and its parasitic impedances in a typical LDO output stage.

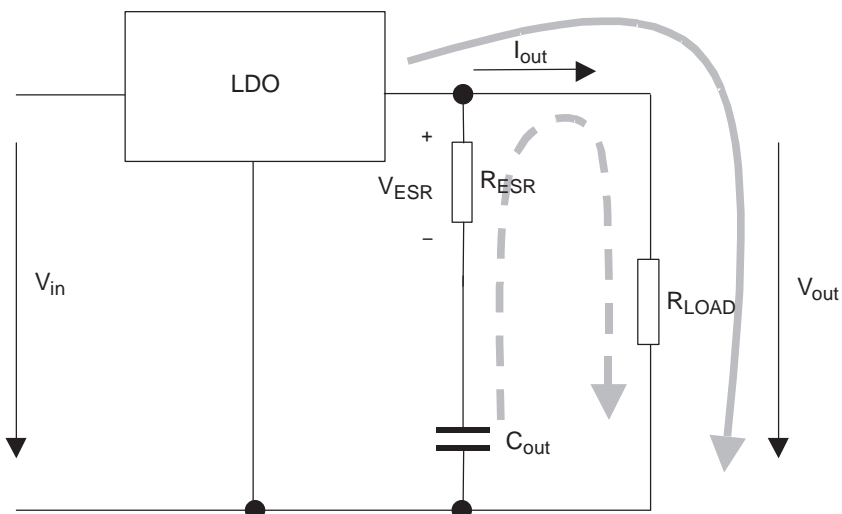


Figure 34. LDO Output Stage with Parasitic Resistances ESR

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ( $V_{(CO)} = V_{OUT}$ ). This means no current is flowing into the  $C_O$  branch. If  $I_{OUT}$  suddenly increases (a transient condition), the following occurs:

- The LDO is not able to supply the sudden current need due to its response time ( $t_1$  in Figure 31). Therefore, capacitor  $C_O$  provides the current for the new load condition (dashed arrow).  $C_O$  now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop occurs at  $R_{ESR}$ . This voltage is shown as  $V_{ESR}$  in Figure 30.
- When  $C_O$  is conducting current to the load, initial voltage at the load will be  $V_O = V_{(CO)} - V_{ESR}$ . Due to the discharge of  $C_O$ , the output voltage  $V_O$  drops continuously until the response time  $t_1$  of the LDO is reached and the LDO resumes supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as  $t_2$  in Figure 35.

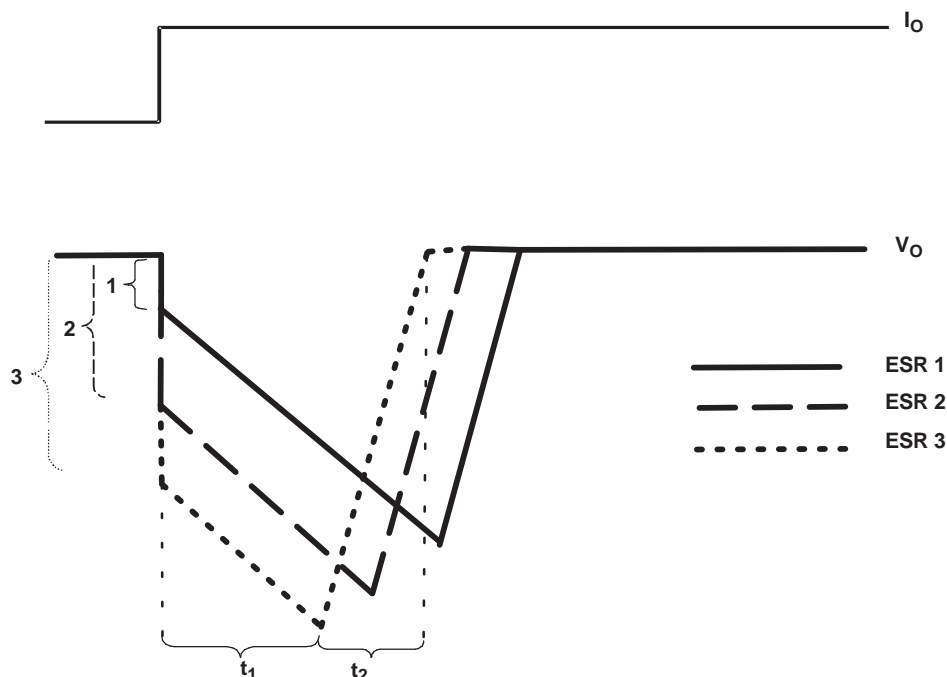


Figure 35. Correlation of Different ESRs and Their Influence on the Regulation of  $V_O$  at a Load Step from Low-to-High Output Current

Figure 35 also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the greater the voltage droop during the LDO response period.

## Conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

## Regulator Protection

Both TPS70175 PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS70175 also features internal current limiting and thermal protection. During normal operation, the TPS70175 regulator 1 limits output current to approximately 1.6 A (typ) and regulator 2 limits output current to approximately 750 mA (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typ), regulator operation resumes.

## Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(max)}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(max)}$ .

The maximum-power-dissipation limit is determined using Equation 1:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}} \quad (1)$$

where:

- $T_{Jmax}$  is the maximum allowable junction temperature
- $R_{\theta JA}$  is the thermal resistance junction-to-ambient for the package; that is, 32.6°C/W for the 20-terminal PWP with no airflow
- $T_A$  is the ambient temperature

The regulator dissipation is calculated using Equation 2:

$$P_D = (V_I - V_O) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS70175QPWPRQ1</a>	Active	Production	HTSSOP (PWP)   20	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	70175Q1
TPS70175QPWPRQ1.A	Active	Production	HTSSOP (PWP)   20	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	70175Q1

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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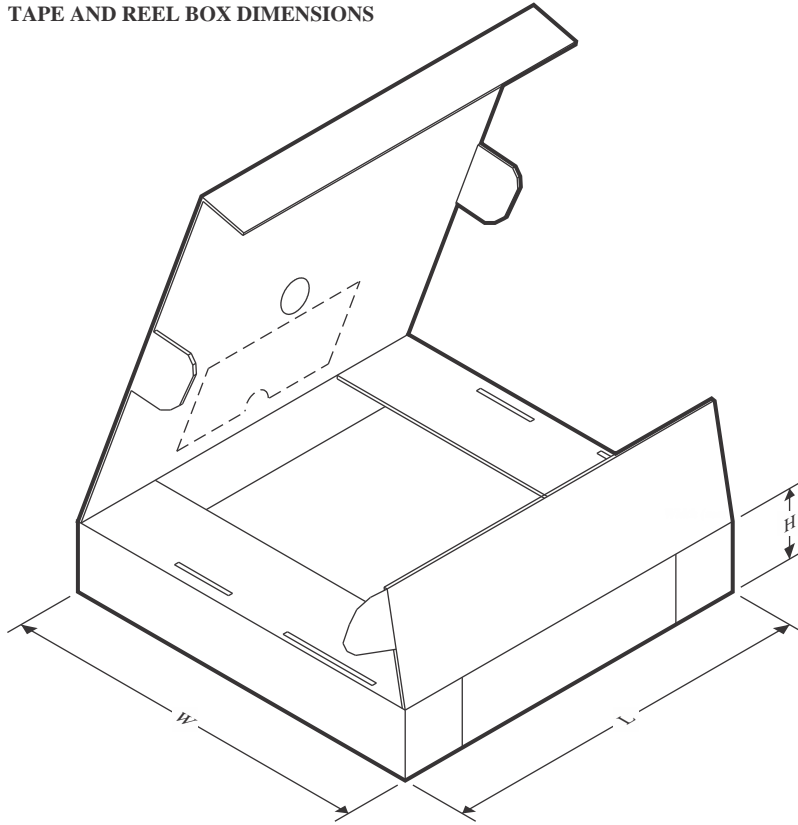
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70175QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70175QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

## GENERIC PACKAGE VIEW

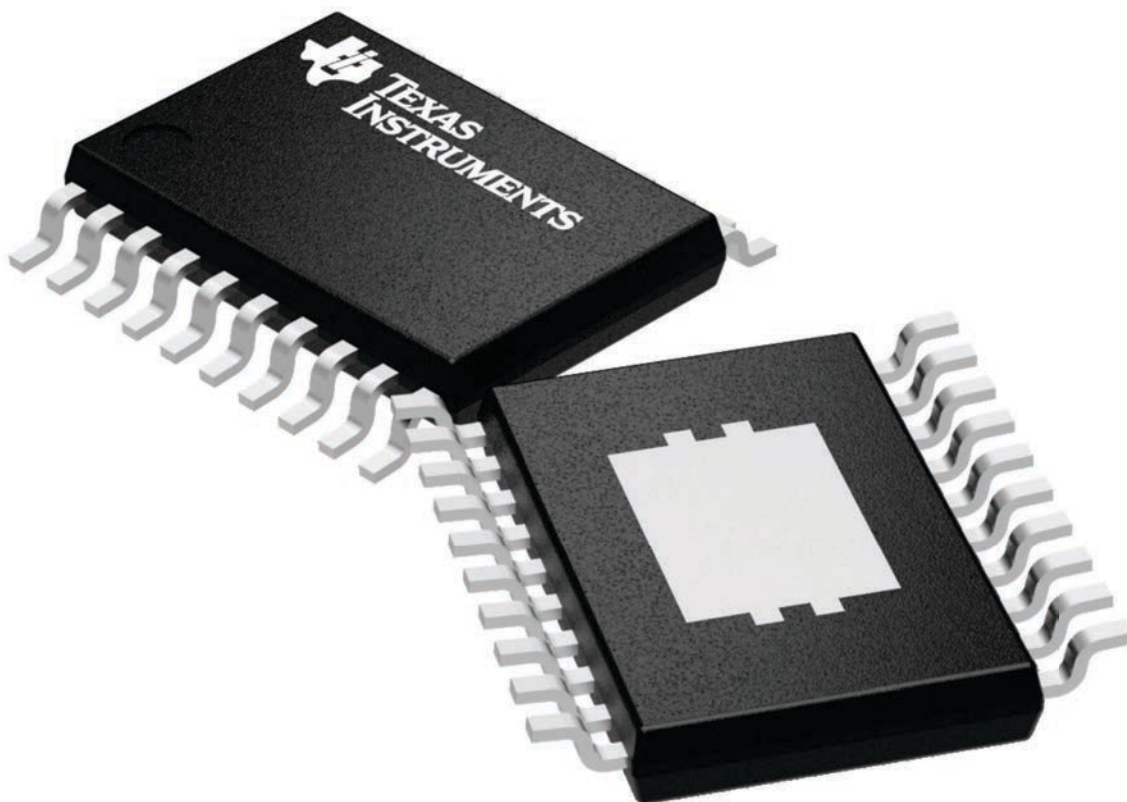
**PWP 20**

**HTSSOP - 1.2 mm max height**

6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

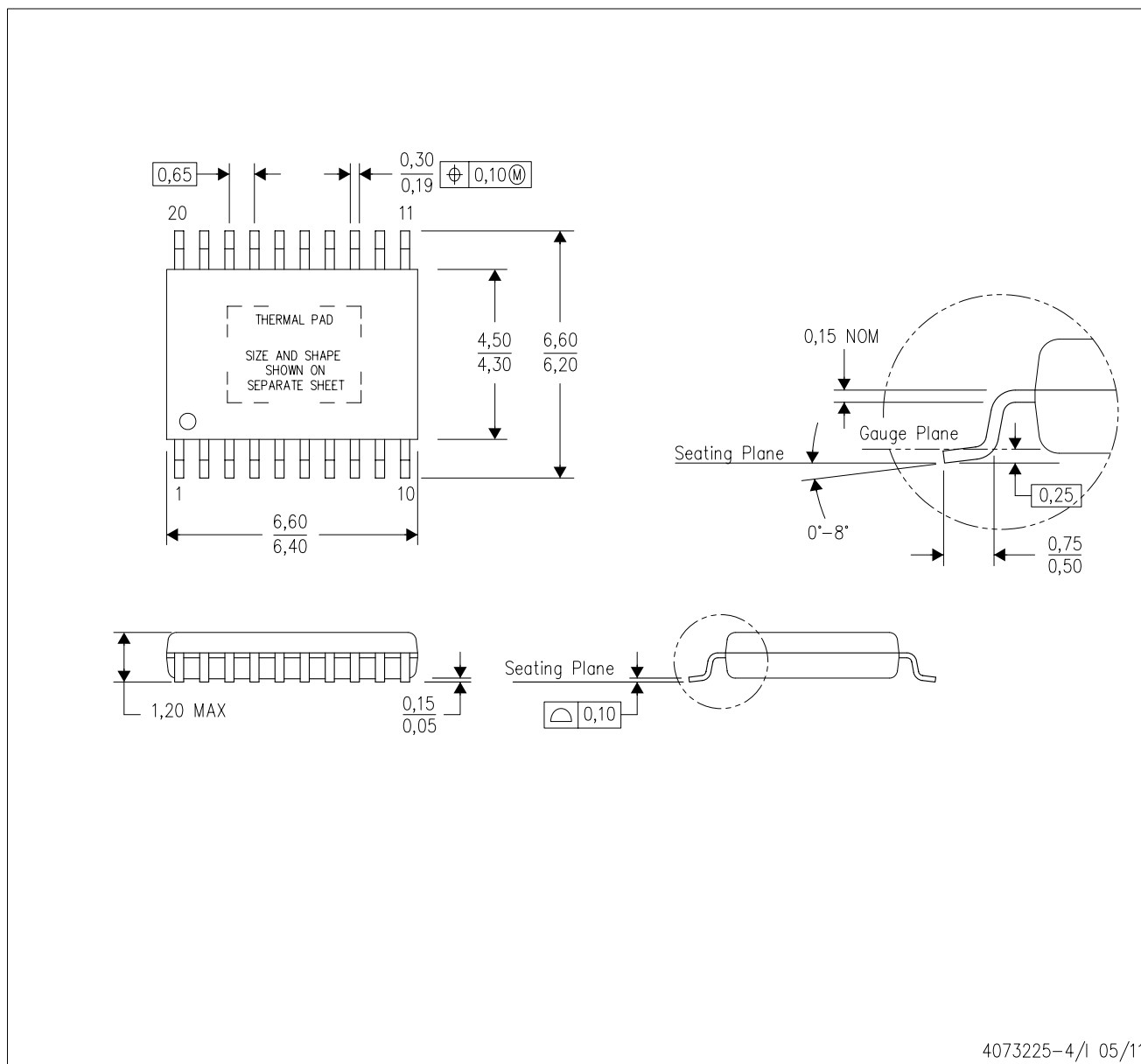
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224669/A

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-4/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

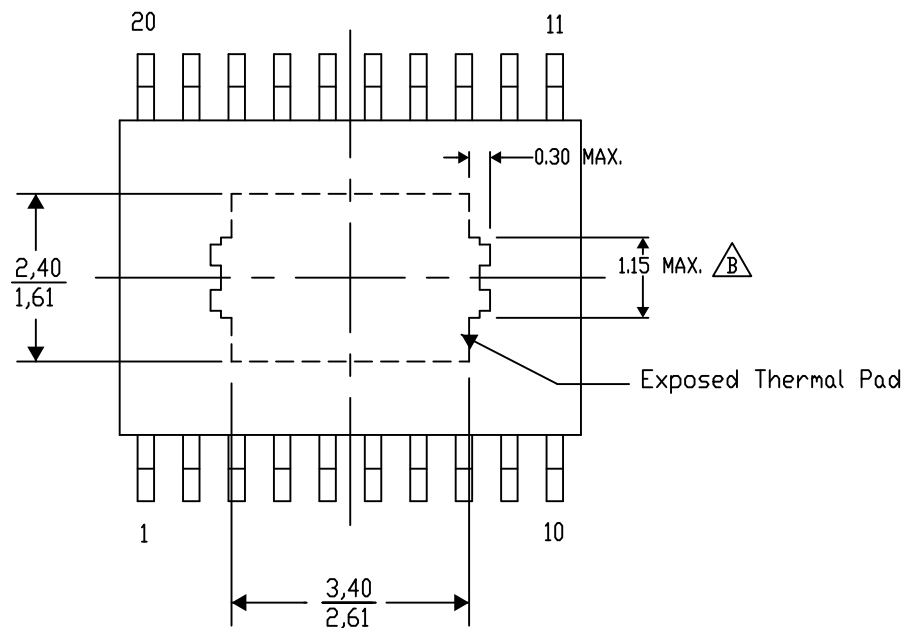
## PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



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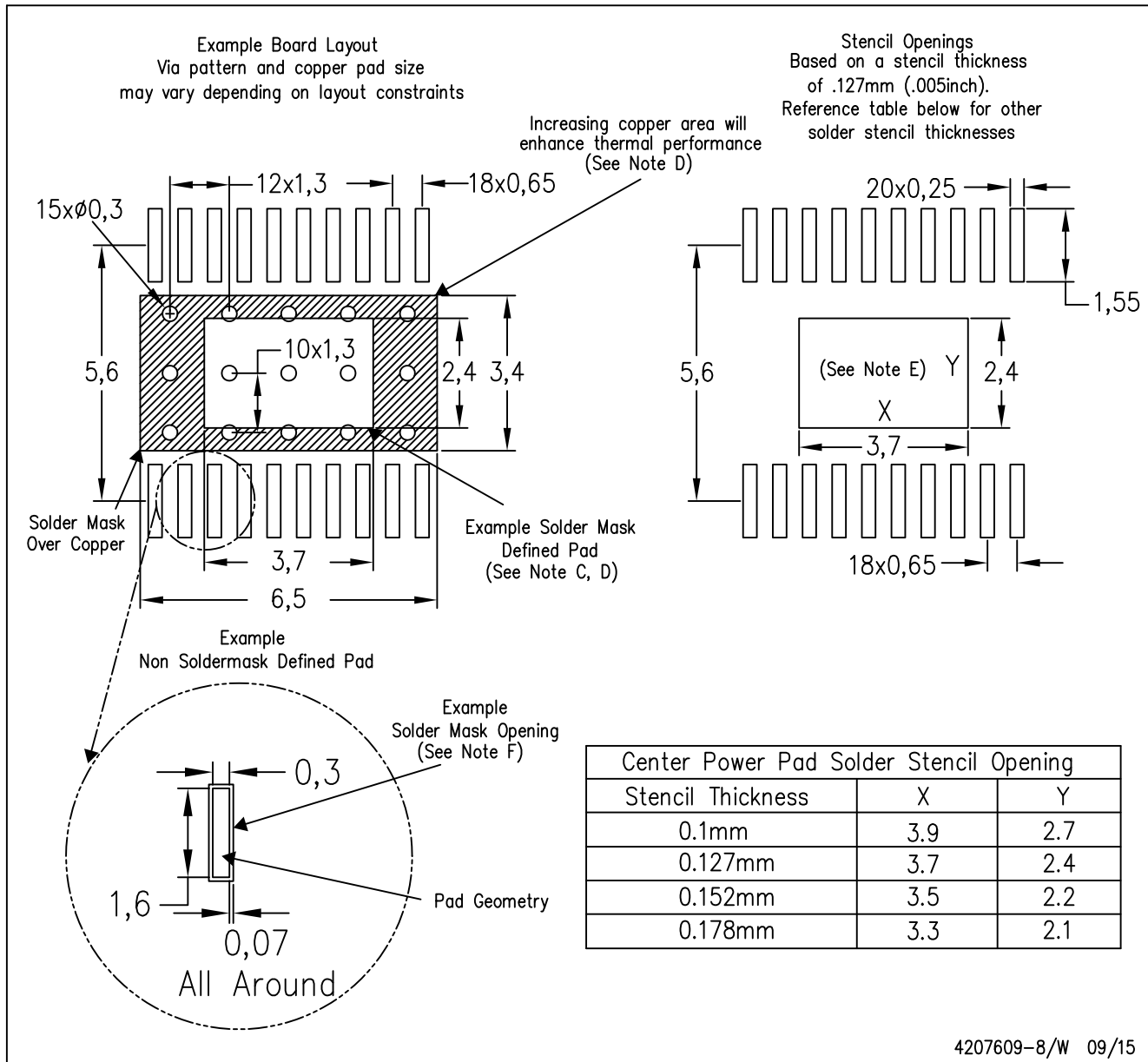
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

## PWP (R-PDSO-G20)

## PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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