Fully Programmable LCD Bias IC for GIP TV with Integrated 12-Ch Level Shifters and 6-Ch Gamma Buffers

1 Features

- 8.6V to 14.7V Input Voltage Range
- Boost Converter V_{DD}: 12.7V…19V (6-Bit)
- Integrated Input-to-Output Isolation Switch
- Buck Converter HV_{DD}: V_{DD} Tracking
- Buck Converter V_{CC}: 1.6V...2.0V & 3.0V…3.6V (4-Bit)
- Positive Charge Pump V_{GH}:
  - 19V…34V for Low Temperature (4-Bit)
  - 17V…32V for High Temperature (4-Bit)
- Negative Charge Pump V_{GL}: –1.8V…–8.1V (6-Bit)
- 6-Ch Gamma Buffer:
  - 3-Ch: V_{DD}…HV_{DD} (9-Bit)
  - 3-Ch: HV_{DD}...GND (9-Bit)
- 9-Bit V_{COM} Reference
- 3-Bit V_{COM} Gain
- Temperature Compensation for V_{GH} and V_{COM}
- Reset Signal with Programmable Delay Time
- Programmable Sequencing Delays (4 × 3-Bit)
- Thermal Shutdown
- 12-Channel Level Shifters:
  - Supports Forward and Reverse Operation
  - Abnormal Operation Detection
- 56-Pin 7mm × 7mm QFN Package

2 Applications

- LCD GIP/GOA TVs
- LCD GIP/GOA Monitors

3 Description

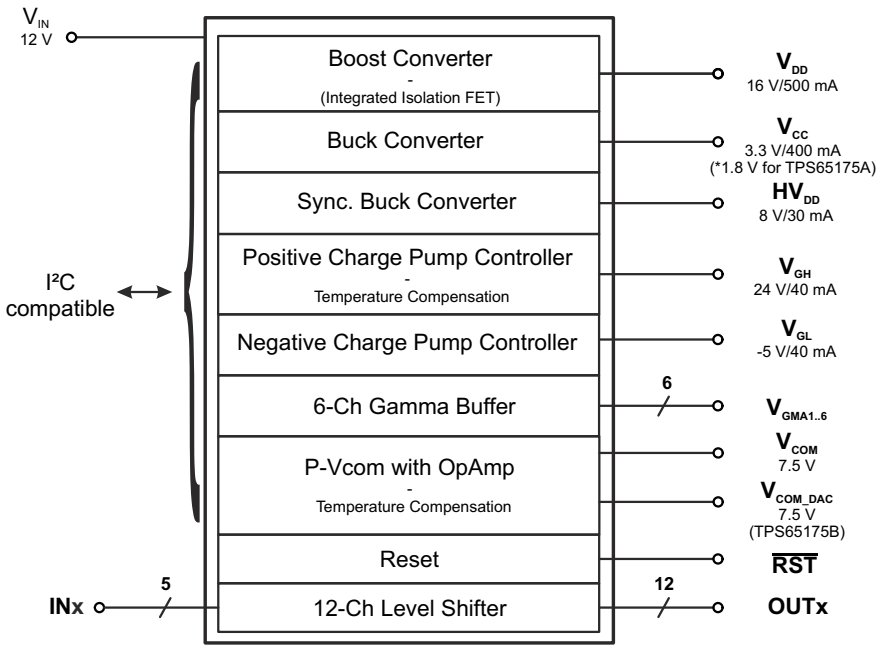
The TPS65175/A provides a simple and economic power supply solution for a wide variety of LCD bias applications. The device provides all supply rails needed by a TFT-LCD panel but also 6 gamma references, a supply rail for LVDS support, as well as a Vcom reference. A 12-Channel Level Shifter is also integrated. The solution is delivered in a small 7x7mm QFN package.

The TPS65175/A provides a simple and economic power supply solution for a wide variety of LCD bias applications. The device provides all supply rails needed by a TFT-LCD panel. V_{CC} and $\overline{RST}$ for the T-Con. V_{DD} and HV_{DD} for the Source Driver. V_{GH} and V_{GL} for the Gate Driver or the Level Shifters. A V_{COM} operational amplifier is also integrated to provide a common plane reference. The V_{GH} and V_{COM} voltages can be compensated for low and high temperatures. The transition from one programmed value to another is made using an external thermistor connected to the IC. In addition, a 6-channel Gamma Buffer as well as a 12-Channel Level Shifter are integrated. All output rails and delay times are programmable by a two-wire interface: a single BOM (Bill of Material) can cover several panel types and sizes whose desired output levels can be programmed in production and stored in a non-volatile memory embedded into the TPS65175/A. The solution is delivered in a small 7mm x 7mm QFN-56 package.

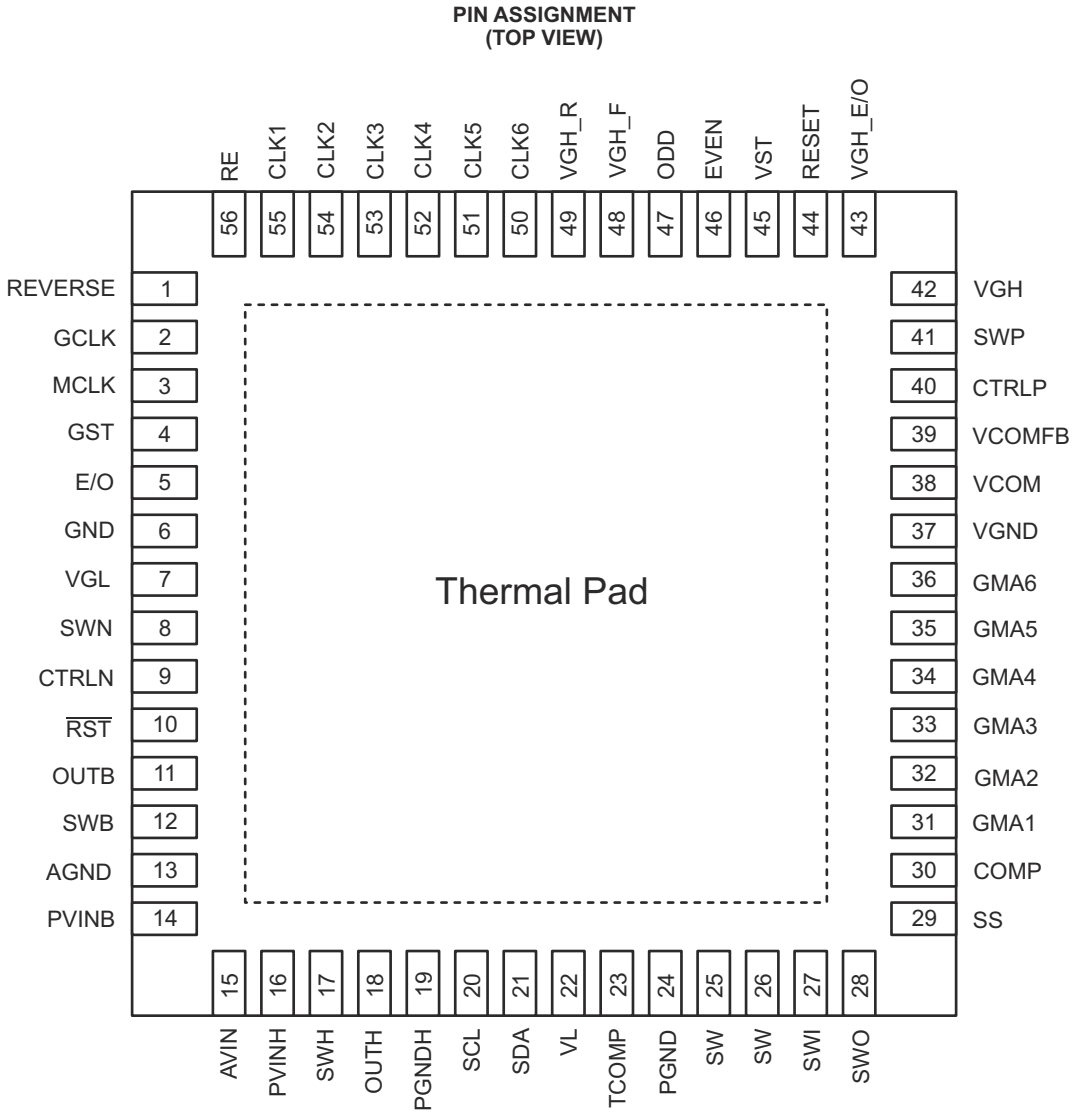
Package Information

PART NUMBER	PACKAGE	PACKAGE SIZE (NOM)(1)
TPS65175ARSHR	WQFN (48)	7.00mm × 7.00mm
TPS65175RSHR		

(1) The package size (length x width) is a nominal value and includes pins, where applicable.



4 Pin Configurations



PIN ASSIGNMENT
(TOP VIEW)

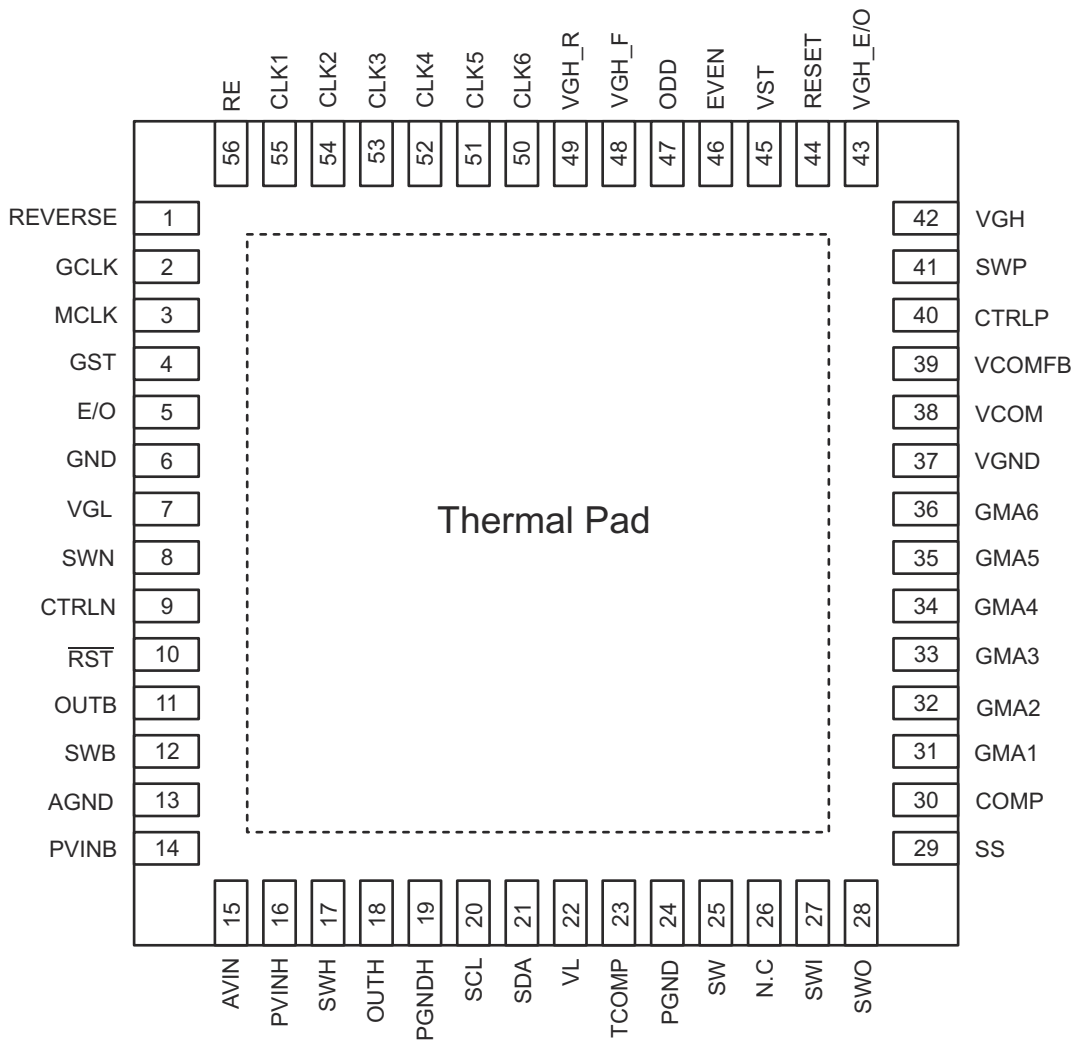


Table 4-1. Pin Descriptions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
REVERSE	1	I	REVERSE input pin
GCLK	2	I	GCLK input pin
MCLK	3	I	MCLK input pin
GST	4	I	GST input pin
E/O	5	I	E/O input pin
GND	6		Ground pin
VGL	7	I	Negative charge pump (V_{GL}) output voltage sense pin
SWN	8	I/O	Negative charge pump (V_{GL}) switch pin
CTRLN	9	O	Negative charge pump (V_{GL}) base drive signal pin
$\overline{RST}$	10	O	Reset generator open drain output pin
OUTB	11	I	Buck converter (V_{CC}) output voltage sense pin
SWB	12	I/O	Buck converter (V_{CC}) switch pin
AGND	13, exposed pad		Analog ground pin. Connect this pin to the PowerPAD™.

Table 4-1. Pin Descriptions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
PVINB	14	I	Buck converter (V_{CC}) input supply pin
AVIN	15	I	Internal regulator supply pin
PVINH	16	I	Synchronous buck converter (HV_{DD}) power input pin
SWH	17	I/O	Synchronous buck converter (HV_{DD}) switch pin
OUTH	18	I	Synchronous buck converter (HV_{DD}) output voltage sense pin
PGNDH	19		Synchronous buck converter (HV_{DD}) power ground pin
SCL	20	I/O	I^2C clock pin
SDA	21	I/O	I^2C data pin
VL	22	O	Internal regulator output pin. Connect an output capacitor to this pin
TCOMP	23	I	Temperature compensation input pin. Connect the thermistor / pull-up resistor network to this pin
PGND	24		Boost converter (V_{DD}) power ground pin
SW	25,26	I/O	Boost converter (V_{DD}) switch pin
SWI	27	I	Isolation switch input pin. The SWI pin is connected to the internal overvoltage protection comparator of the boost converter
SWO	28	O	Isolation switch output pin (V_{DD})
SS	29	O	Boost converter (V_{DD}) soft-start pin. Connect a capacitor to this pin if a soft-start is needed. Open = no soft-start.
COMP	30	I/O	Boost converter (V_{DD}) compensation pin
GMA1	31	O	Gamma buffer 1 output pin. DAC output
GMA2	32	O	Gamma buffer 2 output pin. DAC output
GMA3	33	O	Gamma buffer 3 output pin. DAC output
GMA4	34	O	Gamma buffer 4 output pin. DAC output
GMA5	35	O	Gamma buffer 5 output pin. DAC output
GMA6	36	O	Gamma buffer 6 output pin. DAC output
VGND	37		Ground pin for the V_{COM} Op-Amp
VCOM	38	O	Operational amplifier (V_{COM}) output pin
VCOM_FB	39	I	Operational amplifier (V_{COM}) inverting pin. Connect the panel feedback to this pin
CTRLP	40	O	Positive charge pump (V_{GH}) base drive signal pin
SWP	41	I/O	Positive charge pump (V_{GH}) switch pin
VGH	42	I	Positive charge pump (V_{GH}) output voltage sense pin and level shifters supply pin
VGH_E/O	43	I	EVEN / ODD channels supply pin
RESET	44	O	RESET output pin
VST	45	O	VST output pin
EVEN	46	O	EVEN output pin
ODD	47	O	ODD output pin
VGH_F	48	O	VGH_F output pin
VGH_R	49	O	VGH_R output pin
CLK6	50	O	CLK6 output pin
CLK5	51	O	CLK5 output pin
CLK4	52	O	CLK4 output pin
CLK3	53	O	CLK3 output pin
CLK2	54	O	CLK2 output pin
CLK1	55	O	CLK1 output pin
RE	56	O	Gate shaping resistor connection pin

Table 4-2. TPS65175A Pin Descriptions

PIN		I/O[1]	DESCRIPTION[2]
NAME	NO.		
N.C	26		Not connected

1. I = input, O = output
2. All other pins functions are the same for TPS65175 and TPS65175A.

5 Ordering Information (1)

T_A	ORDERING	PACKAGE	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY	V_{CC} DEFAULT VALUE
–40°C to 85°C	TPS65175RSHR	56-Pin 7x7 QFN	TPS65175	Tape and reel , 3000	3.3 V
	TPS65175ARSHR		TPS65175A		1.8 V

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE		UNIT
	MIN	MAX	
Voltage range on pins CLK1…6, EVEN, ODD, RESET, VGH_F, VGH_R, VST (2)	–10	40	V
Voltage range on pins CTRLP, RE, VGH, VGH_E/O(2)	–0.3	40	V
Voltage range on pins AVIN, GMA1…6, NEG, OUTH, PVINB, PVINH, SW, SWB, SWH, SWI, SWN, SWO, SWP, VCOM, VCOMFB (2)	–0.3	20	V
Voltage on pins COMP, CTRLN, E/O, GCLK, GST, MCLK, OUTB, REVERSE, $\overline{RST}$, SCL, SDA, SS, TCOMP, VL (2)	–0.3	7.0	V
Voltage on pin VGL(2)	–10	0.3	V
ESD rating HBM (Human Body Model)		2	kV
ESD rating MM (Machine Model)		200	V
ESD rating CDM (Charged Device Model)		700	V
Continuous power dissipation	See the Thermal Table		
Operating junction temperature range	–40	150	°C
Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With respect to the GND pin.

6.2 Thermal Information

THERMAL METRIC1		TPS65175/A	UNITS
		RSH (56 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	26.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	13.8	
θ_{JB}	Junction-to-board thermal resistance	4.3	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	4.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.3	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
AV_{IN}	Input voltage range	8.6	12	14.7	V
C_{VL}	Input capacitor on internal regulator input pin VL		1		µF
BOOST CONVERTER					
V_{DD}	Boost output voltage range	12.7		19	V
L	Boost converter inductor	10		22	µH
C_{IN_BOOST}	Input capacitor on boost converter input	20			µF
C_{OUT_BOOST}	Output capacitor on boost converter output on SWI pin	10	20		µF
C_{OUT_ISO}	Output capacitor on isolation MosFET output on SWO pin	30	40		µF
BUCK CONVERTER					
V_{CC}	Buck converter output voltage range	1.6		3.6	V
LB	Buck converter inductor	10		22	µH

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
C_{IN_B}	Input capacitor on buck converter input pin PVINB	10			µF
C_{OUT_B}	Output capacitor on buck converter output	30	40		µF
SYNCHRONOUS BUCK CONVERTER					
HV_{DD}	Synchronous buck converter output voltage range		$V_{DD}/2$		V
LH	Synchronous buck converter inductor	4.7		6.8	µH
C_{IN_H}	Input capacitor on synchronous buck converter input pin PVINH		10		µF
C_{OUT_H}	Output capacitor on synchronous buck converter output	4.7	10	20	µF

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
POSITIVE CHARGE PUMP CONTROLLER					
V_{GH_LT}	Positive charge pump output voltage range Low Temperature	19		34	V
V_{GH_HT}	Positive charge pump output voltage range High Temperature	17		32	V
C_{FLY_CP}	Charge pump flying capacitor		220		nF
C_{STOR_CP}	Charge pump storage capacitor		100		nF
C_{OUT_CP}	Charge pump output capacitor		4.7		µF
NEGATIVE CHARGE PUMP CONTROLLER					
V_{GL}	Negative charge pump output voltage range	–1.8		–8.1	V
C_{FLY_CP}	Charge pump flying capacitor		220		nF
C_{STOR_CP}	Charge pump storage capacitor		100		nF
C_{OUT_CP}	Charge pump output capacitor		4.7		µF
TEMPERATURE					
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

6.4 Electrical Characteristics

AV_{IN} = PV_{INB} = PV_{INH} = 12V, V_{DD} = 16V, HV_{DD} = 8V , V_{CC} = 3.3V for TPS65175 / V_{CC} = 1.8V for TPS65175A , V_{GH_LT} = 30V, V_{GH_HT} = 28V, V_{GL} = –5V, V_{COM} = 7.5V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted). Values in **bold** are guaranteed through test, design or correlations.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		8.6		14.7	V
I_{Q_AVIN}	Supply quiescent current AVIN	Device not switching		2.0	4.0	mA
I_{Q_PVINB}	Supply quiescent current PVINB	Device not switching		0.1	1.0	mA
I_{Q_PVINH}	Supply quiescent current PVINH	Device not switching		1.5	2.5	mA
I_{Q_SWI}	Supply quiescent current SWI	Device not switching		7.3	12	mA
I_{Q_VGH}	Supply quiescent current VGH	E/O, GCLK, GST, MCLK, REVERSE = 0 V		0.4	0.6	mA
$I_{Q\_VGH\_E/O}$	Supply quiescent current VGH_E/O	E/O, GCLK, GST, MCLK, REVERSE = 0 V		0.06	0.1	mA
I_{Q_VGL}	Negative supply current	E/O, GCLK, GST, MCLK, REVERSE = 0 V		0.13	0.25	mA
LCD BIAS MISCELLANEOUS						
V_{UVLO}	Undervoltage lockout	AV_{IN} rising	8.3	8.6	8.9	V
	Undervoltage lockout hysteresis		0.3	0.8	1.3	V
T_{SD}	Thermal shutdown	T_J rising	**130**	138	**150**	°C
T_{HYS}	Thermal shutdown hysteresis	T_J falling	**8.5**	9	**10**	
LOGIC SIGNAL SCL, SDA						
V_{IH}	High level input voltage SCL, SDA	Input rising, AV_{IN} = 8.6 V to 14.7 V	0.65*V_{CC}			V
V_{IL}	Low level input voltage SCL, SDA	Input falling, AV_{IN} = 8.6 V to 14.7 V			0.3 x V_{CC}	
INTERNAL OSCILLATOR						
f_{OSC}	Low switching frequency for the boost, the buck converter and the charge pumps		600	750	900	kHz
	High switching frequency for the boost and the buck converter		1.2	1.5	1.8	MHz
INTERNAL REGULATOR						
V_L (2)	Internal regulator	No load	4.8	5.0	5.2	V
		5 mA current				

AV_{IN} = PV_{INB} = PV_{INH} = 12V, V_{DD} = 16V, HV_{DD} = 8V , V_{CC} = 3.3V for TPS65175 / V_{CC} = 1.8V for TPS65175A , V_{GH_LT} = 30V, V_{GH_HT} = 28V, V_{GL} = –5V, V_{COM} = 7.5V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted). Values in **bold** are guaranteed through test, design or correlations.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CONVERTER [V_{DD}]						
V_{DD_ACC}	Output voltage accuracy	V_{DD} default value	–2%	16	2%	V
$r_{DS(on)}$	N-MOSFET on-resistance - TPS65175	I_{SW} = current limit		90	165	mΩ
	N-MOSFET on-resistance - TPS65175A			100	179	
I_{LIM}	N-MOSFET current limit		3.5	4.3	5.2	A
I_{SS}	Soft-start current	V_{SS} = 1.230 V	7	10	13	µA
	Line regulation	AV_{IN} = 8.6 V to 14.7 V, I_{OUT} = 700 mA		0.002		%/V
	Load regulation	I_{OUT} = 0 A to 1 A		0.066		%/A
ISOLATION SWITCH						
$r_{DS(on)ISO}$	Isolation MOSFET on-resistance	I_{SWI} = 1 A		100	180	mΩ
I_{SC_ISO}	Short circuit current limit	V_{SWI} = 12 V, V_{SWO} = 0 V	100	200	300	mA
BUCK CONVERTER [V_{CC}]						
V_{CC_ACC}	Output voltage accuracy	V_{CC} default value TPS65175	–3%	3.3	3%	V
		V_{CC} default value TPS65175A	–3%	1.8	3%	V
$r_{DS(on)}$	Switch on-resistance	I_{SWB} = current limit		180	300	mΩ
I_{LIM}	Switch current limit		2.6	3.4	4.2	A
	Line regulation	V_{IN} = AV_{IN} = PV_{INB} = 8.6 V to 14.7 V I_{CC} = 200 mA		0.001		%/V
	Load regulation	I_{CC} = 0 A to 800 mA		0.033		%/A
SYNCHRONOUS BUCK CONVERTER [HV_{DD}]						
HV_{DD_ACC}	Output voltage accuracy	HV_{DD} default value	–2%	8	2%	V
$r_{DS(on)}$	MOSFET on-resistance	I_{SBW3} = current limit		320	480	mΩ
I_{LIM}	Switch current limit – source		0.9	1.3	1.7	A
	Switch current limit – sink		–0.9	–1.3	–1.7	
f_{SWH}	Switching frequency synchronous buck converter		1.2	1.5	1.8	MHz
	Line regulation	AV_{IN} = PV_{INH} = 8.6 V to 14.7 V I_{OUT} = ±300 mA		0.003		%/V
	Load regulation	I_{OUT} = –500 mA to 500 mA		0.007		%/A
POSITIVE CHARGE PUMP CONTROLLER [V_{GH}]						
$V_{GH\_LT\_ACC}$	Output voltage accuracy	V_{GH_LT} default value	–3%	30	3%	V
$V_{GH\_HT\_ACC}$		V_{GH_HT} default value	–3%	28	3%	
I_{CTRLP_SC}	Base current during short circuit	VGH = GND	40	55	75	µA
I_{CTRLP_max}	Maximum base current		1	1.6	2	mA
	Line regulation	AV_{IN} = 8.6 V to 14.7 V, I_{GH} = 50 mA		0.004		%/V
	Load regulation	I_{GH} = 0 A to 100 mA		0.414		%/A
NEGATIVE CHARGE PUMP CONTROLLER [V_{GL}]						
V_{GL}	Output voltage accuracy	V_{GL} default value	–3%	–5	3%	V
I_{CTRLN_SC}	Base current during short circuit	VGL = GND	200	320	440	µA
I_{CTRLN_max}	Maximum base current		1	1.6	3	mA
	Line regulation	AV_{IN} = 8.6 V to 14.7 V, I_{GL} = 50 mA		0.001		%/V
	Load regulation	I_{GL} = 0 A to 100 mA		0.817		%/A
GAMMA BUFFER [GMA]						
I_O	Continuous output current		10	30		mA
V_{OH1}	Output voltage swing high GMA1,2,3	I_{OUT} = 10mA	V_{DD}–0.7	V_{DD}–0.5		V
V_{OL1}	Output voltage swing low GMA1,2,3	I_{OUT} = 10mA		HV_{DD}+0.5	HV_{DD}+0.7	
V_{OH2}	Output voltage swing high GMA4,5,6	I_{OUT} = 10mA	HV_{DD}–0.7	HV_{DD}–0.5		V
V_{OL2}	Output voltage swing low GMA4,5,6	I_{OUT} = 10mA		0.5	0.7	
INL_max	Maximum integral nonlinearity			±0.6		LSB

AV_{IN} = PV_{INB} = PV_{INH} = 12V, V_{DD} = 16V, HV_{DD} = 8V , V_{CC} = 3.3V for TPS65175 / V_{CC} = 1.8V for TPS65175A , V_{GH_LT} = 30V, V_{GH_HT} = 28V, V_{GL} = –5V, V_{COM} = 7.5V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted). Values in **bold** are guaranteed through test, design or correlations.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DNL_max	Maximum differential nonlinearity			±0.3		LSB
RESET GENERATOR [$\overline{RST}$](1)						
$V_{\overline{RST}(ON)}$	Low voltage level	$I_{\overline{RST}(ON)}$ = 1 mA			0.4	V
$I_{LEAK\_\overline{RST}}$	Leakage current	$V_{\overline{RST}(ON)}$ = V_{CC} = 3.3 V			2	µA
P-VCOM [VCOM]						
V_{COM}	Output voltage accuracy	V_{COM} default value	–2%	7.5	2%	V
BW	Unity gain -3dB bandwidth	V_{CM} = 7.5 V, V_{IN} = 63 mVpp	**55**	75	**95**	MHz
AV_{OL}	Open loop gain	V_{CM} = 7.5 V	**100**	120	**140**	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = 7.5 V	**95**	110	**125**	dB
PSRR	Power Supply Rejection Ratio	V_{CM} = 7.5 V, V_{DD} = 12.7 V to 19 V	**80**	110	**140**	dB
SR	Slew rate rising	Unity gain, V_{COM_FB} = 7.5 V ± 2 V_{PP}	**23**	45	**80**	V/µs
	Slew rate falling		**25**	45	**80**	
$r_{DS(on)}$	High-side output resistance	I_{OUT} = 10 mA, sourcing, V_{COM} = 9.5 V, V_{NEG} = 7.5 V		20	**40**	Ω
	Low-side output resistance	I_{OUT} = 10 mA, sinking, V_{COM} = 7.5 V, V_{NEG} = 9.5 V		2	**10**	
I_{PK}	Peak output current sourcing	Unity gain, VCOM = GND	400	550		mA
	Peak output current sinking	Unity gain, VCOM = SWO	400	550		
LEVEL SHIFTERS MISCELLANEOUS						
UVLO	Undervoltage lockout rising	V_{GH} rising	5.0	9.2	11	V
	Undervoltage lockout falling	V_{GH} falling	2.0	3.5	5.0	
LEVEL SHIFTERS INPUT SIGNALS (E/O, GCLK, GST, MCLK, REVERSE)						
V_{IH}	High level input voltage E/O, GCLK, GST, MCLK, REVERSE	V_{GH} = 17 V to 34 V, T_A = 25°C ~ 85°C	1.25			V
		V_{GH} = 17 V to 34 V, T_A = -40°C ~ 85°C	1.30			V
V_{IL}	Low level input voltage E/O, GCLK, GST, MCLK, REVERSE	V_{GH} = 17 V to 34 V			0.75	V
I_{IN}	Input current	E/O, GCLK, GST, MCLK = 0 V			±100	nA
		E/O, GCLK, GST, MCLK = 3.3 V			±100	
		REVERSE = 3.3 V	24	33	44	µA
$R_{PULL-DOWN}$	REVERSE pin internal pull-down resistor		75	100	135	kΩ
LEVEL SHIFTERS OUTPUTS (CLK1 to CLK6)						
$r_{DS(on)}$	High side ON resistance	I_{OUT} = 10 mA, sourcing (high side)		12	30	Ω
	Low side ON resistance	I_{OUT} = 10 mA, sinking (low side)		7	15	
t_{PLH}	GCLK rising edge propagation delay	GCLK rising edge to CLK rising edge, C_{OUT} = 300 pF		50	100	ns
t_{PHL}	MCLK falling edge propagation delay	MCLK falling edge to CLK falling edge, C_{OUT} = 300 pF		50	100	ns
LEVEL SHIFTERS OUTPUTS (EVEN, ODD, RESET, VGH_F, VGH_R, VST)						
$r_{DS(on)}$	High side ON resistance	I_{OUT} = 10 mA, sourcing (high side)		35	80	Ω
	Low side ON resistance	I_{OUT} = 10 mA, sinking (low side)		16	40	
t_{PLH}	GST rising edge propagation delay	GST rising edge to VST rising edge, C_{OUT} = 300 pF		60	120	ns
		GST rising edge to RESET rising edge, C_{OUT} = 300 pF		60	120	
t_{PHL}	GST falling edge propagation delay	GST falling edge to VST falling edge, C_{OUT} = 300 pF		60	120	ns
		GST falling edge to RESET falling edge, C_{OUT} = 300 pF		60	120	

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	E/O rising edge propagation delay	E/O rising edge to ODD falling edge, C_{OUT} = 300 pF		60	120	ns
		E/O rising edge to EVEN falling edge, C_{OUT} = 300 pF		60	120	
t_{PHL}	E/O falling edge propagation delay	E/O falling edge to ODD rising edge, C_{OUT} = 300 pF		60	120	ns
		E/O falling edge to EVEN rising edge, C_{OUT} = 300 pF		60	120	
t_{SU}	E/O set-up time during abnormal operation	E/O to GST rising edge		5	30	ns
t_{PLH}	REVERSE rising edge propagation delay	REVERSE rising edge to VGH_F falling edge, C_{OUT} = 300 pF		60	120	ns
t_{PHL}	GST rising edge propagation delay	GST rising edge to VGH_R falling edge, C_{OUT} = 300 pF		60	120	ns
t_{12}	REVERSE dead time	VGH_F falling edge to VGH_R rising edge, C_{OUT} = 300 pF	20	500	1000	ns
t_{13}		VGH_R falling edge to VGH_F rising edge, C_{OUT} = 300 pF	20	500	1000	
GATE VOLTAGE SHAPING (RE)						
$r_{DS(on)}$	Gate shaping resistance	Measured between active CLK channel and RE at 10 mA		70	140	Ω
t_{PHL}	MCLK rising edge propagation delay	MCLK rising edge to CLK falling edge, C_{OUT} = 300 pF		65	100	ns
I_{LEAK}	Gate shaping leakage current	Measured between RE and GND	-10		10	µA

(1) External pull-up resistor to be chosen so that the current flowing into $\overline{RST}$ pin when active ($V_{\overline{RST}}$ = 0 V) is below $I_{\overline{RST}(ON)}$ = 1 mA.
(2) The V_L regulator can supply 5 mA externally

6.5 I²C Interface Timing Characteristics (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	600			ns
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
$t_{hd;STA}$	Hold time for a repeated START condition	Standard mode	4.0			µs
		Fast mode	600			ns
$t_{su;STA}$	Setup time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	600			ns
$t_{su;DAT}$	Data setup time	Standard mode	250			ns
		Fast mode	100			ns
$t_{hd;DAT}$	Data hold time	Standard mode	0.05		3.45	µs
		Fast mode	0.05		0.9	µs
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		1000	ns

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RCL}	Rise time of SCL signal	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{FCL}	Fall time of SCL signal	Standard mode	20 + 0.1C_B		300	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{RDA}	Rise time of SDA signal	Standard mode	20 + 0.1C_B		1000	ns
		Fast mode	20 + 0.1C_B		300	ns
t_{FDA}	Fall time of SDA signal	Standard mode	20 + 0.1C_B		300	ns
		Fast mode	20 + 0.1C_B		300	ns
$t_{su;STO}$	Setup time for STOP condition	Standard mode	4.0			µs
		Fast mode	600			ns
C_B	Capacitive load for SDA and SCL				0.4	nF

(1) Industry standard I²C timing characteristics. Not tested in production.

6.6 I²C Timing Diagrams

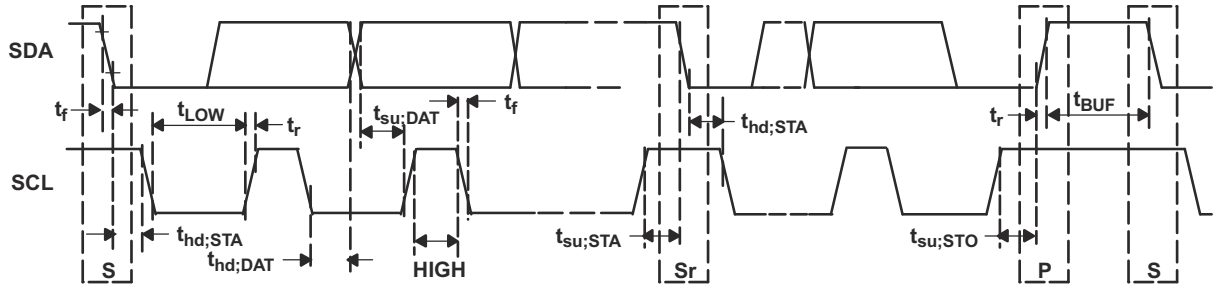


Figure 6-1. Serial Interface Timing for F/S-Mode

Note

The electrical parameters are still valid when using two Schottky diodes in series instead of one on the boost converter block.

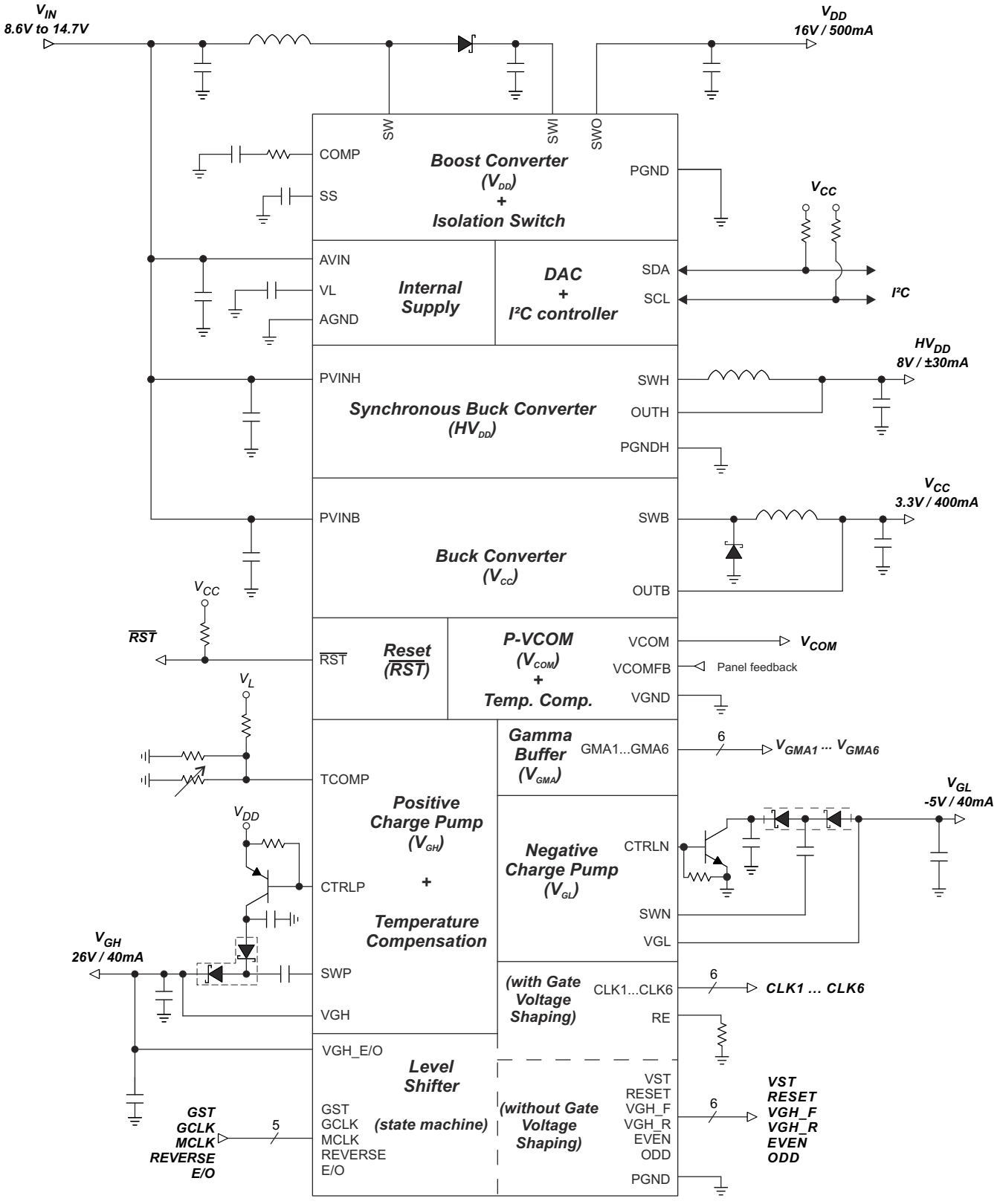


Figure 6-2. Simple Application Schematic

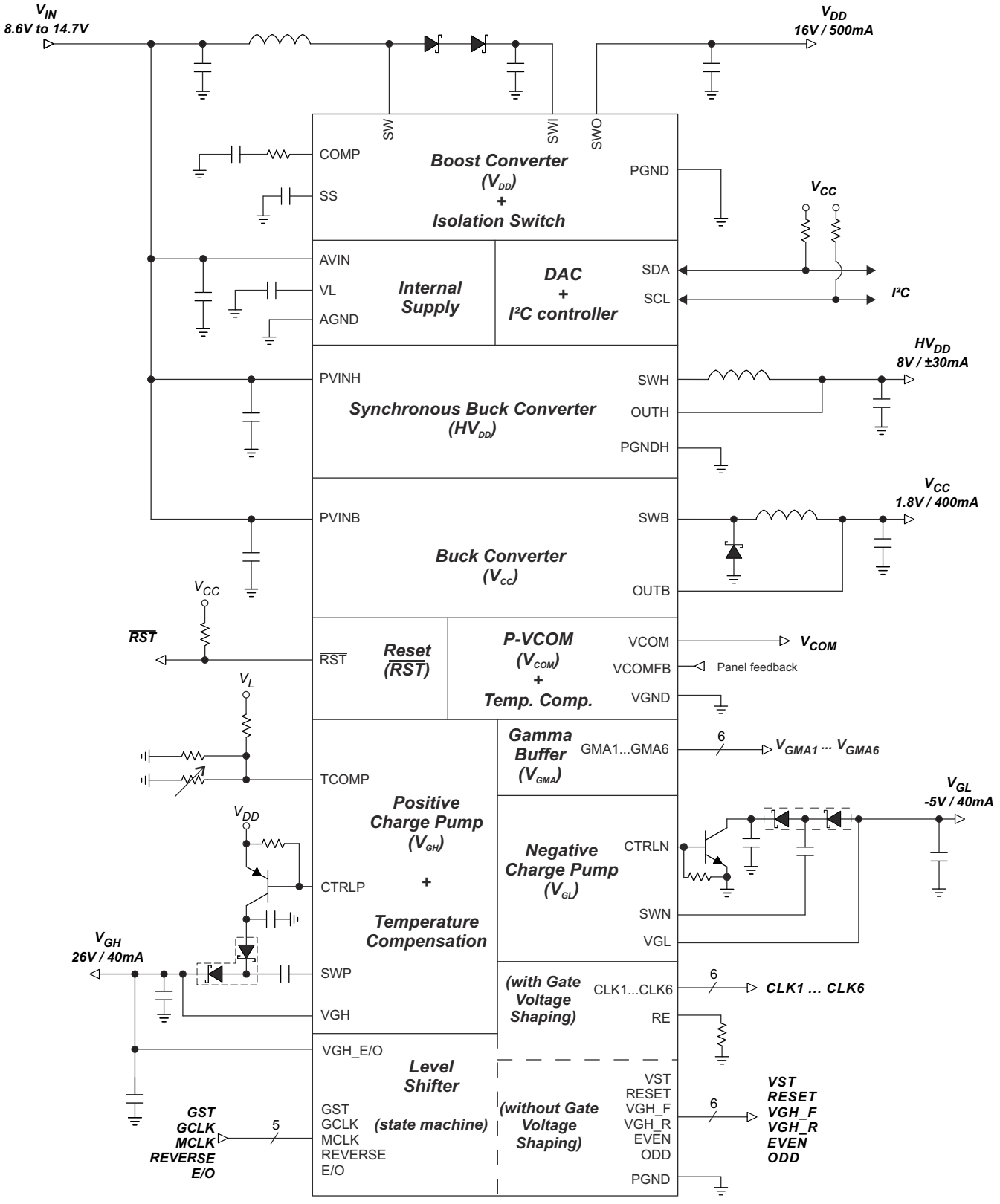


Figure 6-3. Simple Application Schematic using 2 Serial Schottky Diodes for the Boost Converter

6.7 Typical Characteristics

Table 6-1. Table of Graphs

PARAMETER	Conditions	Figure
Buck Converter - (V_{IN} = 12 V, L = 10 µH, C_{OUT} = 40 µF)		
Efficiency vs. Load Current	V_{CC} = 3.3 V	Figure 6-4
PWM Switching – Light Load	V_{CC} = 3.3 V/50 mA	Figure 6-5
PWM Switching – Heavy Load	V_{CC} = 3.3 V/ 500 mA	Figure 6-6
Load Transient Response	V_{CC} = 3.3 V/100 ~ 300 mA	Figure 6-7
Synchronous Buck Converter - (V_{IN} = 12 V, L = 6.8 µH, C_{OUT} = 10 µF)		
Efficiency vs. Load Current	HV_{DD} = 8 V	Figure 6-8
PWM Switching – Light Load	HV_{DD} = 8 V/0 A	Figure 6-9
PWM Switching – Heavy Load (Source)	HV_{DD} = 8 V/500 mA	Figure 6-10
PWM Switching – Heavy Load (Sink)	HV_{DD} = 8 V/–500 mA	Figure 6-11
Load Transient Response	HV_{DD} = 3.3 V/–200 ~ +200 mA	Figure 6-12
Boost Converter - (V_{IN} = 12 V, L = 10 µH, C_{OUT} = 40 µF)		
Efficiency vs. Load Current	V_{DD} = 16 V	Figure 6-13
PWM Switching – Light Load	V_{DD} = 16 V/0 A	Figure 6-14
PWM Switching – Heavy Load	V_{DD} = 16 V/ 700 mA	Figure 6-15
Load Transient Response	V_{DD} = 16 V/ 200 ~ 550 mA	Figure 6-16
Positive Charge Pump - (V_{IN} = 12 V, C_{OUT} = 10 µF)		
Load Transient Response	V_{GH} = 26 V/ 10 ~ 60 mA	Figure 6-17
Negative Charge Pump - (V_{IN} = 12 V, C_{OUT} = 10 µF)		
Load Transient Response	V_{IN} = 12 V, V_{GL} = –5 V/ 10 ~ 50 mA	Figure 6-18
Temperature Compensation		
Voltage Adjustment - [–2°C ~ 25°C]	V_{GH_LT1} = 34 V, V_{GH_HT1} = 17 V V_{GH_LT2} = 27 V, V_{GH_HT2} = 24 V	Figure 6-19
Temperature Adjustment V_{GH_LT} = 28 V, V_{GH_HT} = 22 V	T°C Variation1: 2 °C ~ 18 °C T°C Variation2: 16 °C ~ 32 °C	Figure 6-20
VCOM Operationnal Amplifier		
VCOM Slew Rate	Gain = -4x, IN = VCOM_FB inverted	Figure 6-21
Sequencing		
Power On Sequencing	V_{IN} = 12 V, V_{LOGIC} = 3.3 V, V_{GL}= –5 V V_{DD}= 16 V, HV_{DD} = 8 V, V_{GH} = 26 V	Figure 6-22
Power On Sequencing V_{DD} dependency	V_{IN} = 12 V, V_{DD} = 16 V, V_{GMA1} = 14 V HV_{DD} = 8 V, V_{POS} = 6.5 V, V_{GMA6} = 2 V	Figure 6-23
Level Shifter - Peak Output Current		
CLKx	10 nF load	Figure 6-24
VST, RESET, ODD, EVEN, VGH_F, VGH_R		Figure 6-25
Level Shifter - Rise Time		
CLKx	47 Ω + 10 nF load	Figure 6-26
VST, RESET, ODD, EVEN, VGH_F, VGH_R		Figure 6-27
CLKx	150 pF load	Figure 6-28
VST, RESET, ODD, EVEN, VGH_F, VGH_R		Figure 6-29
Level Shifter - Fall Time		
CLKx	47 Ω + 10 nF load	Figure 6-30
VST, RESET, ODD, EVEN, VGH_F, VGH_R		Figure 6-31
CLKx	150 pF load	Figure 6-32
VST, RESET, ODD, EVEN, VGH_F, VGH_R		Figure 6-33

Table 6-1. Table of Graphs (continued)

PARAMETER	Conditions	Figure
Level Shifter - Sequencing		
Power On Sequencing	CLKx, V_{GL} = 28 V , V_{GL} = -5 V	Figure 6-34
Power Off Sequencing	CLKx, V_{GL} = 28 V , V_{GL} = -5 V	Figure 6-35

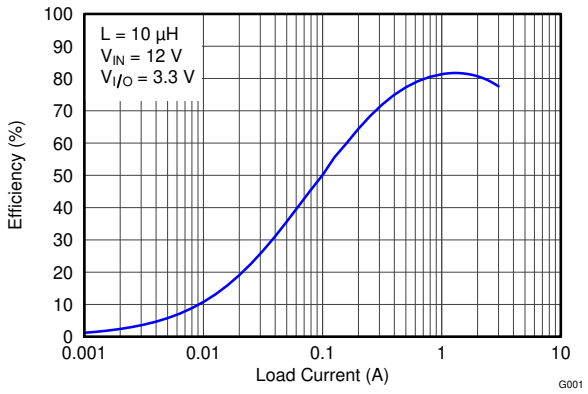


Figure 6-4. BUCK (V_{CC}) EFFICIENCY vs LOAD CURRENT

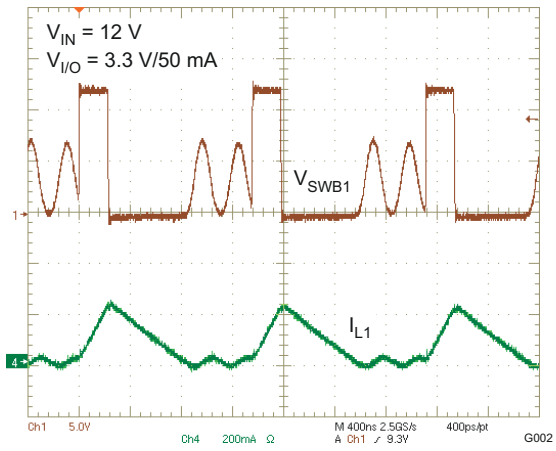


Figure 6-5. BUCK (V_{CC}) PWM SWITCHING – LIGHT LOAD

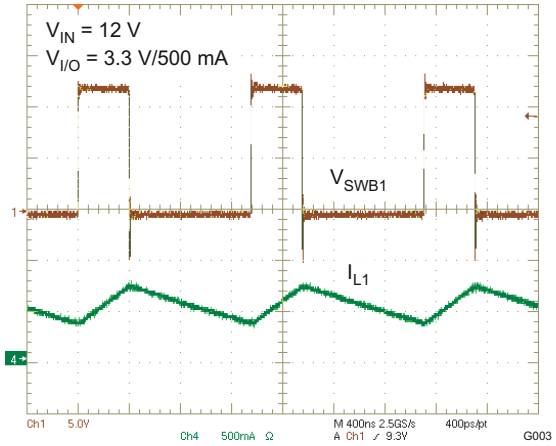


Figure 6-6. BUCK (V_{CC}) PWM SWITCHING – HEAVY LOAD

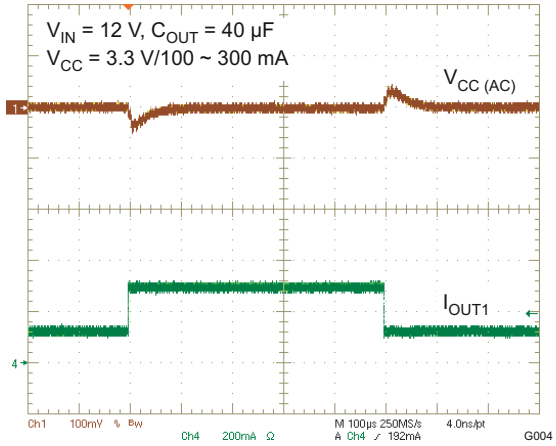


Figure 6-7. BUCK (V_{CC}) LOAD TRANSIENT RESPONSE

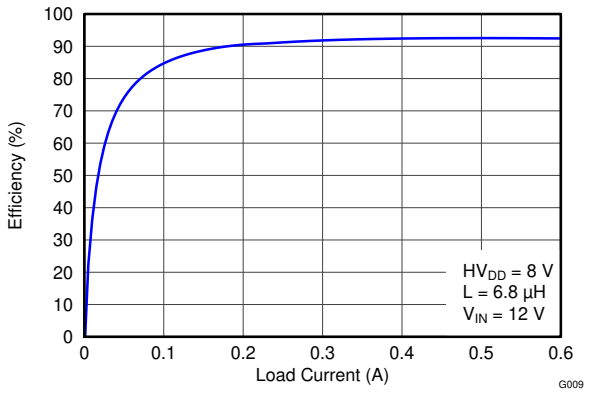


Figure 6-8. SYNCHRONOUS BUCK (HV_{DD}) EFFICIENCY vs LOAD CURRENT

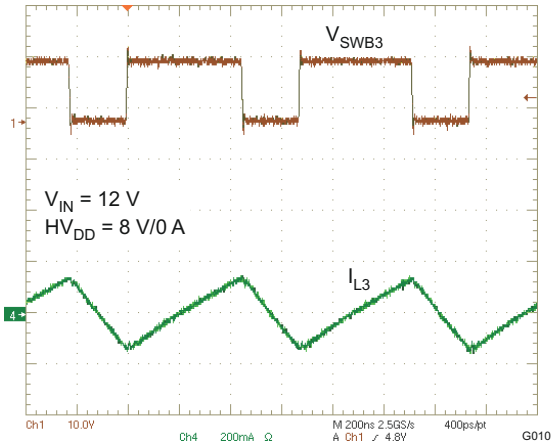


Figure 6-9. SYNCHRONOUS BUCK (HV_{DD}) PWM SWITCHING - LIGHT LOAD

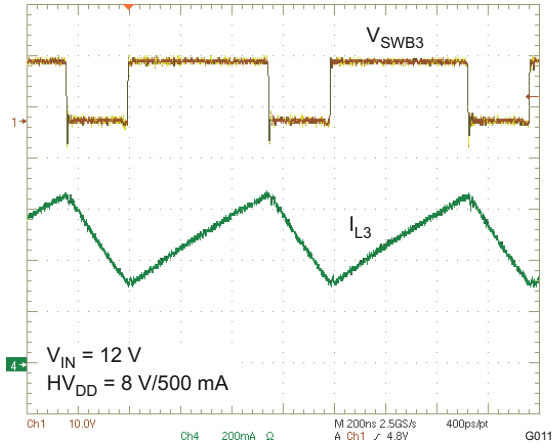


Figure 6-10. SYNCHRONOUS BUCK (HV_{DD}) PWM SWITCHING – HEAVY LOAD (SOURCE)

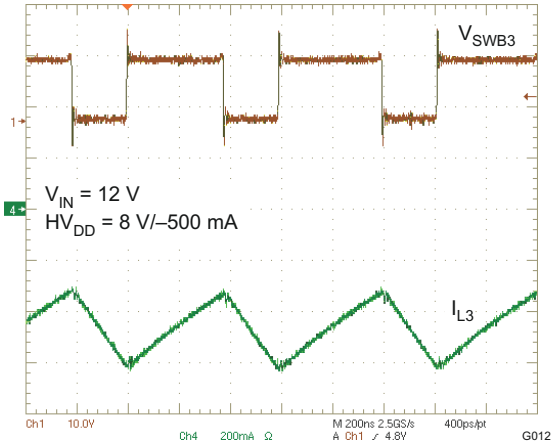


Figure 6-11. SYNCHRONOUS BUCK (HV_{DD}) PWM SWITCHING – HEAVY LOAD (SINK)

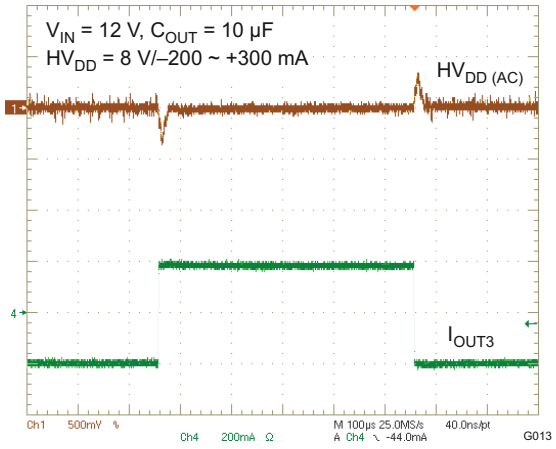


Figure 6-12. SYNCHRONOUS BUCK (HV_{DD}) LOAD TRANSIENT RESPONSE

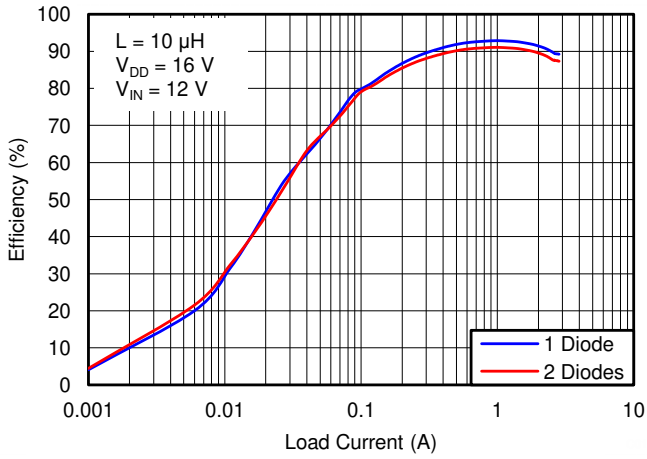


Figure 6-13. BOOST (V_{DD}) EFFICIENCY vs LOAD CURRENT

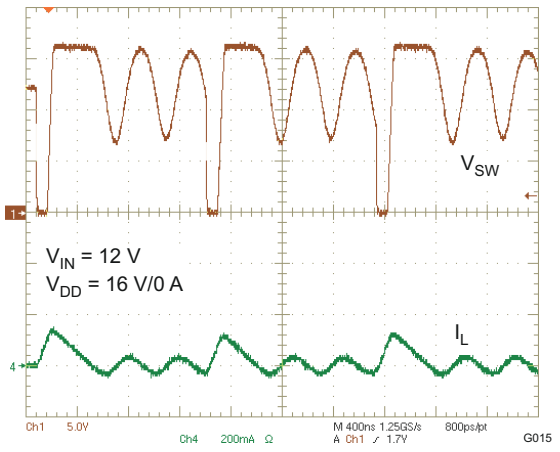


Figure 6-14. BOOST (V_{DD}) PWM SWITCHING – LIGHT LOAD

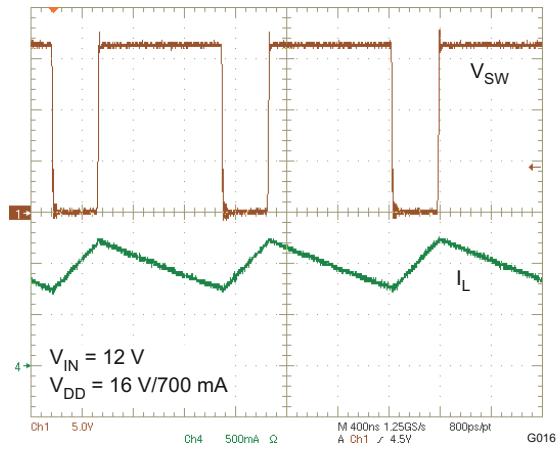


Figure 6-15. BOOST (V_{DD}) PWM SWITCHING – HEAVY LOAD

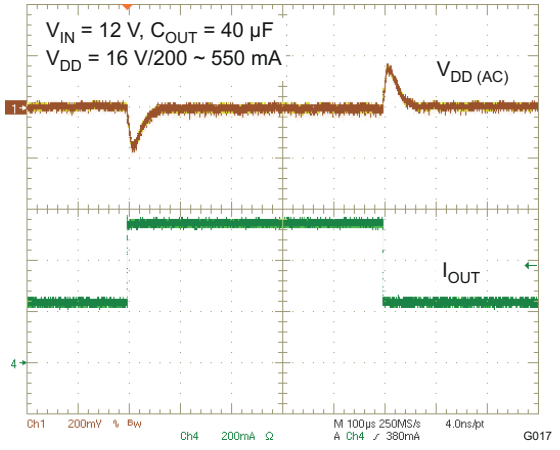


Figure 6-16. BOOST (V_{DD}) LOAD TRANSIENT RESPONSE

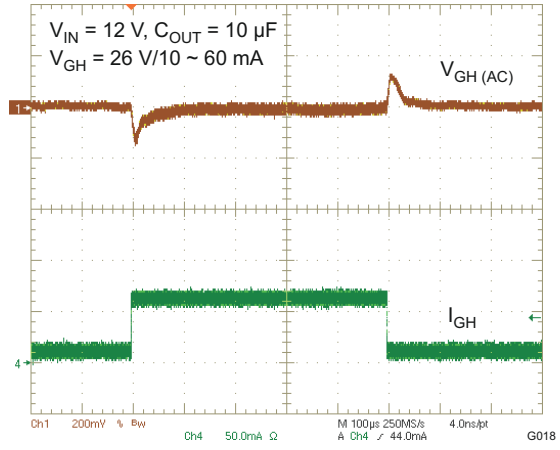


Figure 6-17. CPP (V_{GH}) LOAD TRANSIENT RESPONSE

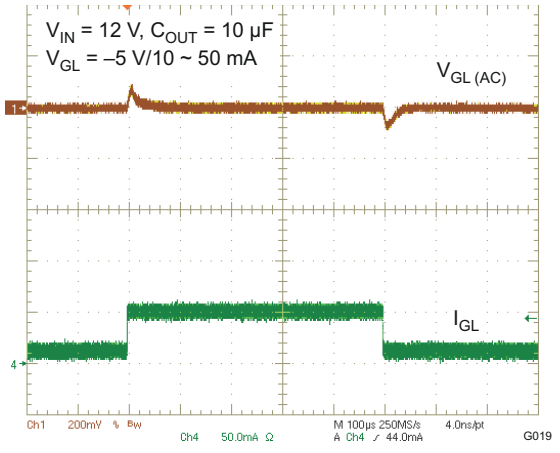


Figure 6-18. CPN (V_{GL}) LOAD TRANSIENT RESPONSE

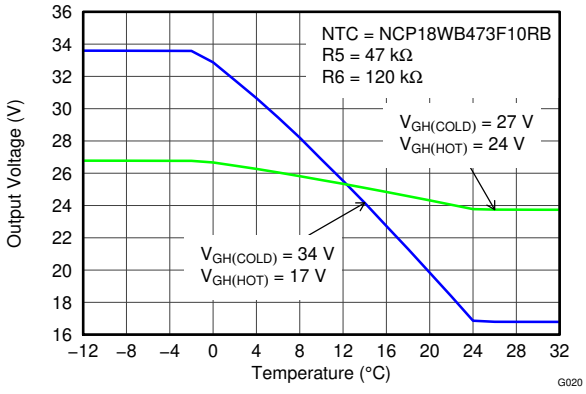


Figure 6-19. TEMPERATURE COMPENSATION VOLTAGE ADJUSTMENT

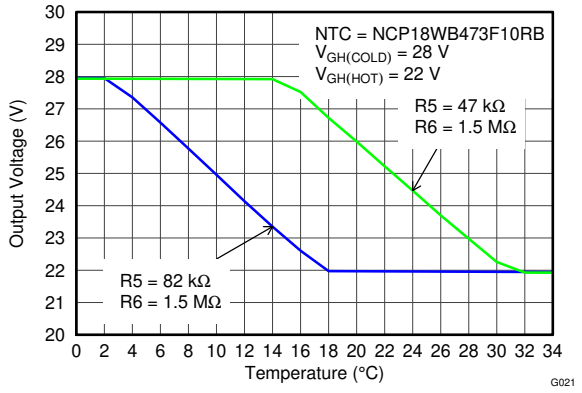


Figure 6-20. TEMPERATURE COMPENSATION VOLTAGE ADJUSTMENT

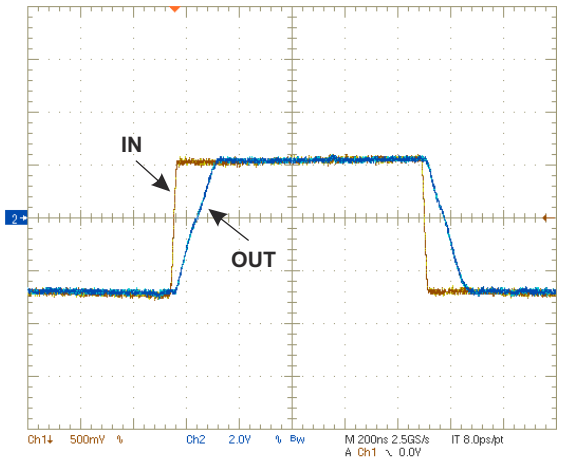


Figure 6-21. VCOM SLEW RATE

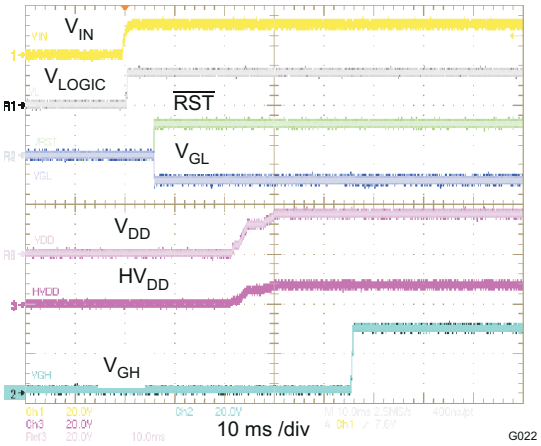


Figure 6-22. STARTUP SEQUENCING

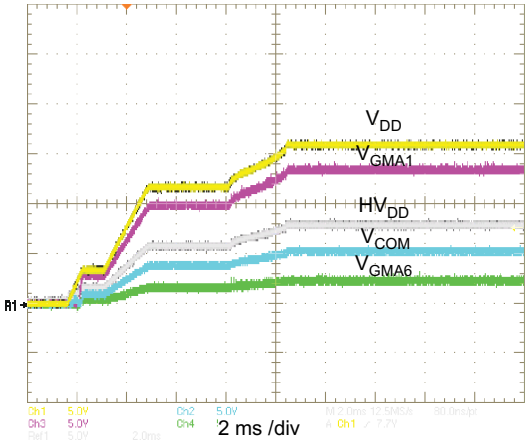


Figure 6-23. STARTUP SEQUENCING

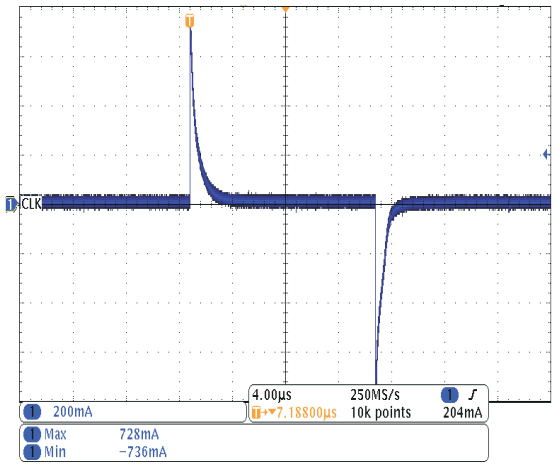


Figure 6-24. PEAK OUTPUT CURRENT - CLKs

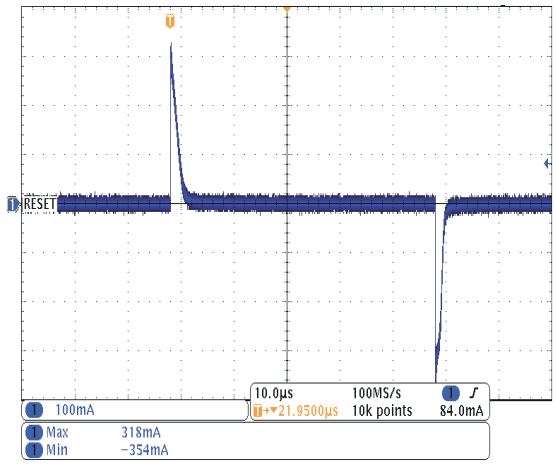


Figure 6-25. PEAK OUTPUT CURRENT - VST, RESET, etc.

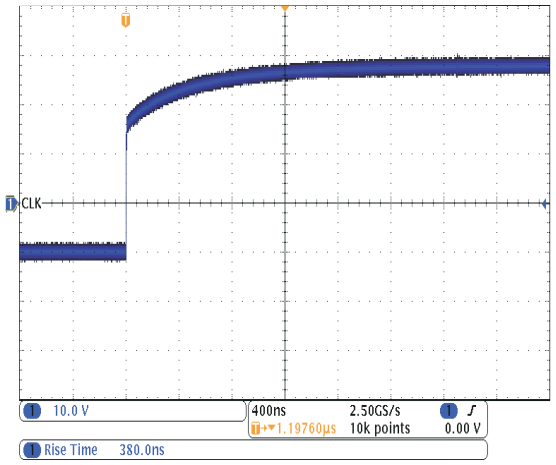


Figure 6-26. RISE TIME - CLKs

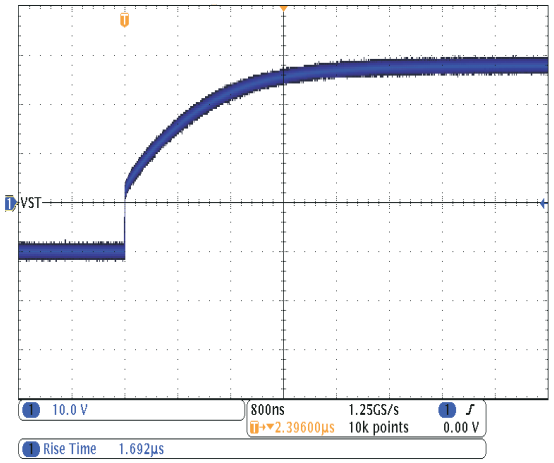


Figure 6-27. RISE TIME – VST, RESET, etc.

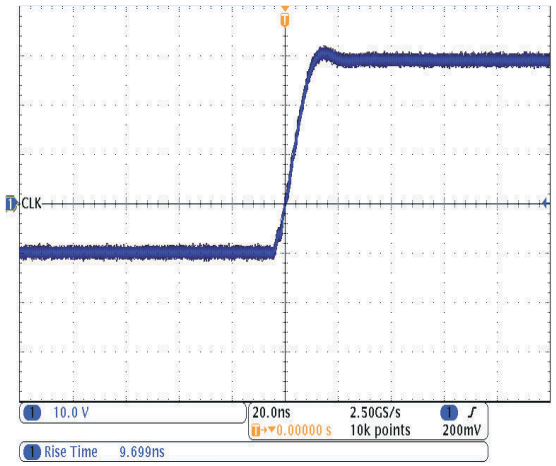


Figure 6-28. RISE TIME - CLKs

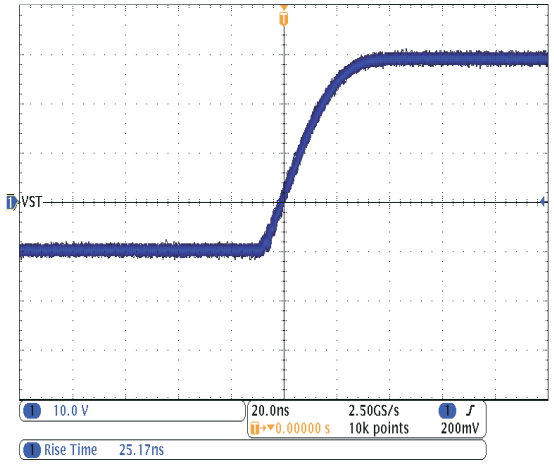


Figure 6-29. RISE TIME - VST, RESET, etc.

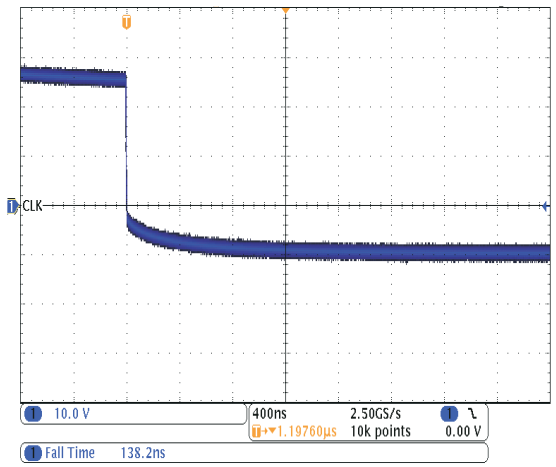


Figure 6-30. FALL TIME – CLKs

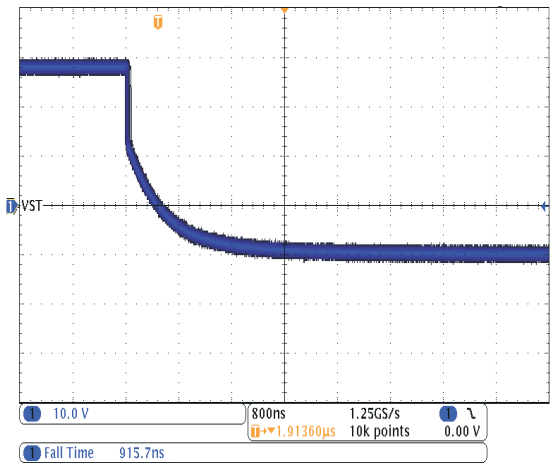


Figure 6-31. FALL TIME – VST, RESET, etc.

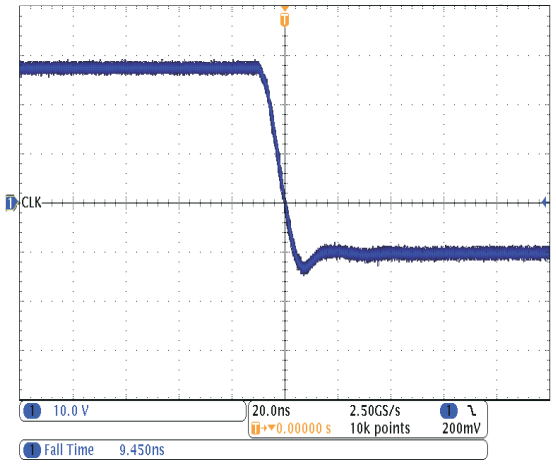


Figure 6-32. FALL TIME – CLKs

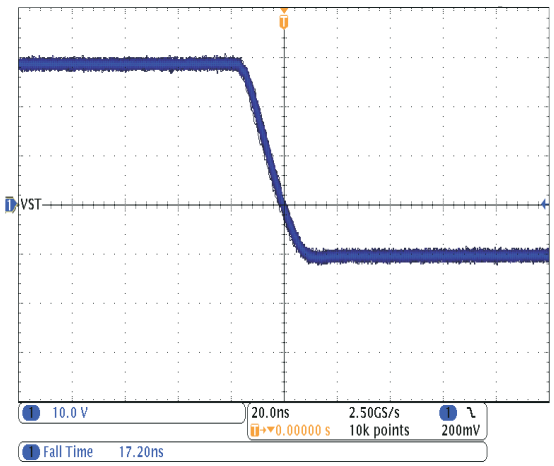


Figure 6-33. FALL TIME – VST, RESET, etc.

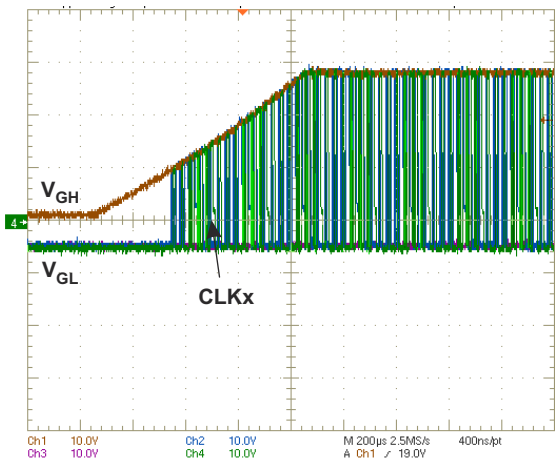


Figure 6-34. POWER UP SEQUENCE

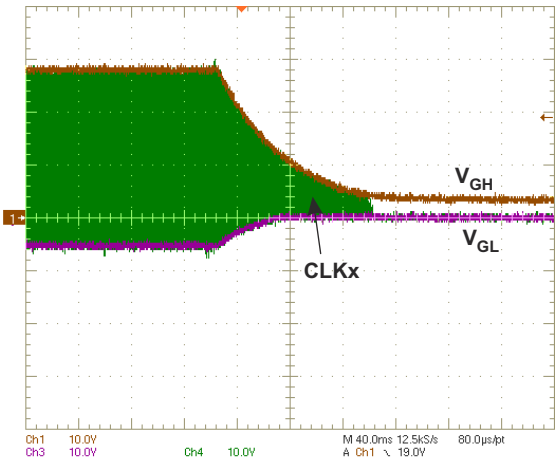


Figure 6-35. POWER DOWN SEQUENCE

7 DAC Range Summary

All outputs are programmable using a two-wire interface.

Boost Converter (V_{DD})

Output voltage selection: programmable with I^2C
Number of bits: 6
Output voltage range: 12.7V…19V
Step size: 100 mV

Boost Converter Frequency (V_{DD} Freq.)

Frequency Selection: programmable with I^2C
Number of bits: 1
Frequencies: 750 kHz, 1.5 MHz

Buck Converter (V_{CC})

Output voltage selection: programmable with I^2C
Number of bits: 4
Output voltage range: 1.6V…2.0V & 3.0V…3.6V
Step size: 100 mV

Buck Converter Frequency (V_{CC} Freq.)

Frequency Selection: programmable with I^2C
Number of bits: 1
Frequencies: 750 kHz, 1.5 MHz

Synchronous Buck Converter (HV_{DD})

Output voltage selection: not possible (V_{DD} tracking)
Number of bits: -
Output voltage range: $V_{DD}/2$
Step size: 50 mV

Positive Charge Pump Controller (V_{GH_LT} – low temperature)

Output voltage selection: programmable with I^2C
Number of bits: 4
Output voltage range: 19V…34V
Step size: 1 V

Positive Charge Pump Controller (V_{GL_HT} - high temperature)

Output voltage selection: programmable with I^2C
Number of bits: 4
Output voltage range: 17V…32V
Step size: 1 V

Negative Charge Pump (V_{GL})

Output voltage selection: programmable with I^2C
Number of bits: 4
Output voltage range: –1.8V…–8.1V
Step size: 100 mV

Gamma Buffer ($V_{GMA1,2,3}$) - (V_{DD} dependency)

Output voltage selection: programmable with I^2C
Number of bits: 9
Output voltage range: $V_{DD}/2…V_{DD}$ (512 steps)
Step size: $V_{DD}/1023$

Gamma Buffer ($V_{GMA4,5,6}$) - (V_{DD} dependency)

Output voltage selection: programmable with I^2C
Number of bits: 9
Output voltage range: $0V…V_{DD}/2$ (512 steps)
Step size: $V_{DD}/1-23$

Vcom Reference (V_{POS}) - (V_{DD} dependency)

Output voltage selection: programmable with I^2C
Number of bits: 9
Output voltage range 1: $(V_{DD}/1023)*250V$ ... $(V_{DD}/1023)*640V$ (391 steps)
Output voltage range 2: $(V_{DD}/1023)*310V$ ... $(V_{DD}/1023)*520V$ (211 steps)
Step size: $V_{DD}/1023$

Vcom Gain

Gain level selection: programmable with I^2C
Number of bits: 3
Gain levels: Buffer, –1x,–2x,–3x, –4x, –5x

Vcom Temperature Compensation Offset (V_{COM_OFFSET}) - (V_{POS} dependency)

Output offset: programmable with I^2C
Number of bits: 4
Output voltage range: $0V…(V_{DD}/1023)*30V$ (16 steps)
Gain levels: Buffer, –1x,–2x,–3x, –4x, –5x

Vcom Temperature Change Range

Range selection: programmable with I^2C
Number of bits: 2
Temperature ranges: 50°C ~ 60°C, 55°C ~ 65°C, 60°C ~ 70°C, 65°C ~ 75°C

7.1 Sequencing

The power-up sequence delays are programmable with a I^2C. DLY0 can be set per steps of 3 ms, up to 24 ms. DLY1, DLY2 and DLY3 can be set per steps of 5 ms, up to 35 ms.

DLY0

Number of bits: 3
Timing delay range: 3ms…24ms (± 20% accuracy)

DLY1, 2, 3

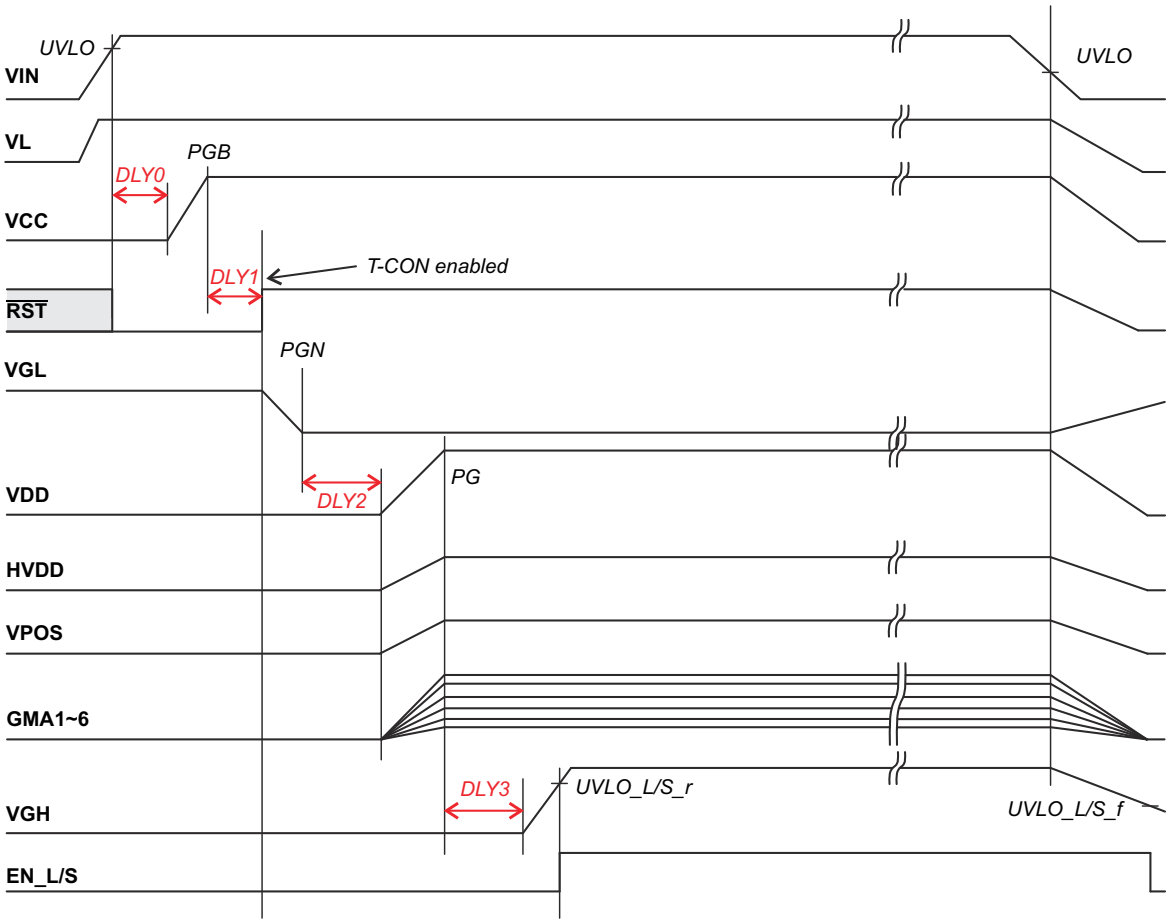
Number of bits: 3
Timing delay range: 0ms…35ms (± 20% accuracy)

7.2 Power-Up

1. When AV_{IN} > 8.6 V the device is enabled, V_L goes into regulation and the $\overline{RST}$ signal is set 'low' **and** DLY0 starts.
2. When the DLY0 has passed, the buck converter (V_{CC}) starts up.
3. When PGB is reached, DLY1 starts.
4. When DLY1 has passed, $\overline{RST}$ is released **and** the negative charge pump controller (V_{GL}) starts.
5. When PGN is reached **and** DLY2 has passed, the boost converter (V_{DD}) **and** the synchronous buck converter (HV_{DD}) start. The Gamma Buffer outputs as well as the V_{COM} output rise at a ratio metric rate of V_{DD}.
6. When PG is reached **and** DLY3 has passed, the positive charge pump controller (V_{GH}) starts.
7. When V_{GH} > 9.2 V, the Level Shifter block is enabled.

7.3 Power-Down

1. When V_{IN} falls down below the UVLO threshold, all blocks are disabled and discharge at a rate driven by the output load and the output capacitors.
2. When V_{GH} falls below the UVLO_L/S threshold, the Level Shifter block is disabled.


UVLO
VIN
VL
PGB
DLY0
VCC
DLY1
T-CON enabled
RST
PGN
VGL
DLY2
PG
VDD
HVDD
VPOS
GMA1~6
DLY3
UVLO_L/S_r
VGH
EN_L/S
UVLO
UVLO_L/S_f

8 Detailed Description

8.1 Boost Converter (V_{DD})

The non-synchronous boost converter uses a current mode topology and operates at a fixed frequency of 750 kHz or 1.5 MHz selectable with EERPOM bit. A typical application circuit is shown in Figure 8-18. The external compensation allows designers to optimize the performance for individual applications, and is easily implemented by connecting a suitable capacitor/resistor network between the COMP pin and AGND (see design procedure section for more details).

8.1.1 Enable Signal (DLY2)

The boost converter is enabled when the power good signal from the negative charge pump controller (V_{GL}) is asserted and the programmed DLY2 has passed (see the *Appendix* section to set DLY2 timing).

8.1.2 Boost Converter Operation

The boost operates either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on the load current. The switch node waveforms for CCM and DCM operation are shown in Figure 6-5 and Figure 6-6. Note that the ringing seen during DCM operation (at light load) occurs because of parasitic capacitance in the PCB layout and is normal for DCM operation. There is very little energy contained in the ringing waveform and it does not significantly affect EMI performance.

8.1.3 Startup (Boost Converter)

The startup of the boost converter block operates in two steps:

1. **Input-to-output isolation switch (IsoFET)**
   As soon as the internal enable signal of the boost converter is activated, the isolation switch is slowly turned on, ramping up smoothly the current flowing from V_{IN} into the output capacitors. The startup current is limited to 200 mA typically until V_{SWO} > 3.5 V (short-circuit condition), and increases linearly with the output voltage. Once V_{SWO} gets close to V_{SWI}, the isolation switch is fully turned on and the boost converter starts switching. The soft-start function is also enabled.
2. **Soft-start (SS)**
   To minimize the inrush current during start-up an external capacitor connected to the soft-start pin SS is used to slowly ramp up the internal current limit of the boost converter. It is charged with a constant current of typically 10 µA. The inductor peak current limit is proportional to the SS voltage and the maximum load current is available after the soft-start is completed (V_{SS} = 0.8 V) or V_{DD} has reached its Power Good value (90% of its nominal voltage). The larger the SS capacitor, the slower the ramp of the current limit and the longer the soft-start time. A 100-nF capacitor is usually sufficient for most applications. When V_{IN} decreases below the undervoltage lockout threshold, the soft-start capacitor is discharged to ground.

8.1.4 Protections (Boost Converter)

The boost converter is protected against potentially damaging conditions such as overvoltage and short circuits.

1. **Short-Circuit Protection**
   The boost converter integrates a short-circuit protection circuit to prevent the inductor or the rectifier diode from overheating when the output rail is shorted to GND. If the boost output is shorted to GND and the voltage on SWO drops below V_{IN} - 0.5 V, the boost converter shuts down and the input-to-output isolation is turned-off. Only when the SWO voltage drops below 2 V typically, the switch turns on again and limits the current to 200 mA typically (start-up behavior). The soft-start capacitor is also discharged to ground.
2. **Overvoltage Protection**
   The boost converter integrates an overvoltage protection. If the output voltage V_{DD} exceeds the OVP threshold of 20.3 V typically , the boost converter stops switching. The output voltage will drop down by the hysteresis and the boost converter will autonomously recover and switch again.

Note

The boost converter stops switching while the positive charge pump is in a short circuit condition. This condition is not latched and the boost converter autonomously resumes normal operation once the short circuit condition has been removed from the positive charge pump.

8.1.5 Setting the Output Voltage V_{DD}

The output voltage of the boost converter is programmable via a two-wire interface between 12.7 V and 19 V with a 6-bit resolution. See the *Appendix* section to set the V_{DD} voltage.

8.2 Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency number from the provided efficiency curves at the application's maximum load or to use a worst case assumption for the expected efficiency, e.g., 85%.

1. Duty Cycle:
$$D = 1 - \frac{V_{IN\_min} \times \eta}{V_S}$$
2. Inductor ripple current:
$$\Delta I_L = \frac{V_{IN\_min} \times D}{f_{OSC} \times L}$$

3. Maximum output current: $$I_{OUT\_max} = \left(I_{LIM\_min} - \frac{\Delta I_L}{2} \right) \times (1 - D)$$

4. Peak switch current of the application: $$I_{SWPEAK} = \frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2}$$

η = Estimated boost converter efficiency (use the number from the efficiency plots or 85% as an estimation)
f_{OSC} = Boost converter switching frequency (750 kHz)
L = Selected inductor value for the boost converter (see the Inductor Selection section)
I_{SWPEAK} = Boost converter switch current at the desired output current (must be < I_{LIM_min} = 3.5 A)
ΔI_L = Inductor peak-to-peak ripple current

The peak switch current is the current that the integrated switch, the inductor and the external Schottky diode have to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest.

8.2.1 Inductor Selection (Boost Converter)

Saturation current: the inductor must handle the maximum peak current (I_{L_SAT} > I_{SWPEAK}, or I_{L_SAT} > I_{LIM_max} as conservative approach)

DC Resistance: the lower the DCR, the lower the losses

Inductor value: with a frequency of 750 kHz, the recommended value is 22 µH. With 1.5 MHz, 10 µH are recommended. The higher the inductor value, the lower the inductor ripple and output voltage ripple but the slower the transient response.

Table 8-1. Inductor Selection Boost / Buck 1

L (µH)	SUPPLIER	COMPONENT CODE	SIZE (L x W x H mm)	DCR TYP (mΩ)	I_{SAT} (A)
10	Sumida	CDRH8D43NP-100N	8.3 x 8.3 x 4.5	29	4
10	Murata	LQH6PPN100M43K	6.0 x 6.0 x 4.3	53	2.6
22	Sumida	CD105NP-100M	10.4 x 9.4 x 5.8	60	2.6
22	Sumida	CDRH129-220M	12.5 x 12.5 x 10	23	5

8.2.2 Rectifier Diode Selection (Boost Converter)

Diode type: Schottky type for better efficiency

Reverse voltage: V_R of the diode must block V_{OVP} voltage (20 V recommended)

Forward current: the diode's averaged rectified forward current I_F must handle the output current since I_F = I_{OUT} (2A recommended as conservative approach, 1A sufficient for lower output current).

Thermal characteristics: the diode must be chosen so that it can dissipate the power (P_D = I_F × V_F, 500 mW should be sufficient for most of the applications)

Table 8-2. Rectifier Diode Selection Boost / Buck 1

PART NUMBER	V_R / I_{AVG}	V_F	$R_{\theta JA}$	SIZE	COMPONENT SUPPLIER
MBRS320	20V / 3A	0.44V at 3A	46°C/W	SMC	International Rectifier
SL22	20V / 2A	0.44V at 2A	75°C/W	SMB	Vishay Semiconductor
SS22	20V / 2A	0.50V at 2A	75°C/W	SMB	Fairchild Semiconductor

8.2.3 Compensation (COMP)

The regulation loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. The compensation capacitor will adjust the low frequency gain and the resistor value will adjust the high frequency gain. Lower output voltages require a higher gain and therefore a lower compensation capacitor value. A good start, that will work for the majority of

the applications is R_{COMP} = 33 kΩ and C_{COMP} = 1 nF. In the case where a 22 uH inductor is used, R_{COMP} = 22 kΩ and C_{COMP} = 1 nF are recommended.

8.2.4 Input Capacitor Selection

For good input voltage filtering low ESR ceramic capacitors are recommended. TPS65175/A has an analog input AVIN. A 1-µF bypass capacitor is required as close as possible from AVIN to GND.

Two 10-µF (or one 22-µF) ceramic input capacitors are sufficient for most applications. For better input voltage filtering this value can be increased. Refer to the *Recommended Operation Conditions* table, Table 8-3 and the *Typical Application* section for input capacitor recommendations.

8.2.5 Output Capacitor Selection

For best output voltage filtering a low ESR output capacitor is recommended. Typically, four 10-µF (or two 22-µF) ceramic output capacitors work for most of the applications. Higher capacitor values can be used to improve the load transient response. *A 10 µF capacitor is also required between the rectifier diode and the SWI pin* (Refer to the *Recommended Operation Conditions* table, Table 8-3 and the *Typical Application* section for output capacitor recommendations).

Table 8-3. Input and Output Capacitor Selection Boost / Buck 1

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMPONENT CODE	COMMENTS
1µF/0603	16V	Taiyo Yuden	EMK107BJ105KA	AVIN bypass
10µF/1206	16V	Taiyo Yuden	EMK212BJ106KG	C_{IN}
10µF/1206	25V	Taiyo Yuden	TMK316BJ106KL	C_{OUT}
22µF/1210	25V	Murata	GRM32ER61E226KE15	C_{IN} / C_{OUT}

To calculate the output voltage ripple, the following equations can be used:

$$\Delta V_C = \frac{V_{DD} - V_{IN}}{V_{DD} \times f_{OSC}} \times \frac{I_{OUT}}{C_{OUT}} \qquad \Delta V_{C\_ESR} = I_{SWPEAK} \times R_{C\_ESR} \tag{1}$$

ΔV_{C_ESR} can be neglected in many cases since ceramic capacitors provide very low ESR.

8.2.6 DCM Mode

The converter being non-synchonous, if the output load is low enough to make the inductor completely discharge (the valley current ripple of the inductor reach 0A), the converter will operate in DCM (Discontinuous Conduction Mode) as shown in Figure 6-14.

8.3 Buck Converter (V_{CC})

The buck converter (step-down) used in TPS65175/A is a non-synchronous type current mode control that runs at a fixed frequency of 750kHz or 1.5MHz selectable with EERPOM bit. The converter features integrated soft-start, bootstrap, and compensation circuits to minimize external component count.

8.3.1 Enable Signal (UVLO)

The buck converter is enabled when the VIN voltage exceeds the UVLO threshold of 8.3 V typically.

8.3.2 Buck converter Operation

The buck 1 operates in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on the load current. The switch node waveforms for CCM and DCM operation are shown in Figure 6-5 and Figure 6-6. Note that the ringing seen during DCM operation (at light load) occurs because of parasitic capacitance in the PCB layout and is normal for DCM operation. There is very little energy contained in the ringing waveform and it does not significantly affect EMI performance.

The buck converter uses a *skip* mode to regulate V_{CC} at very low load currents. This mode allows the converter to maintain its output at the required voltage while still meeting the requirement of a *minimum on time*. During skip mode, the buck converter switches for a few cycles, then stops switching for a few cycles, and then starts switching again and so on, for as long as the output current is below the skip mode threshold. Output voltage ripple can be a little higher during skip mode.

8.3.3 Startup and Short Circuit Protection (Buck Converter)

The buck converter is limiting its switching frequency when its output voltage V_{CC} is below a certain threshold (f_{SWB} = 1/4 × fosc for $V_{FB\_internal}$ < 400mV and f_{SWB} = ½ × fosc for $V_{FB\_internal}$ < 800mV). This feature avoids run away of the inductor current in case of short circuit and helps smoothing the buck converter startup as well.

8.3.4 Setting the Output Voltage V_{CC}

The output voltage of the buck converter is programmable via a two-wire interface between 1.6 V & 2.0V and 3.0 V & 3.6 V with a 6-bit resolution. A minimum output load of 1 mA is required for proper regulation. See the *Appendix* section to set the V_{CC} voltage.

8.4 Buck Converter Design Procedure

1. Duty Cycle: $$D = \frac{V_{CC}}{V_{IN} \times \eta}$$
2. Inductor ripple current: $$\Delta I_L = \frac{(V_{IN\_max} - V_{CC}) \times D}{f_{OSC} \times L}$$
3. Maximum output current: $$I_{CC\_max} = I_{LIM\_min} - \frac{\Delta I_L}{2}$$
4. Peak switch current: $$I_{SWPEAK} = I_{CC\_max} + \frac{\Delta I_L}{2}$$

η = Estimated buck converter efficiency (use the number from the efficiency plots or 85% as an estimation)
f_{OSC} = Buck converter switching frequency (750 kHz)
L = Selected inductor value for the boost converter (see the Inductor Selection section)
I_{SWPEAK} = Buck converter switch current (must be < I_{LIM_min} = 2.6 A)
ΔI_L = Inductor peak-to-peak ripple current

8.4.1 Inductor Selection (Buck Converter)

Refer to the boost converter *Inductor Selection*.

Inductor value: as for the boost converter, the buck converter is designed to work with an inductor range as 10 µH ≤ L ≤ 22 µH.

8.4.2 Rectifier Diode Selection (Buck Converter)

Refer to the boost converter rectifier *Diode Rectifier Selection*.

8.4.3 Input Capacitor Selection (Buck Converter)

Two 10-µF (or one 22-µF) ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering this value can be increased. Refer to the *Recommended Operation Conditions* table, Table 8-3 and the *Typical Application* section for input capacitor recommendations.

8.4.4 Output Capacitor Selection (Buck Converter)

For best output voltage filtering a low ESR output capacitor is recommended. Typically, four 10-µF (or two 22-µF) ceramic output capacitors work for most of the applications. Higher capacitor values can be used to improve the load transient response. Refer to the *Recommended Operation Conditions* table, Table 8-3 and the *Typical Application* section for input capacitor recommendations.

8.4.5 DCM Mode

The converter being non-synchonous, if the output load is low enough to make the inductor completely discharge (the valley current ripple of the inductor reach 0A), the converter will operate in DCM (Discontinuous Conduction Mode) as shown in Figure 6-5.

8.5 Synchronous Buck Converter (HV_{DD})

The TPS65175/A integrates also a synchronous buck converter (step-down) that uses a PWM able to sink and source current up to 500mA.

8.5.1 Enable Signal (DLY2)

The synchronous buck converter is enabled together with the boost converter when the power good of the negative charge pump (VGL) is asserted and that the DLY2 has passed. See the *Appendix* section to set the DLY2 timing.

8.5.2 Startup and Short Circuit Protection (Synchronous Buck Converter)

The synchronous buck converter output voltage tracks the boost converter output voltage at a ratio metric pace during startup. To prevent Source Driver damages, the TPS65175/A implements a protection feature that disables both the boost (V_{DD}) and the synchronous buck (HV_{DD}) converters when short-circuits or over voltages occur on one of the two converters. The converters will autonomously recover after the failure has gone.

8.5.3 Setting the output voltage HVDD

The output voltage of the synchronous buck converter is programmable via a two-wire interface between 6.4 V and 9.55 V with a 6-bit resolution. See the *Appendix* section to set the HV_{DD} voltage.

8.6 Synchronous Buck Converter Design Procedure

1. Duty Cycle: $$D = \frac{HV_{DD}}{V_{IN} \times \eta}$$
2. Inductor ripple current: $$\Delta I_L = \frac{1.85e^{-6}}{L}$$
3. Maximum output current: $$I_{HVDD\_max} = I_{LIM\_min} - \frac{\Delta I_L}{2}$$
4. Peak switch current: $$I_{SWPEAK} = I_{HVDD\_max} + \frac{\Delta I_L}{2}$$

η = Estimated synchronous buck converter efficiency (use the number from the efficiency plots or 80% as an estimation)

f = Synchronous buck converter switching frequency $$f_{SW3} = \frac{HV_{DD} \times (1\text{-}D)}{1.85e^{-6}}$$

L = Selected inductor value for the synchronous buck converter (in µH – for value see the *Inductor Selection* section)
I_{SWPEAK} = Synchronous buck converter switch current (must be < I_{LIM_min} = 0.8 A)
ΔI_L = Inductor peak-to-peak ripple current

The peak switch current is the steady state current that the integrated switches and the inductor have to be able to handle.

8.6.1 Inductor Selection (Synchronous Buck Converter)

Refer to the boost converter *Inductor Selection* section, for more details.

Inductor value: the synchronous buck converter is designed to work with small inductors in the following range: 4.7µH ≤ L ≤ 10 µH. The synchronous buck converter is optimized to work with 6.8 µH.

Table 8-4. Inductor Selection Buck 3 (Chip Inductors)

L (µH)	SUPPLIER	COMPONENT CODE	SIZE (LxWxH mm)	DCR TYP (mΩ)	I_{SAT} (A)
4.7, 6.8, 10	Taiyo Yuden	CBC2518T series	2.5 x 1.8 x 1.8	260 ~ 460	480 ~ 680
4.7, 6.8, 10	Taiyo Yuden	CBC3225T series	3.2 x 2.5 x 2.5	100 ~ 133	900 ~ 1250

8.6.2 Input Capacitor Selection

Typically, one 10-µF ceramic capacitor on PVINH pin is recommended. For better input voltage filtering this value can be increased. Refer to the *Recommended Operation Conditions* table, Table 8-3 and the *Typical Application* section for input capacitor recommendations.

8.6.3 Output Capacitor Selection

Typically, one 10-µF ceramic output capacitor works for most of the applications. Refer to the *Recommended Operation Conditions* table, Table 8-3 and the *Typical Application* section for output capacitor recommendations.

8.7 Positive Charge Pump Controller (V_{GH}) and Temperature Compensation

The positive charge pump (CPP) flying capacitor is driven from SWP pin with an intergated 50% duty cycle push-pull stage. The regulation is achieved using an external PNP transistor controlled by the CTRLP pin. The TPS65175/A also includes a temperature compensation feature that controls the output voltage depending on the temperature sense by an external Negative Thermistor (NTC).

8.7.1 Enable Signal (DLY3)

The positive charge pump controller as well as the push-pull stage on SWP pin are enabled when the boost and synchronous buck converters' power good signals are asserted and that the DLY3 has passed. See the *Appendix* section to set the DLY3 timing.

8.7.2 Positive Charge Pump Controller Operation

During normal operation, the TPS65175/A is able to provide up to 1.5 mA of base current typically and is designed to work best with transistors whose DC gain (h_{FE}) is between 100 and 300. The charge pump is protected against short-circuits on its output, which are detected for voltages below 1 V. During short-circuit mode, the base current available from the CTRLP pin is limited to 60 µA typically. Note that if a short-circuit is detected during normal operation, the boost converter switching activity is also halted until V_{GH} is above 1 V. Typical application circuits are shown in Figure 8-1.

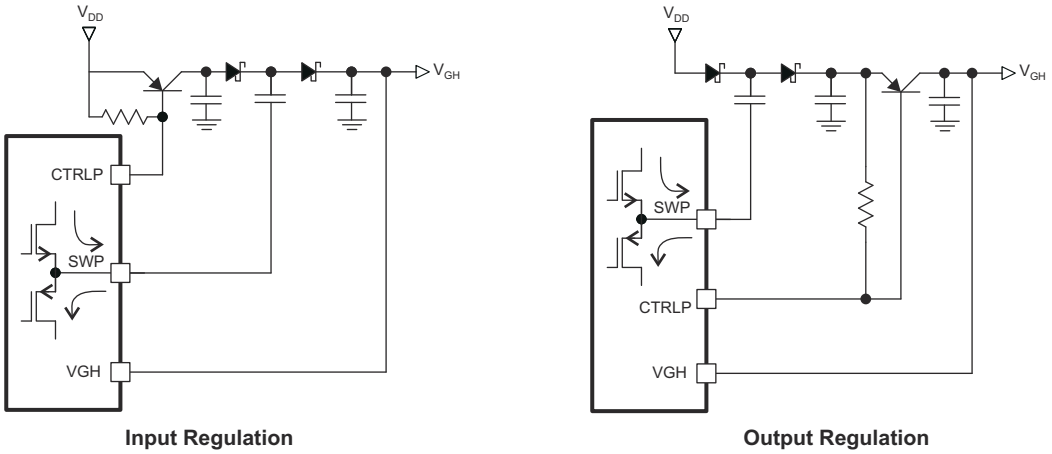


Figure 8-1. Positive Charge Pump Application Circuits

8.8 Positive Charge Pump Design Procedure

The regulation of the positive charge pump (CPP) can be done either on the input (transistor placed between V_{DD} and the diode) or on the output. For better regulation and fewer interactions between the boost converter and the CPP controller, it is recommended to place the transistor on the output. During startup, the inrush current is limited by the SWP push-pull stage that limits the current to 300 mA typically. For proper operation, it is recommended to have a headroom ($2xV_{DD}$-$2xV_{DIODE}$-V_{GH}) of 1 V minimum.

8.8.1 Diodes selection (CPP)

Small-signal diodes can be used for most low current applications (< 50 mA) and higher rated diodes for higher power applications. The average current through the diode is equal to the output current, so that the power dissipated in the diode is given by: $P_D = I_{GH} \times V_F$

The peak current through the diode occurs during start-up for a few cycles may reach the current limit of the push-pull stage (500 mA max.). However, this condition typically lasts for < 1 ms and can be tolerated by many diodes whose repetitive current rating is much lower. The diodes' reverse voltage rating should be equal to $2 \times V_{DD}$.

Table 8-5. Positive Charge Pump Diode Selection

PART NUMBER	I_{AVG}	I_{PK}	V_R	V_F	COMPONENT SUPPLIER
BAV99W	150mA	1A for 1ms	75V	1V at 50mA	NXP
BAT54S	200mA	600mA for 1s	30V	0.8V at 100mA	Fairchild Semiconductor
MBR0540	500mA	5.5A for 8ms	40V	0.51 at 500mA	Fairchild Semiconductor

8.8.2 Capacitors Selection (CPP)

Flying capacitors

A flying capacitor in the range 100 nF to 1 µF is suitable for most applications. Larger values experience a smaller voltage drop by the end of each switching cycle, and allow higher output voltages and/or currents to be achieved. Smaller values tend to be physically smaller and a bit cheaper. For best performance, it is recommended to include a resistor of a few ohms (1 Ω is a good value to start with) in series with the flying capacitor to limited peak currents occurring at the instant of switching.

Storage capacitors

For lowest output voltage ripple, low-ESR ceramic capacitors are recommended. The actual value is not critical and 1 µF to 10 µF is suitable for most applications. Larger capacitors provide better performance in applications where large load transient currents are present.

Transistor placed on the input (Figure 8-1)
A collector capacitor is required. A range of 100 nF to 1µF is suitable for most applications. Larger values are more suitable for high current applications but can affect stability if they are too big.

Transistor placed on the output (Figure 8-1)
An emitter capacitor is required. A range of 1µF to 10 µF is suitable for most applications. A smaller ratio between the emitter capacitor and the output capacitor is better for startup reason. A combination of C_{OUT} = 4.7 µF, C_{FLY} = 220 nF, (and $C_{EMITTER}$ = 4.7 µF) is a good starting point for most applications (the final values can be optimized on a case-by-case basis if necessary).

8.8.3 Selecting the PNP Transistor (CPP)

The PNP transistor used to regulate VGH should have a DC gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump's output current. The transistor should also be able to withstand voltages up to 2×V_{DD} across its collector-emitter (V_{CE}) – in the case where the CPP operates in doubler mode.

The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design. The power dissipated in the transistor is given by the following equation:

The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design. The power dissipated in the transistor is given by the following equation:

$$P_Q = \left[(2 \times V_{DD}) - (2 \times V_F) - V_{GH} \right] \times I_{GH} \quad (2)$$

I_{GH} = Mean output current on V_{GH}
V_F = Diode forward voltage

A pull-up resistor is also required between the transistor's base and emitter. The value of this resistor is not critical, but it should be large enough not to divert significant current away from the base of the transistor. A value of 100 kΩ is suitable for most applications.

8.8.4 Positive Charge Pump Protection

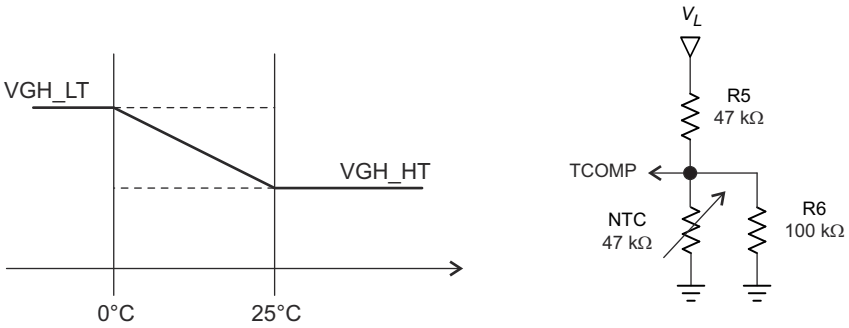
The TPS65175/A contains a circuit to protect the CPP against short circuits on its output. A short circuit condition is detected as long as the VGH voltage is below 1 V. The base current is then limited to 55 µA typically.

8.9 VGH Temperature Compensation

By connecting a fixed-value thermistor between [TCOMP and GND] and a fixed-value pull-up resistor between [VL and TCOMP], the V_{GH} voltage will vary from a given V_{GH_LT} voltage below a pre-defined (by external resistors) 'low' temperature to a lower voltage defined by V_{GH_HT} for 'high' temperatures (also set by the same external resistors). The user has to provide V_{GH_LT} and V_{GH_HT}.

Note

The internal temperature compensation system for VGH is made to work only with 47 kΩ NTC part number **NCP18WB473F10RB**. The other resistors could possibly be adjusted to match other temperatures but would affect the P-Vcom temperature compensation.



8.9.1 Setting the output voltage V_{GH_LT} and V_{GH_HT}

The output voltage of the positive charge pump is programmable via a two-wire interface between 19 V and 34 V with a 4-bit resolution for V_{GH_LT}, and between 17 V and 32 V with a 4-bit resolution for V_{GH_HT}. See the *Appendix* section to set the V_{GH_LT} and V_{GH_HT} voltage.

Note

In the case where $V_{GH\_LT} \leq V_{GH\_HT}$, whatever the temperature is, the output voltage will be V_{GH_HT}.

8.10 Negative Charge Pump (V_{GL})

The negative charge pump (CPN) flying capacitor is driven from SWN pin with an intergated 50% duty cycle push-pull stage. The regulation is achieved using an external NPN transistor controlled by the CTRLN pin. The IC is optimized for use with transistors having a DC gain (h_{FE}) in the range 100 to 300; however, it is possible to use transistors outside this range, depending on the application requirements. A typical application circuit is shown in Figure 8-2.

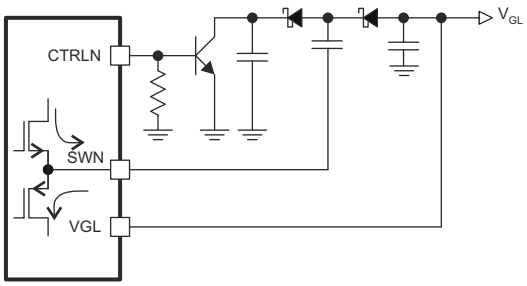


Figure 8-2. Negative Charge Pump Application Circuit

8.10.1 Enable Signal (DLY1)

The negative charge pump controller as well as the push-pull stage on SWN pin are enabled when the buck 2 converters' power good signal is asserted and that the DLY1 has passed. See the *Appendix* section to set the DLY1 timing.

8.10.2 Setting the output voltage V_{GL}

The output voltage of the negative charge pump is programmable via a two-wire interface between –1.8 V and –8.1 V with a 6-bit resolution. See the *Appendix* section to set the V_{GL} voltage.

8.11 Negative Charge Pump Design Procedure

8.11.1 Diodes Selection (CPN)

As for the CPP, the CPN's diodes need to handle the following power: $P_D = I_{GL} \times V_F$. See Table 8-2 for diode selection.

8.11.2 Capacitors selection (CPN)

See the *Capacitors selection (CPP)* section for more detail.

A combination of C_{OUT} = 4.7 µF, C_{FLY} = 100 nF, and $C_{COLLECTOR}$ = 100 nF is a good starting point for most applications (the final values can be optimized on a case-by-case basis if necessary).

8.11.3 Selecting the NPN Transistor (CPN)

The NPN transistor used to regulate V_{GL} should have a DC gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump's output current. The transistor should also be able to withstand voltages up to V_{IN} across its collector-emitter (V_{CE}).

The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design. The power dissipated in the transistor is given by the following equation:

$$P_Q = \left[V_{IN} - (2 \times V_F) - \left| V_{GL} \right| \right] \times I_{GL} \quad (3)$$

I_{GL} = Mean output current on V_{GL}
V_F = Diode forward voltage

A pull-down resistor is also required between the transistor's base and emitter. The value of this resistor is not critical, but it should be large enough not to divert significant current away from the base of the transistor. A value of 100 kΩ is suitable for most applications

8.11.4 Negative Charge Pump Protection

The TPS65175/A contains a circuit to protect the CPN against short circuits on its output. A short circuit condition is detected as long as V_{GL} remains above -0.7 V. The base current is then limited to 320 µA typically.

8.12 P-Vcom Voltage and Gain (V_{COM})

The TPS65175/A integrates a P-Vcom block that allows to set the non-inverting input voltage reference as well as the gain of an external operational amplifier (Op-Amp).

8.12.1 Enable Signal (DLY2)

The P-Vcom is powered by the boost converter and starts operating after the DLY2 has passed. See the *Appendix* section to set the DLY2 timing.

8.13 P-Vcom Design Procedure

The TPS65175/A P-Vcom block includes an internal DAC connected to the non-inverting input of the Op-Amp setting the V_{COM} output voltage. The inverting input is connected to a resistor network allowing the user to set different gains using the internal registers in order to compensate the panel signal fedback on the VCOM_FB pin .

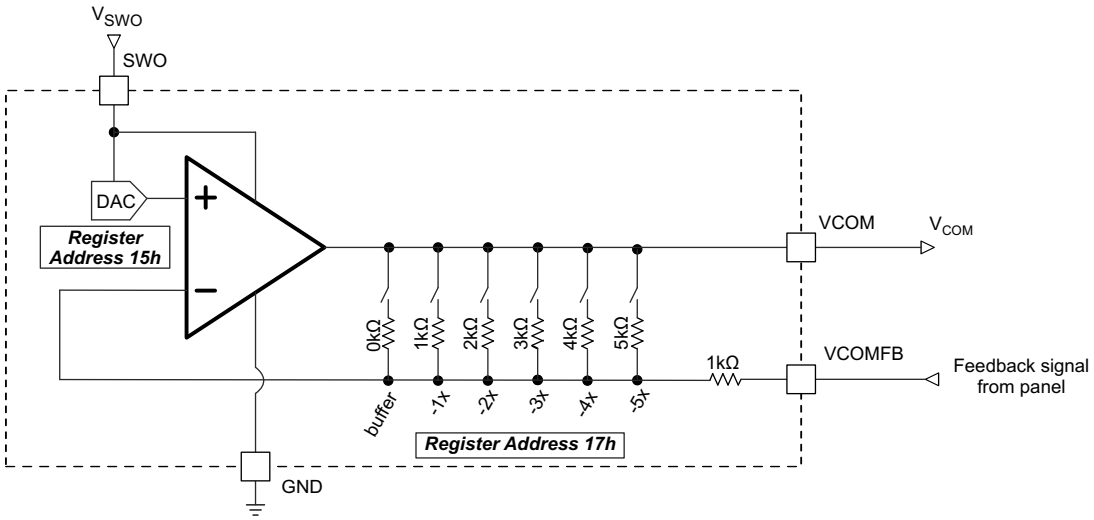


Figure 8-3. P-VCOM Block Diagram

8.13.1 Setting the P-Vcom gain

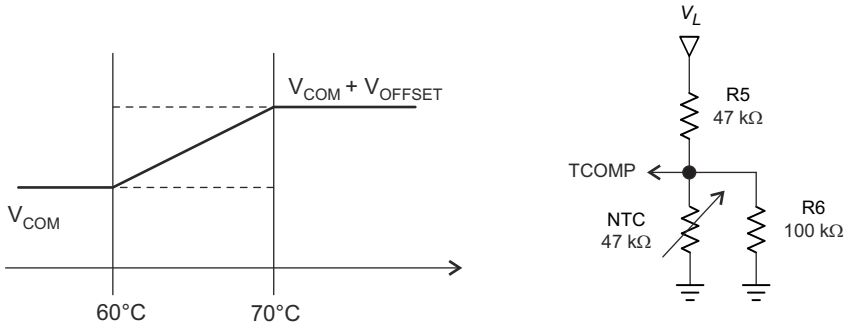
The P-Vcom gain is selectable between 6 different amplification factors (3 bits) via a two-wire interface: Buffer Mode, -1x amplification, -2x, -3x, -4x or -5x. See the *Appendix* section to set the Vcom gain.

8.14 P-Vcom Temperature Compensation

The P-Vcom can be temperature compensated, using the same resistive network and thermistor as the VGH temperature compensation. The user has to provide V_{COM} and V_{COM} high temperature

Note

The internal temperature compensation system is made to work only with 47 kΩ NTC part number **NCP18WB473F10RB** as well as **47 kΩ top-** and **100 kΩ bottom--**resistor (see below).



8.14.1 Setting the V_{COM} output voltage

The V_{COM} voltage is programmable via a two-wire interface with a 9-bit resolution between 250*V_{DD}/1023 and 640*V_{DD}/1023 or 310*V_{DD}/1023 and 520*V_{DD}/1023. The V_{COM} high temperature voltage programmed for the temperature compensation of the Op-Amp output can be programmed between 16 different offsets above the programmed V_{COM} value. See the *Appendix* section to set the V_{COM} voltage as well as the V_{OFFSET}.

8.15 Gamma Buffer (GMA1-GMA6)

The TPS65175/A integrates 6-channel gamma buffer used as voltage references for the Source Driver IC.

8.15.1 Enable Signal (DLY2)

As the gamma buffer channels are supplied by the boost converter output rail, they are following ratio-metrically the V_{DD} voltage from power-on till power-down and start together with the boost converter after the DLY2 has passed. See the *Appendix* section to set the DLY2 timing.

8.15.2 Setting the output voltage of GMA1-GMA6

The output voltage of each of the 6 channels is programmable via a two-wire interface with a 9-bit resolution between V_{DD} and $V_{DD}/2$ for GMA1-GMA3, and between $V_{DD}/2$ and 0 V and for GMA4-GMA6 . See the *Appendix* section to set the V_{GMAX} voltage.

8.15.3 Output Load (Gamma Buffer)

The gamma buffer channels are able to sink and source DC output current of 10 mA (minimum guaranteed).

The output channels are not designed to support high capacitive loads bigger than 150 pF and shall be connected directly to the Source Driver IC without output capacitor.

8.16 Level Shifters

An internal block diagram of the level shifter block is shown in Figure 8-4.

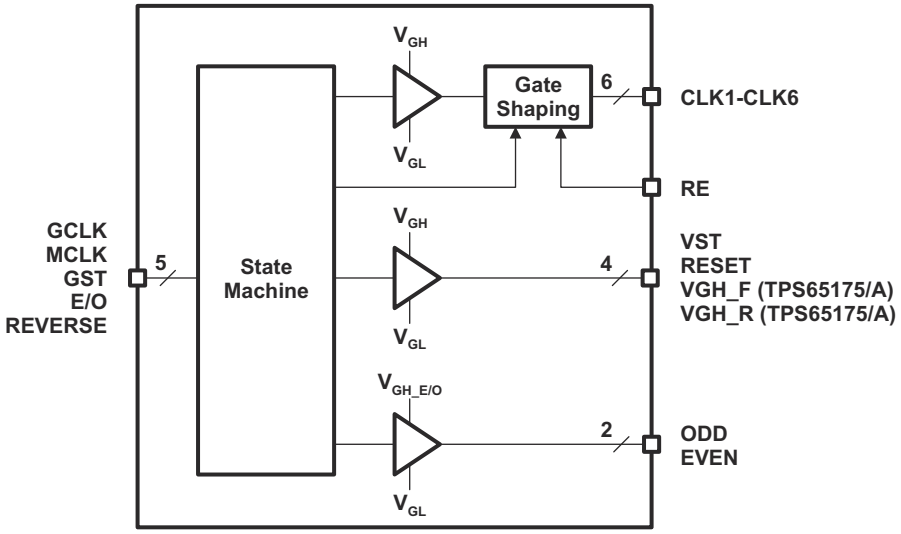


Figure 8-4. Internal Block Diagram

8.17 State Machine

The state machine generates 12 output signals from the 5 input signals, as described below.

8.18 GCLK

The rising edge of GCLK defines the rising edge of the active CLK channel. The phase difference between adjacent CLK signals is 60°, which means that the frequency of the output clocks is exactly one sixth the frequency of the GCLK signal (see Figure 8-5 to Figure 8-8).

The falling edge of GCLK has no effect.

8.19 MCLK

The rising edge of MCLK defines the start of gate-shaping for the active CLK channel. The phase difference between adjacent CLK signals is 60°, which means that the frequency of the output clocks is exactly one sixth the frequency of the MCLK signal (see Figure 8-5 to Figure 8-8).

The falling edge of MCLK defines the falling edge of the active CLK channel (and, by definition, the end of gate-shaping).

8.20 GST

The function of the GST signal depends on the state of GCLK when the GST pulse occurs. When GCLK is low (see Figure 8-5 and Figure 8-11, and section describing VST behavior):

- the rising edge of GST defines the rising edge of VST
- the falling edge of GST defines the falling edge of VST
- the GST signal indicates the start of a new frame, and resets all internal counters in the state machine

When GCLK is high (see Figure 8-6 and Figure 8-8 and section describing RESET behavior):

- the rising edge of GST defines the rising edge of RESET
- the falling edge of GST defines the falling edge of RESET

8.21 E/O

During normal operation a pulse applied to E/O toggles the EVEN and ODD outputs (see section below describing the EVEN and ODD outputs).

See also section describing Abnormal Operation.

8.22 Reverse

The REVERSE signal is used to select forward or reverse operation.

During forward operation (REVERSE = low), VGH_F = high, VGH_R = low and the clock signals are output in the following order:

(start of frame) 4 – 5 – 6 – 1 – 2 – 3 – 4 – 5 – 6 – 1 – 2 – 3 . . . . . 4 – 5 – 6 – 1 – 2 – 3 (end of frame)

During reverse operation (REVERSE = high), VGH_F = low, VGH_R = high and the clock signals are output in the following order:

(start of frame) 3 – 2 – 1 – 6 – 5 – 4 – 3 – 2 – 1 – 6 – 5 – 4 . . . . . 3 – 2 – 1 – 6 – 5 – 4 (end of frame)

The REVERSE pin is internally pulled down by a 100 kΩ (typical) resistor.

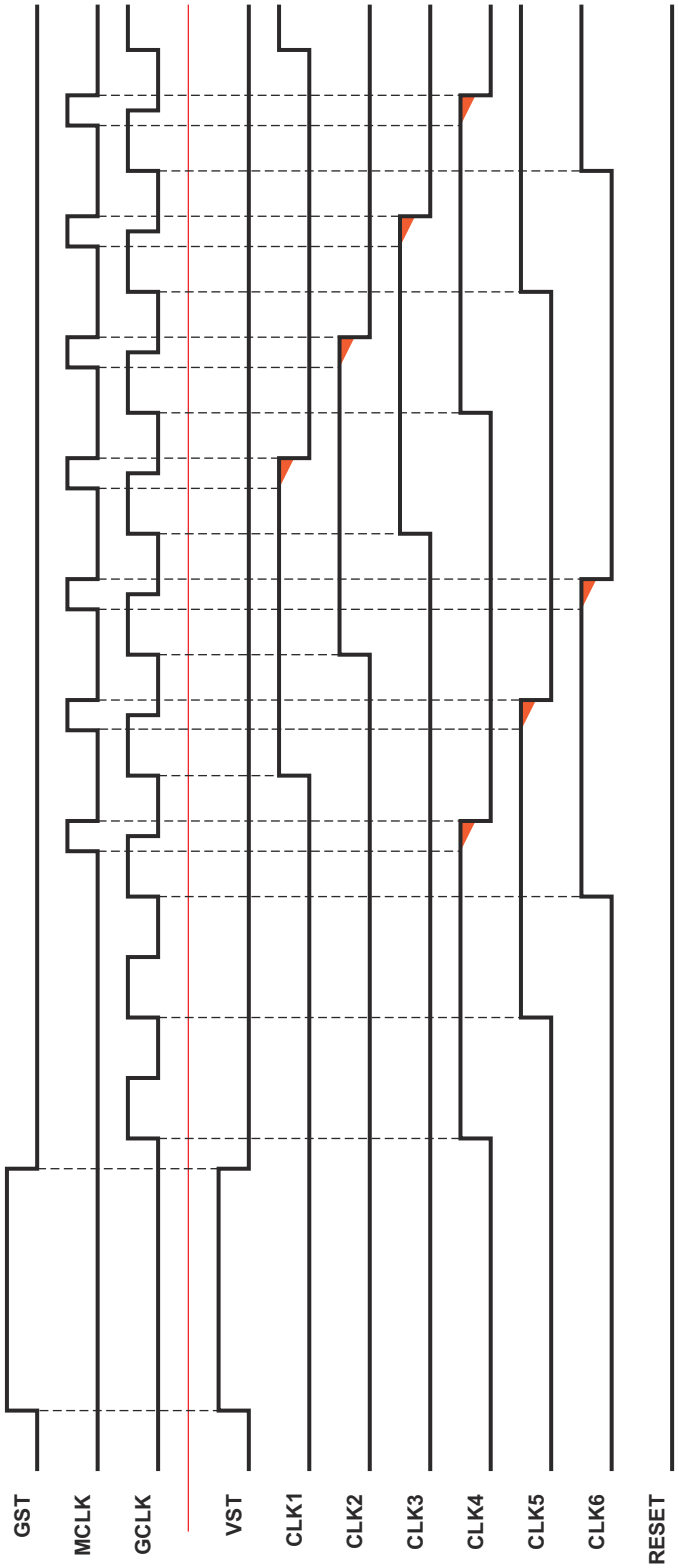


Figure 8-5. Timing Diagram: Normal Operation, Start of Frame

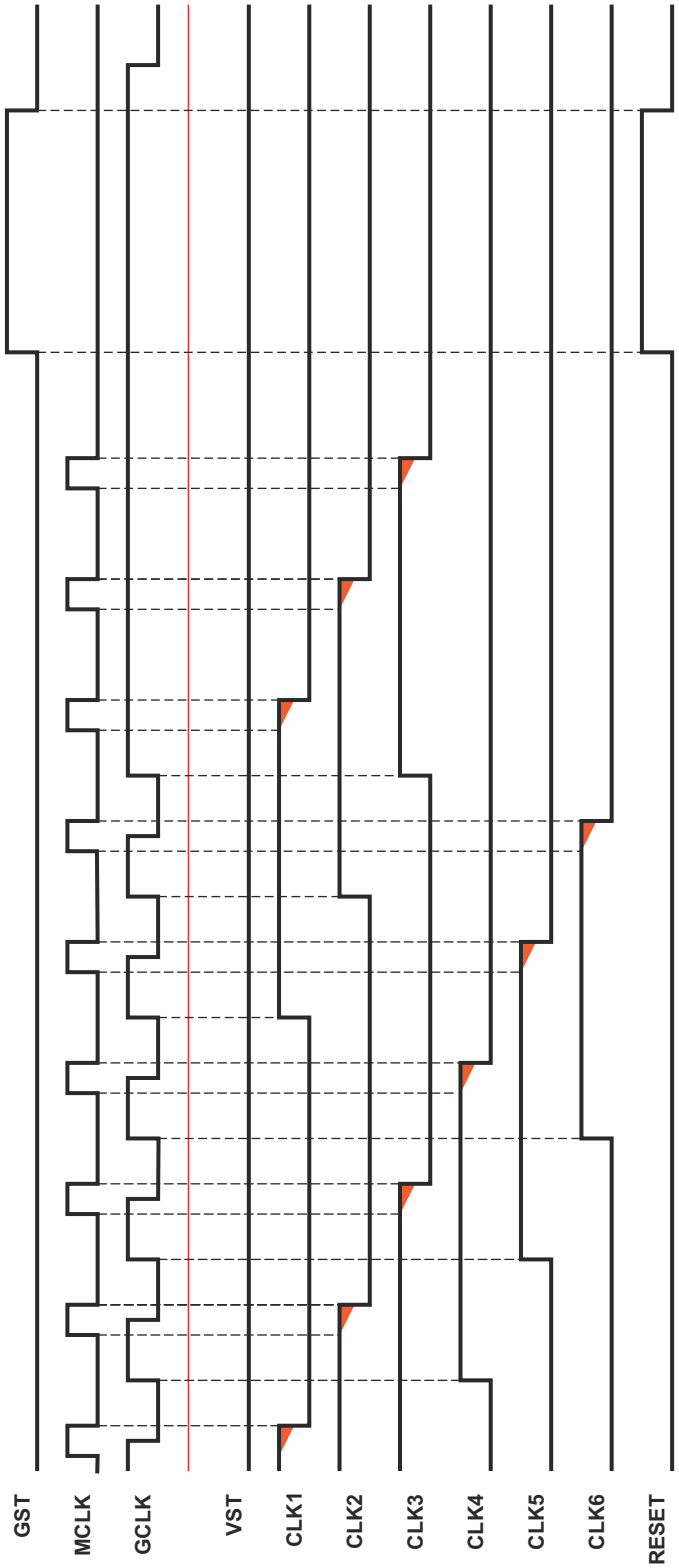


Figure 8-6. Timing Diagram: Normal Operation, End of Frame

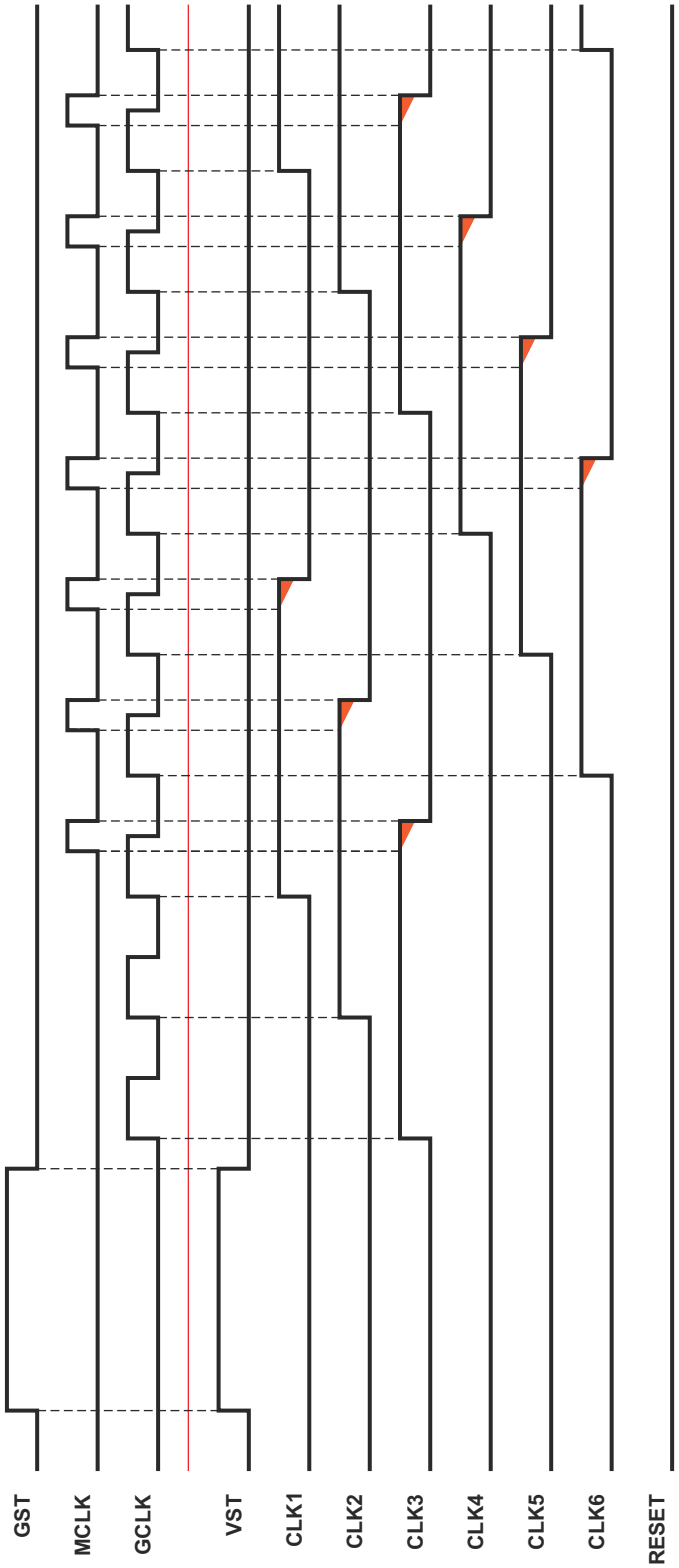


Figure 8-7. Timing Diagram: Reverse Operation, Start of Frame

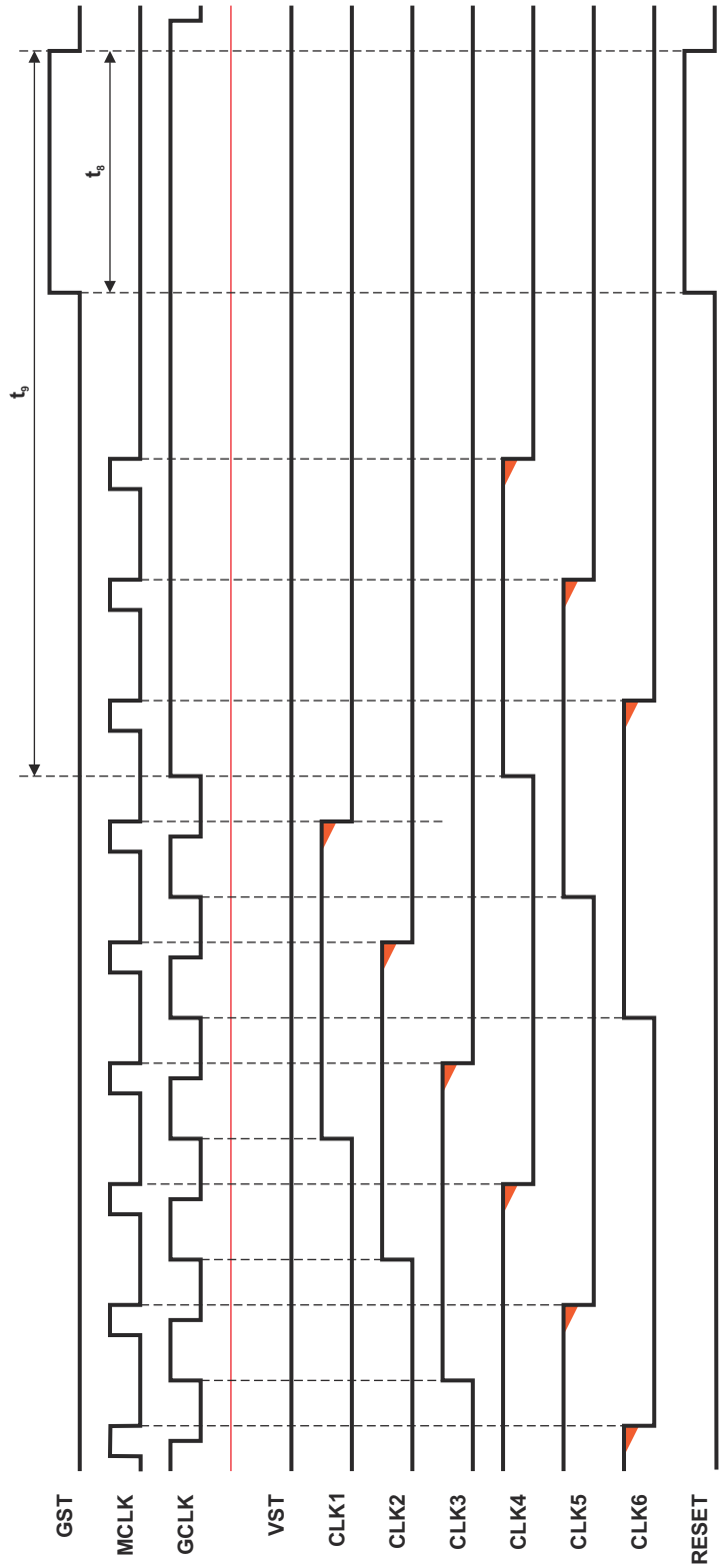


Figure 8-8. Timing Diagram: Reverse Operation, End of Frame

8.23 VGH_F and VGH_R

The VGH_F and VGH_R signals follow the REVERSE and GST inputs in accordance with Table 8-6.

Table 8-6. Truth Table

	INPUTS			OUTPUTS		NORMAL OCCURRENCE
	REVERSE	GST	Q	VGH_F	VGH_R	
Normal	1	X	X	0	1	Reverse, power-up Forward to reverse
	0	X	0	1	0	Forward, power-up
	0	↑	1	1	0	Reverse to forward
	0	0	0	1	0	Forward, power-down
	0	0	1	0	1	Reverse, power-down
Abnormal	Same as Normal mode					

The VGH_F and VGH_R outputs feature a dead time (t_{12} and t_{13}) such that when REVERSE changes state VGH_F and VGH_R are temporarily both low before the active channel goes high (see Figure 8-9).

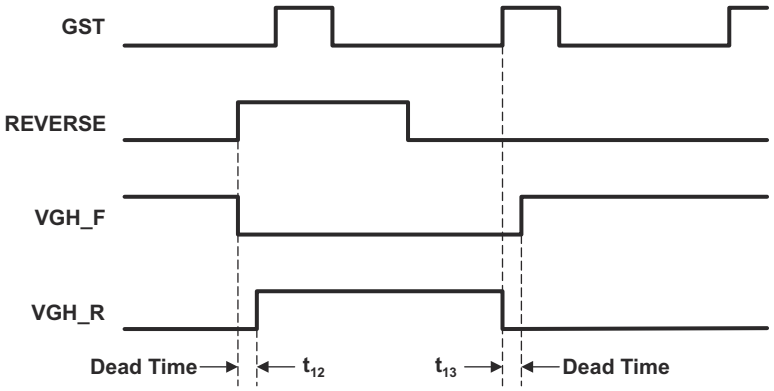


Figure 8-9. VGH_F and VGH_R Operation, Showing Dead Time

To ensure the VGH_F and VGH_R outputs remain valid during power-down (when the REVERSE signal may not be valid), the REVERSE signal is latched on every rising edge of GST (see Figure 8-10).

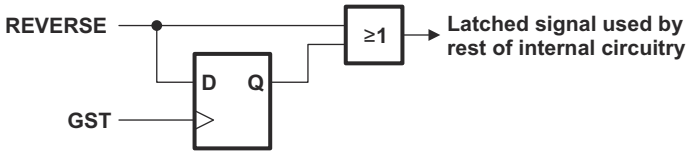


Figure 8-10. REVERSE Latching Scheme

The VGH_F and VGH_R channels follow a well defined characteristic during power-up and power-down (see Power Supply Sequencing).

8.24 VST

The VST signal follows the GST and GCLK input signals in accordance with the truth table below (see also Figure 8-5 to Figure 8-8).

	INPUTS		OUTPUT
OPERATION	GST	GCLK	VST
Normal	1	0	1
	1	1	0
	0	X	0
Abnormal	X	X	0

8.25 RESET

The RESET output is derived from the GST and GCLK signals in accordance with the truth table below (see also Figure 8-5 to Figure 8-8).

	INPUTS		OUTPUT
OPERATION	GST	GCLK	RESET
Normal	0	X	0
	1	0	0
	1	1	1
Abnormal	X	X	0

8.26 EVEN and ODD

The EVEN and ODD outputs toggle on the rising edge of the E/O input signal in accordance with the truth table below. The pulse width of the E/O signal defines a dead time during which both EVEN and ODD outputs are temporarily low (see Figure 8-11).

	INPUT	OUTPUTS	
OPERATION	E/O	EVEN	ODD
Power-Up	X	1	0
Normal	↑	toggle(1)	toggle(1)
Abnormal	X	1	0

(1) With dead time

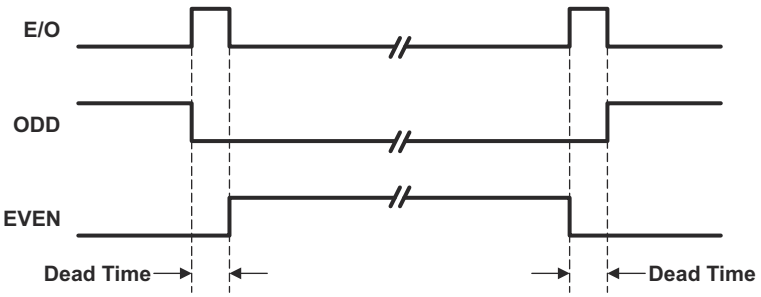


Figure 8-11. EVEN and ODD Generation, Showing Dead Time

8.27 Abnormal Operation

The TPS65198 supports abnormal operation. Abnormal operation is detected when E/O is high during the rising edge of GST (see Figure 8-12), after which the level shifter outputs are forced to the following state:

1. CLK1-CLK6 low
2. VST, RESET low
3. EVEN and ODD in power-up state (EVEN high, ODD low) [1]
4. VGH_F and VGH_R not changed (outputs follow REVERSE input as in normal operation)

Normal operation is resumed the next time E/O is low during the rising edge of GST. Upon exiting abnormal operation the state machine adopts its normal start-of-frame initial state.

[1] Note that because of the dead time introduced by the E/O signal during normal operation, a short low pulse may appear on the EVEN output when abnormal operation is detected (see Figure 8-12).

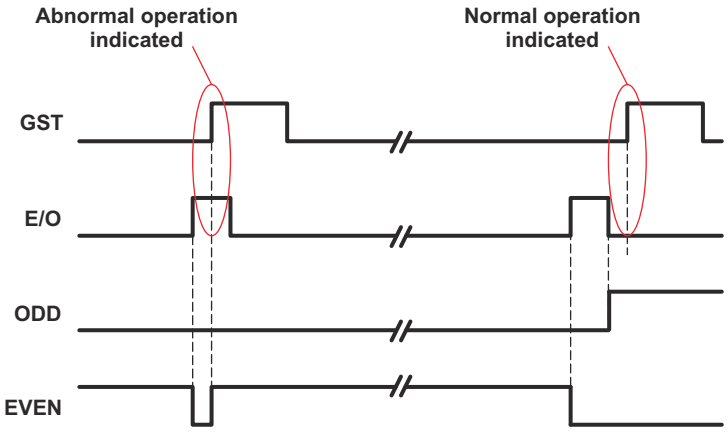


Figure 8-12. E/O During Abnormal Operation, EVEN Initially High

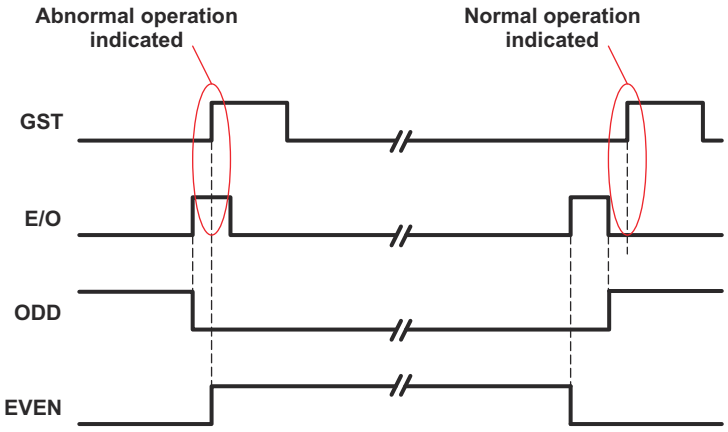


Figure 8-13. E/O During Abnormal Operation, EVEN Initially Low

8.28 CLK1 to CLK6

The CLK outputs go high on the rising edge of GCLK and go low on the falling edge of MCLK. The CLK outputs' frequency is exactly one sixth of the GCLK and MCLK frequencies and adjacent CLK channels are separated by 60° phase difference.

The CLK outputs are generated in a specific order that depends on whether the device is operating in forward or reverse mode (see Figure 8-5 to Figure 8-8 and the section describing REVERSE operation).

8.29 Gate Voltage Shaping

The clock outputs CLK1 to CLK6 support gate voltage shaping, which can help reduce image flickering in certain applications. A simplified block diagram of one of the clock channels is shown in Figure 8-14.

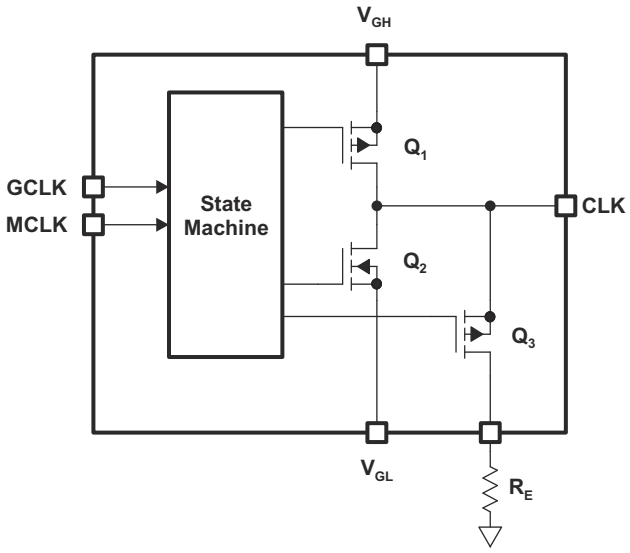


Figure 8-14. CLK Output Stage

- On the rising edge of the GCLK, the active channel's Q_1 is enabled and its Q_2 disabled; the output goes to V_{GH}.
- Gate voltage shaping starts on the rising edge of MCLK, which disables Q_1 and enables Q_3. The LCD panel's pixel and storage capacitor now discharge through Q_3 at a rate determined by the external resistor R_E (see Figure 8-15).
- On the falling edge of MCLK, Q_3 is disabled and Q_2 enabled; the output goes to V_{GL}.

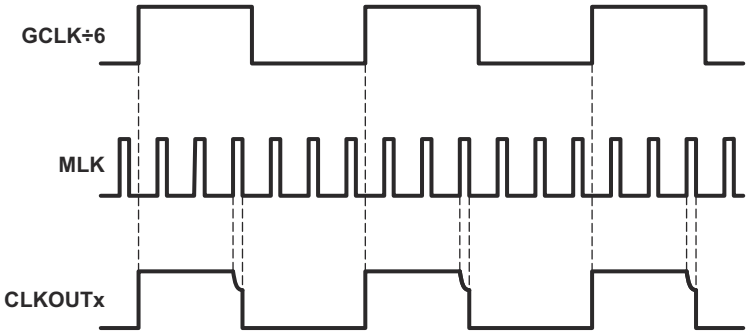


Figure 8-15. Gate Shaping Timing Diagram

8.30 Power Supply Sequencing (CLK1-CLK6, VST, RESET)

These outputs track V_{GL} when $V_{GH} < V_{UVLO\_L/S}$ and operate normally when $V_{GH} > V_{UVLO\_L/S}$ (see Figure 8-16 and Figure 8-17).

8.31 Power Supply Sequencing (EVEN, ODD)

EVEN and ODD track V_{GL} when $V_{GH} < V_{UVLO\_L/S}$ and operate normally when $V_{GH} > V_{UVLO}$ (see Figure 8-16 and Figure 8-17).

8.32 Power Supply Sequencing (VGH_F, VGH_R)

VGH_F and VGH_R track V_{GL} when $V_{GH} < V_{UVLO\_L/S}$ and operate normally when $V_{GH} > V_{UVLO\_L/S}$ (see Figure 8-16 and Figure 8-17).

During power-down these outputs remain in the state they were when the last rising edge of GST occurred.

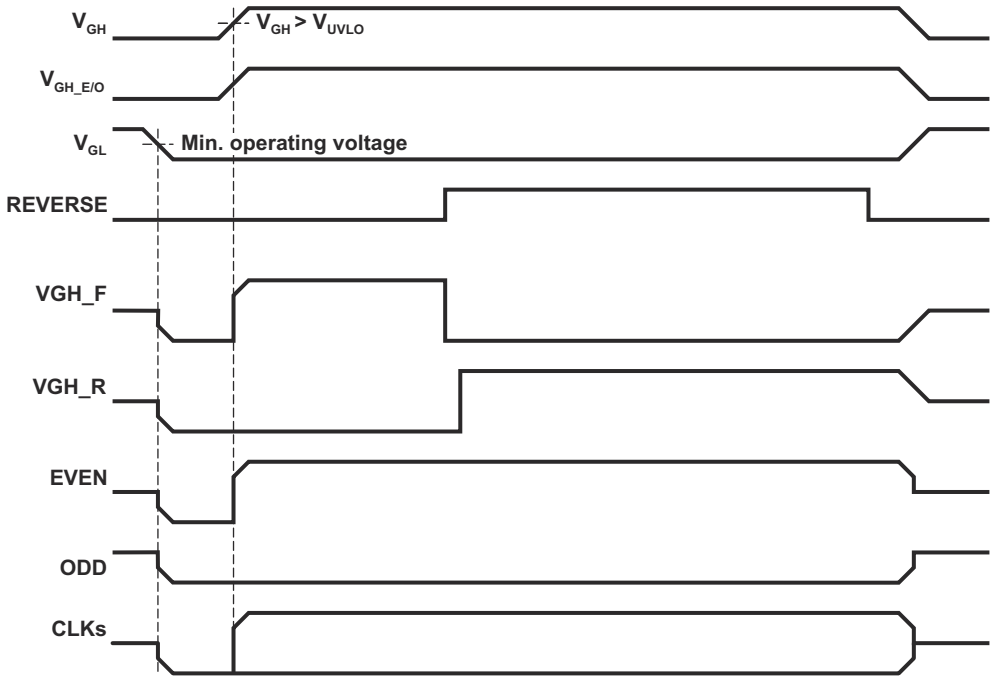


Figure 8-16. Power Supply Sequencing During Forward Operation

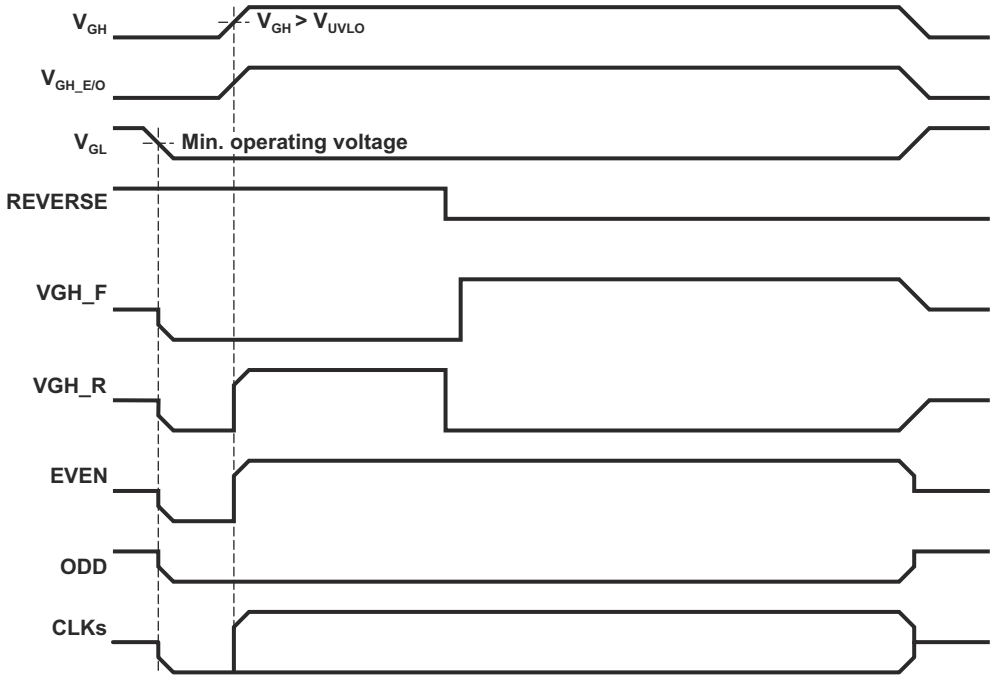


Figure 8-17. Power Supply Sequencing During Reverse Operation

8.33 Typical Applications

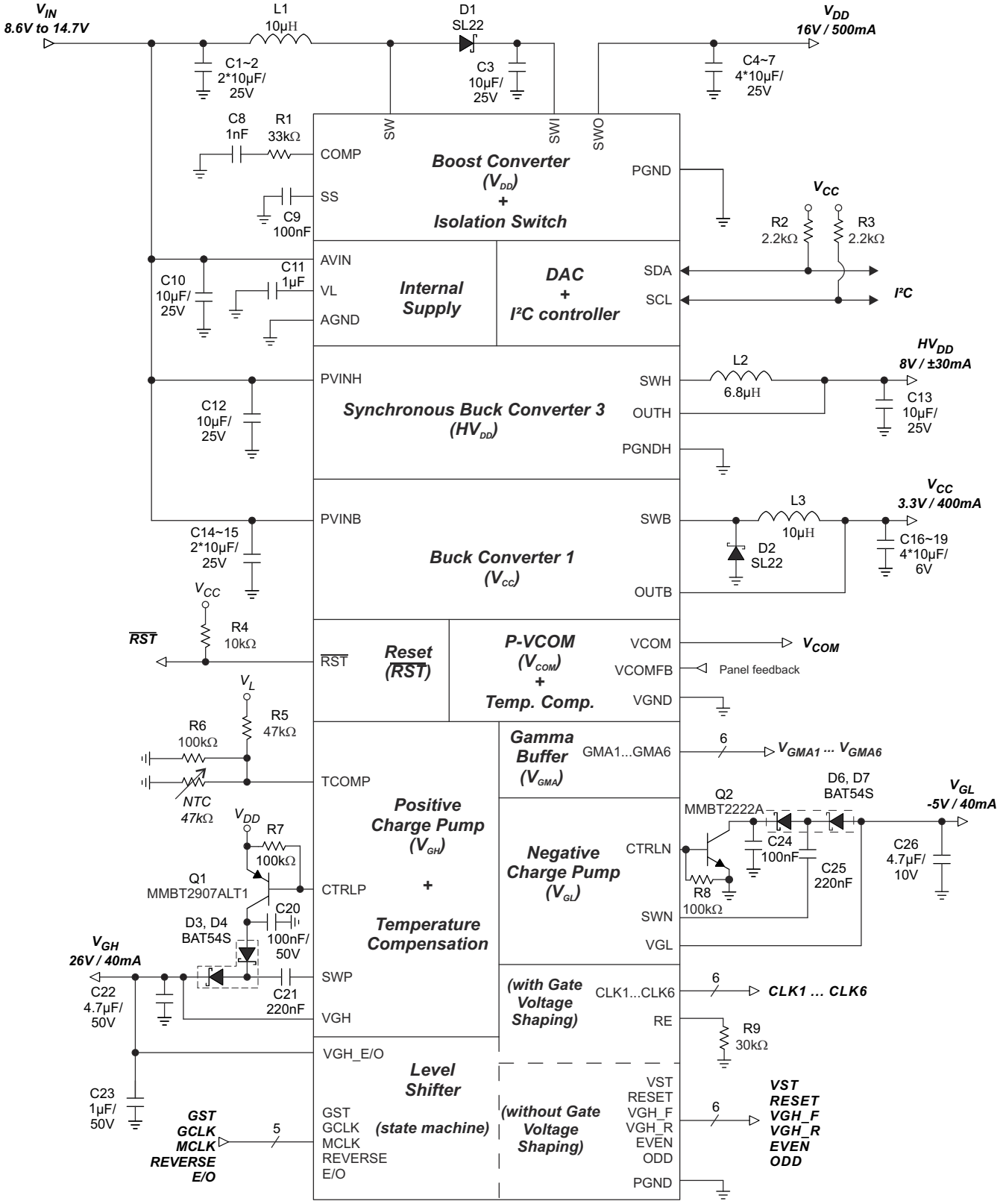


Figure 8-18.

9 APPENDIX – I2C INTERFACE

9.1 I²C Serial Interface Description

The TPS65175/A communicates through an industry standard two-wire interface, I²C, to receive data in slave mode.

The TPS65175/A integrates a non-volatile memory (EEPROM) that allows the storage of the DAC values into the registers with a capability of 1000 programming cycles maximum.

I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS65175/A works as a slave and supports the following data transfer modes, as defined in the I²C-Bus specification: standard mode (100 kbps) and fast mode (400 kbps). The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The TPS65175/A supports 7-bit addressing. The device 7-bit address is defined as '0100000X' (see Figure 9-1), where the LSB enables the write or read function.

(MSB)			Address				(LSB)
0	1	0	0	0	0	0	R/$\overline{W}$

R/ $\overline{W}$ = R/(W)

Figure 9-1. TPS65175/A Slave Address Byte

The device that initiates the communication is called a master, and the devices controlled by the master are slaves. The master generates the serial clock on SCL, controls the bus access, and generates START and STOP conditions (see Figure 9-2). A START initiates a new data transfer to slave. Transitioning SDA from high to low while SCL remains high generates a START condition. A STOP condition ends a data transfer to slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

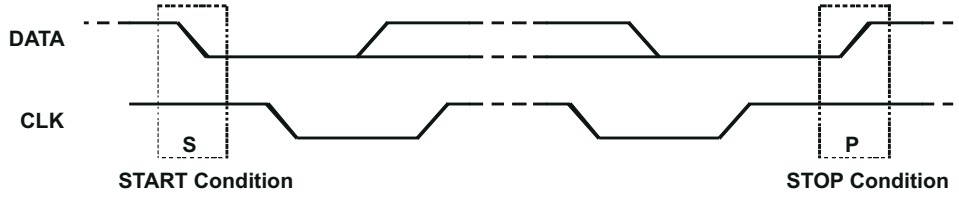


Figure 9-2. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/(W) on the SDA line. During all transmissions, the master ensures that the data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 9-3). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an Acknowledgment, ACK, (see Figure 9-4) by pulling the SDA line low during the entire high period of the SCL cycle. Upon detecting this Acknowledgment, the master knows that communication link with a slave has been established.

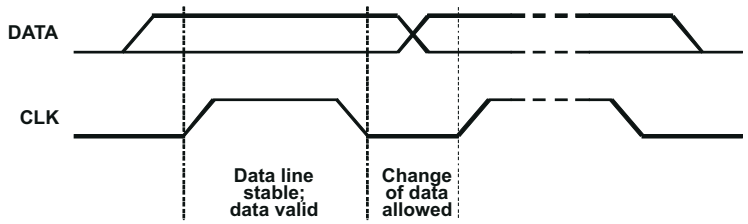


Figure 9-3. Bit Transfer on the Serial Interface

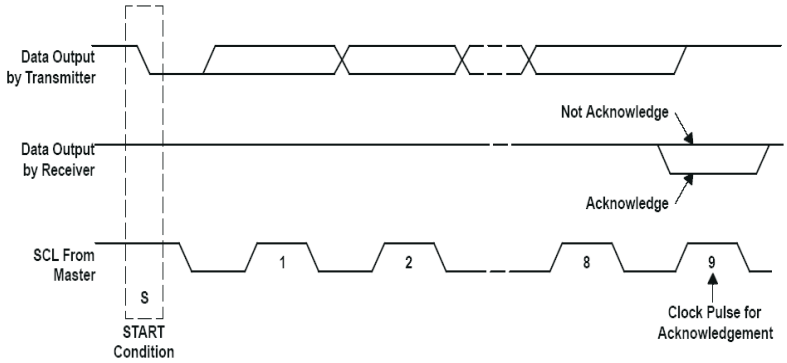


Figure 9-4. Acknowledge on the I²C Bus

The master generates further SCL cycles to either transmit data to the slave (R/(W) bit = 0) or receive data from the slave (R/(W) bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To terminate the data transfer, the master generates STOP condition by pulling the SDA line from low to high while the SCL line is high (see Figure 9-5). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

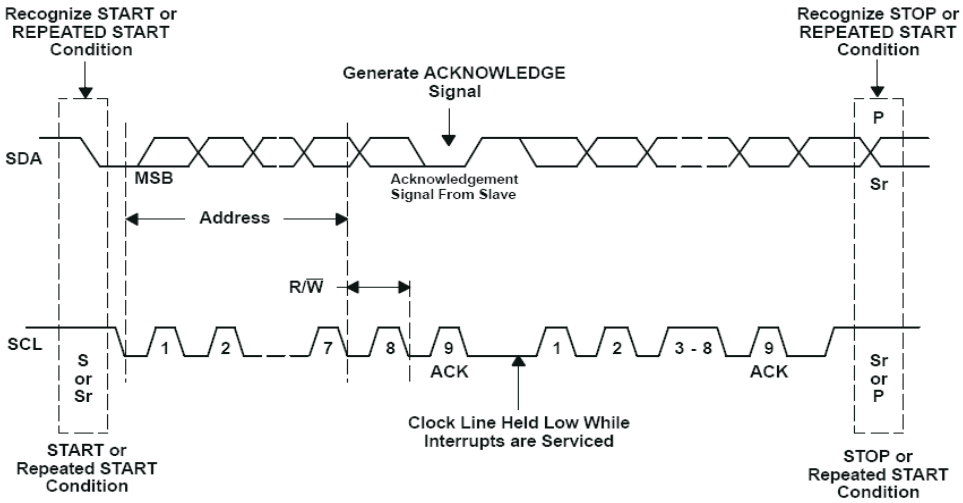


Figure 9-5. Bus Protocol

Attempting to read data from register addresses not listed in the following section will result in 00h being read out.

10 Detailed Description

10.1 DAC Settings

The following tables show the DAC values and the corresponding voltages of each block address.

VDD (00h)

DAC value	VDD	DAC value	VDD
00h	12.7 V	20h	15.9 V
01h	12.8 V	21h	16.0 V
02h	12.9 V	22h	16.1 V
03h	13.0 V	23h	16.2 V
04h	13.1 V	24h	16.3 V
05h	13.2 V	25h	16.4 V
06h	13.3 V	26h	16.5 V
07h	13.4 V	27h	16.6 V
08h	13.5 V	28h	16.7 V
09h	13.6 V	29h	16.8 V
0Ah	13.7 V	2Ah	16.9 V
0Bh	13.8 V	2Bh	17.0 V
0Ch	13.9 V	2Ch	17.1 V
0Dh	14.0 V	2Dh	17.2 V
0Eh	14.1 V	2Eh	17.3 V
0Fh	14.2 V	2Fh	17.4 V
10h	14.3 V	30h	17.5 V
11h	14.4 V	31h	17.6 V
12h	14.5 V	32h	17.7 V
13h	14.6 V	33h	17.8 V
14h	14.7 V	34h	17.9 V
15h	14.8 V	35h	18.0 V
16h	14.9 V	36h	18.1 V
17h	15.0 V	37h	18.2 V
18h	15.1 V	38h	18.3 V
19h	15.2 V	39h	18.4 V
1Ah	15.3 V	3Ah	18.5 V
1Bh	15.4 V	3Bh	18.6 V
1Ch	15.5 V	3Ch	18.7 V
1Dh	15.6 V	3Dh	18.8 V
1Eh	15.7 V	3Eh	18.9 V
1Fh	15.8 V	3Fh	19.0 V

HVDD (= 1/2*VDD)

DAC value	HVDD	DAC value	HVDD
00h	6.35 V	20h	8.95 V
01h	6.40 V	21h	8.00 V
02h	6.45 V	22h	8.05 V
03h	6.50 V	23h	8.10 V
04h	6.55 V	24h	8.15 V
05h	6.60 V	25h	8.20 V
06h	6.65 V	26h	8.25 V
07h	6.70 V	27h	8.30 V
08h	6.75 V	28h	8.35 V
09h	6.80 V	29h	8.40 V
0Ah	6.85 V	2Ah	8.45 V
0Bh	6.90 V	2Bh	8.50 V
0Ch	6.95 V	2Ch	8.55 V
0Dh	7.00 V	2Dh	8.60 V
0Eh	7.05 V	2Eh	8.65 V
0Fh	7.10 V	2Fh	8.70 V
10h	7.15 V	30h	8.75 V
11h	7.20 V	31h	8.80 V
12h	7.25 V	32h	8.85 V
13h	7.30 V	33h	8.90 V
14h	7.35 V	34h	8.95 V
15h	7.40 V	35h	9.00 V
16h	7.45 V	36h	9.05 V
17h	7.50 V	37h	9.10 V
18h	7.55 V	38h	9.15 V
19h	7.60 V	39h	9.20 V
1Ah	7.65 V	3Ah	9.25 V
1Bh	7.70 V	3Bh	9.30 V
1Ch	7.75 V	3Ch	9.35 V
1Dh	7.80 V	3Dh	9.40 V
1Eh	7.85 V	3Eh	9.45 V
1Fh	7.90 V	3Fh	9.50 V

VCC (01h)

DAC value	VCC
00h	1.6 V
01h	1.6 V
02h	1.7 V
03h	1.8 V
04h	1.9 V
05h	2.0 V
06h	3.0 V
07h	3.1 V
08h	3.2 V
09h	3.3 V
0Ah	3.4 V
0Bh	3.5 V
0Ch	3.6 V

VGH_LT - HT
(02h ~ 03h)

DAC value	VGH_LT
00h	19 V
01h	20 V
02h	21 V
03h	22 V
04h	23 V
05h	24 V
06h	25 V
07h	26 V
08h	27 V
09h	28 V
0Ah	29 V
0Bh	30 V
0Ch	31 V
0Dh	32 V
0Eh	33 V
0Fh	34 V

DAC value	VGH_HT
00h	17 V
01h	18 V
02h	19 V
03h	20 V
04h	21 V
05h	22 V
06h	23 V
07h	24 V
08h	25 V
09h	26 V
0Ah	27 V
0Bh	28 V
0Ch	29 V
0Dh	30 V
0Eh	31 V
0Fh	32 V

VGL (04h)

DAC value	VGL
00h	-1.8 V
01h	-1.9 V
02h	-2.0 V
03h	-2.1 V
04h	-2.2 V
05h	-2.3 V
06h	-2.4 V
07h	-2.5 V
08h	-2.6 V
09h	-2.7 V
0Ah	-2.8 V
0Bh	-2.9 V
0Ch	-3.0 V
0Dh	-3.1 V
0Eh	-3.2 V
0Fh	-3.3 V
10h	-3.4 V
11h	-3.5 V
12h	-3.6 V
13h	-3.7 V
14h	-3.8 V
15h	-3.9 V
16h	-4.0 V
17h	-4.1 V
18h	-4.2 V
19h	-4.3 V
1Ah	-4.4 V
1Bh	-4.5 V
1Ch	-4.6 V
1Dh	-4.7 V
1Eh	-4.8 V
1Fh	-4.9 V

DAC value	VGL
20h	-5.0 V
21h	-5.1 V
22h	-5.2 V
23h	-5.3 V
24h	-5.4 V
25h	-5.5 V
26h	-5.6 V
27h	-5.7 V
28h	-5.8 V
29h	-5.9 V
2Ah	-6.0 V
2Bh	-6.1 V
2Ch	-6.2 V
2Dh	-6.3 V
2Eh	-6.4 V
2Fh	-6.5 V
30h	-6.6 V
31h	-6.7 V
32h	-6.8 V
33h	-6.9 V
34h	-7.0 V
35h	-7.1 V
36h	-7.2 V
37h	-7.3 V
38h	-7.4 V
39h	-7.5 V
3Ah	-7.6 V
3Bh	-7.7 V
3Ch	-7.8 V
3Dh	-7.9 V
3Eh	-8.0 V
3Fh	-8.1 V

DLY0 ~ DLY3
(05h ~ 08h)

DAC value	DLY0
00h	3 ms
01h	6 ms
02h	9 ms
03h	12 ms
04h	15 ms
05h	18 ms
06h	21 ms
07h	24 ms

DAC value	DLY1
00h	0 ms
01h	5 ms
02h	10 ms
03h	15 ms
04h	20 ms
05h	25 ms
06h	30 ms
07h	35 ms

DAC value	DLY2
00h	0 ms
01h	5 ms
02h	10 ms
03h	15 ms
04h	20 ms
05h	25 ms
06h	30 ms
07h	35 ms

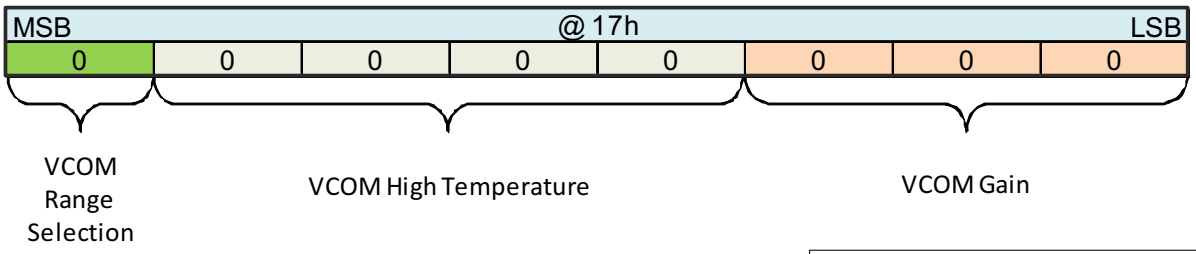
DAC value	DLY3
00h	0 ms
01h	5 ms
02h	10 ms
03h	15 ms
04h	20 ms
05h	25 ms
06h	30 ms
07h	35 ms

VGMA1,2,3
(09h ~ 0Eh)

DAC value	VGMA1,2,3
00-00h	512*(V_{DD}/ 1023)
00-01h	513*(V_{DD}/ 1023)
00-02h	514*(V_{DD}/ 1023)
00-03h	515*(V_{DD}/ 1023)
00-04h	516*(V_{DD}/ 1023)
00-05h	517*(V_{DD}/ 1023)
00-06h	518*(V_{DD}/ 1023)
…	…
01-F9h	1017*(V_{DD}/ 1023)
01-FAh	1018*(V_{DD}/ 1023)
01-FBh	1019*(V_{DD}/ 1023)
01-FCh	1020*(V_{DD}/ 1023)
01-FDh	1021*(V_{DD}/ 1023)
01-FEh	1022*(V_{DD}/ 1023)
01-FFh	1023*(V_{DD}/ 1023)

VGMA4,5,6
(0Fh ~ 14h)

DAC value	VGMA4,5,6
00-00h	0*(V_{DD}/ 1023)
00-01h	1*(V_{DD}/ 1023)
00-02h	2*(V_{DD}/ 1023)
00-03h	3*(V_{DD}/ 1023)
00-04h	4*(V_{DD}/ 1023)
00-05h	5*(V_{DD}/ 1023)
00-06h	6*(V_{DD}/ 1023)
…	…
01-F9h	505*(V_{DD}/ 1023)
01-FAh	506*(V_{DD}/ 1023)
01-FBh	507*(V_{DD}/ 1023)
01-FCh	508*(V_{DD}/ 1023)
01-FDh	509*(V_{DD}/ 1023)
01-FEh	510*(V_{DD}/ 1023)
01-FFh	511*(V_{DD}/ 1023)



VCOM
(15h ~ 16h)

VCOM Range Selection = 0
(391 steps)

DAC value	VCOM
00-00h	250* (V_{DD}/ 1023)
00-01h	251* (V_{DD}/ 1023)
00-02h	252* (V_{DD}/ 1023)
00-03h	253* (V_{DD}/ 1023)
00-04h	254* (V_{DD}/ 1023)
00-05h	255* (V_{DD}/ 1023)
00-06h	256* (V_{DD}/ 1023)
…	…
01-80h	634* (V_{DD}/ 1023)
01-81h	635* (V_{DD}/ 1023)
01-82h	636* (V_{DD}/ 1023)
01-83h	637* (V_{DD}/ 1023)
01-84h	638* (V_{DD}/ 1023)
01-85h	639* (V_{DD}/ 1023)
01-86h	640* (V_{DD}/ 1023)

VCOM Range Selection = 1
(211 steps)

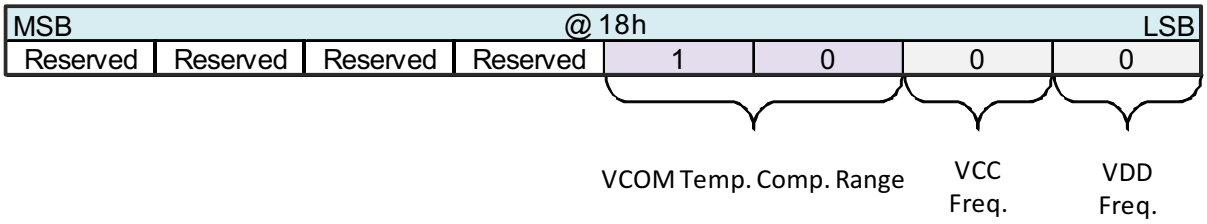
DAC value	VCOM
00-00h	310* (V_{DD}/ 1023)
00-01h	311* (V_{DD}/ 1023)
00-02h	312* (V_{DD}/ 1023)
00-03h	313* (V_{DD}/ 1023)
00-04h	314* (V_{DD}/ 1023)
…	…
00-CEh	516* (V_{DD}/ 1023)
00-CFh	517* (V_{DD}/ 1023)
00-D0h	518* (V_{DD}/ 1023)
00-D1h	519* (V_{DD}/ 1023)
00-D2h	520* (V_{DD}/ 1023)

VCOM High Temperature

Step	VCOM High Temperature
0	V_{COM}
1	V_{COM} + V_{DD}/ 1023*2
2	V_{COM} + V_{DD}/ 1023*4
3	V_{COM} + V_{DD}/ 1023*6
4	V_{COM} + V_{DD}/ 1023*8
5	V_{COM} + V_{DD}/ 1023*10
6	V_{COM} + V_{DD}/ 1023*12
7	V_{COM} + V_{DD}/ 1023*14
8	V_{COM} + V_{DD}/ 1023*16
9	V_{COM} + V_{DD}/ 1023*18
10	V_{COM} + V_{DD}/ 1023*20
11	V_{COM} + V_{DD}/ 1023*22
12	V_{COM} + V_{DD}/ 1023*24
13	V_{COM} + V_{DD}/ 1023*26
14	V_{COM} + V_{DD}/ 1023*28
15	V_{COM} + V_{DD}/ 1023*30

VCOM Gain

Step	VCOM Gain
0	Buffer
1	-1x
2	-2x
3	-3x
4	-4x
5	-5x



VCOM Temperature Compensation Range

Step	VCOM Temp. Comp. Range
0	50°C ~ 60°C (at thermistor)
1	55°C ~ 65°C (at thermistor)
2	60°C ~ 70°C (at thermistor)
3	65°C ~ 75°C (at thermistor)

VCC Frequency

Step	VCC Freq.
0	750 kHz
1	1.5 MHz

VDD Frequency

Step	VDD Freq.
0	750 kHz
1	1.5 MHz

10.2 I²C Interface Protocol

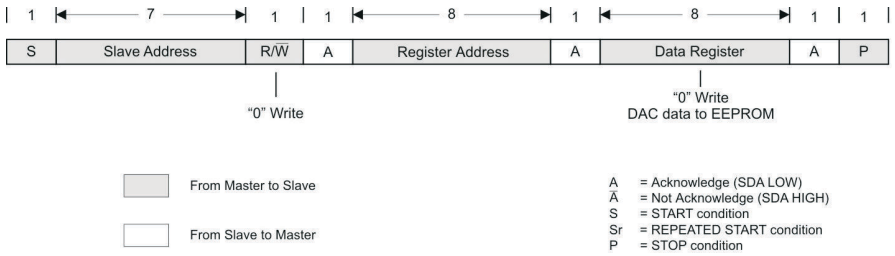


Figure 10-1. "Write" Data to DAC – Transfer Format in F/S-Mode

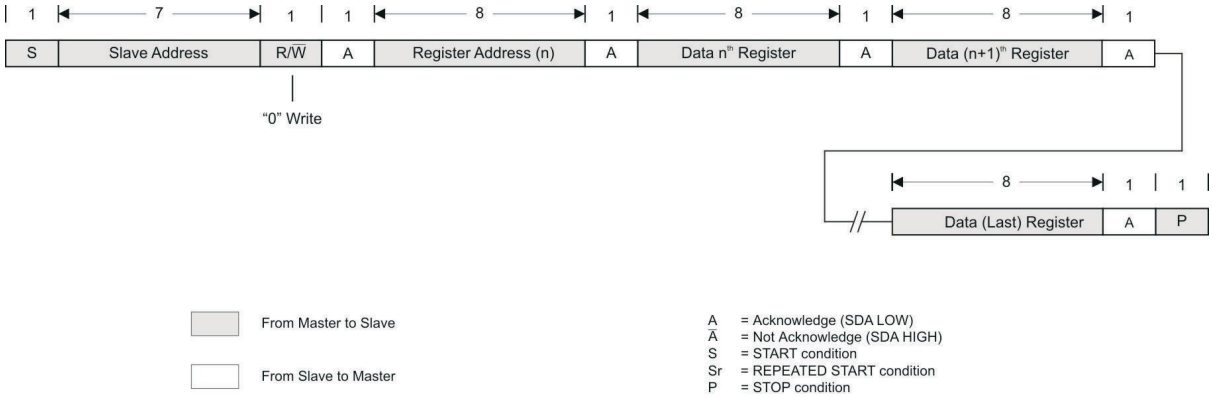


Figure 10-2. "Write" Data to DAC – Transfer Format in F/S-Mode Featuring Register Address Auto-Increment

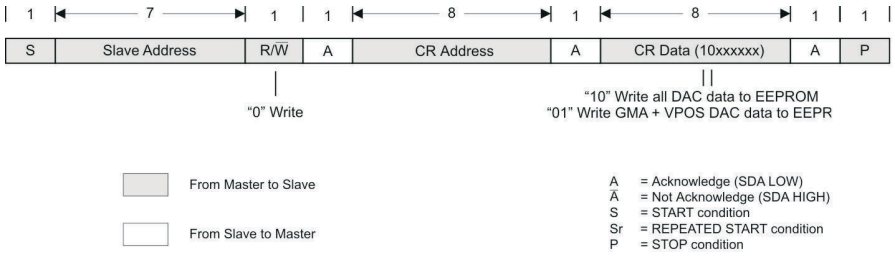


Figure 10-3. "Write" Data to EEPROM – Transfer Format in F/S-Mode Featuring Register Address Auto-Increment

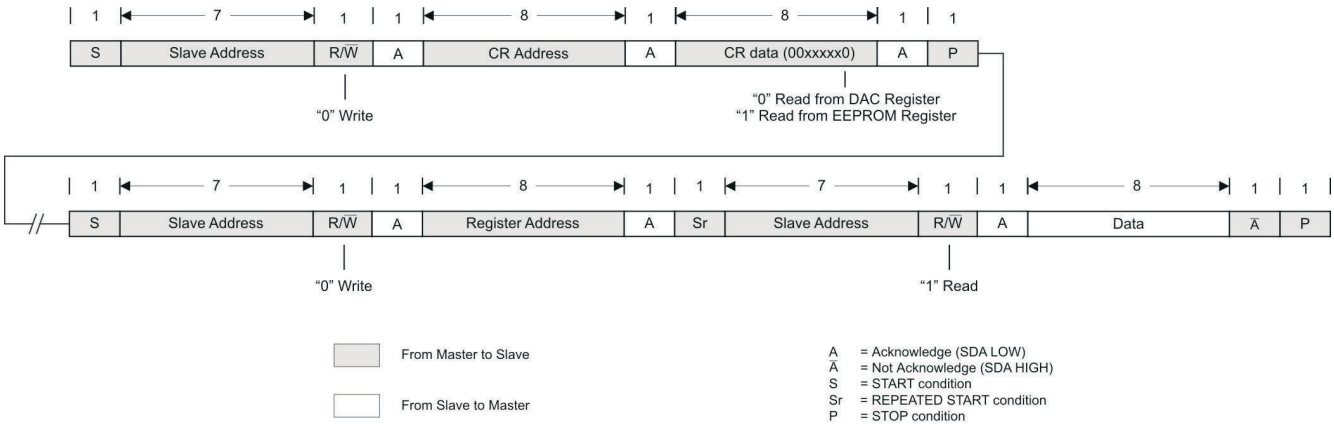


Figure 10-4. "Read" Data From DAC/EEPROM – Transfer Format in F/S-Mode

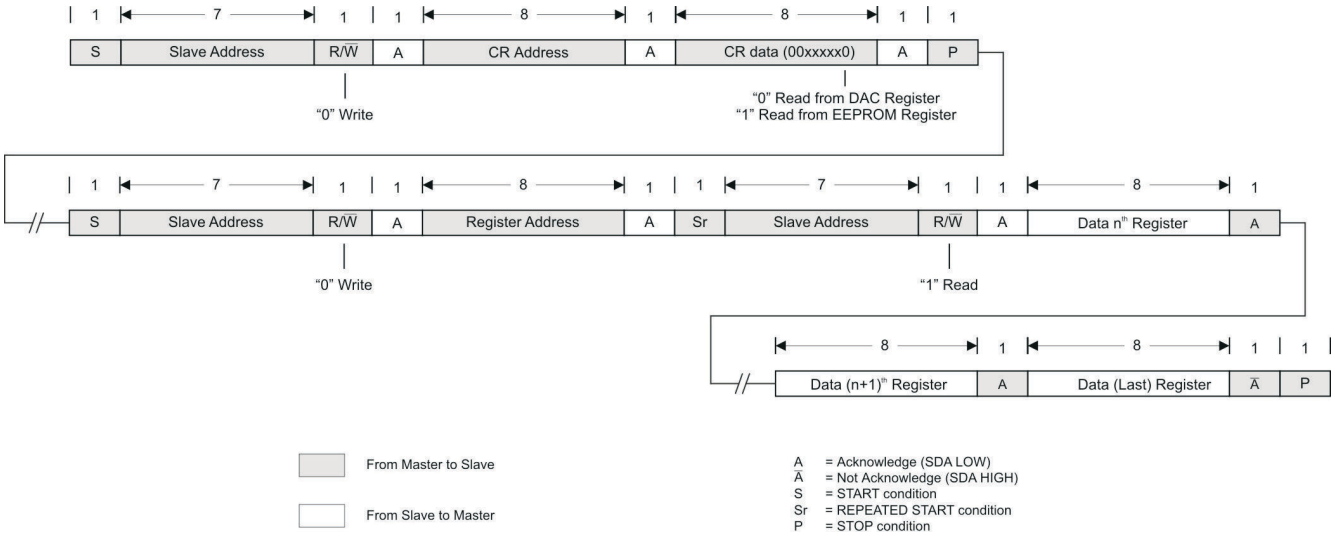
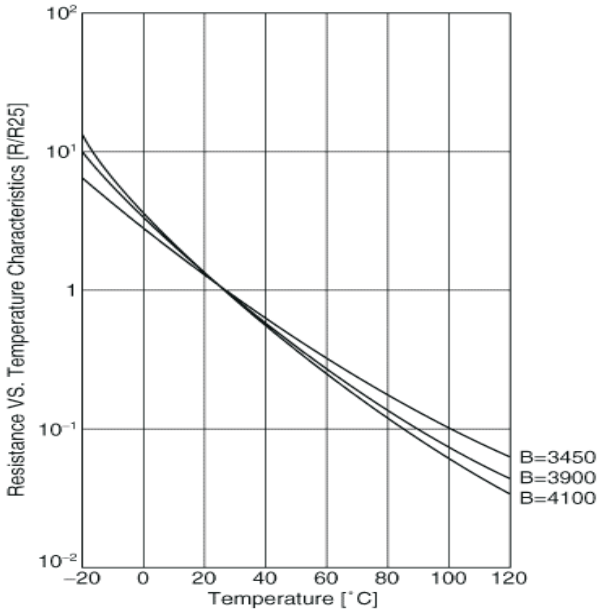


Figure 10-5. "Read" Data From DAC/EEPROM – Transfer Format in F/S-Mode Featuring Register Address Auto-Increment

10.3 Temperature Compensation

Table 10-1. NTC 47 kΩ – NCP18WB473F10RB – Characteristics

Global Part Number	NCP18WB473F10RB
Resistance (25°C)	47 kΩ ±1%
B-Constant (25/50°C)	4050K ±1.5%
B-Constant (25/80°C)(Reference Value)	4101K
B-Constant (25/85°C)(Reference Value)	4108K
B-Constant (25/100°C)(Reference Value)	4131K
Permissive Operating Current (25°C)	0.14mA
Rated Electric Power (25°C)	100mW
Typical Dissipation Constant (25°C)	1mW/°C
Min. Operating Temp. Range	–40°C
Max. Operating Temp. Range	125°C



10.4 PCB Layout Recommendations

- For **high dv/dt** signals (switch pin traces): keep copper to a minimum to prevent making unintentional parallel plate capacitors with other traces or to a ground plane. Best to route signal and return on same layer.
- For **high di/dt** signals: keep traces short, wide and closely spaced. This will reduce stray inductance and decrease the current loop area to help prevent EMI.
- Always avoid vias when possible. They have high inductance and resistance. **If vias are necessary always use more than one in parallel to decrease parasitics especially for power lines.**
- Keep input capacitor close to the IC with low inductance traces.
- **Keep the copper trace between a switch node and a diode as short and wide as possible.**
- **Use single point grounding.**
- **All AGND and PGND pins must be connected to the Power Pad.**
- Isolate analog signal paths from power paths.
- Keep trace from switching node pin to inductor short: **it reduces EMI emissions and noise that may couple into other portions of the converter.**
- Output voltage feedback sampling must be taken right at output capacitor and shielded.

11 Register Map

The TPS65175/A has one non-volatile memory which contains the initial value of the DAC and one volatile memory which contains the DAC setting. The non-volatile memory is called the Initial Value Register (IVR) and the volatile memory is called DAC Register (DR). The non-volatile IVR and the volatile DR are accessed with the same address.

Startup option: At power-up, the value contained in the IVR is loaded into the volatile DR and IVR presets the DAC to the last stored setting. The factory programmed value of the IVR of each address is described on Table 8-2 and, at power-up, these data byte set the output voltage of each rail.

Write description: The user has to program all data registers first (00h ~ 18h), then set the WED (Write EEPROM Data) bit to 1 once all desired data are addressed. A dead time of 50 ms is then initiated during which all the register data (00h ~ 18h) are stored into the non volatile EEPROM cell. During that time, there should be no data flowing through the I^2C because the I^2C interface is momentarily not responding.

After the 50 ms have passed, the WED bit is automatically reset to 0, and the user is able to read the values or program again.

Slave address:	0100000X
X = R/W	R/W = 1 → read mode
	R/W = 0 → write mode

Table 11-1. Register Map

REGISTER	NAME	ADDRESS	FACTORY VALUE	BIT COUNT	STEPS COUNT
VDD	Boost	00h	21h	6	64
VCC	Buck	01h	09h for TPS65175	4	13
			03h for TPS65175A		
VGH_LT	Positive charge pump - Low Temperature	02h	0Bh	4	16
VGH_HT	Positive charge pump - High Temperature	03h	0Bh	4	16
VGL	Negative charge pump	04h	20h	6	64
DLY0	Enable delay	05h	01h	3	8
DLY1	V_{GL} delay	06h	01h	3	8
DLY2	V_{DD} delay	07h	03h	3	8
DLY3	V_{GH} delay	08h	03h	3	8
GMA1	Gamma buffer 1	09h	01h	1	512
		0Ah	5Fh	8	
GMA2	Gamma buffer 2	0Bh	01h	1	512
		0Ch	06h	8	
GMA3	Gamma buffer 3	0Dh	00h	1	512
		0Eh	86h	8	
GMA4	Gamma buffer 4	0Fh	01h	1	512
		10h	86h	8	
GMA5	Gamma buffer 5	11h	01h	1	512
		12h	0Ch	8	
GMA6	Gamma buffer 6	13h	00h	1	512
		14h	9Fh	8	
VCOM	VCOM reference	15h	00h	1	391 / 211
		16h	DFh	8	
VCOM Operation	VCOM Output Range VCOM High Temperature VCOM Gain	17h	00h	8	256

Table 11-1. Register Map (continued)

REGISTER	NAME	ADDRESS	FACTORY VALUE	BIT COUNT	STEPS COUNT
VCOM Temp. + Osc. Freq.	VCOM Temp. Range Oscillator Frequency	18h	08h	4	16
CR	Control Register	FFh	–	8	1

12 DAC Registers

VDD Register (with factory value) – 00h (21h):

MSB			Address 001				LSB
Reserved	Reserved	1	0	0	0	0	1

VCC Register (with factory value) – 01h (09h): for TPS65175

MSB			Address 01h				LSB
Reserved	Reserved	Reserved	Reserved	1	0	0	1

VCC Register (with factory value) – 01h (03h): for TPS65175A

MSB			Address 01h				LSB
Reserved	Reserved	Reserved	Reserved	0	0	1	1

VGH_LT Register (with factory value) – 02h (0Bh):

MSB			Address 02h				LSB
Reserved	Reserved	Reserved	Reserved	1	0	1	1

VGH_HT Register (with factory value) – 03h (0Bh):

MSB			Address 03h				LSB
Reserved	Reserved	Reserved	Reserved	1	0	1	1

VGL Register (with factory value) – 04h (20h):

MSB			Address 04h				LSB
Reserved	Reserved	1	0	0	0	0	0

DLY0 Register (with factory value) – 05h (01h):

MSB			Address 05h				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	0	1

DLY1 Register (with factory value) – 06h (01h):

MSB			Address 06h				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	0	1

DLY2 Register (with factory value) – 06h (03h):

MSB			Address 06h				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	1	1

DLY3 Register (with factory value) – 07h (03h):

MSB				Address 07h			LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	1	1

GMA1 Register (with factory value) – 09h & 0Ah (01 – 5Fh):

MSB				Address 09h (MSB byte)			LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1

MSB				Address 0Ah (LSB byte)			LSB
0	1	0	1	1	1	1	1

GMA2 Register (with factory value) – 0Bh & 0Ch (01 – 06h):

MSB				Address 0Bh (MSB byte)			LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1

MSB				Address 0Ch (LSB byte)			LSB
0	0	0	0	0	1	1	0

GMA3 Register (with factory value) – 0Dh & 0Eh (00 – 86h):

MSB				Address 0Dh (MSB byte)			LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0

MSB				Address 0Eh (LSB byte)			LSB
1	0	0	0	0	1	1	0

GMA4 Register (with factory value) – 0Fh & 10h (01 – 86h):

MSB				Address 0Fh (MSB byte)			LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1

MSB				Address 10h (LSB byte)			LSB
1	0	0	0	0	1	1	0

GMA5 Register (with factory value) – 11h & 12h (01 – 0Ch):

MSB				Address 11h (MSB byte)			LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1

MSB				Address 12h (LSB byte)			LSB
0	0	0	0	1	1	0	0

GMA6 Register (with factory value) – 13h & 14h (00 – 9Fh):

MSB			Address 13h (MSB byte)				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0

MSB			Address 14h (LSB byte)				LSB
1	0	0	1	1	1	1	1

VCOM Register (with factory value) – 15h & 16h (00 – DFh):

MSB			Address 15h (MSB byte)				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0

MSB			Address 16h (LSB byte)				LSB
1	1	0	1	1	1	1	1

VCOM Operation Register (with factory value) – 17h (00h):

MSB			Address 17h				LSB
0	0	0	0	0	0	0	0

VCOM Temp. and Osc. Freq. Register (with factory value) – 18h (08h):

MSB			Address 18h				LSB
Reserved	Reserved	Reserved	Reserved	1	0	0	0

Control Register – FFh:

MSB			Address FFh				LSB
WED	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EE/(DR)

13 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2013) to Revision B (August 2025)	Page
• Updated numbering, formating, and section location to better align with current data sheet standard	1

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

15.1 Package Option Addendum

15.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TPS65175ARSHR	ACTIVE	VQFN	RSH	56	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS65175A
TPS65175RSHR	ACTIVE	VQFN	RSH	56	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS65175

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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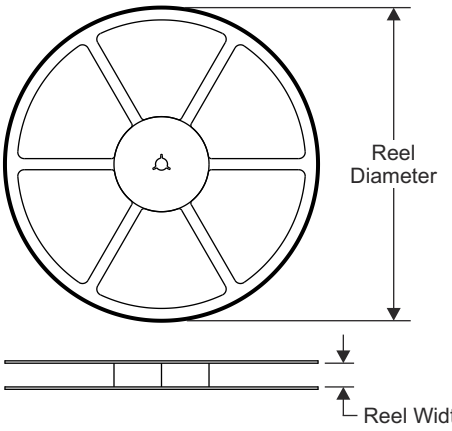
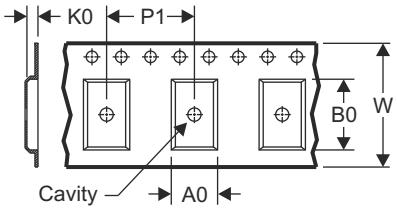
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

15.1.2 Tape and Reel Information

REEL DIMENSIONS

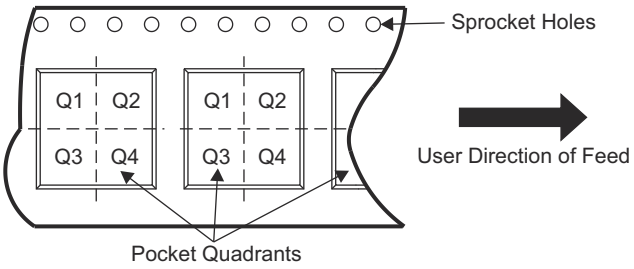


TAPE DIMENSIONS



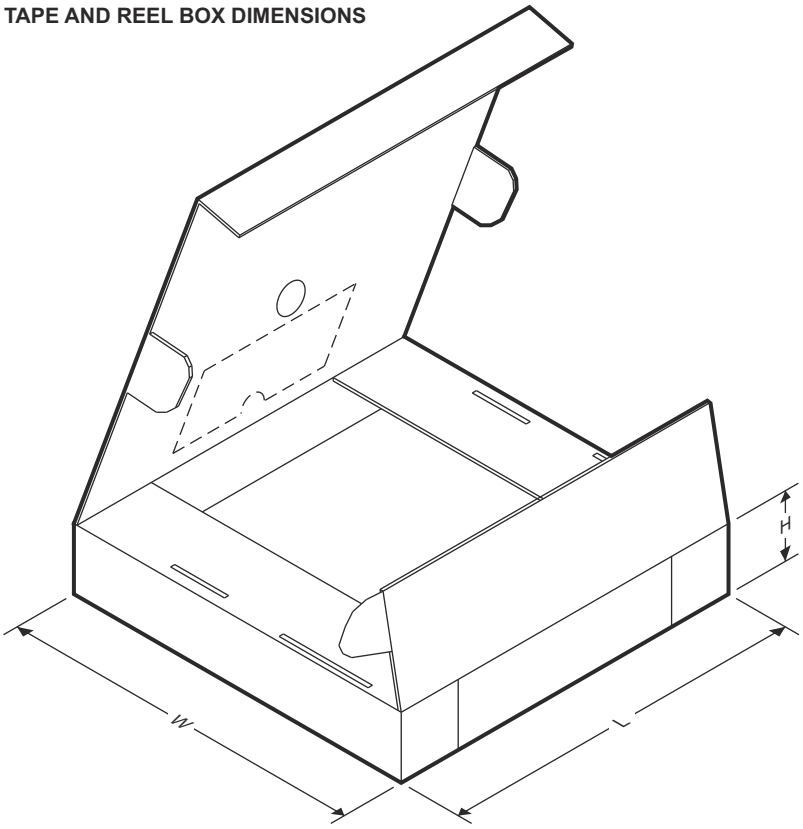
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



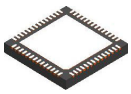
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65175ARSHR	VQFN	RSH	56	3000	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TPS65175RSHR	VQFN	RSH	56	3000	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65175ARSHR	VQFN	RSH	56	3000	367.0	367.0	38.0
TPS65175RSHR	VQFN	RSH	56	3000	367.0	367.0	38.0

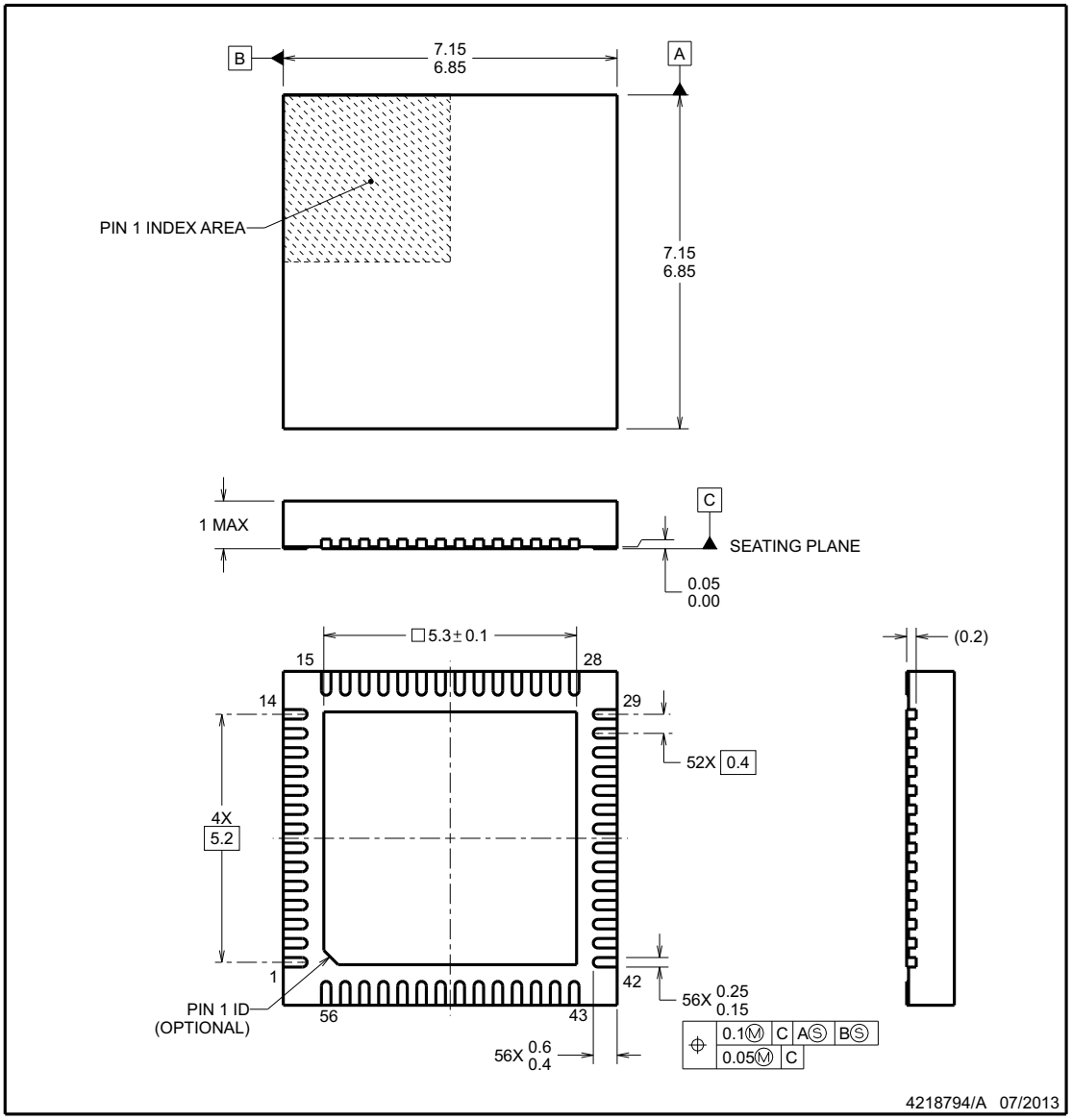
PACKAGE OUTLINE



RSH0056D

VQFN - 1 mm max height

VQFN



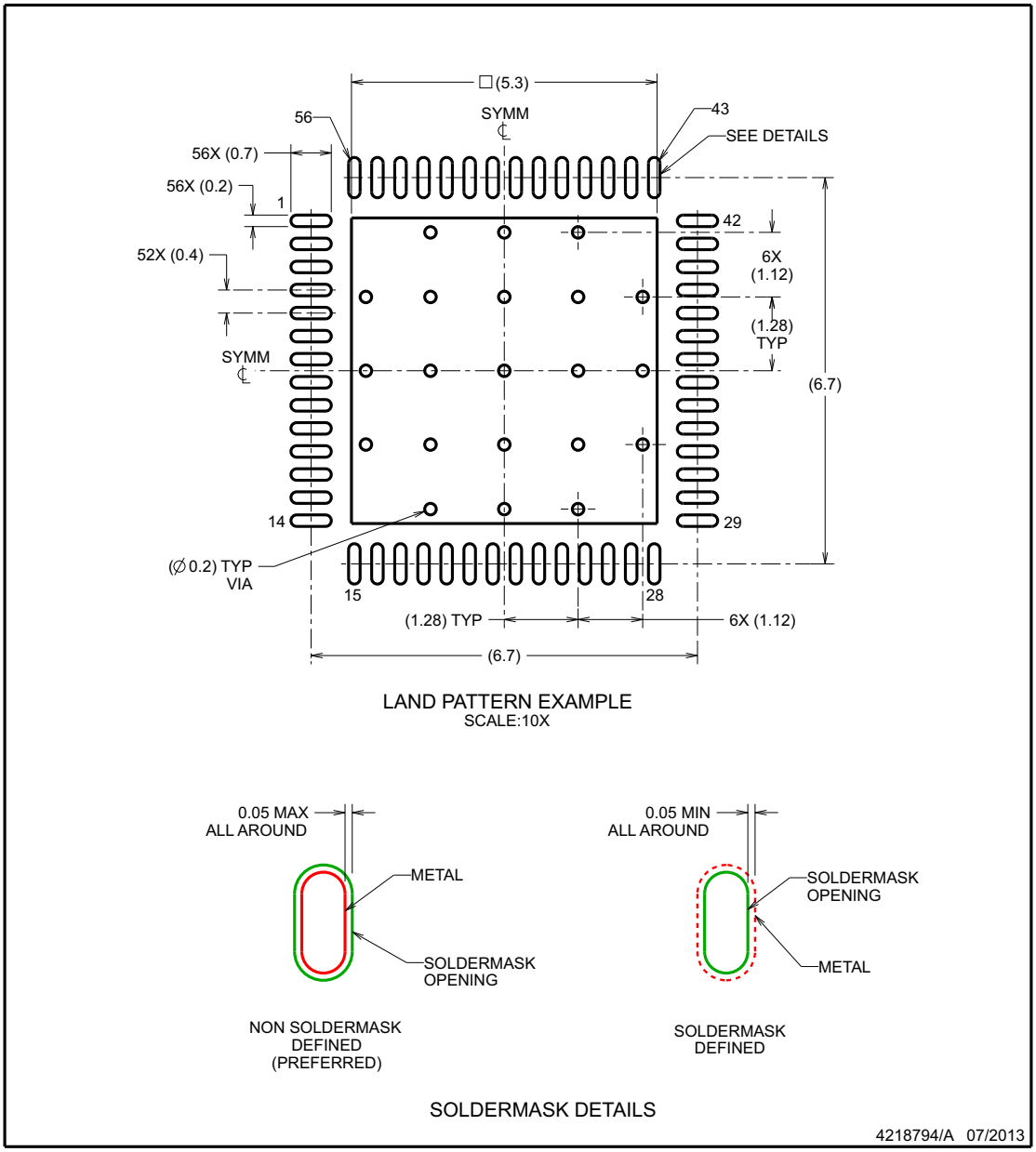
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RSH0056D — VQFN - 1 mm max height

VQFN



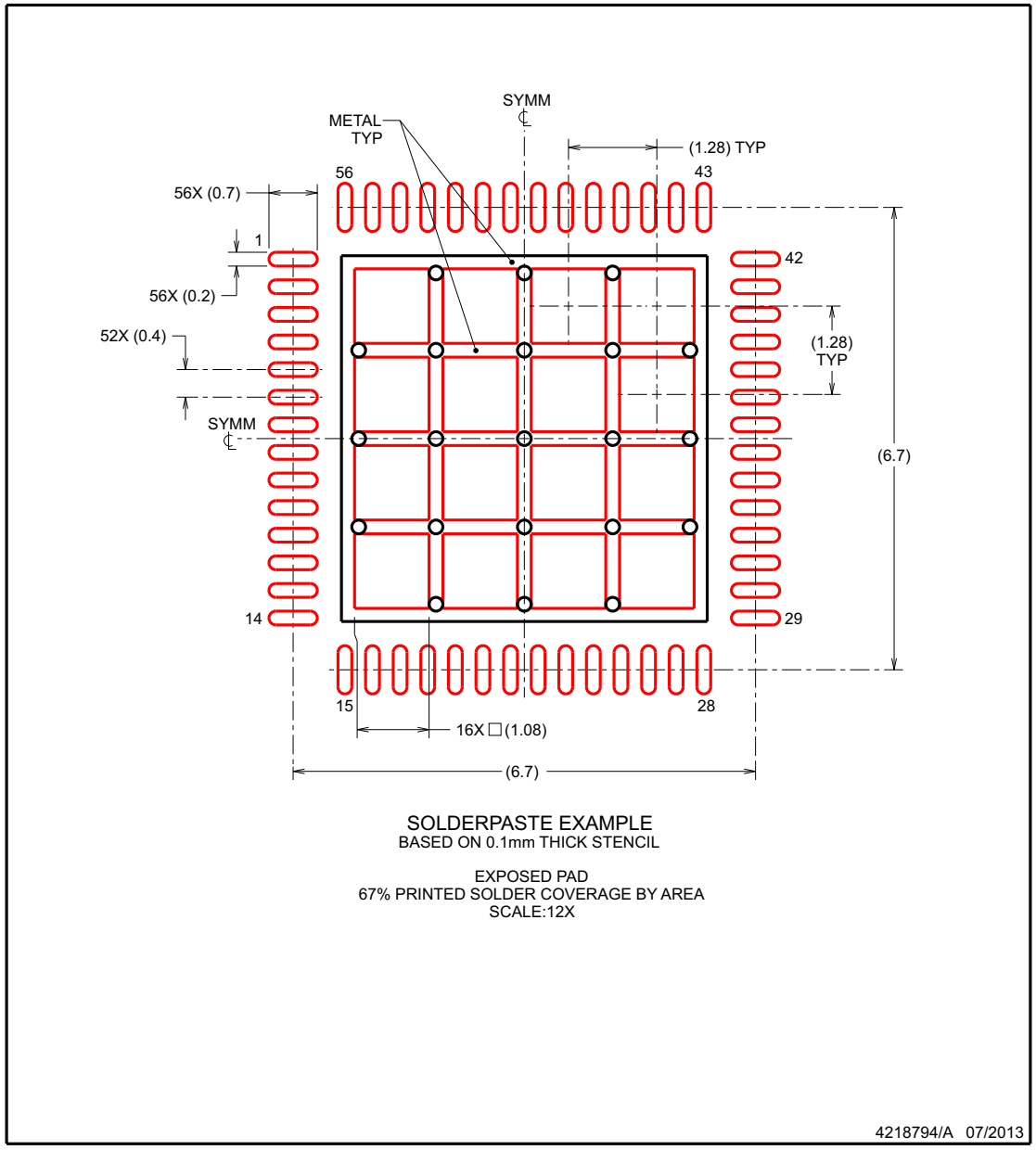
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RSH0056D — VQFN - 1 mm max height

VQFN



SOLDERPASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:12X

NOTES: (continued)

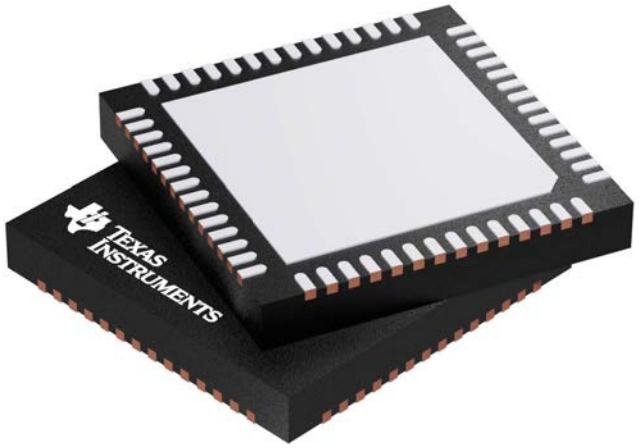
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

RSH 56

VQFN - 1 mm max height

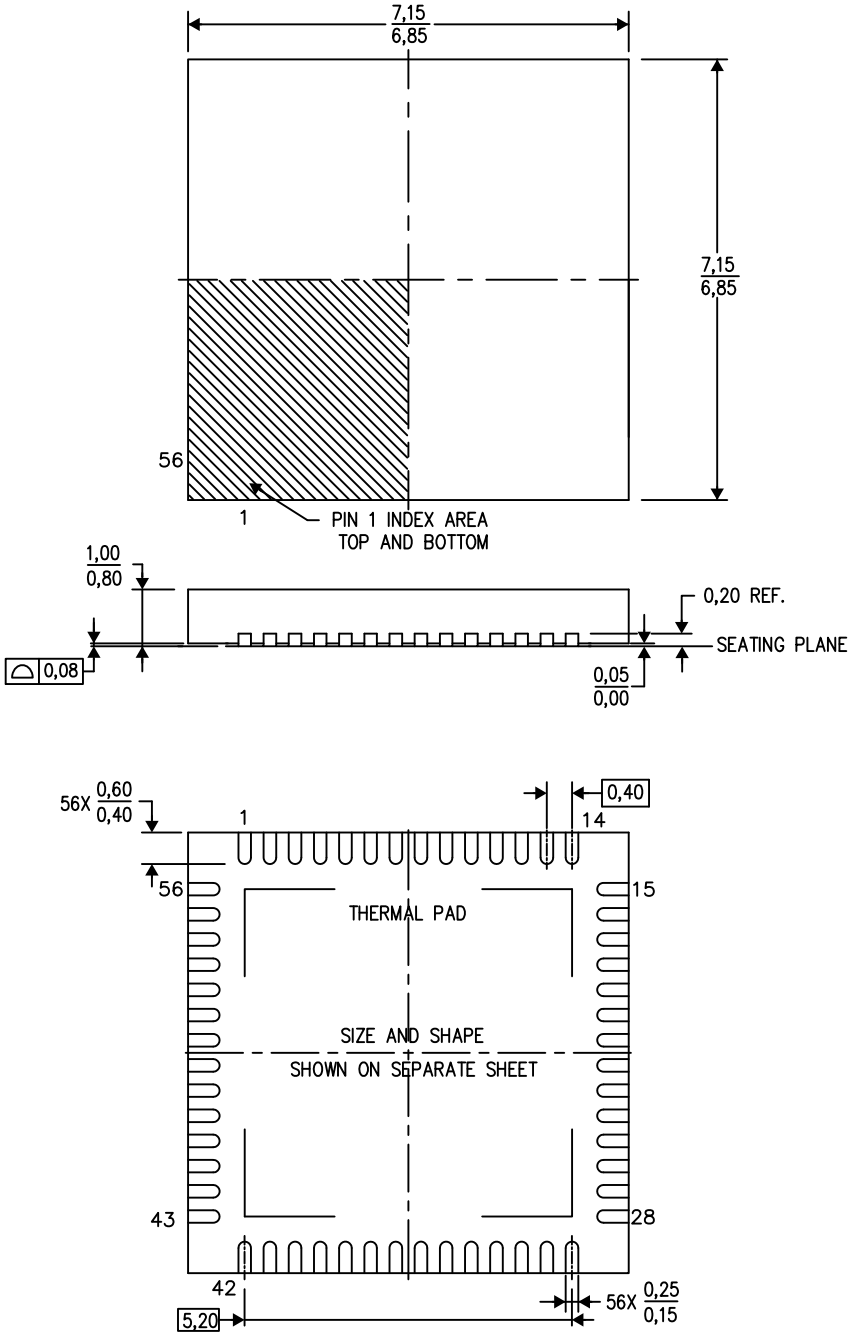
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207513/D

RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

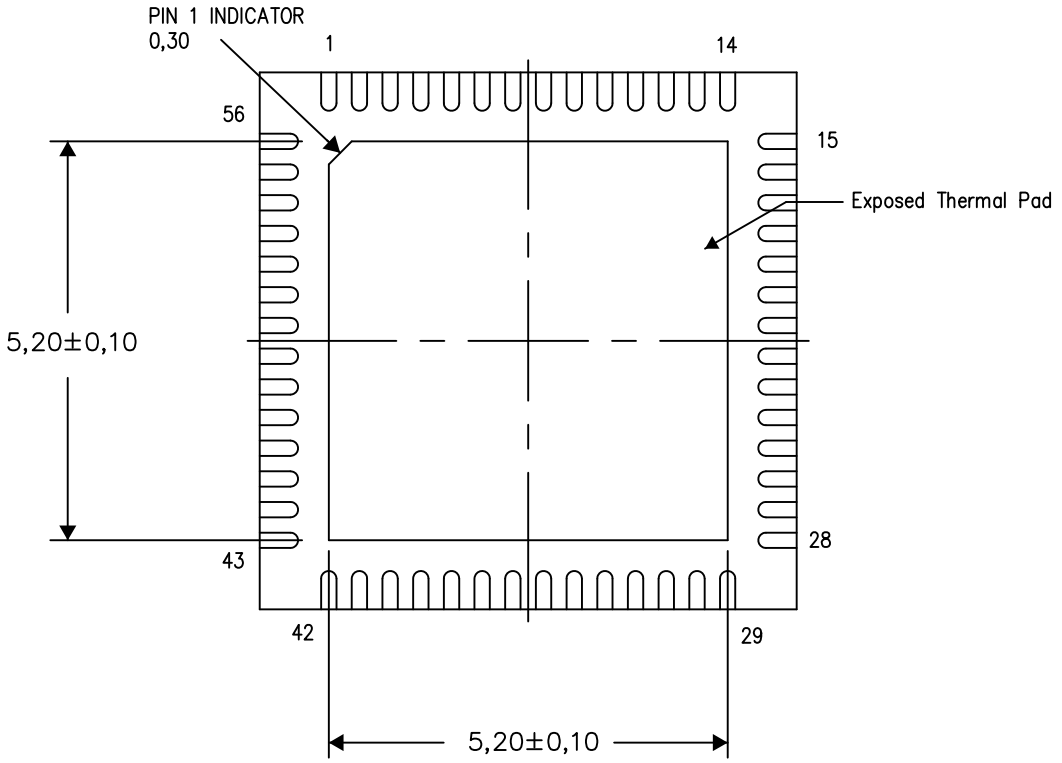
RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



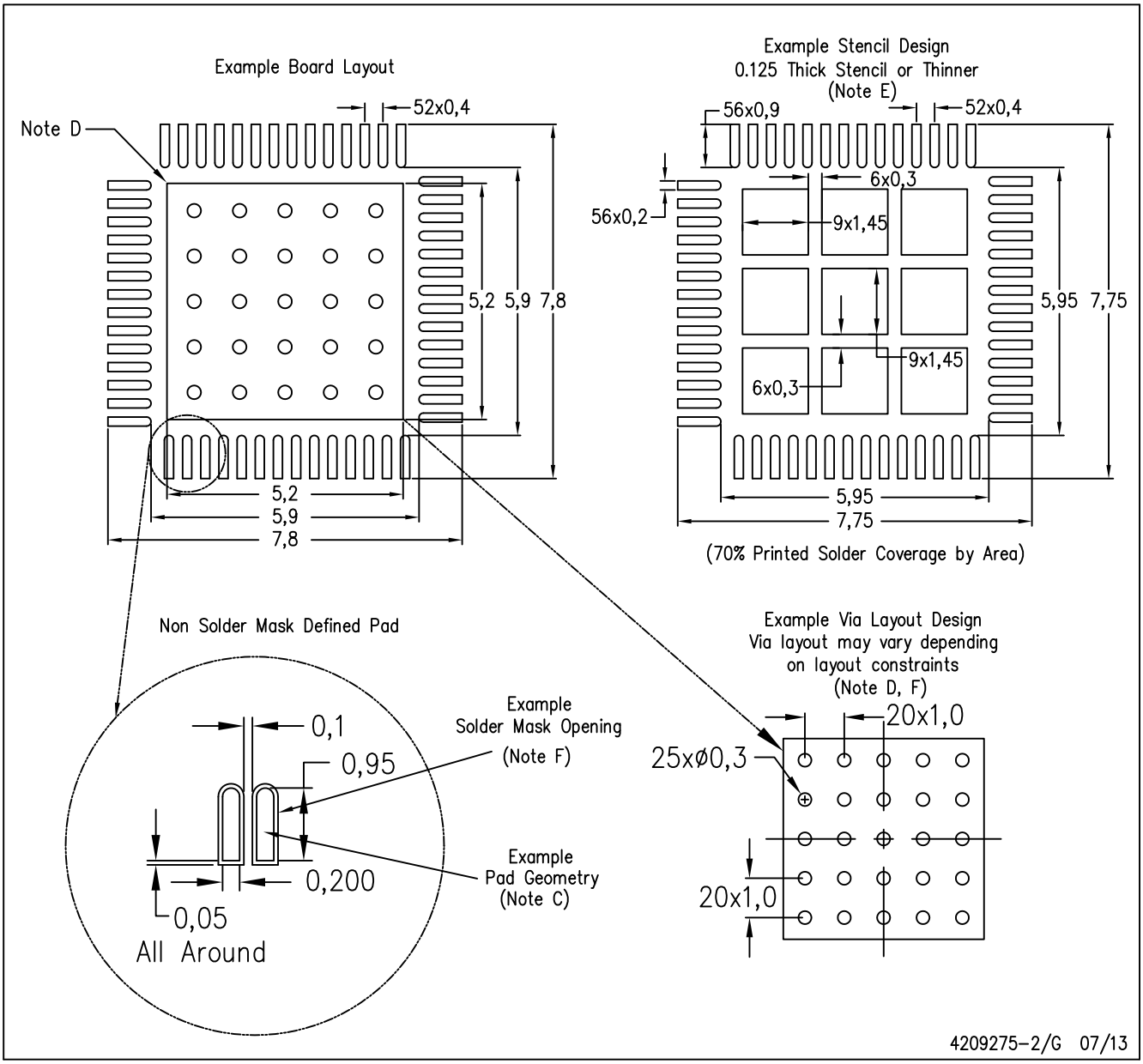
Bottom View

Exposed Thermal Pad Dimensions

4207553–2/I 07/13

NOTE: All linear dimensions are in millimeters

RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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