













TPS65023, TPS65023B

SLVS670L-JUNE 2006-REVISED MAY 2018

TPS65023x Power Management IC (PMIC) With 3 DC/DCs, 3 LDOs, I²C Interface and DVS

Features

- 1.7-A, 90% Efficient Step-Down Converter for Processor Core (VDCDC1)
- 1.2-A, Up to 95% Efficient Step-Down Converter for System Voltage (VDCDC2)
- 1.0-A, 92% Efficient Step-Down Converter for Memory Voltage (VDCDC3)
- 30-mA LDO and Switch for Real Time Clock (VRTC)
- 2 x 200-mA General-Purpose LDO
- Dynamic Voltage Management for Processor Core
- Preselectable LDO Voltage Using Two Digital Input Pins
- Externally Adjustable Reset Delay Time
- **Battery Backup Functionality**
- Separate Enable Pins for Inductive Converters
- I²C-Compatible Serial Interface
- I²C[™] Setup and Hold Timing:
 - TPS65023: 300 ns
 - TPS65023B: 100 ns
- 85-µA Quiescent Current
- Low Ripple PFM Mode
- Thermal Shutdown Protection
- 40-Pin, 5-mm x 5-mm WQFN Package

Applications

- Digital Media Players
- Internet Audio Players
- Digital Still Cameras
- **Smart Phones**
- Supply DaVinci™ DSP Family Solutions

3 Description

The TPS65023x device is an integrated power management IC for applications powered by one Li-Ion or Li-Polymer cell, which require multiple power rails. The TPS65023x provides three highly efficient, step-down converters targeted at providing the core voltage, peripheral, I/O, and memory rails in a processor-based system. The core converter allows on-the-fly voltage changes through interface, allowing the system to implement dynamic power savings. All three step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents.

The TPS65023x also integrates two general-purpose 200-mA LDO voltage regulators, which are enabled with an external input pin. Each LDO operates with an input voltage range from 1.5 V to 6.5 V, thus allowing them to be supplied from one of the stepdown converters or directly from the battery. The default output voltage of the LDOs can be digitally set to 4 different voltage combinations using the DEFLDO1 and DEFLDO2 pins. The serial interface can be used for dynamic voltage scaling, masking interrupts, or for disabling or enabling and setting the LDO output voltages. The interface is compatible with both the fast and standard mode I²C specifications, allowing transfers at up to 400 kHz. The TPS65023x is available in a 40-pin WQFN package, and operates over a free-air temperature of -40°C to 85°C.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
TPS65023	MOEN (40)	5.00 mm × 5.00 mm		
TPS65023B	WQFN (40)	5.00 mm x 5.00 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

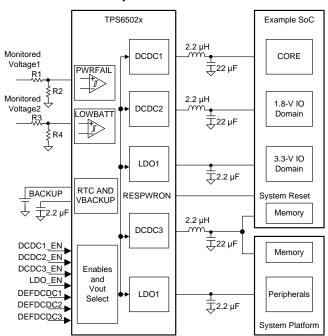




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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	hanges from Revision K (December 2015) to Revision L	Page
•	Changed the title of the data sheet	1
•	Replaced references of TI PowerPAD IC package with thermal pad	6
•	Added the Device Support and Documentation Support sections	46
•	Changed the Electrostatic Discharge Caution statement	46

Changes from Revision J (September 2011) to Revision K Page

 Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section

Changes from Revision I (July 2010) to Revision J Page

Changes from Revision H (December 2009) to Revision I Page • Added I²C Compatible Serial Interface to Features list 1 • Added TPS65023B device specs 1

Added ordering info for TPS65023B device.
 Added specs for TPS65023B device.





•	Changed "VBACKUP threshold" test condition typographical error from "VBACKUP falling" to "VBACKUP rising"	11
•	Added specs for TPS65023B device	
<u>-</u>	Added Differences table for TPS65023 and TPS65023B devices	39
Cł	hanges from Revision G (October 2008) to Revision H	Page
•	Changed I _{O(DCDC1)} MAX from: 1500 mA to: 1700 mA	7
•	Added High level input voltage for the SDAT pin	8
•	Changed I _O from:1500 mA MIN to 1700 mA	11
•	Changed I _O maximum from:1.5 A to: 1.7 A for VDCDC1 fixed and adjustable output voltage test condition specs	11
•	Changed I _O maximum from: 1500 mA to: 1700 mA for VDCDC1 Load Regulation test condition	11
•	Changed VDCDC1 "soft-start ramp time" spec to: "t _{Start} and t _{Ramp} " specifications with MIN TYP MAX values	11
•	Changed VDCDC2 "soft-start ramp time" spec To: "t _{Start} and t _{Ramp} " specifications with MIN TYP MAX values	12
•	Changed VDCDC3 "soft-start ramp time" spec To: "t _{Start} and t _{Ramp} " specifications with MIN TYP MAX values	13
•	Changed FBD graphic to show 1700 mA for DCDC1 Buck Converter	22
•	Changed text string from: "1.2 V or 1.8 V" to: "1.2 V to 1.6 V" in the STEP-DOWN CONVERTERS., VDCDC1 description.	24
•	Changed graphic entity to the one used in the Application Note SLVA273	
Cł	hanges from Revision F (July 2007) to Revision G	Page
•	Changed the Interrupt Management and the INT Pin section	28
Cl	hanges from Revision E (January 2007) to Revision F Changed text string from: "If it is tied to VCC, the default is 2.5 V" To: "If it is tied to VCC, the default is 3.3 V"	Page 24
CI	hanges from Revision D (December 2006) to Revision E	Page
•	Changed LDO1 output voltage range from: 3.3 to: 3.3	9
•	Changed text string from: "VDCDC2 converter defaults to 1.8 V or 2.5 V" to: "VDCDC2 converter defaults to 1.8 V or 3.3 V"	24
Cl	hanges from Revision C (October 2006) to Revision D	Page
•	Changed Typical Configuration for Ti DaVinci Processors	39
CI	hanges from Revision B (June 2006) to Revision C	Page
•	Changed from: AD Coupled to: AD Coupled - Figure 16	17
<u>.</u>	Changed from: AD Coupled to: AD Coupled - Figure 17	18
CI	hanges from Revision A (June 2006) to Revision B	Page
•	Changed from: 1.5A and 97% Efficient Step-Down to: 1.7A and 90% Efficient Step-Down	1
•	Changed from: 6 mm × 6 mm QFN Package to: 5 mm × 5 mm QFN Package	1
•	Changed from: RHA package to: RSB package	
•	Changed from: _{O(DCDC2)} to: I _{O(DCDC1)}	7
•	Changed Forward current limit - removed TBD and added values	11

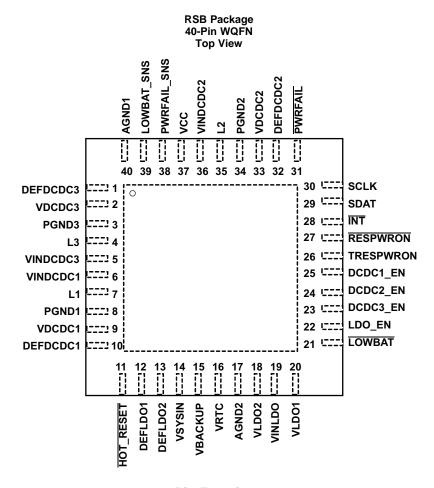
TPS65023, TPS65023B



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Changed Fixed output voltage - removed TBD and added values	11
Changed Fixed output voltage - removed TBD and added values	
Added VINDCDC3 = 3.6 V to Maximum output current	
Changed Fixed output voltage - removed TBD and added values	13
Changed Figure 3 (DVS Timing)	15
Changed Figure 11 (Graph - DCDC2: OUTPUT VOLTAGE)	
Added Figure 12 (Graph - DCDC3: OUTPUT VOLTAGE)	17
Changed Figure 20 (Graph - VDCDC2 OUTPUT VOLTAGE RIPPLE)	18
Added Reset Condition of DCDC1 Information	37
Changed Typical Configuration for Ti DaVinci Processors	39
Changed from: TPS65023 typically use a 3.3 μH output inductor to: TPS65023 typically use a 2.2 μH	output inductor 40
Changed from: VDCDC3 to: VDCDC1	41
Changed from: VDEFDCDC3 to: DEFDCDC1	41
Changed from: 2.5 V to 3.3 V (Table 20)	41
nanges from Original (May 2006) to Revision A	Page
Changed Electrical Characteristics: VDCDC1 Step-Down Converter	11
Changed Electrical Characteristics: VDCDC3 Step-Down Converter	12
Changed CON_CTRL Register Address - Column B0 default value changed from 1 to 0	33
Changed VDCDC# to VDCDC1	35



5 Pin Configuration and Functions



Pin Functions

PIN			DECORPTION					
NAME NO.		1/0	DESCRIPTION					
SWITCHING REG	SWITCHING REGULATOR SECTION							
AGND1	40	_	Analog ground. All analog ground pins are connected internally on the chip.					
AGND2	17	_	Analog ground. All analog ground pins are connected internally on the chip.					
DCDC1_EN	25	- 1	VDCDC1 enable pin. A logic high enables the regulator, a logic low disables the regulator.					
DCDC2_EN	24	I	VDCDC2 enable pin. A logic high enables the regulator, a logic low disables the regulator.					
DCDC3_EN	23	- 1	VDCDC3 enable pin. A logic high enables the regulator, a logic low disables the regulator.					
		Input signal indicating default VDCDC1 voltage, 0 = 1.2 V, 1 = 1.6 V DEFDCDC1 can also be connected to a resistor divider between VDCDC1 and GND, if the output voltage of the DCDC1 converter is set in a range from 0.6 V to VINDCDC1 V.						
		Input signal indicating default VDCDC2 voltage, 0 = 1.8 V, 1 = 3.3 V DEFDCDC2 can also be connected to a resistor divider between VDCDC2 and GND, if the output voltage of the DCDC2 converter is set in a range from 0.6 V to VINDCDC2 V.						
DEFDCDC3 1		ı	Input signal indicating default VDCDC3 voltage, 0 = 1.8 V, 1 = 3.3 V DEFDCDC3 can also be connected to a resistor divider between VDCDC3 and GND, if the output voltage of the DCDC3 converter is set in a range from 0.6 V to VINDCDC3 V.					
L1	7	_	Switch pin of VDCDC1 converter. The VDCDC1 inductor is connected here.					
L2	35	_	Switch pin of VDCDC2 converter. The VDCDC2 inductor is connected here.					
L3	4		Switch pin of VDCDC3 converter. The VDCDC3 inductor is connected here.					
PGND1	8	_	Power ground for VDCDC1 converter					

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Pin Functions (continued)

PIN			1 III I diletions (continued)
NAME	NO.	I/O	DESCRIPTION
PGND2	34	_	Power ground for VDCDC2 converter
PGND3	3	_	Power ground for VDCDC3 converter
VCC	37	I	Power supply for digital and analog circuitry of VDCDC1, VDCDC2, and VDCDC3 DC-DC converters. VCC must be connected to the same voltage supply as VINDCDC3, VINDCDC1, and VINDCDC2. VCC also supplies serial interface block.
VDCDC1	9	I	VDCDC1 feedback voltage sense input. Connect directly to VDCDC1
VDCDC2	33	1	VDCDC2 feedback voltage sense input. Connect directly to VDCDC2
VDCDC3	2	1	VDCDC3 feedback voltage sense input. Connect directly to VDCDC3
VINDCDC1	6	I	Input voltage for VDCDC1 step-down converter. VINDCDC1 must be connected to the same voltage supply as VINDCDC2, VINDCDC3, and VCC.
VINDCDC2	36	I	Input voltage for VDCDC2 step-down converter. VINDCDC2 must be connected to the same voltage supply as VINDCDC1, VINDCDC3, and VCC.
VINDCDC3	5	ı	Input voltage for VDCDC3 step-down converter. VINDCDC3 must be connected to the same voltage supply as VINDCDC1, VINDCDC2, and VCC.
Thermal Pad	_	_	Connect the power pad to analog ground
LDO REGULATOR	R SECTION	ON	
DEFLD01	12	Ι	Digital input. DEFLD01 sets the default output voltage of LDO1 and LDO2.
DEFLD02	13	I	Digital input. DEFLD02 sets the default output voltage of LDO1 and LDO2.
LDO_EN	22	- 1	Enable input for LDO1 and LDO2. A logic high enables the LDOs and a logic low disables the LDOs.
VBACKUP	15	I	Connect the backup battery to this input pin
VINLDO	19	I	Input voltage for LDO1 and LDO2
VLDO1	20	0	Output voltage of LDO1
VLDO2	18	0	Output voltage of LDO2
VRTC	16	0	Output voltage of the LDO and switch for the real time clock
VSYSIN	14	I	Input of system voltage for VRTC switch
CONTROL AND I ²	C SECT	ION	
HOT_RESET	11	I	Push button input that reboots or wakes up the processor through the RESPWRON output pin.
ĪNT	28	0	Open-drain output
LOW_BAT	21	0	Open-drain output of LOW_BAT comparator
LOWBAT_SNS	39	I	Input for the comparator driving the LOW_BAT output.
PWRFAIL	31	0	Open-drain output. Active low when PWRFAIL comparator indicates low VBAT condition.
PWRFAIL_SNS	38	I	Input for the comparator driving the PWRFAIL output
RESPWRON	27	0	Open-drain system reset output
SCLK	30	I	Serial interface clock line
SDAT	29	I/O	Serial interface data and address
TRESPWRON	26	I	Connect the timing capacitor to TRESPWRON to set the reset delay time: 1 nF → 100 ms

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
VI	Input voltage on all pins except AGND and PGND pins with respect to AGND	-0.3	7	V
	Current at VINDCDC1, L1, PGND1, VINDCDC2, L2, PGND2, VINDCDC3, L3, PGND3		2000	mA
	Peak current at all other pins		1000	mA
	Continuous total power dissipation	See Therma	I Information	
T _A	Operating free-air temperature	-40	85	°C
T _J	Maximum junction temperature		125	°C
T _{stg}	Storage temperature	-65	150	°C

⁽¹⁾ Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V	Flootrootatio dipoharas	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	\/
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Input voltage step-down converters (VINDCDC1, VINDCDC2, VINDCDC3); pins need to be tied to the same voltage rail	2.5		6	V
	Output voltage for VDCDC1 step-down converter ⁽¹⁾	0.6		VINDCDC1	
Vo	Output voltage for VDCDC2 step-down converter ⁽¹⁾	0.6		VINDCDC2	V
	Output voltage for VDCDC3 step-down converter ⁽¹⁾	0.6		VINDCDC3	
VI	Input voltage for LDOs (VINLDO1, VINLDO2)	1.5		6.5	V
Vo	Output voltage for LDOs (VLDO1, VLDO2)	1		VINLDO1-2	V
I _{O(DCDC1)}	Output current at L1			1700	mA
	Inductor at L1 (2)	1.5	2.2		μН
C _{I(DCDC1)}	Input capacitor at VINDCDC1 (2)	10			μF
C _{O(DCDC1)}	Output capacitor at VDCDC1 (2)	10	22		μF
I _{O(DCDC2)}	Output current at L2			1200	mA
	Inductor at L2 (2)	1.5	2.2		μН
C _{I(DCDC2)}	Input capacitor at VINDCDC2 (2)	10			μF
C _{O(DCDC2)}	Output capacitor at VDCDC2 (2)	10	22		μF
I _{O(DCDC3)}	Output current at L3			1000	mA
	Inductor at L3 (2)	1.5	2.2		μН
C _{I(DCDC3)}	Input capacitor at VINDCDC3 (2)	10			μF
C _{O(DCDC3)}	Output capacitor at VDCDC3 (2)	10	22		μF
C _{I(VCC)}	Input capacitor at VCC (2)	1			μF
C _{i(VINLDO)}	Input capacitor at VINLDO (2)	1			μF
C _{O(VLDO1-2)}	Output capacitor at VLDO1, VLDO2 (2)	2.2			μF

⁽¹⁾ When using an external resistor divider at DEFDCDC3, DEFDCDC2, and DEFDCDC1

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

⁽²⁾ See *Application Information* section for more information.



Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I _{O(VLDO1-2)}	Output current at VLDO1, VLDO2			200	mA
C _{O(VRTC)}	Output capacitor at VRTC (2)	4.7			μF
T _A	Operating ambient temperature	-40		85	°C
TJ	Operating junction temperature	-40		125	°C
	Resistor from VINDCDC3, VINDCDC2, VINDCDC1 to VCC used for filtering (3)		1	10	Ω

⁽³⁾ Up to 3 mA can flow into V_{CC} when all 3 converters are running in PWM. This resistor causes the UVLO threshold to be shifted accordingly.

6.4 Thermal Information

		TPS65023x	
	THERMAL METRIC ⁽¹⁾	RSB (WQFN)	UNIT
		40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	°C/W
ΨЈТ	Junction-to-top characterization parameter	0.1	°C/W
ΨЈВ	Junction-to-board characterization parameter	5.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, $T_A = -40 ^{\circ}\text{C}$ to $85 ^{\circ}\text{C}$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
CONTROL SIG	NALS: SCLK, SDAT (INPUT) FOR TPS65023					
V _{IH}	High level input voltage (except the SDAT pin)	Resistor pullup at SCLK = 4.7 k Ω , pulled to VRTC	1.3		V _{CC}	V
V _{IH}	High level input voltage for the SDAT pin	Resistor pullup at SDAT = 4.7 k Ω , pulled to VRTC	1.45		V _{CC}	V
V _{IL}	Low level input voltage	Resistor pullup at SCLK and SDAT = 4.7 k Ω , pulled to VRTC	0		0.4	V
I _H	Input bias current			0.01	0.1	μА
CONTROL SIG	NALS: SCLK, SDAT (INPUT) FOR TPS65023B					
V _{IH}	High level input voltage for the SCLK pin	Rpullup at SCLK = 4.7 k Ω , pulled to VRTC; For V _{CC} = 2.5 V to 5.25 V	1.4		V _{CC}	V
V _{IH}	High level input voltage for the SDAT pin	Rpullup at SDAT = 4.7 k Ω , pulled to VRTC; For V _{CC} = 2.5 V to 5.25 V	1.69		V _{CC}	V
V _{IH}	High level input voltage for the SDAT pin	Rpullup at SDAT = 4.7 k Ω , pulled to VRTC; For V _{CC} = 2.5 V to 4.5 V	1.55		V _{cc}	V
V _{IL}	Low level input voltage	Rpullup at SCLK and SDAT = 4.7 k Ω , pulled to VRTC	0		0.35	V
I _H	Input bias current			0.01	0.1	μА
CONTROL SIG	NALS: HOT_RESET, DCDC1_EN, DCDC2_EN, DCD	DC3_EN, LDO_EN, DEFLDO1, DEFLDO2				
V _{IH}	High-level input voltage		1.3		V _{CC}	V
V _{IL}	Low-level input voltage		0		0.4	V
I _{IB}	Input bias current			0.01	0.1	μА
t _{deglitch}	Deglitch time at HOT_RESET		25	30	35	ms

(1) Typical values are at $T_A = 25$ °C, unless otherwise noted.

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Electrical Characteristics (continued)

 $VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 \ V, \ VBACKUP = 3 \ V, \ T_A = -40 ^{\circ}C \ to \ 85 ^{\circ}C \ (unless \ otherwise \ noted)$

noteu)	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
CONTROL SIGNALS: L	OWBAT, PWRFAIL, RESPWRON, INT, SDA	AT (OUTPUT)				
V _{OH}	High-level output voltage				6	V
V _{OL}	Low-level output voltage	I _{IL} = 5 mA	0		0.3	V
	Duration of low pulse at RESPWRON	External capacitor 1 nF		100		ms
ICONST	Internal charge / discharge current on pin TRESPWRON	Used for generating RESPWRON delay	1.7	2	2.3	μΑ
TRESPWRON_LOWTH	Internal lower comparator threshold on pin TRESPWRON	Used for generating RESPWRON delay	0.225	0.25	0.275	V
TRESPWRON_UPTH	Internal upper comparator threshold on pin TRESPWRON	Used for generating RESPWRON delay	0.97	1	1.103	V
	Resetpwron threshold	VRTC falling	-3%	2.4	3%	V
	Resetpwron threshold	VRTC rising	-3%	2.52	3%	V
I _{LK}	Leakage current	Output inactive high			0.1	μА
VLDO1 AND VLDO2 LO	W DROPOUT REGULATORS					
VI	Input voltage range for LDO1, 2		1.5		6.5	V
V _{O(LD01)}	LDO1 output voltage range		1		3.15	V
V _{O(LDO2)}	LDO2 output voltage range		1		3.3	V
	Maximum output current for LDO1,	V _I = 1.8 V, V _O = 1.3 V	200			A
lo	LDO2	V _I = 1.5 V, V _O = 1.3 V		120		mA
I _(SC)	LDO1 and LDO2 short-circuit current limit	$V_{(LDO1)} = GND, V_{(LDO2)} = GND$			400	mA
		I _O = 50 mA, VINLDO = 1.8 V			120	
	Minimum voltage drop at LDO1, LDO2	I _O = 50 mA, VINLDO = 1.5 V		65	150	mV
		I _O = 200 mA, VINLDO = 1.8 V			300	
	Output voltage accuracy for LDO1, LDO2	I _O = 10 mA	-2%		1%	
	Line regulation for LDO1, LDO2	VINLDO1, 2 = VLDO1,2 + 0.5 V (min. 2.5 V) to 6.5 V, I _O = 10 mA	-1%		1%	
	Load regulation for LDO1, LDO2	I _O = 0 mA to 50 mA	-1%		1%	
	Regulation time for LDO1, LDO2	Load change from 10% to 90%		10		μS
ANALOGIC SIGNALS D	EFDCDC1, DEFDCDC2, DEFDCDC3		<u> </u>		,	
V _{IH}	High-level input voltage		1.3		VCC	V
V _{IL}	Low-level input voltage		0		0.1	V
	Input bias current			0.001	0.05	μΑ
THERMAL SHUTDOWN						
T _(SD)	Thermal shutdown	Increasing junction temperature		160		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C
INTERNAL UNDERVOL	TAGE LOCK OUT					
UVLO	Internal UVLO	VCC falling	-2%	2.35	2%	V
V _(UVLO_HYST)	Internal UVLO comparator hysteresis			120		mV
VOLTAGE DETECTOR	COMPARATORS				1.	
	Comparator threshold (PWRFAIL_SNS, LOWBAT_SNS)	Falling threshold	-1%	1	1%	٧
	Hysteresis		40	50	60	mV
	Propagation delay	25-mV overdrive			10	μS
POWER-GOOD			*			
V _(PGOODF)		VDCDC1, VDCDC2, VDCDC3, VLDO1, VLDO2, decreasing	-12%	-10%	-8%	
V _(PGOODR)		VDCDC1, VDCDC2, VDCDC3, VLDO1, VLDO2, increasing	-7%	-5%	-3%	



6.6 Electrical Characteristics: Supply Pins VCC, VINDCDC1, VINDCDC2, VINDCDC3

 $VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 \text{ V}, VBACKUP = 3 \text{ V}, T_A = -40 ^{\circ}\text{C} \text{ to } 85 ^{\circ}\text{C} \text{ (unless otherwise } 1.0 ^{\circ}\text{C} \text{ (unless otherwis$ noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
	Operating guidecent	All 3 DCDC converters enabled, zero load, and no switching, LDOs enabled	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)} = 0 \text{ V}$		85	100	
		All 3 DCDC converters enabled, zero load, and no switching, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)} = 0 \text{ V}$		78	90	
Operating quiescent current, PFM	DCDC1 and DCDC2 converters enabled, zero load, and no switching, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)} = 0 \text{ V}$		57	70	μА	
		DCDC1 converter enabled, zero load, and no switching, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)} = 0 \text{ V}$		43	43 55	
		All 3 DCDC converters enabled and running in PWM, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)} = 0 \text{ V}$		2	3	
II	Current into VCC; PWM	DCDC1 and DCDC2 converters enabled and running in PWM, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)} = 0 \text{ V}$		1.5	2.5	mA
		VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)} = 0 \text{ V}$		0.85	2		
			VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)} = 0 \text{ V}$		23	33	μА
$I_{(q)}$	Quiescent current	All converters disabled, LDOs off	VCC = 2.6 V, VBACKUP = 3 V; $V_{(VSYSIN)} = 0 \text{ V}$		3.5	5	μΑ
			VCC = 3.6 V, VBACKUP = 0 V; $V_{(VSYSIN)} = 0 \text{ V}$			43	μА

⁽¹⁾ Typical values are at $T_A = 25$ °C, unless otherwise noted.

6.7 Electrical Characteristics: Supply Pins VBACKUP, VSYSIN, VRTC, VINLDO

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = -40°C to 85°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
VBAC	KUP, VSYSIN, VRTC					
I _(q)	Operating quiescent current	VBACKUP = 3 V, VSYSIN = 0 V; VCC = 2.6 V, current into VBACKUP		20	33	μА
$I_{(SD)}$	Operating quiescent current	VBACKUP < V_VBACKUP, current into VBACKUP		2	3	μΑ
	VRTC LDO output voltage	VSYSIN = VBACKUP = 0 V, I _O = 0 mA		3		V
lo	Output current for VRTC	VSYSIN < 2.57 V and VBACKUP < 2.57 V			30	mA
	VRTC short-circuit current limit	VRTC = GND; VSYSIN = VBACKUP = 0 V			100	mA
	Maximum output current at VRTC for RESPWRON = 1	$VRTC > 2.6 \text{ V}, V_{CC} = 3 \text{ V};$ VSYSIN = VBACKUP = 0 V	30			mA
Vo	Output voltage accuracy for VRTC	VSYSIN = VBACKUP = 0 V; I _O = 0 mA	-1%		1%	
	Line regulation for VRTC	VCC = VRTC + 0.5 V to 6.5 V, $I_O = 5 \text{ mA}$	-1%		1%	
	Load regulation VRTC	$I_O = 1$ mA to 30 mA; VSYSIN = VBACKUP = 0 V	-3%		1%	
	Regulation time for VRTC	Load change from 10% to 90%		10		μS
I _{lkg}	Input leakage current at VSYSIN	VSYSIN < V_VSYSIN			2	μΑ
	r _{DS(on)} of VSYSIN switch				12.5	Ω
	r _{DS(on)} of VBACKUP switch				12.5	Ω
	Input voltage range at VBACKUP ⁽²⁾		2.73		3.75	V
	Input voltage range at VSYSIN (2)		2.73		3.75	V
	VSYSIN threshold	VSYSIN falling	-3%	2.55	3%	V

⁽¹⁾ Typical values are at $T_A = 25$ °C, unless otherwise noted.

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Based on the requirements for the Intel PXA270 processor. (2)



Electrical Characteristics: Supply Pins VBACKUP, VSYSIN, VRTC, VINLDO (continued)

 $VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 \ V, \ VBACKUP = 3 \ V, \ T_A = -40 ^{\circ}C \ to \ 85 ^{\circ}C \ (unless \ otherwise \ noted)$

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
	VSYSIN threshold	VSYSIN rising	-3%	2.65	3%	V
	VBACKUP threshold	VBACKUP falling	-3%	2.55	3%	V
	VBACKUP threshold	VBACKUP rising	-3%	2.65	3%	V
VINLDO)					
I _(q)	Operating quiescent current	Current per LDO into VINLDO for LDO_CTRL = 0x0		16	30	μΑ
I _(SD)	Shutdown current	Total current for both LDOs into VINLDO, VLDO = 0 V		0.1	1	μΑ

6.8 Electrical Characteristics: VDCDC1 Step-Down Converter

 $VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 \ V, \ VBACKUP = 3 \ V, \ T_A = -40 ^{\circ}C \ to \ 85 ^{\circ}C \ (unless \ otherwise \ noted)$

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
VI	Input voltage range, VIND	CDC1		2.5		6	V
Io	Maximum output current			1700			mA
I _(SD)	Shutdown supply current i	n VINDCDC1	DCDC1_EN = GND		0.1	1	μΑ
r _{DS(on)}	P-channel MOSFET on-re	sistance	VINDCDC1 = V _(GS) = 3.6 V		125	261	mΩ
I _{lkg}	P-channel leakage current	t	VINDCDC1 = 6 V			2	μΑ
r _{DS(on)}	N-channel MOSFET on-re	sistance	VINDCDC1 = V _(GS) = 3.6 V		130	260	mΩ
I _{lkg}	N-channel leakage curren	t	V _(DS) = 6 V		7	10	μΑ
	Forward current limit (P-ch N-channel)	nannel and	2.5 V < V _{I(MAIN)} < 6 V	1.94	2.19	2.44	Α
f _S	Oscillator frequency			1.95	2.25	2.55	MHz
	Fixed output voltage FPWMDCDC1 = 0	- All VDCDC1	VINDCDC1 = 2.5 V to 6 V; 0 mA \leq I _O \leq 1.7 A	-2%		2%	
	Fixed output voltage FPWMDCDC1 = 1	All VDCDC1	VINDCDC1 = 2.5 V to 6 V; $0 \text{ mA} \le I_O \le 1.7 \text{ A}$	-1%		1%	l
	Adjustable output voltage at DEFDCDC1; FPWMDC		VINDCDC1 = VDCDC1 + 0.5 V (min 2.5 V) to 6 V; 0 mA \leq I _O \leq 1.7 A	-2%		2%	
	Adjustable output voltage at DEFDCDC1; FPWMDC		VINDCDC1 = VDCDC1 + 0.5 V (min 2.5 V) to 6 V; 0 mA \leq I _O \leq 1.7 A	-1%		1%	
	Line Regulation		VINDCDC1 = VDCDC1 + 0.3 V (min. 2.5 V) to 6 V; I _O = 10 mA		0%		V
	Load Regulation		I _O = 10 mA to 1700 mA		0.25%		Α
t _{Start}	Start-up time		Time from active EN to start switching	145	175	200	μS
t _{Ramp}	V _{OUT} ramp-up time		Time to ramp from 5% to 95% of V _{OUT}	400	750	1000	μS
	Internal resistance from L	I to GND			1		ΜΩ
	VDCDC1 discharge resista	ance	DCDC1 discharge = 1		300		Ω

⁽¹⁾ Typical values are at $T_A = 25$ °C, unless otherwise noted.



6.9 Electrical Characteristics: VDCDC2 Step-Down Converter

 $VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 \text{ V}, VBACKUP = 3 \text{ V}, T_A = -40 ^{\circ}\text{C} \text{ to } 85 ^{\circ}\text{C} \text{ (unless otherwise } 1.0 ^{\circ}\text{C} \text{ (unless otherwis$ noted)

	PARAMETE	R	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
VI	Input voltage range, VI	NDCDC2		2.5		6	V
			DEFDCDC2 = GND	1200			
lo	Maximum output curre	nt	VINDCDC2 = 3.6 V; 3.3 V - 1% ≤ VDCDC2 ≤ 3.3V + 1%	1000			mA
$I_{(SD)}$	Shutdown supply curre	ent in VINDCDC2	DCDC2_EN = GND		0.1	1	μΑ
r _{DS(on)}	P-channel MOSFET or	n-resistance	VINDCDC2 = $V_{(GS)}$ = 3.6 V		140	300	$\text{m}\Omega$
I _{lkg}	P-channel leakage cur	rent	VINDCDC2 = 6 V			2	μΑ
r _{DS(on)}	N-channel MOSFET or	n-resistance	VINDCDC2 = $V_{(GS)}$ = 3.6 V		150	297	$m\Omega$
I _{lkg}	N-channel leakage cur	rent	V _(DS) = 6 V		7	10	μΑ
I _{LIMF}	Forward current limit (I channel)	P-channel and N-	2.5 V < VINDCDC2 < 6 V	1.74	1.94	2.12	Α
f_S	Oscillator frequency			1.95	2.25	2.55	MHz
	Fixed output voltage FPWMDCDC2=0	VDCDC2 = 1.8 V	VINDCDC2 = 2.5 V to 6 V; $0 \text{ mA} \le I_0 \le 1.2 \text{ A}$	-2%		2%	
		VDCDC2 = 3.3 V	VINDCDC2 = 3.7 V to 6 V; $0 \text{ mA} \le I_0 \le 1.2 \text{ A}$	-1%		1%	
	Fixed output voltage	VDCDC2 = 1.8 V	VINDCDC2 = 2.5 V to 6 V; $0 \text{ mA} \le I_O \le 1.2 \text{ A}$	-2%		2%	
	FPWMDCDC2=1	VDCDC2 = 3.3 V	VINDCDC2 = 3.7 V to 6 V; $0 \text{ mA} \le I_0 \le 1.2 \text{ A}$	-1%		1%	
	Adjustable output volta divider at DEFDCDC2		VINDCDC2 = VDCDC2 + 0.3 V (min 2.5 V) to 6 V; 0 mA \leq I _O \leq 1 A	-2%		2%	
	Adjustable output volta divider at DEFDCDC2;		VINDCDC2 = VDCDC2 + 0.3 V (min 2.5 V) to 6 V; 0 mA \leq I $_{0} \leq$ 1 A	-1%		1%	
	Line Regulation		VINDCDC2 = VDCDC2 + 0.3 V (min. 2.5 V) to 6 V; I _O = 10 mA		0%		V
	Load Regulation		I _O = 10 mA to 1000 mA		0.25%		Α
t _{Start}	Start-up time		Time from active EN to start switching	145	175	200	μs
t _{Ramp}	V _{OUT} ramp-up time		Time to ramp from 5% to 95% of V _{OUT}	400	750	1000	μS
-	Internal resistance from	n L2 to GND			1		МΩ
	VDCDC2 discharge re	sistance	DCDC2 discharge =1		300		Ω

⁽¹⁾ Typical values are at $T_A = 25$ °C, unless otherwise noted.

6.10 Electrical Characteristics: VDCDC3 Step-Down Converter

 $VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 \text{ V}, VBACKUP = 3 \text{ V}, T_A = -40 ^{\circ}\text{C} \text{ to } 85 ^{\circ}\text{C} \text{ (unless otherwise } 1.0 ^{\circ}\text{C} \text{ (unless otherwis$ noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
VI	Input voltage range, VINDCDC3		2.5		6	V
		DEFDCDC3 = GND	1000			
I _O	Maximum output current	VINDCDC3 = 3.6 V; 3.3V - 1% ≤ VDCDC3 ≤ 3.3V + 1%	525			mA
I _(SD)	Shutdown supply current in VINDCDC3	DCDC3_EN = GND		0.1	1	μΑ
r _{DS(on)}	P-channel MOSFET on-resistance	VINDCDC3 = V _(GS) = 3.6 V		310	698	mΩ
I _{lkg}	P-channel leakage current	VINDCDC3 = 6 V		0.1	2	μΑ
r _{DS(on)}	N-channel MOSFET on-resistance	VINDCDC3 = V _(GS) = 3.6 V		220	503	mΩ
I _{lkg}	N-channel leakage current	V _(DS) = 6 V		7	10	μΑ
	Forward current limit (P-channel and N-channel)	2.5 V < VINDCDC3 < 6 V	1.28	1.49	1.69	Α

Typical values are at $T_A = 25$ °C, unless otherwise noted.

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Electrical Characteristics: VDCDC3 Step-Down Converter (continued)

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, $T_A = -40$ °C to 85°C (unless otherwise noted)

	PARAMETER	₹	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
f _S	Oscillator frequency			1.95	2.25	2.55	MHz
	Fixed output voltage	VDCDC3 = 1.8 V	VINDCDC3 = 2.5 V to 6 V; 0 mA \leq I _O \leq 1 A	-2%		2%	
	FPWMDCDC3=0	VDCDC3 = 3.3 V	VINDCDC3 = 3.6 V to 6 V; 0 mA \leq I _O \leq 1 A	-1%		1%	
	Fixed output voltage	VDCDC3 = 1.8 V	VINDCDC3 = 2.5 V to 6 V; 0 mA \leq I _O \leq 1 A	-2%		2%	
	FPWMDCDC3=1	VDCDC3 = 3.3 V	VINDCDC3 = 3.6 V to 6 V; 0 mA \leq I _O \leq 1 A	-1%		1%	
	Adjustable output volta divider at DEFDCDC3		VINDCDC3 = VDCDC3 + 0.5 V (min 2.5 V) to 6 V; 0 mA \leq I _O \leq 800 mA	-2%		2%	
	Adjustable output volta divider at DEFDCDC3		VINDCDC3 = VDCDC3 + 0.5 V (min 2.5 V) to 6 V; 0 mA \leq I _O \leq 800 mA	-1%		1%	
	Line Regulation		VINDCDC3 = VDCDC3 + 0.3 V (min. 2.5 V) to 6 V; I_0 = 10 mA		0%		V
	Load Regulation		I _O = 10 mA to 1000 mA		0.25%		Α
t _{Start}	Start-up time		Time from active EN to start switching	145	175	200	μs
t _{Ramp}	V _{OUT} ramp-up time		Time to ramp from 5% to 95% of V _{OUT}	400	750	1000	μS
	Internal resistance from	m L3 to GND			1		ΜΩ
	VDCDC3 discharge re	esistance	DCDC3 discharge =1		300		Ω

6.11 I²C Timing Requirements for TPS65023B

 $VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 2.5 \ V \ to \ 5.5 \ V, \ VBACKUP = 3.0 \ V, \ T_A = -40 \ ^{\circ}C \ to \ 85 \ ^{\circ}C$

		MIN	MAX	UNIT
f_{MAX}	Clock frequency		400	kHz
t _{wH(HIGH)}	Clock high time	600		ns
$t_{WL(LOW)}$	Clock low time	1300		ns
t_R	DATA and CLK rise time		300	ns
t_{F}	DATA and CLK fall time		300	ns
t _{h(STA)}	Hold time (repeated) START condition (after this period the first clock pulse is generated)	600		ns
t _{su(DATA)}	Setup time for repeated START condition	600		ns
t _{h(DATA)}	Data input hold time	100		ns
t _{su(DATA)}	Data input setup time	100		ns
t _{su(STO)}	STOP condition setup time	600		ns
t _(BUF)	Bus free time	1300		ns



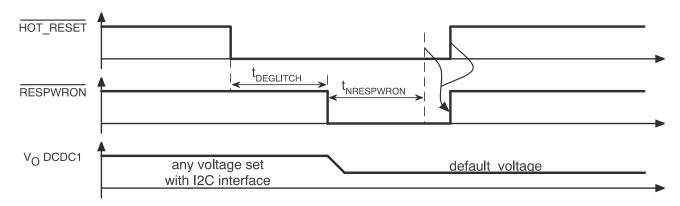


Figure 1. HOT_RESET Timing

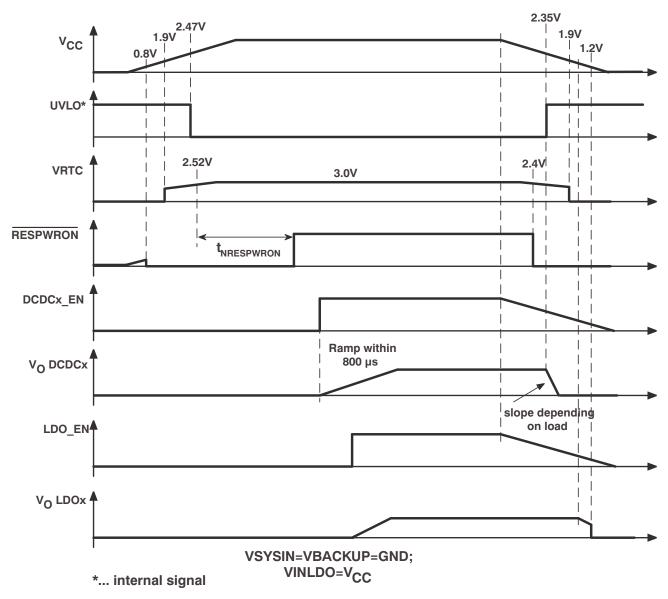


Figure 2. Power-Up and Power-Down Timing

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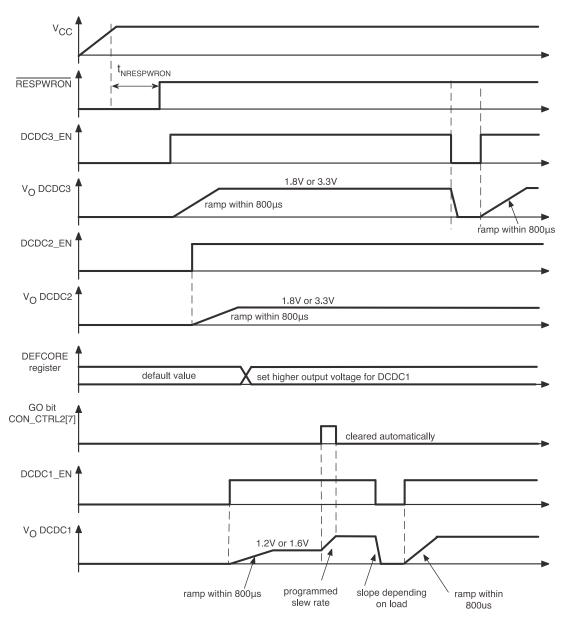


Figure 3. DVS Timing

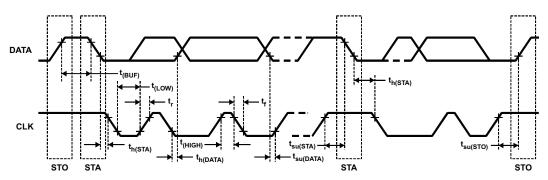


Figure 4. Serial I/F Timing Diagram



6.12 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
η	Efficiency	vs Output current	Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, Figure 10
	Output voltage	vs Output current at 85°C	Figure 11, Figure 12
	Line transient response		Figure 13, Figure 14, Figure 15
	Load transient response		Figure 16, Figure 17, Figure 18
	VDCDC2 PFM operation		Figure 19
	VDCDC2 low ripple PFM operation		Figure 20
	VDCDC2 PWM operation		Figure 21
	Startup VDCDC1, VDCDC2 and VDCDC3		Figure 22
	Startup LDO1 and LDO2		Figure 23
	Line transient response		Figure 24, Figure 25, Figure 26
	Load transient response		Figure 27, Figure 28, Figure 29

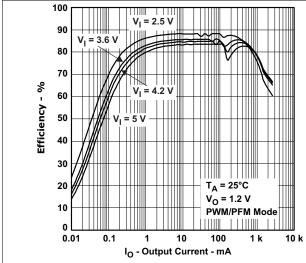
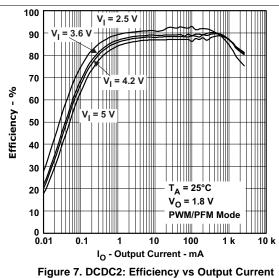


Figure 5. DCDC1: Efficiency vs Output Current



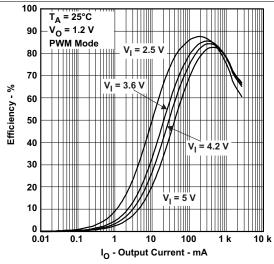


Figure 6. DCDC1: Efficiency vs Output Current

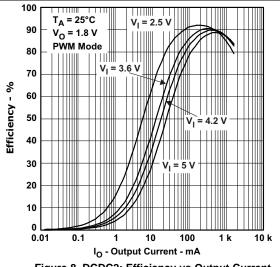
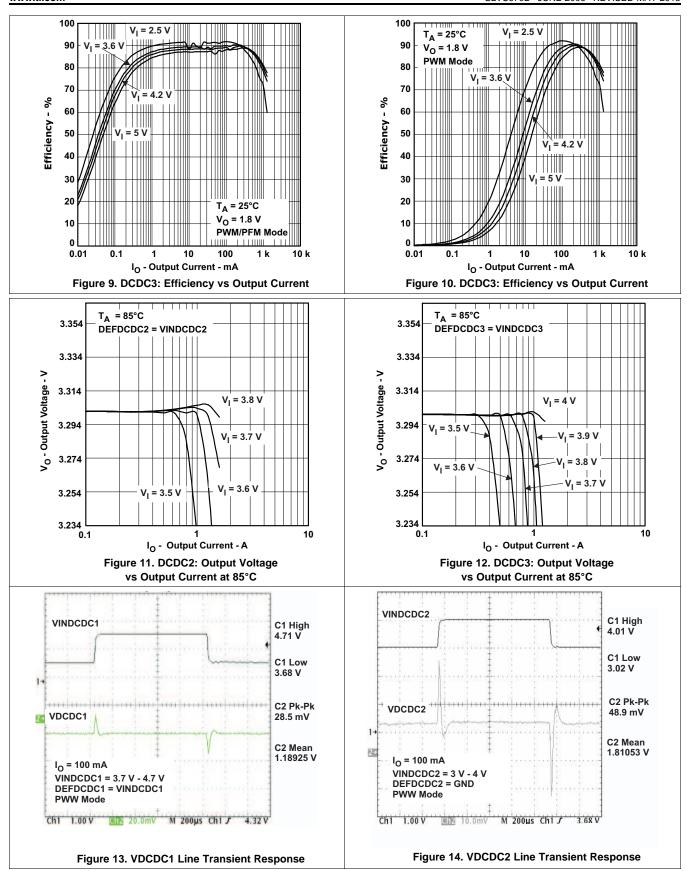
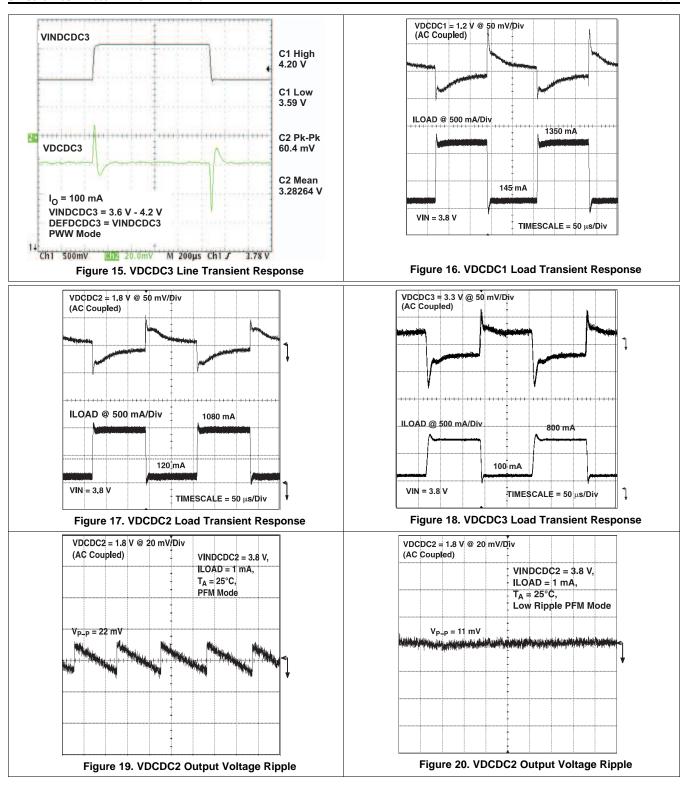


Figure 8. DCDC2: Efficiency vs Output Current

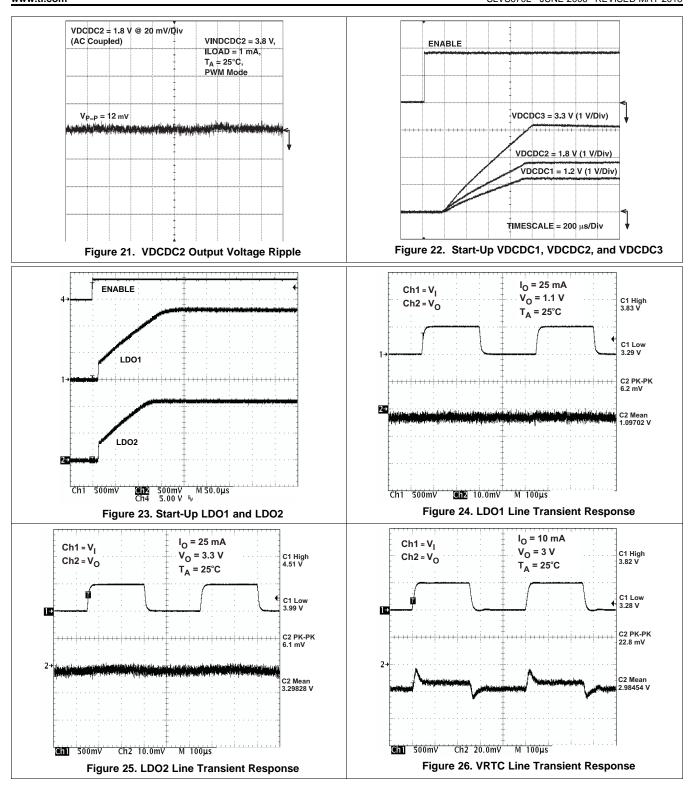




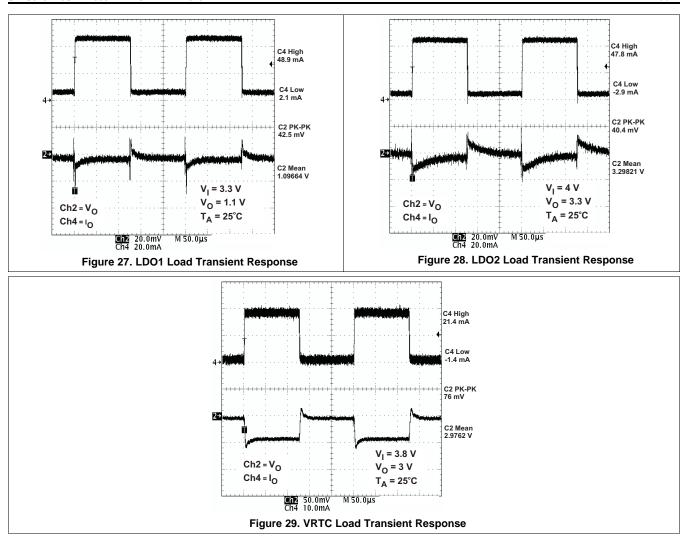














7 Detailed Description

7.1 Overview

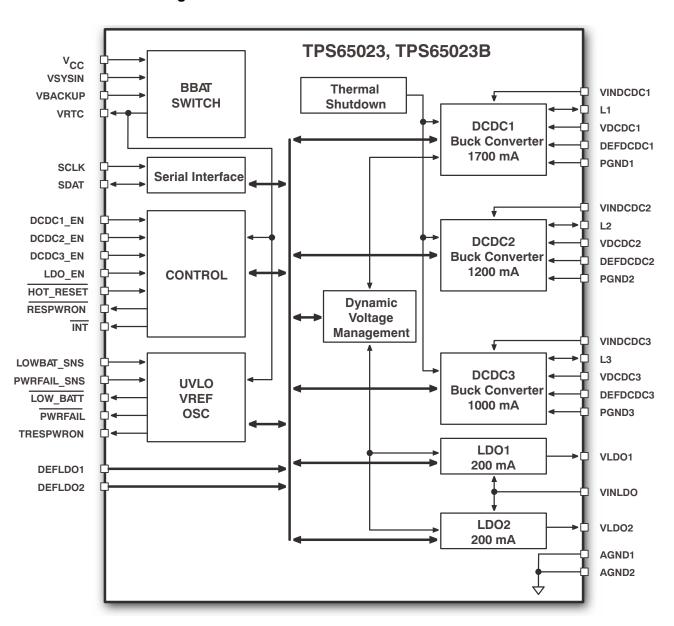
TPS65023x has 5 regulator channels, 3 DCDCs and 2 LDOs. DCDC3 has dynamic voltage scaling feature (DVS) that allows for power reduction to CORE supplies during idle operation or overvoltage during heavy-duty operation. With DVS and 2 more DCDCs plus 2 LDOs, the TPS65023x is ideal for CORE, Memory, IO, and peripheral power for the entire system of a wide range of suitable applications.

The device incorporates enables for the DCDCs and LDOs, I²C for device control, push button, and a reset interface that complete the system and allow the TPS65023x to be adapted for different kinds of processors or FPGAs.

For noise-sensitive circuits, the DCDCs can be synchronized out of phase from one another, reducing the peak noise at the switching frequency. Each converter can be forced to operate in PWM mode to ensure constant switching frequency across the entire load range. However, for low load efficiency performance the DCDCs automatically enter PSM mode which reduces the switching frequency when the load current is low, saving power at idle operation.



7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VRTC Output and Operation With or Without Backup Battery

The VRTC pin is an always-on output, intended to supply up to 30 mA to a permanently required rail (that is, for a real time clock). The TPS65023x asserts the RESPWRON signal if VRTC drops below 2.4 V. VRTC is selected from a priority scheme based on the VSYSIN and VBACKUP inputs.

When the voltage at the VSYSIN pin exceeds 2.65 V, VRTC connects to the VSYSIN input through a PMOS switch and all other paths to VRTC are disabled. The PMOS switch drops a maximum of 375 mV at 30 mA, which must be considered when using VRTC. VSYSIN can be connected to any voltage source with the appropriate input voltage, including VCC or, if set to 3.3-V output, DCDC2 or DCDC3. When VSYSIN falls below 2.65 V or shorts to ground, the PMOS switch connecting VRTC and VSYSIN opens and VRTC then connects to either VBACKUP or the output of a dedicated 3-V or 30-mA LDO.



NOTE

Texas Instruments recommends connecting VSYSIN to VCC or ground – VCC if a non-replaceable primary cell is connected to VBACKUP and ground if the VRTC output will float.

If the PMOS switch between VSYSIN and VRTC is open and VBACKUP exceeds 2.65 V, VRTC connects to VBACKUP through a PMOS switch. The PMOS switch drops a maximum of 375 mV at 30 mA, which must be considered if using VRTC. A typical application may connect VBACKUP to a primary Li button cell, but any battery that provides a voltage between 2.65 V and 6 V (that is, a single Li-lon cell or a single boosted NiMH battery) is acceptable, to supply the VRTC output.

NOTE

In systems with no backup battery, the VBACKUP pin must be connected to GND.

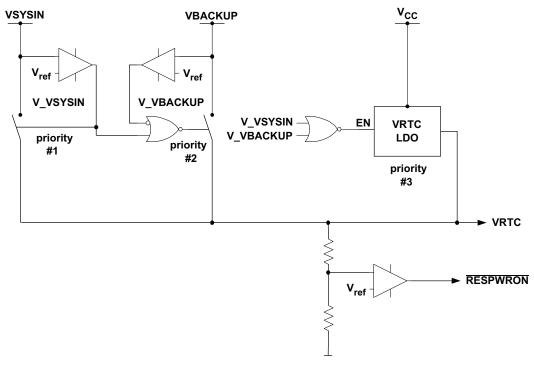
If the switches between VRTC and VSYSIN or VBACKUP are open, the dedicated 3-V or 30-mA LDO, driven from VCC, connects to VRTC. This LDO is disabled if the voltage at the VSYSIN input exceeds 2.65 V.

Inside TPS65023x there is a switch (Vmax switch) which selects the higher voltage between V_{CC} and VBACKUP. This is used as the supply voltage for some basic functions. The functions powered from the output of the Vmax switch are:

- INT output
- RESPWRON output
- HOT RESET input
- LOW_BATT output
- PWRFAIL output
- Enable pins for DC-DC converters, LDO1 and LDO2
- Undervoltage lockout comparator (UVLO)
- Reference system with low frequency timing oscillators
- LOW BATT and PWRFAIL comparators

The main 2.25-MHz oscillator, and the I²C interface are only powered from V_{CC}.





- A. V_VSYSIN, V_VBACKUP thresholds: falling = 2.55 V, rising = 2.65 V ±3%
- B. RESPWRON thresholds: falling = 2.4 V, rising = 2.52 V ±3%

Figure 30. RTC and nRESPWRON

7.3.2 Step-Down Converters, VDCDC1, VDCDC2, and VDCDC3

The TPS65023x incorporates three synchronous step-down converters operating typically at 2.25-MHz, fixed frequency pulse width modulation (PWM) at moderate to heavy-load currents. At light-load currents, the converters automatically enter the power save mode (PSM), and operate with pulse frequency modulation (PFM). The VDCDC1 converter is capable of delivering 1.5-A output current, the VDCDC2 converter is capable of delivering up to 1 A.

The converter output voltages can be programmed through the DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins. The pins can either be connected to GND, VCC, or to a resistor divider between the output voltage and GND. The VDCDC1 converter defaults to 1.2 V or 1.6 V depending on the DEFDCDC1 configuration pin. If DEFDCDC1 is tied to ground, the default is 1.2 V. If it is tied to VCC, the default is 1.6 V. When the DEFDCDC1 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC1 V. See Application Information for more details. The core voltage can be reprogrammed through the serial interface in the range of 0.8 V to 1.6 V with a programmable slew rate. The converter is forced into PWM operation whilst any programmed voltage change is underway, whether the voltage is being increased or decreased. The DEFCORE and DEFSLEW registers are used to program the output voltage and slew rate during voltage transitions.

The VDCDC2 converter defaults to 1.8 V or 3.3 V depending on the DEFDCDC2 configuration pin. If DEFDCDC2 is tied to ground, the default is 1.8 V. If it is tied to VCC, the default is 3.3 V. When the DEFDCDC2 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC2 V.

The VDCDC3 converter defaults to 1.8 V or 3.3 V depending on the DEFDCDC3 configuration pin. If DEFDCDC3 is tied to ground the default is 1.8 V. If it is tied to VCC, the default is 3.3 V. When the DEFDCDC3 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC3 V.

The step-down converter outputs (when enabled) are monitored by power-good (PG) comparators, the outputs of which are available through the serial interface. The outputs of the DC-DC converters can be optionally discharged through on-chip $300-\Omega$ resistors when the DC-DC converters are disabled.

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During PWM operation, the converters use a unique fast response voltage mode controller scheme with input voltage feedforward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on. The inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch if the current limit of the P-channel switch is exceeded. After the adaptive dead-time used to prevent shoot through current, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal, again turning off the N-channel rectifier and turning on the P-channel switch.

The three DC-DC converters operate synchronized to each other with the VDCDC1 converter as the master. A 180° phase shift between the VDCDC1 switch turn on and the VDCDC2 and a further 90° shift to the VDCDC3 switch turn on decreases the input RMS current and smaller input capacitors can be used. This is optimized for a typical application where the VDCDC1 converter regulates a Li-lon battery voltage of 3.7 V to 1.2 V, the VDCDC2 converter from 3.7 V to 1.8 V, and the VDCDC3 converter from 3.7 V to 3.3 V. The phase of the three converters can be changed using the CON_CTRL register.

7.3.3 Power Save Mode Operation

As the load current decreases, the converters enter the power save mode operation. During PSM, the converters operate in a burst mode (PFM mode) with a frequency between 750 kHz and 2.25 MHz, nominal for one burst cycle. However, the frequency between different burst cycles depends on the actual load current and is typically far less than the switching frequency with a minimum quiescent current to maintain high efficiency.

To optimize the converter efficiency at light load, the average current is monitored and if in PWM mode the inductor current remains below a certain threshold, then PSM is entered. The typical threshold to enter PSM is calculated as shown in Equation 1, Equation 2 and Equation 3.

$$I_{PFMDCDC1}$$
 enter = $\frac{VINDCDC1}{24 \Omega}$ (1)

$$I_{PFMDCDC2} \ enter = \frac{VINDCDC2}{26 \ \Omega} \tag{1}$$

$$I_{PFMDCDC3}$$
 enter = $\frac{VINDCDC3}{39 \Omega}$ (3)

During the PSM the output voltage is monitored with a comparator, and by maximum skip burst width. As the output voltage falls below the threshold, set to the nominal V_0 , the P-channel switch turns on and the converter effectively delivers a constant current defined in Equation 4, Equation 5 and Equation 6.

$$I_{PFMDCDC1}$$
 leave = $\frac{VINDCDC1}{18 \Omega}$ (4)

$$I_{PFMDCDC2}$$
 leave = $\frac{VINDCDC2}{20 \Omega}$ (5)

$$I_{PFMDCDC3}$$
 leave = $\frac{VINDCDC3}{29 \Omega}$ (6

If the load is below the delivered current then the output voltage rises until the same threshold is crossed in the other direction. All switching activity ceases, reducing the quiescent current to a minimum until the output voltage has again dropped below the threshold. The power save mode is exited, and the converter returns to PWM mode if either of the following conditions are met:

- 1. the output voltage drops 2% below the nominal V_{O} due to increasing load current
- 2. the PFM burst time exceeds 16 x 1/fs (7.11 μ s typical).

These control methods reduce the quiescent current to typically 14 μ A per converter, and the switching activity to a minimum, thus achieving the highest converter efficiency. Setting the comparator thresholds at the nominal output voltage at light-load current results in a low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor. Increasing capacitor values makes the output ripple tend to zero. The PSM is disabled through the I²C interface to force the individual converters to stay in fixed frequency PWM mode.



7.3.4 Low Ripple Mode

Setting bit 3 in register CON-CTRL to 1 enables the low ripple mode for all of the DC-DC converters if operated in PFM mode. For an output current less than approximately 10 mA, the output voltage ripple in PFM mode is reduced, depending on the actual load current. The lower the actual output current on the converter, the lower the output ripple voltage. For an output current above 10 mA, there is only minor difference in output voltage ripple between PFM mode and low ripple PFM mode. As this feature also increases switching frequency, it is used to keep the switching frequency above the audible range in PFM mode down to a low output current.

7.3.5 Soft-Start

Each of the three converters has an internal soft-start circuit that limits the inrush current during start-up. The soft-start is realized by using a low current to initially charge the internal compensation capacitor. The soft-start time is typically 750 μ s if the output voltage ramps from 5% to 95% of the final target value. If the output is already precharged to some voltage when the converter is enabled, then this time is reduced proportionally. There is a short delay of typically 170 μ s between the converter being enabled and switching activity actually starting. This allows the converter to bias itself properly, to recognize if the output is precharged, and if so to prevent discharging of the output while the internal soft-start ramp catches up with the output voltage.

7.3.6 100% Duty Cycle Low Dropout Operation

The TPS65023x converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage required to maintain DC regulation depends on the load current and output voltage. It is calculated in Equation 7.

$$Vin_{min} = Vout_{min} + Iout_{max} \times (r_{DS(on)} max + R_L)$$

where

- lout_{max} = maximum load current (Note: ripple current in the inductor is zero under these conditions)
- r_{DS(on)}max = maximum P-channel switch r_{DS(on)}
- R_I = DC resistance of the inductor
- Vout_{min} = nominal output voltage minus 2% tolerance limit

(7)

7.3.7 Active Discharge When Disabled

When the VDCDC1, VDCDC2, and VDCDC3 converters are disabled, due to an UVLO, DCDC_EN or OVERTEMP condition, it is possible to actively pull down the outputs. This feature is disabled per default and is individually enabled through the CON_CTRL2 register in the serial interface. When this feature is enabled, the VDCDC1, VDCDC2, and VDCDC3 outputs are discharged by a $300-\Omega$ (typical) load which is active as long as the converters are disabled.

7.3.8 Power-Good Monitoring

All three step-down converters and both the LDO1 and LDO2 linear regulators have power-good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value with 5% hysteresis. The outputs of these comparators are available in the PGOODZ register through the serial interface. An interrupt is generated when any voltage rail drops below the 10% threshold. The comparators are disabled when the converters are disabled and the relevant PGOODZ register bits indicate that power is good.



7.3.9 Low-Dropout Voltage Regulators

The low-dropout voltage regulators are designed to operate well with low-value ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 300 mV at rated output current. Each LDO supports a current limit feature. Both LDOs are enabled by the LDO_EN pin, both LDOs can be disabled or programmed through the serial interface using the REG_CTRL and LDO_CTRL registers. The LDOs also have reverse conduction prevention. This allows the possibility to connect external regulators in parallel in systems with a backup battery. The TPS65023x step-down and LDO voltage regulators automatically power down when the $V_{\rm CC}$ voltage drops below the UVLO threshold or when the junction temperature rises above 160°C.

7.3.10 Undervoltage Lockout

The undervoltage lockout circuit for the five regulators on the TPS65023x prevents the device from malfunctioning at low-input voltages and from excessive discharge of the battery. It disables the converters and LDOs. The UVLO circuit monitors the VCC pin, the threshold is set internally to 2.35 V with 5% (120 mV) hysteresis. When any of the DC-DC converters are running, there is an input current at the VCC pin, which is up to 3 mA when all three converters are running in PWM mode. Consider this current if an external RC filter is used at the VCC pin to remove switching noise from the TPS65023x internal analog circuitry supply.

7.3.11 Power-Up Sequencing

The TPS65023x power-up sequencing is designed to be entirely flexible and customer driven. This is achieved by providing separate enable pins for each switch-mode converter, and a common enable signal for the LDOs. The relevant control pins are described in Table 2.

PIN NAME	I/O	FUNCTION
DEFDCDC3	ı	Defines the default voltage of the VDCDC3 switching converter. DEFDCDC3 = 0 defaults VDCDC3 to 1.8 V, DEFDCDC3 = VCC defaults VDCDC3 to 3.3 V.
DEFDCDC2	ı	Defines the default voltage of the VDCDC2 switching converter. DEFDCDC2 = 0 defaults VDCDC2 to 1.8 V, DEFDCDC2 = VCC defaults VDCDC2 to 3.3 V.
DEFDCDC1	ı	Defines the default voltage of the VDCDC1 switching converter. DEFDCDC1 = 0 defaults VDCDC1 to 1.2 V, DEFDCDC1 = VCC defaults VDCDC1 to 1.6 V.
DCDC3_EN	I	Set DCDC3_EN = 0 to disable and DCDC3_EN = 1 to enable the VDCDC3 converter
DCDC2_EN	I	Set DCDC2_EN = 0 to disable and DCDC2_EN = 1 to enable the VDCDC2 converter
DCDC1_EN	I	Set DCDC1_EN = 0 to disable and DCDC1_EN = 1 to enable the VDCDC1 converter
HOT_RESET	I	The HOT_RESET pin generates a reset (RESPWRON) for the processor.HOT_RESET does not alter any TPS65023x settings except the output voltage of VDCDC1. Activating HOT_RESET sets the voltage of VDCDC1 to its default value defined with the DEFDCDC1 pin. HOT_RESET is internally de-bounced by the TPS65023x.
RESPWRON	0	RESPWRON is held low when power is initially applied to the TPS65023x. The VRTC voltage is monitored: RESWPRON is low when VRTC < 2.4 V and remains low for a time defined by the external capacitor at the TRESPWRON pin. RESPWRON can also be forced low by activation of the HOT_RESET pin.
TRESPWRON	I	Connect a capacitor here to define the RESET time at the RESPWRON pin (1 nF typically gives 100 ms).

Table 2. Control Pins and Status Outputs for DC-DC Converters

7.4 Device Functional Modes

The TPS6502x devices are either in the ON or the OFF mode. The OFF mode is entered when the voltage on VCC is below the UVLO threshold, 2.35 V (typically). Once the voltage at VCC has increased above UVLO, the device enters ON mode. In the ON mode, the DCDCs and LDOs are available for use.



7.5 Programming

7.5.1 System Reset + Control Signals

The RESPWRON signal can be used as a global reset for the application. It is an open-drain output. The RESPWRON signal is generated according to the power-good comparator of VRTC, and remains low for t_{nrespwron} seconds after VRTC has risen above 2.52 V (falling threshold is 2.4 V, 5% hysteresis). t_{nrespwron} is set by an external capacitor at the TRESPWRON pin. 1 nF gives typically 100 ms. RESPWRON is also triggered by the HOT RESET input. This input is internally debounced, with a filter time of typically 30 ms.

The PWRFAIL and LOW BAT signals are generated by two voltage detectors using the PWRFAIL SNS and LOWBAT_SNS input signals. Each input signal is compared to a 1-V threshold (falling edge) with 5% (50 mV) hysteresis.

The DCDC1 converter is reset to its default output voltage defined by the DEFDCDC1 input, when HOT_RESET is asserted. Other I²C registers are not affected. Generally, the DCDC1 converter is set to its default voltage with one of these conditions: HOT RESET active, VRTC lower than its threshold voltage, undervoltage lockout (UVLO) condition, or RESPWRON active.

7.5.1.1 DEFLDO1 and DEFLDO2

These two pins are used to set the default output voltage of the two 200-mA LDOs. The digital value applied to the pins is latched during power up and determines the initial output voltage according to Table 3. The voltage of both LDOs can be changed during operation with the I²C interface as described in the interface description.

DEFLDO2 DEFLDO1 VLD01 VLD₀₂ 0 0 1.3 V 3.3 V 0 1 2.8 V 3.3 V 1 0 1.3 V 1.8 V 1 1.8 V 3.3 V 1

Table 3. LDO1 and LDO2 Default Voltage Options

7.5.1.2 Interrupt Management and the INT Pin

The INT pin combines the outputs of the PGOOD comparators from each DC-DC converter and the LDOs. The INT pin is used as a POWER_OK pin to indicate when all enabled supplies are in regulation. The INT pin remains active (low state) during power up as long as all enabled power rails are below their regulation limit. Once the last enabled power rail is within regulation, the INT pin transitions to a high state.

During operation, if one of the enabled supplies goes out of regulation, INT transitions to a low state, and the corresponding bit in the PGOODZ register goes high. If the supply goes back to its regulation limits, INT transitions back to a high state.

While INT is in an active-low state, reading the PGOODZ register through the I²C bus forces INT into a high-Z state. Because this pin requires an external pullup resistor, the INT pin transitions to a logic high state even though the supply in question is still out of regulation. The corresponding bit in the PGOODZ register still indicates that the power rail is out of regulation.

Interrupts can be masked using the MASK register; default operation is not to mask any DCDC or LDO interrupts because this provides the POWER OK function. If none of the DCDC converters or LDos are enabled, /INT defaults to a low state independently of the settings of the MASK register.

7.5.2 Serial Interface

The serial interface is compatible with the standard and fast mode I²C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as V_{CC} remains above 2 V. The TPS65023x has a 7-bit address: 1001000, other addresses are available upon contact with the factory. Attempting to read data from the register addresses not listed in this section results in FFh being read out.



For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS65023x device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS65023x device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge—related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS65023x device must leave the data line high to enable the master to generate the stop condition. See \(\begin{align*} PC \) Timing Requirements for TPS65023B for more information.

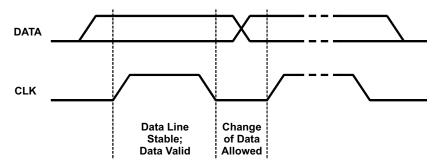


Figure 31. Bit Transfer on the Serial Interface

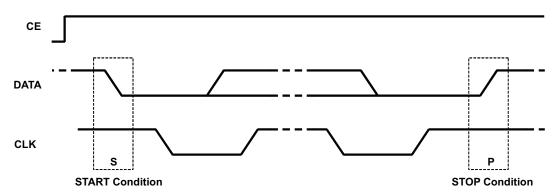
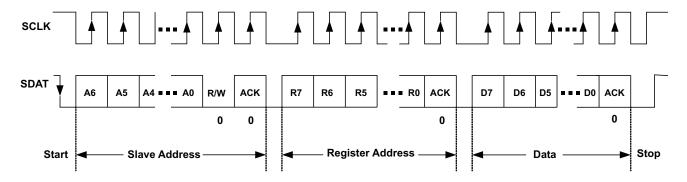


Figure 32. START and STOP Conditions



Note: SLAVE = TPS65023

Figure 33. Serial I/F WRITE to TPS65023x Device



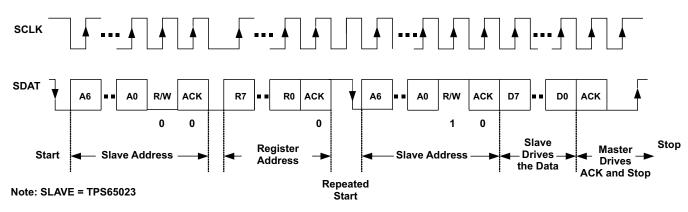
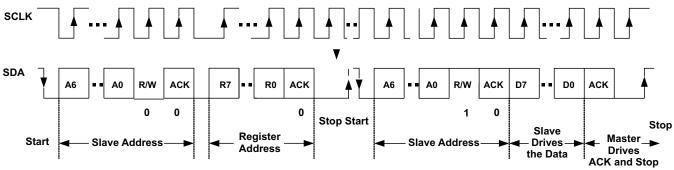


Figure 34. Serial I/F READ from TPS65023x: Protocol A



Note: SLAVE = TPS65023

Figure 35. Serial I/F READ from TPS65023x: Protocol B



7.6 Register Maps

7.6.1 VERSION Register Address: 00h (Read Only)

Table 4. VERSION Register

VERSION	В7	В6	B5	B4	В3	B2	B1	В0
Bit name and function	0	0	1	0	0	0	1	1
Read and write	R	R	R	R	R	R	R	R

7.6.2 PGOODZ Register Address: 01h (Read Only)

Table 5. PGOODZ Register

PGOODZ	B7	В6	B5	B4	В3	B2	B1	В0
Bit name and function	PWRFAILZ	LOWBATTZ	PGOODZ VDCDC1	PGOODZ VDCDC2	PGOODZ VDCDC3	PGOODZ LDO2	PGOODZ LDO1	_
Set by signal	PWRFAIL	LOWBATT	PGOODZ VDCDC1	PGOODZ VDCDC2	PGOODZ VDCDC3	PGOODZ LDO2	PGOODZ LDO1	_
Default value loaded	PWRFAILZ	LOWBATTZ	PGOOD VDCDC1	PGOOD VDCDC2	PGOOD VDCDC3	PGOOD LDO2	PGOOD LDO1	_
Read and write	R	R	R	R	R	R	R	R

Bit 7 PWRFAILZ:

- 0 = indicates that the PWRFAIL_SNS input voltage is above the 1-V threshold.
- 1 = indicates that the PWRFAIL_SNS input voltage is below the 1-V threshold.

Bit 6 LOWBATTZ:

- 0 = indicates that the LOWBATT_SNS input voltage is above the 1-V threshold.
- 1 = indicates that the LOWBATT_SNS input voltage is below the 1-V threshold.

Bit 5 PGOODZ VDCDC1:

- 0 = indicates that the VDCDC1 converter output voltage is within its nominal range. This bit is zero if the VDCDC1 converter is disabled.
- 1 = indicates that the VDCDC1 converter output voltage is below its target regulation voltage

Bit 4 PGOODZ VDCDC2:

- 0 = indicates that the VDCDC2 converter output voltage is within its nominal range. This bit is zero if the VDCDC2 converter is disabled.
- 1 = indicates that the VDCDC2 converter output voltage is below its target regulation voltage

Bit 3 PGOODZ VDCDC3: .

- 0 = indicates that the VDCDC3 converter output voltage is within its nominal range. This bit is zero if the VDCDC3 converter is disabled and during a DVM controlled output voltage transition
- 1 = indicates that the VDCDC3 converter output voltage is below its target regulation voltage

Bit 2 PGOODZ LDO2:

- 0 = indicates that the LDO2 output voltage is within its nominal range. This bit is zero if LDO2 is disabled.
- 1 = indicates that LDO2 output voltage is below its target regulation voltage

Bit 1 PGOODZ LDO1

0 = indicates that the LDO1 output voltage is within its nominal range. This bit is zero if LDO1 is disabled.



1 = indicates that the LDO1 output voltage is below its target regulation voltage

7.6.3 MASK Register Address: 02h (Read and Write), Default Value: C0h

Table 6. MASK Register

MASK	В7	В6	B5	B4	В3	B2	B1	В0
Bit name and function	MASK PWRFAILZ	MASK LOWBATTZ	MASK VDCDC1	MASK VDCDC2	MASK VDCDC3	MASK LDO2	MASK LDO1	_
Default	1	1	0	0	0	0	0	0
Default value loaded	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	_
Read and write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-

The MASK register can be used to mask particular fault conditions from appearing at the $\overline{\text{INT}}$ pin. MASK<n> = 1 masks PGOODZ<n>.

7.6.4 REG_CTRL Register Address: 03h (Read and Write), Default Value: FFh

The REG_CTRL register is used to disable or enable the power supplies through the serial interface. The contents of the register are logically AND'ed with the enable pins to determine the state of the supplies. A UVLO condition resets the REG_CTRL to 0xFF, so the state of the supplies defaults to the state of the enable pin. The REG_CTRL bits are automatically reset to default when the corresponding enable pin is low.

Table 7. REG_CTRL Register

REG_CTRL	В7	В6	B5	B4	В3	B2	B1	В0
Bit name and function	-	_	VDCDC1 ENABLE	VDCDC2 ENABLE	VDCDC3 ENABLE	LDO2 ENABLE	LDO1 ENABLE	_
Default	1	1	1	1	1	1	1	1
Set by signal	-	-	DCDC1_ENZ	DCDC2_ENZ	DCDC3_ENZ	LDO_ENZ	LDO_ENZ	_
Default value loaded	_	_	UVLO	UVLO	UVLO	UVLO	UVLO	_
Read and write	_	-	R/W	R/W	R/W	R/W	R/W	-

Bit 5 VDCDC1 ENABLE

DCDC1 Enable. This bit is logically AND'ed with the state of the DCDC1_EN pin to turn on the DCDC1 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the pin DCDC1_EN is pulled to GND, allowing DCDC1 to turn on when DCDC1_EN returns high.

Bit 4 VDCDC2 ENABLE

DCDC2 Enable. This bit is logically AND'ed with the state of the DCDC2_EN pin to turn on the DCDC2 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the pin DCDC2_EN is pulled to GND, allowing DCDC2 to turn on when DCDC2 EN returns high.

Bit 3 VDCDC3 ENABLE

DCDC3 Enable. This bit is logically AND'ed with the state of the DCDC3_EN pin to turn on the DCDC3 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the pin DCDC3_EN is pulled to GND, allowing DCDC3 to turn on when DCDC3_EN returns high.

Bit 2 LDO2 ENABLE

LDO2 Enable. This bit is logically AND'ed with the state of the LDO2_EN pin to turn on LDO2. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the pin LDO_EN is pulled to GND, allowing LDO2 to turn on when LDO_EN returns high.



Bit 1 LDO1 ENABLE

LDO1 Enable. This bit is logically AND'ed with the state of the LDO1_EN pin to turn on LDO1. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 through the serial interface. The bit is reset to 1 when the pin LDO_EN is pulled to GND, allowing LDO1 to turn on when LDO_EN returns high.

7.6.5 CON_CTRL Register Address: 04h (Read and Write), Default Value: B1h

Table 8. CON_CTRL Register

CON_CTRL	B7	В6	B5	B4	В3	B2	B1	В0
Bit name and function	DCDC2 PHASE1	DCDC2 PHASE0	DCDC3 PHASE1	DCDC3 PHASE0	LOW RIPPLE	FPWM DCDC2	FPWM DCDC1	FPWM DCDC3
Default	1	0	1	1	0	0	0	0
Default value loaded	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO
Read and write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The CON_CTRL register is used to force any or all of the converters into forced PWM operation, when low output voltage ripple is vital. It is also used to control the phase shift between the three converters to minimize the input rms current, hence reduce the required input blocking capacitance. The DCDC1 converter is taken as the reference and consequently has a fixed zero phase shift.

Table 9. DCDC2 and DCDC3 Phase Delay

CON_CTRL<7:6>	DCDC2 CONVERTER DELAYED BY	CON_CTRL<5:4>	DCDC3 CONVERTER DELAYED BY
00	zero	00	zero
01	1/4 cycle	01	1/4 cycle
10	1/2 cycle	10	1/2 cycle
11	3/4 cycle	11	3/4 cycle

Bit 3 LOW RIPPLE:

- 0 = PFM mode operation optimized for high efficiency for all converters
- 1 = PFM mode operation optimized for low output voltage ripple for all converters

Bit 2 FPWM DCDC2:

- 0 = DCDC2 converter operates in PWM / PFM mode
- 1 = DCDC2 converter is forced into fixed frequency PWM mode

Bit 1 FPWM DCDC1:

- 0 = DCDC1 converter operates in PWM / PFM mode
- 1 = DCDC1 converter is forced into fixed frequency PWM mode

Bit 0 FPWM DCDC3:

- 0 = DCDC3 converter operates in PWM / PFM mode
- 1 = DCDC3 converter is forced into fixed frequency PWM mode

7.6.6 CON_CTRL2 Register Address: 05h (Read and Write), Default Value: 40h

Table 10. CON CTRL2 Register

CON_CTRL2	B7	В6	B5	B4	В3	B2	B1	В0
Bit name and function	GO	Core adj allowed	-	_	_	DCDC2 discharge	DCDC1 discharge	DCDC3 discharge
Default	0	1	0	0	0	0	0	0

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Table 10. CON_CTRL2 Register (continued)

CON_CTRL2	В7	В6	B5	B4	В3	B2	B1	В0
Default value loaded	UVLO + DONE	RESET(1)	-	_	_	UVLO	UVLO	UVLO
Read and write	R/W	R/W	_	_	_	R/W	R/W	R/W

The CON CTRL2 register can be used to take control the inductive converters.

RESET(1): CON_CTRL2[6] is reset to its default value by one of these events:

- undervoltage lockout (UVLO)
- HOT_RESET pulled low
- RESPWRON active
- VRTC below threshold

Bit 7 GO:

- 0 = no change in the output voltage for the DCDC1 converter
- 1 = the output voltage of the DCDC1 converter is changed to the value defined in DEFCORE with the slew rate defined in DEFSLEW. This bit is automatically cleared when the DVM transition is complete. The transition is considered complete in this case when the desired output voltage code has been reached, not when the VDCDC1 output voltage is actually in regulation at the desired voltage.

Bit 6 CORE ADJ Allowed:

- 0 = the output voltage is set with the I^2C register
- 1 = DEFDCDC1 is either connected to GND or VCC or an external voltage divider. When connected to GND or VCC, VDCDC1 defaults to 1.2 V or 1.6 V respectively at start-up
- Bit 2– 0 0 = the output capacitor of the associated converter is not actively discharged when the converter is disabled
 - 1 = the output capacitor of the associated converter is actively discharged when the converter is disabled. This decreases the fall time of the output voltage at light load

7.6.7 DEFCORE Register Address: 06h (Read and Write), Default Value: 14h/1Eh

Table 11. DEFCORE Register

DEFCORE	B7	B6	B5	B4	В3	B2	B1	В0
Bit name and function	_	_	_	CORE4	CORE3	CORE2	CORE1	CORE0
Default	0	0	0	1	DEFDCDC1	DEFDCDC1	DEFDCDC1	DEFDCDC1
Default value loaded	_	-	_	RESET(1)	RESET(1)	RESET(1)	RESET(1)	RESET(1)
Read and write	-	-	-	R/W	R/W	R/W	R/W	R/W

RESET(1): DEFCORE is reset to its default value by one of these events:

- undervoltage lockout (UVLO)
- HOT_RESET pulled low
- RESPWRON active
- VRTC below threshold

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Table 12. DCDC3 DVS Voltages

CORE4	CORE3	CORE2	CORE1	CORE0	VDCDC1	CORE4	CORE3	CORE2	CORE1	CORE0	VDCDC1
CUKE4				COREU	= = =	CORE4	CORES	COREZ			
0	0	0	0	0	0.8 V	1	0	0	0	0	1.2 V
0	0	0	0	1	0.825 V	1	0	0	0	1	1.225 V
0	0	0	1	0	0.85 V	1	0	0	1	0	1.25 V
0	0	0	1	1	0.875 V	1	0	0	1	1	1.275 V
0	0	1	0	0	0.9 V	1	0	1	0	0	1.3 V
0	0	1	0	1	0.925 V	1	0	1	0	1	1.325 V
0	0	1	1	0	0.95 V	1	0	1	1	0	1.35 V
0	0	1	1	1	0.975 V	1	0	1	1	1	1.375 V
0	1	0	0	0	1 V	1	1	0	0	0	1.4 V
0	1	0	0	1	1.025 V	1	1	0	0	1	1.425 V
0	1	0	1	0	1.05 V	1	1	0	1	0	1.45 V
0	1	0	1	1	1.075 V	1	1	0	1	1	1.475 V
0	1	1	0	0	1.1 V	1	1	1	0	0	1.5 V
0	1	1	0	1	1.125 V	1	1	1	0	1	1.525 V
0	1	1	1	0	1.15 V	1	1	1	1	0	1.55 V
0	1	1	1	1	1.175 V	1	1	1	1	1	1.6 V

7.6.8 DEFSLEW Register Address: 07h (Read and Write), Default Value: 06h

Table 13. DEFSLEW Register

DEFSLEW	В7	В6	B5	B4	В3	B2	B1	В0
Bit name and function	_	-	_	_	_	SLEW2	SLEW1	SLEW0
Default	_	_	_	_	_	1	1	0
Default value loaded	-	-	_	_	-	UVLO	UVLO	UVLO
Read and write	_	_	_	_	_	R/W	R/W	R/W

Table 14. DCDC3 DVS Slew Rate

SLEW2	SLEW1	SLEW0	VDCDC1 SLEW RATE
0	0	0	0.225 mV/μs
0	0	1	0.45 mV/μs
0	1	0	0.9 mV/μs
0	1	1	1.8 mV/μs
1	0	0	3.6 mV/μs
1	0	1	7.2 mV/μs
1	1	0	14.4 mV/μs
1	1	1	Immediate

7.6.9 LDO_CTRL Register Address: 08h (Read and Write), Default Value: Set with DEFLDO1 and DEFLDO2

Table 15. LDO_CTRL Register

					_				
LDO_CTRL	B7	В6	B5	B4	В3	B2	B1	В0	
Bit name and function	RSVD	LDO2_2	LDO2_1	LDO2_0	RSVD	LDO1_2	LDO1_1	LDO1_0	
Default	-	DEFLDOx	DEFLDOx	DEFLDOx	-	DEFLDOx	DEFLDOx	DEFLDOx	
Default value loaded	_	UVLO	UVLO	UVLO	-	UVLO	UVLO	UVLO	
Read and write	-	R/W	R/W	R/W	-	R/W	R/W	R/W	

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The LDO_CTRL registers are used to set the output voltage of LDO1 and LDO2. LDO_CTRL[7] and LDO_CTRL[3] are reserved and must always be written to **0**.

The default voltage is set with DEFLDO1 and DEFLDO2 pins as described in Table 16.

Table 16. LDO2 and LDO3 I2C Voltage Options

LDO2_2	LDO2_1	LDO2_0	LDO2 OUTPUT VOLTAGE	LDO1_2	LDO1_1	LDO1_0	LDO1 OUTPUT VOLTAGE
0	0	0	1.05 V	0	0	0	1 V
0	0	1	1.2 V	0	0	1	1.1 V
0	1	0	1.3 V	0	1	0	1.3 V
0	1	1	1.8 V	0	1	1	1.8 V
1	0	0	2.5 V	1	0	0	2.2 V
1	0	1	2.8 V	1	0	1	2.6 V
1	1	0	3.0 V	1	1	0	2.8 V
1	1	1	3.3 V	1	1	1	3.15 V

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Voltage Connection

The low power section of the control circuit for the step-down converters DCDC1, DCDC2, and DCDC3 is supplied by the VCC pin while the circuitry with high power such as the power stage is powered from the VINDCDC1, VINDCDC2, and VINDCDC3 pins. For proper operation of the step-down converters, VINDCDC1, VINDCDC2, VNDCDC3, and VCC must be tied to the same voltage rail. Step-down converters that are planned to be not used, still need to be powered from their input pin on the same rails than the other step-down converters and VCC.

LDO1 and LDO2 share a supply voltage pin which can be powered from the V_{CC} rails or from a voltage lower than V_{CC} , for example, the output of one of the step-down converters as long as it is operated within the input voltage range of the LDOs. If both LDOs are not used, the VINLDO pin can be tied to GND.

8.1.2 Unused Regulators

In case a step-down converter is not used, its input supply voltage pin VINDCDCx still needs to be connected to the V_{CC} rail along with supply input of the other step-down converters. TI recommends closing the control loop such that an inductor and output capacitor is added in the same way as it would be when operated normally. If one of the LDOs is not used, its output capacitor must be added as well. If both LDOs are not used, the input supply pin as well as the output pins of the LDOs (VINLDO, VLDO1, VLDO2) must be tied to GND.

8.1.3 Reset Condition of DCDC1

If DEFDCDC1 is connected to ground and DCDC1_EN is pulled high after VINDCDC1 is applied, the output voltage of DCDC1 defaults to 1.225 V instead of 1.2 V (high by 2%). Figure 36 illustrates the problem.

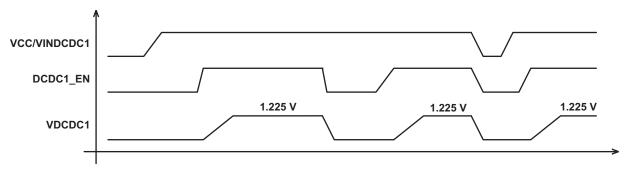


Figure 36. Default DCDC1

Application Information (continued)

One workaround is to tie DCDC1_EN to VINDCDC1 (Figure 37).

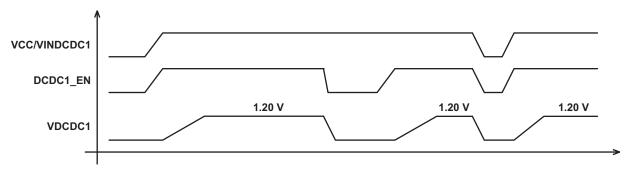


Figure 37. Workaround 1

Another workaround is to write the correct voltage to the DEF_CORE register through I²C. This can be done before or after the converter is enabled. If written before the enable, the only bit changed is DEF_CORE[0]. The voltage is 1.2 V, however, when the enable is pulled high (Figure 38).

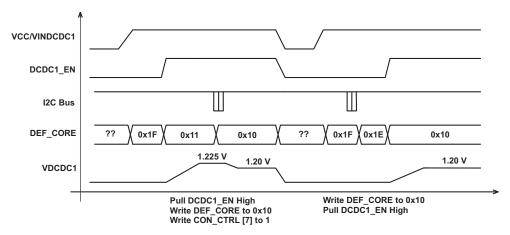


Figure 38. Workaround 2

A third workaround is to generate a HOT_RESET after enabling DCDC1 (Figure 39)

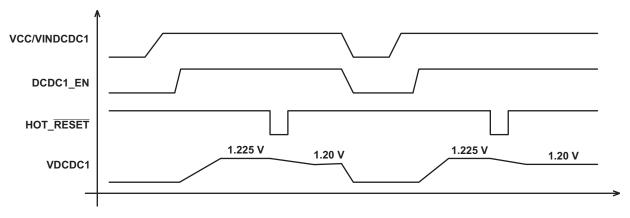


Figure 39. Workaround 3



Application Information (continued)

Table 17. Changes of TPS65023B vs TPS65023

ITEM	DESCRIPTION	Reference	TPS65023	TPS65023B
V _{IH}	High level input voltage for the SDAT pin	Electrical	Minimum 1.3 V	Minimum 1.69 V; Vcc = 2.5 V to 5.25 V Minimum 1.55 V; Vcc = 2.5 V to 4.5 V
V _{IH}	High level input voltage for the SCLK pin	Characteristics	Minimum 1.3 V	Minimum 1.4 V; Vcc = 2.5 V to 5.25 V
V _{IL}	Low level input voltage for SCLK and SDAT pin		Maximum 0.4 V	Maximum 0.35 V
t _{h(DATA)}	Data input hold time I ² C Timing		Minimum 300 ns	Minimum 100 ns
t _{su(DATA)}	Data input setup time	Requirements for TPS65023B	Minimum 300 ns	Minimum 100 ns

8.2 Typical Application

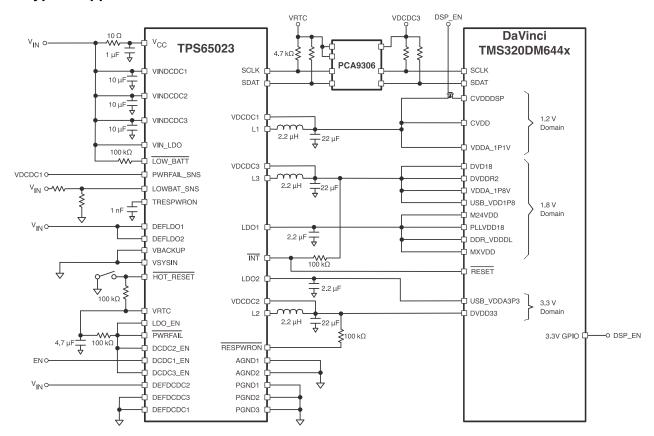


Figure 40. Typical Configuration for the Texas Instruments TMS320DM644x DaVinci™ Processors

8.2.1 Design Requirements

The TPS6502x devices have only a few design requirements. Use the following parameters for the design examples:

- 1- μ F bypass capacitor on VCC, located as close as possible to the VCC pin to ground
- VCC and VINDCDCx must be connected to the same voltage supply with minimal voltage difference.
- Input capacitors must be present on the VINDCDCx and VIN_LDO supplies if used
- Output inductor and capacitors must be used on the outputs of the DC-DC converters if used
- Output capacitors must be used on the outputs of the LDOs if used

(9)



Typical Application (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection for the DC-DC Converters

Each of the converters in the TPS65023x typically use a 2.2-μH output inductor. Larger or smaller inductor values are used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance must be selected for highest efficiency.

For a fast transient response, a 2.2-μH inductor in combination with a 22-μF output capacitor is recommended.

Equation 8 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current as calculated with Equation 8. This is needed because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_{L} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f}$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_{L}}{2}$$
(8)

where

- f = Switching Frequency (2.25 MHz typical)
- L = Inductor Value
- ΔI_1 = Peak-to-Peak inductor ripple current

The highest inductor current occurs at maximum Vin.

Open-core inductors have a soft saturation characteristic, and they can usually handle higher inductor currents versus a comparable shielded inductor.

A conservative approach is to select the inductor current rating just for the maximum switch current of the TPS65023x (2 A for the VDCDC1 and VDCDC2 converters, and 1.5 A for the VDCDC3 converter). The core material from inductor to inductor differs and has an impact on the efficiency especially at high switching frequencies.

See Table 18 and the typical applications for possible inductors.

Table 18. Tested Inductors

DEVICE	INDUCTOR VALUE	TYPE	COMPONENT SUPPLIER
All converters	2.2 μΗ	LPS4012-222LMB	Coilcraft
All converters	2.2 μΗ	VLCF4020T-2R2N1R7	TDK
For DCDC2 or DCDC3	2.2 uH	LQH32PN2R2NN0	Murata
For DCDC1	1.5 uH	LQH32PN1R5NN0	Murata
All converters	2.2 uH	PST25201B-2R2MS	Cyntec

8.2.2.2 Output Capacitor Selection

The advanced fast response voltage mode control scheme of the inductive converters implemented in the TPS65023x allow the use of small ceramic capacitors with a typical value of 10 μF for each converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. See Table 19 for recommended components.



If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. Just for completeness, the RMS ripple current is calculated in Equation 10.

$$I_{RMSCout} = V_{out} \quad x \quad \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}}$$
(10)

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{\text{out}} = V_{\text{out}} \times \frac{1 - \frac{V_{\text{out}}}{V_{\text{in}}}}{L \times f} \times \left(\frac{1}{8 \times C_{\text{out}} \times f} + \text{ESR} \right)$$

where

The highest output voltage ripple occurs at the highest input voltage Vin

At light load currents, the converters operate in PSM and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

8.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Each DC-DC converter requires a 10- μ F ceramic input capacitor on its input pin VINDCDCx. The input capacitor is increased without any limit for better input voltage filtering. The VCC pin is separated from the input for the DC-DC converters. A filter resistor of up to 10R and a 1- μ F capacitor is used for decoupling the VCC pin from switching noise. Note that the filter resistor may affect the UVLO threshold since up to 3 mA can flow through this resistor into the VCC pin when all converters are running in PWM mode.

CAPACITOR VALUE CASE SIZE COMPONENT SUPPLIER COMMENTS 22 µF 1206 TDK C3216X5R0J226M Ceramic 22 μF 1206 Taiyo Yuden JMK316BJ226ML Ceramic 22 μF 0805 TDK C2012X5R0J226MT Ceramic 22 μF 0805 Taiyo Yuden JMK212BJ226MG Ceramic 10 μF 0805 Taiyo Yuden JMK212BJ106M Ceramic 10 μF 0805 TDK C2012X5R0J106M Ceramic

Table 19. Possible Capacitors

8.2.2.4 Output Voltage Selection

The DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins are used to set the output voltage for each step-down converter. See Table 20 for the default voltages if the pins are pulled to GND or to VCC. If a different voltage is needed, an external resistor divider can be added to the DEFDCDCx pin as shown in Figure 41.

The output voltage of VDCDC1 is set with the I²C interface. If the voltage is changed from the default, using the DEFCORE register, the output voltage only depends on the register value. Any resistor divider at DEFDCDC1 does not change the voltage set with the register.

Table 20. DCDC1, DCDC2, and DCDC3 Default Voltage Levels

PIN	LEVEL	DEFAULT OUTPUT VOLTAGE
DEEDCDC4	VCC	1.6 V
DEFDCDC1	GND	1.2 V
DEEDODGO	VCC	3.3 V
DEFDCDC2	GND	1.8 V



Table 20. DCDC1, DCDC2, and DCDC3 Default Voltage Levels (continued)

PIN	LEVEL	DEFAULT OUTPUT VOLTAGE		
DEEDCDC3	VCC	3.3 V		
DEFDCDC3	GND	1.8 V		

Using an external resistor divider at DEFDCDCx:

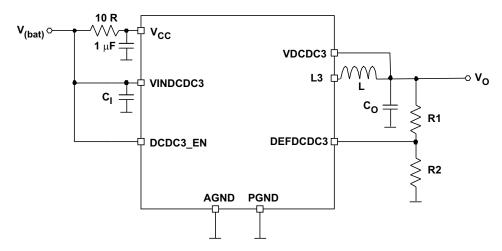


Figure 41. External Resistor Divider

When a resistor divider is connected to DEFDCDCx, the output voltage can be set from 0.6 V up to the input voltage $V_{(bat)}$. The total resistance (R1 + R2) of the voltage divider must be kept in the 1-MR range to maintain a high efficiency at light load.

$$V_{\text{OUT}} = V_{\text{DEFDCDCx}} \times \frac{R1 + R2}{R2} \qquad R1 = R2 \times \left(\frac{V_{\text{OUT}}}{V_{\text{DEFDCDCx}}}\right) - R2$$
(12)

8.2.2.5 VRTC Output

It is required that a 4.7-μF (minimum) capacitor be added to the VRTC pin even if the output is not used.

8.2.2.6 LDO1 and LDO2

The LDOs in the TPS65023x are general-purpose LDOs which are stable using ceramics capacitors. The minimum output capacitor required is 2.2 μ F. The LDOs output voltage can be changed to different voltages between 1 V and 3.3 V using the I²C interface. Therefore, they can also be used as general-purpose LDOs in applications powering processors different from DaVinci. The supply voltage for the LDOs needs to be connected to the VINLDO pin, giving the flexibility to connect the lowest voltage available in the system and provides the highest efficiency.

8.2.2.7 TRESPWRON

This is the input to a capacitor that defines the reset delay time after the voltage at VRTC rises above 2.52 V. The timing is generated by charging and discharging the capacitor with a current of 2 μ A between a threshold of 0.25 V and 1 V for 128 cycles. A 1-nF capacitor gives a delay time of 100 ms.

While there is no real upper and lower limit for the capacitor connected to TRESPWRON, TI recommends not leaving signal pins open.

$$t_{(reset)}$$
 = 2 x 128 x $\left(\frac{(1 \text{ V - 0.25 V}) \text{ x } C_{(reset)}}{2 \mu A}\right)$

where

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- t_(reset) is the reset delay time
- C_(reset) is the capacitor connected to the TRESPWRON pin

(13)

The minimum and maximum values for the timing parameters called ICONST (2 uA), TRESPWRON_UPTH (1 V), and TRESPWRON_LOWTH (0.25 V) can be found under *Electrical Characteristics*.

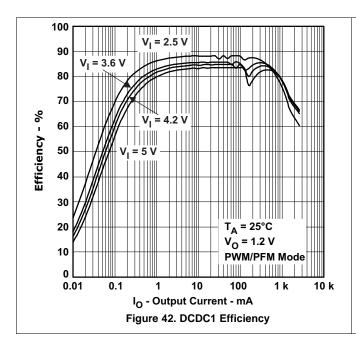
8.2.2.8 V_{CC} Filter

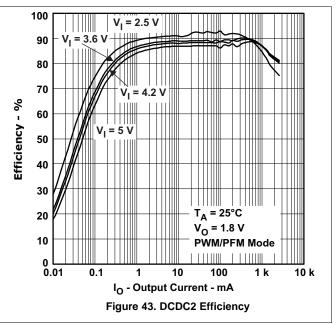
An RC filter connected at the VCC input is used to keep noise from the internal supply for the bandgap and other analog circuitry. A typical value of 1 R and 1 μ F is used to filter the switching spikes, generated by the DC-DC converters. A larger resistor than 10 R must not be used because the current into VCC of up to 3 mA causes a voltage drop at the resistor causing the undervoltage lockout circuitry connected at VCC internally to switch off too early.

8.2.3 Application Curves

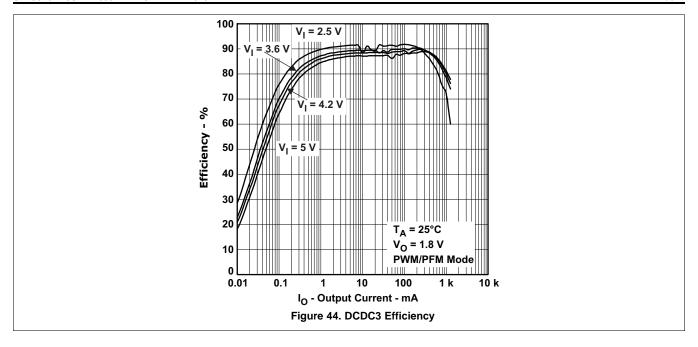
Graphs were taken using the EVM with the following inductor and output capacitor combinations:

CONVERTER	INDUCTOR	OUTPUT CAPACITOR	OUTPUT CAPACITOR VALUE
VDCDC1	VLCF4020-2R2	C2012X5R0J106M	2 × 10 μF
VDCDC2	VLCF4020-2R2	C2012X5R0J106M	2 × 10 μF
VDCDC3	VLF4012AT-2R2M1R5	C2012X5R0J106M	2 × 10 μF









9 Power Supply Recommendations

9.1 Requirements for Supply Voltages Below 3.0 V

For a supply voltage on pins V_{cc} , VINDCDC1, VINDCDC2, and VINDCDC3 below 3.0 V, TI recommends enabling the DCDC1, DCDC2, and DCDC3 converters in sequence. If all 3 step-down converters are enabled at the same time while the supply voltage is close to the internal reset detection threshold, a reset may be generated during power-up. Therefore TI recommends enabling the DC-DC converters in sequence. This can be done by driving one or two of the enable pins with a RC delay or by driving the enable pin by the output voltage of one of the other step-down converters. If a voltage above 3.0 V is applied on pin VBACKUP while V_{CC} and VINDCDCx is below 3.0 V, there is no restriction in the power-up sequencing as VBACKUP will be used to power the internal circuitry.



10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Take care in board layout to get the specified performance. If the layout is not carefully done, the regulators may show poor line, load regulation, or both, along with stability issues and EMI problems. It is critical to provide a low impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitors must be placed as close as possible to the IC pins as well as the inductor and output capacitor.

For TPS65023x, connect the PGND pins of the device to the thermal pad land of the PCB and connect the analog ground connections (AGND) to the PGND at the thermal pad. It is essential to provide a good thermal and electrical connection of all GND pins using multiple vias to the GND-plane. Keep the common path to the AGND pins, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The VDCDCx line must be connected right to the output capacitor and routed away from noisy components and traces (for example, the L1, L2, and L3 traces).

10.2 Layout Example

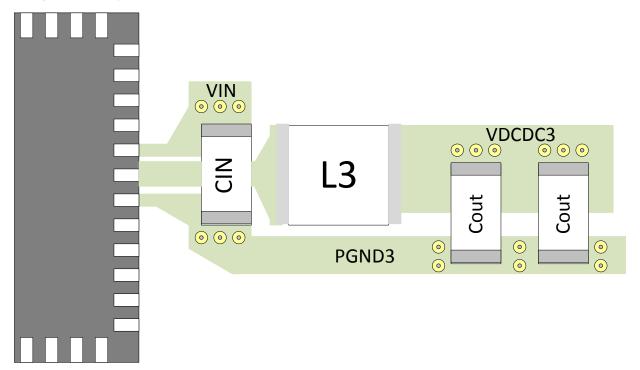


Figure 45. Layout Example of a DC-DC Converter

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

For development support, refer to:

- Altera Cyclone IV FPGA Power Reference Design with TPS65023
- Altera Cyclone III FPGA Power Reference Design with TPS65023
- Integrated Power Supply Reference Design for Xilinx Artix[®]-7, Spartan[®]-7, and Zynq[®]-7000 FPGAs
- Integrated Power Supply Reference Design for Xilinx Zyng® UltraScale+™ ZU2CG-ZU5EV MPSoCs

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, DaVinci™ Sequencing Using The TPS65023 application report
- Texas Instruments, Empowering Designs With Power Management IC (PMIC) for Processor Applications application report
- Texas Instruments, Optimizing Resistor Dividers at a Comparator Input application report
- Texas Instruments, Optimizing OMAP3630 BOOT Sequence Using the TPS65023-Q1 application report
- Texas Instruments, Power Supply Design for NXP i.MX 6 Using the TPS65023 application report
- Texas Instruments, Power Supply Design for NXP i.MX 7 Using the TPS65023 application report
- Texas Instruments, Power Supply Reference Design for Freescale™ i.MX35 Using TPS65021 reference guide
- Texas Instruments, Powering OMAP™3 With TPS65023: Design-In Guide application report
- Texas Instruments, Push-Button Circuit application report
- Texas Instruments, TPS65023x Check List
- Texas Instruments, TPS65023EVM user's guide
- Texas Instruments, TPS65023B/TPS650231EVM user's guide

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 21. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS65023	Click here	Click here	Click here	Click here	Click here
TPS65023B	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration

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Community Resources (continued)

among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TPS65023BRSBR	Active	Production	WQFN (RSB) 40	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023B
TPS65023BRSBR.B	Active	Production	WQFN (RSB) 40	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023B
TPS65023BRSBT	Active	Production	WQFN (RSB) 40	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023B
TPS65023BRSBT.B	Active	Production	WQFN (RSB) 40	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023B
TPS65023BRSBTG4	Active	Production	WQFN (RSB) 40	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023B
TPS65023BRSBTG4.B	Active	Production	WQFN (RSB) 40	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023B
TPS65023RSBR	Active	Production	WQFN (RSB) 40	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023
TPS65023RSBR.B	Active	Production	WQFN (RSB) 40	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023
TPS65023RSBRG4	Active	Production	WQFN (RSB) 40	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023
TPS65023RSBT	Active	Production	WQFN (RSB) 40	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023
TPS65023RSBT.B	Active	Production	WQFN (RSB) 40	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023
TPS65023RSBTG4	Active	Production	WQFN (RSB) 40	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65023

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

PACKAGE OPTION ADDENDUM

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS65023:

Automotive: TPS65023-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65023BRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65023BRSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65023BRSBTG4	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65023RSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65023RSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2



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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65023BRSBR	WQFN	RSB	40	3000	346.0	346.0	33.0
TPS65023BRSBT	WQFN	RSB	40	250	210.0	185.0	35.0
TPS65023BRSBTG4	WQFN	RSB	40	250	210.0	185.0	35.0
TPS65023RSBR	WQFN	RSB	40	3000	346.0	346.0	33.0
TPS65023RSBT	WQFN	RSB	40	250	210.0	185.0	35.0





NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.





NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



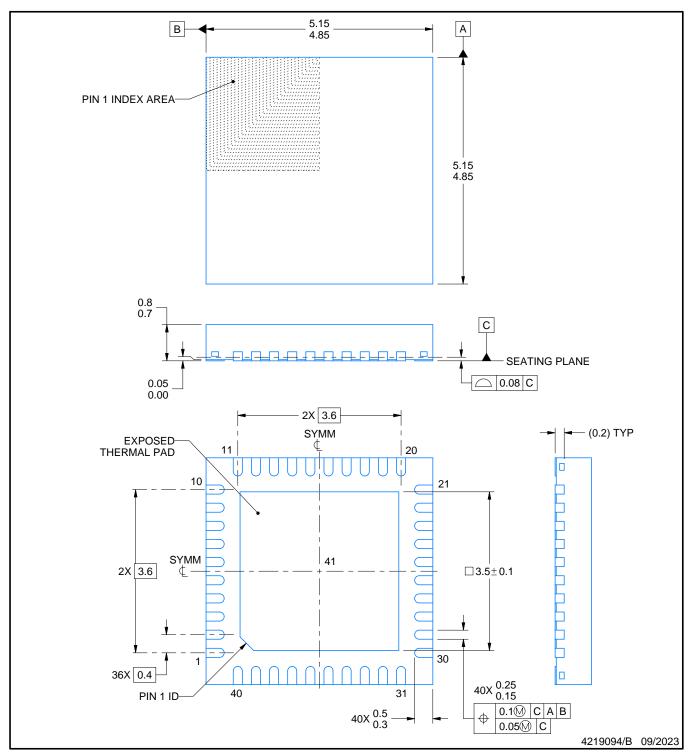


NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



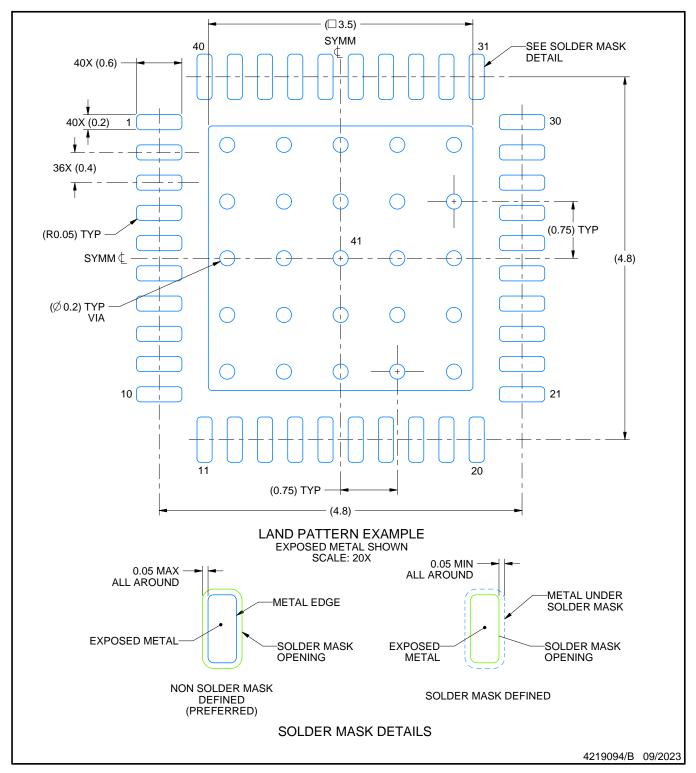




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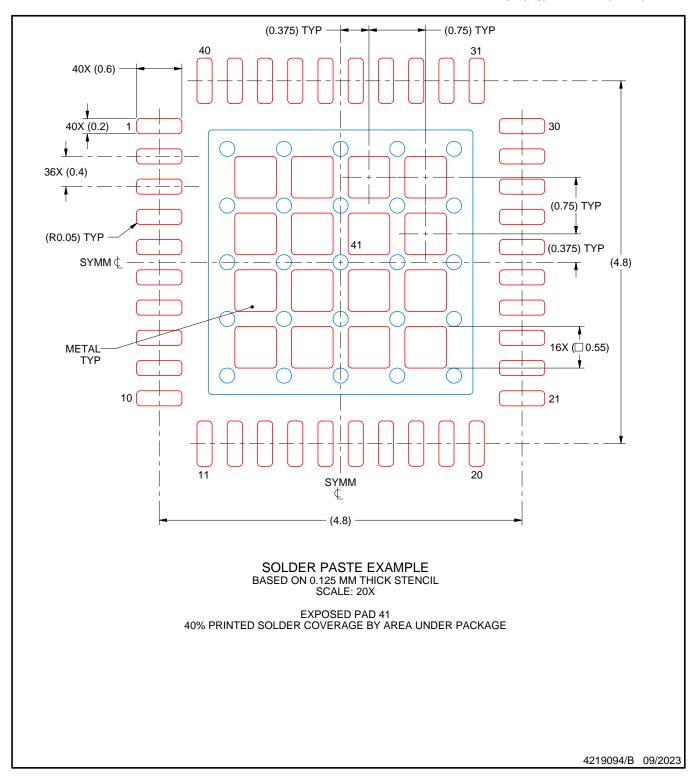




NOTES: (continued)

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NOTES: (continued)

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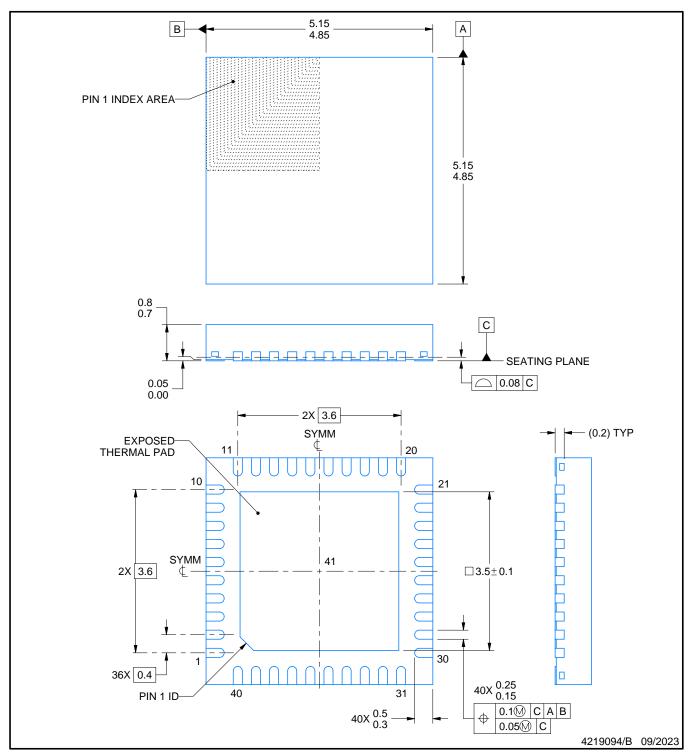
5 x 5 mm, 0.4 mm pitch



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



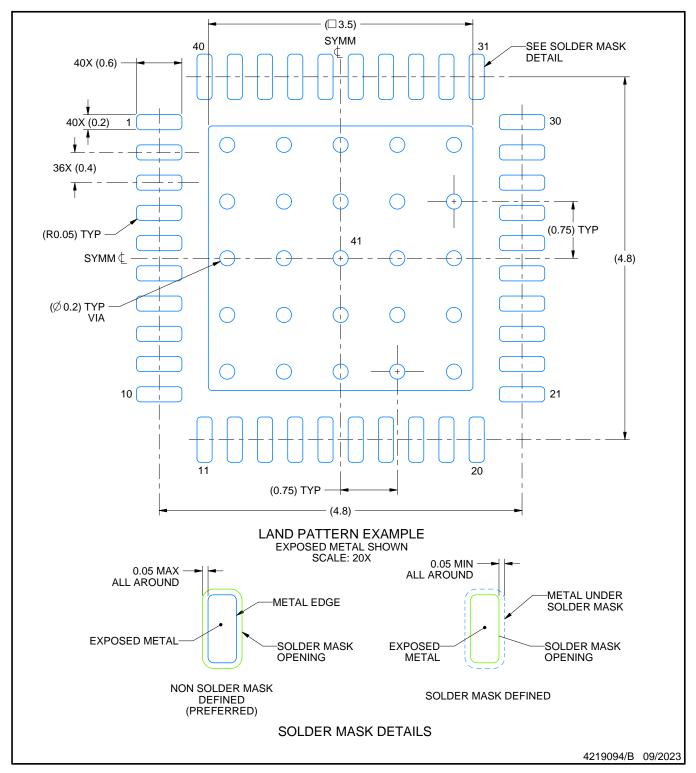




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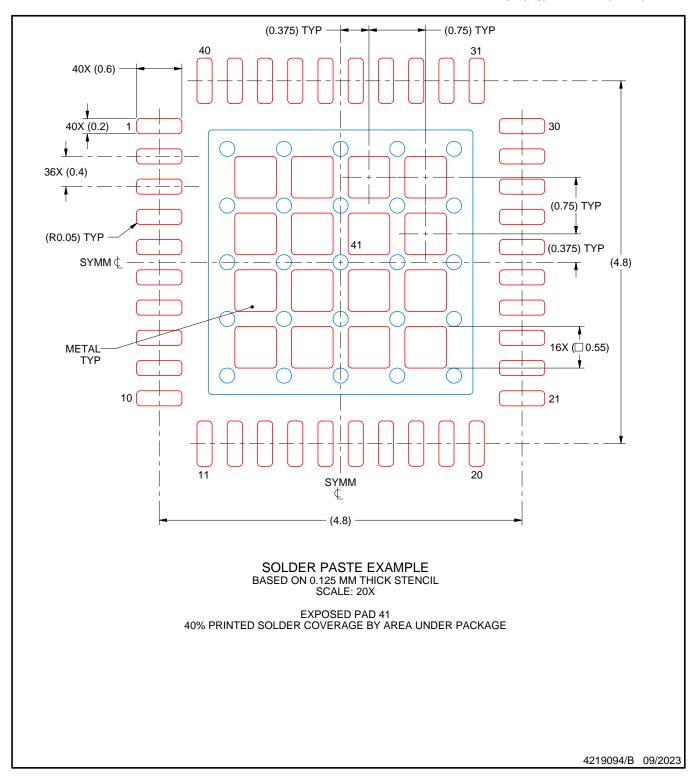




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