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Peak Current Limited Step Down Converter for USB Applications

FEATURES

- High Efficiency Step Down Converter
- Max Peak Current Limit of 1A, Ideal for USB Powered Applications
- V_{IN} Range Optimized for USB from 2V to 6V
- 2.25 MHz Fixed Frequency Operation
- Power Save Mode at Light Load Currents
- Output Voltage Accuracy in PWM mode ±1.5%
- Typ. 15 μA Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- Soft Start
- Voltage Positioning at Light Loads
- Available in a Small 2x2x0,8mm SON package
- Allows <1mm Solution Height

APPLICATIONS

- Portable USB Peripherals
- Wireless Modem Applications
- USB PCTV Applications

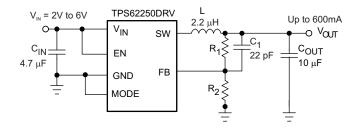
DESCRIPTION

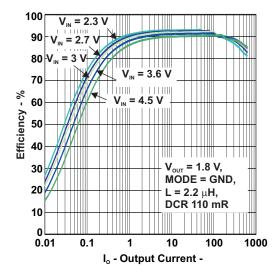
The TPS62250 device is a high efficient synchronous step down dc-dc converter optimized for USB powered applications. It provides up to 1A peak output current and limits the average input current to 700mA, making it ideal for applications connected to a USB host. With an wide input voltage range of 2V to 6V, the device supports applications powered by the USB host as well as general applications requiring large output capacitors.

The TPS62250 operates at 2.25MHz fixed switching frequency and enters Power Save Mode operation at light load currents to maintain high efficiency over the entire load current range.

The Power Save Mode is optimized for low output voltage ripple. For low noise applications such as USB Wireless Modems, the device can be forced into fixed frequency PWM mode by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1 μ A. TPS62250 allows the use of small inductors and capacitors to achieve a small solution size.

The TPS62250 is available in a very small 2x2 6 pin SON package.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T _A	$T_A \hspace{1cm} PART \hspace{1cm} OUTPUT \hspace{1cm} VOLTAGE^{(2)}$		PACKAGE ⁽³⁾	PACKAGE DESIGNATOR	ORDERING	PACKAGE Marking	
-40°C to 85°C	TPS62250	adjustable	SON 2x2-6	DRV	TPS62250DRV	NXH	

- (1) The DRV (2x2-6 SON) package is available in tape & reel. Add R suffix to order quantities of 3000 parts per reel.
- 2) Contact TI for other fixed output voltage options
- (3) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
	Input voltage range (2)		-0.3 to 7	
	Voltage range at EN, Mo	-0.3 to V _{IN} +0.3, ≤ 7	V	
	Voltage on SW		-0.3 to 7	
	Peak output current		Internally limited	Α
		HBM Human body model	2	kV
	ESD rating (3)	CDM Charge device model	1	KV
		Machine model	200	V
TJ	Maximum operating junction temperature		-40 to 125	°C
T _{stg}	Storage temperature rar	nge	-65 to 150	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	POWER RATING FOR T _A ≤ 25°C	DERATING FACTOR ABOVE T _A = 25°C
DRV	76°C/W	1300 mW	13 mW/°C

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM MAX	UNIT
V_{IN}	Supply voltage	2	6	V
	Output voltage range for adjustable voltage	0.6	VIN	٧
T_A	Operating ambient temperature	-40	85	ô
T_J	Operating junction temperature	-40	125	°C

Product Folder Link(s): TPS62250

⁽³⁾ The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

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ELECTRICAL CHARACTERISTICS

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6V. External components C_{IN} = 4.7 μ F 0603, C_{OUT} = 10 μ F 0603, L = 2.2 μ H, see the parameter measurement information.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V _{IN}	Input voltage range		2.3		6	V
		I _{OUT} = 0 mA, PFM mode enabled (MODE = GND) device not switching		15		
I _Q	Operating quiescent current	I_{OUT} = 0 mA, PFM mode enabled (MODE = GND) device switching, V_{OUT} = 1.8 V, See $^{(1)}$		18.5		μΑ
		$I_{OUT} = 0$ mA, switching with no load (MODE = V_{IN}), PWM operation, $V_{OUT} = 1.8$ V, $V_{IN} = 3$ V		3.8		mA
I _{SD}	Shutdown current	EN = GND		0.1	1	μΑ
		Falling		1.85		.,
UVLO	Undervoltage lockout threshold	Rising		1.95		V
ENABLE,	MODE		·			
V _{IH}	High level input voltage, EN, MODE	2 V ≤ V _{IN} ≤ 6 V	1		VIN	V
V _{IL}	Low level input voltage, EN, MODE	2 V ≤ V _{IN} ≤ 6 V	0		0.4	V
I _{IN}	Input bias current, EN, MODE	EN, MODE = GND or VIN		0.01	1	μΑ
POWER S	WITCH					
D	High side MOSFET on-resistance	V - V - 26 V T - 25°C		240	480	mΩ
R _{DS(on)}	Low side MOSFET on-resistance	$V_{IN} = V_{GS} = 3.6 \text{ V}, T_A = 25^{\circ}\text{C}$		185	380	11122
I _{LIMF}	Forward current limit MOSFET high-side and low side	$V_{IN} = V_{GS} = 3.6 \text{ V}$	0.8	1	1.2	Α
_	Thermal shutdown	Increasing junction temperature		140		°C
T _{SD}	Thermal shutdown hysteresis	Decreasing junction temperature		20		C
OSCILLA [®]	TOR					
f_{SW}	Oscillator frequency	$2 \text{ V} \leq \text{V}_{IN} \leq 6 \text{ V}$	2	2.25	2.5	MHz
OUTPUT						
V _{OUT}	Adjustable output voltage range		0.6		V_{IN}	V
V_{ref}	Reference voltage			600		mV
	Feedback voltage PWM Mode	$\label{eq:model} \begin{array}{ll} \text{MODE} = \text{V}_{\text{IN}}, \text{ PWM operation, for fixed output} \\ \text{voltage versions V}_{\text{FB}} = \text{V}_{\text{OUT}}, \\ 2.5 \text{ V} \leq \text{V}_{\text{IN}} \leq 6 \text{ V}, \text{ 0 mA} \leq \text{I}_{\text{OUT}} \leq 600 \text{ mA} \end{array} $	-1.5%	0%	1.5%	
V_{FB}	Feedback voltage PFM mode	MODE = GND, device in PFM mode, voltage positioning active ⁽¹⁾		1%		
	Load regulation	PWM Mode		-0.5		%/A
t _{Start Up}	Start-up time	Time from active EN to reach 95% of V _{OUT} nominal		500		μs
t _{Ramp}	V _{OUT} ramp up time	Time to ramp from 5% to 95% of V _{OUT}		250		μs
I _{lkg}	Leakage current into SW pin	$V_{IN} = 3.6 \text{ V}, V_{IN} = V_{OUT} = V_{SW}, EN = GND^{(3)}$		0.1	1	μΑ

⁽¹⁾ In PFM mode, the internal reference voltage is set to typ. 1.01xV_{ref}. See the parameter measurement information.

Product Folder Link(s): TPS62250

⁽²⁾ For $V_{IN} = V_O + 0.6 \text{ V}$

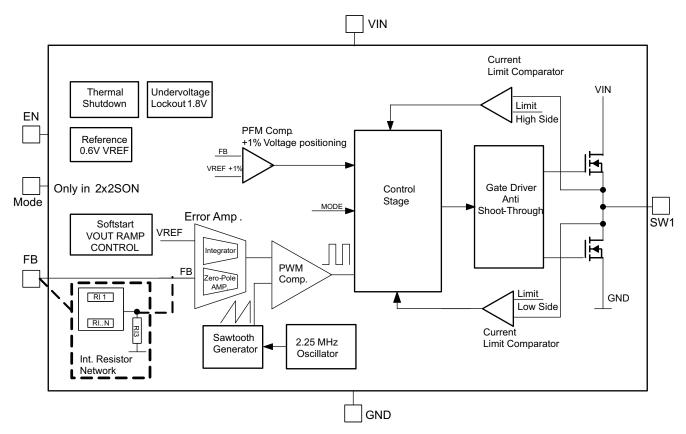
⁽³⁾ In fixed output voltage versions, the internal resistor divider network is disconnected from FB pin.



TERMINAL FUNCTIONS

TERM	IINAL		
NAME	NO. SON 2x2-6	I/O	DESCRIPTION
V_{IN}	5	PWR	VIN power supply pin.
GND	6	PWR	GND supply pin
EN	4	ı	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
SW	1	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
FB	3	ı	Feedback Pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
MODE	2	I	This pin is only available at SON package option. MODE pin = high forces the device to operate in fixed frequency PWM mode. MODE pin = low enables the Power Save Mode with automatic transition from PFM mode to fixed frequency PWM mode.

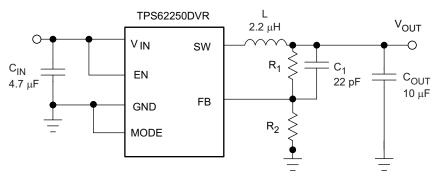
FUNCTIONAL BLOCK DIAGRAM



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PARAMETER MEASUREMENT INFORMATION



L: LPS3015 2.2 μH, 110 mΩ C $_{\rm IN}$ GRM188R60J475K 4.7 μF Murata 0603 size C_{OUT} GRM188R60J106M 10 μF Murata 0603 size



TYPICAL CHARACTERISTICS

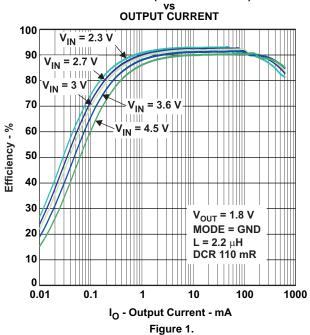
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EFFICIENCY (PWM Mode)

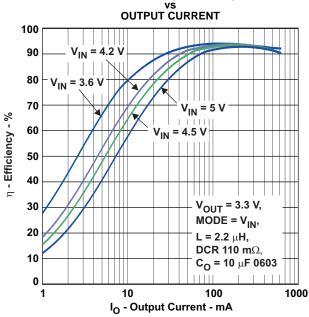
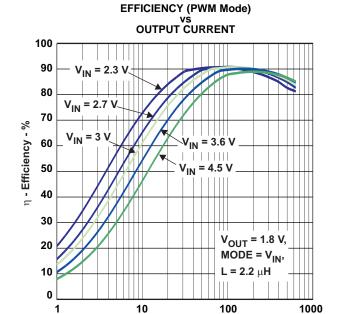


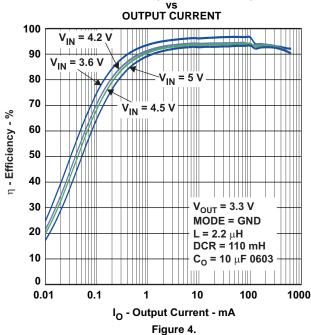
Figure 3.



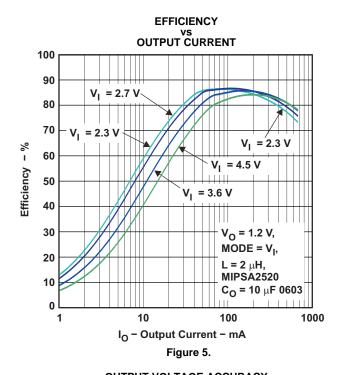
EFFICIENCY (Power Save Mode)

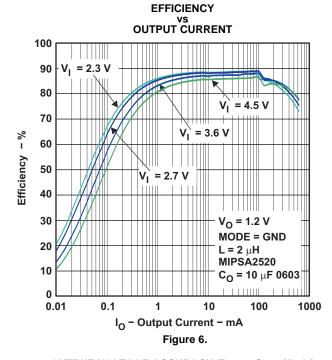
IO - Output Current - mA

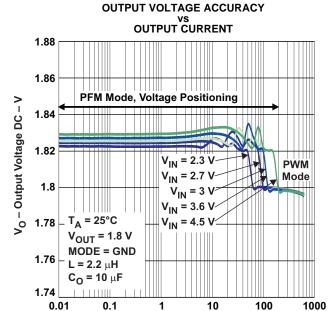
Figure 2.





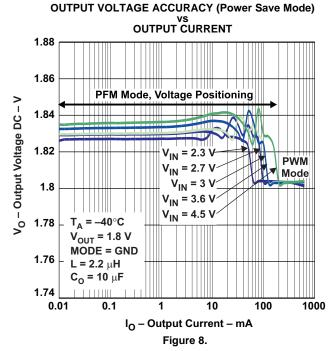






IO - Output Current - mA

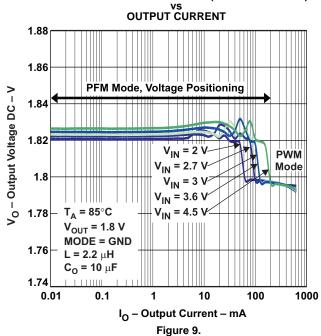
Figure 7.



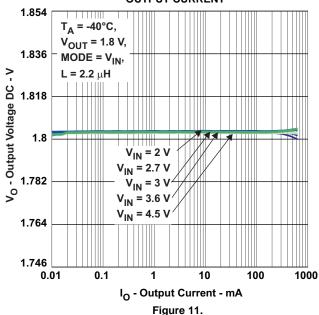


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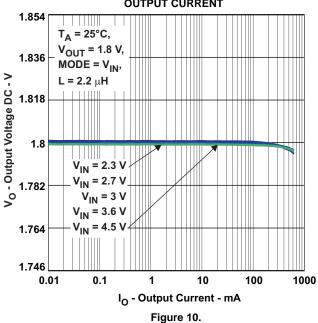
OUTPUT VOLTAGE ACCURACY (Power Save Mode)



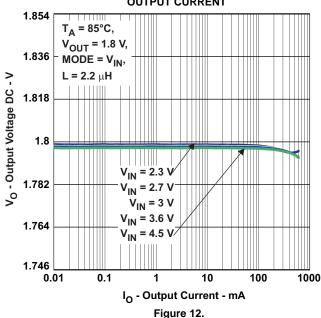
OUTPUT VOLTAGE ACCURACY (PWM Mode) vs OUTPUT CURRENT



OUTPUT VOLTAGE ACCURACY (PWM Mode) vs OUTPUT CURRENT



OUTPUT VOLTAGE ACCURACY (PWM Mode) vs OUTPUT CURRENT







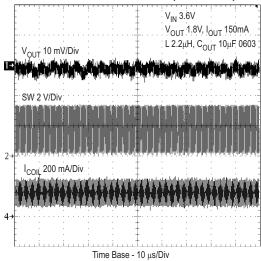


Figure 13.

MODE PIN TRANSITION FROM PWM TO PFM MODE AT LIGHT LOAD

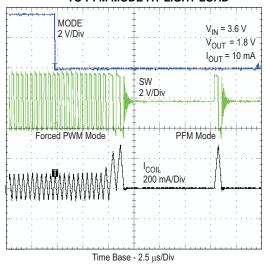


Figure 15.

MODE PIN TRANSITION FROM PFM TO FORCED PWM MODE AT LIGHT LOAD

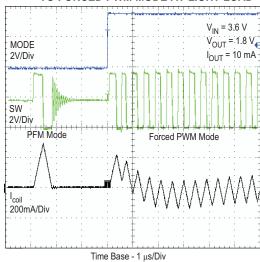


Figure 14.

START-UP TIMING

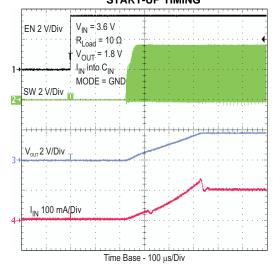


Figure 16.



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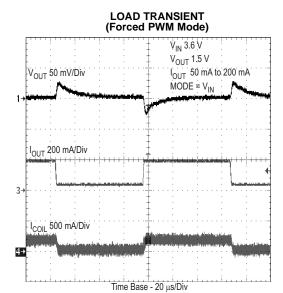


Figure 17.

LOAD TRANSIENT (Forced PFM Mode To PWM Mode) SW 2 V/Div V_{IN} 3.6 V V_{OUT} 1.5 V I_{OUT} 150 μA to 400 mA MODE = GND 1I_{OUT} 500 mA/Div 150 μA

Figure 19.

Time Base - 500 μs/Div

LOAD TRANSIENT (Forced PWM Mode)

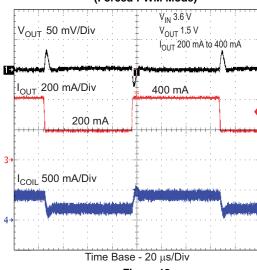


Figure 18.

LOAD TRANSIENT (Forced PWM Mode To PFM Mode)

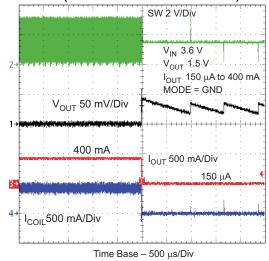


Figure 20.

I_{COIL}, 500mA/Div



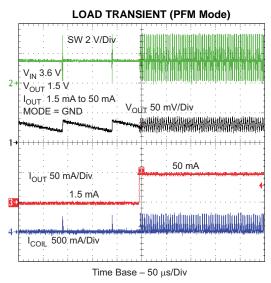
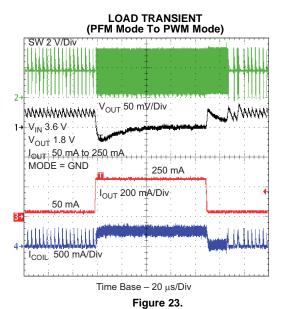


Figure 21.



LOAD TRANSIENT (PFM Mode)

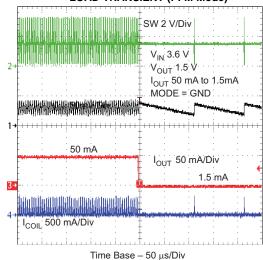


Figure 22.

LOAD TRANSIENT (PFM Mode To PWM Mode)

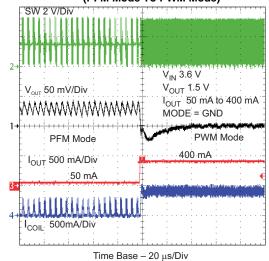


Figure 24.



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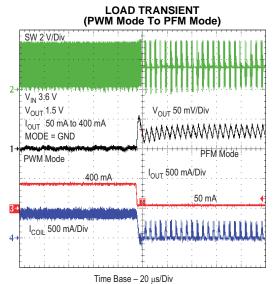


Figure 25.

LINE TRANSIENT (PWM Mode)

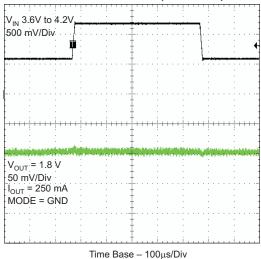


Figure 27.

LINE TRANSIENT (PFM Mode)

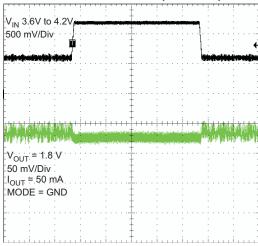


Figure 26.

TYPICAL OPERATION (PFM Mode)

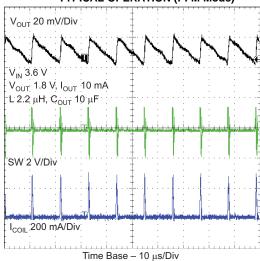


Figure 28.



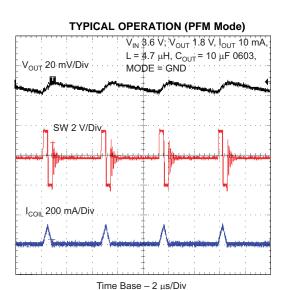
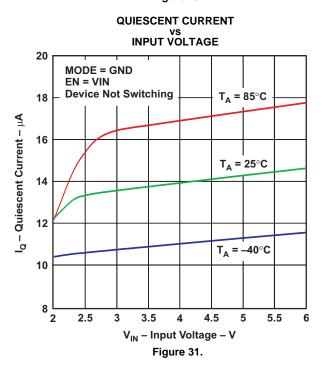
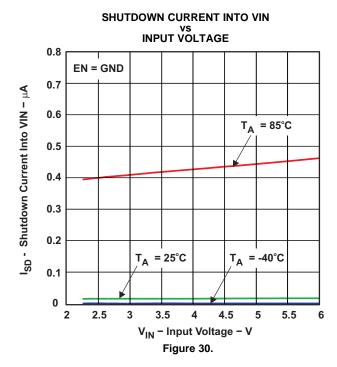
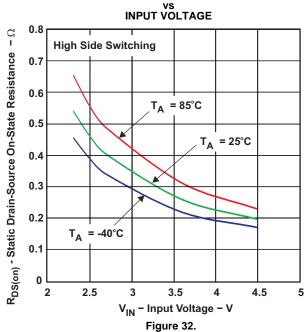


Figure 29.



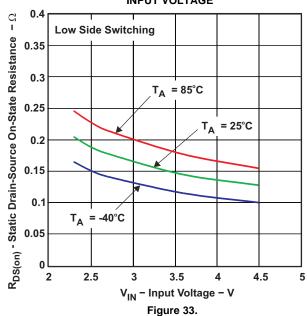


STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs



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STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs INPUT VOLTAGE



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DETAILED DESCRIPTION

OPERATION

The TPS62250 step down converter operates with typically 2.25 MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converter can automatically enter Power Save Mode and operates then in PFM mode.

During PWM operation the converter use a unique fast response voltage mode control scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the High Side MOSFET switch is turned on. The current flows now from the input capacitor via the High Side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic will turn off the switch. The current limit comparator will also turn off the switch in case the current limit of the High Side MOSFET switch is exceeded. After a dead time preventing shoot through current, the Low Side MOSFET rectifier is turned on and the inductor current will ramp down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the Low Side MOSFET rectifier.

The next cycle will be initiated by the clock signal again turning off the Low Side MOSFET rectifier and turning on the on the High Side MOSFET switch.

POWER SAVE MODE

The Power Save Mode is enabled with MODE Pin set to low level. If the load current decreases, the converter will enter Power Save Mode operation automatically. During Power Save Mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage typically +1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the Low Side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the Power Save Mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} nominal +1%, the device starts a PFM current pulse. The High Side MOSFET switch will turn on, and the inductor current ramps up. After the On-time expires, the switch is turned off and the Low Side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single threshold comparator, the output voltage ripple during PFM mode operation can be kept small. The PFM Pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values will minimize the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode. The Power Save Mode can be disabled through the MODE pin set to high. The converter will then operate in fixed frequency PWM mode.

Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is active in Power Save Mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

Submit Documentation Feedback

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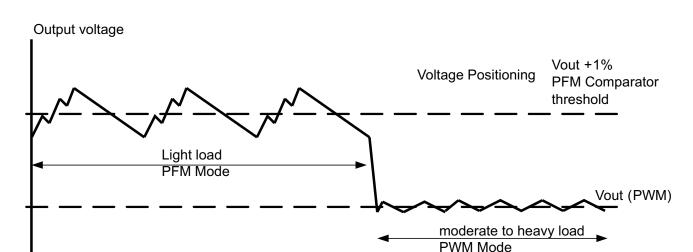


Figure 34. Power Save Mode Operation with automatic Mode transition

100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the High Side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing VIN the High Side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

 $V_{IN}min = V_{O}max + I_{O}max \times (R_{DS(on)}max + R_{L})$

With:

I_Omax = maximum output current plus inductor ripple current

 $R_{DS(on)}$ max = maximum P-channel switch $R_{DS(on)}$.

 $R_1 = DC$ resistance of the inductor

V_Omax = nominal output voltage plus maximum output voltage tolerance

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85V with falling V_{IN} .

MODE SELECTION

The MODE pin allows mode selection between forced PWM mode and Power Save Mode.

Connecting this pin to GND enables the Power Save Mode with automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

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ENABLE

The device is enabled setting EN pin to high. During the start up time $t_{Start\ Up}$ the internal circuits are settled and the soft start circuit is activated. The EN input can be used to control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode in which all internal circuits are disabled. In fixed output voltage versions, the internal resistor divider network is then disconnected from FB pin.

SOFT START

The TPS62250 has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typical 250µs. This limits the inrush current in the converter during ramp up and prevents possible input voltage drops when a battery or high impedance power source is used. The soft start circuit is enabled within the start up time t_{Start Up}.

SHORT-CIRCUIT PROTECTION

The High Side and Low Side MOSFET switches are short-circuit protected with maximum switch current = I_{LIMF}. The current in the switches is monitored by current limit comparators. Once the current in the High Side MOSFET switch exceeds the threshold of it's current limit comparator, it turns off and the Low Side MOSFET switch is activated to ramp down the current in the inductor and High Side MOSFET switch. The High Side MOSFET switch can only turn on again, once the current in the Low Side MOSFET switch has decreased below the threshold of its current limit comparator.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J , exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

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APPLICATION INFORMATION

Figure 35. TPS62250DRV Adjustable 1.2-V Output

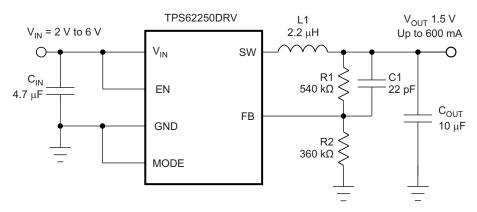


Figure 36. TPS62250 adjustable 1.5-V Output

OUTPUT VOLTAGE SETTING

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)_{\text{with an internal reference voltage } V_{REF} \text{ typical } 0.6\text{V}.$$

To minimize the current through the feedback divider network, R_2 should be 180 k Ω or 360 k Ω . The sum of R_1 and R_2 should not exceed ~ $1M\Omega$, to keep the network robust against noise. An external feed forward capacitor C₁ is required for optimum load transient response. The value of C₁ should be in the range between 22pF and 33pF.

Route the FB line away from noise sources, such as the inductor or the SW line.

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The TPS62250 is designed to operate with inductors in the range of 1.5µH to 4.7µH and with output capacitors in the range of 4.7μ F to 22μ F. The part is optimized for operation with a 2.2μ H inductor and 10μ F output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1µH effective inductance and 3.5µF effective capacitance.

Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_1) decreases with higher inductance and increases with higher V₁ or V₀.

The inductor selection has also impact on the output voltage ripple in PFM mode. Higher inductor values will lead to lower output voltage ripple and higher PFM frequency, lower inductor values will lead to a higher output voltage ripple but lower PFM frequency.

Equation 1 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

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$$\Delta I_{L} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f}$$
(1)

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_{L}}{2}$$
(2)

With:

f = Switching Frequency (2.25MHz typical)

L = Inductor Value

 ΔI_1 = Peak-to-Peak inductor ripple current

I_{Lmax} = Maximum Inductor current

A more conservative approach is to select the inductor current rating just for the switch current limit I_{LIMF} of the converter.

Accepting larger values of ripple current allows the use of lower inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- · Radiation losses

Table 1. List of Inductors

DIMENSIONS [mm ³]	Inductance μH	INDUCTOR TYPE	SUPPLIER
2.5x2.0x1.0max	2.0	MIPS2520D2R2	FDK
2.5x2.0x1.2max	2.0	MIPSA2520D2R2	FDK
2.5x2.0x1.0max	2.2	KSLI-252010AG2R2	Htachi Metals
2.5x2.0x1.2max	2.2	LQM2HPN2R2MJ0L	Murata
3x3x1.5max	2.2	LPS3015 2R2	Coilcraft

Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS62250 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{\text{RMSCout}} = \text{Vout} \times \frac{1 - \frac{\text{Vout}}{\text{Vin}}}{\text{L} \times f} \times \frac{1}{2 \times \sqrt{3}}$$
(3)

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta \text{Vout} = \text{Vout} \times \frac{1 - \frac{\text{Vout}}{\text{Vin}}}{\text{L} \times f} \times \left(\frac{1}{8 \times \text{Cout} \times f} + \text{ESR}\right)$$
(4)

At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor and inductor value. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten DC output accuracy in PFM mode.

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Input Capacitor Selection

An input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a $4.7\mu F$ to $10\mu F$ ceramic capacitor is recommended. Because ceramic capacitor loses up to 80% of its initial capacitance at 5 V, it is recommended that $10\mu F$ input capacitors be used for input voltages > 4.5V. The input capacitor can be increased without any limit for better input voltage filtering. Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or VIN step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 2. List of Capacitors

CAPACITANCE	TYPE	SIZE	SUPPLIER		
4.7μF	GRM188R60J475K	0603 1.6x0.8x0.8mm ³	Murata		
10μF	GRM188R60J106M69D	0603 1.6x0.8x0.8mm ³	Murata		

LAYOUT CONSIDERATIONS

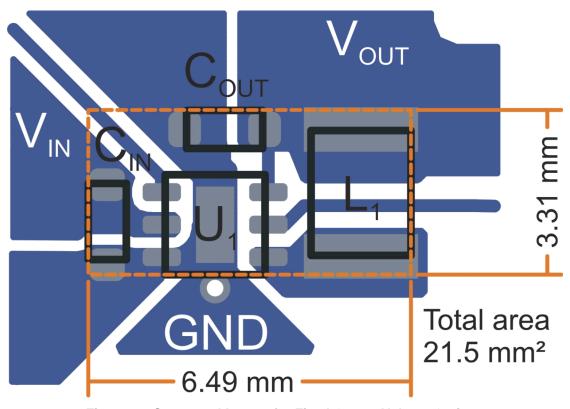


Figure 37. Suggested Layout for Fixed Output Voltage Options



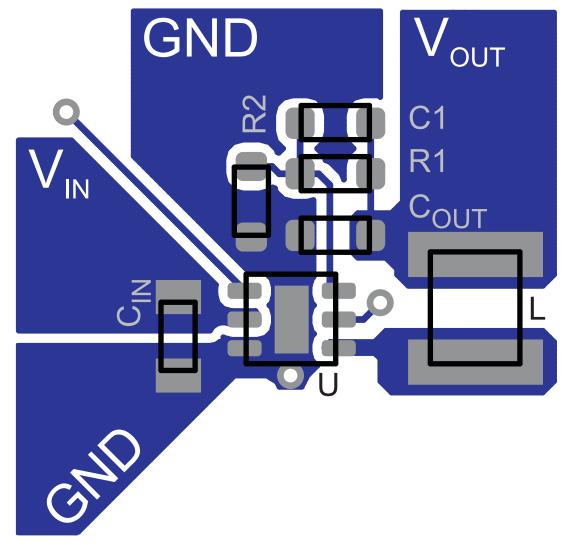


Figure 38. Suggested Layout for Adjustable Output Voltage Version

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND Pin of the device to the PowerPAD™ land of the PCB and use this pad as a star point. Use a common Power GND node and a different node for the Signal GND to minimize the effects of ground noise. Connect these ground nodes together to the PowerPAD land (star point) underneath the IC. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected right to the output capacitor and routed away from noisy components and traces (e.g., SW line).

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ MSL rating/		Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TPS62250DRVR	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	NXH
TPS62250DRVR.A	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXH
TPS62250DRVR.B	Active	Production	WSON (DRV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXH
TPS62250DRVT	Active	Production	WSON (DRV) 6	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	NXH
TPS62250DRVT.A	Active	Production	WSON (DRV) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXH
TPS62250DRVT.B	Active	Production	WSON (DRV) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXH

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62250DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62250DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62250DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS62250DRVT	WSON	DRV	6	250	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4206925/F







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.





NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
- number SLUA271 (www.ti.com/lit/slua271).

 5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.





NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







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NOTES: (continued)

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