TPS61299-Q1 95nA Quiescent Current, 5.5V Boost Converter with Input Current Limit and Fast Transient Performance

1 Features

- AEC-Q100 qualified:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Input voltage range: 0.5V to 5.5V
- 0.7V minimum input voltage for start-up
- Input operating voltage down to 150mV with signal V_{IN} > 0.7V
- Output voltage range: 1.8V to 5.5V VSEL pin select output voltage
- Average input current limit: 1.2A
- 95nA typical quiescent current from VOUT
- 60nA typical shutdown current from VIN and SW
- Up to 91% efficiency at V_{IN} = 3.6V, V_{OUT} = 5V, and I_{OUT} = 10µA
- Up to 94 % efficiency at V_{IN} = 3.6V, V_{OUT} = 5V, and I_{OUT} = 200mA
- True disconnection at EN low
- Automatic PFM/PWM mode transition
- Auto pass-through at V_{IN} > V_{OUT}
- Output SCP and thermal shutdown protections
- SOT563 package (1.6mm x 1.6mm)

2 Applications

- Automotive infotainment and cluster
- Automotive rear lighting
- Advanced driver-assistance system (ADAS)

3 Description

The TPS61299-Q1 is a synchronous boost converter with 95nA ultra-low quiescent current and average input current limit. The device provides a power solution for portable equipment with alkaline battery and coin cell battery. This device operates at high efficiency under light-load condition to achieve long operation time and average input current limit can avoid battery discharging with high current.

The TPS61299-Q1 has wide input voltage range from 0.5V to 5.5V and output voltage range from 1.8V to 5.5V. The average input current limit of this device is 1.2A. The TPS61299-Q1 with 1.2A current limit can support up to 500mA output current from 3V to 5V conversion and achieve approximately 94% efficiency at 200mA load.

The TPS61299-Q1 has optional fast-load transient performance at output voltage is 4.5V, 5V, or 5.5V.

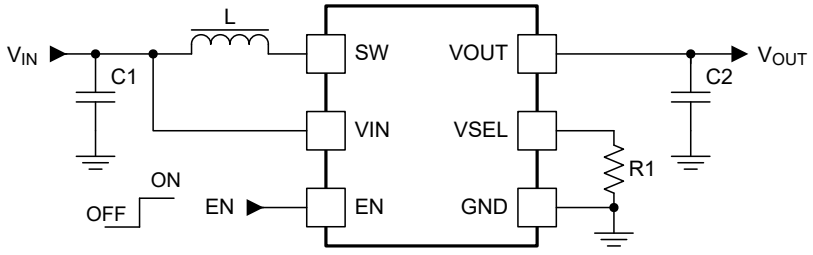
The TPS61299-Q1 supports true shutdown function when it is disabled.

TThe TPS61299-Q1 offers a very small solution size with 1.6mm × 1.6mm SOT563 package.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS61299-Q1	SOT563	1.6mm × 1.6mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

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4 Pin Configuration and Functions

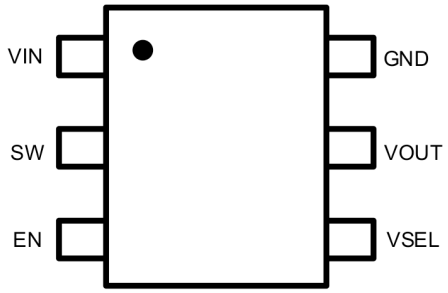


Figure 4-1. DRL Package Top View

Table 4-1. Pin Functions

TERMINAL		I/O	DESCRIPTION
NAME	DRL		
VIN	1	PWR	IC power supply input
SW	2	I	The switch pin of the converter. It is connected to the drain of the internal low-side power MOSFET and source of the internal high-side power MOSFET.
EN	3	I	Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device.
VSEL	4	I	Boost output voltage selection pin. Connect a resistor between this pin and ground to select one of 21 output voltages.
VOUT	5	PWR	Boost converter output
GND	6	PWR	Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VIN, VOUT, SW, EN, VSEL	–0.3	6.5	V
	SW spike at 10 ns	-0.7	8	V
	SW spike at 1 ns	-0.7	10	V
T_J	Operating Junction Temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0.5		5.5	V
V_{OUT}	Boost output voltage	1.8		5.5	V
T_J	Junction temperature	–40		125	°C
L	Effective Inductance	0.47*0.7	1.0	1.0*1.3	µH
C_{OUT}	Effective Output Capacitance at the OUT pin, with output currrent lower than 1A	5*0.8	10		µF
	Effective Output Capacitance at the OUT pin, with output currrent higher than 1A or TPS612997Q is used		20		uF
C_{IN}	Effective Input Capacitance at the VIN pin	2.2			µF

5.4 Thermal Information

THERMAL METRIC(1)		TPS61299-Q1 DRL 6-PINS Standard	TPS61299-Q1 DRL-6PINS EVM	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.6	93.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.6	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.6	7.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.4	39.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

T_J = -40°C to 150°C, V_{IN} = 3.6V and V_{OUT} = 5.0V. Typical values are at T_J = 25°C, unless otherwise noted.

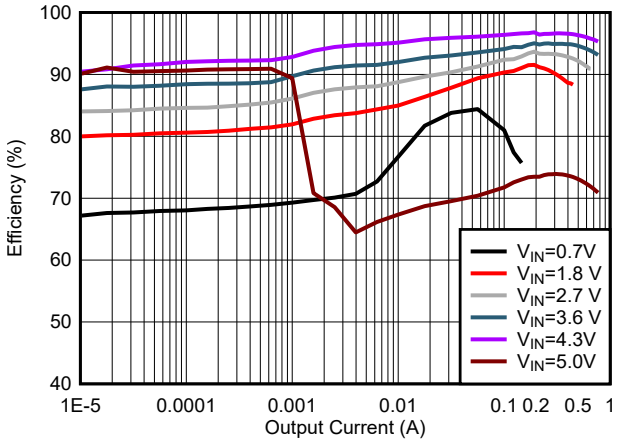
PARAMETER		Version	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{IN}	Input voltage range	All		0.5		5.5	V
V_{IN_UVLO}	Under-voltage lockout threshold	All	V_{IN} rising			0.7	V
V_{IN_UVLO}	Under-voltage lockout threshold	All	V_{IN} falling			0.5	V
I_Q	Quiescent current into VIN pin	All	IC enabled, No load, No switching, T_J up to 85°C		0.5		nA
I_Q	Quiescent current into VOUT pin	All	IC enabled, No load, No switching, T_J up to 85°C		95	300	nA
I_{SD}	Shutdown current into VIN pin	All	EN = LOW, VIN = 3.6V, VOUT = 0V		60		nA
I_{LKG_SW}	Leakage current into SW pin (from SW pin to VOUT pin)	All	VSW = 3.0V, V_{OUT} = 0V, TJ = 25°C		1	4	nA
I_{LKG_SW}	Leakage current into SW pin (from SW pin to VOUT pin)	All	VSW = 3.0V, V_{OUT} = 0V, TJ = 85°C		1		nA
I_{LKG_SW}	Leakage current into SW pin (from SW pin to GND pin)	All	VSW = 3.0V, V_{OUT} = 0V, TJ = 25°C		1	15	nA
I_{LKG_SW}	Leakage current into SW pin (from SW pin to GND pin)	All	VSW = 3.0V, V_{OUT} = 0V, TJ up to 85°C		1	200	nA
OUTPUT							
V_{OUT}	Output voltage setting range	All		1.8		5.5	V
$V_{OUT\_PWM\_ACY}$	Output voltage accuracy	All	PWM, PFM mode	-2		2	%
$V_{OUT\_SNOOZE\_ACY}$	Output voltage accuracy	All	normal mode	$V_{OUT\_PWM\_ACY}$+37.5mV			V
			fast mode	$V_{OUT\_PWM\_ACY}$+15mV			V

T_J = -40°C to 150°C, V_{IN} = 3.6V and V_{OUT} = 5.0V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		Version	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(on)}$	High-side MOSFET on resistance	All	V_{OUT} = 5.0V		150		mΩ
$R_{DS(on)}$	Low-side MOSFET on resistance	All	V_{OUT} = 5.0V		88		mΩ
I_{LIM}	Input current limit	TPS61299Q	V_{IN} = 3.6V, V_{OUT} = 5.0V	0.96	1.2	1.44	A
I_{LH}	Inductor current ripple	TPS61299Q	PWM		350		mA
APPLICATION							
LOGIC INTERFACE							
V_{EN_H}	EN logic high threshold	All	V_{IN} >= 1.05V			0.84	V
V_{EN_L}	EN logic low threshold	All	V_{IN} >= 1.05V	0.36			V
V_{EN_H}	EN logic high threshold	All	V_{IN} < 1.05V			0.8*VIN	V
V_{EN_L}	EN logic low threshold	All	V_{IN} < 1.05V	0.2*VIN			V
I_{EN_LKG}	Leakage current into EN pin	All	VEN=5V		1	50	nA
R_{EN}	EN pin pulldown resistor	All	EN=low		800		kΩ
PROTECTION							
T_{SD}	Thermal shutdown threshold		T_J rising		150		°C
T_{SD_HYS}	Thermal shutdown hysteresis		T_J falling below T_{SD}		20		°C

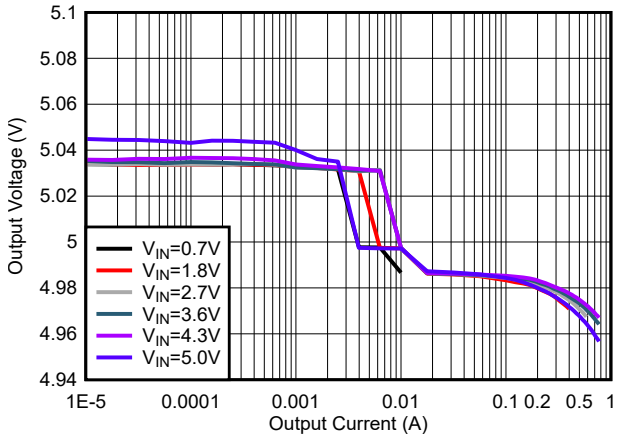
5.6 Typical Characteristics

V_{IN} = 3.6V, V_{OUT} = 5V, Normal Mode, T_J = 25°C, unless otherwise noted



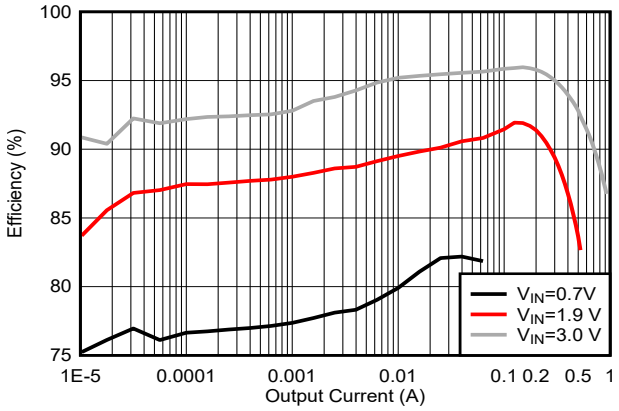
V_{IN} = 0.7V, 1.8V, 2.7V, 3.6V, 4.3V, 5.0V; V_{OUT} = 5.0V

Figure 5-1. 5.0V VOUT Efficiency with Different Inputs Under Normal Mode



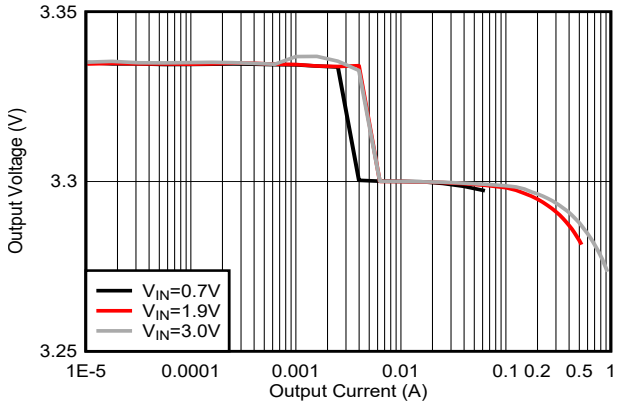
V_{IN} = 0.7V, 1.8V, 2.7V, 3.6V, 4.3V, 5.0V; V_{OUT} = 5.0V

Figure 5-2. 5.0V VOUT Efficiency with Different Inputs Under Normal Mode



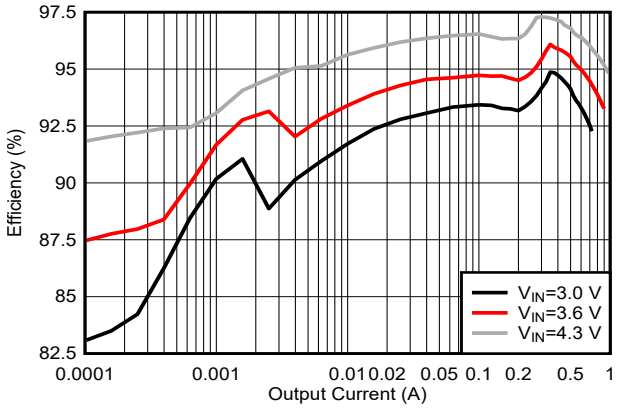
V_{IN} = 0.7V, 1.9V, 3.0V ; V_{OUT} = 3.3V

Figure 5-3. 3.3V VOUT Efficiency with Different Inputs Under Normal Mode



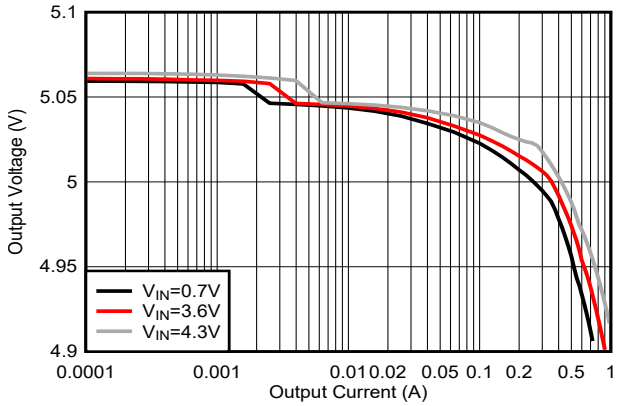
V_{IN} = 0.7V, 1.9V, 3.0V ; V_{OUT} = 3.3V

Figure 5-4. 3.3V VOUT Load Regulation Under Normal Mode



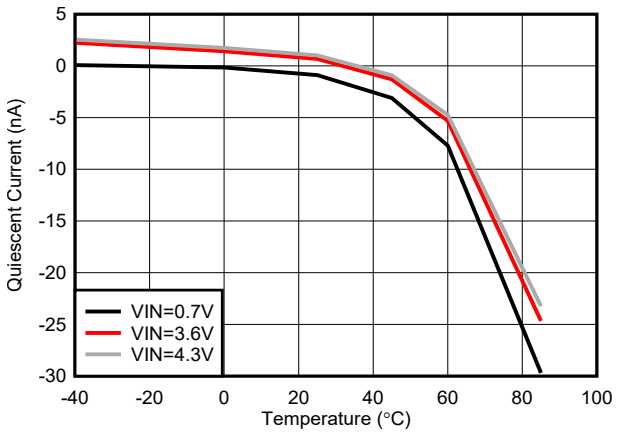
V_{IN} = 3.0V, 3.6V, 4.3V; V_{OUT} = 5.0V

Figure 5-5. 5.0V VOUT Efficiency with Different Inputs Under Fast Mode



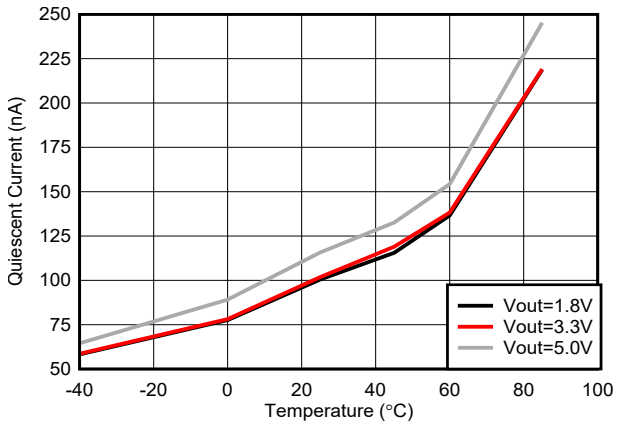
V_{IN} = 3.0V, 3.6V, 4.3V; V_{OUT} = 5.0V

Figure 5-6. 5.0V VOUT Load Regulation with Different InputsUnder Fast Mode



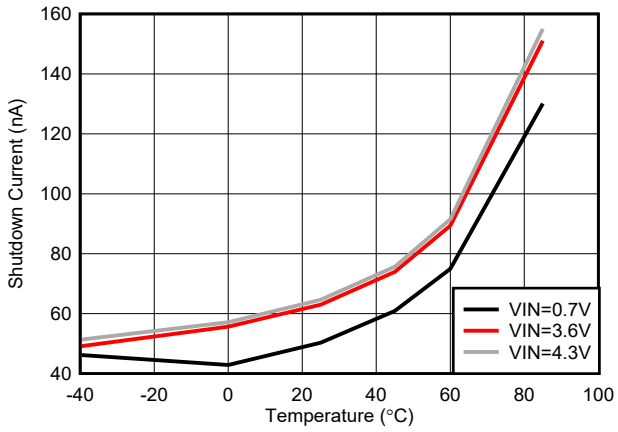
V_{IN} = 0.7V, 3.6V 4.3V; V_{OUT} = 5V, T_J = –40°C to +85 °C, No switching

Figure 5-7. Quiescent Current into VIN vs Temperature



V_{IN} = 1.5V; V_{OUT} = 1.8V , 3.3V , 5V, T_J = –40°C to +85 °C, No switching

Figure 5-8. Quiescent Current into VOUT vs Temperature



V_{IN} = 0.7V, 3.6V 4.3V; V_{OUT} = 0V, T_J = –40°C to +85 °C

Figure 5-9. Shutdown Current vs Temperature

6 Detailed Description

6.1 Overview

The TPS61299-Q1 is a synchronous step-up converter and operates in a hysteretic control scheme. The TPS61299-Q1 has a wide input voltage supply range between 0.5V and 5.5V (0.7V rising voltage for start-up). It only consumes 95nA quiescent current and can achieve up high efficiency under light load condition.

The TPS61299-Q1 support the average input current limit of 1.2A and support true shutdown function at EN is low.

TPS61299-Q1 provides a fast transient performance mode and accurate load regulation mode for different system.

6.2 Functional Block Diagram

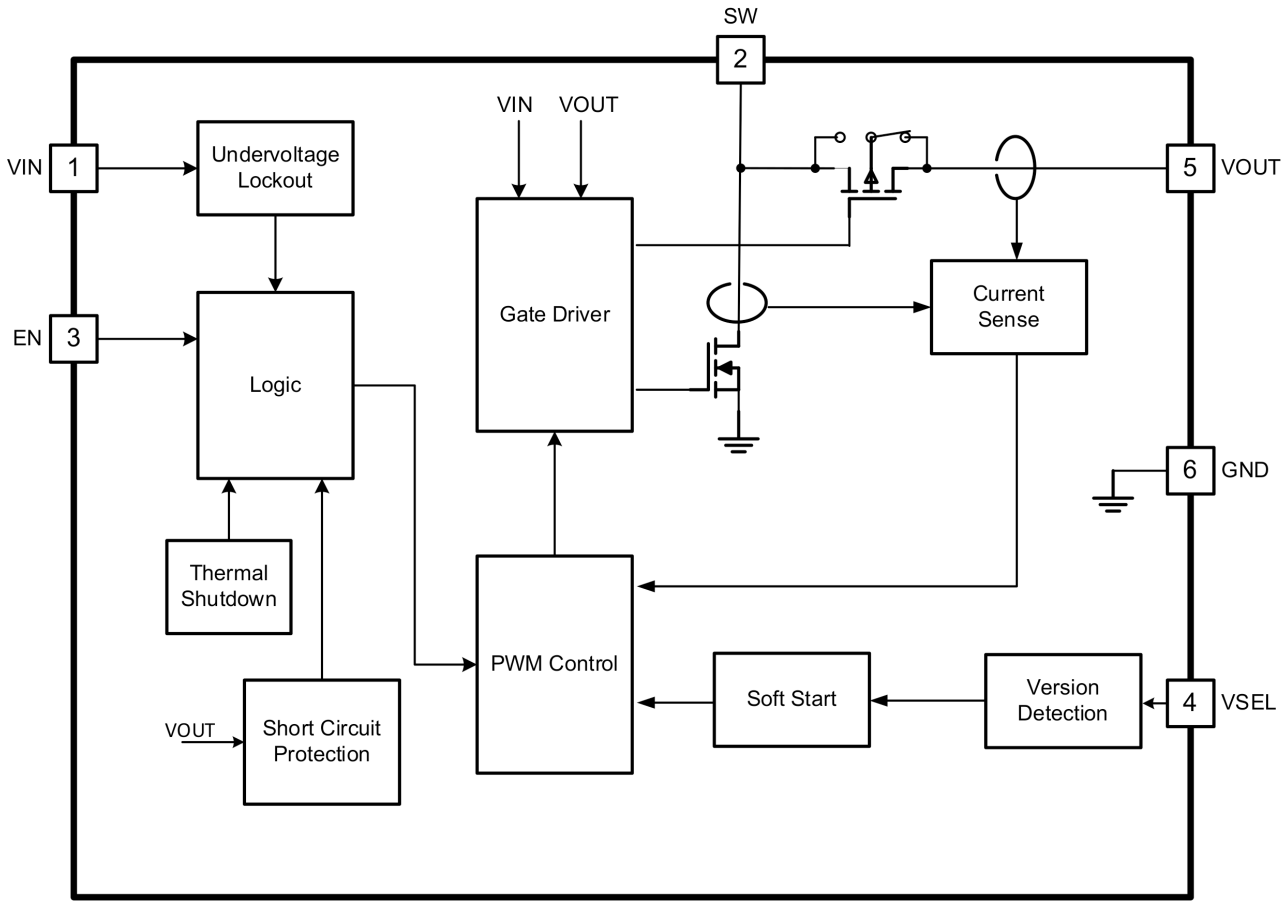


Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Boost Control Operation

The TPS61299-Q1 boost converter is controlled by a hysteretic current mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant in the range of 350mA and adjusting the valley current of this inductor depending on the output load. Since the input voltage, output voltage and inductor value all affect the rising and falling slopes of inductor ripple current, the switching frequency is not fixed and is determined by the operation condition. If the required average input current is lower than the average inductor current defined by this constant ripple, the inductor current goes discontinuously to keep the efficiency high under light load condition. If the load current is reduced further, the boost converter enters into Burst mode. In Burst mode, the boost converter ramps up the output voltage with several switching cycles. Once the output voltage exceeds a setting threshold (Vout_target + 50mV in normal mode and Vout_target + 25mV in fast load transient mode), the device stops switching and goes into a sleep status. In sleep status, the device consumes less quiescent current, 95nA. The boost converter resumes switching when the output voltage is below the setting threshold (Vout_target + 25mV in normal mode and Vout_target + 10mV in fast load transient mode). The device exits the Burst mode when the output current can no longer be supported in this mode.

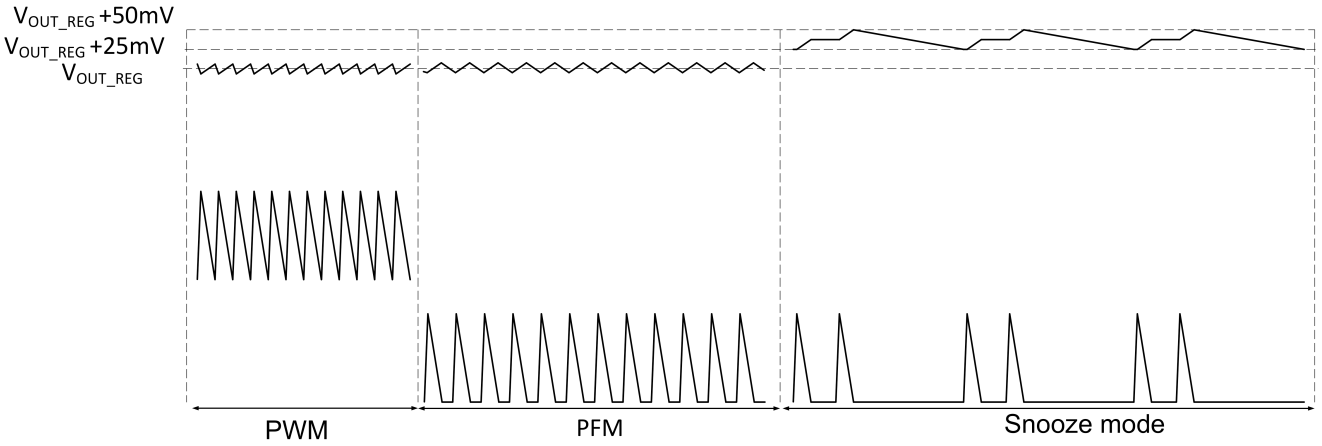


Figure 6-2. Control Modes under Different Load

6.3.2 Version Detection

The TPS61299-Q1 supports 21 internal output voltage setting options by connecting a resistor between the VSEL pin and ground.

During start-up, when output voltage reaches close to 1.8V, the device starts to detect the configuration

conditions of the VSEL pin. The TPS61299-Q1 checks the VSEL pin by lowering resistance setting options to higher setting options until the user finds the setting configuration by a 10µs clock. After detecting the configuration, the TPS61299-Q1 latches the setting output regulation voltage.

The TPS61299-Q1 does not detect the VSEL pins during operation, so changing the resistor during operation does not change the VSEL setting. Toggling the EN pin during operation is one way to refresh it.

For proper operation, TI suggests that the setting resistance accuracy must be 1% and the parasitic capacity of

the VSEL pin be less than 10pF.

Table 6-1. VSEL Pin Configuration

Resistance (kΩ)	VOUT_REG (V)	Resistance (kΩ)	VOUT_REG (V)	Resistance (kΩ)	VOUT_REG (V)	Resistance (kΩ)	VOUT_REG (V)
0(GND)	3.3	12.1	4.5	49.9	3.6	191	2.5
3.01	5.5	14.7	4.5(fast)	75	3.5	237	2.2
4.75	5.5(fast)	18.2	4.3	100	3.2	294	2
6.19	5.2	22.6	4	124	3	365	1.8
7.87	5	28.7	3.8	154	2.8	442/ VOUT pin	5(fast)
9.76	4.8						

6.3.3 Under-voltage Lockout

The TPS61299-Q1 has a built-in under-voltage lockout (UVLO) circuit to ensure the device working properly. When the input voltage is above the UVLO rising threshold of 0.7V, the TPS61299-Q1 can be enabled to boost the output voltage. After the TPS61299-Q1 starts up and the output voltage is above 1.8V, the TPS61299-Q1 can work with the input voltage as low as 0.5V.

6.3.4 Switching Frequency

The TPS61299-Q1 boost converter does not have fixed frequency and it maintains a constant inductor ripple current in the range of 350mA, so the frequency is determined by the operation condition. The frequency is approximately 3MHz, the input is 3.6V, output is 5V, inductor is 1µH. Refer to to calculate the efficiency. The estimated switching frequency f in continuous current mode can be calculated by Equation 1. The switching frequency is not a constant value, but is determined by induction, input voltage, and output voltage.

$$f = \frac{V_{IN} \times (V_{OUT} - V_{OUT} \times \eta)}{L \times I_{LH} \times V_{OUT}} \quad (1)$$

where

- L is the inductor value
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

6.3.5 Input Current Limit

The TPS61299-Q1 employs the input average current protection (OCP) function. If the inductor average current reaches the current limit threshold ILIM, the control loop can limit the inductor average current. In this case the output voltage decreases until the power balance between input and output is achieved. If the output drops below the input voltage, the TPS61299-Q1 enters into Down Mode. If the output drops below 1.6V, the TPS61299-Q1 enters into startup process again. In Pass-Through operation, input current limit function is not enabled.

6.3.6 Enable and Disable

When the input voltage is above UVLO rising threshold and the EN pin is pulled to high voltage, the TPS61299-Q1 is enabled. When the EN pin is pulled to low voltage, the TPS61299-Q1 goes into true shutdown mode. . In true shutdown mode, the device stops switching and the high-side MOSFET fully turns off, providing the completed disconnection between input and output. Less than 60nA input current is consumed in shutdown mode.

6.3.7 Soft-Start Timing

After the EN pin is tied to high voltage, the TPS61299-Q1 begins to startup.

For the high input current limit is 250mA, 500mA, 1.2A and 1.9A version, at the beginning, when output voltage is lower than 0.5V, device limits the output power for the short protection. As output voltage is higher than 0.5V, the device operates at the boundary of Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM), and the inductor peak current is limited to around 350mA during this stage. After the output voltage reaches close to 1.8V, the TPS61299-Q1starts to detect the output voltage configuration of the VSEL pins, then latches the configuration. The version detection time depends on the resistance at VSEL pin, the higher resistance, the longer version detection time. Eg. for 5V normal version, the TPS61299-Q1 needs approximately 170µs for version detection. After version detection, TPS61299-Q1 continues switching and output ramps up further. The internal soft-start time is approximately 1.3ms, and the output soft start time varies with the different output capacitance, load condition, and configuration conditions. The TPS61299-Q1 limits the inductor average current lower than 500mA, (input current limit to 250mA for 250mA version) when output voltage is lower than 2.5V. In this way, the soft start function reduces the inrush current during startup.

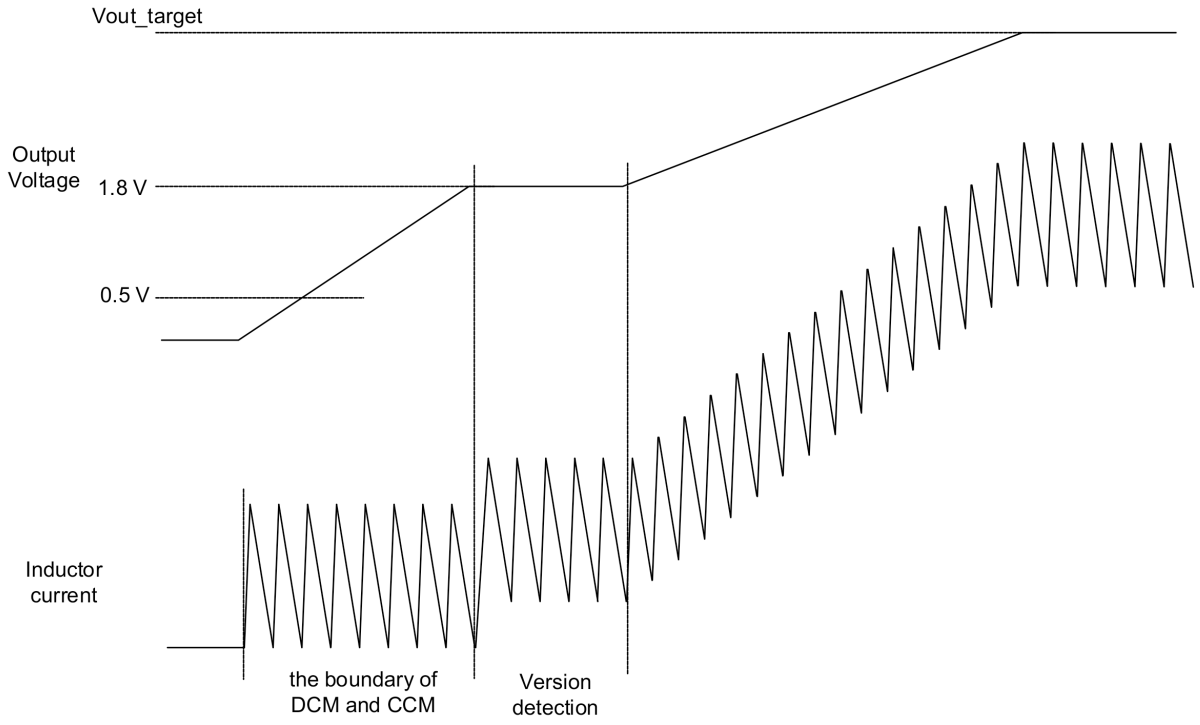


Figure 6-3. Soft-Start Timing

6.3.8 Down Mode

During the start-up, when the input voltage is higher than the output voltage, the TPS61299-Q1 works at the down mode to keep the switching. In the Down Mode, the behavior of the rectifying PMOS by pulling its gate to input voltage instead of to ground. In this way, the voltage drop across the PMOS is increasing as high as to regulate the output voltage. The high side PMOS works under saturation area, thus the effciency is much lower than boost mode. The power loss also increases in this mode, which needs to be taken into account for thermal consideration. Moreover, the current limit decreases as well under down mode, with TPS61299-Q1decreasing by 20%.

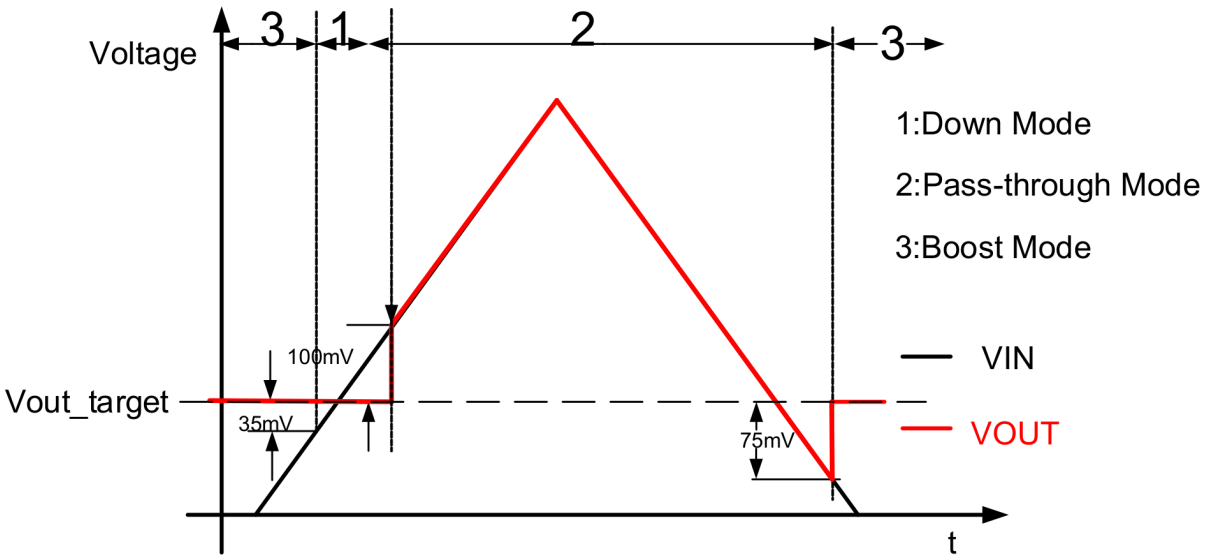
6.3.9 Pass-Through Operation

The TPS61299-Q1 features down mode and pass-through operation when input voltage is close to or higher than output voltage.

During down mode operation, the device regulates the output voltage to the target voltage even when the input voltage is higher than the output voltage. The control circuit changes the behavior of the rectifying P-channel MOSFET by pulling its gate to input voltage instead of to ground. In this way, the voltage drop across the P-channel MOSFET is increasing as high as to regulate the output voltage.

In pass through mode, the TPS61299-Q1 stops switching and turns on the high-side P-channel MOSFET. The output voltage is the input voltage minus the voltage drop across the DCR of the inductor and the on-resistane ($R_{DS(on)}$) of the P-channel MOSFET. During pass though operation, the device disables the input current limit function, reverse current protection, and thermal shutdown.

For TPS61299-Q1, with input voltage ramping up, the device goes into down mode when Vin >Vout-35mV. The device stays in down mode until Vin >Vout+100mV and then goes automatically into pass through operation. In the pass through operation, output voltage follows input voltage. The TPS61299-Q1 exits pass though operation and goes back to boost mode when the output voltage drops below the setting target voltage minus 75mV.



A. Down mode
B. Pass-through mode
C. Boost mode

Figure 6-4. Mode Transition for TPS61299-Q1

6.3.10 Output Short-to-Ground Protection

When the VOUT pin is short to ground and the output voltage describes to less than 0.5V, the TPS61299-Q1 device begins to limit the inductor current, the same with soft-start operation. The TPS61299-Q1 works at the boundary of discontinuous conduction mode (DCM) and continuous conduction mode (CCM) when the input voltage is lower than 1.8V and works at DCM at input voltage is higher than 1.8V.

After the short circuit is released, the TPS61299-Q1 goes through the soft-start sequence again to the regulated output voltage.

6.3.11 Thermal Shutdown

The TPS61299-Q1 goes into thermal shutdown once the junction temperature exceeds 150°C. When the junction temperature drops below the thermal shutdown temperature threshold less the hysteresis, typically 130°C, the device starts operating again.

6.4 Device Functional Modes

6.4.1 Fast Load Transient Mode and Normal Mode

The TPS61299-Q1 has two modes, fast load transient mode and normal mode, which is selected by VSEL pin.

In the fast load transient mode, the loop response speed is fast. Eg the load transient settling time is about 8 us when output current transient from 0A to 200mA at 3.6V to 5V condition. But the trade-off is the load regulation. Normal mode has the better load regulation.

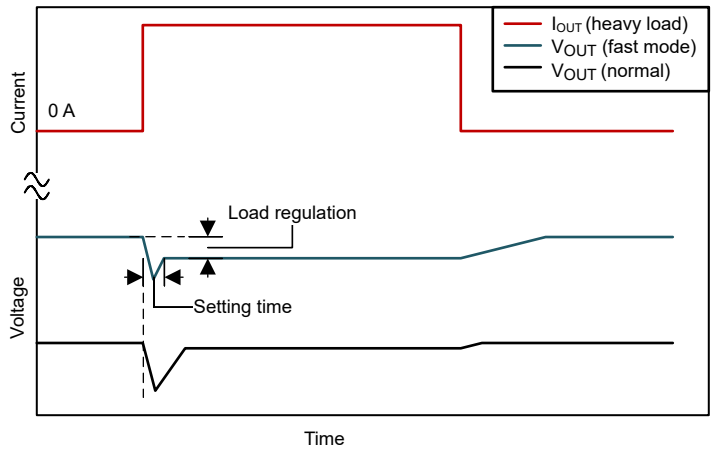


Figure 6-5. Transient Performance Comparison Under Fast Mode and Normal Mode

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS61299-Q1 is a synchronous step-up converter and operates in a hysteretic control scheme. The TPS61299-Q1 has a wide input voltage supply range between 0.5V and 5.5V(0.7V rising voltage for start up). The device only consumes 95nA quiescent current and can achieve up high efficiency under light load condition.

The TPS61299-Q1 provides the input current limit of 1.2A and supports true shutdown function at EN is low.

TPS61299-Q1 provides a fast transient performance mode and accurate load regulation mode for different system.

7.2 Typical Application-Li-ion Battery to 5V Boost Converter Under Fast Mode

The TPS61299-Q1 can operate under fast transient mode with 8μs settling time under 0 to 200mA load step. Set the VSEL according to table 8-1 to select different target VOUT under fast mode.

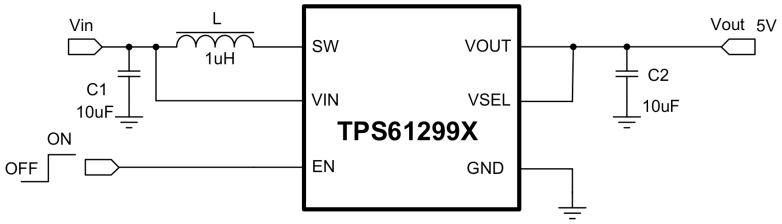


Figure 7-1. 3.6V Input Source to 5V Boost Converter Under Fast Mode

7.2.1 Design Requirements

The design parameters are listed in Table 7-1.

Table 7-1. Design Requirements

PARAMETERS	VALUES
Input Voltage	2.7V ~ 4.3V
Output Voltage	5V (fast mode)
Output Current	500mA
Output Voltage Ripple	± 50mV

7.2.2 Detailed Design Procedure

7.2.2.1 Maximum Output Current

The maximum output capability of the TPS61299-Q1 is determined by the input-to-output ratio and the current limit of the boost converter. The maximum output current can be estimated by Equation 2.

$$I_{OUT\,(max)} = \frac{V_{IN}\,I_{LIM}}{V_{OUT}}\eta \tag{2}$$

where

- η is the conversion efficiency, use 85% for estimation.
- I_{LIM} is the average switch current limit.

Minimum input voltage, maximum boost output voltage, and minimum current limit I_{LIM} are used as the worst case condition for the estimation.

7.2.2.2 Inductor Selection

The TPS61299-Q1 boost converter does not have fixed frequency and it keeps the inductor ripple current constant in the range of 350mA, so the frequency is determined by the inductance and working voltage.

The TPS61299-Q1 is designed to work with inductor value of 1µH.

Table 7-2. Recommended Inductors for the TPS61299-Q1

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (LxWxH)	VENDOR(1)
HTTH16080H-1R0MSR-99	1	110	2.3	1.6 × 0.8 × 0.8	Cyntec
WIP252010P-1R0ML	1	54	3.5	2.5 x 2.0 x 1.0	INPAQ
WPN252010H1R0MT	1	76	3.5	2.5 x 2.0 x 1.0	Sunlord

(1) See the *Third-Party Products* disclaimer

7.2.2.3 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. The ripple voltage is related to capacitor capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple voltage can be calculated by Equation 3.

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}} \quad (3)$$

where

- D_{MAX} is the maximum switching duty cycle.
- V_{RIPPLE} is the peak-to-peak output ripple voltage.
- I_{OUT} is the maximum output current.
- f_{SW} is the switching frequency.

The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used. The output peak-to-peak ripple voltage caused by the ESR of the output capacitors can be calculated by Equation 4.

$$V_{RIPPLE(ESR)} = I_{L(P)} \times R_{ESR} \quad (4)$$

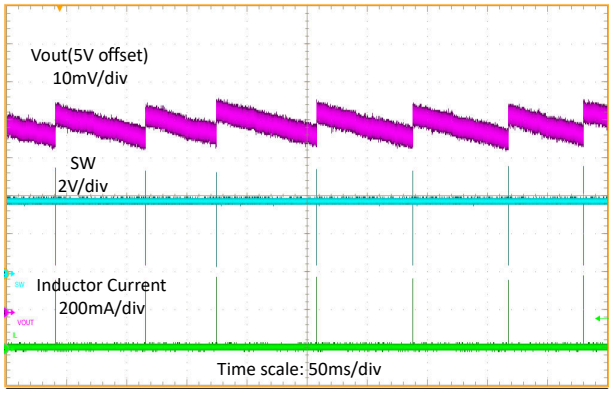
Take care when evaluating the derating of a ceramic capacitor under DC bias voltage, aging, and AC signal. For example, the DC bias voltage can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to make sure there is adequate capacitance at the required output voltage. Increasing the output capacitor makes the output ripple voltage smaller in PWM mode.

TI recommends using the X5R or X7R ceramic output capacitor in the range of 4µF to 1000µF effective capacitance. The output capacitor affects the small signal control loop stability of the boost regulator. Effective output capacitance should be no less than 20uF as soon as output current is higher than 1A. If the output capacitor is below the range, the boost regulator can potentially become unstable.

7.2.2.4 Input Capacitor Selection

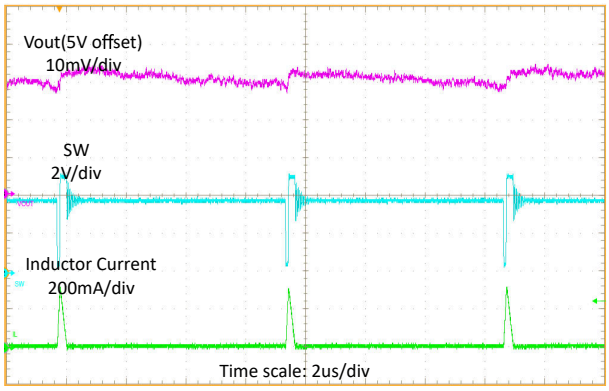
Multilayer X5R or X7R ceramic capacitors are excellent choices for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 10µF input capacitor is sufficient for most applications, larger values can be used to reduce input current ripple without limitations. Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the part. In this circumstance, place additional bulk capacitance (tantalum or aluminum electrolytic capacitor) between ceramic input capacitor and the power source to reduce ringing that can occur between the inductance of the power source leads and ceramic input capacitor.

7.2.3 Application Curves



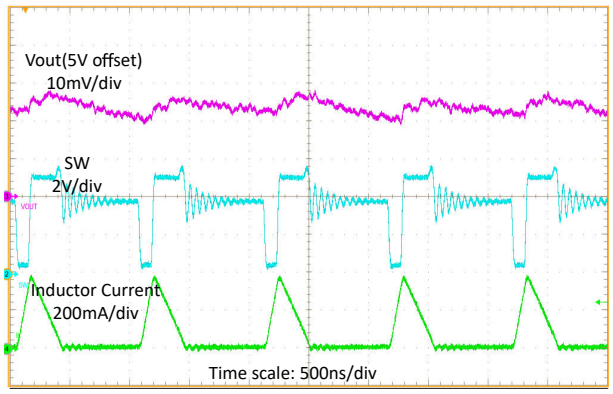
V_{IN} = 3.6V I_{OUT} = 0A

Figure 7-2. Switching Waveform at Open Load



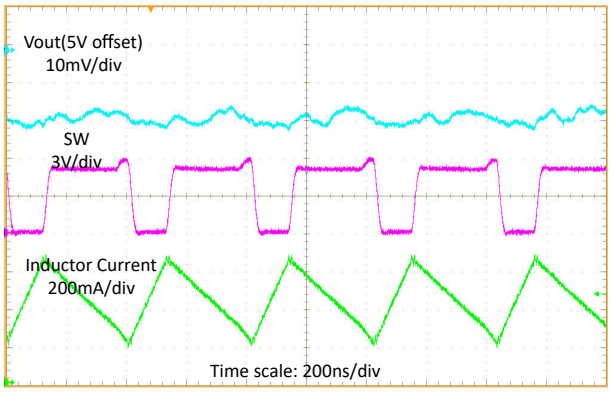
V_{IN} = 3.6V I_{OUT} = 5mA

Figure 7-3. Switching Waveform at Light Load



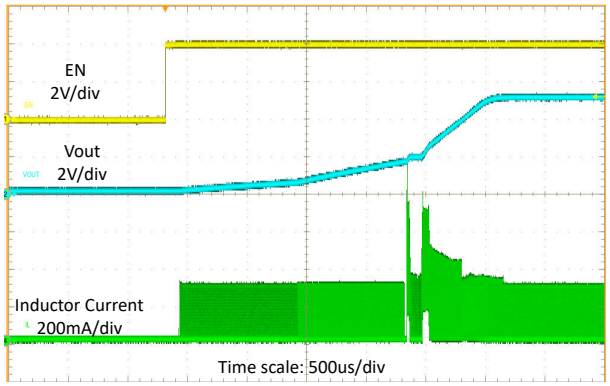
V_{IN} = 3.6V I_{OUT} = 50mA

Figure 7-4. Switching Waveform at Medium Load



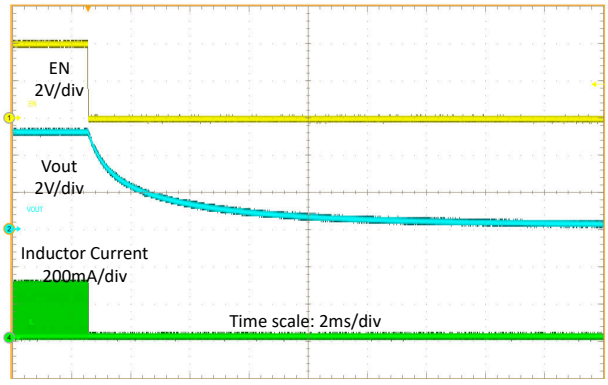
V_{IN} = 3.6V I_{OUT} = 300mA

Figure 7-5. Switching Waveform at Heavy Load



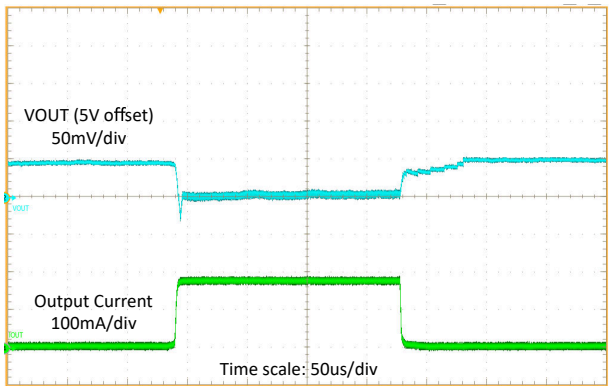
V_{IN} = 3.6V V_{OUT} = 5V | R_{load} = 500Ω

Figure 7-6. Start-Up by EN



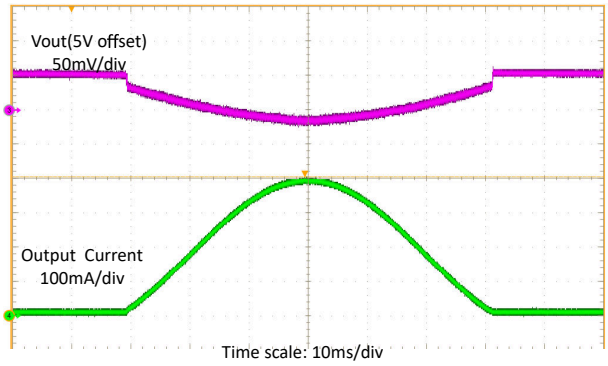
V_{IN} = 3.6V V_{OUT} = 5V | R_{load} = 500Ω

Figure 7-7. Shutdown by EN



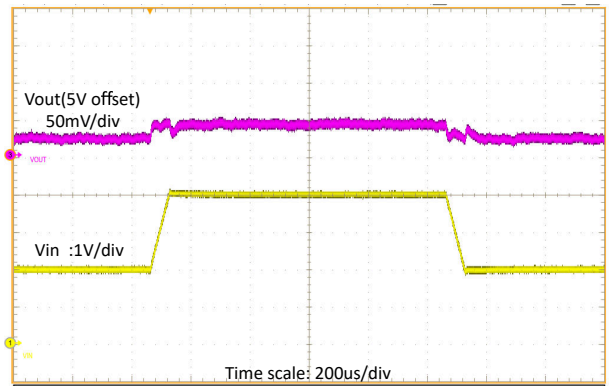
V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 0 to 200mA with 20-µs slew rate

Figure 7-8. Load Transient



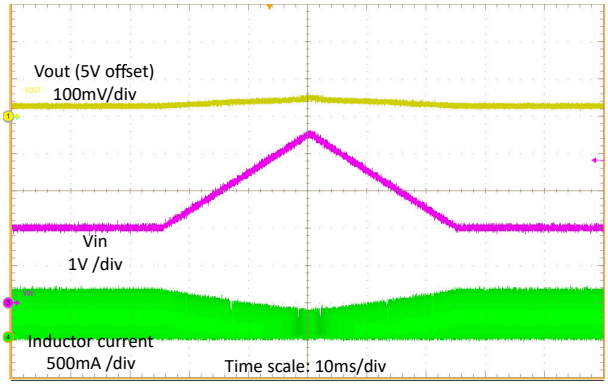
V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 0 to 400mA sweep

Figure 7-9. Load Sweep



V_{IN} = 2V to 4V with 20-us slew rate, V_{OUT} = 5V, R_{load} = 50Ω

Figure 7-10. Line Transient



V_{IN} = 2V to 4.5V Sweep, V_{OUT} = 5V, R_{load} = 25Ω

Figure 7-11. Line Sweep

7.3 Typical Application-Li-ion Battery to 5V Boost Converter Under Normal Mode

The TPS61299-Q1 can also operate under normal mode with slightly slower transient performance than fast mode. Set the VSEL according to table 8-1 to select different target output voltage during fast mode operation. Table 9-3 lists the design parameters.

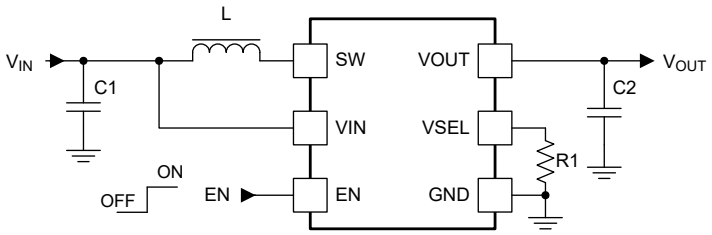


Figure 7-12. 3.6V Input Source to 5V Boost Converter Under Normal Mode

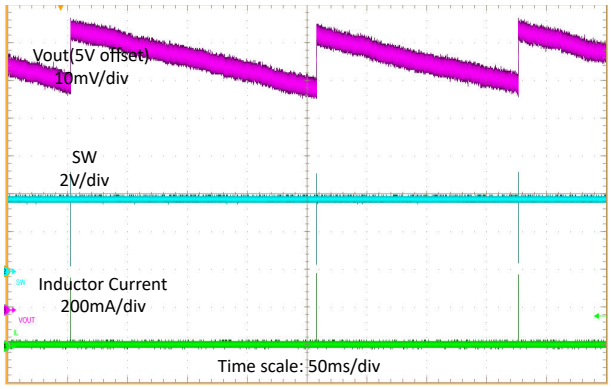
7.3.1 Design Requirements

The design parameters are listed in Table 7-1.

Table 7-3. Design Requirements

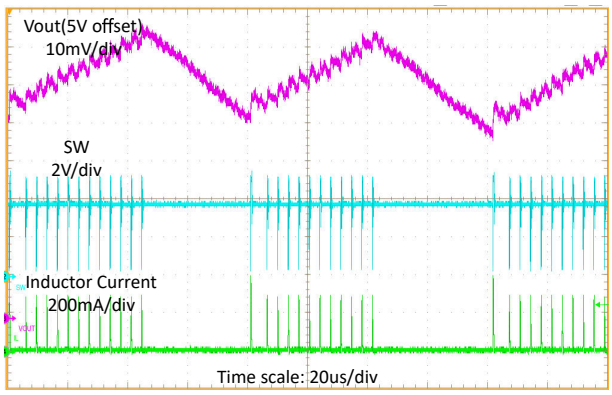
PARAMETERS	VALUES
Input Voltage	2.7V ~ 4.3V
Output Voltage	5V (normal mode)
Output Current	10mA
Output Voltage Ripple	± 50mV

7.3.2 Application Curves



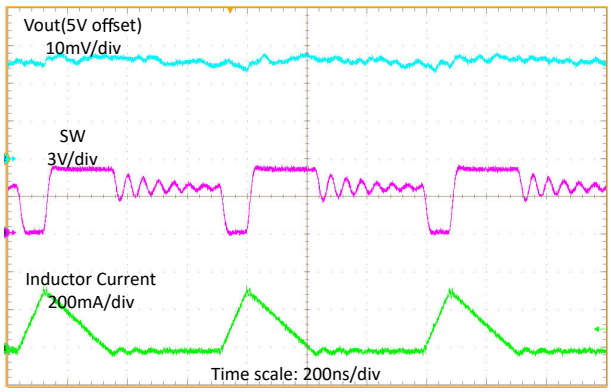
V_{IN} = 3.6V I_{OUT} = 0A

Figure 7-13. Switching Waveform at Open Load



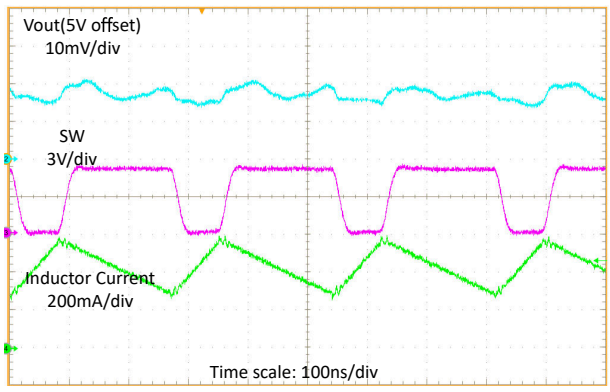
V_{IN} = 3.6V I_{OUT} = 5mA

Figure 7-14. Switching Waveform at Light Load



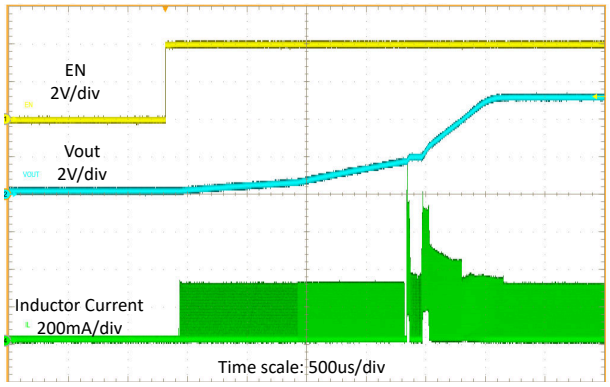
V_{IN} = 3.6V I_{OUT} = 50mA

Figure 7-15. Switching Waveform at Medium Load



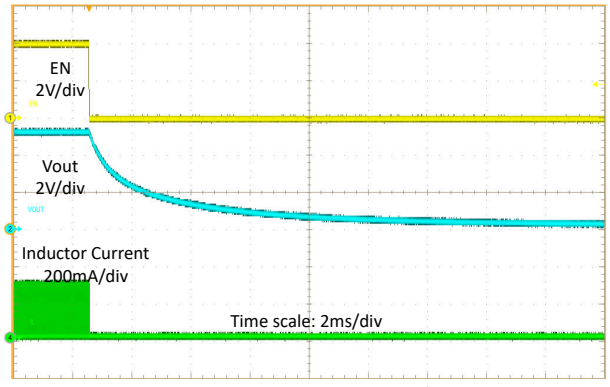
V_{IN} = 3.6V I_{OUT} = 300mA

Figure 7-16. Switching Waveform at Heavy Load



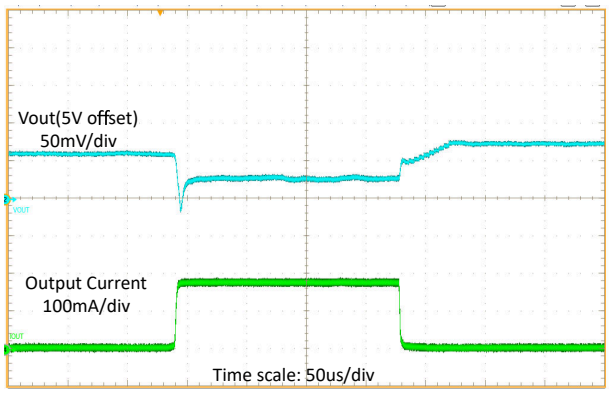
V_{IN} = 3.6V V_{OUT} = 5V | R_{load} = 500Ω

Figure 7-17. Start-Up by EN



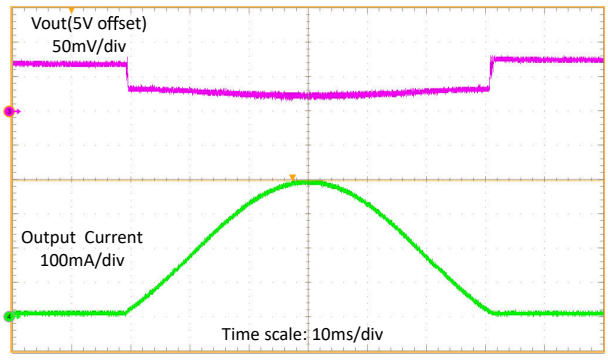
V_{IN} = 3.6V V_{OUT} = 5V | R_{load} = 500Ω

Figure 7-18. Shutdown by EN



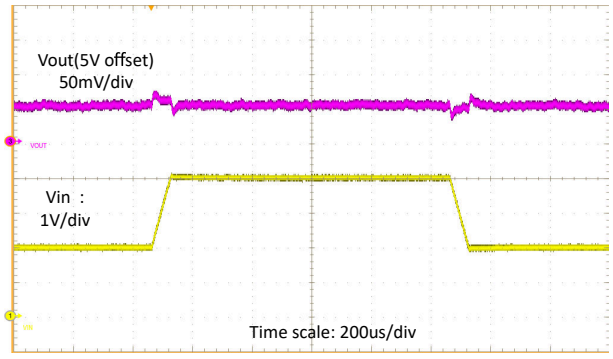
V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 0 to 200mA with 20-µs slew rate

Figure 7-19. Load Transient



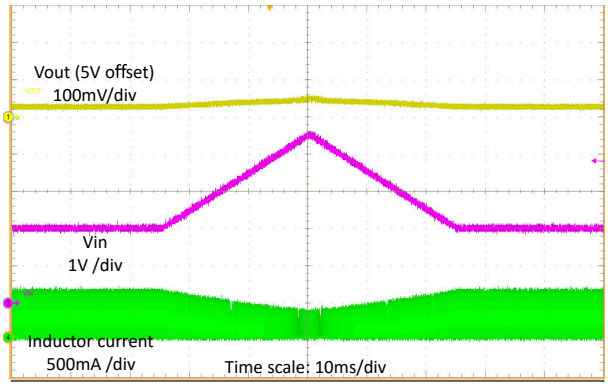
V_{IN} = 3.6V, V_{OUT} = 5V, I_{OUT} = 0 to 400mA sweep

Figure 7-20. Load Sweep



V_{IN} = 2V to 4V with 20-us slew rate, V_{OUT} = 5V, R_{load} = 50Ω

Figure 7-21. Line Transient



V_{IN} = 2V to 4.5V Sweep, V_{OUT} = 5V, R_{load} = 25Ω

Figure 7-22. Line Sweep

7.4 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 0.7V to 5.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is a tantalum or aluminum electrolytic capacitor with a value of 100µF. Output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPS61299-Q1.

7.5 Layout

7.5.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitors , as well as the inductor are placed as close as possible to the device.

7.5.2 Layout Example

The bottom layer is a large GND plane connected by vias.

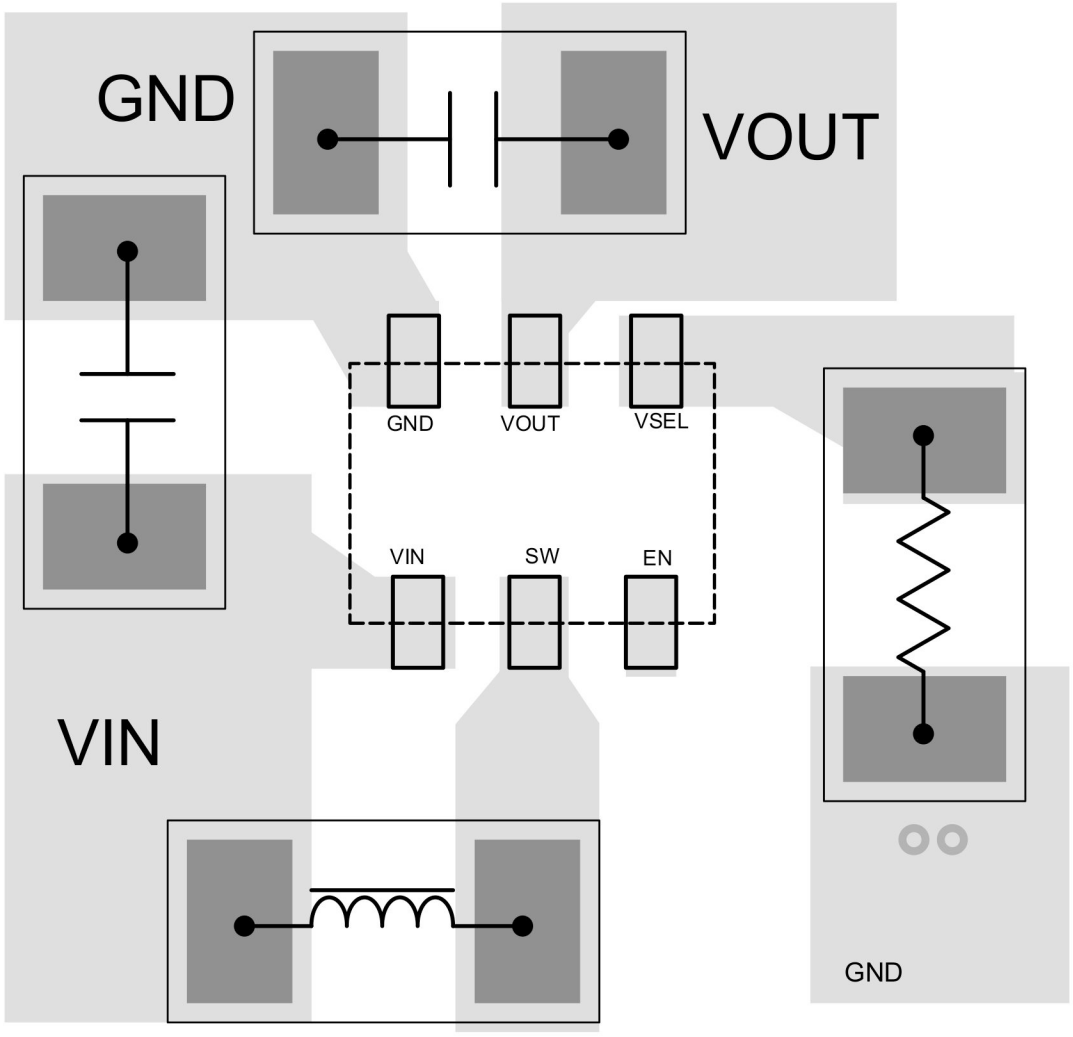


Figure 7-23. Layout Example-DRL

7.5.3 Thermal Information

The maximum junction temperature is restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and maintain the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 5.

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \quad (5)$$

where

- T_A is the maximum ambient temperature for the application
- Θ_{JA} is the junction-to-ambient thermal resistance given in the Thermal Information table.

The TPS61299-Q1 comes in a WCSP or SOT583 package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type and layout. Using thick PCB copper and soldering GND pin to a large ground plate enhances the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Performing Accurate PFM Mode Efficiency Measurements Application Report*
- Texas Instruments, *Accurately Measuring Efficiency of Ultra-low-IQ Devices Technical Brief*
- Texas Instruments, *IQ: What it is, What it isn't, and How to Use it Techanical Brief*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

DATE	REVISION	NOTES
February 2024	*	Initial release

10 Mechanical, Packaging, and Orderable Information

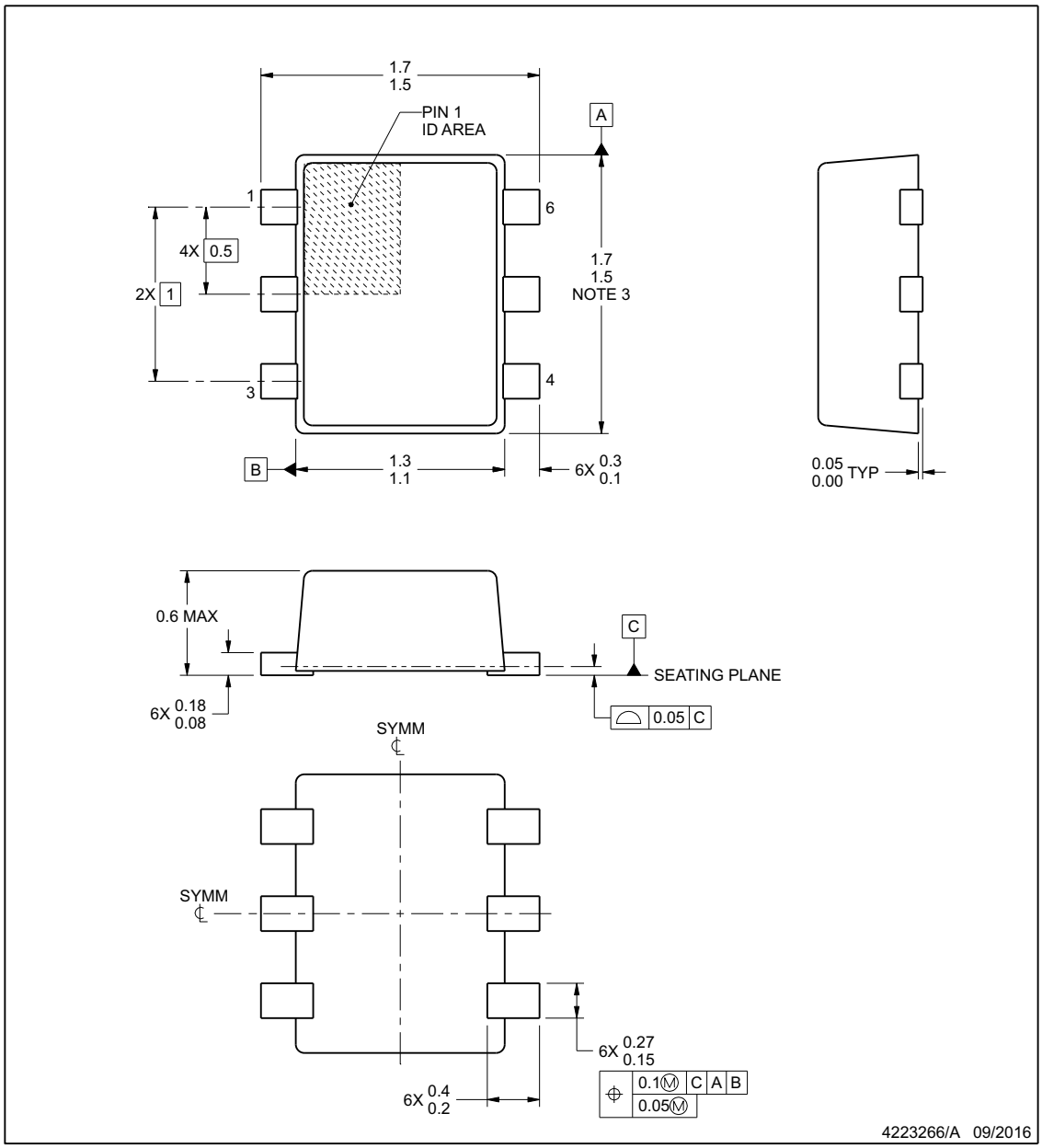
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

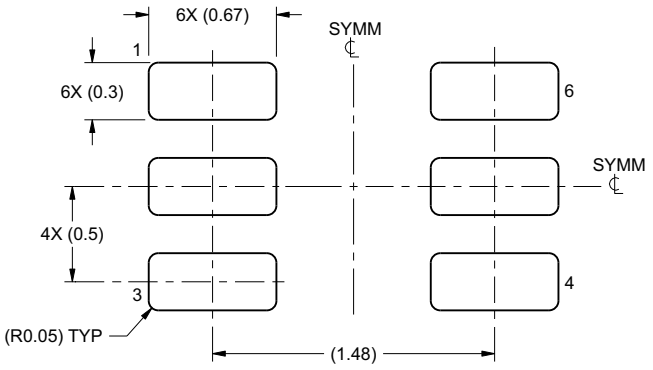
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

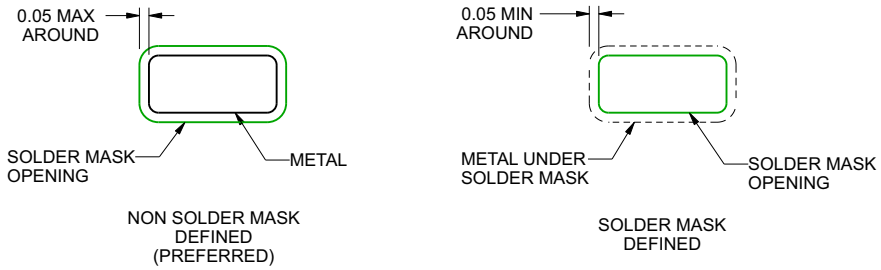
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/A 09/2016

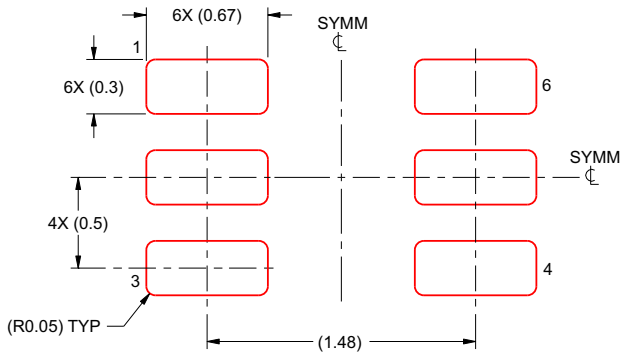
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0006A — **SOT - 0.6 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/A 09/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61299QDRLRQ1	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	299Q
TPS61299QDRLRQ1.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	299Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS61299-Q1 :

- Catalog : TPS61299

NOTE: Qualified Version Definitions:

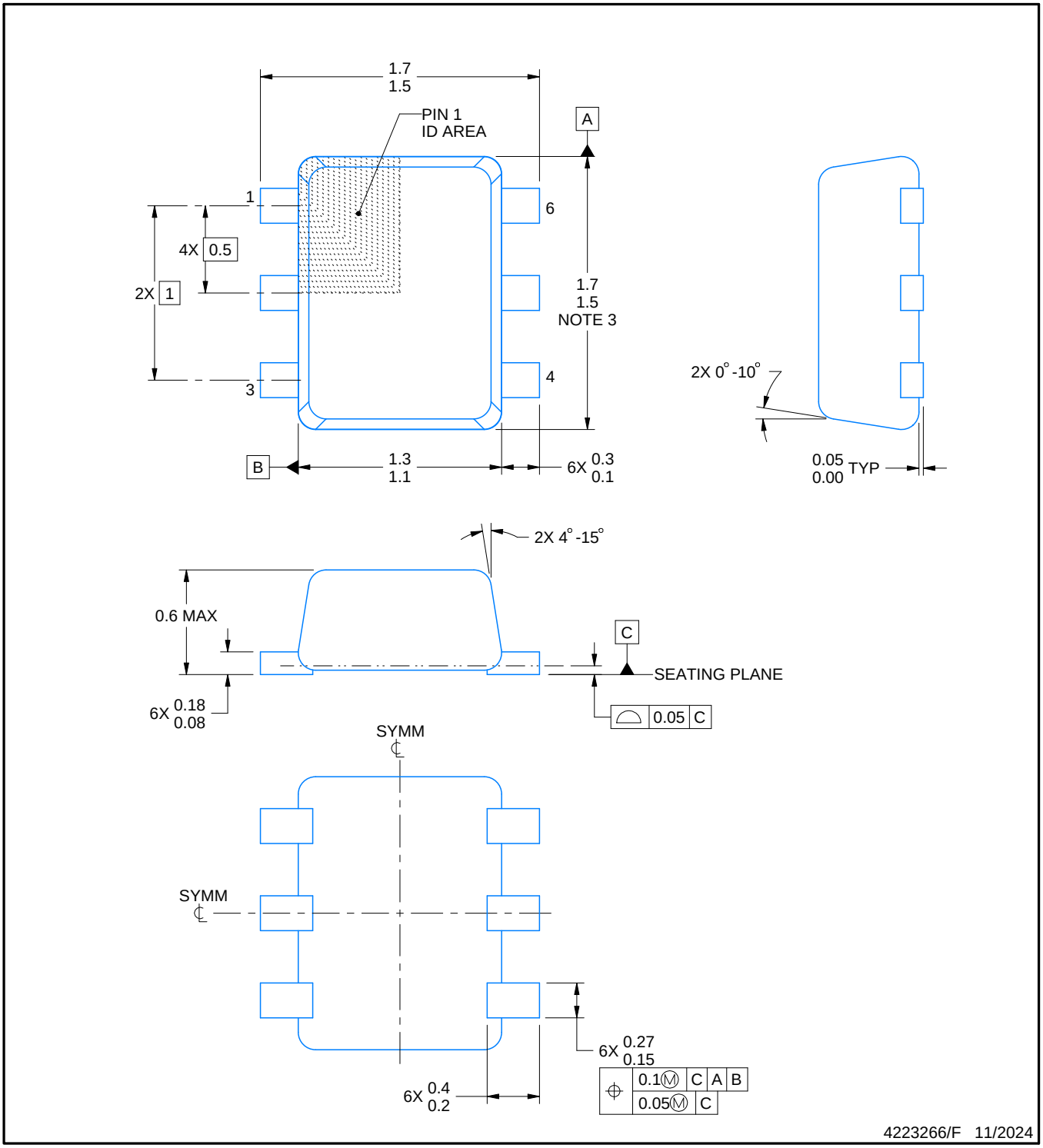
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

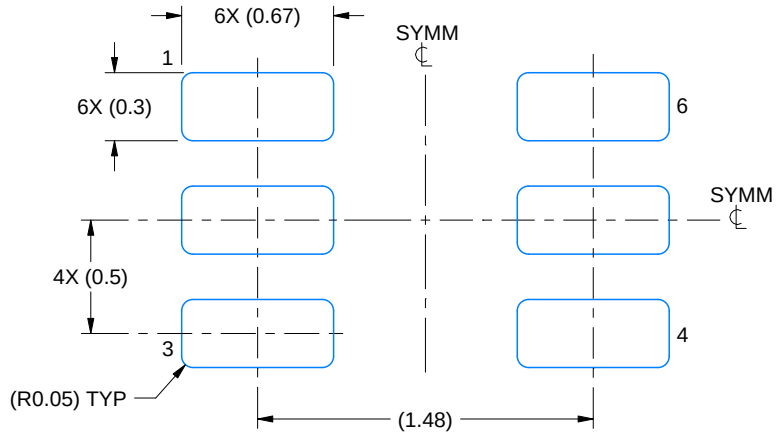
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

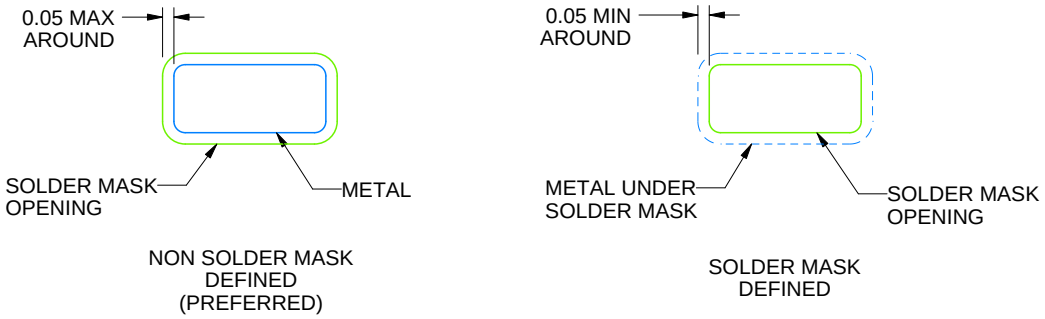
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

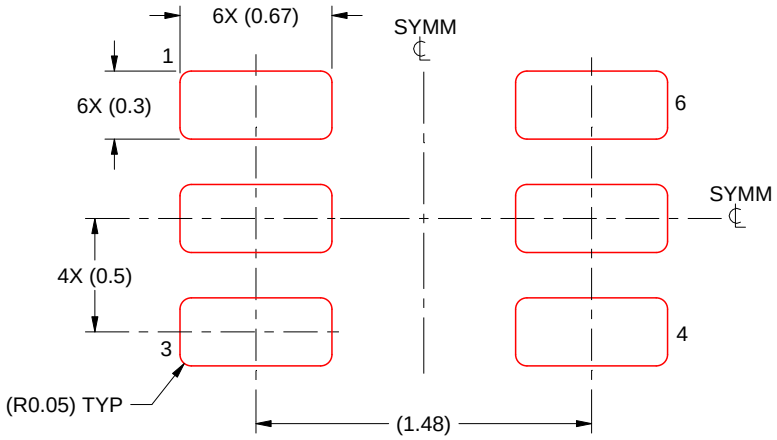
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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