











TPS61161-Q1

SLVSA18A - SEPTEMBER 2009-REVISED JULY 2015

# TPS61161-Q1 White Led Driver with Digital and Pwm Brightness Control for up to 10 **LEDs In Series**

#### **Features**

- **Qualified for Automotive Applications**
- 2.7-V to 18-V Input Voltage Range
- 38-V Open LED Protection for 10 LEDs
- 200-mV Reference Voltage With ±2% Accuracy
- Flexible Digital and PWM Brightness Control
- Built-In Soft Start
- Up to 90% Efficiency
- 2-mm × 2-mm × 0.8-mm 6-pin QFN (DRV) Package With Thermal Pad

## 2 Applications

- **Automotive Cluster Backlighting**
- High-Brightness LED Lighting
- White LED Backlighting Media Form Factor Displays

## 3 Description

With a 40-V rated integrated switch FET, the TPS61161-Q1 is a boost converter that drives up to 10 LEDs in series. The boost converter runs at 600kHz fixed switching frequency to reduce output ripple, improve conversion efficiency, and allow for the use of small external components.

The default white LED current is set with the external sensor resistor Rset, and the feedback voltage is regulated to 200 mV, as shown in the typical application. During the operation, the LED current can be controlled using the 1-wire digital interface (EasyScale<sup>™</sup> protocol) through the CTRL pin. Alternatively, a pulse width modulation (PWM) signal can be applied to the CTRL pin through which the duty cycle determines the feedback reference voltage. In either digital or PWM mode, the TPS61161-Q1 does not burst the LED current; therefore, it does not generate audible noises on the output capacitor. For maximum protection, the device features integrated open LED protection that disables the TPS61161-Q1 to prevent the output from exceeding the absolute maximum ratings during open LED conditions.

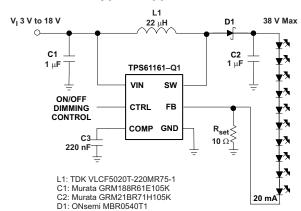
The TPS61161 is available in a space-saving, 2-mm x 2-mm QFN (DRV) package with thermal pad.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61161-Q1	SON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### **Typical Application**





## **Table of Contents**

1	Features 1	8 Applications and Implementation	
2	Applications 1	8.1 Application Information	
3	Description 1	8.2 Typical Application	16
4	Revision History2	9 Power Supply Recommendations	19
5	Pin Configuration and Functions3	10 Layout	20
6	Specifications3	10.1 Layout Guidelines	20
•	6.1 Absolute Maximum Ratings	10.2 Layout Example	20
	6.2 ESD Ratings	10.3 Thermal Considerations	20
	6.3 Recommended Operating Conditions	11 Device and Documentation Support	2 <sup>-</sup>
	6.4 Thermal Information	11.1 Device Support	2
	6.5 Electrical Characteristics 5	11.2 Documentation Support	2 <sup>-</sup>
	6.6 Typical Characteristics	11.3 Community Resources	2 <sup>2</sup>
7	Detailed Description9	11.4 Trademarks	2
•	7.1 Overview	11.5 Electrostatic Discharge Caution	2 <sup>-</sup>
	7.2 Functional Block Diagram9	11.6 Glossary	2 <sup>2</sup>
	7.3 Feature Description	12 Mechanical, Packaging, and Orderable	
	7.4 Device Functional Modes	Information	2 <sup>r</sup>

# 4 Revision History

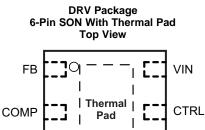
### Changes from Original (September 2009) to Revision A

Page

Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section



# 5 Pin Configuration and Functions



### **Pin Functions**

**GND** 

Р	IN	1/0	DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
COMP	2	0	Output of the transconductance error amplifier. Connect an external capacitor to this pin to compensate the regulator.
CTRL	5	I	Control pin of the boost regulator. It is a multi-functional pin which can be used for enable control, PWM and digital dimming.
FB	1	ı	Feedback pin for current. Connect the sense resistor from FB to GND.
GND	3	0	Ground
SW	4	1	This is the switching node of the IC. Connect the inductor between the VIN and SW pin. This pin is also used to sense the output voltage for open LED protection
VIN	6	I	The input supply pin for the IC. Connect VIN to a supply voltage from 2.7 V to 18 V.
Thermal P	ad	_	The thermal pad should be soldered to the analog ground plane. If possible, use thermal via to connect to ground plane for ideal power dissipation.

# 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Supply voltage on VIN (2)	-0.3	20	V
VI	Voltage on CTRL <sup>(2)</sup>	-0.3	20	V
	Voltage on FB and COMP <sup>(2)</sup>	-0.3	3	V
	Voltage on SW <sup>(2)</sup>	-0.3	40	V
$T_J$	Operating junction temperature range	-40	150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±1000		
	Charged-device model (CDM), per AEC Q100-011	±1000	V	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Product Folder Links: TPS61161-Q1

<sup>(2)</sup> All voltage values are with respect to network ground terminal.



### 6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
$V_{I}$	Input voltage range, VIN				18	V
$V_{O}$	Output voltage range				38	V
L	Inductor <sup>(1)</sup>				22	μH
f <sub>dim</sub>	f <sub>dim</sub> PWM dimming frequency				100	kHz
Dt	DIA/AA dustu aaala saaalasti aa	At 10 kHz	0.5%			
Duty	PWM duty cycle resolution	At 30 kHz	1.5%			
$C_{IN}$	C <sub>IN</sub> Input capacitor					μF
Co	Output capacitor <sup>(1)</sup>				10	μF
T <sub>A</sub>					125	°C

<sup>(1)</sup> These values are recommended values that have been successfully tested in several applications. Other values may be acceptable in other applications but should be fully tested by the user.

### 6.4 Thermal Information

		TPS61161-Q1	
	THERMAL METRIC <sup>(1)</sup>	DRV (SON)	UNIT
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.9	°C/W
ΨЈТ	Junction-to-top characterization parameter	3.2	°C/W
ΨЈВ	Junction-to-board characterization parameter	66.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	40.8	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

Product Folder Links: TPS61161-Q1



## 6.5 Electrical Characteristics

VIN = 3.6 V, CTRL = VIN,  $T_A = -40 ^{\circ}\text{C}$  to 125  $^{\circ}\text{C}$ , typical values are at  $T_A = 25 ^{\circ}\text{C}$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CU	IRRENT					
V <sub>I</sub>	Input voltage range, VIN		2.7		18	V
	Operating quiescent current into VIN	Device PWM switching no load			1.8	mA
I <sub>SD</sub>	Shutdown current	CRTL = GND, VIN = 4.2 V			1	μΑ
UVLO	Undervoltage lockout threshold	VIN falling		2.2	2.5	V
V <sub>hys</sub>	Undervoltage lockout hysteresis	5		70		mV
•	ID REFERENCE CONTROL	1	-			
V <sub>(CTRLh)</sub>	CTRL logic high voltage	VIN = 2.7 V to 18 V	1.2			V
V <sub>(CTRLI)</sub>	CTRL logic low voltage	VIN = 2.7 V to 18 V			0.4	V
R <sub>(CTRL)</sub>	CTRL pulldown resistor		400	800	1600	kΩ
t <sub>off</sub>	CTRL pulse width to shutdown	CTRL high to low	2.5			ms
t <sub>es det</sub>	EasyScale detection time <sup>(1)</sup>	CTRL pin low	260			μs
es_det	EasyScale detection delay	CTAL piir low	100			μs
	EasyScale detection window time	Measured from CTRL high	1			ms
t <sub>es_win</sub> VOI TAGE A	AND CURRENT CONTROL					1110
V <sub>REF</sub>	Voltage feedback regulation voltage		196	200	204	mV
* KEF		V <sub>FB</sub> = 50 mV	47	50	53	1117
$V_{(REF\_PWM)}$	Voltage feedback regulation voltage under brightness control	$V_{FB} = 30 \text{ mV}$	17	20	23	mV
ı	Voltage feedback input bias current	V <sub>FB</sub> = 200 mV	17	20	23	μA
FB	· · · · · · · · · · · · · · · · · · ·	V <sub>FB</sub> = 200 IIIV	500	600	700	kHz
fs	Oscillator frequency	\/ 100 m\/	90%	93%	700	KITZ
D <sub>max</sub>	Maximum duty cycle	V <sub>FB</sub> = 100 mV	90%			
t <sub>min_on</sub>	Minimum on pulse width			40		ns
sink	Comp pin sink current			100		μA
source	Comp pin source current		0.40	100	400	μA
G <sub>ea</sub>	Error amplifier transconductance		240	320	400	µmho
R <sub>ea</sub>	Error amplifier output resistance			6		ΜΩ
f <sub>ea</sub>	Error amplifier crossover frequency	5 pF connected to COMP		500		kHz
POWER SW	ИТСН	T				
R <sub>DS(on)</sub>	N-channel MOSFET on-resistance	VIN = 3.6 V		0.3	0.6	Ω
DO(011)		VIN = 3 V			0.7	
LN_NFET	N-channel leakage current	V <sub>SW</sub> = 35 V, T <sub>A</sub> = 25°C			1	μΑ
OC and OLF						
LIM	N-Channel MOSFET current limit	D = D <sub>max</sub>	0.56	0.7	0.84	Α
LIM_Start	Start-up current limit	D = D <sub>max</sub>		0.4		Α
Half_LIM	Time step for half current limit			5		ms
$V_{ovp}$	Open LED protection threshold		37	38	39	V
$V_{(FB\_OVP)}$	Open LED protection threshold on FB	Measured on the FB pin, percentage of Vref, Vref = 200 mV and 20 mV		50%		
t <sub>REF</sub>	V <sub>REF</sub> filter time constant			180		μs
t <sub>step</sub>	V <sub>REF</sub> ramp up time			213		μs
EasyScale 1	<b>TIMING</b>				"	
t <sub>start</sub>	Start time of program stream		2			μs
EOS	End time of program stream		2		360	μs
t <sub>H_LB</sub>	High time low bit	Logic 0	2		180	μs
$t_L\_LB$	Low time low bit	Logic 0	$2 \times t_{H LB}$		360	μs

<sup>(1)</sup> To select EasyScale mode, the CTRL pin must be low for more than  $t_{\text{es\_det}}$  during  $t_{\text{es\_win}}$ 



### **Electrical Characteristics (continued)**

VIN = 3.6 V, CTRL = VIN,  $T_A = -40$ °C to 125°C, typical values are at  $T_A = 25$ °C (unless otherwise noted)

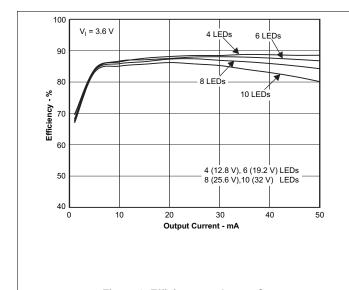
	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
t <sub>L_HB</sub>	Low time high bit	Logic 1	2	180	) µs
V <sub>ACKNL</sub>	Acknowledge output voltage low	Open drain, R <sub>pullup</sub> =15 kΩ to VIN		0.4	V
t <sub>valACKN</sub>	Acknowledge valid time	See (2)		2	μs
t <sub>ACKN</sub>	Duration of acknowledge condition	See (2)		512	2 μs
THERMAL	SHUTDOWN				
T <sub>shutdown</sub>	Thermal shutdown threshold			160	°C
T <sub>hysteresis</sub>	Thermal shutdown threshold hysteresis			15	°C

<sup>(2)</sup> Acknowledge condition active 0, this condition will only be applied in case the RFA bit is set. Open-drain output, line needs to be pulled high by the host with resistor load.

## 6.6 Typical Characteristics

**Table 1. Table of Graphs** 

		FIGURE
Efficiency TPS61161-Q1	VIN = 3.6 V; 4, 6, 8, 10 LEDs; L = 22 μH	Figure 1
Efficiency TPS61161-Q1		Figure 2
Current limit	T <sub>A</sub> = 25°C	Figure 3
Current limit		Figure 4
EasyScale step		Figure 5
PWM dimming linearity	VIN = 3.6 V; PWM Freq = 10 kHz and 40 kHz	Figure 5
Output ripple at PWM dimming	8 LEDs; VIN = 3.6 V; I <sub>LOAD</sub> = 20 mA; PWM Freq = 10 kHz	Figure 7
Switching waveform	8 LEDs; VIN = 3.6 V; $I_{LOAD}$ = 20 mA; L = 22 $\mu$ H	Figure 8
Start-up	8 LEDs; VIN = 3.6 V; I <sub>LOAD</sub> = 20 mA; L =22 μH	Figure 9
Open LED protection	8 LEDs; VIN = 3.6 V; $I_{LOAD}$ = 20 mA; L = 22 $\mu$ H	Figure 10



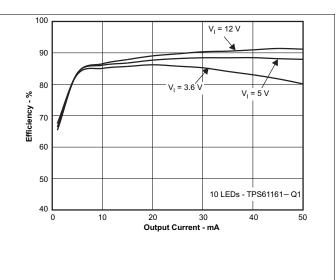


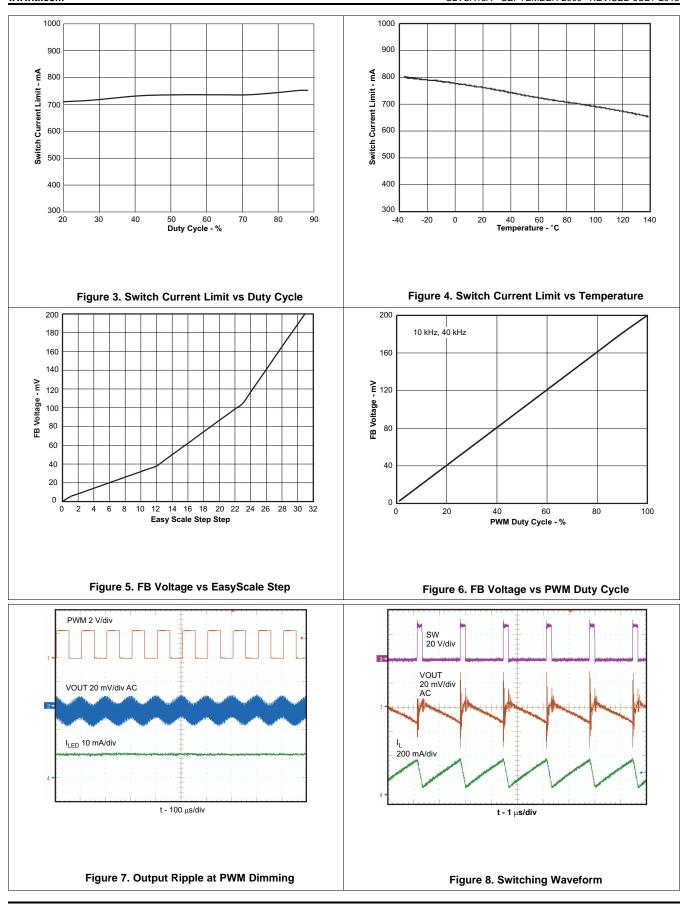
Figure 1. Efficiency vs Output Current

Figure 2. Efficiency vs Output Current

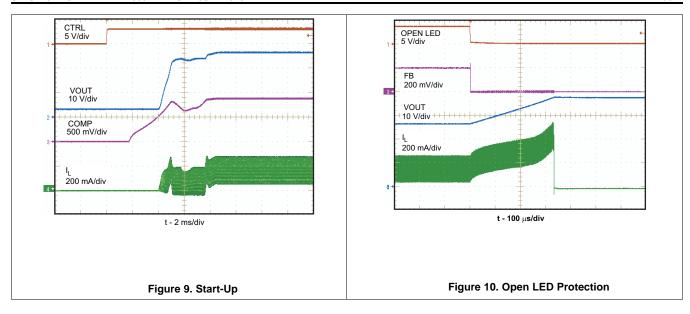
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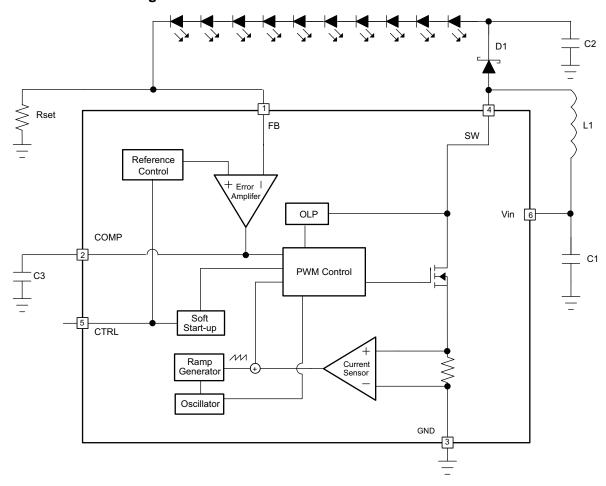


## 7 Detailed Description

#### 7.1 Overview

The TPS61161-Q1 is a high-efficiency, high-output voltage boost converter in small package size, The device is ideal for driving up to 10 white LED in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. The device integrates 40-V/0.7-A switch FET and operates in pulse width modulation (PWM) with 600kHz fixed switching frequency. For operation see the block diagram. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The control architecture is based on traditional current-mode control; therefore, a slope compensation is added to the current signal to allow stable operation for duty cycles larger than 50%. The feedback loop regulates the FB pin to a low reference voltage (200mV typical), reducing the power dissipation in the current sense resistor.

#### 7.2 Functional Block Diagram



#### 7.3 Feature Description

## 7.3.1 Soft Start-Up

Soft-start circuitry is integrated into the IC to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage in 32 steps, each step takes 213 µs. This ensures that the output voltage rises slowly to reduce the input current. Additionally, for the first 5 ms after the COMP voltage ramps, the current limit of the switch is set to half of the normal current limit spec. During this period, the input current is kept below 400 mA (typical). See the start-up waveform of a typical example, Figure 9.



### **Feature Description (continued)**

#### 7.3.2 Open LED Protection

Open LED protection circuitry prevents IC damage as the result of white LED disconnection. The TPS61161-Q1 monitors the voltage at the SW pin and FB pin during each switching cycle. The circuitry turns off the switch FET and shuts down the IC as soon as the SW voltage exceeds the Vovp threshold and the FB voltage is less than half of regulation voltage for 8 clock cycles. As a result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by toggling the CTRL pin logic. To allow the use of inexpensive low-voltage output capacitor, the TPS61161-Q1 has different open lamp protection thresholds to prevent the internal 40V FET from breaking down. The threshold is set at 38 V. The devices can be selected according to the number of external LEDs and their maximum forward voltage.

#### 7.3.3 Shutdown

The TPS61161-Q1 enters shutdown mode when the CTRL voltage is logic low for more than 2.5 ms. During shutdown, the input supply current for the device is less than 1  $\mu$ A (max). Although the internal FET does not switch in shutdown, there is still a dc current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown. However, in the typical application with two or more LEDs, the forward voltage is large enough to reverse bias the Schottky and keep leakage current low.

#### 7.3.4 Undervoltage Lockout

An undervoltage lockout prevents operation of the device at input voltages less than typical 2.2 V. When the input voltage is below the undervoltage threshold, the device is shutdown and the internal switch FET is turned off. If the input voltage rises by undervoltage lockout hysteresis, the IC restarts.

#### 7.3.5 Thermal Shutdown

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

### 7.4 Device Functional Modes

### 7.4.1 LED Brightness Dimming Mode Selection

The CTRL pin is used for the control input for both dimming modes, PWM dimming and 1 wire dimming. The dimming mode for the TPS61161-Q1 is selected each time the device is enabled. The default dimming mode is PWM dimming. To enter the 1 wire mode, the following digital pattern on the CTRL pin must be recognized by the IC every time the IC starts from the shutdown mode.

- 1. Pull CTRL pin high to enable the TPS61161-Q1, and to start the 1 wire detection window.
- 2. After the EasyScale detection delay ( $t_{es\_delay}$ , 100  $\mu$ s) expires, drive CTRL low for more than the EasyScale detection time ( $t_{es\_detect}$ , 260  $\mu$ s).
- 3. The CTRL pin must be low for more than EasyScale detection time before the EasyScale detection window (t<sub>es\_win</sub>, 1 ms) expires. EasyScale detection window starts from the first CTRL pin low to high transition.

The IC immediately enters the 1-wire mode once these three conditions are met. The EasyScale communication can start before the detection window expires. Once the dimming mode is programmed, it can not be changed without another start-up. This means the IC needs to be shutdown by pulling the CTRL low for 2.5 ms and restarts. See the *Dimming Mode Detection and Soft Start* (Figure 11) for a graphical explanation.

Product Folder Links: TPS61161-Q1



### **Device Functional Modes (continued)**

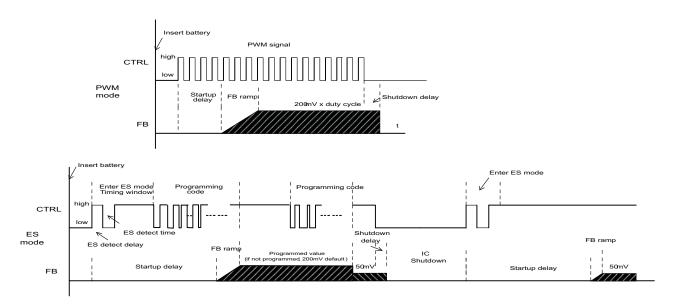


Figure 11. Dimming Mode Detection and Soft Start PWM Brightness Dimming

### 7.4.2 PWM Brightness Dimming

When the CTRL pin is constantly high, the FB voltage is regulated to 200 mV typically. However, the CTRL pin allows a PWM signal to reduce this regulation voltage; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and FB voltage is given by Equation 1.

$$V_{FR} = Duty \times 200 \text{ mV}$$

where

Duty = duty cycle of the PWM signal
 200 mV = internal reference voltage

regulation voltage is independent of the PWM logic voltage level which often has large variations.

As shown in Figure 12, the IC chops up the internal 200-mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED dc current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other scheme which filters the PWM signal for analog dimming, TPS61161-Q1

For optimum performance, use the PWM dimming frequency in the range of 5 kHz to 100 kHz. The requirement of minimum dimming frequency comes from the EasyScale detection delay and detection time specification in the dimming mode selection. Because the CTRL pin is logic only pin, adding external RC filter applied to the pin does not work.

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### **Device Functional Modes (continued)**

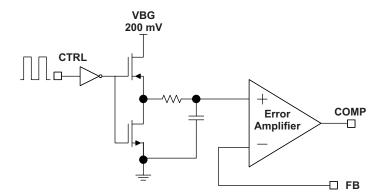


Figure 12. Block Diagram of Programmable FB Voltage Using PWM Signal

### 7.4.3 Digital 1 Wire Brightness Dimming

The CTRL pin features a simple digital interface to allow digital brightness control. The digital dimming can save the processor power and battery life as it does not require a PWM signal all the time, and the processor can enter idle mode if available.

The TPS61161-Q1 adopts the EasyScale protocol for the digital dimming, which can program the FB voltage to any of the 32 steps with single command. The step increment increases with the voltage to produce pseudo logarithmic curve for the brightness step. See the Table 2 for the FB pin voltage steps. The default step is full scale when the device is first enabled ( $V_{FB} = 200 \text{ mV}$ ). The programmed reference voltage is stored in an internal register. A power reset clears the register value and reset it to default.

## 7.4.4 EasyScale: 1-Wire Digital Dimming

EasyScale is a simple but flexible one-pin interface to configure the FB voltage. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor. Figure 13 and Table 3 give an overview of the protocol. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 72 hex. The data byte consists of five bits for information, two address bits, and the RFA bit. The RFA bit set to high indicates the *Request for Acknowledge* condition. The Acknowledge condition is only applied if the protocol was received correctly. The advantage of EasyScale compared with other on pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates from 1.7 kbit/s and up to 160 kbit/s.



Table 2. Selectable FB Voltage

	Table 2. Gelectable . B Tellage					
	FB voltage (mV)	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	5	0	0	0	0	1
2	8	0	0	0	1	0
3	11	0	0	0	1	1
4	14	0	0	1	0	0
5	17	0	0	1	0	1
6	20	0	0	1	1	0
7	23	0	0	1	1	1
8	26	0	1	0	0	0
9	29	0	1	0	0	1
10	32	0	1	0	1	0
11	35	0	1	0	1	1
12	38	0	1	1	0	0
13	44	0	1	1	0	1
14	50	0	1	1	1	0
15	56	0	1	1	1	1
16	62	1	0	0	0	0
17	68	1	0	0	0	1
18	74	1	0	0	1	0
19	80	1	0	0	1	1
20	86	1	0	1	0	0
21	92	1	0	1	0	1
22	98	1	0	1	1	0
23	104	1	0	1	1	1
24	116	1	1	0	0	0
25	128	1	1	0	0	1
26	140	1	1	0	1	0
27	152	1	1	0	1	1
28	164	1	1	1	0	0
29	176	1	1	1	0	1
30	188	1	1	1	1	0
31	200	1	1	1	1	1
-	+					

DATA IN

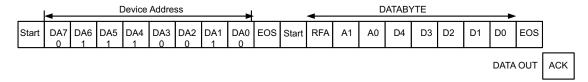


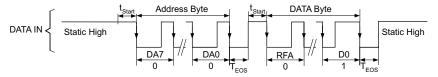
Figure 13. EasyScale Protocol Overview



### Table 3. EasyScale Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
	7	DA7		0 MSB device address
	6	DA6		1
Device	5	DA5	IN	1
Address	4	DA4		1
Byte 72 hex	3	DA3	IIN	0
	2	DA2		0
	1	DA1		1
	0	DA0		0 LSB device address
	7 (MSB)	RFA		Request for acknowledge. If high, acknowledge is applied by device
	6	A1		0 Address bit 1
	5	A0		0 Address bit 0
Data byte	4	D4	IN	Data bit 4
Data byte	3	D3	IIN	Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0
		ACK	OUT	Acknowledge condition active 0, this condition will only be applied in case RFA bit is set. Open-drain output, Line needs to be pulled high by the host with a pullup resistor. This feature can only be used if the master has an open-drain output stage. In case of a push pull output stage Acknowledge condition may not be requested!

### Easy Scale Timing, without acknowledge RFA = 0



### Easy Scale Timing, with acknowledge RFA = 1

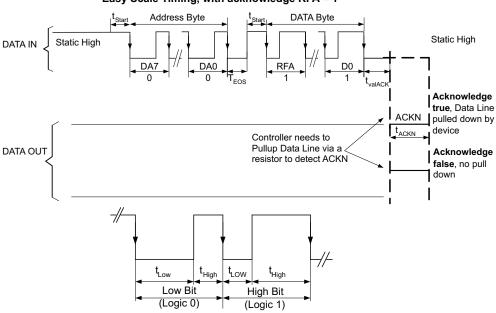


Figure 14. EasyScale™— Bit Coding

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All bits are transmitted MSB first and LSB last. Figure 14 shows the protocol without acknowledge request (Bit RFA = 0), Figure 14 with acknowledge (Bit RFA = 1) request. Before both bytes, device address byte and data byte, a start condition must be applied. For this, the CTRL pin must be pulled high for at least  $t_{start}$  (2  $\mu$ s) before the bit transmission starts with the falling edge. If the CTRL pin is already at high level, no start condition is needed before the device address byte. The transmission of each byte is closed with an End of Stream condition for at least  $t_{EOS}$  (2  $\mu$ s).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between  $t_{LOW}$  and  $t_{HIGH}$ . It can be simplified to:

High Bit:  $t_{HIGH} > t_{LOW}$ , but with  $t_{HIGH}$  at least 2x  $t_{LOW}$ , see Figure 14. Low Bit:  $t_{HIGH} < t_{LOW}$ , but with  $t_{LOW}$  at least 2x  $t_{HIGH}$ , see Figure 14.

The bit detection starts with a falling edge on the CTRL pin and ends with the next falling edge. Depending on the relation between  $t_{HIGH}$  and  $t_{LOW}$ , the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by a set RFA bit.
- The transmitted device address matches with the device address of the device.
- 16 bits is received correctly.

If the device turns on the internal ACKN-MOSFET and pulls the CTRL pin low for the time  $t_{ACKN}$ , which is 512 µs maximum then the Acknowledge condition is valid after an internal delay time  $t_{valACK}$ . This means that the internal ACKN-MOSFET is turned on after  $t_{valACK}$ , when the last falling edge of the protocol was detected. The master controller keeps the line low in this period. The master device can detect the acknowledge condition with its input by releasing the CTRL pin after  $t_{valACK}$  and read back a logic 0. The CTRL pin can be used again after the acknowledge condition ends.

The acknowledge condition may only be requested in case the master device has an open-drain output. For a push-pull output stage, TI recommends using a series resistor in the CRTL line to limit the current to 500 μA for such cases as:

- · an accidentally requested acknowledge
- to protect the internal ACKN-MOSFET



## 8 Applications and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

In the application, TPS61161-Q1 drives 10 LEDs, the output current is set at 20mA, the circuit can support wide range input voltage from 3 V to 18 V. By applying PWM signal on CTRL pin, the circuit can realize PWM dimming control.

### 8.2 Typical Application

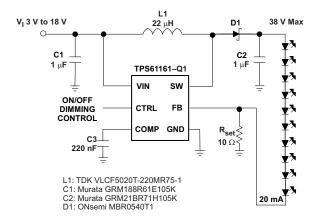


Figure 15. LED Drivers With 10 White LEDs Schematic

#### 8.2.1 Design Requirements

Table 4 lists the input parameters for this design example.

**Table 4. Design Parameters** 

PARAMETER	EXAMPLE VALUE				
Brightness control	PWM Dimming				
Input voltage	3 V to 18 V				
Output current	20 mA				
LED loads	10 LEDs				

#### 8.2.2 Detailed Design Procedure

## 8.2.2.1 Current Program

The FB voltage is regulated by a low 0.2-V reference voltage. The LED current is programmed externally using a current-sense resistor in series with the LED string. The value of the RSET is calculated using Equation 2:

$$I_{LED} = \frac{V_{FB}}{R_{SFT}}$$

where

- I<sub>LED</sub> = output current of LEDs
- V<sub>FB</sub> = regulated voltage of FB
- R<sub>SET</sub> = current sense resistor

(2)



The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.

### 8.2.2.2 Maximum Output Current

The overcurrent limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current; therefore, the ripple must be subtracted to derive maximum dc current. The ripple current is a function of switching frequency, inductor value and duty cycle. The following equations take into account of all of the previous factors for maximum output current calculation.

$$I_{P} = \frac{1}{\left\lceil L \times F_{S} \times \left( \frac{1}{V_{OUT} + V_{F} + V_{IN}} + \frac{1}{V_{IN}} \right) \right\rceil}$$

where

- I<sub>P</sub> = inductor peak to peak ripple
- L = inductor value
- V<sub>F</sub> = Schottky diode forward voltage
- F<sub>S</sub> = switching frequency
- V<sub>OUT</sub> = output voltage of the boost converter. It is equal to the sum of VFB and the voltage drop across LEDs.

$$I_{OUT\_MAX} = \frac{V_{IN} \times \left(I_{LIM} - \frac{I_P}{2}\right) \times \eta}{V_{OUT}}$$

where

- $I_{OLIT\ MAX}$  = maximum output current of the boost converter
- I<sub>IIM</sub> = overcurrent limit

• 
$$\eta = \text{efficiency}$$
 (4)

For instance, when VIN is 3 V, 8 LEDs output equivalent to VOUT of 26 V, the inductor is 22 µH, the Schottky forward voltage is 0.2 V; and then the maximum output current is 65 mA in typical condition. When VIN is 5 V, 10 LEDs output equivalent to VOUT of 32 V, the inductor is 22 µH, the Schottky forward voltage is 0.2 V; and then the maximum output current is 85 mA in typical condition.

#### 8.2.2.3 Inductor Selection

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, dc resistance and saturation current. Considering inductor value alone is not enough.

The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating, according to half of the peak-to-peak ripple current given by Equation 3, pause the inductor dc current given by:

$$I_{IN\_DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$
(5)

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0-A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, TI recommends a 10-µH to 22-µH inductor value range. A 22-µH inductor optimized the efficiency for most application while maintaining low inductor peak to peak ripple. Table 5 lists the recommended inductor for the TPS61161-Q1. When recommending inductor value, the factory has considered -40% and 20% tolerance from its nominal value.

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TPS61161-Q1 has built-in slope compensation to avoid sub-harmonic oscillation associated with current mode control. If the inductor value is lower than 10  $\mu$ H, the slope compensation may not be adequate, and the loop can be unstable. Therefore, customers must verify the inductor in their application if it is different from the recommended values.

Table 5. Recommended Inductors for TPS61161-Q1

PART NUMBER	L (µH)	DCR MAX (Ω)	SATURATION CURRENT (mA)	SIZE (L × W × H mm)	VENDOR
LQH3NPN100NM0	10	0.3	750	3×3×1.5	Murata
VLCF5020T-220MR75-1	22	0.4	750	5×5×2	TDK
CDH3809/SLD	10	0.3	570	4×4×1	Sumida
A997AS-220M	22	0.4	510	4×4×1.8	TOKO

### 8.2.2.4 Schottky Diode Selection

The high switching frequency of the TPS61161-Q1 demands a high-speed rectification for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED protection voltage. The ONSemi MBR0540 and the ZETEX ZHCS400 are recommended for TPS61161-Q1.

### 8.2.2.5 Compensation Capacitor Selection

The compensation capacitor C3 (see the block diagram), connected from COMP pin to GND, is used to stabilize the feedback loop of the TPS61161-Q1. Use a 220-nF ceramic capacitor for C3.

### 8.2.2.6 Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by

$$C_{OUT} = \frac{(V_{OUT} - V_{IN})I_{OUT}}{V_{OUT} \times F_S \times V_{RIPPLE}}$$

where

The additional output ripple component caused by ESR is calculated using:

$$V_{RIPPLE\_ESR} = I_{OUT} \times R_{ESR}$$
 (7)

Due to its low ESR, Vripple\_ESR can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Take care when evaluating a ceramic capacitor's derating under dc bias, aging, and ac signal. For example, larger form factor capacitors (in 1206 size) have a resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The dc bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance at the required output voltage.

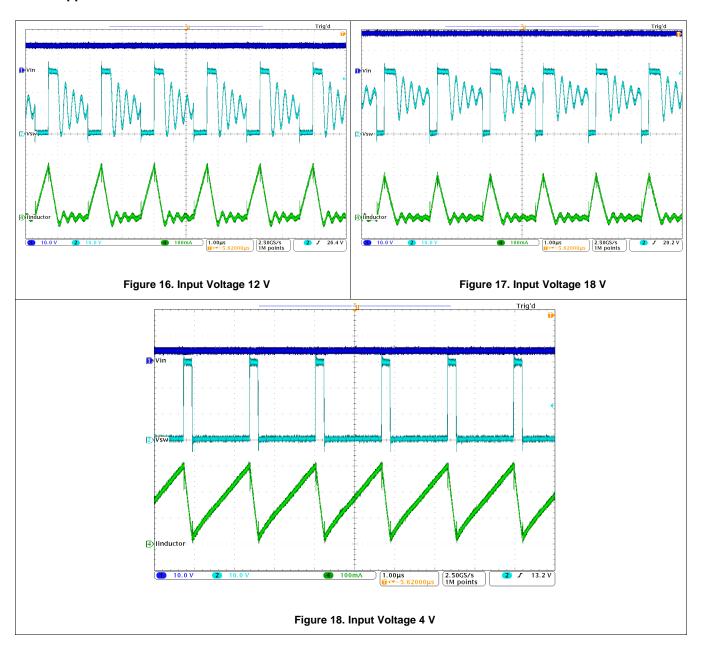
TI recommends the capacitor in the range of 1  $\mu$ F to 4.7  $\mu$ F for input side. The output requires a capacitor in the range of 0.47  $\mu$ F to 10  $\mu$ F. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. For example, if use the output capacitor of 0.1  $\mu$ F, a 470 nF compensation capacitor must be used for the loop stable.

The popular vendors for high value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)
Murata (http://www.murata.com/cap/index.html)



### 8.2.3 Application Curves



# 9 Power Supply Recommendations

The TPS61161-Q1 device requires a single supply input voltage. This voltage can range from 3 V to 18 V and be able to supply enough current for a given application.



## 10 Layout

### 10.1 Layout Guidelines

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To reduce switching losses, the SW pin rise and fall times are made as short as possible. To prevent radiation of high frequency resonance problems, proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling. The loop including the PWM switch, Schottky diode, and output capacitor, contains high current rising and falling in nanosecond and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin to reduce the IC supply ripple. Figure 19 shows a sample layout.

#### 10.2 Layout Example

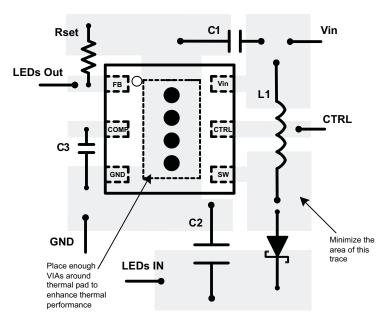


Figure 19. TPS61161-Q1 Layout Example

#### 10.3 Thermal Considerations

The maximum IC junction temperature should be restricted to  $125^{\circ}$ C under normal operating conditions. This restriction limits the power dissipation of the TPS61161-Q1. Calculate the maximum allowable dissipation,  $P_{D(max)}$ , and keep the actual dissipation less than or equal to  $P_{D(max)}$ . The maximum-power-dissipation limit is determined using Equation 8:

$$P_{D(max)} = \frac{125^{\circ}C - T_{A}}{R_{\theta,JA}}$$

where

T<sub>A</sub> is the maximum ambient temperature for the application.

R<sub>BJA</sub> is the thermal resistance junction-to-ambient given in *Thermal Information*.

The TPS61161-Q1 comes in a thermally enhanced SON package. This package includes a thermal pad that improves the thermal capabilities of the package. The  $R_{\theta JA}$  of the SON package greatly depends on the PCB layout and thermal pad connection. The thermal pad must be soldered to the analog ground on the PCB. Using thermal vias underneath the thermal pad as illustrated in the layout example. Also see the *QFN/SON PCB* 

Attachment application report (SLUA271).

Product Folder Links: TPS61161-Q1

(8)



## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Third-Party Products Disclaimer

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### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- How to Use Analog Dimming With the TPS6116x, SLVA471
- Design Tool for Analog Dimming Using a PWM Signal, SLVC336
- QFN/SON PCB Attachment, SLUA271

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.4 Trademarks

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#### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Product Folder Links: *TPS61161-Q1* 

10-Nov-2025 www.ti.com

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
TPS61161QDRVRQ1	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PSJQ
TPS61161QDRVRQ1.B	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PSJQ

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF TPS61161-Q1:

Catalog: TPS61161

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

www.ti.com 10-Nov-2025

NOTE: Qualified Version Definitions:

 $_{\bullet}$  Catalog - TI's standard catalog product

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 19-Jul-2025

### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61161QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 19-Jul-2025



### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
TPS61161QDRVRQ1	WSON	DRV	6	3000	213.0	191.0	35.0	



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4206925/F





PLASTIC SMALL OUTLINE - NO LEAD



### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
- number SLUA271 (www.ti.com/lit/slua271).

  5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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