TPS542A52 4-V to 18-V Input, 15-A, Synchronous Buck Converter With Differential Remote Sense

1 Features

- Integrated 9.1-mΩ and 2.6-mΩ MOSFETs support up to 15-A output current
- 0.5-V to 5.5-V output voltage range
- Fixed-frequency voltage control mode with selectable internal compensation
- Seven selectable frequency settings from 400 kHz to 2.2 MHz
- Synchronizes to an external clock
- Fully differential remote sense
- Six selectable over-current limits, four soft-start slew rates
- Monotonic start-up into pre-biased outputs
- EN pin allowing for adjustable input UVLO
- Power good indicator
- 17-µA typical shutdown quiescent current draw
- Selectable FCCM or PFM for light load efficiency
- –40 to +150°C operating junction temperature
- 4-mm × 4.5-mm VQFN package
- Create a custom design using the TPS542A52 with the WEBENCH® Power Designer

2 Applications

- Wireless communications
- Analog front end power
- Test and measurement equipment
- Medical imaging

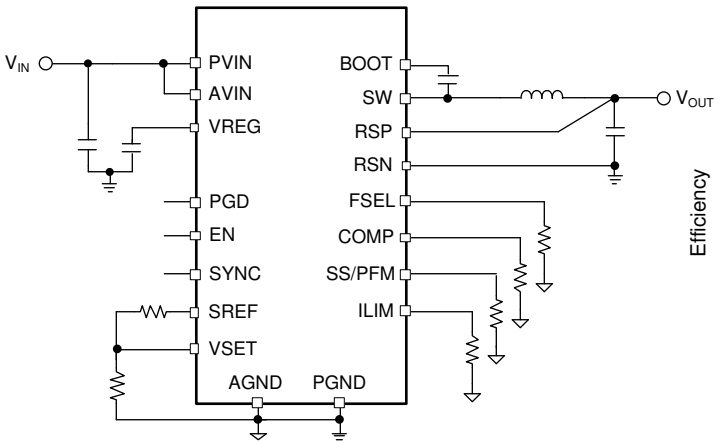
3 Description

The TPS542A52 is a high-efficiency synchronous buck converter with differential remote sense. This device features fixed-frequency, voltage-control mode with pinstrap selectable internal compensation for reduced system cost and complexity. The PWM can be synchronized to an external clock through the SYNC pin. Other key features include PFM for high light load efficiency, low shutdown quiescent current draw, adjustable UVLO through the EN pin and monotonic start up into pre-biased conditions. The TPS542A52 is a lead-free device. It is fully RoHS compliant without exemption.

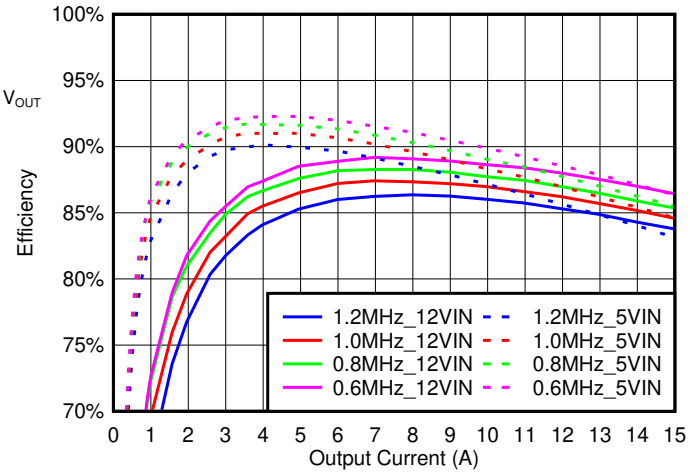
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS542A52	VQFN (33)	4.50 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



Typical Efficiency at 1 V_{OUT}

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2021) to Revision C (December 2021)	Page
• Added the pulse-width limitations on the enable pin	14
• Added the resistance-tolerance value recommended to be placed on the V_{SET} resistor divider network	14
• Added the maximum voltage ringing level value recommended	15
• Added clarification on when Power Good is forced low	18
• Added methods on how to prevent an over-current fault trigger at start-up	18

Changes from Revision A (October 2020) to Revision B (October 2021)	Page
• Changed "V_{VRSF}" to "V_{RSP}" for I_Q – PFM Mode current test condition in the *Electrical Characteristics*	5
• Changed R_{FSEL} test condition values under *Switching Frequency* in the *Electrical Characteristics*	5
• Changed "K" to "k" under *Switching Frequency* in the *Electrical Characteristics*	5
• Changed R_{ILIM} test condition values under *Current Sense and Protection* in the *Electrical Characteristics*	5
• Changed R_{FSEL} values in Table 7-1	15
• Changed R_{COMP} values in Table 7-2	15
• Changed $R_{SS/PFM}$ values in Table 7-5	17
• Changed R_{ILIM} values in Table 7-7	18
• Updated all figures in Section 8.2.1.4 to demonstrate new R_{FSEL}, R_{COMP}, $R_{SS/PFM}$ and R_{ILIM} values	25

5 Pin Configuration and Functions

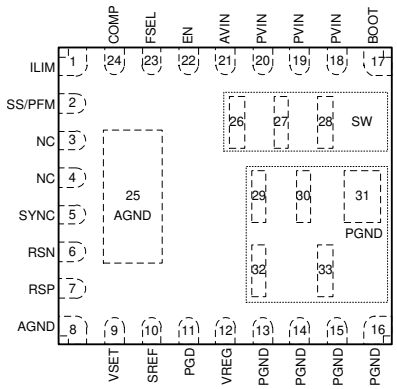


Figure 5-1. RJM Package 33-Pin VQFN Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	8, 25	G	Ground of the internal analog and digital circuitry
AVIN	21	P	Power input to the controller. Tie this pin to PVIN. It is best to use an RC filter from PVIN such as 10-Ω and 100 nF to 1 µF.
BOOT	17	P	Gate drive voltage for high-side FET. Connect a bootstrap capacitor between this pin and SW.
COMP	24	I	A resistor to ground sets the compensation network. This pin can be grounded to select the default compensation and reduce BOM count.
EN	22	I	Enable pin. Float to enable, enable/disable with an external signal, or adjust the input undervoltage lockout with a resistor divider.
FSEL	23	I	A resistor to ground sets the switching frequency of the converter. This pin can be grounded to select the default switching frequency to reduce BOM count.
ILIM	1	I	A resistor to ground sets the overcurrent protection limit. This pin can be grounded to select default settings and reduce BOM count.
PGD	11	O	Open-drain power good status
PGND	13-16, 29-33	G	Power ground. These pins are internally connected to the return of the internal low-side FET.
PVIN	18-20	P	Power inputs to the power stage. Low impedance bypassing of these pins to PGND is critical. At least 10 nF to 100 nF capacitor from PVIN to PGND is required.
RSN	6	I	Remote sense ground return
RSP	7	I	Remote sense connection to V_{OUT}
NC	3	N/A	No connect
NC	4	N/A	No connect
SREF	10	O	1.2-V nominal system reference
SS/PFM	2	I	A resistor to ground sets the soft-start slew rate and PFM mode. To reduce BOM count, this pin can be grounded to use the default soft-start rate and enable PFM mode.
SYNC	5	I	This pin is a clock input for synchronizing the oscillator.
SW	26-28	O	Switch node output of the converter. Connect this pin to the output inductor to ground.
VREG	12	I/O	Bypass pin for the internal power stage LDO. It is recommended to use a 4.7-µF ceramic capacitor.
VSET	9	I	Output voltage reference for the control loop. This must be the mid-point of a resistive divider from SREF to AGND. Set this voltage to be 1/5 of the desired V_{OUT}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input	PVIN, AVIN	–0.3	20	V
	PVIN - SW	–0.3	24	
	BOOT	–0.3	27.5	
	BOOT-SW	–0.3	5.5	
	EN, SYNC	–0.3	6	
	FS, COMP, ILIM, SS/PFM, SREF, VSET	–0.3	1.98	
	RSP	–0.3	6	
	PGD	–0.3	6	
Output	SW	–0.3	22	V
	SW transient (<10 ns)	–2	22	
	VREG	–0.3	6	
	Operating junction temperature, T_J	–40	150	°C
	Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_J = -40°C to 150°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
PVIN, AVIN	Input voltage	4	12	18	V
VOUT	Output voltage	0.5		5.5	V
IOUT	Output current	0		15	A
EN		0		5.5	V
SYNC		0		3.3	V
FS, COMP, ILIM, SS/PFM,SREF, VSET		0		1.8	V
T_J	Junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS542A52 RJM (VQFN) 33 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.9	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance EVM PCB Layout	22.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = -40℃ to 150℃ (unless otherwise noted)

PARAMETER (1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (PVIN, AVIN PINS)						
V_{IN}	PVIN and AVIN supply range		4	12	18	V
I_Q	Shutdown current	EN < 0.4 V		17		µA
	PFM Mode current	V_{IN} = 12 V, V_{OUT} = 1 V, EN > 1.2 V, no switching, V_{RSP} > 5*V_{VSET}		1800		
ENABLE and UVLO (EN PIN)						
V_{EN}	Enable threshold: ON/OFF	Rising and falling		1.2		V
I_{EN}	Enable input current	Enable threshold – 50 mV		–0.6		µA
		Enable threshold + 50 mV		–5		
UVLO (AVIN, PVIN PINS)						
AVIN, PVIN	UVLO rising threshold		3.75	3.85	4	V
	UVLO falling threshold		3.50	3.6	3.7	
	Hysteresis			0.25		
INTERNAL REGULATOR, POWER STAGE (VREG PIN)						
V_{VREG}	LDO output voltage	LDO output current = 0A	4.3	4.7	4.96	V
V_{VREG}	LDO output voltage	LDO output current = 30mA		4.7		V
	Output current limit	V_{VREG} = 4.7V	120	170	220	mA
	Nominal output current	f_{sw} = 2.2 MHz, output current = 15 A, V_{VREG} = 4.7V		30		mA
$V_{REG(UVLO)}$	UVLO rising yhreshold			2.8		V
	UVLO falling threshold			2.6		
	UVLO hysteresis			0.2		
CONTROL REFERENCE VOLTAGE (SREF PIN)						
V_{SREF}	SREF output voltage	Tolerance included in RSP/RSN accuracy		1.2		V
ISREF	SREF current sourcing capability	Resistance > 6 kΩ			200	µA

T_J = -40°C to 150°C (unless otherwise noted)

PARAMETER (1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE REGULATION ACCURACY						
	Output Voltage Accuracy; Vout = 1V	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 0.2V, –40 to 150°C	-15		15	mV
	Output Voltage Accuracy; Vout =1V	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 0.2V, –40 to 125°C	-13		13	mV
	Output Voltage Accuracy; Vout = 1V	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 0.2V, 0 to 105°C	-11.0		9.0	mV
	Output Voltage Accuracy; Vout = 0.8V	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 0.16V, –40 to 150°C	-15		15	mV
	Output Voltage Accuracy; Vout = 1.2V	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 0.24V, –40 to 150°C	-15		15	mV
	Output Voltage Accuracy; Vout = 5.5V (1)	Total internal accuracy, measured at the RSP and RSN pins = 5*VSET, VSET = 1.1V, –40 to 150°C	-30		30	mV
REMOTE SENSE AMPLIFIER						
	Unity gain bandwidth (1)			7		MHz
	Open loop gain (1)			83		dB
	Slew rate (1)			2.5		V/us
	Input common mode range (1)		-0.05		1.1	V
Vos	Input offset voltage (RSA and EA combined offset trim) (1)			0.25		mV
SWITCHING FREQUENCY						
FSW_1MHz	Switching frequency 1MHz	R_{FSEL} = 35.7 kΩ or Short	900	1000	1100	kHz
FSW_400kHz	Switching frequency 400 kHz	R_{FSEL} = 7.5 kΩ	-10		15	%
FSW_600kHz	Switching frequency 600 kHz	R_{FSEL} = 18.2 kΩ	-10		15	%
FSW_800kHz	Switching frequency 800 kHz	R_{FSEL} = 26.1 kΩ	-10		15	%
FSW_1.2MHz	Switching frequency 1.2 MHz	R_{FSEL} = 47.5 kΩ	-9		11	%
FSW_2MHz	Switching frequency 2 MHz	R_{FSEL} = 61.9 kΩ	-10		15	%
FSW_2.2MHz	Switching frequency 2.2 MHz	R_{FSEL} = 78.7 kΩ	-10		15	%
	Minimum On-Time			12		ns
	Minimum Off-Time			85		ns
SYNC						
$V_{IH(SYNC)}$	High-level input voltage	EN = High	1.35			V
$V_{IL(SYNC)}$	Low-level input voltage				0.8	V
	Sync input minimum pulse width				50	ns
Δf_{SYNC}	SYNC pin frequency range from f_{SW}		–10%		15%	
$V_{IH(SYNC)-PROG}$	High-level input voltage to enter programming mode when EN = 0V	EN = Low	1.35			V
POWER STAGE						
$R_{ds(on)1}$	Main high-side MOSFET on-resistance	V_{VREG} = 4.7 V, T_J = 25°C		9.1		mΩ
$R_{ds(on)2}$	Main Low-side MOSFET on-resistance	V_{VREG} = 4.7 V, T_J = 25°C		2.6		mΩ

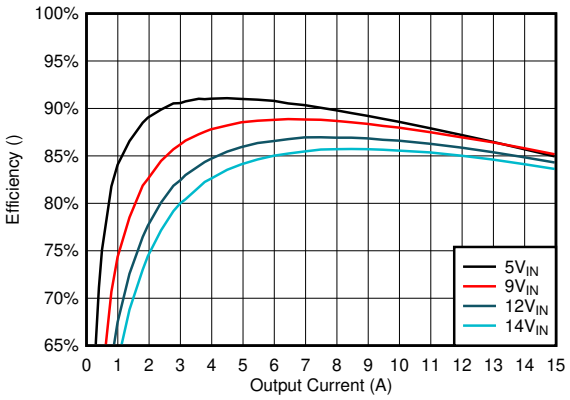
T_J = -40°C to 150°C (unless otherwise noted)

PARAMETER [1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Tdt(L-H)	Dead-time between low-side off and high-side on transition	VREG = 4.7V, T_J = 25°C		10		ns
Tdt(H-L)	Dead-time between high-side off and low-side on transition	VREG = 4.7V, T_J = 25°C		10		ns
CURRENT SENSE AND PROTECTION						
IS1	OC limit HS FET			20		A
IS2	OC limit LS FET 6	R_{ILIM} = 61.9 kΩ	17.60	20	22	A
	OC limit LS FET 5	R_{ILIM} = 47.5 kΩ	14.78	16.5	18.48	
	OC limit LS FET 4	R_{ILIM} = 35.7 kΩ	11.56	13	15.62	
	OC limit LS FET 3	R_{ILIM} = 26.1 kΩ	9.26	10.5	13.56	
	OC limit LS FET 2	R_{ILIM} = 18.2 kΩ	6.96	8	11.60	
	OC limit LS FET 1	R_{ILIM} = 7.5 kΩ	4.66	5.5	9.60	
IS2	Negative OC limit LS FET			-8.5		A
IS2	Zero-cross detection comparator trip point			135		mA
SOFT-START COUNTER						
t_{SS}	SS setting 1: 2.0MHz CLK	V_{VSET} = 0.1 V to 0.28 V		0.45		ms
	SS setting 2: 1.0MHz CLK	V_{VSET} = 0.1 V to 0.28 V		0.9		
	SS setting 3: 0.5MHz CLK	V_{VSET} = 0.1 V to 0.28 V		1.8		
	SS setting 4: 0.25MHz CLK	V_{VSET} = 0.1 V to 0.28 V		3.6		
INTERNAL BOOTSTRAP SWITCH						
	Forward voltage	$V_{VREG(BOOT)}$, I_F = 10 mA, T_A = 25°C		0.16	0.3	V
OUTPUT VOLTAGE OVERSHOOT REDUCTION						
POWER-ON DELAY						
	Power-on delay time	From EN to SS; V_{IN} > 4 V		500		us
POWER GOOD and OV/UV WARNING						
V_{RSP}	OV warning level	RSP rising (fault)	105	110	115	% 5*V_{VSET}
	OV warning level	RSP falling (reset)	100	105	109	
	UV warning level	RSP falling (fault)	87	90	93.5	
	UV warning level	RSP rising (reset)	91	95	99	
	PGD delay time	Delay from SS finish to PGD high		500		µs
$R_{ds(on)PGDFET}$		PGD FET On Resistance, I_{PGOOD} =5mA	4.1	5.8	9.1	Ω
OUTPUT OVERVOLTAGE PROTECTION (OVP)						
V_{RSP}	OVP trip level	RSP rising (fault), V_{VSET} ≤ 1.04 V	110	115	120	% 5*V_{VSET}
	OVP reset level	RSP falling	76	80	84	
	OVP delay			100		ns
OUPUT UNDERVOLTAGE PROTECTION (UVP)						
V_{RSP}	UVP detect voltage		76	80	84	% 5*V_{SET}
	UV delay			100		ns
THERMAL SHUTDOWN						
T_{SDN}	Shutdown temperature[1]		155	165		°C
	Hysteresis[1]			15		°C

(1) Specified by design. Not production tested.

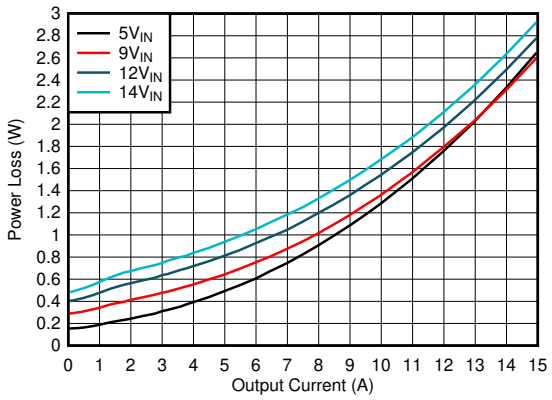
6.6 Typical Characteristics

Measured at 25°C unless otherwise specified



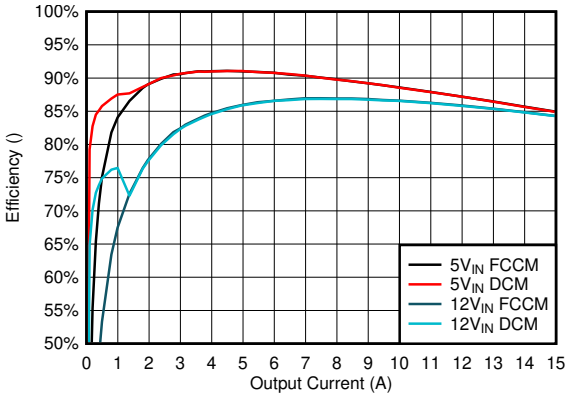
V_{OUT} = 1 V f_{SW} = 1 MHz, FCCM

Figure 6-1. Efficiency vs Output Current



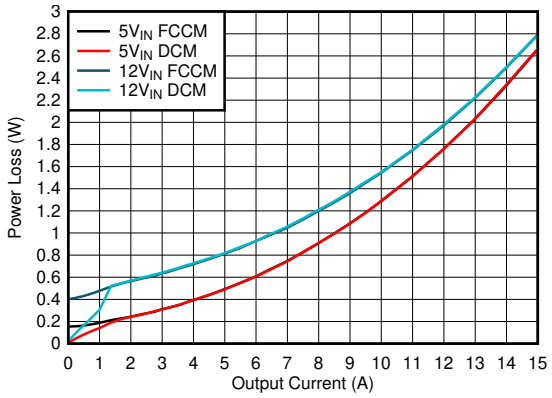
V_{OUT} = 1 V f_{SW} = 1 MHz, FCCM

Figure 6-2. Power Loss vs Output Current



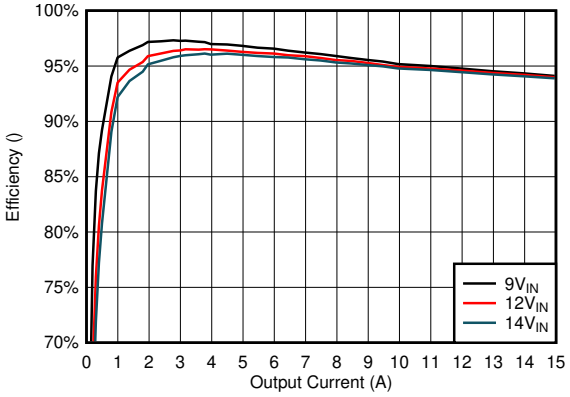
V_{OUT} = 1 V f_{SW} = 1 MHz, DCM versus FCCM

Figure 6-3. Efficiency vs Output Current



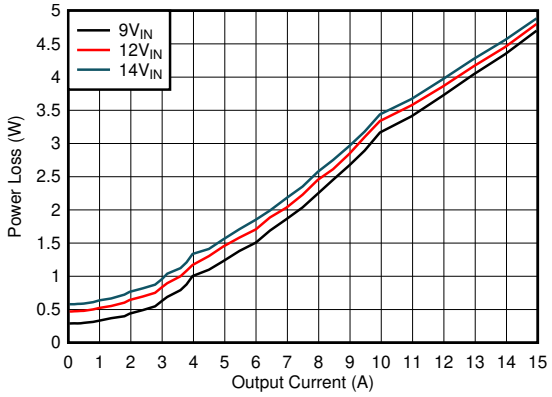
V_{OUT} = 1 V f_{SW} = 1 MHz, DCM versus FCCM

Figure 6-4. Power Loss vs Output Current



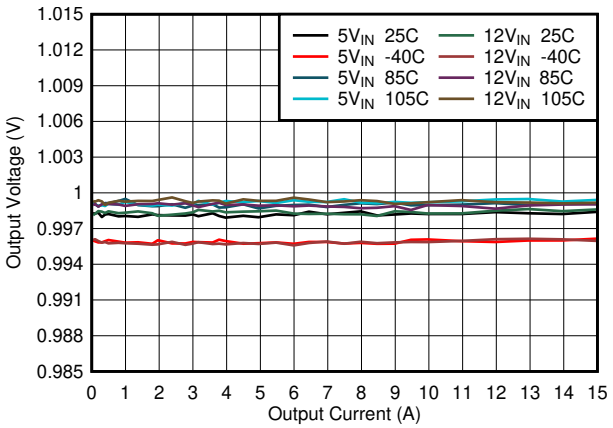
V_{OUT} = 5 V f_{SW} = 400 kHz, FCCM

Figure 6-5. Efficiency vs Output Current



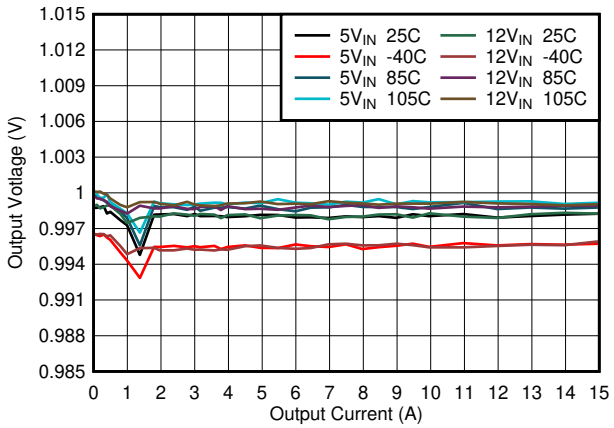
V_{OUT} = 5 V f_{SW} = 400 kHz, FCCM

Figure 6-6. Power Loss vs Output Current



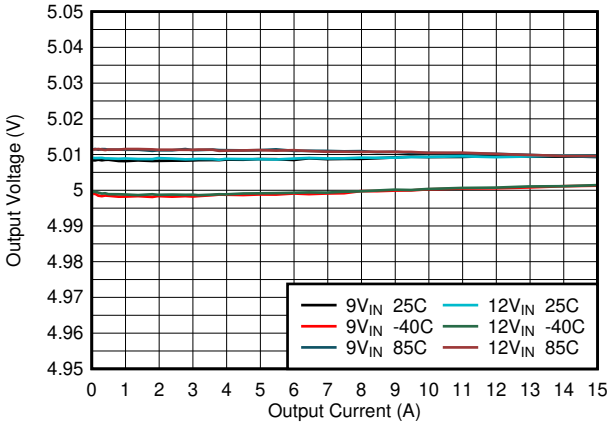
V_{OUT} = 1 V f_{SW} = 1 MHz, FCCM

Figure 6-7. Load Regulation



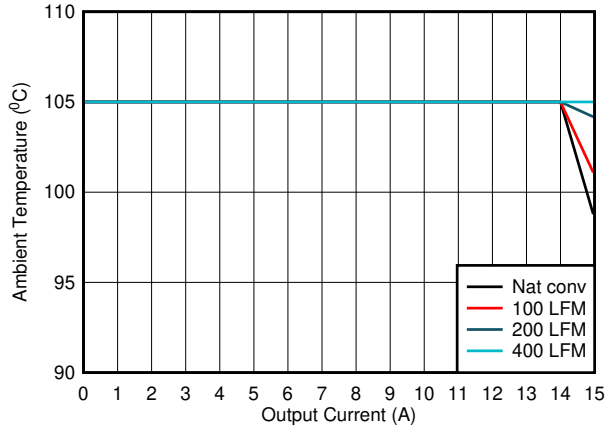
V_{OUT} = 1 V f_{SW} = 1 MHz, DCM

Figure 6-8. Line Regulation



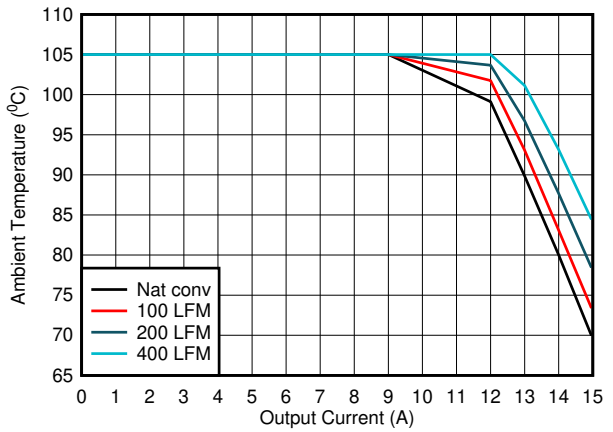
V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 400 KHz, FCCM

Figure 6-9. Line Regulation



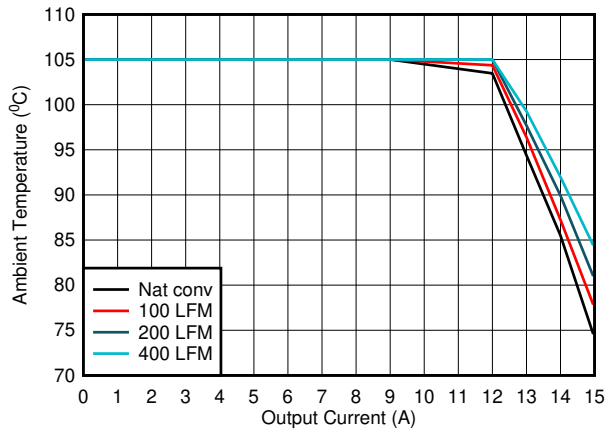
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1 MHz

Figure 6-10. Ambient Temperature vs Output Current



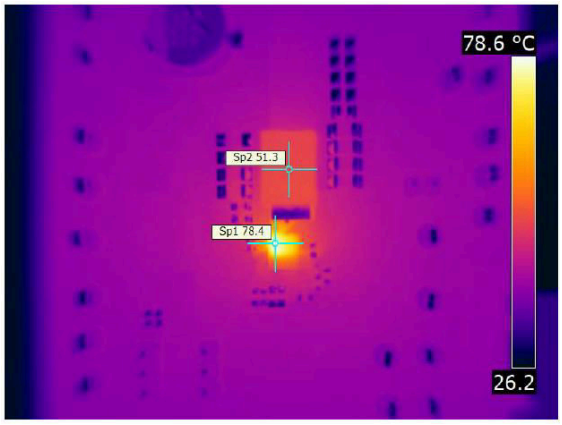
V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 600 kHz

Figure 6-11. Ambient Temperature vs Output Current



V_{IN} = 5.5 V V_{OUT} = 1 V f_{SW} = 2.2 MHz

Figure 6-12. Ambient Temperature vs Output Current

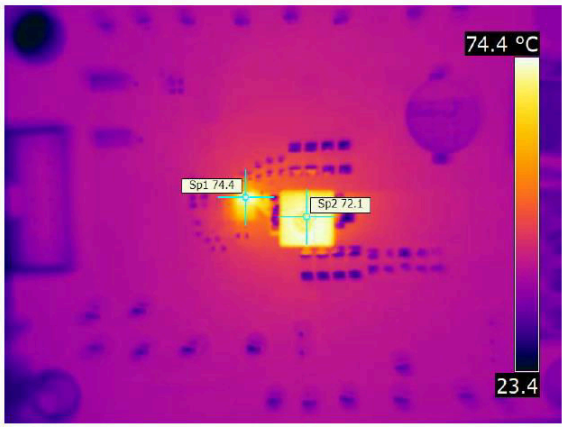


V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1 MHz

Figure 6-13. Thermal Image at 15-A Output Current

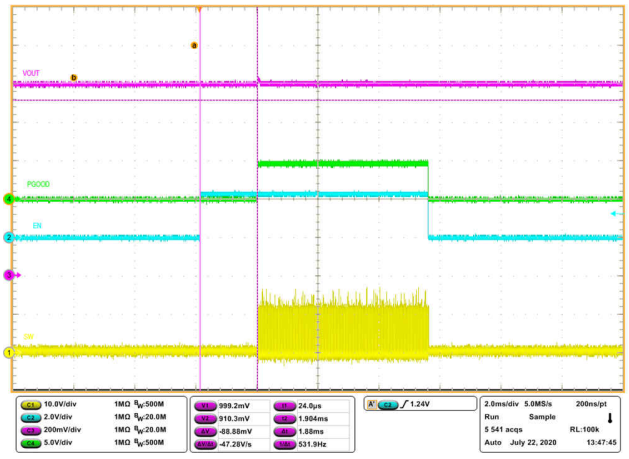
V_{IN} = 5.5 V V_{OUT} = 1 V f_{SW} = 2.2 MHz

Figure 6-14. Thermal Image at 14-A Output Current



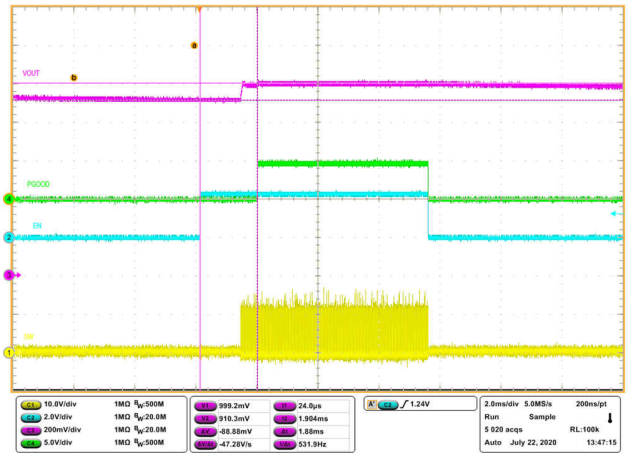
V_{IN} = 12 V V_{OUT} = 5 V f_{SW} = 0.6 MHz

Figure 6-15. Thermal Image at 12-A Output Current



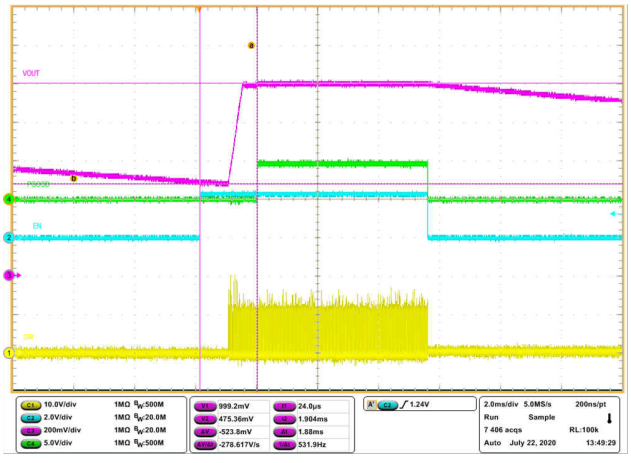
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-16. 100% Pre-biased Start-up by EN at 0-A Output Current



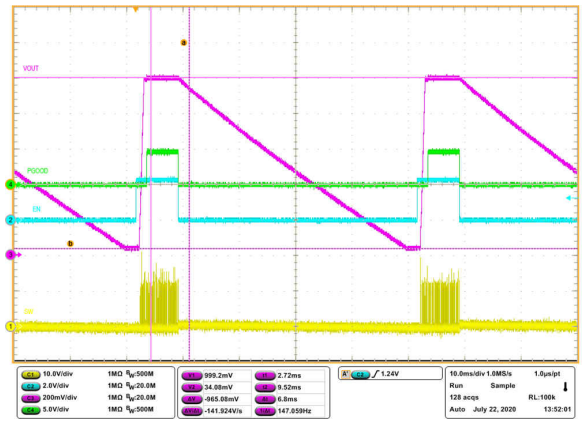
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-17. 90% Pre-biased Start-up by EN at 0-A Output Current



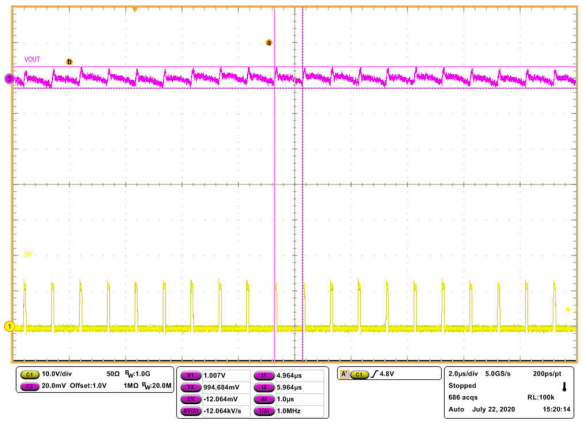
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-18. 50% Pre-biased Start-up by EN at 0-A Output Current



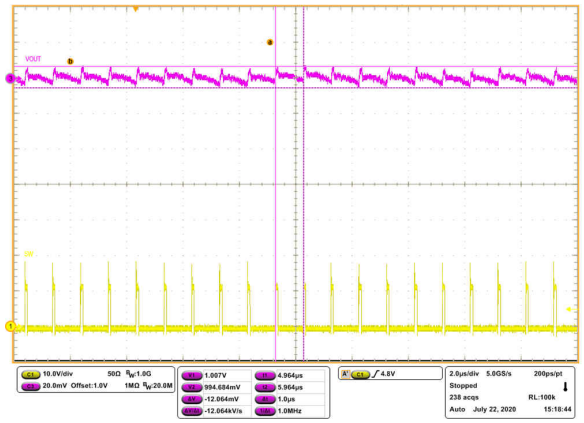
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-19. Start-up and Shutdown by EN at 0-A Output Current



V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-20. Steady State at 0-A Output Current

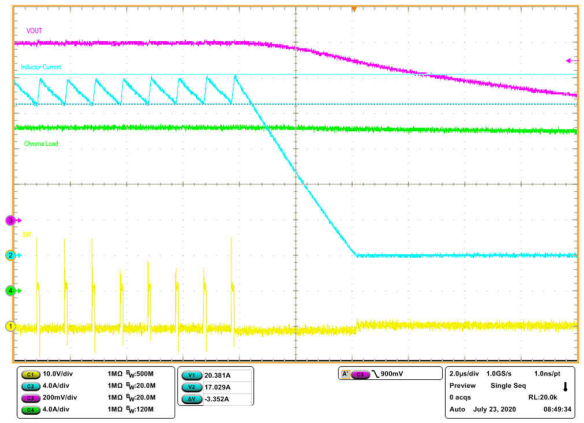


V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-21. Steady State at 10-A Output Current

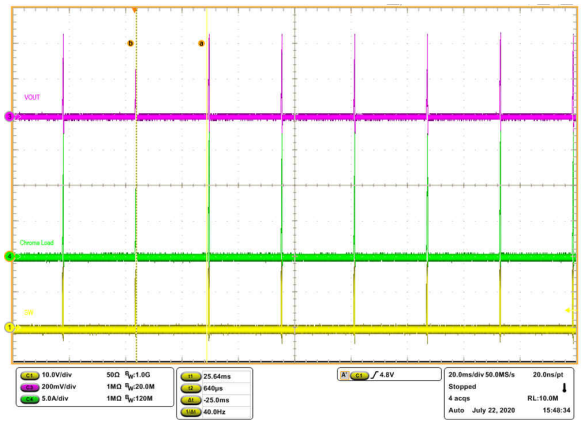
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-22. Switch Node Ringing and Dead-Time at 10-A Output Current



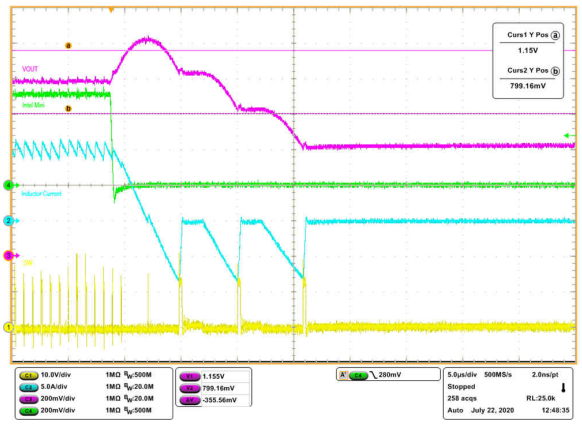
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-23. 20-A Overcurrent Protection by Chroma Electronic Load



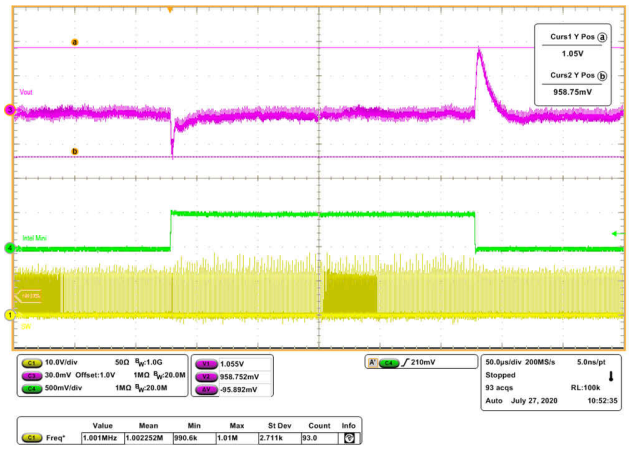
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-24. Short Overcurrent Protection Hiccup by Chroma Electronic Load



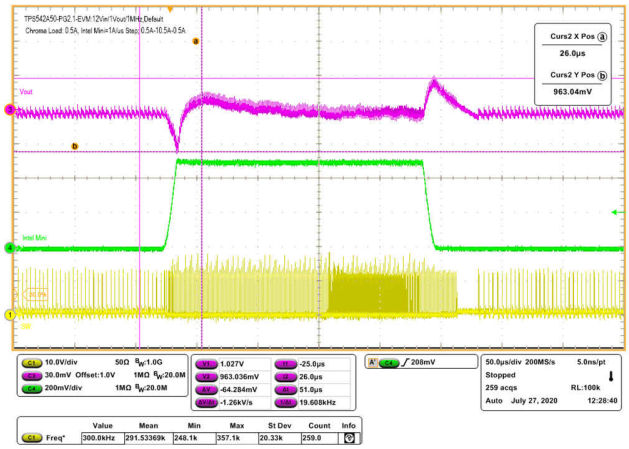
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.2 MHz BOM

Figure 6-25. Overvoltage Protection, Negative OCP, then Undervoltage Protection by Load Step Down



V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

Figure 6-26. Load Transient 2 A to 12 A to 2 A at 20 A/µs



V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.0 MHz BOM

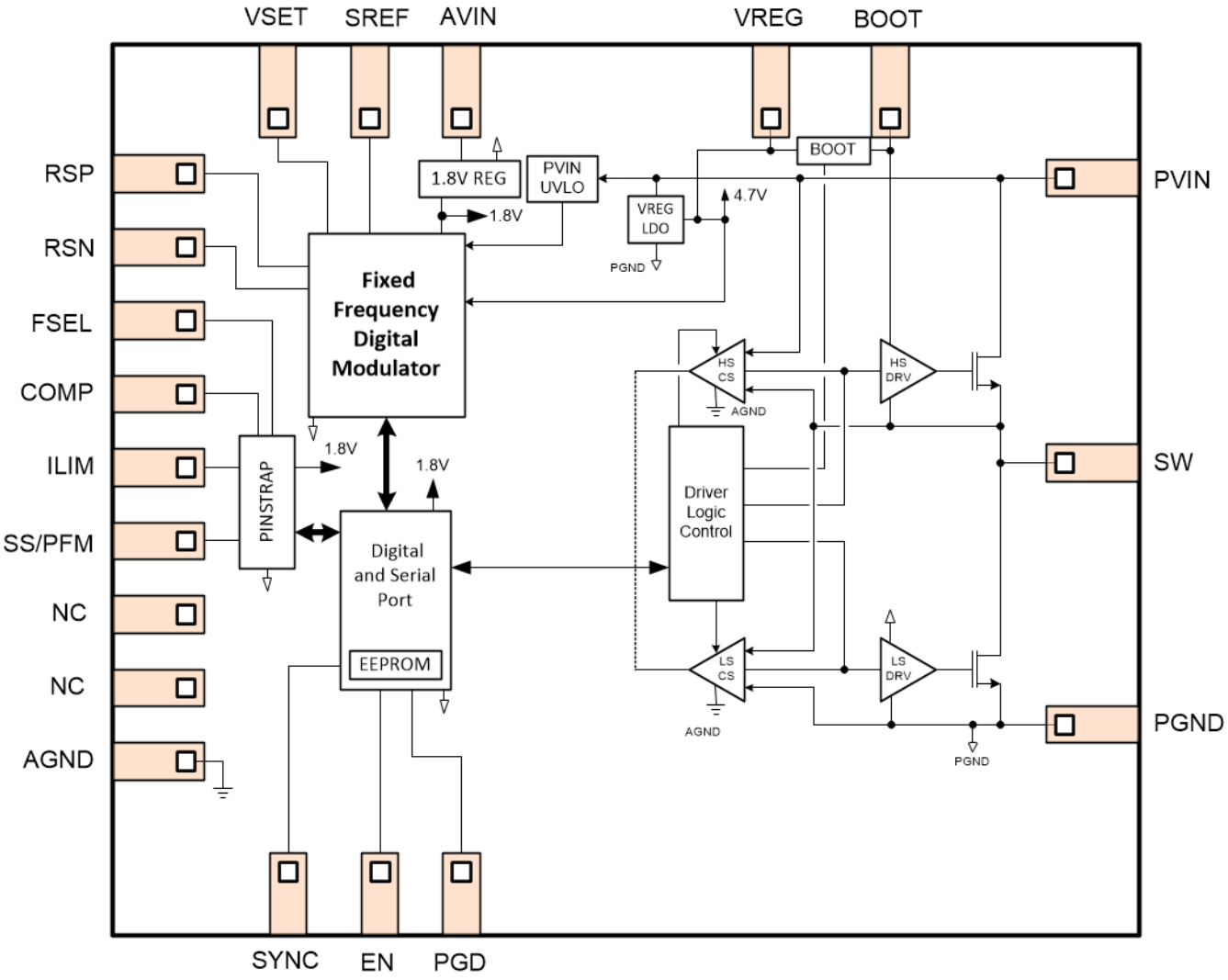
Figure 6-27. Load Transient in DCM to FCM 0.5 A to 10.5 A to 0.5 A at 1 A/µs

7 Detailed Description

7.1 Overview

The TPS542A52 is a high-efficiency, single-channel, synchronous buck converter with integrated n-channel MOSFETs. The device suits low-output voltage point-of-load applications with 15-A or lower current. The TPS542A52 has a maximum operating junction temperature of 150°C making it suitable for high-ambient temperature applications such as wireless infrastructure. The input voltage range is 4 V to 18 V, and the output voltage range is 0.5 V to 5.5 V. The device features a fixed-frequency, voltage-control mode with a switching frequency range of 400 kHz to 2.2 MHz allowing for efficiency and size optimization when selecting output filter components. The controller features selectable internal compensation that makes the device easy to use with low external component count. The internal compensation networks support a wide range of output inductance and capacitance, supporting all types of capacitors. The controller uses a digital PWM modulator that allows for very narrow on-times with low jitter, making it ideal for high-frequency and high-step down ratio applications. The switching frequency of the device can be synchronized to an external clock applied to the SYNC pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Adjustable Undervoltage Lockout

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage (typically 1.2 V), the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low power shutdown.

The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. The EN pin can also be externally driven high or low. When the pulse-width is less than 22 µs, the EN pin will detect the pulse as a low and cause the device to enter hiccup-mode. If the pulse-width is greater than 22 µs, then the EN pin will detect the pulse as low but will not enter hiccup-mode.

For adjustable input undervoltage lockout (UVLO), connect the EN pin to the middle point of an external resistor divider. Once the EN pin voltage exceeds the threshold, an additional 5 µA of hystersis current is added to facilitate UVLO hysteresis. Equation 1 shows the calculation of resistor divider network.

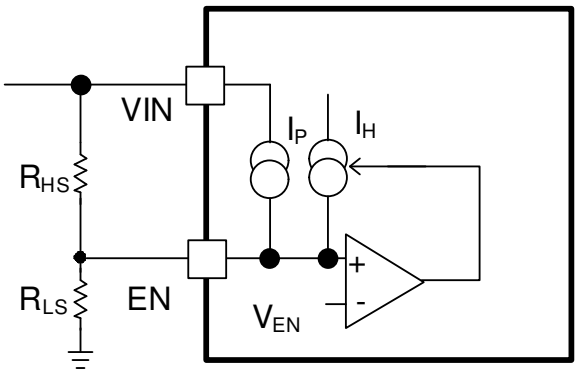


Figure 7-1. EN UVLO

$$R_{HS} = \frac{V_{START} - V_{STOP}}{I_H}$$

$$R_{LS} = \frac{R_{HS} \cdot V_{EN}}{V_{STOP} - V_{EN} + R_{HS}\left(I_P + I_H\right)}$$

$$V_{EN} = 1.2V;\ I_P = 0.6\mu A;\ I_H = 5\mu A \quad (1)$$

7.3.2 Input and VREG Undervoltage Lockout Protection

The TPS542A52 provides fixed VIN and VREG UVLO thresholds and hysteresis. The typical VIN turnon threshold is 3.85 V and hystersis is 0.25 V. The typical VREG turnon threshold is 2.8 and hysteresis is 0.2 V. There is no power-up sequence. Once all of the UVLO requirements have been met and the EN pin voltage exceeds the enable threshold, the converter begins operation.

7.3.3 Voltage Reference and Setting the Output Voltage

The device has a 1.2-V reference that comes out on the SREF pin. To set the reference voltage of the converter, connect the VSET pin to the mid-point of a resistor divider between SREF and AGND. TI recommends that the total impedance of this divider network be > 6 kΩ. For best accuracy, the resistor's tolerance of 0.1% is recommended. Do not connect anything other than a resistor divider network to SREF.

There is an internal 5:1 resistor divider between the RSP and RSN feedback pins, so the VSET voltage must be set to 1/5 of the desired output voltage. VSET can be programmed to any value between 0.1 and 1.1 V.

7.3.4 Remote Sense Function

RSP and RSN pins are used for remote sensing purposes. Always connect RSP to the positive sensing point of the load, and always connect the RSN pin to the load return. There is an internal 5:1 divider in the device, so do

not connect an external feedback resistor divider. The converter loop gain measurement can tolerate 10 Ω to 50 Ω in series with RSP and output voltage.

7.3.5 Switching Frequency

The internal oscillator of the device can be set to one of seven switching frequencies by a resistor to ground on the FSEL pin. The FSEL pin can be shorted to ground to reduce BOM component count. When shorted to ground, the default converter switching frequency is used.

Table 7-1. Frequency Resistor Selection

R_{FSEL} (kΩ)	f_{SW} (kHz)
Short	1000
7.5	400
18.2	600
26.1	800
35.7	1000
47.5	1200
61.9	2000
78.7	2200

The oscillator can also be synchronized to an external clock on the SYNC pin. The external clock frequency must be within -10% and +15% of the programmed frequency of the converter. The SYNC pin has an internal pulldown so it can be left floating externally.

When the converter operates at 2 MHz or 2.2 MHz, it is recommended to set the OCP at 13 A or lower and without a snubber circuit. For operation with OCP at 16.5 A, a snubber circuit is required. The snubber circuit components can start with a 470-pF cap and 2-Ω resistor to help reduce voltage ringing levels. It is recommended for the ringing levels to be 2-V below the *Absolute Maximum Ratings* between SW and GND at room temperature. The component values will need to be tuned to achieve optimal results.

7.3.6 Voltage Control Mode Internal Compensation

The TPS542A52 has 15 unique internal compensation settings to cover a wide range of output inductors and capacitors. For each switching frequency option, there are four compensation options that can be chosen using a single resistor to ground on the COMP pin.

Table 7-2. Compensation Resistor Selection

R_{COMP} (kΩ)++	COMPENSATION SETTING
Short	COMP 2
7.5	COMP 1
18.2	COMP 2
26.1	COMP 3
35.7	COMP 4
47.5	COMP 1
61.9	COMP 2
78.7	COMP 3
102	COMP 4

Each compensation network consists of two zeros and one high frequency pole. Table 7-3 maps the compensation settings to the first zero frequency at different output voltage range, second zero frequency, and high frequency pole.

Table 7-3. Compensation Settings

FREQUENCY (kHz)	COMPENSATION SETTING	ZERO 1 (kHz) for VOUT = 0.5 V-1.1 V	ZERO 1 (kHz) for VOUT = 1.2 V-1.5 V	ZERO 1 (kHz) for VOUT = 1.6 V-2.8 V	ZERO 1 (kHz) for VOUT = 2.9 V-4.0 V	ZERO 1 (kHz) for VOUT = 4.1 V-5.5 V	ZERO 2 (kHz)	POLE (kHz)
400	COMP 1	2.2	2.1	1.8	1.6	1.2	5.5	60
	COMP 2	2.2	2.1	1.8	1.6	1.2	7.3	80
	COMP 3	3.6	3.4	3.0	2.7	2.0	14.5	159
	COMP 4	7.2	7.0	6.1	5.4	4.1	28.4	312
600	COMP 1	2.2	2.1	1.8	1.6	1.2	5.5	60
	COMP 2	2.7	2.6	2.3	2.0	1.5	11.0	121
	COMP 3	4.5	4.3	3.8	3.4	2.5	18.1	199
	COMP 4	10.5	10.1	8.8	7.9	5.9	45.2	497
800	COMP 1	2.2	2.1	1.8	1.6	1.2	7.3	80
	COMP 2	3.6	3.4	3.0	2.7	2.0	14.5	159
	COMP 3	7.2	7.0	6.0	5.4	4.1	28.4	312
	COMP 4	13.5	13	11.4	10.1	7.6	55.6	612
1000	COMP 1	2.2	2.1	1.9	1.7	1.2	9.0	99
	COMP 2	4.5	4.3	3.8	3.4	2.5	18.1	199
	COMP 3	9.0	8.7	7.6	6.7	5.1	37.1	408
	COMP 4	18.8	18.2	15.9	14.1	10.6	72.3	796
1200	COMP 1	2.7	2.6	2.3	2.0	1.5	11.0	121
	COMP 2	4.5	4.3	3.8	3.4	2.5	18.1	199
	COMP 3	10.5	10.1	8.8	7.9	5.9	45.2	497
	COMP 4	23.5	22.7	19.9	17.7	13.3	90.4	995
2000	COMP 1	4.5	4.3	3.8	3.4	2.5	18.1	199
	COMP 2	9	8.7	7.6	6.7	5.1	37.1	408
	COMP 3	18.8	18.2	15.9	14.1	10.6	72.3	796
	COMP 4	37.7	36.4	31.8	28.3	21.2	144.7	1592
2200	COMP 1	4.5	4.3	3.8	3.4	2.5	18.1	199
	COMP 2	9	8.7	7.6	6.7	5.1	37.1	408
	COMP 3	18.8	18.2	15.9	14.1	10.6	72.3	796
	COMP 4	37.7	36.4	31.8	28.3	21.2	144.7	1592

Table 7-4 shows the second zero frequency placement about two times based on a ratio (f_O/f_{SW}) of the LC frequency (f_O) to the switching frequency and lists the values in Table 7-3. The second zero frequency does not change with the output voltage. The high frequency pole is about 10 times of the second zero frequency to attenuate the switching frequency noise and to have a safe gain margin.

The output filter LC frequency should be designed between the first and second zero frequencies. The ratio of the LC frequency to the switching frequency in Table 7-4 is a guide to select the LC frequency f_O. For example, the LC frequency for 1-MHz switching frequency is 10 kHz at 1% ratio. Given 1-V output voltage, COMP2 has the first zero at 4.5 kHz to compensate the LC filter double poles. For the same LC filter and switching frequencies of 3.3-V output voltage, COMP3 has the first zero at 6.7 kHz to compensate the LC filter double poles. The compensation setting needs to consider for the output capacitor derating, especially ceramic capacitor and inductor tolerance. It is recommended to verify the load transient and bode plot based upon the compensation selection.

Table 7-4. Second Zero Frequency

f_O/f_{SW}	COMPENSATION SETTING	SECOND ZERO FREQUENCY
0.5%	COMP 1	~2X of 0.5% f_O/f_{SW}
1%	COMP 2	~2X of 1% f_O/f_{SW}
2%	COMP 3	~2X of 2% f_O/f_{SW}
4%	COMP 4	~2X of 4% f_O/f_{SW}

7.3.7 Soft Start and Prebiased Output Start-up

The TPS542A52 uses a programmable soft-start rate to gradually ramp the output voltage reference to reduce inrush currents. The device prevents current from being discharged from the output during start-up when a pre-biased condition exists. No switching pulses occur until the internal soft-start reference exceeds the voltage on the error amplifier input voltage (RSP and RSN pins). The TPS542A52 supports the output voltage with pre-biasd up to 100%.

The soft-start clock in Table 7-5 can be programmed on the SS/PFM pin along with enabling/disabling PFM and hiccup time. The soft-start timing in Table 7-6 can be programmed based upon the output voltage and soft-start clock. There are four choices of soft-start time to select at different soft-start clock. To prevent an OC fault trigger at start-up, it is recommended to increase the duration of start-time to reduce the inrush current from exceeding the peak current limit. For example of 1-V output voltage, the soft-start time equals to 1.8 ms at 0.5-MHz SS CLK and 0.45 ms at 2.0-MHz SS CLK.

Table 7-5. Soft-Start CLK and PFM Resistor Selection and Hiccup Time

$R_{SS/PFM}$ (kΩ)++	PFM	SS CLK (MHz)	HICCUP DURATION (ms)
Short	Disable	1.0	25.2
7.5	Enable	2.0	12.6
18.2		1.0	25.2
26.1		0.50	50.4
35.7		0.25	100.8
47.5	Disable	2.0	12.6
61.9		1.0	25.2
78.7		0.50	50.4
102		0.25	100.8

Table 7-6. Soft-Start Timing versus Output Voltage

VSET (V)	VOUT (V)	LSB SIZE (mV)	SS TIMING (ms) AT CLK: 2.0 MHz	SS TIMING (ms) AT CLK: 1.0 MHz	SS TIMING (ms) AT CLK: 0.5 MHz	SS TIMING (ms) AT CLK: 0.25 MHz
0.1	0.5	0.112	0.45	0.9	1.8	3.6
0.2	1	0.223	0.45	0.9	1.8	3.6
0.28	1.4	0.313	0.45	0.9	1.8	3.6
0.3	1.5	0.167	0.9	1.8	3.6	7.2
0.4	2.0	0.223	0.9	1.8	3.6	7.2
0.5	2.5	0.279	0.9	1.8	3.6	7.2
0.56	2.8	0.313	0.9	1.8	3.6	7.2
0.6	3.0	0.167	1.8	3.6	7.2	14.4
0.7	3.5	0.195	1.8	3.6	7.2	14.4
0.8	4	0.223	1.8	3.6	7.2	14.4
0.9	4.5	0.251	1.8	3.6	7.2	14.4
1	5.0	0.279	1.8	3.6	7.2	14.4

7.3.8 Power Good

The power good pin is an open-drain output and needs to pull up to a voltage supply if a designer uses this feature. During normal converter operation, the device leaves this pin floating. Power good warnings occur if the output voltage is not within the OV or UV warning levels. Power Good (PGD) is forced low if OV or UV is exceeded, when the converter is in soft start, and when the converter is in shutdown or programming mode. The PGD pin is released to floating after the PGD delay time when all of the above conditions are met.

TI recommends connecting a pullup resistor to a voltage source that is 5.5 V or less, such as to the device VREG pin.

7.3.9 Overvoltage and Undervoltage Protection

An output overvoltage (OV) fault is triggered if the output voltage, sensed by RSP/RSN, is greater than the OVP trip level. When this condition is detected, the converter terminates the switching cycle and turns on the low-side FET to discharge the output voltage. The low-side FET remains on until the low-side FET current reaches the negative overcurrent limit. When the negative overcurrent limit is reached, the low set FET turns off for 2000 ns. After the 2000 ns delay, the low-side FET turns back on until the negative over-current limit is reached. This process repeats until the output voltage is discharged below the undervoltage fault threshold (typically 80% set V_{OUT}). The converter then enters hiccup for seven cycles of soft-start CLK frequency due to the output voltage being below the UV threshold.

An output undervoltage fault is triggered if the output voltage, sensed by RSP/RSN, is less than UVP threshold. When this condition is detected, power conversion is disabled, and the converter enters hiccup for seven cycles of soft-start CLK frequency.

7.3.10 Overcurrent Protection

The device senses overcurrent (OC) in both the high-side and low-side power MOSFETs using cycle by cycle detection. OC is detected in the low-side FET by sensing the voltage across the FET while it is on. After the low-side FET turns on, there is a blanking time of approximately 70 ns to allow noise to settle before the OC comparator begins sensing. If the peak current limit is hit, then an OC fault condition is detected which causes the device stops switching and enters hiccup for seven cycles of soft-start CLK frequency. The overcurrent limit is set through a single resistor to ground on the ILIM pin. The ILIM pin can be shorted to ground to reduce BOM component count. When shorted to ground the default current limit is used. Current limits shown in Table 7-7 can be programmed on the ILIM pin.

Table 7-7. Current Limit Resistor Selection

R_{ILIM} (kΩ)	TYPICAL LIMIT (A)
Short	20
7.5	5.5
18.2	8
26.1	10.5
35.7	13
47.5	16.5
61.9	20

The device also senses negative overcurrent in the low-side FET by sensing the voltage across the FET while it is on. After the low-side FET turns on, there is a blanking time to allow noise to settle before the OC comparator begins sensing. Once a negative OC fault condition is detected the device stops switching and enters hiccup for seven cycles of soft-start CLK frequency. The negative overcurrent threshold is fixed to a single value.

Overcurrent is detected in the high-side FET by sensing the voltage across the FET while it is on. After the high-side FET turns on, there is a blanking time to allow noise to settle before the OC comparator begins sensing. Once an OC fault condition is detected, the device stops switching and enters hiccup for seven cycles of soft-start CLK frequency. At start-up, the inrush current has the potential of exceeding the peak current limit, thereby causing the device to enter hiccup. To prevent an OC fault trigger at start-up, it is recommended to increase the soft-start time or decrease the load at the output to reduce the inrush current from exceeding the

peak current limit. The high-side overcurrent threshold is fixed to a single value. For an application with on-time less than 70 ns, the high-side FET over-current is not guaranteed to enable. In this case, the low-side OC will dominate and protect the load while the output current ramps up gradually. With on-times less than 70 ns and a hard short at the load, the controller loop will extend the on-time to respond to the output voltage drooping, and as a result, both high-side and low-side OC protections will engage to protect the load.

7.3.11 High-Side FET Throttling

When the high-side FET turns on or off, the ringing voltage across the FET depends on the output current, loop inductance, and PCB parasitic inductance. To diminish the ringing voltage during turning on or off, the TPS542A52 reduces the gate driver strength when TPS542A52 detects PVIN higher than 14 V with 0.5-V hysteresis.

7.3.12 Overtemperature Protection

When the device senses a temperature above the thermal shutdown limit (typically 165°C), power conversion is disabled. The converter remains disabled until the temperature cools down to the thermal recovery limit (typically 150°C). At this point the converter enters hiccup for seven cycles of soft-start CLK frequency.

7.4 Device Functional Modes

7.4.1 Pulse-Frequency Modulation Eco-mode™ Light Load Operation

When the SS/PFM pin is terminated with a 35.7-kΩ or lower resistance, the TPS542A52 operates in pulse-frequency modulation (PFM) for light load conditions to maintain high efficiency.

As the output current decreases from heavy-load conditions, the inductor current also decreases until the valley of the inductor current reaches zero amps, which is the boundary between continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM). The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs in DCM. In DCM operation, the on-time is maintained to a level approximately the same as during CCM and the converter off-time is modulated to maintain the proper output voltage. For the application of 5-V input voltage, it is not recommend to operate in PFM due to the accuracy of the zero comparator which will be reduced because of the low input voltage.

7.4.2 Forced Continuous-Conduction Mode

When the SS/PFM pin is terminated with a 47.5-kΩ or higher resistance, the TPS542A52 operates in forced continuous conduction mode (FCCM) for all load currents. During FCCM, the switching frequency is set by an internal oscillator for which the frequency can either be selected by the FSEL pin or an external clock on the SYNC pin.

7.4.3 Soft Start

The TPS542A52 operates in FCCM during soft start regardless of the setting selected by the SS/PFM pin. If PFM is enabled by the SS/PFM pin, the PFM operation begins after PGD is asserted. The delay between soft start finishing and PGD being asserted is typically 500 µs. During the start-up, the TPS542A52 has the low-side current limit at 16.5 A when the OCP configures 20 A. However, if the OCP configures below 16.5 A such as 13 A, then the current limit during soft start sets to be at 13 A. To prevent an OC fault trigger at start-up, it is recommended to increase the duration of soft-start time to reduce the inrush current from exceeding the peak current limit.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS542A52 is a high-efficiency, single-channel, synchronous buck converter with integrated n-channel MOSFETs. The device suits low-output voltage point-of-load applications with 15-A or lower current. The TPS542A52 has a maximum operating junction temperature of 150°C, which makes it suitable for high-ambient temperature applications such as wireless infrastructure. The input voltage range is 4 V to 18 V, and the output voltage range is 0.5 V to 5.5 V. The device features a fixed-frequency voltage-control mode with a switching frequency range of 400 kHz to 2.2 MHz, allowing for efficiency and size optimization when selecting output filter components. The controller features selectable internal compensation making the device easy to use with a low external-component count. The internal compensation networks are able to support a wide range of output inductance and capacitance, supporting all types of capacitors. The controller utilizes a digital PWM modulator that allows for very narrow on-times making it ideal for high-frequency and high-step down ratio applications. The switching frequency of the device can be synchronized to an external clock applied to the SYNC pin.

8.2 Typical Application

8.2.1 Full Analog Configuration

A resistor to ground on the FSEL, COMP, SS/PFM, and ILIM pins configure the device. Any of these pins can be grounded to use the default values and reduce component count.

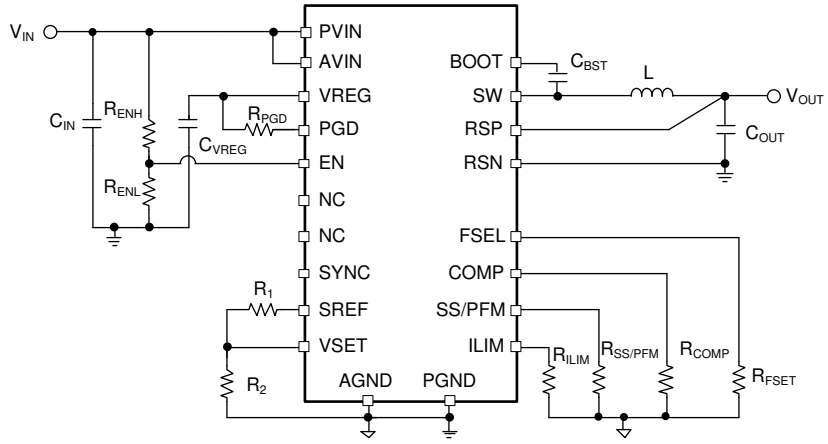


Figure 8-1. Full Analog Configuration

8.2.1.1 Design Requirements

For this design example, use the input parameters shown in Table 8-1.

Table 8-1. Design Example Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}, Input Voltage		9	12	14	V
$V_{IN(ripple)}$, Input Ripple Voltage				0.2	V
V_{OUT}, Output Voltage			1		V
V_{PP}, Ouput Ripple Voltage			15		mV
V_{OVER}, Transient Response Overshoot	I_{STEP} = 5 A at 1 A/µs		30		mV

Table 8-1. Design Example Specifications (continued)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{UNDER}, Transient Response Undershoot	I_{STEP} = 5 A at 1 A/µs		30		mV
I_{OUT}, Output Current			10		A
I_{OC}, Over-Current Trip Point			16		A
F_{SW}, Switching Frequency			1.2		MHz
t_{SS}, Soft-start time			0.5		ms

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS542A52 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Output Voltage Calculation

The output voltage equals five times of VSET. To set VSET voltage, a resistor divider network is required from SREF (1.2 V). Equation 2 shows the output voltage calculation. It is recommended to use R_1 and R_2 in the range of 1 kΩ to 100 kΩ with a resistance-tolerance of 0.1% for best accuracy and that the total impedance of this divider network be > 6 kΩ. For example, R_1 equals 50 kΩ and R_2 equals 10 kΩ for 1-V output voltage.

$$V_{OUT} = 5 \times VSET$$
$$VSET = \frac{R_2}{R_1 + R_2} \times 1.2$$
$$V_{OUT} = 5 \times \frac{R_2}{R_1 + R_2} \times 1.2 \quad (2)$$

8.2.1.2.3 Switching Frequency Selection

There is a trade off between higher and lower switching frequencies. Higher switching frequencies can produce a smaller solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which decrease efficiency and impacts thermal performance. In this design, a moderate switching frequency of 1.2 MHz achieves both a small solution size and a high efficiency operation is selected. The TPS542A52 offers seven choices of switching frequency in Table 7-1. RFSET equals to 47.5 kΩ for 1.2-MHz switching frequency.

8.2.1.2.4 Inductor Selection

The inductor value is a compromise between having a good load step transient response, output ripple voltage, and efficiency. A good practice is to select the inductor ripple current value between 15% to 50% of the maximum output current. The output capacitor absorbs the inductor-ripple current. Therefore, selecting a high inductor-ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple-current rating equal to or greater than the inductor-ripple current. Using 35% target ripple current, the required inductor size can be calculated as shown in Equation 3.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{OUT} \times 0.35} = \frac{1.0\ V \times (12\ V - 1.0\ V)}{12\ V \times 1.2\ MHz \times 10\ A \times 0.35} = 218\ nH \quad (3)$$

A standard inductor value of 220 nH is selected.

8.2.1.2.5 Input Capacitor Selection

The TPS542A52 requires a high-quality, ceramic, type X5R or X7R, input decoupling capacitor with a value of at least 1 µF of effective capacitance on the PVIN pin, relative to PGND. The power stage input decoupling capacitance (effective capacitance at the PVIN and PGND pins) must be sufficient to supply the high switching currents demanded when the high-side MOSFET switches on, while providing minimal input voltage ripple as a result. This effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated by Equation 4.

$$I_{CIN(rms)} = I_{OUT(max)} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = 2.8\ Amps \quad (4)$$

The minimum input capacitance and ESR values for a given input voltage ripple specification, $V_{IN(ripple)}$, are shown in Equation 5. The input ripple is composed of a capacitive portion, $V_{IN(RIPPLE\_CAP)}$, and a resistive portion, $V_{IN(RIPPLE\_ESR)}$.

$$C_{IN(min)} = \frac{I_{OUT(max)} \times (1 - D) \times D}{V_{IN(RIPPLE\_CAP)} \times f_{SW}} = 6.4\ \mu F$$

$$ESR_{CIN(max)} = \frac{V_{IN(RIPPLE\_ESR)}}{I_{OUT(max)} + \frac{I_{RIPPLE}}{2}} = 8.5\ m\Omega$$

where

- D is the duty cycle

(5)

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The input capacitor must also be selected with the DC bias taken into account. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. For this design, allow 0.1-V input ripple for $V_{IN(RIPPLE\_CAP)}$, and 0.1-V input ripple for $V_{IN(RIPPLE\_ESR)}$. UsingEquation 5, the minimum input capacitance for this design is 6.4 µF, and the maximum ESR is 8.5 mΩ. In a real application, it is recommended to use a combination of small capacitors such as 0.1-µF and larger value 10-µF or 22-µF ceramic capacitors in parallel for the power stage.

8.2.1.2.6 Bootstrap Capacitor Selection

A ceramic capacitor with a value of 0.1 µF must be connected between the BOOT and SW pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. Use a capacitor with a voltage rating of 25 V or higher.

8.2.1.2.7 R-C Snubber and VIN Pin High-Frequency Bypass

Though it is possible to operate the TPS542A52 within absolute maximum ratings without voltage ringing reduction techniques, some designs can require external components to further reduce ringing levels. This example uses two approaches: a high frequency power stage bypass capacitor on the VIN pins, and an R-C snubber between the SW area and GND.

The high-frequency VIN bypass capacitor is a lossless ringing reduction technique which helps minimize the outboard parasitic inductances in the power stage, which store energy during the high-side MOSFET on-time,

and discharge once the high-side MOSFET is turned off. For this example two of 0.1-µF to 1-µF, 25-V, 0402-sized high-frequency capacitors are used. The placement of these capacitors is critical to its effectiveness.

Additionally, an optional R-C snubber circuit is added to this example. To balance efficiency and spike levels, a 220-pF capacitor and a 2-Ω resistor are chosen. In this example, a 0805-sized resistor is chosen, which is rated for 0.125 W, nearly twice the estimated power dissipation. It is recommended for the R-C snubber circuit to sustain the ringing levels 2-V below the *Absolute Maximum Ratings* at room temperature. See the *Seminar 900 Topic 2 - Snubber Circuits: Theory, Design and Application* application note for more information about snubber circuits.

8.2.1.2.8 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor affects three criteria:

- Stability
- Regulator response to a change in load current or load transient
- Output voltage ripple

These three considerations are important when designing regulators that must operate where the electrical conditions are unpredictable. The output capacitance needs to be selected based on the most stringent of these three criteria.

8.2.1.2.9 Response to a Load Transient

The output capacitance must supply the load with the required current when current is not immediately provided by the regulator. When the output capacitor supplies load current, the impedance of the capacitor greatly affects the magnitude of voltage deviation (such as undershoot and overshoot) during the transient.

Use Equation 6 and Equation 7 to calculate the minimum output capacitance to meet the undershoot and overshoot requirements. For this example, $C_{OUT(min\_under)}$ is 136-µF and 92-µF for $C_{OUT(min\_over)}$. In a real application, the value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. It is recommended to check the capacitor datasheet and account for the capacitance derating.

$$C_{OUT(min\_under)} = \frac{L \times \Delta I_{LOAD(max)}^{2}}{2 \times \Delta V_{LOAD(INSERT)} \times (V_{IN}-V_{VOUT})} + \frac{\Delta I_{LOAD(max)} \times (1-D) \times t_{SW}}{\Delta V_{LOAD(INSERT)}} \quad (6)$$

$$C_{OUT(min\_over)} = \frac{L_{OUT} \times \left(\Delta I_{LOAD(max)}\right)^{2}}{2 \times \Delta V_{LOAD(release)} \times V_{OUT}} \quad (7)$$

where

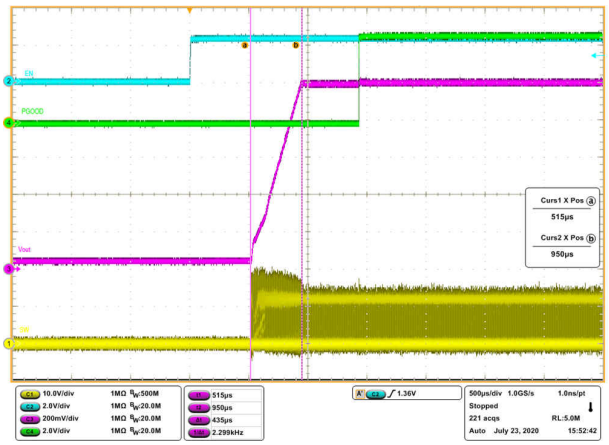
- $C_{OUT(min\_under)}$ is the minimum output capacitance to meet the undershoot requirement
- $C_{OUT(min\_over)}$ is the minimum output capacitance to meet the overshoot requirement
- D is the duty cycle
- L is the output inductance value (0.22 µH)
- $\Delta I_{LOAD(max)}$ is the maximum transient step (5 A)
- V_{OUT} is the output voltage value (1 V)
- t_{SW} is the switching period (0.833 µs)
- V_{IN} is the minimum input voltage for the design (12 V)
- $\Delta V_{LOAD(insert)}$ is the undershoot requirement (30 mV)
- $\Delta V_{LOAD(release)}$ is the overshoot requirement (30 mV)

8.2.1.2.10 Pin-Strap Setting

For overcurrent protection at 16.5 A, 47.5 kΩ is chosen from Table 7-7. For 0.5-ms soft start and FCCM operation, 47.5 kΩ is chosen from Table 7-5 and Table 7-6.

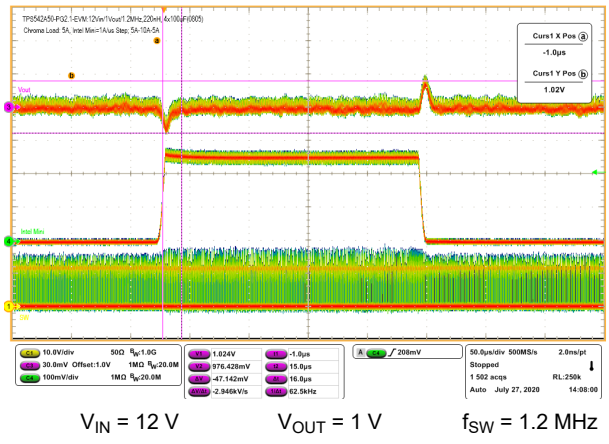
For converter stability and selecting the compensation network, Table 7-3 provides four compensation choices. First, the power stage double pole filter frequency needs to be known. For this example, the output capacitor bank selects as 4x100-µF ceramic capacitors in 0805 size to account the capacitor derating factors. Next, the LC filter frequency is calculated to 17 kHz. Finally, COMP3 becomes the best choice to select by using a 26.1-kΩ or 78.7-kΩ resistor on the COMP pin to GND.

8.2.1.3 Application Curves



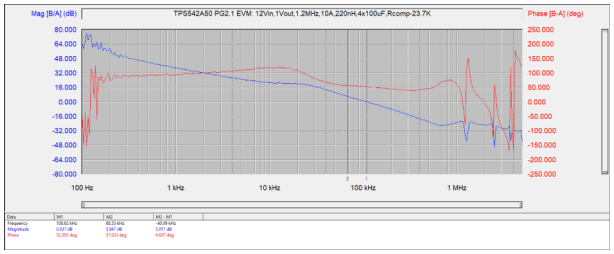
V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.2 MHz

Figure 8-2. 450 µs Start-up by EN at 0-A Output Current



V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.2 MHz

Figure 8-3. Load Transient 5 A to 10 A to 5 A at 1 A/µs



V_{IN} = 12 V V_{OUT} = 1 V f_{SW} = 1.2 MHz

Figure 8-4. Bode Plot at 10-A Output Current

8.2.1.4 Typical Application Circuits

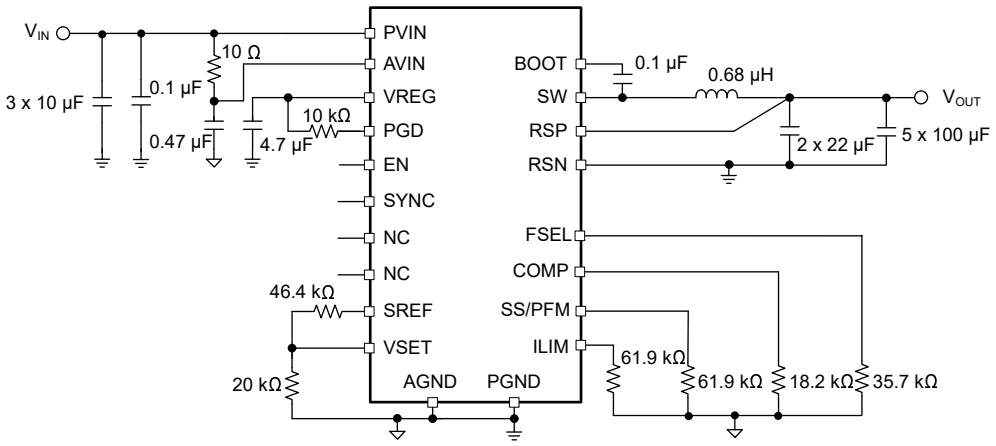


Figure 8-5. Typical Application Circuit for 1.8-V Output at 1.0 MHz

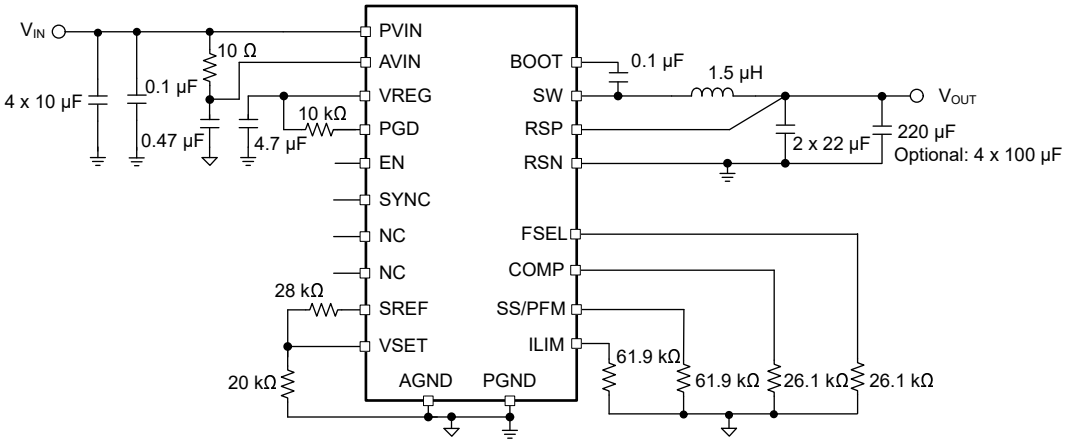


Figure 8-6. Typical Application Circuit for 2.5-V Output at 0.8 MHz

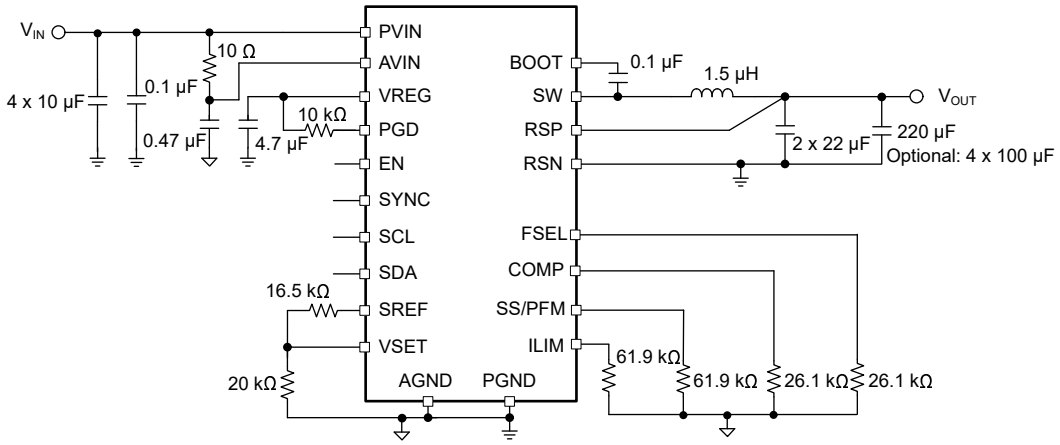


Figure 8-7. Typical Application Circuit for 3.3-V Output at 0.8 MHz

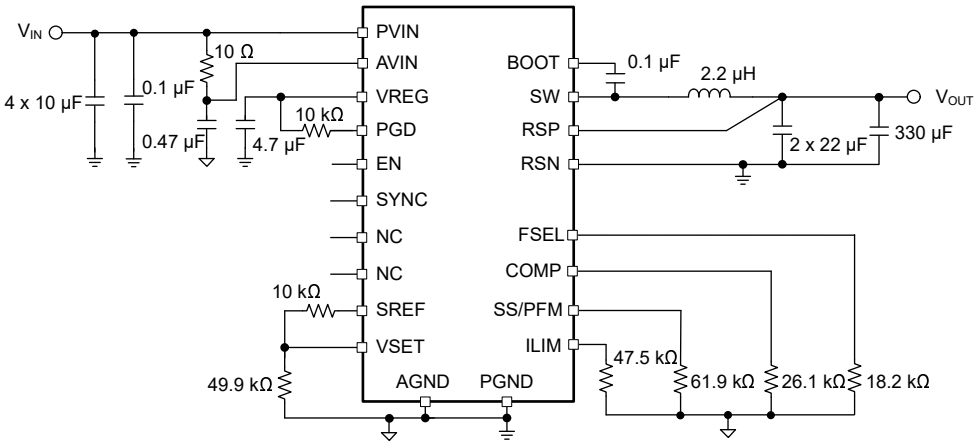


Figure 8-8. Typical Application Circuit for 5-V Output at 0.6 MHz

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4 V and 18 V. This input supply must be well regulated. Proper bypassing of input supplies (AVIN and PVIN) is critical for noise performance, as is the PCB layout and grounding scheme. See the recommendations in *Section 10*.

10 Layout

10.1 Layout Guidelines

1. The PVIN pins are the power inputs to the main half bridge and AVIN is the power input to the controller.
2. Connect AVIN and PVIN together on the PCB. It is important that these pins are at the same voltage potential because the controller feedforward block uses this voltage information in the modulator to increase transient performance. For AVIN, it is best to use RC filter from PVIN such as 10 Ω and 100 nF.
3. To minimize the power loop inductance for the half bridge, place the bypassing capacitors as close as possible to the PVIN pins on the converter. When using a multilayer PCB (more than two layers), the power loop inductance is minimized by having the return path to the input capacitor small and directly underneath the first layer as shown below. Loop inductance is reduced due to flux cancellation as the return current is directly underneath and flowing in the opposite direction.
4. Place the bias capacitor for VREG pin as close as possible to the pin as shown below.
5. The resistor divider network for SREF and VSET needs to placed as close as possible to the pins. Limit the high frequency noise source coupling onto these components.
6. RSP and RSN signals are best to route parallel to the load sense location. It is recommended to limit high frequency noise source coupling onto these traces.
7. PGND thermal vias: It is recommended to add vias under and outside the IC of PGND plane as shown below.
8. AGND thermal vias: It is recommended to add at least 2 vias under the IC of AGND plane as shown below.
9. AGND plane can be routed as separate island in an internal layer. AGND can connect as a net tied to PGND between the two thermal grounds under the IC as shown below.
10. Total PCB area can be routed in 17 mm by 14 mm as shown below. See the EVM userguide for more details.

10.2 Layout Example

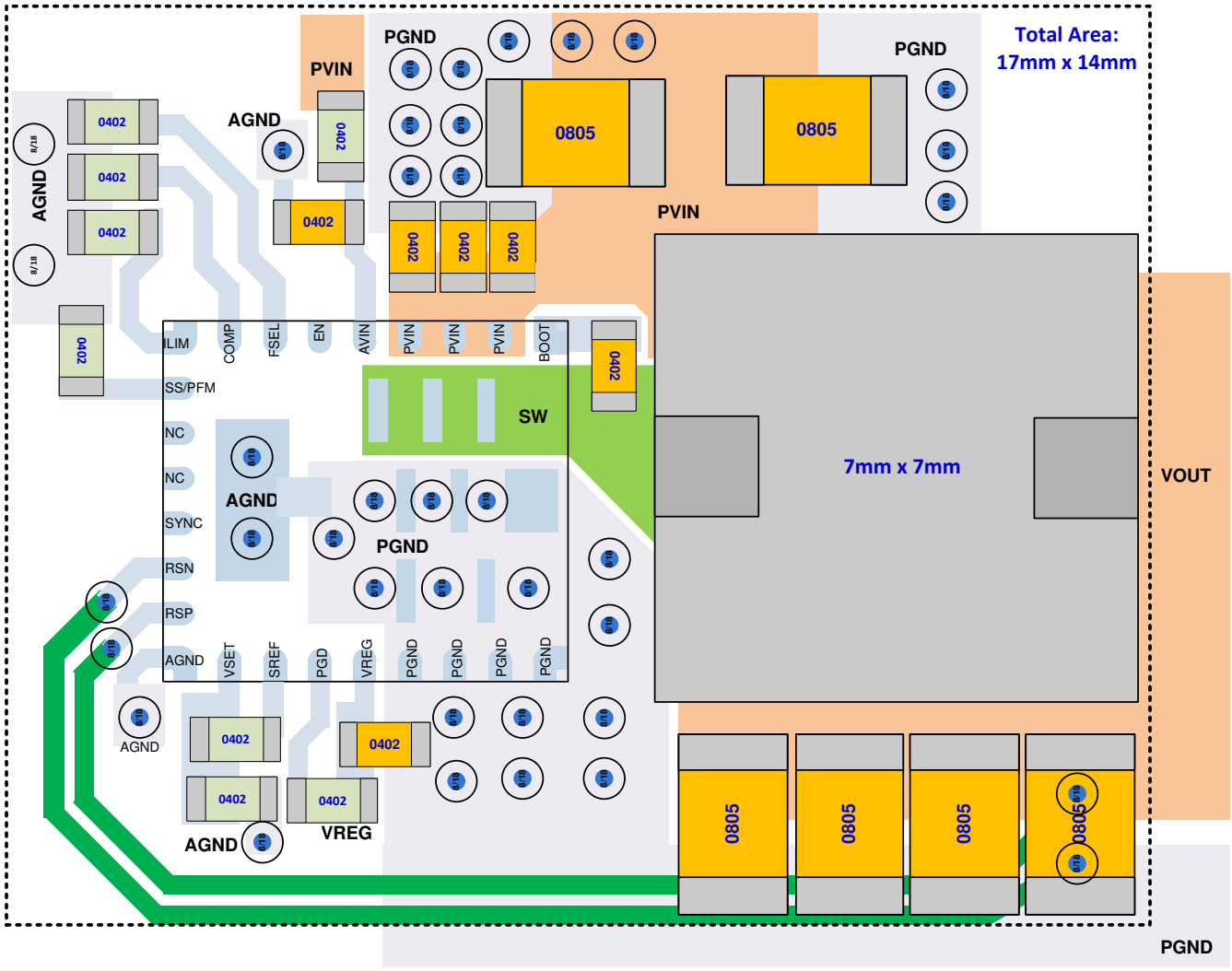


Figure 10-1. Example PCB Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS542A52 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS542A52RJMR	Active	Production	VQFN-HR (RJM) | 33	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	542A52
TPS542A52RJMR.A	Active	Production	VQFN-HR (RJM) | 33	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	542A52
TPS542A52RJMR.B	Active	Production	VQFN-HR (RJM) | 33	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

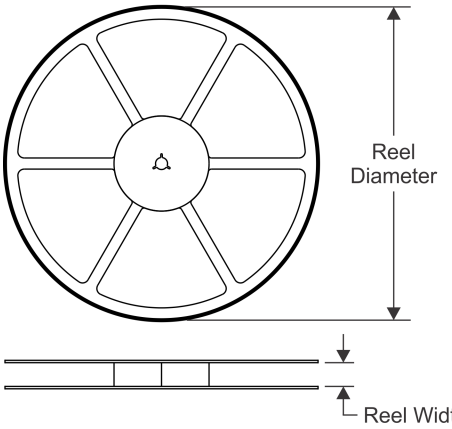
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

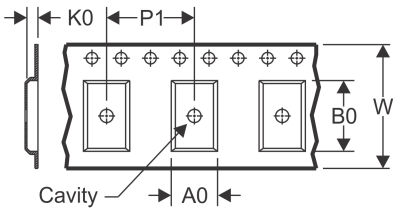
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

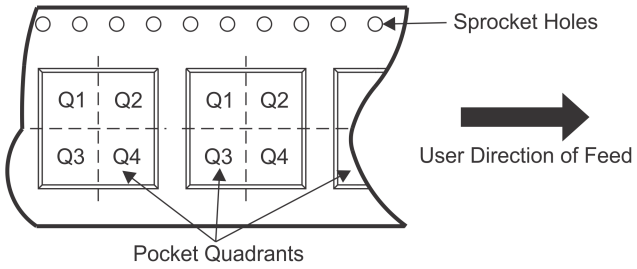


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

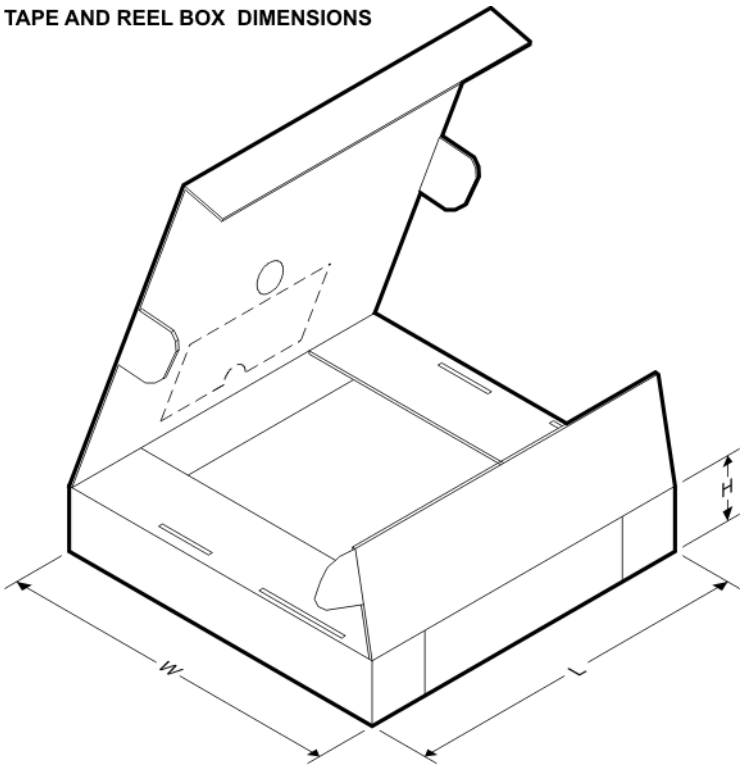
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS542A52RJMR	VQFN-HR	RJM	33	3000	330.0	12.4	4.25	4.75	1.2	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

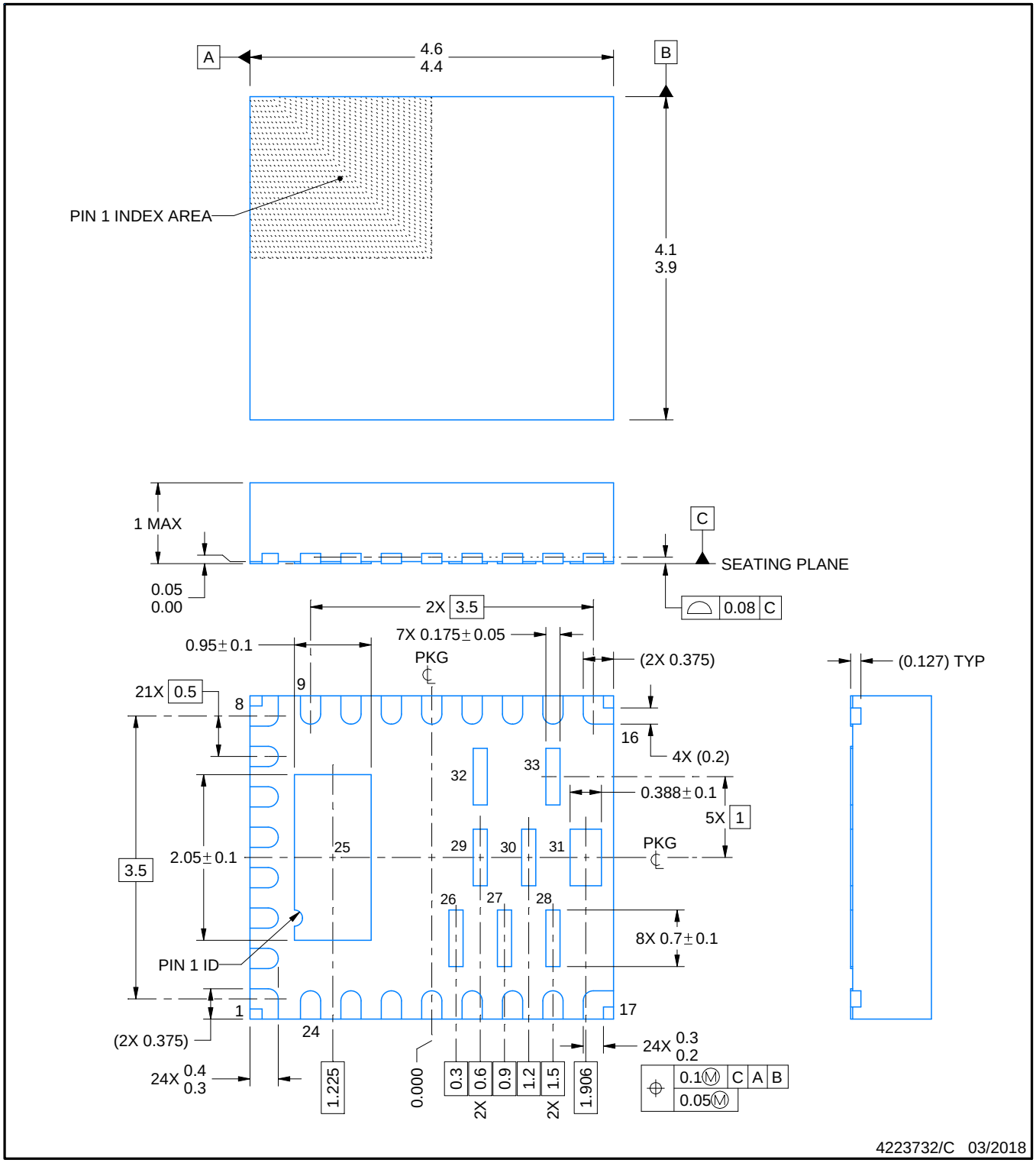
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS542A52RJMR	VQFN-HR	RJM	33	3000	367.0	367.0	38.0

PACKAGE OUTLINE

RJM0033A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

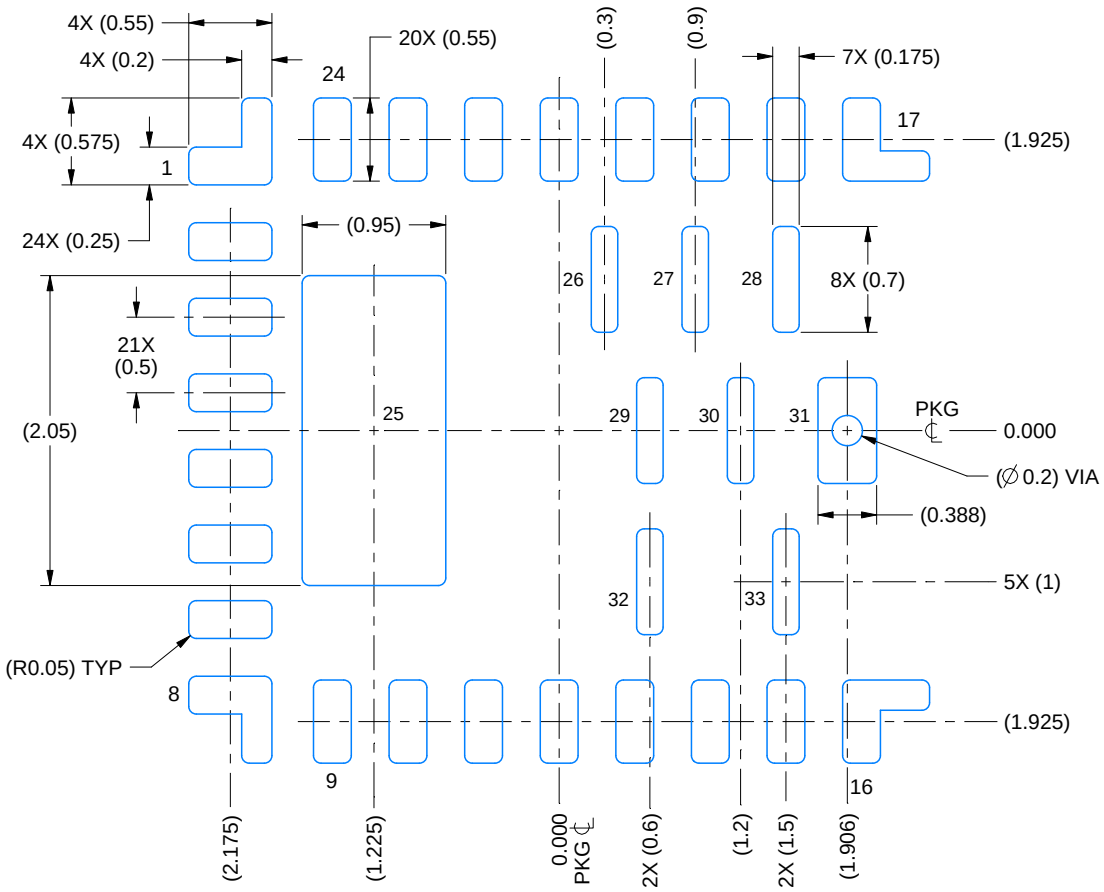
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

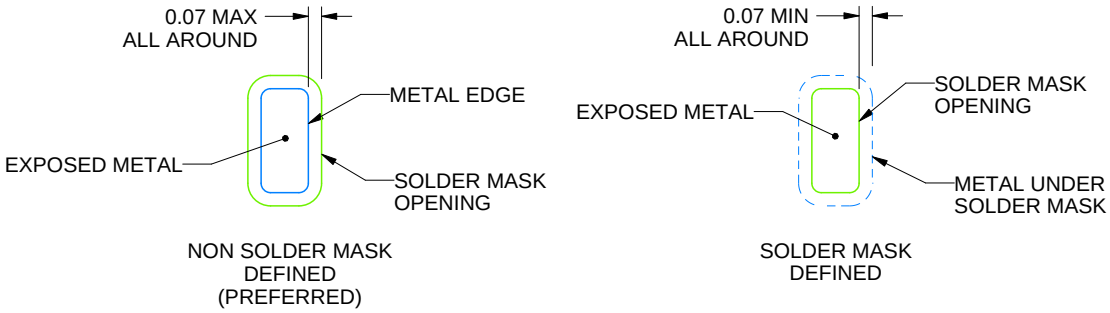
RJM0033A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

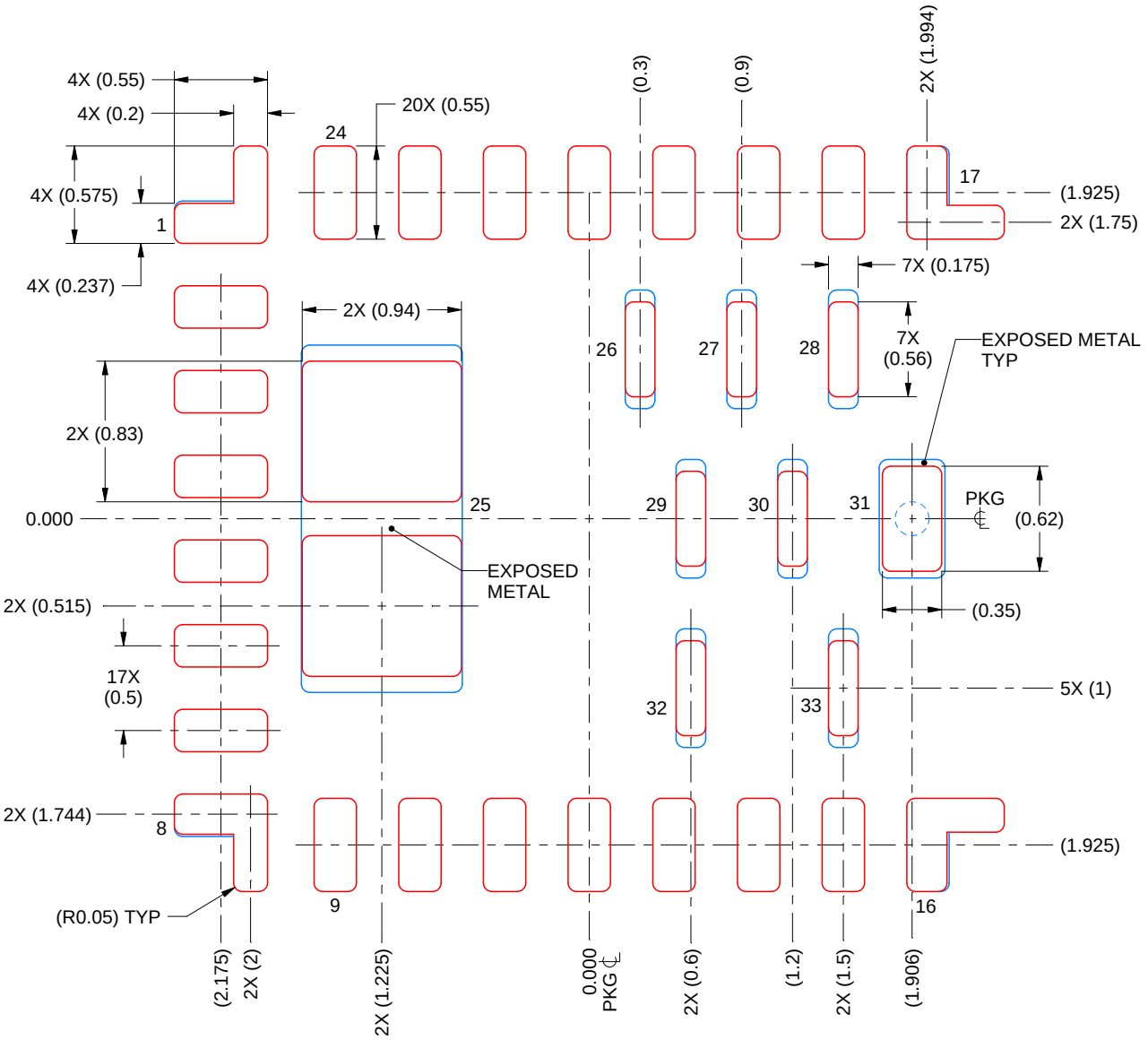
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RJM0033A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 8, 16, 17: 95%; PADS 25-33: 80%
SCALE:25X

4223732/C 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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