

TPS51100 3-A Sink / Source DDR Termination Regulator

1 Features

- Input Voltage Range: 4.75 V to 5.25 V
- VLDOIN Voltage Range: 1.2 V to 3.6 V
- 3-A Sink/Source Termination Regulator Includes Droop Compensation
- Requires Only 20- $\mu$ F Ceramic Output Capacitance
- Supports Hi-Z in S3 and Soft-Off in S5
- 1.2-V Input (VLDOIN) Helps Reduce Total Power Dissipation
- Integrated Divider Tracks 0.5 VDDQSNS for VTT and VTTREF
- Remote Sensing (VTTSNS)
- $\pm$ 20-mV Accuracy for VTT and VTTREF
- 10-mA Buffered Reference (VTTREF)
- Built-In Soft-Start, UVLO, and OCL
- Thermal Shutdown
- Supports JEDEC Specifications

2 Applications

- DDR, DDR2, DDR3 Memory Termination
- SSTL-2, SSTL-18, and HSTL Termination

3 Description

The TPS51100 is a 3-A, sink/source tracking termination regulator. The device is specifically designed for low-cost and low-external component count systems where space is a premium.

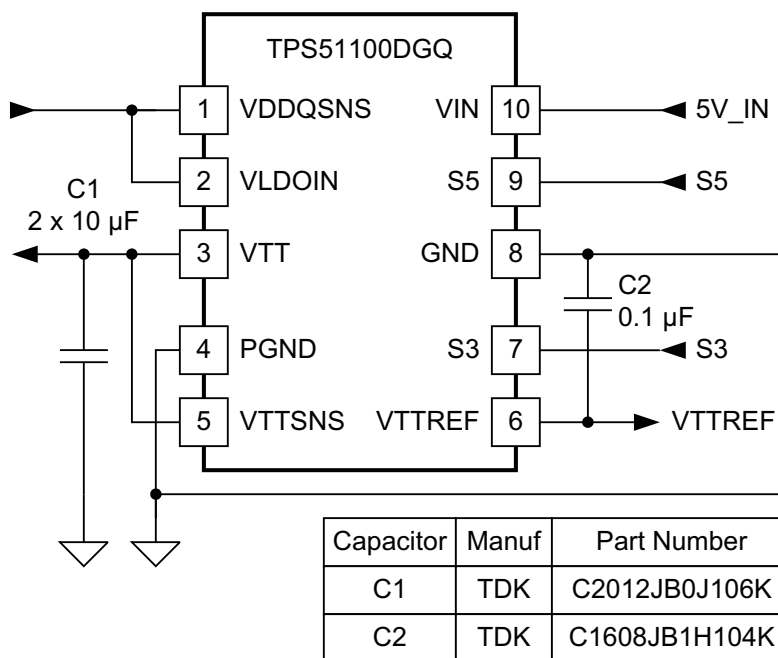
The TPS51100 maintains fast transient response, only requiring 20  $\mu$ F ( $2 \times 10 \mu$ F) of ceramic output capacitance. The TPS51100 supports remote sensing functions and all features required to power the DDR and DDR2 VTT bus termination according to the JEDEC specification. The part also supports DDR3 VTT termination with VDDQ at 1.5 V (typical). In addition, the TPS51100 includes integrated sleep-state controls, placing VTT in Hi-Z in S3 (suspend to RAM) and soft-off for VTT and VTTREF in S5 (suspend to disk). The TPS51100 is available in the thermally efficient 10-pin MSOP PowerPAD™ package and is specified from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE     | BODY SIZE (NOM)   |
|-------------|-------------|-------------------|
| TPS51100    | HVSSOP (10) | 3.00 mm x 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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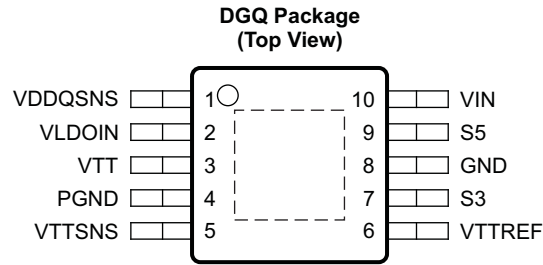
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (May 2012) to Revision E                                                                                                                                                                                                                                                                                                                                                                          | Page     |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| <ul style="list-style-type: none"> <li>Added <i>Pin Configuration and Functions</i> section, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul> | <b>1</b> |

| Changes from Revision C (June 2008) to Revision D                                  | Page     |
|------------------------------------------------------------------------------------|----------|
| <ul style="list-style-type: none"> <li>Added updated Thermal data .....</li> </ul> | <b>4</b> |

## 5 Pin Configuration and Functions



Actual Size  
3,05 mm x 4,98 mm

P0083-01

NOTE: For more information on the DGQ package, see the *PowerPAD Thermally Enhanced Package* application report (SLMA002).

### Pin Functions

| PIN     |     | I/O | DESCRIPTION                                                                            |
|---------|-----|-----|----------------------------------------------------------------------------------------|
| NAME    | NO. |     |                                                                                        |
| GND     | 8   | –   | Signal ground. Connect to negative terminal of the output capacitor                    |
| PGND    | 4   | –   | Power ground output for the VTT LDO                                                    |
| S3      | 7   | I   | S3 signal input                                                                        |
| S5      | 9   | I   | S5 signal input                                                                        |
| VDDQSNS | 1   | I   | VDDQ sense input                                                                       |
| VIN     | 10  | I   | 5-V power supply                                                                       |
| VLDOIN  | 2   | I   | Power supply for the VTT LDO and VTTREF output stage                                   |
| VTT     | 3   | O   | Power output for the VTT LDO                                                           |
| VTTREF  | 6   | O   | VTT reference output. Connect to GND through 0.1-μF ceramic capacitor.                 |
| VTTSNS  | 5   | I   | Voltage sense input for the VTT LDO. Connect to plus terminal of the output capacitor. |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                               |                                      | MIN  | MAX | UNIT |
|-------------------------------|--------------------------------------|------|-----|------|
| Input voltage <sup>(2)</sup>  | VIN, VLDOIN, VTTSNS, VDDQSNS, S3, S5 | –0.3 | 6   | V    |
|                               | PGND                                 | –0.3 | 0.3 |      |
| Output voltage <sup>(2)</sup> | VTT, VTTREF                          | –0.3 | 6   | V    |
| T <sub>A</sub>                | Operating ambient temperature        | –40  | 85  | °C   |
| T <sub>stg</sub>              | Storage temperature                  | –55  | 150 | °C   |

- (1) Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal unless otherwise noted.

### 6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                 |                                | MIN   | MAX  | UNIT |
|-----------------|--------------------------------|-------|------|------|
| V <sub>IN</sub> | Supply voltage                 | 4.75  | 5.25 | V    |
| Voltage range   | S3, S5                         | –0.10 | 5.25 | V    |
|                 | VLDOIN, VDDQSNS, VTT, VTTSNS   | –0.1  | 3.6  |      |
|                 | VTTREF                         | –0.1  | 1.8  |      |
|                 | PGND                           | –0.1  | 0.1  |      |
| T <sub>A</sub>  | Operating free-air temperature | –40   | 85   | °C   |

### 6.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TPS51100 | UNIT |
|-------------------------------|----------------------------------------------|----------|------|
|                               |                                              | DGQ      |      |
|                               |                                              | 10 PINS  |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 60.3     | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 63.5     |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 51.6     |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 1.5      |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 22.3     |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 9.5      |      |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.4 Electrical Characteristics

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{\text{VIN}} = 5\text{ V}$ , VLDOIN and VDDQSNS are connected to 2.5 V (unless otherwise noted)

| PARAMETER                |                                               | TEST CONDITIONS                                                                                                                                   | MIN                     | TYP   | MAX | UNIT |
|--------------------------|-----------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-------|-----|------|
| SUPPLY CURRENT           |                                               |                                                                                                                                                   |                         |       |     |      |
| I <sub>VIN</sub>         | Supply current, VIN                           | T <sub>A</sub> = 25°C, V <sub>VIN</sub> = 5 V, no load, V <sub>S3</sub> = V <sub>S5</sub> = 5 V                                                   | 0.25                    | 0.5   | 1   | mA   |
| I <sub>VINSTB</sub>      | Standby current, VIN                          | T <sub>A</sub> = 25°C, V <sub>VIN</sub> = 5 V, no load, V <sub>S3</sub> = 0 V, V <sub>S5</sub> = 5 V                                              | 25                      | 50    | 80  | µA   |
| I <sub>VINSN</sub>       | Shutdown current, VIN                         | T <sub>A</sub> = 25°C, V <sub>VIN</sub> = 5 V, no load, V <sub>S3</sub> = V <sub>S5</sub> = 0 V, V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 0 V |                         | 0.3   | 1   | µA   |
| I <sub>VLDOIN</sub>      | Supply current, VLDOIN                        | T <sub>A</sub> = 25°C, V <sub>VIN</sub> = 5 V, no load, V <sub>S3</sub> = V <sub>S5</sub> = 5 V                                                   | 0.7                     | 1.2   | 2   | mA   |
| I <sub>VLDOINSTB</sub>   | Standby current, VLDOIN                       | T <sub>A</sub> = 25°C, V <sub>VIN</sub> = 5 V, no load, V <sub>S3</sub> = 0 V, V <sub>S5</sub> = 5 V                                              |                         | 6     | 10  | µA   |
| I <sub>VLDOINSN</sub>    | Shutdown current, VLDOIN                      | T <sub>A</sub> = 25°C, V <sub>VIN</sub> = 5 V, no load, V <sub>S3</sub> = V <sub>S5</sub> = 0 V                                                   |                         | 0.3   | 1   | µA   |
| INPUT CURRENT            |                                               |                                                                                                                                                   |                         |       |     |      |
| I <sub>VDDQSNS</sub>     | Input current, VDDQSNS                        | V <sub>VIN</sub> = 5 V, V <sub>S3</sub> = V <sub>S5</sub> = 5 V                                                                                   | 1                       | 3     | 5   | µA   |
| I <sub>VTTSNS</sub>      | Input current, VTTSNS                         | V <sub>VIN</sub> = 5 V, V <sub>S3</sub> = V <sub>S5</sub> = 5 V                                                                                   | –1                      | –0.25 | 1   | µA   |
| VTT OUTPUT               |                                               |                                                                                                                                                   |                         |       |     |      |
| V <sub>VTTSNS</sub>      | Output voltage, VTT                           | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 2.5 V                                                                                                | 1.25                    |       |     | V    |
|                          |                                               | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 1.8 V                                                                                                | 0.9                     |       |     |      |
|                          |                                               | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 1.5 V                                                                                                | 0.75                    |       |     |      |
| V <sub>VTTTOL25</sub>    | Output voltage tolerance to VTTREF, VTT       | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 2.5 V,  I <sub>VTT</sub>   = 0 A                                                                     | –20                     |       | 20  | mV   |
|                          |                                               | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 2.5 V,  I <sub>VTT</sub>   = 1.5 A                                                                   | –30                     |       | 30  |      |
|                          |                                               | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 2.5 V,  I <sub>VTT</sub>   = 3 A                                                                     | –40                     |       | 40  |      |
| V <sub>VTTTOL18</sub>    |                                               | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 1.8 V,  I <sub>VTT</sub>   = 0 A                                                                     | –20                     |       | 20  |      |
|                          |                                               | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 1.8 V,  I <sub>VTT</sub>   = 1 A                                                                     | –30                     |       | 30  |      |
|                          |                                               | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 1.8 V,  I <sub>VTT</sub>   = 2 A                                                                     | –40                     |       | 40  |      |
| V <sub>VTTTOL15</sub>    |                                               | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 1.5 V,  I <sub>VTT</sub>   = 0 A                                                                     | –20                     |       | 20  |      |
|                          |                                               | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 1.5 V,  I <sub>VTT</sub>   = 1 A                                                                     | –30                     |       | 30  |      |
| I <sub>VTTCLSRC</sub>    | Source current limit, VTT                     | $V_{TT} = \left( \frac{V_{VDDQSNS}}{2} \right) \times 0.95$ , PGOOD = High                                                                        | 3                       | 3.8   | 6   | A    |
|                          |                                               | V <sub>VTT</sub> = 0 V                                                                                                                            | 1.5                     | 2.2   | 3   |      |
| I <sub>VTTCLSNK</sub>    | Sink current limit, VTT                       | $V_{TT} = \left( \frac{V_{VDDQSNS}}{2} \right) \times 1.05$ , PGOOD = High                                                                        | 3                       | 3.6   | 6   | A    |
|                          |                                               | V <sub>VTT</sub> = V <sub>VDDQ</sub>                                                                                                              | 1.5                     | 2.2   | 3   |      |
| I <sub>VTTLK</sub>       | Leakage current, VTT                          | $V_{TT} = \left( \frac{V_{VDDQSNS}}{2} \right) \times 1.25$ V, T <sub>A</sub> = 25°C                                                              | –1                      | 0.5   | 10  | µA   |
|                          |                                               | V <sub>S3</sub> = 0 V, V <sub>S5</sub> = 5 V                                                                                                      |                         |       |     |      |
| I <sub>VTTSNSLK</sub>    | Leakage current, VTTSNS                       | $V_{TT} = \left( \frac{V_{VDDQSNS}}{2} \right) \times 1.25$ V, T <sub>A</sub> = 25°C                                                              | –1                      | 0.01  | 1   | µA   |
| I <sub>DSCHRG</sub>      | Discharge current, VTT                        | T <sub>A</sub> = 25°C, V <sub>VDDQSNS</sub> = 0 V, V <sub>S3</sub> = V <sub>S5</sub> = 0 V, V <sub>VTT</sub> = 0.5 V                              | 10                      | 17    |     | mA   |
| VTTREF OUTPUT            |                                               |                                                                                                                                                   |                         |       |     |      |
| V <sub>VTTREF</sub>      | Output voltage, VTTREF                        |                                                                                                                                                   | $\frac{V_{VDDQSNS}}{2}$ |       |     | V    |
| V <sub>VTTREFTOL25</sub> | Output voltage tolerance to VDDQSNS/2, VTTREF | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 2.5 V, I <sub>VTTREF</sub> < 10 mA                                                                   | –20                     |       | 20  | mV   |
| V <sub>VTTREFTOL18</sub> |                                               | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 1.8 V, I <sub>VTTREF</sub> < 10 mA                                                                   | –17                     |       | 17  |      |
| V <sub>VTTREFTOL15</sub> |                                               | V <sub>VLDOIN</sub> = V <sub>VDDQSNS</sub> = 1.5 V, I <sub>VTTREF</sub> < 10 mA                                                                   | –15                     |       | 15  |      |
| I <sub>VTTREFOCI</sub>   | Source current limit, VTTREF                  | V <sub>VTTREF</sub> = 0 V                                                                                                                         | 10                      | 20    | 30  | mA   |

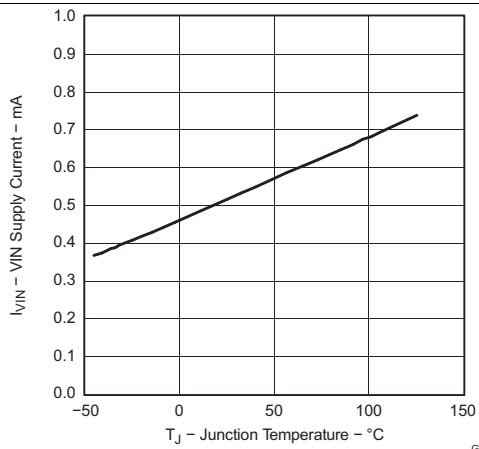
**TPS51100**

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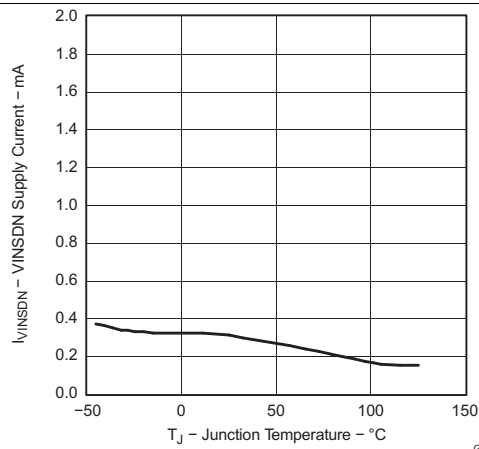
[www.ti.com](http://www.ti.com)
**Electrical Characteristics (continued)**
 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{\text{VIN}} = 5\text{ V}$ , VLDOIN and VDDQSNS are connected to 2.5 V (unless otherwise noted)

| PARAMETER                   |                             | TEST CONDITIONS                    | MIN  | TYP  | MAX  | UNIT               |
|-----------------------------|-----------------------------|------------------------------------|------|------|------|--------------------|
| <b>UVLO/LOGIC THRESHOLD</b> |                             |                                    |      |      |      |                    |
| $V_{\text{VINUV}}$          | UVLO threshold voltage, VIN | Wake up                            | 3.4  | 3.7  | 4    | V                  |
|                             |                             | Hysteresis                         | 0.15 | 0.25 | 0.35 |                    |
| $V_{\text{IH}}$             | High-level input voltage    | S3, S5                             | 1.6  |      |      | V                  |
| $V_{\text{IL}}$             | Low-level input voltage     | S3, S5                             |      |      | 0.3  | V                  |
| $V_{\text{IHYST}}$          | Hysteresis voltage          | S3, S5                             |      | 0.2  |      | V                  |
| $I_{\text{LEAK}}$           | Logic input leakage current | S2, S5, $T_A = 25^{\circ}\text{C}$ | –1   |      | 1    | $\mu\text{A}$      |
| <b>THERMAL SHUTDOWN</b>     |                             |                                    |      |      |      |                    |
| $T_{\text{SDN}}$            | Thermal shutdown threshold  | Shutdown temperature               |      | 160  |      | $^{\circ}\text{C}$ |
|                             |                             | Hysteresis                         |      | 10   |      |                    |

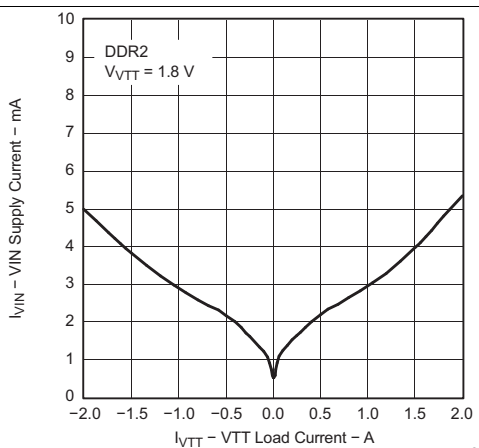
## 6.5 Typical Characteristics



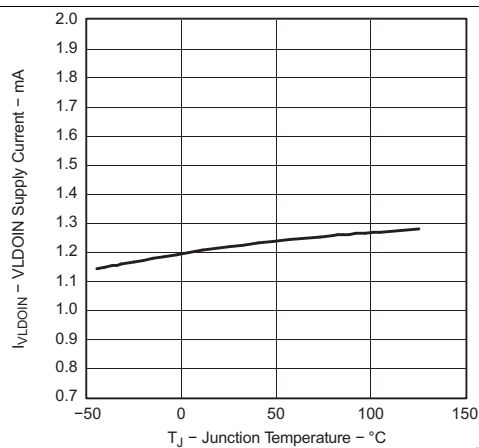
**Figure 1. VIN Supply Current vs Temperature**



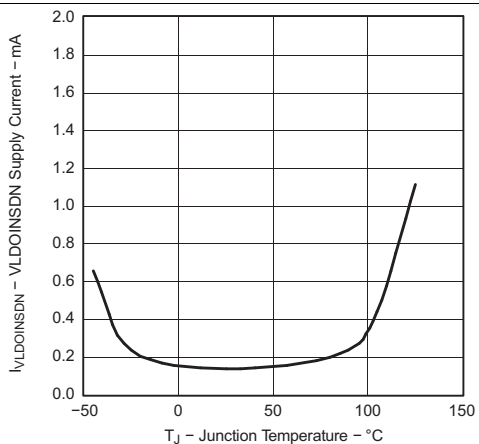
**Figure 2. VIN Shutdown Current vs Temperature**



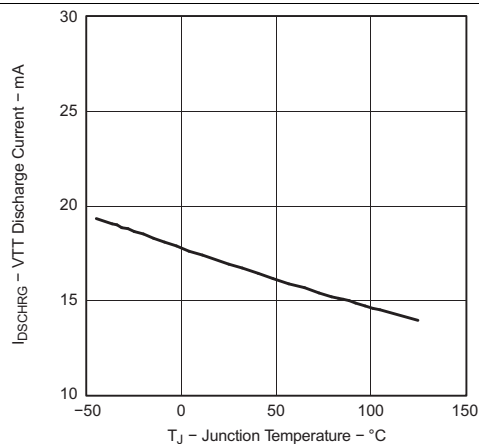
**Figure 3. VIN Supply Current vs VTT Load Current**



**Figure 4. VLDOIN Supply Current vs Temperature**



**Figure 5. VLDOIN Shutdown Current vs Temperature**



**Figure 6. Discharge Current vs Temperature**

## Typical Characteristics (continued)

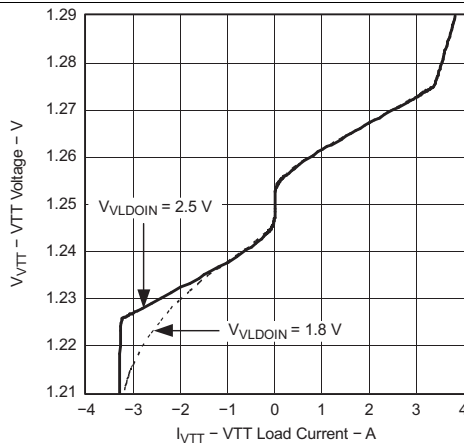


Figure 7. VTT Voltage Load Regulation vs VTT Load Current (DDR)

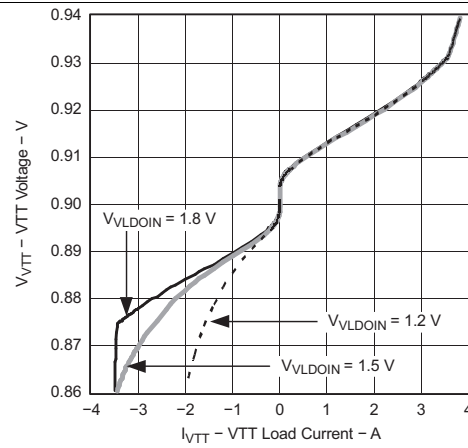


Figure 8. VTT Voltage Load Regulation vs VTT Load Current (DDR2)

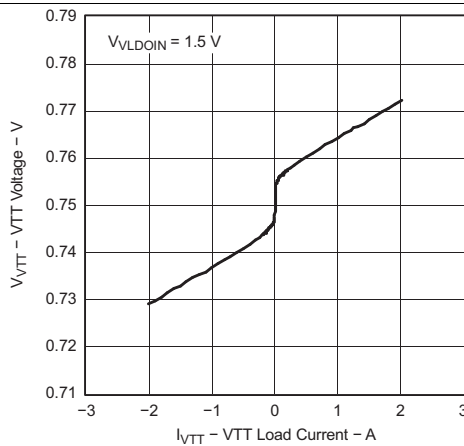


Figure 9. VTT Voltage Load Regulation vs VTT Load Current (DDR3)

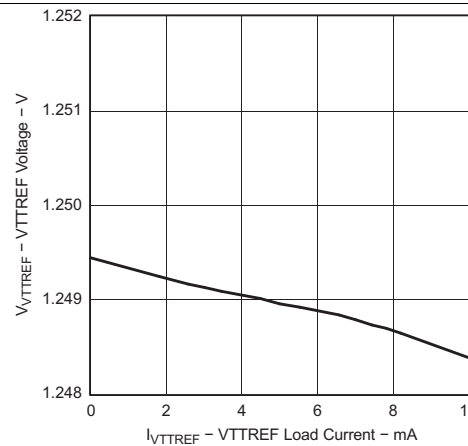


Figure 10. VTTREF Voltage Load Regulation vs VTTREF Load Current (DDR)

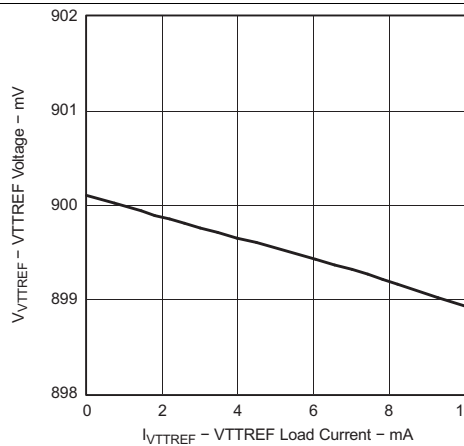


Figure 11. VTTREF Voltage Load Regulation vs VTTREF Load Current (DDR2)

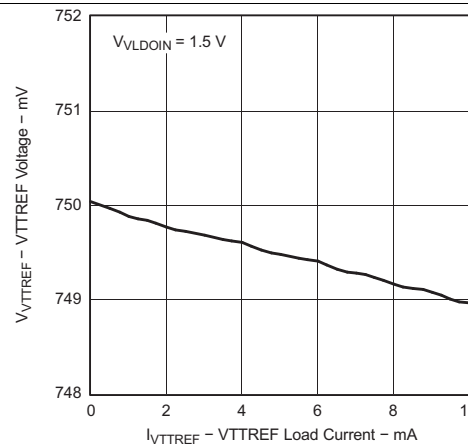
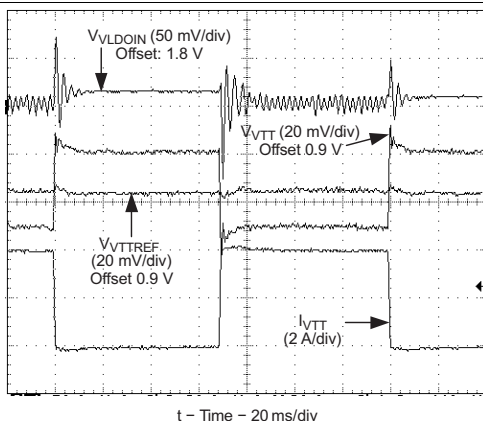
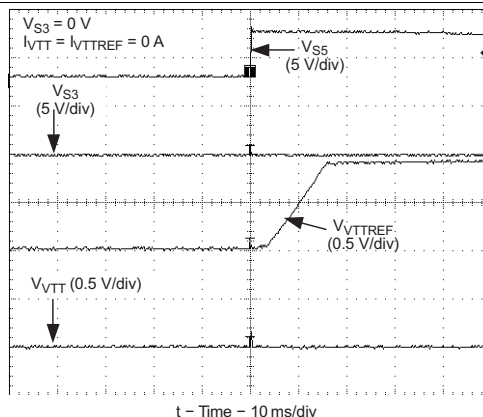


Figure 12. VTTREF Voltage Load Regulation vs VTTREF Load Current (DDR3)

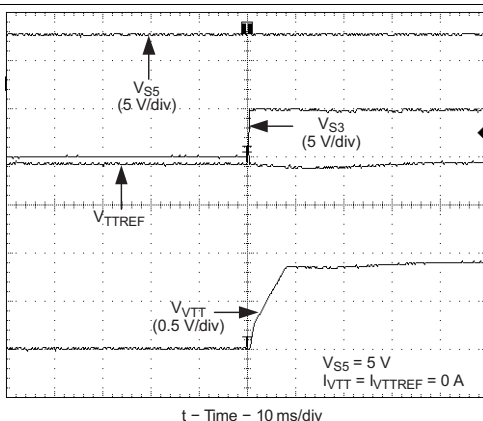
## Typical Characteristics (continued)



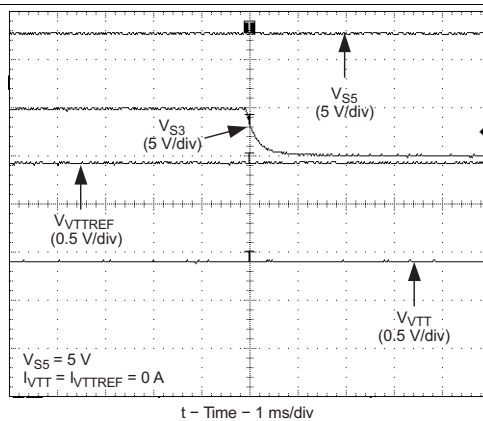
**Figure 13. VTT Voltage Load Transient Response**



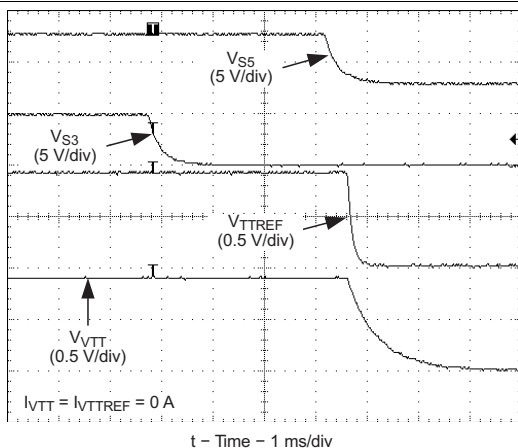
**Figure 14. Startup Waveforms S5 Low-to-High**



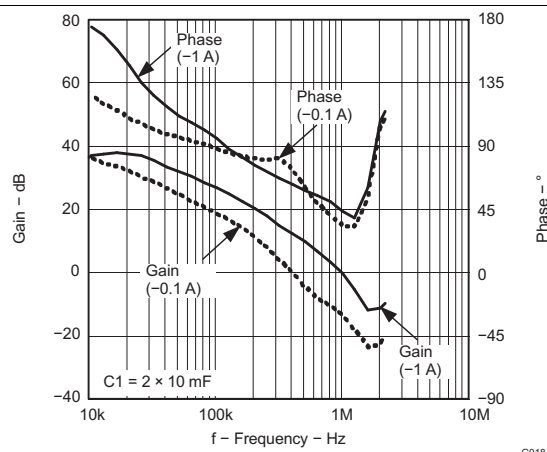
**Figure 15. Startup Waveforms S3 Low-to-High**



**Figure 16. Shutdown Waveforms S3 High-to-Low**



**Figure 17. Shutdown Waveforms S3 and S5 High-to-Low**



**Figure 18. Bode Plot DDR Source**

## Typical Characteristics (continued)

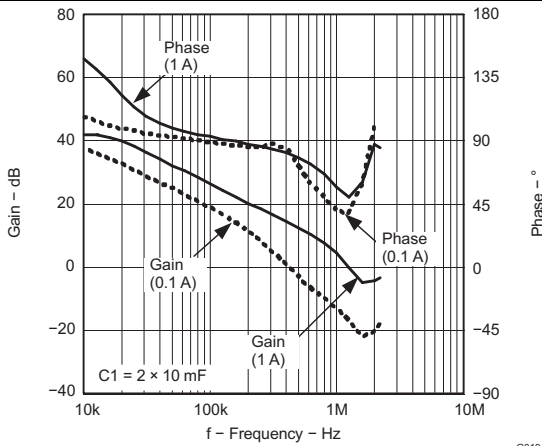


Figure 19. Bode Plot DDR Sink

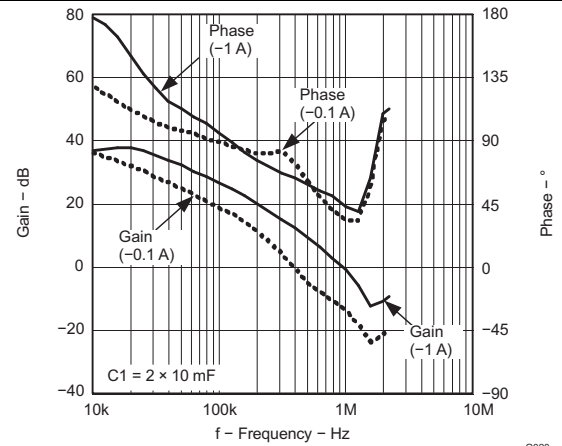


Figure 20. Bode Plot DDR2 Source

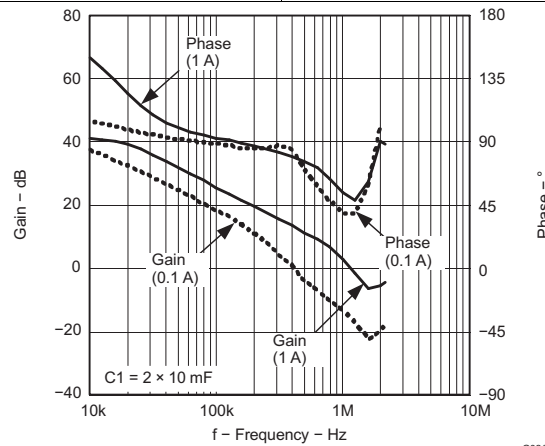


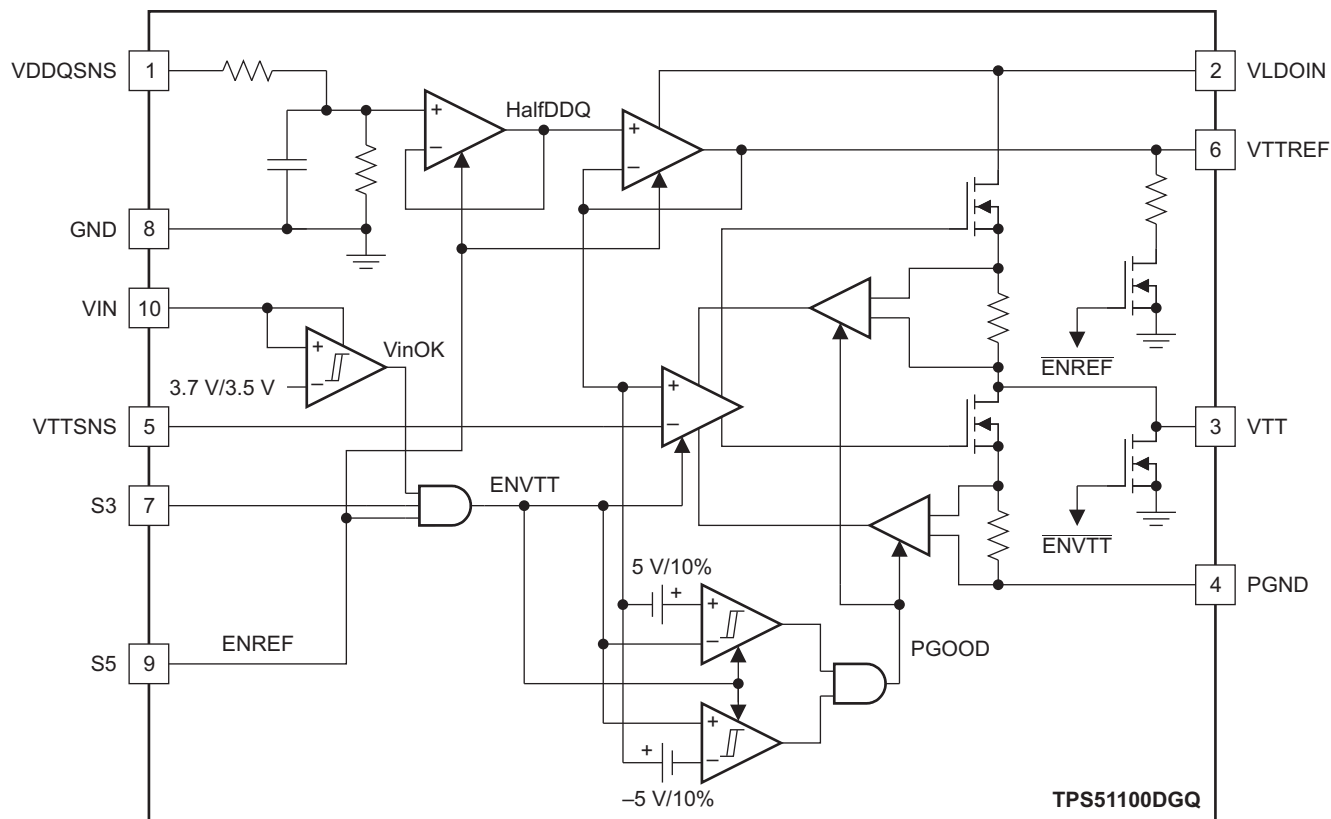
Figure 21. Bode Plot DDR2 Sink

## 7 Detailed Description

### 7.1 Overview

The TPS51100 is a sink / source double data rate (DDR) termination regulator with VTTREF buffered reference output.

### 7.2 Functional Block Diagram



B0319-01

Figure 22. Simplified Block Diagram

### 7.3 Feature Description

#### 7.3.1 VTT Sink/Source Regulator

The TPS51100 is a 3-A sink/source tracking termination regulator designed specially for low-cost, low-external-components systems where space is at premium, such as notebook PC applications. The TPS51100 integrates a high-performance, low-dropout linear regulator that is capable of sourcing and sinking current up to 3 A. This VTT linear regulator employs an ultimate fast-response feedback loop so that small ceramic capacitors are enough to keep tracking to the VTTREF within  $\pm 40$  mV under all conditions, including fast load transient. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, VTTSENS, should be connected to the positive node of the VTT output capacitor(s) as a separate trace from the high-current line from VTT.

#### 7.3.2 VTTREF Regulator

The VTTREF block consists of an on-chip 1/2 divider, low-pass filter (LPF), and buffer. This regulator can source current up to 10 mA. Bypass VTTREF to GND using a 0.1- $\mu$ F ceramic capacitor to ensure stable operation.

## Feature Description (continued)

### 7.3.3 Soft-Start

The soft-start function of the VTT is achieved via a current clamp, allowing the output capacitors to be charged with low and constant current that gives linear ramp-up of the output voltage. The current-limit threshold is changed in two stages using an internal powergood signal. When VTT is outside the powergood threshold, the current limit level is 2.2 A. When VTT rises above ( $V_{TTREF} - 5\%$ ) or falls below ( $V_{TTREF} + 5\%$ ), the current limit level switches to 3.8 A. The thresholds are typically  $V_{TTREF} \pm 5\%$  (from outside regulation to inside) and  $\pm 10\%$  (when it falls outside). The soft-start function is completely symmetrical, and it works not only from GND to  $V_{TTREF}$  voltage, but also from  $V_{DDQ}$  to  $V_{TTREF}$  voltage. Note that the VTT output is in a high-impedance state during the S3 state ( $S3 = \text{low}$ ,  $S5 = \text{high}$ ), and its voltage can be up to  $V_{DDQ}$  voltage, depending on the external condition. Note that VTT does not start under a full-load condition.

### 7.3.4 VTT Current Protection

The LDO has a constant overcurrent limit (OCL) at 3.8 A. This trip point is reduced to 2.2 A before the output voltage comes within  $\pm 5\%$  of the target voltage or goes outside of  $\pm 10\%$  of the target voltage.

### 7.3.5 VIN UVLO Protection

For VIN undervoltage lockout (UVLO) protection, the TPS51100 monitors VIN voltage. When the VIN voltage is lower than UVLO threshold voltage, the VTT regulator is shut off. This is a non-latch protection.

### 7.3.6 Thermal Shutdown

TPS51100 monitors its temperature. If the temperature exceeds the threshold value, typically  $160^{\circ}\text{C}$ , the VTT and  $V_{TTREF}$  regulators are shut off. This is also a non-latch protection.

## 7.4 Device Functional Modes

### 7.4.1 S5 Control and Soft-Off

The S3 and S5 terminals should be connected to SLP\_S3 and SLP\_S5 signals, respectively. Both  $V_{TTREF}$  and VTT are turned on at the S0 state ( $S3 = \text{high}$ ,  $S5 = \text{high}$ ).  $V_{TTREF}$  is kept alive while VTT is turned off and left high-impedance in the S3 state ( $S3 = \text{low}$ ,  $S5 = \text{high}$ ). Both VTT and  $V_{TTREF}$  outputs are turned off and discharged to ground through internal MOSFETs during S4/S5 state (both S3 and S5 are low).

**Table 1. S3 and S5 Control Table**

| STATE                | S3 | S5 | $V_{TTREF}$   | VTT           |
|----------------------|----|----|---------------|---------------|
| S0                   | H  | H  | 1             | 1             |
| S3 <sup>(1)</sup>    | L  | H  | 1             | 0 (Hi-Z)      |
| S4/S5 <sup>(1)</sup> | L  | L  | 0 (discharge) | 0 (discharge) |

- (1) In case S3 is forced to H and S5 to L,  $V_{TTREF}$  is discharged and VTT is at Hi-Z state. This condition is not recommended.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS51100 is typically used as a sink / source tracking termination regulator, witch converter a voltage from VTT.

### 8.2 Typical Application

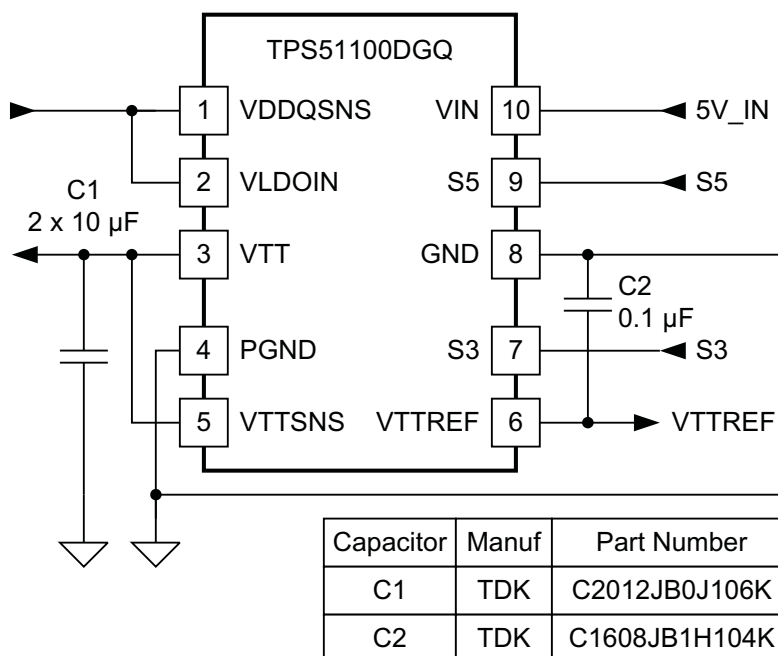


Figure 23. TPS51100 5-V Input / 1.8-V Output Reference Design

#### 8.2.1 Design Requirements

Table 2. Design Parameters

| DESIGN PARAMETERS | EXAMPLE VALUE    |
|-------------------|------------------|
| VIN               | 4.75 V to 5.25 V |
| VDDQSNS, VLDOIN   | 1.8 V            |
| Output Current    | ±3 A             |

#### 8.2.2 Detailed Design Procedure

Table 3. Design Specifications

| REFERENCE DESIGNATOR | SPECIFICATION                  | MANUFACTURER | PART NUMBER   |
|----------------------|--------------------------------|--------------|---------------|
| C1                   | 10-μf, 6.3-V, X5R, 1212 (0805) | TDK          | C2012JB0J106K |
| C2                   | 0.1-μf, 50-V, X5R, 1608 (0603) | TDK          | C1608JB1H104K |

### 8.2.2.1 Output Capacitor

For stable operation, total capacitance of the VTT output terminal can be equal to or greater than 20  $\mu\text{F}$ . Attach two 10- $\mu\text{F}$  ceramic capacitors in parallel to minimize the effect of ESR and ESL. If the ESR is greater than 2  $\text{m}\Omega$ , insert an R-C filter between the output and the VTTSNS input to achieve loop stability. The R-C filter time constant should be almost the same or slightly lower than the time constant of the output capacitor and its ESR.

Soft-start duration,  $t_{\text{SS}}$ , is also a function of this output capacitance. Where  $I_{\text{TTOCL}} = 2.2 \text{ A}$  (typ),  $t_{\text{SS}}$  can be calculated as,

$$t_{\text{SS}} = \left( \frac{C_{\text{OUT}} \times V_{\text{VTT}}}{I_{\text{TTOCL}}} \right) \quad (1)$$

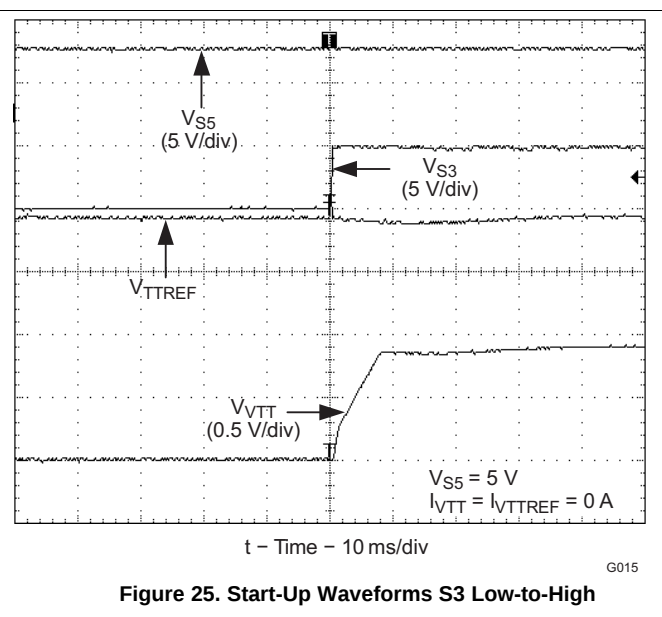
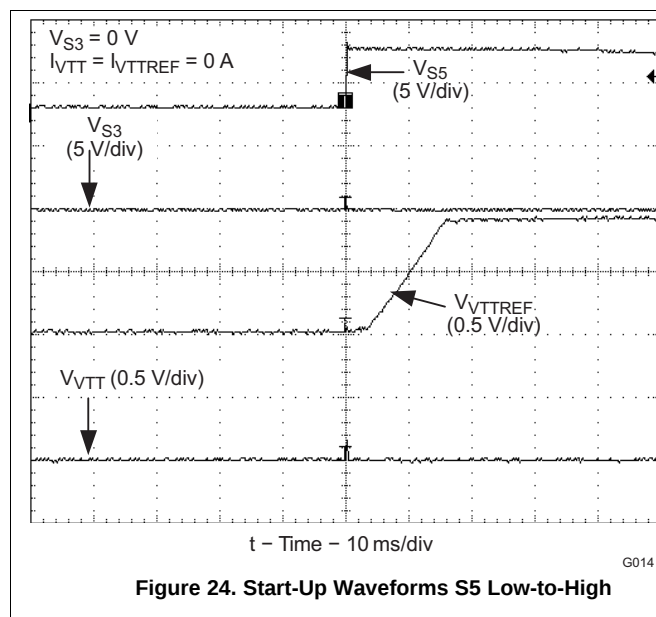
### 8.2.2.2 Input Capacitor

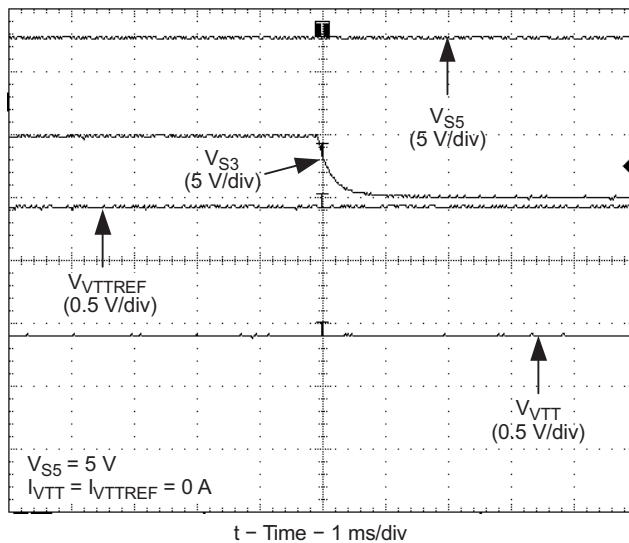
Depending on the trace impedance between the VLDOIN bulk power supply to the part, transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10- $\mu\text{F}$  (or more) ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VTT. In general, use  $1/2 C_{\text{OUT}}$  for the input.

### 8.2.2.3 VIN Capacitor

Add a ceramic capacitor with a value between 1  $\mu\text{F}$  and 4.7  $\mu\text{F}$  placed close to the VIN pin, to stabilize 5 V from any parasitic impedance from the supply.

## 8.2.3 Application Curves





G016

**Figure 26. Shutdown Waveforms S3 High-to-Low**

## 9 Power Supply Recommendations

TPS51100 is designed for a sink / source double data rate (DDR) termination regulator with VTTREF buffered reference output. Supply input voltage (VIN) support voltage from 4.75 V to 5.25 V; VLDOIN input voltage supports from 1.2 V to 3.6 V.

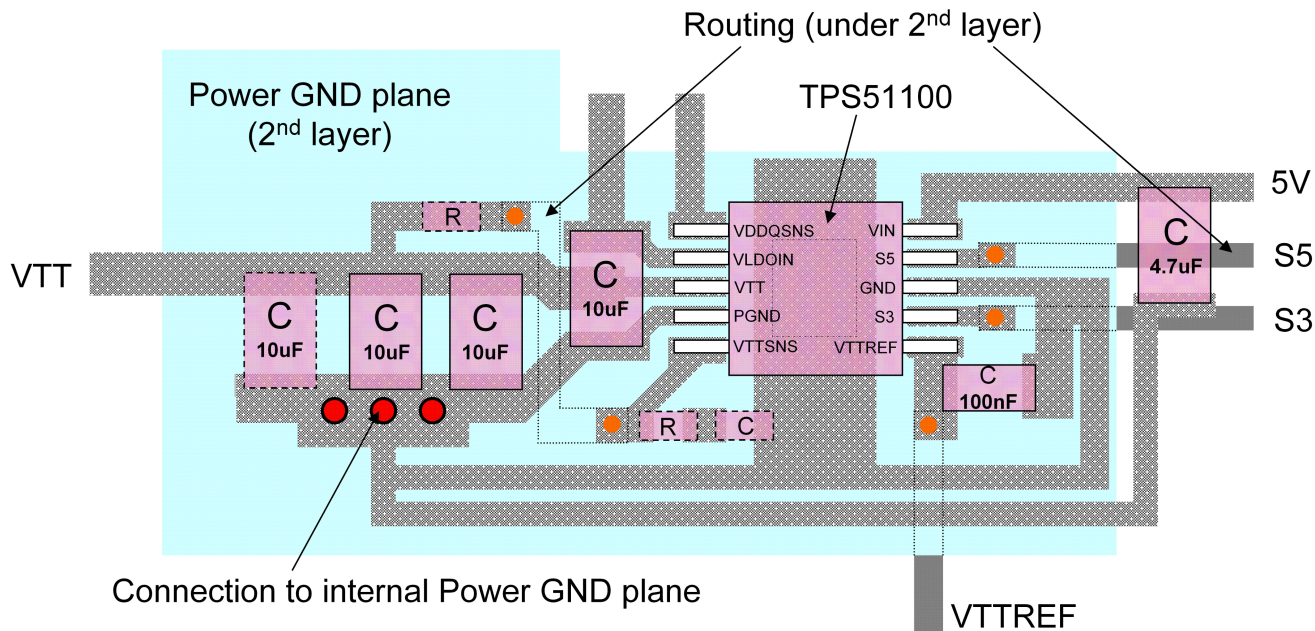
## 10 Layout

### 10.1 Layout Guidelines

Consider the following points before the layout of TPS51100 design begins.

- The input bypass capacitor for VLDOIN should be placed to the pin as close as possible with a short and wide connection.
- The output capacitor for VTT should be placed close to the pin with a short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current power line and is strongly recommended to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point. Also, it is recommended to minimize any additional ESR and/or ESL of the ground trace between the GND pin and the output capacitor(s).
- Consider adding an LPF at VTTSNS in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ.
- VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise generative lines.
- The negative node of the VTT output capacitor(s) and the VTTREF capacitor should be tied together, avoiding common impedance to the high-current path of the VTT source/sink current.
- The GND (signal GND) pin node represents the reference potential for the VTTREF and VTT outputs. Connect GND to the negative nodes of the VTT capacitor(s), VTTREF capacitor, and VDDQ capacitor(s) with care to avoid additional ESR and/or ESL. GND and PGND (Power GND) should be isolated, with a single point connection between them.
- In order to remove heat from the package effectively, prepare the thermal land and solder to the package thermal pad. The wide trace of the component-side copper, connected to this thermal land, helps heat spreading. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to help dissipation.

## 10.2 Layout Example



M0118-01

- NOTES:
1. The positive terminal of each output capacitor should be directly connected to VTT of the IC; do not use a VIA.
  2. The negative terminal of each output capacitor should be directly connected to GND of the IC; do not use a VIA.
  3. VIAs
    - VIA between 1<sup>st</sup> and 2<sup>nd</sup> layers
    - VIA between 1<sup>st</sup> and other layers under 2<sup>nd</sup>
  4. Rs and Cs with dotted outlines are options.

**Figure 27. TPS51100 PCB Layout Guideline**

## 10.3 Thermal Considerations

As the TPS51100 is a linear regulator, the VTT current flow in both source and sink directions generates power dissipation from the device. In the source phase, the potential difference between  $V_{VLDOIN}$  and  $V_{VTT}$  times VTT current becomes the power dissipation,  $W_{DSRC}$ .

$$W_{DSRC} = (V_{VLDOIN} - V_{VTT}) \times I_{VTT} \quad (2)$$

In this case, if VLDOIN is connected to an alternative power supply lower than  $V_{DDQ}$  voltage, power loss can be decreased.

For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation, and  $W_{DSNK}$ , is calculated by:

$$W_{DSNK} = V_{VTT} \times I_{VTT} \quad (3)$$

Because the device does not sink and source the current at the same time and  $I_{VTT}$  varies rapidly with time, the actual power dissipation that must be considered for thermal design is an average over the thermal relaxation duration of the system. Another power consumption is the current used for internal control circuitry from the VIN supply and VLDOIN supply. This can be estimated as 20 mW or less at normal operational conditions. This power must be effectively dissipated from the package. Maximum power dissipation allowed to the package is calculated by,

$$W_{PKG} = \frac{(T_{J(max)} - T_{A(max)})}{\theta_{JA}} \quad (4)$$

where

$T_{J(max)}$  is 125°C

## Thermal Considerations (continued)

$T_{A(max)}$  is the maximum ambient temperature in the system

$\theta_{JA}$  is the thermal resistance from the silicon junction to the ambient

This thermal resistance strongly depends on the board layout. TPS51100 is assembled in a thermally enhanced PowerPAD package that has an exposed die pad underneath the body. For improved thermal performance, this die pad must be attached to the ground trace via thermal land on the PCB. This ground trace acts as a heat sink/spread. The typical thermal resistance, 57.7°C/W, is achieved based on a 3 mm × 2 mm thermal land with two vias without air flow. It can be improved by using larger thermal land and/or increasing the number of vias. For example, assuming a 3 mm × 3 mm thermal land with four vias without air flow, it is 45.4°C/W. Further information about the PowerPAD package and its recommended board layout is described in the *PowerPAD Thermally Enhanced Package* application report (SLMA002). This document is available at [www.ti.com](http://www.ti.com).

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Third-Party Products Disclaimer

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### 11.2 Trademarks

PowerPAD is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS51100DGQ</a>  | Active        | Production           | HVSSOP (DGQ)   10 | 80   TUBE             | Yes         | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM                | -40 to 85    | 51100               |
| TPS51100DGQ.A                | Active        | Production           | HVSSOP (DGQ)   10 | 80   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 51100               |
| TPS51100DGQ.B                | Active        | Production           | HVSSOP (DGQ)   10 | 80   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 51100               |
| TPS51100DGQG4                | Active        | Production           | HVSSOP (DGQ)   10 | 80   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 51100               |
| <a href="#">TPS51100DGQR</a> | Active        | Production           | HVSSOP (DGQ)   10 | 2500   LARGE T&R      | Yes         | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM                | -40 to 85    | 51100               |
| TPS51100DGQR.A               | Active        | Production           | HVSSOP (DGQ)   10 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 51100               |
| TPS51100DGQR.B               | Active        | Production           | HVSSOP (DGQ)   10 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 51100               |
| TPS51100DGQRG4               | Active        | Production           | HVSSOP (DGQ)   10 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 51100               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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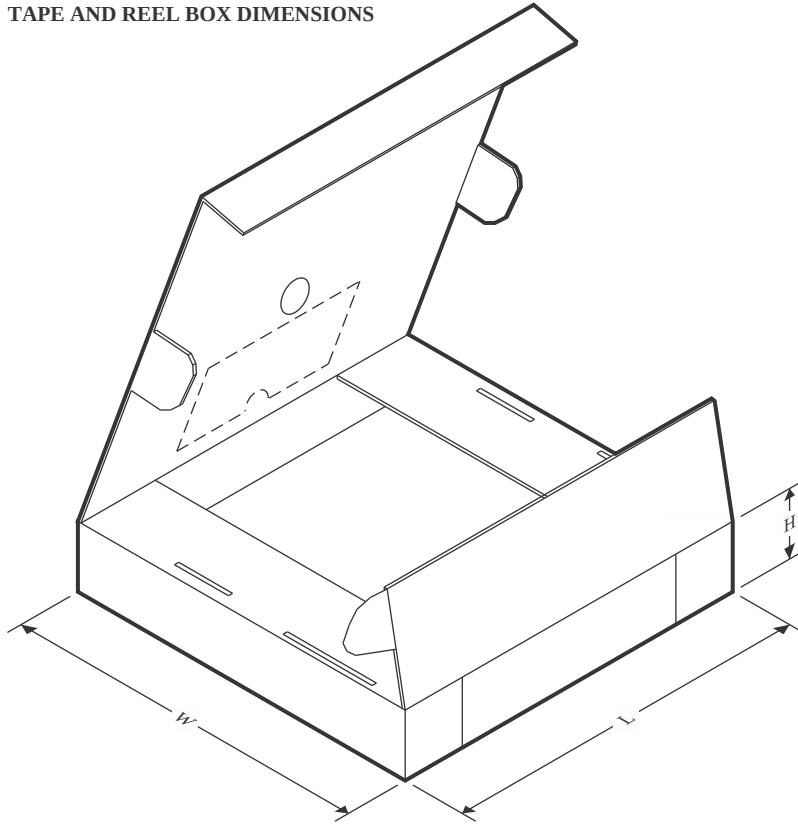
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS51100DGQR | HVSSOP       | DGQ             | 10   | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TPS51100DGQR | HVSSOP       | DGQ             | 10   | 2500 | 330.0              | 12.4               | 5.3     | 3.3     | 1.3     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS51100DGQR | HVSSOP       | DGQ             | 10   | 2500 | 364.0       | 364.0      | 27.0        |
| TPS51100DGQR | HVSSOP       | DGQ             | 10   | 2500 | 346.0       | 346.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS51100DGQ   | DGQ          | HVSSOP       | 10   | 80  | 330    | 6.55   | 500    | 2.88   |
| TPS51100DGQ   | DGQ          | HVSSOP       | 10   | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS51100DGQ.A | DGQ          | HVSSOP       | 10   | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS51100DGQ.A | DGQ          | HVSSOP       | 10   | 80  | 330    | 6.55   | 500    | 2.88   |
| TPS51100DGQ.B | DGQ          | HVSSOP       | 10   | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS51100DGQ.B | DGQ          | HVSSOP       | 10   | 80  | 330    | 6.55   | 500    | 2.88   |
| TPS51100DGQG4 | DGQ          | HVSSOP       | 10   | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS51100DGQG4 | DGQ          | HVSSOP       | 10   | 80  | 330    | 6.55   | 500    | 2.88   |

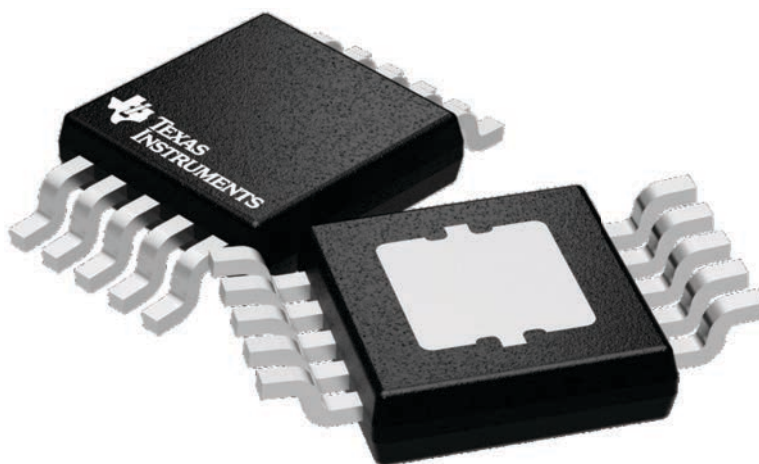
## GENERIC PACKAGE VIEW

**DGQ 10**

**PowerPAD™ HVSSOP - 1.1 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224775/A



## PowerPAD™ - 1.1 mm max height

5.05  
4.75 TYP  
 PIN 1 ID AREA  
 10  
 8X 0.5  
 2X 2  
 6  
 10X 0.27  
0.17  
 3.1  
2.9  
NOTE 3  
 5  
 3.1  
2.9  
NOTE 4  
 SEATING PLANE  
 0.1 C  
 1.1 MAX  
 0.23  
0.13 TYP  
 SEE DETAIL A  
 EXPOSED THERMAL PAD  
 5  
 6  
 10  
 1  
 1.89  
1.69  
 1.83  
1.63  
 0.25  
 GAGE PLANE  
 0° - 8°  
 0.7  
0.4  
 DETAIL A  
TYPICAL

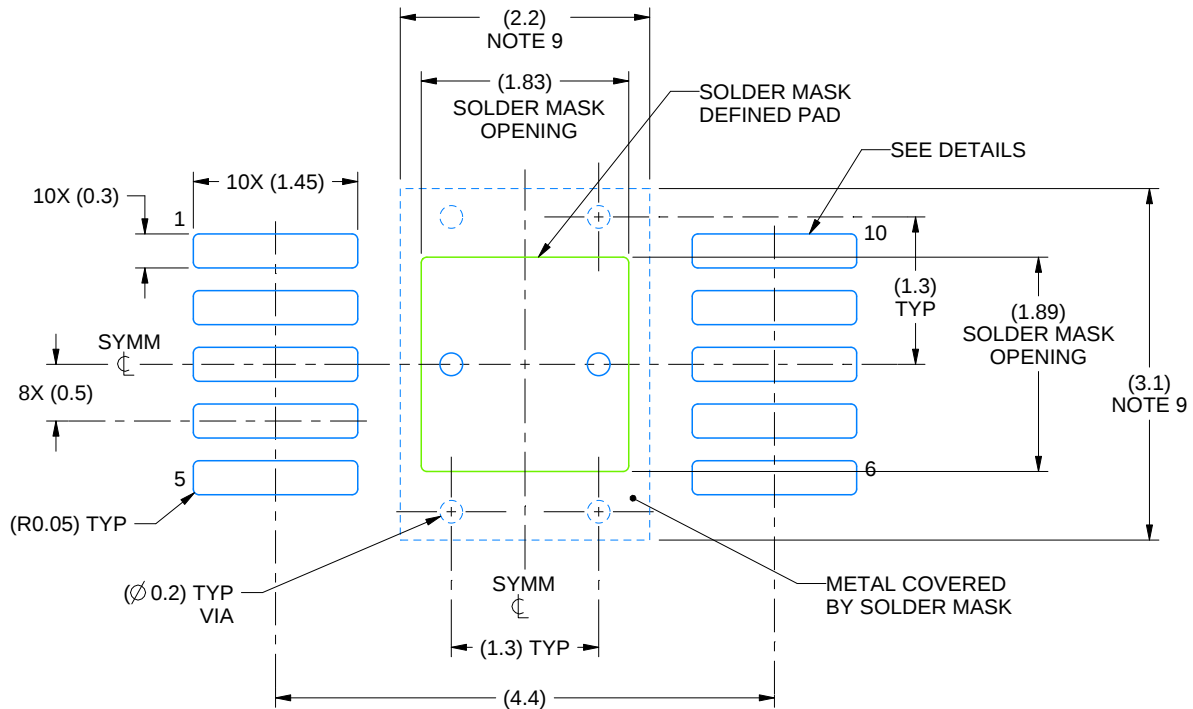
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.

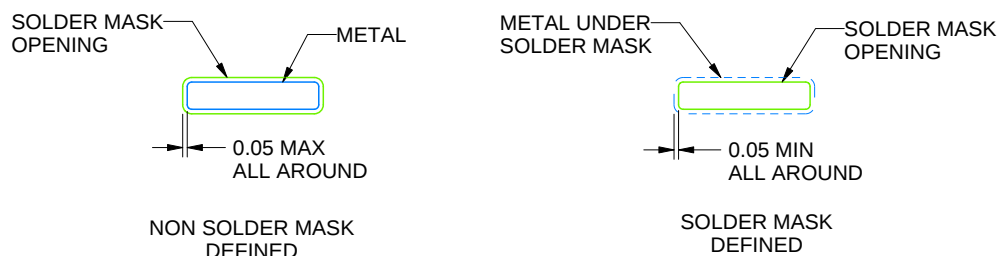
**DGQ0010D**

## PowerPAD™ - 1.1 mm max height

## PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:15X



## SOLDER MASK DETAILS

4218842/B 04/2024

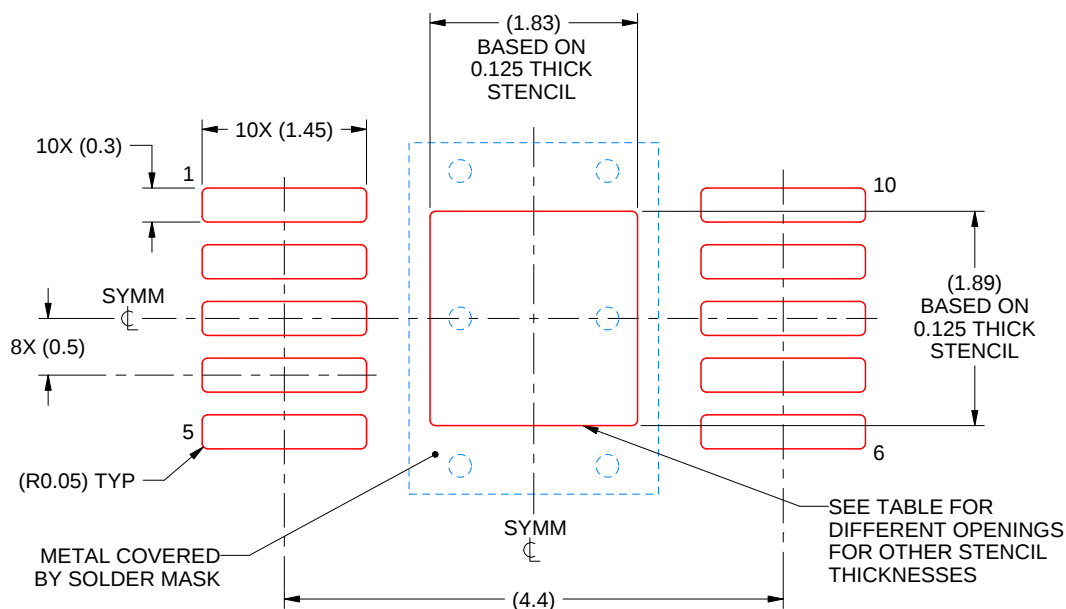
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.

**DGQ0010D**

## PowerPAD™ - 1.1 mm max height

## PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 2.05 X 2.11            |
| 0.125             | 1.83 X 1.89 (SHOWN)    |
| 0.150             | 1.67 X 1.73            |
| 0.175             | 1.55 X 1.60            |

4218842/B 04/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

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