

# TPS389006/08-Q1,TPS389R0-Q1 Multichannel Overvoltage and Undervoltage I<sup>2</sup>C Programmable Voltage Supervisor and Monitor

## 1 Features

- · ASIL-D Functional Safety-Compliant
  - Development target for Functional Safety applications
  - Documentation to aid ISO 26262 system design
  - Systematic capability up to ASIL D
  - Hardware capability up to ASIL D
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C
- Monitor state-of-the art SOCs
  - ±6mV threshold accuracy (–40°C to +125°C)
  - Input voltage range: 2.5V to 5.5V
  - Undervoltage lockout (UVLO): 2.48V
  - Low standby quiescent current: 200µA
  - 6 channels with 2 remote sense (TPS389006-Q1)
  - 6 channels with 2 remote sense and Reset output (TPS389R06-Q1)
  - 8 channels (TPS389008-Q1)
  - Fixed window threshold levels
    - 5mV steps from 0.2V to 1.475V
    - 20mV steps from 0.8V to 5.5V
- Miniature solution and minimal component cost
  - 3mm x 3mm QFN package
  - Adjustable glitch immunity via I<sup>2</sup>C
  - User adjustable voltage threshold levels via I<sup>2</sup>C
- Designed for safety applications
  - Active-low open-drain NIRQ output
  - Active-low open-drain NRST output (TPS389R0-Q1)
  - Built-in 8-bit ADC for real-time voltage readouts
  - Cyclic Redundancy Checking (CRC)
  - Packet Error Checking (PEC)
  - Sequence and fault logging
- Sync function for rail tagging
  - Connect with a multichannel sequencer for sequencing functionality

# 2 Applications

- Advanced driver assistance system (ADAS)
- Sensor fusion

## 3 Description

The TPS389006/08-Q1 device is an ASIL-D compliant six/eight-channel window supervisor IC with two remote sense pins (six channel version) available in a 16-pin 3mm x 3mm QFN package. The TPS389R06-Q1 device is a six channel window supervisor IC with 2 remote sense pins and a Reset output. This high accuracy multichannel voltage supervisor is designed for systems that operate on low-voltage supply rails and have narrow margin supply tolerances.

Remote sense pins enable a highly accurate voltage measurement on the high current core rail by accounting for voltage drop across PCB traces. I<sup>2</sup>C functionality gives flexibility in selecting thresholds, reset delays, glitch filters, and pin functionality. The internal glitch immunity and noise filters eliminate the need for external RC components to reduce false resets resulting from power transients. In addition, device does not require any external resistors for setting overvoltage and undervoltage reset thresholds, which further optimizes overall accuracy, cost, size, and improves reliability for safety systems.

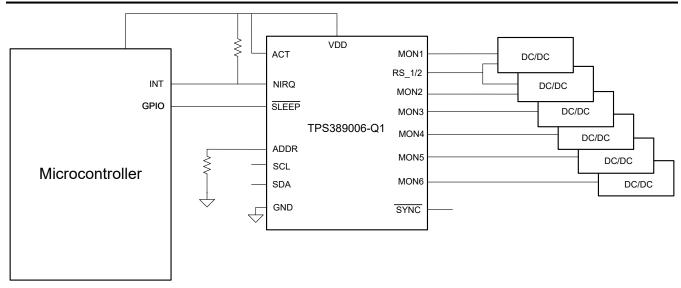
This device offers CRC error checking, sequence logging during turn ON or turn OFF, and a built-in ADC for voltage readouts to provide redundant error checking. In addition, TPS389006 offers a sync feature for tagging the rails as the device powers up. The TPS389006 device also pairs with TI's power-supply sequencer TPS38700 to enable proper power-on sequence in addition to voltage monitoring for SIL-3 level compliance.

#### **Device Information**

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TPS389006-Q1		
TPS389008-Q1 Preview	WQFN (16)	3mm x 3mm
TPS389R0-Q1 Preview		

- For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.





**TPS389006-Q1 Typical Circuit** 



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# **4 Device Comparison**

Figure 4-1 shows the device nomenclature of the TPS389006/08-Q1,TPS389R0-Q1. Table 4-1 provides a summary of available device functions and corresponding part number. Contact TI sales representatives or go online to TI's E2E forum for details and availability of other options; minimum order quantities apply.

See Section 9.1 for more information regarding the device ordering codes. Table 9-1 and Table 9-3 show how to decode the function of the device based on the part number.

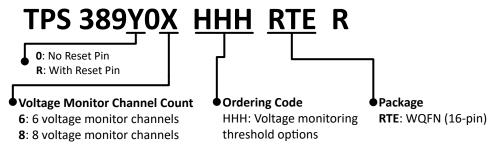


Figure 4-1. TPS389006/08-Q1,TPS389R0-Q1 Device Nomenclature

**Table 4-1. Multichannel Supervisor Summary Table** 

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Specification	TPS38900x-Q1	TPS389R0x-Q11	TPS38800x-Q11	TPS388R0x-Q11	TPS389C0x-Q1	TPS388C0x-Q11
Hardware ASIL Rating	D	D	В	В	D	В
Monitoring Channel Count	4 to 8	4 to 7	4 to 8	4 to 7	3 to 6	3 to 6
Monitoring Range	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V
Comparator Monitoring (HF Faults)	✓	✓	✓	✓	✓	✓
ADC Monitoring (LF Faults)	✓	✓	х	х	✓	х
Watchdog	х	х	х	х	Q&A	Window
Voltage Telemetry	✓	<b>√</b>	х	х	✓	х
Monitor Glitch Filtering	✓	✓	✓	✓	✓	✓
Sequence Logging	✓	х	<b>√</b>	х	✓	1
NIRQ PIN	✓	✓	✓	<b>√</b>	✓	1
NRST PIN	х	✓	х	✓	✓	✓
SYNC PIN	✓	х	х	х	х	x
WDO PIN	х	х	х	х	✓	✓
WDI PIN	х	х	х	х	х	✓
ESM PIN	х	x	х	x	✓	х

<sup>1.</sup> Preview, contact TI sales representatives or on TI's E2E forum for details and availability of other options

# **5 Pin Configuration and Functions**

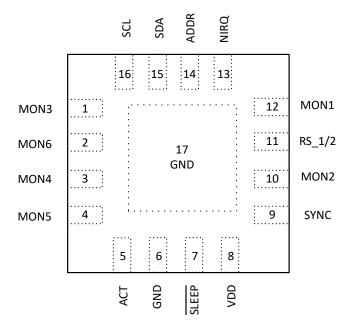


Figure 5-1. RTE Package 16-Pin WQFN TPS389006-Q1 Top View

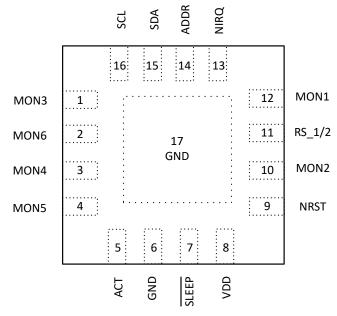


Figure 5-2. RTE Package 16-Pin WQFN TPS389R0-Q1 Top View



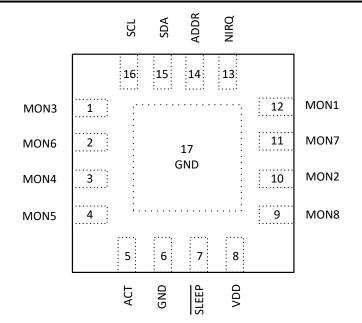


Figure 5-3. RTE Package 16-Pin WQFN TPS389008-Q1 Top View

**Table 5-1. Pin Functions** 

	PIN			
NO.	TPS389006/08-Q1	TPS389R0-Q1	I/O	DESCRIPTION
NO.	NAME	NAME		
1	MON3	MON3	I	Voltage monitor channel 3
2	MON6	MON6	I	Voltage monitor channel 6
3	MON4	MON4	I	Voltage monitor channel 4
4	MON5	MON5	I	Voltage monitor channel 5
5	ACT	ACT	I	Active high device enable
6	GND	GND	-	Power ground
7	SLEEP	SLEEP	I	Active low sleep enable
8	VDD	VDD	-	Power supply rail
9	SYNC/MON8	-	I/O	Sequence logging synchronization across multiple devices/Voltage monitor channel 8
9	-	NRST	0	Open Drain Reset Output
10	MON2	MON2	I	Voltage monitor channel 2
11	RS_1/2/MON7	RS_1/2	1	Voltage monitor channel 1/2 remote sense/ Voltage monitor channel 7
12	MON1	MON1	I	Voltage monitor channel 1
13	NIRQ	NIRQ	0	Active-low open-drain interrupt output
14	ADDR	ADDR	I	I <sup>2</sup> C address select pin
15	SDA	SDA	I/O	I <sup>2</sup> C data pin
16	SCL	SCL	I	I <sup>2</sup> C clock pin
17	GND	GND	-	Exposed power ground pad



# **6 Specifications**

# 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD	-0.3	6	V
Voltage	NIRQ, NRST	-0.3	6	V
Voltage	ACT, SLEEP, SCL, SDA	-0.3	6	V
Voltage	SYNC	-0.3	VDD+0.3	V
Voltage	ADDR	-0.3	2	V
Voltage	MONx	-0.3	6	V
Current	NIRQ, NRST		±10	mA
	Continuous total power dissipation	See the Thermal Information		
Temperature <sup>(2)</sup>	Operating junction temperature, T <sub>J</sub>	-40	150	°C
remperature (2)	Operating free-air temperature, T <sub>A</sub>	-40	125	°C
	Storage temperature, T <sub>stg</sub>	-65	150	°C

<sup>(1)</sup> Stresses beyond values listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 6.2 ESD Ratings

				VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDE	C JS-001 <sup>(1)</sup>	±2000	
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per AEC	All pins	±500	V
	a.ss.ia.gs	Q100-011	Corner pins	±750	

<sup>(1)</sup> AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

# **6.3 Recommended Operating Conditions**

		MIN	NOM MAX	UNIT
VDD	Supply pin voltage	2.5	5.5	V
NIRQ,NRST	Pin voltage	0	5.5	V
I <sub>NIRQ</sub> ,I <sub>NRST</sub>	Pin Currents	0	±5	mA
ADDR	Address pin voltage	0	1.8	V
MONx	Monitor Pins	0	5.5	V
ACT, SLEEP, SCL, SDA	Pin Voltage	0	5.5	V
SYNC	Pin Voltage	0	VDD	V
R <sub>UP</sub> (1)	Pull-up resistor (Open Drain config)	10	100	kΩ

<sup>(2)</sup> As a result of the low dissipated power in this device, it is assumed that  $T_J = T_A$ .



## **6.4 Thermal Information**

		TPS389006	
	THERMAL METRIC <sup>(1)</sup>	RTE (WQFN)	UNIT
		PINS	
R <sub>0JA</sub>	Junction-to-ambient thermal resistance	53.4	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	51.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	17.2	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	20.7	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.9	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

At 2.6V <= VDD <= 5.5V, NIRQ,NRST Voltage =  $10k\Omega$  to  $V_{DD}$ , NIRQ,NRST load = 10pF, and over the operating free-air temperature range of  $-40^{\circ}C$  to  $125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_{J}$  =  $25^{\circ}C$ , typical conditions at VDD= 3.3V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PA	RAMETERS		'			
VDD	Input supply voltage		2.6		5.5	V
VDD	Rising Threshold		2.67		2.81	V
VDD <sub>UVLO</sub>	Falling Threshold		2.48		2.60	V
V <sub>POR</sub>	Power on Reset Voltage (2)				1.65	V
I <sub>DD_Active</sub>	Supply current into VDD pin (MON = LF/HF active) ACT = High, Sleep = High	VDD <= 5.5V		1.55	2	mA
I <sub>DD_Sleep</sub>	Supply current into VDD pin (MON = LF/HF active) ACT = High ,Sleep = Low,I2C = Sleep power bit set to 1	VDD <= 5.5V		1.55	2	mA
$I_{DD\_Idle}$	Supply current into VDD pin (MON = OVLF active) ACT = Low, Idle state-I2C active and OVLF mon	VDD <= 5.5V >10ms BIST		200	280	μА
I <sub>DD_Deep</sub> Sleep	Supply current into VDD pin (MON = HF active), ACT = High, Sleep = Low, I2C = Sleep power bit set to 0	VDD <= 5.5V		275	380	μΑ
V <sub>MONX</sub>	MON voltage range		0.2		5.5	V
I <sub>MONX</sub>	Input current MONx pins	V <sub>MON</sub> = 5V			20	μA
MONX_ADJ	Input current for ADJ version (1x)	V <sub>MON</sub> = 5V			0.1	μA
VMON LF	1x mode (No scaling)		0.2		1.475	V
VIVIOIN_LI	with 4x scaling		0.8		5.5	V
VMON HF	1x mode (No scaling)		0.2		1.475	V
V IVIOIN_I II'	with 4x scaling		0.8		5.5	V
Threshold	1x mode (No scaling) LSB			5		mV
granularity_H F	4x mode (With scaling) LSB			20		mV
LPF cutoff LF	Range of Programmable values (I <sup>2</sup> C selectable)	Low Freq channel	250		4000	Hz
LPF cutoff HF		High Freq channel		4		Mhz



## 6.5 Electrical Characteristics (continued)

At 2.6V <= VDD <= 5.5V, NIRQ,NRST Voltage =  $10k\Omega$  to  $V_{DD}$ , NIRQ,NRST load = 10pF, and over the operating free-air temperature range of  $-40^{\circ}C$  to  $125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_{J}$  =  $25^{\circ}C$ , typical conditions at VDD= 3.3V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		0.2V≤V <sub>MONX</sub> ≤1.0V	-6		6	mV
A	VANCAL	1.0V <v<sub>MONX≤1.475V</v<sub>	-7.5		7.5	mV
Accuracy_HF	VMON	1.475V <v<sub>MONX≤2.95V</v<sub>	-0.6		0.6	%
		VMONX>2.95V	-0.7		0.7	%
	Hysteresis on UV,OV pin(Hysteresis is	0.2V≤V <sub>MONX</sub> ≤1.475V		5	11	\/
V <sub>HYS_HF</sub>	with respect of the tripoint ((UV),(OV))	1.475V <v<sub>MONX≤2.95V</v<sub>		9	16	mV
	(1)	VMONX>2.95V		17	28	mV
MON_OFF	OFF Voltage threshold	Monitored falling edge of V <sub>MON</sub>	140		215	mV
LKG	Output leakage current -NIRQ	VDD=V <sub>NIRQ</sub> =5.5V			300	nA
ACT_L	Logic Low input	DEV_CONFIG.SOC_IF1=1			0.36	V
ACT_H	Logic high input	DEV_CONFIG.SOC_IF1=1	0.84			٧
SLEEP_L	Logic Low input	DEV_CONFIG.SOC_IF1=1			0.36	V
SLEEP_H	Logic high input	DEV_CONFIG.SOC_IF1=1	0.84			V
SYNC_L	Input High	DEV_CONFIG.SOC_IF1=1			0.36	V
SYNC_H	Input Low	DEV_CONFIG.SOC_IF1=1	0.84			V
SYNC_PU	Internal Pull-up		25		100	kΩ
SYNC_OL	with 10kΩ external pull up				0.1	V
ACT	Internal Pull down			100		kΩ
SLEEP	Internal Pull down		,	100		kΩ
	Steps/Resolution	0.2V <v<sub>MONX≤1.475V</v<sub>		5		.,
UV,OV		0.8V <v<sub>MONX&lt;5.5V</v<sub>		20		mV
V <sub>OL</sub>	Low level output voltage-NIRQ	NIRQ ,5.5V/5mA			100	mV
lkg(OD)	Open-Drain output leakage current-NIRQ	NIRQ pin in High Impedance,V <sub>NIRQ</sub> = 5.5, Not asserted state			90	nA
V <sub>OL</sub>	Low level output voltage-NRST	NRST ,5.5V/5mA			100	mV
lkg(OD)	Open-Drain output leakage current-NRST	NRST pin in High Impedance,V <sub>NRST</sub> = 5.5, Not asserted state			600	nA
ADDR	ADDR pin current			20		μA
		R=5.36k		0x30		
		R=16.2k		0x31		
		R=26.7k		0x32		
<sup>2</sup> C ADDR	(Hay format)	R=37.4k		0x33		
-C ADDR	(Hex format)	R=47.5k		0x34		
		R=59.0k		0x35		
		R=69.8k		0x36		
		R=80.6k	,	0x37		
TSD	Thermal Shutdown			155		°C
TSD Hys	Thernal Shutdown Hysterisis			20		°C
RS	Remote sense range		-100		100	mV
ADC SPECIFI	CATION	· · · · · · · · · · · · · · · · · · ·				
√in	Input Range		0.2		5.5	V
	Danah dian	1x mode (No scaling)		5		mV
Res_LF	Resolution	4x mode		20		mV



## **6.5 Electrical Characteristics (continued)**

At 2.6V <= VDD <= 5.5V, NIRQ,NRST Voltage =  $10k\Omega$  to  $V_{DD}$ , NIRQ,NRST load = 10pF, and over the operating free-air temperature range of –  $40^{\circ}C$  to  $125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_{J}$  =  $25^{\circ}C$ , typical conditions at VDD= 3.3V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>S</sub>	Sample Rate			125		ksps
V <sub>HYS_LF</sub>	Hysteresis LF faults	1x mode (No scaling)		10	15	mV
V <sub>HYS_LF</sub>	Hysteresis LF faults	4x mode		40	55	mV
A	VMON	1x mode (No scaling)	-12		+12	mV
Accuracy_LF		4x mode	-40		+40	mV
12C ELECTRIC	CAL SPECIFICATIONS					
C <sub>B</sub>	Capacitive load for SDA and SCL				400	pF
SDA,SCL	Low Threshold	DEV_CONFIG.SOC_IF1=0			0.8	V
SDA,SCL	High Threshold	DEV_CONFIG.SOC_IF1=0	2.0			V

<sup>(1)</sup> Hysteresis is with respect of the tripoint  $(V_{IT-(UV)}, V_{IT+(OV)})$ .

# 6.6 Timing Requirements

At  $2.6\text{V} \le \text{VDD} \le 5.5\text{V}$ , NIRQ,NRST Voltage =  $10\text{k}\Omega$  to VDD, NIRQ,NRST load = 10pF, and over the operating free-air temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ , typical conditions at VDD = 3.3V.

			MIN	NOM	MAX	UNIT
COMMON F	PARAMETERS				-	
t <sub>BIST</sub>	POR to ready with BIST, TEST_CFG.AT_POR=1	includes OTP load			12	ms
t <sub>NBIST</sub>	POR to ready without BIST, TEST_CFG.AT_POR=0	includes OTP load			2	ms
BIST	BIST time,TEST_CFG.AT_POR=1 or TEST_CFG.AT_SHDN=1				10	ms
t <sub>I2C_ACT</sub>	I <sup>2</sup> C active from BIST complete				0	μs
t <sub>SEQ_Range</sub>	Sequence timestamp range, ACT or SLEEP edge to max counter				4	S
t <sub>SEQ_LSB</sub>	Sequence timestamp resolution			50		μs
t <sub>MON_ACT</sub>	Monitoring active from ACT rising edge				10	μs
t <sub>SEQ_ACT</sub>	Sequence tagging active from ACT or SLEEP edge				12	μs
t <sub>NIRQ</sub>	Fault detection to NIRQ assertion latency (except OV/UV faults)				25	μs
t <sub>NRST</sub>	Fault detection to NRST assertion latency (except OV/UV faults)				25	μs
t <sub>PD_NIRQ_1X</sub>	HF fault Propagation detect delay (default deglitch filter) includes digitial delay	VIT_OV/UV +/- 100mV			650	ns
t <sub>PD_NIRQ_4X</sub>	HF fault Propagation detect delay (default deglitch filter) includes digitial delay	VIT_OV/UV +/- 400mV			750	ns
t <sub>PD_NRST_1X</sub>	HF fault Propagation detect delay (default deglitch filter) includes digitial delay	VIT_OV/UV +/- 100mV			650	ns
t <sub>PD_NRST_4X</sub>	HF fault Propagation detect delay (default deglitch filter) includes digitial delay	VIT_OV/UV +/- 400mV			750	ns
t <sub>SEQ_ACC</sub>	Accuracy of sequence timestamp		-5		5	%

<sup>(2)</sup> V<sub>POR</sub> is the minimum V<sub>DDX</sub> voltage level for a controlled output state.



## 6.6 Timing Requirements (continued)

At  $2.6\text{V} \leq \text{VDD} \leq 5.5\text{V}$ , NIRQ,NRST Voltage =  $10\text{k}\Omega$  to VDD, NIRQ,NRST load = 10pF, and over the operating free-air temperature range of –  $40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , unless otherwise noted. Typical values are at T<sub>J</sub> =  $25^{\circ}\text{C}$ , typical conditions at VDD = 3.3V.

			MIN NOM	MAX	UNIT
		I2C Register time delay =000			μs
		I2C Register time delay =001	1	1	
		I2C Register time delay =010	10		ms
	DECET II	I2C Register time delay =011	16	ms	
t <sub>D</sub>	RESET time delay	I2C Register time delay =100	20		ms
		I2C Register time delay =101	70		ms
		I2C Register time delay =110	100		ms
		I2C Register time delay =111 200		ms	
t <sub>GI_R</sub>	UV & OV debounce range via I2C	FLT_HF(N)	0.1 1	102.4	μs



## 6.6 Timing Requirements (continued)

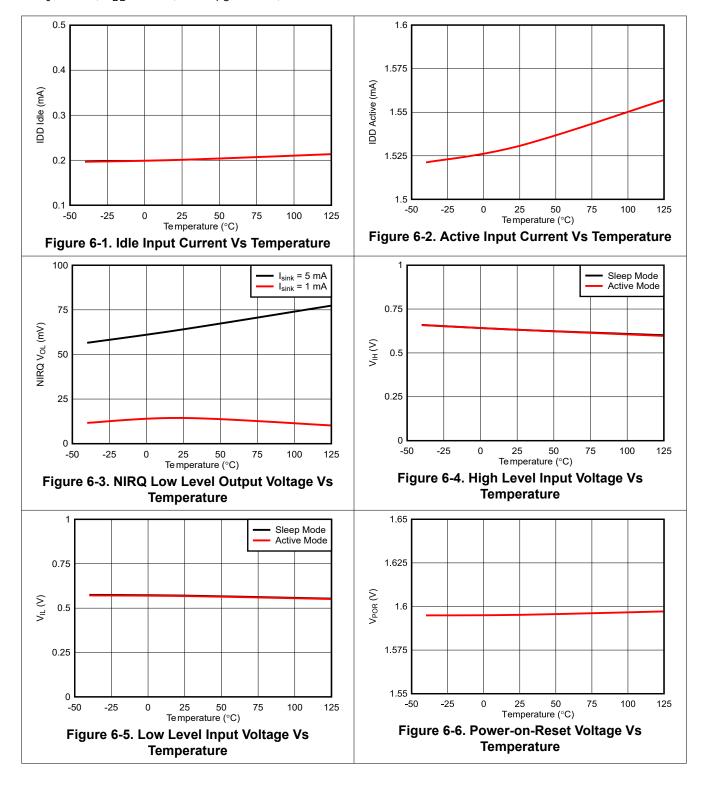
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3.3V .			MIN	NOM	MAX	UNIT
I2C TIMIN	NG CHARACTERISTICS					
f <sub>SCL</sub>	Serial clock frequency	Standard mode			100	kHz
f <sub>SCL</sub>	Serial clock frequency	Fast mode			400	kHz
SCL	Serial clock frequency	Fast mode +			1	MHz
Low	SCL low time	Standard mode	4.7			μs
Low	SCL low time	Fast mode	1.3			μs
Low	SCL low time	Fast mode +	0.5			μs
HIGH	SCL high time	Standard mode	4			μs
HIGH	SCL high time	Fast mode +	0.26			μs
SU;DAT	Data setup time	Standard mode	250			ns
SU;DAT	Data setup time	Fast mode	100			ns
SU;DAT	Data setup time	Fast mode +	50			ns
HD;DAT	Data hold time	Standard mode	10			ns
HD;DAT	Data hold time	Fast mode	10			ns
HD;DAT	Data hold time	Fast mode +	10			ns
SU;STA	Setup time for a Start or Repeated Start condition	Standard mode	4.7			μs
SU;STA	Setup time for a Start or Repeated Start condition	Fast mode	0.6			μs
SU;STA	Setup time for a Start or Repeated Start condition	Fast mode +	0.26			μs
HD:STA	Hold time for a Start or Repeated Start condition	Standard mode	4			μs
HD:STA	Hold time for a Start or Repeated Start condition	Fast mode	0.6			μs
HD:STA	Hold time for a Start or Repeated Start condition	Fast mode +	0.26			μs
BUF	Bus free time between a STOP and START condition	Standard mode	4.7			μs
BUF	Bus free time between a STOP and START condition	Fast mode	1.3			μs
BUF	Bus free time between a STOP and START condition	Fast mode +	0.5			μs
SU;STO	Setup time for a Stop condition	Standard mode	4			μs
su;sto	Setup time for a Stop condition	Fast mode	0.6			μs
su;sto	Setup time for a Stop condition	Fast mode +	0.26			μs
rDA	Rise time of SDA signal	Standard mode			1000	
rDA	Rise time of SDA signal	Fast mode	20		300	ns
rDA	Rise time of SDA signal	Fast mode +			120	ns
fDA	Fall time of SDA signal	Standard mode			300	ns
fDA	Fall time of SDA signal	Fast mode	1.4		300	ns
fDA	Fall time of SDA signal	Fast mode +	6.5		120	ns
rCL	Rise time of SCL signal	Standard mode			1000	ns
rCL	Rise time of SCL signal	Fast mode	20		300	ns
rCL	Rise time of SCL signal	Fast mode +			120	ns
tfCL	Fall time of SCL signal	Standard mode			300	ns
fCL	Fall time of SCL signal	Fast mode	6.5		300	ns
fCL	Fall time of SCL signal	Fast mode +	6.5		120	ns
tSP	Pulse width of SCL and SDA spikes that are suppressed	Standard mode, Fast mode and Fast mode +			50	ns



## **6.7 Typical Characteristics**

At  $T_J$  = 25°C,  $V_{DD}$  = 3.3V , and  $R_{PU}$  = 10k $\Omega$ , unless otherwise noted.





# 7 Detailed Description

## 7.1 Overview

The TPS389006/08 family of devices has six/eight channels that can be configured for over voltage, under voltage or both in a window configuration. The TPS389006/08 features highly accurate window threshold voltages (up to  $\pm 6$ mV) and a variety of voltage thresholds which can be factory configured or set on boot up by  $I^2C$  commands.

The TPS389006/08 includes the resistors used to set the overvoltage and undervoltage thresholds internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors.

The TPS389006 has a sequence logging feature to monitor and assign timestamps/log for the power rails turning on and off. It can perform sequence logging on a single device or across multiple devices on a board. It uses the SYNC pin to communicate across multiple devices. When either the ACT or SLEEP pin transitions from low to high or high to low, the sequence logging function becomes active until the expiry of the sequence timeout (SEQ\_TOUT). During the sequence timeout, the UV faults can be masked (Automask - AMSK).

The TPS389006/08 is designed to assert active low output signals (NIRQ) when the monitored voltage is outside the safe window. The factory configuration can have the interrupts disabled for over voltage and under voltage faults, sequence timeout, BIST enabled at POR, sequence fault interrupts disabled, and over voltage and under voltage deglitch settings depending on the OTP. The TPS389R0 also has an open drain NRST output that can be selectively mapped to UV/OV or any UV faults for either all the monitored voltages or a single monitored voltage.

## 7.2 Functional Block Diagram

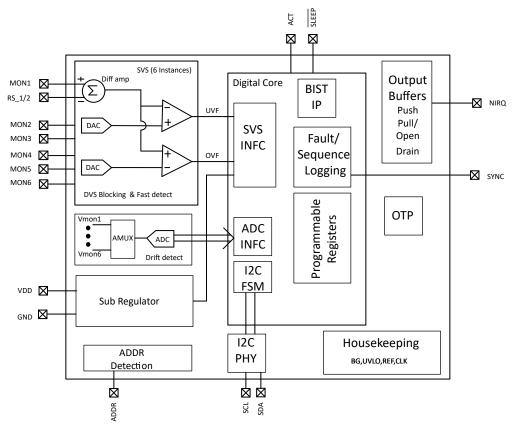


Figure 7-1. TPS389006-Q1 Block Diagram



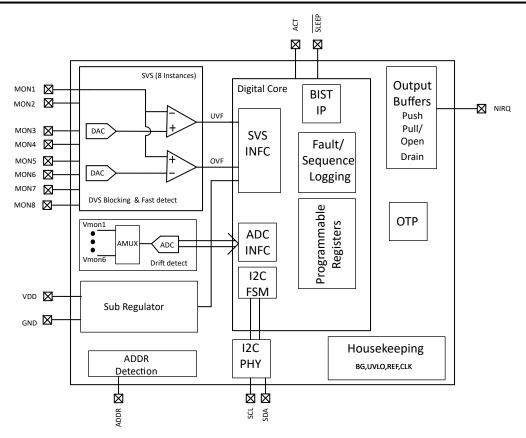


Figure 7-2. TPS389008-Q1 Block Diagram



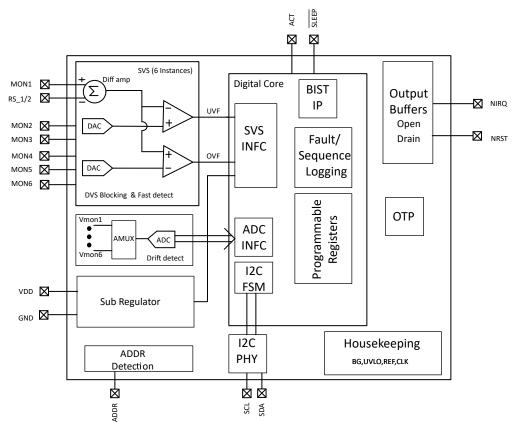


Figure 7-3. TPS389R0-Q1 Block Diagram

# 7.3 Feature Description

## 7.3.1 I<sup>2</sup>C

The TPS389006 device follows the  $I^2C$  protocol (up to 1MHz) to manage communication with host devices such as a MCU or System on Chip (SoC).  $I^2C$  is a two wire communication protocol implemented using two signals, clock (SCL) and data (SDA). The host device is the primary controller of communication. TPS389006 device responds over the data line during read or write operations as defined by  $I^2C$  protocol. Both SCL and SDA signals are open drain topology and can be used in a wired-OR configuration with other devices to share the communication bus. Both SCL and SDA pins need an external pull up resistor to supply voltage ( $10k\Omega$  recommended).

Figure 7-4 shows the timing relationship between SCL and SDA lines to transfer 1 byte of data. SCL line is always controlled by host. To transfer 1 byte data, host needs to send 9 clocks on SCL. 8 clocks for data and 1 clock for ACK or NACK. SDA line is controlled by either the host or TPS389006 device based on the read or write operation. Figure 7-4 and Figure 7-5 highlight the communication protocol flow and which device controls SDA line at various instances during active communication.

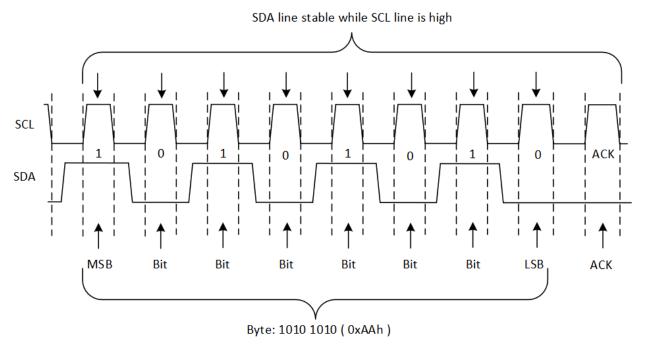


Figure 7-4. SCL to SDA Timing for 1 Byte Data Transfer



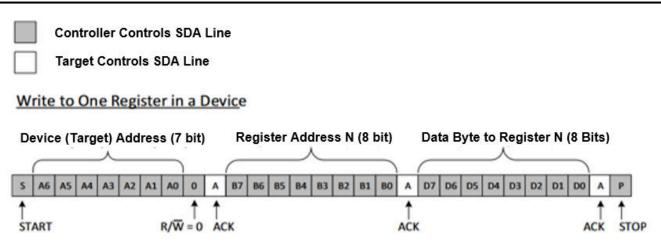


Figure 7-5. I<sup>2</sup>C Write Protocol

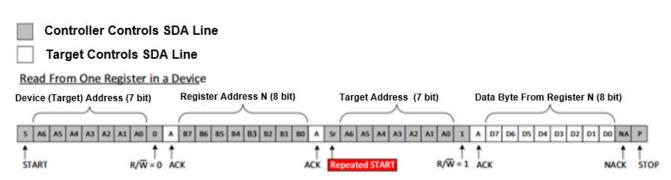


Figure 7-6. I<sup>2</sup>C Read Protocol

Before initiating communication over  $I^2C$  protocol, host needs to confirm the  $I^2C$  bus is available for communication. Monitor the SCL and SDA lines, if any line is pulled low, the  $I^2C$  bus is occupied. Host needs to wait until the bus is available for communication. Once the bus is available for communication, the host can initiate read or write operation by issuing a START condition. Once the  $I^2C$  communication is complete, release the bus by issuing STOP command. Figure 7-7 shows how to implement START and STOP condition.



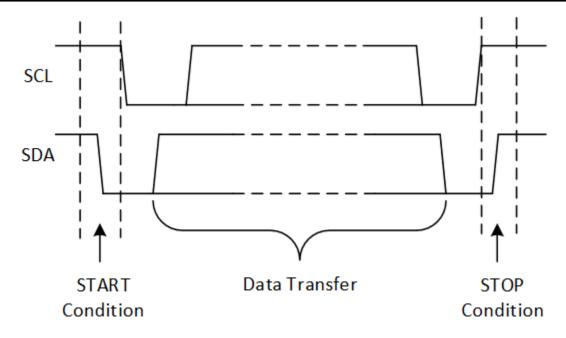


Figure 7-7. I<sup>2</sup>C START and STOP Condition

Table 7-1 shows the different functionality available when programming with I<sup>2</sup>C. **Table 7-1. User Programmable I<sup>2</sup>C Functions** 

FUNCTIONS	DESCRIPTION
Thresholds for OV/UV- fast loop	Adjustable in 5mV steps from 0.2V to 1.475V and 20mV steps from 0.8V to 5.5V
Thresholds for drift -positive and negative	Adjustable in 5mV steps from 0.2V to 1.475V and 20mV steps from 0.8V to 5.5V
Voltage Monitoring scaling	1 or 4
Glitch (debounce) immunity for OV/UV-fast loop	0.1 us to 102.4 us
Low pass filter cut off Frequency	250Hz to 4kHz
Enable sequence timeout	1ms to 4s
Sleep sequence timeout	1ms to 4s
SYNC pulse width	50us to 2600us
Expected ON/OFF Sequence on ACT	Used for sequence logging
Expected ON/OFF Sequence on Sleep	Used for sequence logging
Auto Mask OFF-ON-OFF via ACT	Selectable for each MON channel
Auto Mask OFF-ON-OFF via SLEEP	Selectable for each MON channel
Packet error checking for I <sup>2</sup> C	Enabling or Disabling
Force NIRQ assertion	Controlled by I <sup>2</sup> C register
Individual channel MON	Enable or Disable
Interrupt disable functions	BIST, PEC, TSD, CRC

## 7.3.2 Auto Mask (AMSK)

In the case of power up AMSK\_ON and AMSK\_EXS registers apply. It masks interrupts till the MON voltage crosses the UVLF threshold or sequence timeout expires whichever is sooner. In the case of power down AMSK\_OFF and AMSK\_ENS registers apply. It masks interrupts till the MON voltage is below the OFF threshold and then the OVLF interrupts are active.

Table 7-2 summarizes the auto-mask operation for the ACT and SLEEP transitions.



# **Table 7-2. Transition Table**

TRANSITION	AUTO-MASK APPLIED	AUTO-MASK APPLIES TO	AUTO-MASK INACTIVE	
ACT (Low -> High)	AMSK_ON	IEN_UVLF, IEN_UVHF, IEN_OVHF	SEQ_TOUT expires or rail crosses UVLF	At ACT=High
ACT (High -> Low)	AMSK_OFF	IEN_UVLF, IEN_UVHF, IEN_OVHF	Auto-mask active in transition till SEQ_TOUT expires	Until SEQ_TOUT expires
SLEEP (Low -> High) ACT = High	AMSK_EXS	IEN_UVLF, IEN_UVHF, IEN_OVHF	SEQ_TOUT expires or rail crosses UVLF	Always active
SLEEP (High -> Low) ACT = High	AMSK_ENS	IEN_UVLF, IEN_UVHF, IEN_OVHF	Auto-mask active	Always active



## 7.3.3 Packet Error Checking (PEC)

TPS389C03-Q1 supports Packet Error Checking (PEC) as a way to implement Cyclic Redundancy Checking (CRC). PEC is a dynamic CRC that happens only during read or write transactions if enabled. With the initial value of CRC set to 0x00, the PEC uses a CRC-8 represented by the polynomial:

$$C(x) = x^8 + x^2 + x + 1 \tag{1}$$

The polynomial is meant to catch any bit flips or noise in I2C communication which cause data and PEC byte to have a mismatch. The PEC calculation includes all bytes in the transmission, including address, command and data. The PEC calculation does not include ACK or NACK bits or START, STOP or REPEATED START conditions. If PEC is enabled, and the TPS389C03-Q1 is transmitting data, then the TPS389C03-Q1 is responsible for sending the PEC byte. If PEC is enabled, and the TPS389C03-Q1 is reveiving data from the MCU, then the MCU is responsible for sending the PEC byte. In case of faster communications needs like servicing the watchdog the required PEC feature can be effectively used to handle missing PEC information and to avoid triggering faults. Figure 7-8 and Figure 7-9 highlight the communication protocol flow when PEC is required and which device controls SDA line at various instances during active communication.

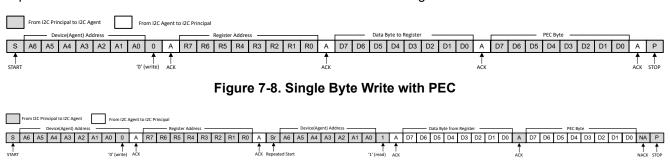


Figure 7-9. Single Byte Read with PEC

Table 7-3 summarises the registers associated with a PEC Write command and resulting device behavior. Table 7-4 summarises the registers associated with a PEC Read command and resulting device behavior.

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# Table 7-3. PEC Write Summary

EN_PEC	REQ_PEC	PEC_INT	Interrupt Status
0	х	х	PEC byte is not required in write operation, NO NIRQ assertion.
1	0	х	A write command missing a PEC byte is treated as OK, the write command executes and result in a I2C ACK. A write command with an incorrect PEC is treated as an error, the write command does not execute and result in a I2C NACK. NO NIRQ assertion.
1	1	0	A missing PEC is treated as an error, a write command only executes if the correct PEC byte is provided. I2C communication still responds with an ACK although write command did not execute. A write command with an incorrect PEC is treated as an error, the write command does not execute and result in a I2C NACK. NO NIRQ assertion.
1	1	1	A missing PEC is treated as an error, a write command only executes if the correct PEC byte is provided. I2C communication still responds with an ACK although write command did not execute. A write command with an incorrect PEC is treated as an error, the write command does not execute and results in a I2C NACK. NIRQ is asserted when a write command with a incorrect or missing PEC byte is attempted.

## Table 7-4. PEC Read Summary

EN_PEC	REQ_PEC	PEC_INT	Interrupt Status
0	х	х	I2C read operation reponds with data stored in register, I2C read command does not respond with registers corresponding PEC byte.
1	х	х	I2C read operation reponds with data stored in register and corresponding PEC byte.

#### 7.3.4 VDD

The TPS389006 is designed to operate from an input voltage supply range between 2.5V to 5.5V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a  $1\mu$ F capacitor between the VDD pin and the GND pin.

V<sub>DD</sub> needs to be at or above V<sub>DD(MIN)</sub> for at least the start-up delay (t<sub>SD</sub>+ t<sub>D</sub>) for the device to be fully functional.

#### 7.3.5 MON

The TPS389006/08 and TPS389R0 combines two comparators with a precision reference voltage and a trimmed resistor divider per monitor (MON) channel. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Both comparators also include built-in hysteresis that provides noise immunity and makes sure stable operation.

Although not required in most cases, for noisy applications good analog design practice is to place a 1nF to 10nF bypass capacitor at the MON input to reduce sensitivity to transient voltages on the monitored signal. Specific deglitch times can also be set independently for each MON via I<sup>2</sup>C registers

When monitoring VDD supply voltage, the MON pin can be connected directly to VDD. The output (NIRQ) and (NRST) is high impedance when voltage at the MON pin is between upper and lower boundary of threshold.

#### 7.3.6 NIRQ

NIRQ is a interrupt error ouput with latched behavior, if a monitored voltage falls or rises outside of the programmed OVHF and UVHF thresholds NIRQ is asserted. NIRQ remains in its low state until the action causing the fault is no longer present and a 1-to-clear is written to the bit signaling the fault. Un-mapping NIRQ from a fault reporting register does not de-assert the NIRQ signal. NIRQ is In a typical TPS389006/08-Q1,TPS389R0-Q1 application, the NIRQ output is connected to a reset or enable input of a processor [such as a digital signal processor (DSP) or application-specific integrated circuit (ASIC), or other processor type].

The TPS389006/08-Q1,TPS389R0-Q1 has an open drain active low output that requires a pull-up resistor to hold these lines high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to

enable the output to be connected to other devices at the correct interface voltage levels. The pull-up resistor value is determined by  $V_{OL}$ , output capacitive loading, and output leakage current. These values are specified in Section 6. The open drain output can be connected as a wired-OR logic with other open drain signals such as another TPS389006/08-Q1,TPS389R0-Q1 NIRQ pin.

#### 7.3.7 ADC

The ADC used in the TPS389006 runs on a 1Mhz clock with an effective sampling rate of 1/8MHz (= 125kHz). Initially, the ADC records with a resolution of 12 bits (1LSB = 0.41667mV) which is later round off to 8-bit data for I<sup>2</sup>C transaction. (1LSB = 5mV) The ADC uses ping-pong architecture in which it requires 2us for both sampling and conversion per channel with a total of 2 sampling channels. While CH0 performs coarse conversion, CH1 does fine conversion and vice verse.

Digitized 8-bit data is updated once the fine conversion is completed, which occurs once every 8µs. Each I<sup>2</sup>C transaction initiated for reading 8-bit MON\_LVL data (the ADC data of a particular channel), 8-bit data is paused from updating until the I<sup>2</sup>C transaction completes.

Voltage scaling is done using a resistor ladder, but for differential mode channels, a chopping circuit is used to get the average of both of the voltages (VMON + VMON\_RS)/2 since VMON\_RS can be negative and can't be converted into an ADC code. VMON – VMON\_RS is calculated digitally by subtracting ((VMON + VMON\_RS) /2) from VMON and then multiplying by 2.

The MONX channels can be configured in 1x (0.2V to 1.475V) or 4x mode (0.8V to 5.5V). For differential mode channels configured in 1x mode, (MON1 and MON2) the ADC range is limited up to 1.7V. To configure an ADC channel above 1.7V, please use 4x mode.

Real time voltage measurements use Equation 2.

$$V_{|V|} = ((ADC[7:0] * 5mV) + 0.2) * (VRANGE_MULT)$$
 (2)

- 1. ADC[7:0] is translated to a corresponding decimal value. The value of ADC[7:0] corresponding to MON1-MON6 can be read from registers 0x40-0x45 of Section 7.5.1.
- 2. VRANGE MULT corresponds to the selected monitor voltage multiplier set in register 0x1F of Section 7.5.2.
- 3. VRANGE MULT is set to a decimal 1 or 4 value depending on monitored value.

#### 7.3.8 Time Stamp

Time stamp measurement use Equation 3. The time stamps are used for sequence logging purposes to determine the order in which the rails are turned on or off.

$$t_{\text{stamp}} = 50\mu\text{s}^*\text{CLOCK}[15:0] \tag{3}$$

1. CLOCK[15:0] translated to corresponding decimal value. The value of CLOCK[15:0] corresponding to MON1-MON6 can be read from registers 0x90-0x9B of BANK0.

#### 7.3.9 NRST

The NRST pin in the TPS389R0-Q1 features a programmable reset delay time that can be adjusted from 0.2ms to 200ms when using TI\_CONTROL register. NRST is an open-drain output that must be pulled up through a  $1k\Omega$  to  $100k\Omega$  pullup resistor. When the device is powered up and POR is complete, NRST is asserted low until the BIST is complete. After the BIST, NRST remains high (not asserted) until it is triggered by a mappable fault condition. An NRST\_MISMATCH fault will be asserted if the NRST pin is pulled to an unexpected state. For example, if the NRST pin is in a high-impedance state (logic high) and is externally pulled low, then an NRST\_MISMATCH fault will assert. During an NRST toggle NRST mismatch will be active after  $2\mu s$ , NRST must exceed 0.6\*VDD to be considered in a logic high state. For conditions resulting in a Failsafe mode NRST pin will assert low and stay asserted until a power cycle.

NRST is also mappable to the OVHF and UVHF faults using the FC\_LF[n] registers. If a monitored voltage falls or rises outside of the programmed OVHF and UVHF thresholds, then NRST is asserted, driving the NRST pin low. When the monitored voltage comes back into the valid window, a reset delay circuit is enabled that holds

NRST low for a specified reset delay period  $(t_D)$ . Note if NRST is un-mapped from OVHF and UVHF faults while NRST is asserted then NRST deasserts, NRST reasserts when re-mapped assuming the voltage is still outside the valid window

The  $t_D$  period is determined by the RST\_DLY[2:0] value found in the TI\_CONTROL register. When the reset delay has elapsed, the NRST pin goes to a high-impedance state and uses a pullup resistor to hold NRST high. The pullup resistor must be connected to the proper voltage rail to allow other devices to be connected at the correct interface voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by output logic low voltage (VOL), capacitive loading, and leakage current.

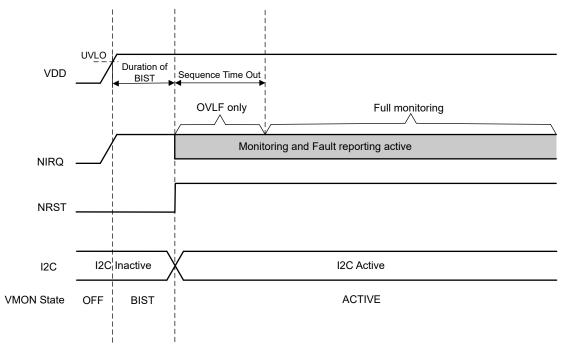


Figure 7-10. TPS389R0-Q1Start up Behavior Reset Pin

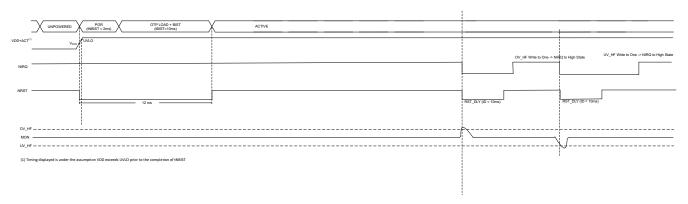


Figure 7-11. TPS389R0-Q1Reset Timing diagram for voltage faults

#### 7.3.10 Register Protection

TPS389006/08-Q1 and TPS389R0-Q1 features register protection enabled through registers PROT1 0xF1h and PROT2 0xF2h. Registers PROT1 and PROT2 composition is shown in table Table 7-5.



**Table 7-5. PROT1 Register Description** 

Register	Bit	7	6	5	4	3	2	1	0
PROT1 (0xF1)	R/W	RSVD	RSVD	WRKC	WRKS	CFG	IEN	MON	SEQ
PROT2 (0xF2)	R/W	RSVD	RSVD	WRKC	WRKS	CFG	IEN	MON	SEQ

To write-protect a register group, the host must set the relevant bit in both registers PROT1 and PROT2. Register groups are split up into categories as shown in Table 7-6. Register groups are only applicable to registers in Bank One.

**Table 7-6. Write-Protect Register Group Summary** 

Register name	PROT group	Register name	PROT group
VMON_CTL	WRKC	TI_CONTROL	N/A
VMON_MISC	CFG	AMSK_ON	IEN
TEST_CFG	CFG	AMSK_OFF	IEN
IEN_UVHP	IEN	SEQ_TOUT_MSB	SEQ
IEN_UVLP	IEN	SEQ_TOUT_LSB	SEQ
IEN_OVHP	IEN	SEQ_UP_THLD	SEQ
IEN_OVLP	IEN	SEQ_DN_THLD	SEQ
IEN_CONTROL	IEN	BANK_SEL	N/A
IEN_TEST	IEN	MON4 settings	MON[4]
IEN_VENDOR	IEN	MON5 settings	MON[5]
VIN_CH_EN	CFG	MON6 settings	MON[6]
VRANGE_MULT	CFG	MON7 settings	MON[7]
MON1 settings	MON[1]	MON8 settings	MON[8]
MON2 settings	MON[2]	-	-
MON3 settings	MON[3]	-	-

If individual monitor protection is desired this can be achieved through the use of register PROT\_MON (0xF3) as seen in figure Table 7-7.

Table 7-7. PROT\_MON Register Description

				_					
Register	Bit	7	6	5	4	3	2	1	0
PROT_MON (0xF3)	R/W	MON[8]	MON[7]	MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	MON[1]

Register PROT\_MON selects the monitor channel which is protected once PROT1 AND PROT2 registers are written to protect the MON group. Register PROT\_MON is set to a value of 0xFF by default, this makes it such that when MON protection is applied through registers PROT1 and PROT2 the protection is applied to all monitors. If a user wishes to not apply protection to a specific monitor channel then the user must set the bit corresponding to the monitor channel in question to a value of 0 prior to PROT1 and PROT2 being set.

At start up registers PROT1 and PROT2 are set to a default value of 0x00. Once a bit is set to 1 in PROT1 or PROT2 the bit will become read-only and cannot be cleared by a write command. To reset PROT1 and PROT2 the user can utilize RESET\_PROT, bit 3 of the VMON\_CTL register. RESET\_PROT is part of the WRKC register set therefore if the user desires to use RESET\_PROT's functionality WRKC protection should be included when configuring PROT1 and PROT2 protection registers. If WRKC protection is enabled when configuring PROT1 and PROT2 then protection registers can only be reset through a device power cycle.



#### 7.4 Device Functional Modes

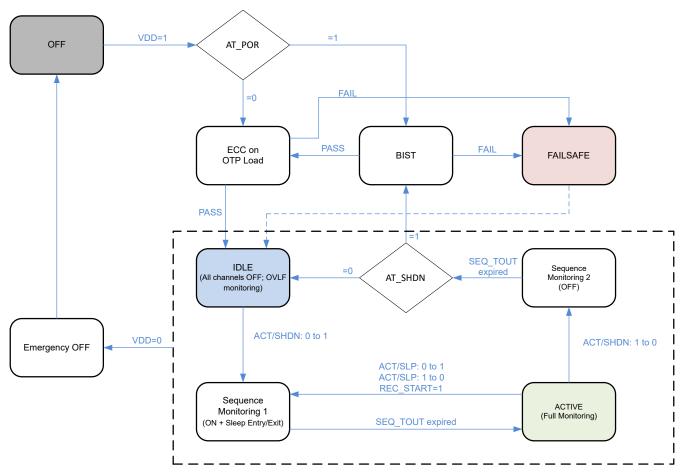


Figure 7-12. TPS389006/08-Q1,TPS389R0-Q1 State Diagram

## 7.4.1 Built-In Self Test and Configuration Load

Built-In Self Test (BIST) is performed:

- 1. At Power On Reset (POR), if TEST CFG.AT POR=1
- When exiting ACTIVE state due to ACT transitioning from 1→0, if TEST\_CFG.AT\_SHDN=1

Configuration load from OTP is assisted by ECC (supporting SEC-DED). This is to protect against data integrity issues and to maximize system availability.

During BIST, NIRQ is de-asserted (asserted in case of failure),NRST is asserted (for devices with NRST pin), input pins are ignored,  $\overline{\text{SYNC}}$  is tri-stated, and the I²C block is inactive with SDA and SCL de-asserted. The BIST includes device testing to meet the Functional Safety goals outlined in functional safety documentation. Once BIST is completed without failure, I²C is immediately active and the device enters the IDLE sate after loading the configuration data from OTP. If BIST fails and/or ECC reports Double-Error Detection (DED; meant for detecting multiple bit flips when loading data from memory), NIRQ and NRST (for devices with NRST pin) is asserted, the device enters FAILSAFE state, and a best effort attempt is made to keep the I²C function active. TEST\_INFO register can provide additional information on the test results.

The detailed behavior upon success/failure of the BIST is controlled by INT\_TEST and IEN\_TEST registers. Reporting of the BIST results is carried out through:

- NIRQ pin: pulled low depending on the test result and BIST C and BIST bits in IEN TEST
- NRST pin (if applicable): pulled low depending on the test result and BIST C and BIST bits in IEN TEST
- I BIST C and BIST bits in INT TEST register depending on IEN TEST settings



- VMON\_STAT.ST\_BIST\_C register bit
- TEST\_INFO[3:0] register bits

#### 7.4.1.1 Notes on BIST Execution

Upon Power-On-Reset, the TPS389006/08-Q1,TPS389R0-Q1 needs to make a decision whether to run BIST or not, based on the value of the TEST\_CFG.AT\_POR register bit. Assuming that ECC on this register is performed after BIST has checked the ECC logic itself, verification of the data integrity before running BIST is not possible.

#### 7.4.2 TPS389006/08-Q1,TPS389R0-Q1 Power ON

When the TPS389006/08-Q1,TPS389R0-Q1 is powered ON, BIST is optionally executed (depending on TEST\_CFG.AT\_POR register bit); I<sup>2</sup>C and fault reporting (through NIRQ) become active as soon as BIST is completed and configuration is loaded from OTP (assisted by ECC, supporting SEC-DED).

The details of the configuration load ECC and BIST results are reported in TEST\_INFO register.

Upon detection of the ACT rising edge, the TPS389006/08-Q1,TPS389R0-Q1 starts the sequence timeout timer and the monitoring of the power ON sequence. SLEEP is ignored until ACT is High and the sequence timeout has expired. The TPS389006/08-Q1,TPS389R0-Q1 will then act on SLEEP transitions to monitor/record Sleep Entry/Exit sequences.

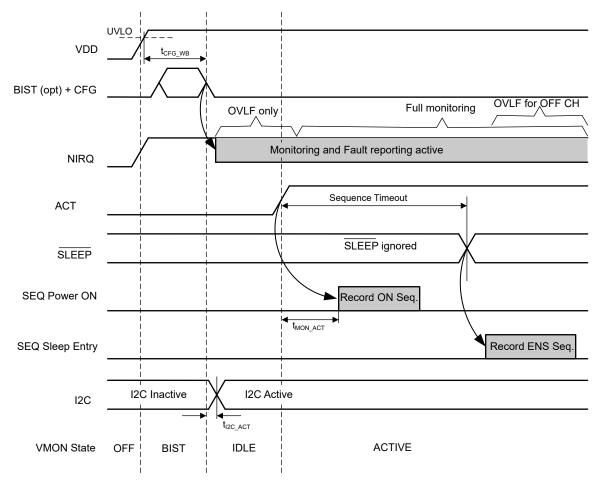


Figure 7-13. TPS389006/08-Q1 Power ON Signaling and Internal States

BIST completion can be detected through interrupt or register polling:

- Interrupt: INT TEST.I BIST C flag is set and NIRQ is asserted if IEN TEST.BIST C=1
- Polling: VMON STAT register can be polled to read the ST\_BIST\_C bit



## 7.4.3 General Monitoring

TPS389006/08 and TPS389R0 has multiple monitoring modes including IDLE, ACTIVE, SLEEP, and DEEP SLEEP. These modes refer to the monitoring states of the device shown in Table 7-8.

#### 7.4.3.1 IDLE Monitoring

The TPS389006/08-Q1,TPS389R0-Q1 is in IDLE state when ACT is Low and BIST is completed.

In this state, all monitored channels are expected to be in the OFF state (below the OFF threshold).

For the enabled channels in OFF state, only the Overvoltage Low Frequency (OVLF) thresholds are monitored to make sure the reliability limits are not violated.

#### 7.4.3.2 ACTIVE Monitoring

The TPS389006/08-Q1, TPS389R0-Q1 is in ACTIVE state when ACT is High.

VMON monitors high frequency channel levels (comparator sense path) and low frequency channel levels (ADC sense path) against Undervoltage High Frequency (UVHF), Overvoltage High Frequency (OVHF), Undervoltage Low Frequency (UVLF), and Overvoltage Low Frequency (OVLF) thresholds.

Some channels can be connected to rails which are controlled by user software. Such channels can be in the OFF state (below the OFF threshold) when the TPS389006/08-Q1,TPS389R0-Q1 is in an ACTIVE state, and have the UVLF/UVHF interrupts normally disabled. Once these rails are turned ON, the TPS389006/08-Q1,TPS389R0-Q1 host enables the channels UVLF/UVHF interrupts to allow full monitoring. Similarly, before these rails are turned OFF, the TPS389006/08-Q1,TPS389R0-Q1 host disables the channels UVLF/UVHF interrupts to avoid false UV violations during the ramp down. As these channels are not part of the sequencing initiated by ACT or SLEEP, the UVLF/UVHF/OVHF interrupts cannot be automatically enabled/disabled using the auto-mask registers. While in the OFF state, only the OVLF thresholds are monitored to make sure the reliability limits are not violated.

Other enabled channels can be in OFF state as a result of the SLEEP 1→0 transition sequence. Those channels are identified by the AMSK\_ENS auto-mask register, used to avoid UVLF interrupts (as well as UVHF and OVHF interrupts) during the transition. For those channels in the OFF state and identified by the AMSK\_ENS register, only the OVLF thresholds are monitored to make sure the reliability limits are not violated.

Monitored-Triggers NIRQ if CHx Mode **Pin/Bit Condition** Iq Status only **ADC/Telemetry** enabled ACT=High, **ACTIVE** OVLF, UVLF, OVHF, UVHF 1.5mA OFF **Fnabled** Sleep=High **IDLE** ACT=Low, Sleep=X 230uA **OVLF** OFF Disabled CHx not assigned to OVLF, UVLF, OVHF, UVHF OFF Sleep SLEEP ACT=High, CHx assigned to OFF 1.5mA **OVLF** Enabled Sleep (AMSK=1) SLEEP=Low Sleep Power bit=1 CHx assigned to OVLF, UVLF, OVHF, UVHF OFF Sleep (AMSK=0) CHx not assigned to OVHF, UVHF **DEEP SLEEP** Sleep ACT=High, CHx assigned to 330uA Disabled No monitoring Sleep (AMSK=1) SLEEP=Low Sleep Power bit=0 CHx assigned to OVHF, UVHF Sleep (AMSK=0)

**Table 7-8. Modes of Operation Summary** 

## 7.4.3.3 Sequence Monitoring 1

In addition to voltage monitoring, voltage rails sequences are also monitored on ACT and SLEEP changes, or on setting SEQ\_REC\_CTL.REC\_START=1.



Sequence Monitoring 1 is a transitional state entered when:

- 1. ACT transitions 0→1
- SLEEP transitions 0→1, if ACT=1
- 3. SLEEP transitions 1→0, if ACT=1
- 4. Host sets SEQ\_REC\_CTL.REC\_START=1

The first three transitions trigger the same set of actions, with the TPS389006/08-Q1,TPS389R0-Q1 always ending in the ACTIVE state. However, the registers used to log and check the sequencing information are different.

The fourth method to start sequence monitoring (register bit set by the host) gives the flexibility to the host to decide when and where to track a sequence while the external signals are static. This is useful, for example, when software shutdown is initiated using FORCE SHUTDOWN[1:0].

The following sections describe the actions for the first three cases explicitly for clarity.

#### 7.4.3.3.1 ACT Transitions 0→1

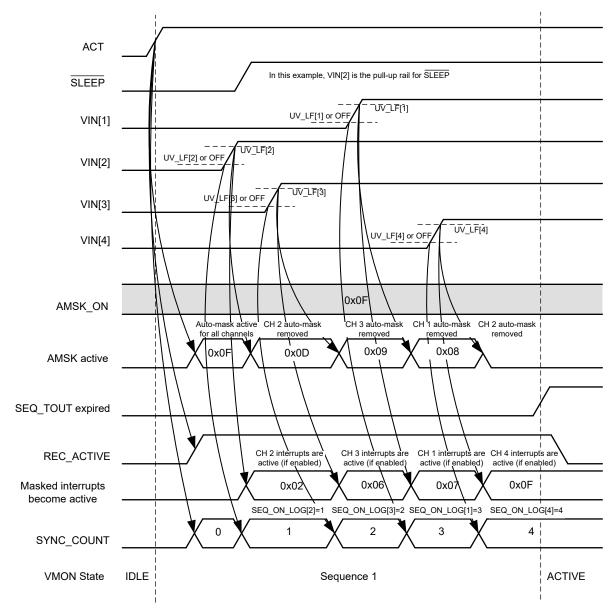


Figure 7-14. ACT 0→1 Transition

1. The TPS389006/08-Q1,TPS389R0-Q1 takes several actions on the ACT 0→1 transition:

- a. The synchronization counter is reset to 0.
- b. The REC\_ACTIVE bit is set, and SEQ[1:0] bits are updated to 00b.
- c. If the sequence overwrite bit is enabled (EN\_SEQ\_OW=1), the sequence logging registers (SEQ\_ON\_LOG[N]) are overwritten with new data. If there was data in the registers that was not read by the host (SEQ\_ON\_RDY still set), the sequence overwrite flag (SEQ\_ON\_OW) gets set.
- d. If the timestamps overwrite bit is enabled (EN\_TS\_OW=1), the timestamp logging registers (SEQ\_TIME\_xSB[N]) are overwritten with new data. If there was data in the registers that was not read by the host (TS\_RDY still set), the timestamp overwrite flag (TS\_OW) is set.
- e. If the sequence overwrite bit is disabled (EN\_SEQ\_OW=0) and there was data in the registers SEQ\_ON\_LOG[N] that was not read and acknowledged by the host (SEQ\_ON\_RDY still set), the sequence overwrite flag (SEQ\_ON\_OW) is set and does not overwrite the registers with new data.
- f. If the timestamp overwrite bit is disabled (EN\_TS\_OW=0) and there was data in the registers SEQ\_TIME\_xSB[N] that was not read and acknowledged by the host (TS\_RDY still set), the timestamp overwrite flag (TS\_OW) is set and does not overwrite the registers with new data.
- g. The internal sequence timer is (re)started.
- 2. All TPS389006/08-Q1,TPS389R0-Q1 inputs selected with auto-mask register AMSK\_ON start with masked (disabled) interrupts for Undervoltage Low Frequency (UVLF), Undervoltage High Frequency (UVHF), and Overvoltage High Frequency (OVHF) conditions.
- 3. As each rail passes the UVLF threshold (UV\_LF[N]), automatically (and expected to happen within about 5-10µs) the relevant UV and OV interrupts are unmasked and enabled/disabled according to the IEN\_UVLF, IEN\_UVHF, and IEN\_OVHF registers.
- 4. As each rail passes the UVLF or OFF threshold (depending on SEQ\_UP\_THLD.OFF\_UV[N] register setting), the rail is tagged with a counter corresponding to the order of rising edge transition. A timestamp is also logged.
  - a. the tag value stored in the relevant status register SEQ\_ON\_LOG[N] if allowed as per overwrite settings and status. also, the timestamp of the event is stored in registers SEQ\_TIME\_MSB[N] and SEQ\_TIME\_LSB[N] as allowed by the overwrite settings and status.
  - b. the SEQ\_ON\_LOG[N] register is compared to the expected sequence order value defined in register SEQ\_EXP[N], and an interrupt is generated if different and if the relevant interrupt enable bit is set (IEN\_SEQ\_ON). Note that if overwrite settings and recording status do not allow writing new data to the logging registers, then the comparison cannot be performed and no interrupt will be generated.
- 5. After a timeout, tagging stops.
  - a. Clear the REC ACTIVE bit.
  - b. If rails are up with the correct sequence, TPS389006/08-Q1,TPS389R0-Q1 is in ACTIVE state and starts normal monitoring.
  - c. If any rail has a tag not matching the configured value in SEQ\_ON\_EXP[N] register, NIRQ is asserted. The TPS389006/08-Q1,TPS389R0-Q1 continues normal monitoring.
  - d. If SLEEP is low, the TPS389006/08-Q1,TPS389R0-Q1 will not start recording the Sleep Entry sequence, as sequence recording is started on ACT and SLEEP transitions, or when initiated through I<sup>2</sup>C command.



#### 7.4.3.3.2 SLEEP Transition 1→0

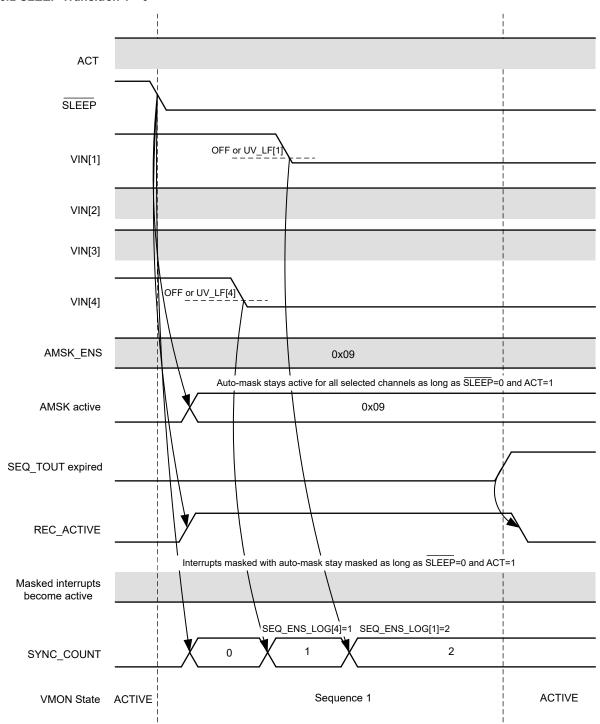


Figure 7-15. SLEEP  $1\rightarrow 0$  Transition

- 1. The TPS389006/08-Q1,TPS389R0-Q1 takes several actions on the  $\overline{\text{SLEEP}}$  1 $\rightarrow$ 0 transition:
  - a. The synchronization counter is reset to 0.
  - b. The REC\_ACTIVE bit is set, and SEQ[1:0] bits are updated to 11b.



- c. If the sequence overwrite bit is enabled (EN\_SEQ\_OW=1), the sequence logging registers (SEQ\_ENS\_LOG[N]) are overwritten with new data. If there was data in the registers that was not read by the host (SEQ\_ENS\_RDY still set), the timestamp overwrite flag (TS\_OW) is set.
- d. If the timestamp overwrite bit is enabled (EN\_TS\_OW=1), the timestamp logging registers (SEQ\_TIME\_xSB[N]) are overwritten with new data. If there was data in the registers that was not read by the host (TS\_RDY still set), the timestamp overwrite flag (TS\_OW) is set.
- e. If the sequence overwrite bit is disabled (EN\_SEQ\_OW=0) and there was data in the registers SEQ\_ENS\_LOG[N] that was not read and acknowledged by the host (SEQ\_ENS\_RDY still set), the sequence overwrite flag (SEQ\_ENS\_OW) is set, and the registers are not overwritten with new data.
- f. If the timestamp overwrite bit is disabled (EN\_TS\_OW=0) and there was data in the registers SEQ\_TIME\_xSB[N] that was not read and acknowledged by the host (TS\_RDY still set), the timestamp overwrite flag (TS\_OW) is set, and the registers are not overwritten with new data.
- g. The internal sequence timer is (re)started.
- 2. Relevant TPS389006/08-Q1,TPS389R0-Q1 inputs selected with auto-mask register AMSK\_ENS are set with masked interrupts for UVLF, UVHF and OVHF conditions.
- 3. As each rail passes the OFF or UVLF threshold (depending on SEQ\_DN\_THLD.OFF\_UV[N] register setting), the rail is tagged with a counter corresponding to the order of falling edge transition. A timestamp is also logged.
  - a. The tag value is stored in the relevant status register SEQ\_ENS\_LOG[N] if allowed as per overwrite settings and status. Also, the timestamp of the event is stored in registers SEQ\_TIME\_MSB[N] and SEQ\_TIME\_LSB[N] as allowed by the overwrite settings and status.
  - b. The SEQ\_ENS\_LOG[N] register is compared to the expected sequence order value defined in register SEQ\_ENS\_EXP[N], and an interrupt is generated if different and if the relevant interrupt enable bit is set (IEN\_SEQ\_ENS). Note that if overwrite settings and recording status do not allow writing new data to the logging registers, then the comparison cannot be performed and no interrupt is generated.
- 4. After timeout, tagging stops.
  - a. The REC ACTIVE bit is cleared.
  - b. If rails are down with the correct sequence, TPS389006/08-Q1,TPS389R0-Q1 is in ACTIVE state and continues normal monitoring (only OVLF thresholds are monitored for enabled channels in OFF state).

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#### 7.4.3.3.3 SLEEP Transition 0→1

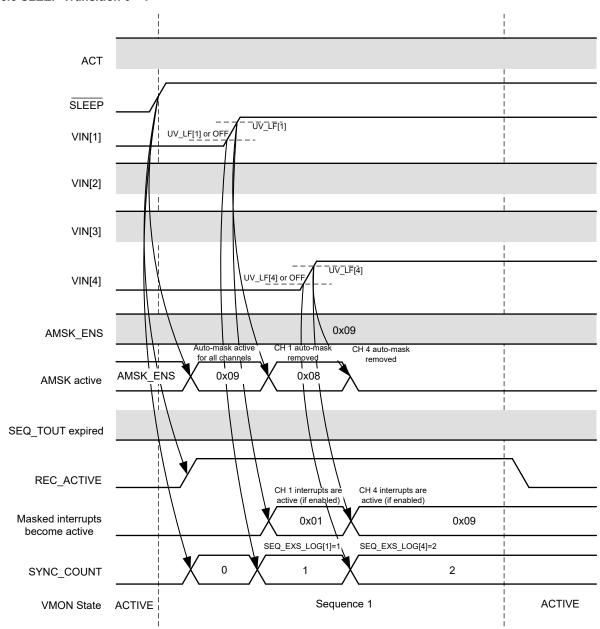


Figure 7-16. SLEEP 0→1 Transition

- 1. The TPS389006/08-Q1,TPS389R0-Q1 takes several actions on the  $\overline{\text{SLEEP}}$  0 $\rightarrow$ 1 transition:
  - a. The synchronization counter is reset to 0.
  - b. The REC\_ACTIVE bit is set, and SEQ[1:0] bits are updated to 10b.
  - c. If the sequence overwrite bit is enabled (EN\_SEQ\_OW=1), the sequence logging registers (SEQ\_EXS\_LOG[N]) are overwritten with new data. If there was data in the registers that was not read by the host (SEQ\_EXS\_RDY still set), the sequence overwrite flag (SEQ\_EXS\_OW) is set.
  - d. If the timestamp overwrite bit is enabled (EN\_TS\_OW=1), the timestamp logging registers (SEQ\_TIME\_xSB[N]) are overwritten with new data. If there was data in the registers that was not read by the host (TS\_RDY still set), the timestamp overwrite flag (TS\_OW) is set.



- e. If the sequence overwrite bit is disabled (EN\_SEQ\_OW=0) and there was data in the registers SEQ\_EXS\_LOG[N] that was not read and acknowledged by the host (SEQ\_EXS\_RDY still set), the sequence overwrite flag (SEQ\_EXS\_OW) is set, and the registers are not overwritten with new data.
- f. If the timestamp overwrite bit is disabled (EN\_TS\_OW=0) and there was data in the registers SEQ\_TIME\_xSB[N] that was not read and acknowledged by the host (TS\_RDY still set), the timestamp overwrite flag (TS\_OW) is set, and the registers are not overwritten with new data.
- g. The internal sequence timer is (re)started.
- 2. Relevant TPS389006/08-Q1,TPS389R0-Q1 inputs selected with auto-mask register AMSK\_EXS are set with masked (disabled) interrupts for UVLF, UVHF, and OVHF conditions.
- 3. As each rail passes the UVLF threshold (UV\_LF[N]), automatically (and expected to happen within about 5-10 μs) the relevant UV and OV interrupts are unmasked and enabled/disabled according to the IEN\_UVLF, IEN\_UVHF, and IEN\_OVHF registers.
- 4. As each rail passes the UVLF or OFF threshold (depending on SEQ\_UP\_THLD.OFF\_UV[N] register setting), the rail is tagged with a counter corresponding to the order of rising edge transition. A timestamp is also logged.
  - a. The tag value is stored in the relevant status register SEQ\_EXS\_LOG[N] if allowed as per overwrite settings and status. Also, the timestamp of the event is stored in registers SEQ\_TIME\_MSB[N] and SEQ\_TIME\_LSB[N] as allowed by the overwrite settings and status.
  - b. The SEQ\_EXS\_LOG[N] register is compared to the expected sequence order value defined in register SEQ\_EXS\_EXP[N], and an interrupt is generated if different and if relevant interrupt enable bit is set (IEN\_SEQ\_EXS). Note that if overwrite settings and recording status do not allow writing new data to the logging registers, then the comparison cannot be performed and no interrupt is generated.
- 5. After a timeout, tagging stops.
  - a. The REC ACTIVE bit is cleared.
  - b. If rails are up with the correct sequence, TPS389006/08-Q1,TPS389R0-Q1 is in ACTIVE state and starts normal monitoring.
  - c. If any rail has a tag not matching the configured value in SEQ\_EXS\_EXP[N] register, NIRQ is asserted. TPS389006/08-Q1,TPS389R0-Q1 continues normal monitoring.

#### 7.4.3.4 Sequence Monitoring 2

Sequence Monitoring 2 is very similar to Sequence Monitoring 1, however, an extra step is taken when exiting this transitioning state depending on the TEST\_CFG.AT\_SHDN register bit.

Sequence Monitoring 2 is entered when ACT transitions  $1\rightarrow 0$ . The actions taken are described in Section 7.4.3.4.1.

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#### 7.4.3.4.1 ACT Transition 1→0

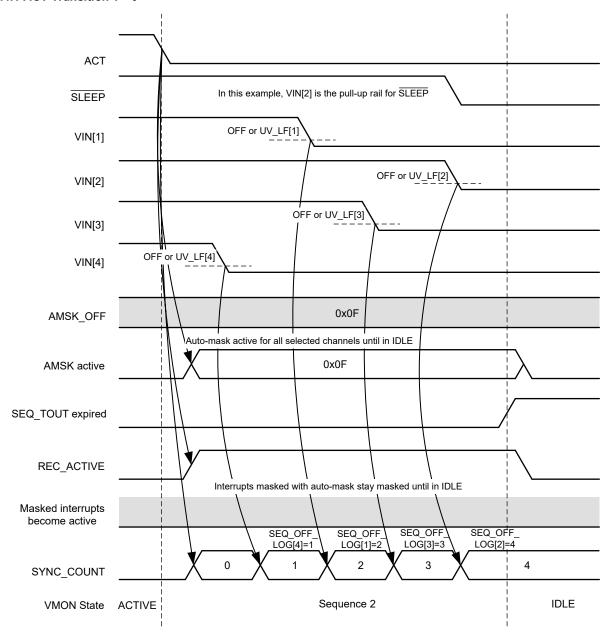


Figure 7-17. ACT 1→0 Transition

- 1. The TPS389006/08-Q1,TPS389R0-Q1 takes several actions on the ACT 1→0 transition:
  - a. The synchronization counter is reset to 0.
  - b. The REC\_ACTIVE bit is set, and SEQ[1:0] bits are updated to 01b.
  - c. If the sequence overwrite bit is enabled (EN\_SEQ\_OW=1), the sequence logging registers (SEQ\_OFF\_LOG[N]) are overwritten with new data. If there was data in the registers that was not read by the host (SEQ\_OFF\_RDY still set), the sequence overwrite flag (SEQ\_OFF\_OW) is set.
  - d. If the timestamp overwrite bit is enabled (EN\_TS\_OW=1), the timestamp logging registers (SEQ\_TIME\_xSB[N]) are overwritten with new data. If there was data in the registers that was not read by the host (TS\_RDY still set), the timestamp overwrite flag (TS\_OW) is set.



- e. If the sequence overwrite bit is disabled (EN\_SEQ\_OW=0) and there was data in the registers SEQ\_OFF\_LOG[N] that was not read and acknowledged by the host (SEQ\_OFF\_RDY still set), the sequence overwrite flag (SEQ\_OFF\_OW) is set, and the registers are not overwritten with new data.
- f. If the timestamp overwrite bit is disabled (EN\_TS\_OW=0) and there was data in the registers SEQ\_TIME\_xSB[N] that was not read and acknowledged by the host (TS\_RDY still set), the timestamp overwrite flag (TS\_OW) is set, and the registers are not overwritten with new data.
- g. The internal sequence timer is (re)started.
- 2. All TPS389006/08-Q1,TPS389R0-Q1 inputs selected with auto-mask register AMSK\_OFF are set with masked (disabled) interrupts for UVLF, UVHF, and OVHF conditions.
- 3. As each rail passes the OFF or UVLF threshold (depending on SEQ\_DN\_THLD.OFF\_UV[N] register setting), the rail is tagged with a counter corresponding to the order of falling edge transition. A timestamp is also logged.
  - a. The tag value is stored in the relevant status register SEQ\_OFF\_LOG[N] if allowed as per overwrite settings and status. Also, the timestamp of the event is stored in registers SEQ\_TIME\_MSB[N] and SEQ\_TIME\_LSB[N] as allowed by the overwrite settings and status.
  - b. The SEQ\_OFF\_LOG[N] register is compared to the expected sequence order value defined in register SEQ\_OFF\_EXP[N], and an interrupt is generated if different and if relevant interrupt enable bit is set (IEN\_SEQ\_OFF). Note that if overwrite settings and recording status do not allow writing new data to the logging registers, then the comparison cannot be performed and no interrupt will be generated.
- 4. After timeout, tagging stops.
  - a. The REC ACTIVE bit is cleared.
  - b. If rails are down with the correct sequence, proceed to check TEST\_CFG.AT\_SHDN register bit.
  - c. If any rail has a tag not matching the configured value in SEQ\_OFF\_EXP[N] register, NIRQ is asserted. TPS389006/08-Q1,TPS389R0-Q1 proceeds to check TEST\_CFG.AT\_SHDN register bit.
- 5. If TEST CFG.AT SHDN register bit is set, BIST is executed (next state depends on BIST results).
- 6. If TEST\_CFG.AT\_SHDN register bit is no set, the TPS389006/08-Q1,TPS389R0-Q1 enters IDLE state.



#### 7.5 Register Maps

The register map is designed to support up to 16 channels through register banks, with the following organization:

- Bank 0 Status Register Set Summary:
  - Vendor info and usage registers (bank independent)
  - Interrupt registers
  - Status registers
  - Bank selection register (bank independent)
  - Protection registers (bank independent)
  - Device configuration registers (bank independent)
- Bank 1 Channel 1-8 Configuration Register Set Summary:
  - Vendor info and usage registers (bank independent)
  - Control registers (device global registers)
  - Monitor configuration registers (channel specific registers)
  - Sequence configuration registers (both device global and channel specific registers)
  - Bank selection register (bank independent)
  - Protection registers (bank independent)
  - Device configuration registers (bank independent)

Bank independent registers are accessible at the same address irrespective of the current bank selection. Access to other registers requires the proper bank being selected.

All registers are 8-bit wide, and are loaded at boot with the default value described here or with the OTP value programmed at the factory.

Unused registers addresses are reserved for future use and support up to 16 channels.

Write accesses to protected registers (see PROT1/2 details), invalid registers, or valid registers with invalid data, should be NACK'd.

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### 7.5.1 BANK0 Registers

Table 7-9 lists the memory-mapped registers for the BANK0 registers. All register offset addresses not listed in Table 7-9 should be considered as reserved locations and the register contents should not be modified.

Table 7-9. BANK0 Registers

			Table 7-9. BANKU Registers								
Addres s	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
0x10	INT_SRC	F_OTHER		RESE	RVED		TEST	CONTROL	MONITOR		
0x11	INT_MONITOR	SEQ_ON	SEQ_OFF	SEQ_EXS	SEQ_ENS	OV_LF	OV_HF	UV_LF	UV_HF		
0x12	INT_UVHF				UVH	IF[N]					
0x14	INT_UVLF				UVL	.F[N]					
0x16	INT_OVHF				OVH	IF[N]					
0x18	INT_OVLF				OVL	.F[N]					
0x1A	INT_SEQ_ON				F_SEQ	_ON[N]					
0x1C	INT_SEQ_OFF				F_SEQ	_OFF[N]					
0x1E	INT_SEQ_EXS				F_SEQ	_EXS[N]					
0x20	INT_SEQ_ENS				F_SEQ_	_ENS[N]					
0x22	INT_CONTROL		RESERVED		F_CRC	F_NIRQ	F_TSD	F_SYNC	F_PEC		
0x23	INT_TEST		RESE	RVED		ECC_SEC	ECC_DED	I_BIST_C	BIST		
0x24	INT_VENDOR	Self- Test_CRC	LDO_OV_Er ror	NRST_mism atch	Freq_DEV_ Error	SHORT_DE T	OPEN_DET	RESE	RVED		
0x30	VMON_STAT	FAILSAFE	ST_BIDT_C	ST_VDD	ST_NIRQ	ST_ACTSL P	ST_ACTSH DN	ST_SYNC	RESERVED		
0x31	TEST_INFO	RESE	RESERVED ECC_SEC			BIST_VM	BIST_NVM	BIST_L	BIST_A		
0x32	OFF_STAT				VIN	VIN[N]					
0x34	SEQ_REC_STAT	REC_ACTIV E	SI	ΕQ	TS_RDY	SEQ_ON_R DY	SEQ_OFF_ RDY	SEQ_EXS_ RDY	SEQ_ENS_ RDY		
0x35	SEQ_OW_STAT		RSVD		TS_OW	SEQ_ON_O W	SEQ_OFF_ OW	SEQ_EXS_ OW	SEQ_ENS_ OW		
0x36	SEQ_ORD_STA T				SYNC_C	OUNT[7:0]					
0x40	MON_LVL[1]				ADC	[7:0]					
0x41	MON_LVL[2]				ADC	ADC[7:0]					
0x42	MON_LVL[3]				ADC	C[7:0]					
0x43	MON_LVL[4]				ADC[7:0]						
0x44	MON_LVL[5]				ADC	C[7:0]					
0x45	MON_LVL[6]				ADC	[7:0]					
0x46	MON_LVL[7]				ADC	[7:0]					
0x47	MON_LVL[8]				ADC	[7:0]					
0x50	SEQ_ON_LOG[1 ]				ORDE	ER[7:0]					
0x51	SEQ_ON_LOG[2 ]	ORDER[7:0]									
0x52	SEQ_ON_LOG[3	ORDER[7:0]									
0x53	SEQ_ON_LOG[4	ORDER[7:0]									
0x54	SEQ_ON_LOG[5				ORDE	ER[7:0]					
0x55	SEQ_ON_LOG[6				ORDE	ER[7:0]					
	·	1									



Table 7-9. BANK0 Registers (continued)

			Table 1-3	. BANKO R	egisters (c	onunueu)			
Addres s	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x56	SEQ_ON_LOG[7			1	ORDE	R[7:0]		1	
0x57	SEQ_ON_LOG[8				ORDE	ER[7:0]			
0x60	SEQ_OFF_LOG[ 1]				ORDE	ER[7:0]			
0x61	SEQ_OFF_LOG[ 2]				ORDE	ER[7:0]			
0x62	SEQ_OFF_LOG[				ORDE	ER[7:0]			
0x63	SEQ_OFF_LOG[ 4]				ORDE	ER[7:0]			
0x64	SEQ_OFF_LOG[ 5]				ORDE	ER[7:0]			
0x65	SEQ_OFF_LOG[ 6]				ORDE	ER[7:0]			
0x66	SEQ_OFF_LOG[ 7]				ORDE	ER[7:0]			
0x67	SEQ_OFF_LOG[ 8]				ORDE	ER[7:0]			
0x70	SEQ_EXS_LOG[ 1]				ORDE	ER[7:0]			
0x71	SEQ_EXS_LOG[ 2]				ORDE	ER[7:0]			
0x72	SEQ_EXS_LOG[				ORDE	ER[7:0]			
0x73	SEQ_EXS_LOG[ 4]				ORDE	ER[7:0]			
0x74	SEQ_EXS_LOG[ 5]				ORDE	ER[7:0]			
0x75	SEQ_EXS_LOG[ 6]				ORDE	ER[7:0]			
0x76	SEQ_EXS_LOG[ 7]				ORDE	ER[7:0]			
0x77	SEQ_EXS_LOG[ 8]				ORDE	ER[7:0]			
0x80	SEQ_ENS_LOG[ 1]				ORDE	ER[7:0]			
0x81	SEQ_ENS_LOG[ 2]				ORDE	ER[7:0]			
0x82	SEQ_ENS_LOG[ 3]				ORDE	ER[7:0]			
0x83	SEQ_ENS_LOG[ 4]				ORDE	ER[7:0]			
0x84	SEQ_ENS_LOG[ 5]				ORDE	ER[7:0]			
0x85	SEQ_ENS_LOG[ 6]				ORDE	ER[7:0]			
0x86	SEQ_ENS_LOG[ 7]				ORDE	ER[7:0]			
0x87	SEQ_ENS_LOG[ 8]				ORDE	ER[7:0]			

Table 7-9. BANKO Registers (continued)

	Table 7-9. BANK0 Registers (continued)								
Addres s	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x90	SEQ_TIME_MS B[1]		CLOCK[7:0]						
0x91	SEQ_TIME_LS B[1]				CLOC	CK[7:0]			
0x92	SEQ_TIME_MS B[2]				CLOC	CK[7:0]			
0x93	SEQ_TIME_LS B[2]				CLOC	CK[7:0]			
0x94	SEQ_TIME_MS B[3]				CLOC	CK[7:0]			
0x95	SEQ_TIME_LS B[3]				CLOC	K[7:0]			
0x96	SEQ_TIME_MS B[4]				CLOC	CK[7:0]			
0x97	SEQ_TIME_LS B[4]		CLOCK[7:0]						
0x98	SEQ_TIME_MS B[5]		CLOCK[7:0]						
0x99	SEQ_TIME_LS B[5]				CLOC	CK[7:0]			
0x9A	SEQ_TIME_MS B[6]				CLOC	K[7:0]			
0x9B	SEQ_TIME_LS B[6]				CLOC	CK[7:0]			
0x9C	SEQ_TIME_MS B[7]				CLOC	CK[7:0]			
0x9D	SEQ_TIME_LS B[7]				CLOC	CK[7:0]			
0x9E	SEQ_TIME_MS B[8]				CLOC	CK[7:0]			
0x9F	SEQ_TIME_LS B[8]		CLOCK[7:0]						
0xF0	BANK_SEL	RESERVED BANK SELECTION				BANK SELECTION			
0xF1	PROT1	RESERVED WRKC WRKS CFG IEN MON SEQ				SEQ			
0xF2	PROT2	RESE	RVED	WRKC	WRKS	CFG	IEN	MON	SEQ
0xF3	PROT_MON2	RESE	RVED		1	MO	 N[N]	1	1
0xF9	I2CADDR	RESERVED		ADDR_N	NVM[3:0]			DDR_STRAP[	2:0]
0xFA	DEV_CFG				RESERVED		1	<del>-</del>	SOC_IF

Complex bit access types are encoded to fit into small table cells. Table 7-10 shows the codes that are used for access types in this section.

Table 7-10. BANKO Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear



Table 7-10. BANK0 Access Type Codes (continued)

Access Type	Code	Description
Reset or Default	Value	
-n		Value after reset or the default value

### 7.5.1.1 INT\_SRC Register (Address = 0x10) [Reset = 0xX0]

INT SRC is shown in Table 7-11.

Return to the Summary Table.

Global Interrupt Source Status register. This register contains fault interrupts on UV/OV HF/LF interrupts and internal fault interrupt and other interrupt. INT\_SRC represents the reason why NIRQ was asserted. When the host processor receives NIRQ, the processor can read this register to quickly determine the source of the interrupt. If this register is clear, then the device did not assert NIRQ.

Table 7-11. INT SRC Register Field Descriptions

D:4				Beautistics
Bit	Field	Туре	Reset	Description
7	F_OTHER	R	Ob	Vendor specific internal fault.  Details reported in INT_F_OTHER.  This bit represents the ORed value of all bits in INT_F_OTHER.  0b = No fault reported in INT_F_OTHER  1b = Fault reported in INT_F_OTHER
6:3	RESERVED	R	b	Reserved
2	TEST	R	xb	Internal test or configuration load fault. Details reported in INT_TEST. Represents ORed value of all bits in INT_TEST. 0b = No test/configuration fault detected 1b = Test/configuration fault detected
1	CONTROL	R	xb	Control status or communication fault.  Details reported in INT_CONTROL.  Represents ORed value of all bits in INT_CONTROL.  0b = No status or communication fault detected  1b = Status or communication fault detected
0	MONITOR	R	xb	Voltage or sequence monitor fault. Details reported in INT_MONITOR. Represents ORed value of all bits in INT_MONITOR.  0b = No voltage or sequence fault detected 1b = Voltage or sequence fault detected

#### 7.5.1.2 INT\_MONITOR Register (Address = 0x11) [Reset = 0xX0]

INT MONITOR is shown in Table 7-12.

Return to the Summary Table.

Voltage and Sequence Monitor Interrupt Status register. This register contains fault interrupts for sequence entry/exit from act/sleep modes and HF and LF faults.

Table 7-12. INT\_MONITOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	SEQ_ON	R	Ob	Power ON Sequence Fault.  Details reported in INT_SEQ_ON.  Represents ORed value of all bits in INT_SEQ_ON.  A Power ON Sequence fault occurs when the content of SEQ_ON_LOG[N] register does not match the value defined in SEQ_ON_EXP[N] register.  0b = No Power ON Sequence fault detected  1b = Power ON Sequence fault detected

Table 7-12. INT\_MONITOR Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
6	SEQ_OFF	R	0b	Power OFF Sequence Fault.  Details reported in INT_SEQ_OFF.  Represents ORed value of all bits in INT_SEQ_OFF.  A Power OFF Sequence fault occurs when the content of SEQ_OFF_LOG[N] register does not match the value defined in SEQ_OFF_EXP[N] register.  0b = No Power OFF Sequence fault detected  1b = Power OFF Sequence fault detected
5	SEQ_EXS	R	Ob	Exit Sleep Sequence Fault.  Details reported in INT_SEQ_EXS.  Represents ORed value of all bits in INT_SEQ_EXS.  An Exit Sleep Sequence fault occurs when the content of SEQ_EXS_LOG[N] register does not match the value defined in SEQ_EXS_EXP[N] register.  0b = No Exit Sleep Sequence fault detected  1b = Exit Sleep Sequence fault detected
4	SEQ_ENS	R	Ob	Entry Sleep Sequence Fault.  Details reported in INT_SEQ_ENS.  Represents ORed value of all bits in INT_SEQ_ENS.  An Entry Sleep Sequence fault occurs when the content of SEQ_ENS_LOG[N] register does not match the value defined in SEQ_ENS_EXP[N] register.  0b = No Entry Sleep Sequence fault detected  1b = Entry Sleep Sequence fault detected
3	OV_LF	R	xb	Overvoltage Low Frequency Fault. Details reported in INT_OVLF. Represents ORed value of all bits in INT_OVLF. 0b = No OVLF fault detected 1b = OVLF fault detected
2	OV_HF	R	xb	Overvoltage High Frequency Fault.  Details reported in INT_OVHF.  Represents ORed value of all bits in INT_OVHF.  0b = No OVHF fault detected  1b = OVHF fault detected
1	UV_LF	R	xb	Undervoltage Low Frequency Fault.  Details reported in INT_UVLF.  Represents ORed value of all bits in INT_UVLF.  0b = No UVLF fault detected  1b = UVLF fault detected
0	UV_HF	R	xb	Undervoltage High Frequency Fault.  Details reported in INT_UVHF.  Represents ORed value of all bits in INT_UVHF.  0b = No UVHF fault detected  1b = UVHF fault detected

## 7.5.1.3 INT\_UVHF Register (Address = 0x12) [Reset = 0xX0]

INT\_UVHF is shown in Table 7-13.

Return to the Summary Table.

High Frequency channel Undervoltage Interrupt Status register. This register contains informtation on which channel had a UV HF fault.



### Table 7-13. INT\_UVHF Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	UVHF[N]	R/W1C	xxxxb	Undervoltage High Frequency Fault for channel N (1 through 8). Trips if channel N High Frequency signal goes below UV_HF[N]. The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (channel N High Frequency signal is above UV_HF[N]). 0b = Channel N has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1b = Channel N has UVHF fault detected

#### 7.5.1.4 INT\_UVLF Register (Address = 0x14) [Reset = 0xX0]

INT\_UVLF is shown in Table 7-14.

Return to the Summary Table.

Low Frequency channel Undervoltage Interrupt Status register. This register contains informtation on which channel had a UV LF fault.

Table 7-14. INT\_UVLF Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	UVLF[N]	R/W1C	xxxxb	Undervoltage Low Frequency Fault for channel N (1 through 8). Trips if channel N Low Frequency signal goes below UV_LF[N]. The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the UVLF fault condition is also removed (channel N Low Frequency signal is above UV_LF[N]). 0b = Channel N has no UVLF fault detected (or interrupt disabled in IEN_UVLF register) 1b = Channel N has UVLF fault detected

#### 7.5.1.5 INT\_OVHF Register (Address = 0x16) [Reset = 0xX0]

INT\_OVHF is shown in Table 7-15.

Return to the Summary Table.

High Frequency channel Overvoltage Interrupt Status register. This register contains informtation on which channel had an OV HF fault.

Table 7-15. INT\_OVHF Register Field Descriptions

			_	•
Bit	Field	Туре	Reset	Description
7:0	OVHF[N]	R/W1C	xxxxb	Overvoltage High Frequency Fault for channel N (1 through 8). Trips if channel N High Frequency signal goes above OV_HF[N]. The recovery of the fault condition does NOT clear the bit. The faultcan only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (channel N High Frequency signal is below OV_HF[N]). Ob = Channel N has noOVHF fault detected (or interrupt disabled in IEN_OVHF register)  1b = Channel N has OVHF fault detected

### 7.5.1.6 INT\_OVLF Register (Address = 0x18) [Reset = 0xX0]

INT\_OVLF is shown in Table 7-16.

Return to the Summary Table.

Low Frequency channel Overvoltage Interrupt Status register. This register contains informtation on which channel had an OV LF fault.

Table 7-16. INT\_OVLF Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	OVLF[N]	R/W1C	xxxxb	Overvoltage Low Frequency Fault for channel N (1 through 8). Trips if channel N Low Frequency signal goes above OV_LF[N]. The recovery of the fault condition does NOT clear the bit. The fault only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the OVLF fault condition is also removed (channel N Low Frequency signal is below OV_LF[N]). 0b = Channel N has no OVLF fault detected (or interrupt disabled in IEN_OVLF register) 1b = Channel N has OVLF fault detected

#### 7.5.1.7 INT\_SEQ\_ON Register (Address = 0x1A) [Reset = 0xX0]

INT\_SEQ\_ON is shown in Table 7-17.

Return to the Summary Table.

Power ON Sequence (ACT/ SLEEP 0 to 1) Interrupt Status register. This register contains informtation on which channel did not follow on sequence.

Table 7-17. INT\_SEQ\_ON Register Field Descriptions

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Bit	Field	Туре	Reset	Description
7:0	F_SEQ_ON[N]	R/W1C	xxxxb	Power ON Sequence Fault for channel N (1 through 8). Trips if channel N recorded Power ON Sequence counter in SEQ_ON_LOG[N] register does not match the value defined in SEQ_ON_EXP[N] register. The recovery of the fault condition does NOT clear the bit.The fault only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit. The bit sets again during next sequence if the same fault is detected. 0b = Channel N has no Power ON Sequence fault detected (or interrupt disabled in IEN_SEQ_ON register) 1b = Channel N has Power ON Sequence fault detected

#### 7.5.1.8 INT\_SEQ\_OFF Register (Address = 0x1C) [Reset = 0xX0]

INT\_SEQ\_OFF is shown in Table 7-18.

Return to the Summary Table.

Power OFF Sequence (ACT/ SLEEP 1 to 0) Interrupt Status register. This register contains informtation on which channel did not follow off sequence.

Table 7-18. INT\_SEQ\_OFF Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	F_SEQ_OFF[N]	R/W1C	xxxxb	Power OFF Sequence Fault for channel N (1 through 8). Trips if channel N recorded Power OFF Sequence counter in SEQ_OFF_LOG[N] register does not match the value defined in SEQ_OFF_EXP[N] register. The recovery of the fault condition does NOT clear the bit. The fault only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit. The bit sets again during next sequence if the same fault is detected. 0b = Channel N has no Power OFF Sequence fault detected (or interrupt disabled in IEN_SEQ_OFF register) 1b = Channel N has Power OFF Sequence fault detected

#### 7.5.1.9 INT\_SEQ\_EXS Register (Address = 0x1E) [Reset = 0xX0]

INT\_SEQ\_EXS is shown in Table 7-19.

Return to the Summary Table.

Exit Sleep Sequence (ACT/ SLEEP 0 to 1) Interrupt Status register. This register contains informtation on which channel did not follow sleep exit sequence.

Table 7-19. INT SEQ EXS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	F_SEQ_EXS[N]	R/W1C	xxxxb	Exit Sleep Sequence Fault for channel N (1 through 8).  Trips if channel N recorded Exit Sleep Sequence counter in SEQ_EXS_LOG[N] register does not match the value defined in SEQ_EXS_EXP[N] register.  The recovery of the fault condition does NOT clear the bit. The fault only be cleared by the host with a write-1-to-clear.  Write-1-to-clear clears the bit.  The bit sets again during next sequence if the same fault is detected.  0b = Channel N has no Exit Sleep Sequence fault detected (or interrupt disabled in IEN_SEQ_EXS register)  1b = Channel N has Exit Sleep Sequence fault detected

#### 7.5.1.10 INT\_SEQ\_ENS Register (Address = 0x20) [Reset = 0xX0]

INT SEQ ENS is shown in Table 7-20.

Return to the Summary Table.

Entry Sleep Sequence (SLEEP 1 to 0) Interrupt Status register. This register contains information on which channel did not follow sleep entry sequence.

Table 7-20. INT\_SEQ\_ENS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	F_SEQ_ENS[N]	R/W1C	xxxxb	Entry Sleep Sequence Fault for channel N (1 through 8).  Trips if channel N recorded Entry Sleep Sequence counter in SEQ_ENS_LOG[N] register does not match the value defined in SEQ_ENS_EXP[N] register.  0b = Channel N has no Entry Sleep Sequence fault detected (or interrupt disabled in IEN_SEQ_ENS register)  1b = Channel N has Entry Sleep Sequence fault detected

## 7.5.1.11 INT\_CONTROL Register (Address = 0x22) [Reset = 0xX0]

INT CONTROL is shown in Table 7-21.

Return to the Summary Table.

Control and Communication Interrupt Status Register.

Table 7-21. INT\_CONTROL Register Field Descriptions

<b>_</b>				
Bit	Field	Туре	Reset	Description
7:5	RESERVED	R	b	Reserved
4	F_CRC	R/W1C	Ob	Runtime register CRC Fault: The recovery of the fault condition does NOT clear the bit. The fault only be cleared by the host with a write-1-to-clear.  Write-1-to-clear clears the bit.  The bit sets again during next register CRC check if the same fault is detected.  0b = No fault detected (or IEN_CONTROL.RT_CRC is disabled)  1b = Register CRC fault detected

Table 7-21. INT\_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description (Softmaca)
3	F_NIRQ	R/W1C	xb	Interrupt pin fault (fault bit always enabled no enable bit available): The recovery of the fault condition does NOT clear the bit. The fault only be cleared by the host with a write-1-to-clear.  Write-1-to-clear clears the bit only if the NIRQ fault condition is also removed.  0b = No fault detected on NIRQ pin 1b = Low resistance path to supply detected on NIRQ pin
2	F_TSD	R/W1C	xb	Thermal Shutdown fault: The recovery of the fault condition does NOT clear the bit. The fault only be cleared by the host with a write-1-to-clear.  Write-1-to-clear clears the bit only if the TSD fault condition is also removed.  0b = No TSD fault detected (or IEN_CONTROL.TSD is disabled) 1b = TSD fault detected
1	F_SYNC	R/W1C	xb	\$\overline{\subsetsYNC}\$ pin fault: The recovery of the fault condition does NOT clear the bit. The fault only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the \$\overline{\subsetsYNC}\$ fault condition is also removed.  0b = No fault detected on \$\overline{\subsetsYNC}\$ pin (or IEN_CONTROL.SYNC is disabled)  1b = Low resistance path to supply detected on \$\overline{\subsetsYNC}\$ pin
0	F_PEC	R/W1C	xb	Packet Error Checking fault: The recovery of the fault condition does NOT clear the bit. The fault only be cleared by the host with a write-1-to-clear.  Write-1-to-clear clears the bit.  The bit will be set again during next I2C transaction if the same fault is detected.

### 7.5.1.12 INT\_TEST Register (Address = 0x23) [Reset = 0xX0]

INT\_TEST is shown in Table 7-22.

Return to the Summary Table.

Internal Test and Configuration Load Interrupt Status Register.

Table 7-22. INT\_TEST Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:4	RESERVED	R	b	Reserved
3	ECC_SEC	R/W1C	xb	ECC single-error corrected on OTP configuration load: Write-1-to-clear clears the bit.  The bit will be set again during next OTP configuration load if the same fault is detected.  0b = No single-error corrected (or IEN_TEST.ECC_SEC is disabled)  1b = Single-error corrected
2	ECC_DED	R/W1C	xb	ECC double-error detected on OTP configuration load: The fault bit is always enabled (there is no associated interrupt enable bit). Write-1-to-clear clears the bit. The bit will be set again during next OTP configuration load if the same fault is detected.  0b = No double-error detected on OTP load 1b = Double-error detected on OTP load
1	I_BIST_C	R/W1C	xb	Indication of Built-In Self-Test complete: Write-1-to-clear clears the bit.  The bit sets again on completion of next BIST execution.Write-1-to-clear clears the bit.  The bit sets again on completion of next BIST execution.  Ob = BIST not complete (or IEN_TEST.BIST_C is disabled)  1b = BIST complete



Table 7-22. INT\_TEST Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
0	BIST	R/W1C	xb	Built-In Self-Test fault: Write-1-to-clear clears the bit. The bit sets again during next BIST execution if the same fault is detected.  0b = No BIST fault detected (or IEN_TEST.BIST is disabled) 1b = BIST fault detected

### 7.5.1.13 INT\_VENDOR Register (Address = 0x24) [Reset = 0xX0]

INT\_VENDOR is shown in Table 7-23.

Return to the Summary Table.

This register contains various internal faults and ADDR detect pin fault.

Table 7-23. INT\_VENDOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	Self-Test_CRC	R/W1C	0b	Startup register CRC 0b 0= Self-test Pass 0b 1 = Self-test Fail Write- 1-to clear
6	LDO_OV_Error	R/W1C	Ob	Internal LDO fault: 0 = No internal LDO fault detected 1 = Internal LDO fault detected Write- 1-to-clear clears the bit.
5	NRST_mismatch	R/W1C	0b	NRST PIN drive state and read back state error 1b = Mismatch fault detected The recovery of the fault condition does NOT clear the bit.The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the NRST fault condition is also removed.
4	Freq_DEV_Error	R/W1C	0b	Internal Oscillator fault:  0 = No internal oscillator fault detected  1 = Internal oscillator fault detected Write-  1-to-clear clears the bit.
3	SHORT_DET	R/W1C	xb	Address Pin fault: 0 = No address pin fault detected 1 = Address pin fault detected Write- 1-to-clear clears the bit.
2	OPEN_DET	R/W1C	xb	Address Pin fault: 0 = No address pin fault detected 1 = Address pin fault detected Write- 1-to-clear clears the bit.
1:0	RESERVED	R	b	Reserved

## 7.5.1.14 VMON\_STAT Register (Address = 0x30) [Reset = 0xX0]

VMON\_STAT is shown in Table 7-24.

Return to the Summary Table.

Status flags for internal operations and other non critical conditions. Status register showing completion of BIST, whether active or sleep or active/shutdown.

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Table 7-24. VMON\_STAT Register Field Descriptions

	Table 1-24. Villon_OTAL Register Field Descriptions					
Bit	Field	Туре	Reset	Description		
7	FAILSAFE	R	Ob	Fail Safe state: 0 = Not in Fail Safe state 1 = In Fail Safe state		
6	ST_BIDT_C	R	0b	Built-In Self-Test state: 0 = BIST not complete 1 = BIST complete		
5	ST_VDD	R	Ob	Current state of VDD pin: 0 = VDD pin is low. 1 = VDD pin is high.		
4	ST_NIRQ	R	Ob	Current state of NIRQ input: 0 = NIRQ pin driven low by system. 1 = NIRQ pin driven high by system.		
3	ST_ACTSLP	R	xb	Current state of SLEEP input: 0 = SLEEP pin driven low by system. 1 = SLEEP pin driven high by system.		
2	ST_ACTSHDN	R	xb	Current state of ACT input:  0 = ACT pin driven low by system.  1 = ACT pin driven high by system.		
1	ST_SYNC	R	xb	Current state of SYNC pin:  0 = SYNC pin is low.  1 = SYNC pin is high.		
0	RESERVED	R	b	Reserved		

# 7.5.1.15 TEST\_INFO Register (Address = 0x31) [Reset = 0xX0]

TEST\_INFO is shown in Table 7-25.

Return to the Summary Table.

Internal Self-Test and ECC information.

Table 7-25. TEST\_INFO Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:6	RESERVED	R	b	Reserved
5	ECC_SEC	R	0b	Status of ECC single-error correction on OTP configuration load.  0 = no error correction applied  1 = single-error correction applied
4	ECC_DED	R	0b	Status of ECC double-error detection on OTP configuration load.  0 = no double-error detected  1 = double-error detected
3	BIST_VM	R	xb	Status of Volatile Memory test output from BIST.  0 = Volatile Memory test pass  1 = Volatile Memory test fail
2	BIST_NVM	R	xb	Status of Non-Volatile Memory test output from BIST.  0 = Non-Volatile Memory test pass  1 = Non-Volatile Memory test fail
1	BIST_L	R	xb	Status of Logic test output from BIST.  0 = Logic test pass  1 = Logic test fail
0	BIST_A	R	xb	Status of Analog test output from BIST.  0 = Analog test pass  1 = Analog test fail



### 7.5.1.16 OFF\_STAT Register (Address = 0x32) [Reset = 0xX0]

OFF\_STAT is shown in Table 7-26.

Return to the Summary Table.

Channel OFF status.

### Table 7-26. OFF\_STAT Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	VIN[N]	R		This register represents the OFF status of each channel: 0 = channel N is NOT OFF 1 = channel N is OFF (below OFF threshold)

### 7.5.1.17 SEQ\_REC\_STAT Register (Address = 0x34) [Reset = 0xX0]

SEQ\_REC\_STAT is shown in Table 7-27.

Return to the Summary Table.

Sequence recording status register.

### Table 7-27. SEQ\_REC\_STAT Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	REC_ACTIVE	R	Ob	Indicates the status of sequence logging (recording):  0 = No sequence recording active.  1 = ACT or SLEEP or SEQ_REC_CTL.REC_START initiated a power sequence and recording is active.
6:5	SEQ	R	Ob	Current sequence being recorded: 00b = Power ON (ACT 01) 01b = Power OFF (ACT 10) 10b = Sleep Exit (SLEEP 01) 11b = Sleep Entry (SLEEP 10)
4	TS_RDY	R	Ob	Timestamp data availability in SEQ_TIME_xSB registers: If EN_TS_OW=  0 this bit is cleared when TS_ACK is written to 1 by the host.  If EN_TS_OW= 1 this bit is cleared when all the SEQ_TIME_xSB[N] registers for the enabled channels (in VIN_CH_EN register) are read.  If the bit is set and REC_ACTIVE is also set, then the data in SEQ_TIME_xSB registers is being overwritten.  0 = No new data available or data already read.  1 = New data available (data still needs to be read).
3	SEQ_ON_RDY	R	xb	Power ON sequence data availability in SEQ_ON_LOG registers: If EN_SEQ_OW=  0 this bit is cleared when SEQ_ON_ACK is written to  1 by the host.  If EN_SEQ_OW=  1 this bit is cleared when all the SEQ_ON_LOG registers for the enabled channels (in VIN_CH_EN register) are read.  If the bit is set and REC_ACTIVE is set and SEQ[  1:  0]=  00b, then the data in SEQ_ON_LOG registers is being overwritten.  0 = No new data available or data already read.  1 = New data available (data still needs to be read).

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### Table 7-27. SEQ\_REC\_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description (Continued)
2	SEQ_OFF_RDY	R	xb	Power OFF sequence data availability in SEQ_OFF_LOG registers:  If EN_SEQ_OW=  0 this bit is cleared when SEQ_OFF_ACK is written to  1 by the host.  If EN_SEQ_OW=  1 this bit is cleared when all the SEQ_OFF_LOG registers for the enabled channels (in VIN_CH_EN register) are read.  If the bit is set and REC_ACTIVE is set and SEQ[  1:  0]=  01b, then the data in SEQ_OFF_LOG registers is being overwritten.  0 = No new data available or data already read.  1 = New data available (data still needs to be read).
1	SEQ_EXS_RDY	R	xb	Sleep Exit sequence data availability in SEQ_EXS_LOG registers: If EN_SEQ_OW=  0 this bit is cleared when SEQ_EXS_ACK is written to  1 by the host.  If EN_SEQ_OW=  1 this bit is cleared when all the SEQ_EXS_LOG registers for the enabled channels (in VIN_CH_EN register) are read.  If the bit is set and REC_ACTIVE is set and SEQ[  1:  0]=  10b, then the data in SEQ_EXS_LOG registers is being overwritten.  0 = No new data available or data already read.  1 = New data available (data still needs to be read).
0	SEQ_ENS_RDY	R	xb	Sleep Entry sequence data availability in SEQ_ENS_LOG registers:  If EN_SEQ_OW=  0 this bit is cleared when SEQ_ENS_ACK is written to  1 by the host.  If EN_SEQ_OW=  1 this bit is cleared when all the SEQ_ENS_LOG registers for the enabled channels (in VIN_CH_EN register) are read.  If the bit is set and REC_ACTIVE is set and SEQ[  1:  0]=  11b, then the data in SEQ_ENS_LOG registers is being overwritten.  0 = No new data available or data already read.  1 = New data available (data still needs to be read).

### 7.5.1.18 SEQ\_OW\_STAT Register (Address = 0x35) [Reset = 0xX0]

SEQ\_OW\_STAT is shown in Table 7-28.

Return to the Summary Table.

Sequence recording overwrite status register.

### Table 7-28. SEQ\_OW\_STAT Register Field Descriptions

	Bit	Field	Туре	Reset	Description
Ī	7:5	RSVD	R	0b	RSVD
	4	TS_OW	R	0b	Timestamp data overwritten status:  0 = No data was overwritten  1 = Data was overwritten (if VMON_MISC.EN_TS_OW=  1), or data can not be written (if VMON_MISC.EN_TS_OW=  0)
	3	SEQ_ON_OW	R	xb	Power ON sequence data overwritten status:  0 = No data was overwritten  1 = Data was overwritten (if VMON_MISC.EN_SEQ_OW=  1), or data can not be written (if VMON_MISC.EN_SEQ_OW=  0)



### Table 7-28. SEQ\_OW\_STAT Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
2	SEQ_OFF_OW	R	xb	Power OFF sequence data overwritten status:  0 = No data was overwritten  1 = Data was overwritten (if VMON_MISC.EN_SEQ_OW=  1), or data can not be written (if VMON_MISC.EN_SEQ_OW=  0)
1	SEQ_EXS_OW	R	xb	Sleep Exit sequence data overwritten status:  0 = No data was overwritten  1 = Data was overwritten (if VMON_MISC.EN_SEQ_OW=  1), or data can not be written (if VMON_MISC.EN_SEQ_OW=  0)
0	SEQ_ENS_OW	R	xb	Sleep Entry sequence data overwritten status:  0 = No data was overwritten  1 = Data was overwritten (if VMON_MISC.EN_SEQ_OW=  1), or data can not be written (if VMON_MISC.EN_SEQ_OW=  0)

#### 7.5.1.19 SEQ\_ORD\_STAT Register (Address = 0x36) [Reset = 0xX0]

SEQ\_ORD\_STAT is shown in Table 7-29.

Return to the Summary Table.

Sequencing/SYNC counter (rail order) register value.

## Table 7-29. SEQ\_ORD\_STAT Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	SYNC_COUNT[7:0]	R	xxxxb	This register represents the counter value during a power/sleep sequence.  It corresponds to the number of SYNC falling edges detected, and used as tag value for monitored channels.

### 7.5.1.20 MON\_LVL[1] Register (Address = 0x40) [Reset = 0xX0]

MON\_LVL[1] is shown in Table 7-30.

Return to the Summary Table.

For ADC readout -of each channel - 8bits

#### Table 7-30. MON\_LVL[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ADC[7:0]	R	xxxxb	This register represents the 8-bit voltage level of channel 1. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2V to 1.475V with 1LSB=5mV. With scaling set to 4x, the 8-bit value represents the range 0.8V to 5.9V with 1LSB=20mV.

### 7.5.1.21 MON\_LVL[2] Register (Address = 0x41) [Reset = 0xX0]

MON\_LVL[2] is shown in Table 7-31.

Return to the Summary Table.

For ADC readout -of each channel - 8bits

Table 7-31. MON\_LVL[2] Register Field Descriptions

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	Bit	Field	Туре	Reset	Description		
	7:0	ADC[7:0]	R	xxxxb	This register represents the 8-bit voltage level of channel 2. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling set to 1x, the 8-bit value represents the range 0.2V to 1.475V with 1LSB=5mV.  With scaling set to 4x, the 8-bit value represents the range 0.8V to 5.9V with 1LSB=20mV.		

### $7.5.1.22 \text{ MON\_LVL}[3] \text{ Register (Address = 0x42) [Reset = 0xX0]}$

MON\_LVL[3] is shown in Table 7-32.

Return to the Summary Table.

For ADC readout -of each channel - 8bits

#### Table 7-32. MON\_LVL[3] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ADC[7:0]	R	xxxxb	This register represents the 8-bit voltage level of channel 3. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling set to 1x, the 8-bit value represents the range 0.2V to 1.475V with 1LSB=5mV.  With scaling set to 4x, the 8-bit value represents the range 0.8V to 5.9V with 1LSB=20mV.
		-10		

# 7.5.1.23 MON\_LVL[4] Register (Address = 0x43) [Reset = 0xX0]

MON\_LVL[4] is shown in Table 7-33.

Return to the Summary Table.

For ADC readout -of each channel - 8bits

### Table 7-33. MON\_LVL[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ADC[7:0]	R	xxxxb	This register represents the 8-bit voltage level of channel 4. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2V to 1.475V with 1LSB=5mV. With scaling set to 4x, the 8-bit value represents the range 0.8V to 5.9V with 1LSB=20mV.

### $7.5.1.24 \text{ MON\_LVL}[5] \text{ Register (Address = 0x44) [Reset = 0xX0]}$

MON\_LVL[5] is shown in Table 7-34.

Return to the Summary Table.

For ADC readout -of each channel - 8bits



Table 7-34. MON\_LVL[5] Register Field Descriptions

_					
	Bit	Field	Туре	Reset	Description
	7:0	ADC[7:0]	R	xxxxb	This register represents the 8-bit voltage level of channel 5. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2V to 1.475V with 1LSB=5mV. With scaling set to 4x, the 8-bit value represents the range 0.8V to 5.9V with 1LSB=20mV.

### 7.5.1.25 MON\_LVL[6] Register (Address = 0x45) [Reset = 0xX0]

MON\_LVL[6] is shown in Table 7-35.

Return to the Summary Table.

For ADC readout -of each channel - 8bits

### Table 7-35. MON\_LVL[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ADC[7:0]	R	xxxxb	This register represents the 8-bit voltage level of channel 6. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2V to 1.475V with 1LSB=5mV. With scaling set to 4x, the 8-bit value represents the range 0.8V to 5.9V with 1LSB=20mV.

# 7.5.1.26 MON\_LVL[7] Register (Address = 0x46) [Reset = 0xX0]

MON\_LVL[7] is shown in Table 7-36.

Return to the Summary Table.

For ADC readout -of each channel - 8bits

### Table 7-36. MON\_LVL[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ADC[7:0]	R	xxxxb	This register represents the 8-bit voltage level of channel 5. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2V to 1.475V with 1LSB=5mV. With scaling set to 4x, the 8-bit value represents the range 0.8V to 5.9V with 1LSB=20mV.

# 7.5.1.27 MON\_LVL[8] Register (Address = 0x47) [Reset = 0xX0]

MON\_LVL[8] is shown in Table 7-37.

Return to the Summary Table.

For ADC readout -of each channel - 8bits

Table 7-37. MON\_LVL[8] Register Field Descriptions

				9.000. 1 1010. 2 000. 1 0110
Bit	Field	Туре	Reset	Description
7:0	ADC[7:0]	R	xxxxb	This register represents the 8-bit voltage level of channel 6. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling set to 1x, the 8-bit value represents the range 0.2V to 1.475V with 1LSB=5mV. With scaling set to 4x, the 8-bit value represents the range 0.8V to 5.9V with 1LSB=20mV.

### 7.5.1.28 SEQ\_ON\_LOG[1] Register (Address = 0x50) [Reset = 0xX0]

SEQ\_ON\_LOG[1] is shown in Table 7-38.

Return to the Summary Table.

Channel N Power ON sequence order value (ACT/ SLEEP 0 to 1).

#### Table 7-38. SEQ\_ON\_LOG[1] Register Field Descriptions

-					
	Bit	Field	Туре	Reset	Description
	7:0	ORDER[7:0]	R	xxxxb	This register stores the Power ON sequence order value for channel 1.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage rising level passes the UV_LF[N] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.29 SEQ\_ON\_LOG[2] Register (Address = 0x51) [Reset = 0xX0]

SEQ\_ON\_LOG[2] is shown in Table 7-39.

Return to the Summary Table.

Channel N Power ON sequence order value (ACT/ SLEEP 0 to 1).

#### Table 7-39. SEQ\_ON\_LOG[2] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power ON sequence order value for channel 2.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage rising level passes the UV_LF[N] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.30 SEQ\_ON\_LOG[3] Register (Address = 0x52) [Reset = 0xX0]

SEQ\_ON\_LOG[3] is shown in Table 7-40.

Return to the Summary Table.

Channel N Power ON sequence order value (ACT/ SLEEP 0 to 1).



#### Table 7-40. SEQ\_ON\_LOG[3] Register Field Descriptions

				1
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power ON sequence order value for channel 3.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage rising level passes the UV_LF[N] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.31 SEQ\_ON\_LOG[4] Register (Address = 0x53) [Reset = 0xX0]

SEQ\_ON\_LOG[4] is shown in Table 7-41.

Return to the Summary Table.

Channel N Power ON sequence order value (ACT/ SLEEP 0 to 1).

#### Table 7-41. SEQ ON LOG[4] Register Field Descriptions

		· · · · · · - · - ·		1
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power ON sequence order value for channel 4.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage rising level passes the UV_LF[N] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.32 SEQ\_ON\_LOG[5] Register (Address = 0x54) [Reset = 0xX0]

SEQ\_ON\_LOG[5] is shown in Table 7-42.

Return to the Summary Table.

Channel N Power ON sequence order value (ACT/ SLEEP 0 to 1).

#### Table 7-42, SEQ ON LOGI51 Register Field Descriptions

	10.010		<u>-</u>	1.109.010. 1.10.0 2.000p.1.01.0
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power ON sequence order value for channel 5.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage rising level passes the UV_LF[N] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.33 SEQ\_ON\_LOG[6] Register (Address = 0x55) [Reset = 0xX0]

SEQ\_ON\_LOG[6] is shown in Table 7-43.

Return to the Summary Table.

Channel N Power ON sequence order value (ACT/ SLEEP 0 to 1).

Table 7-43. SEQ\_ON\_LOG[6] Register Field Descriptions

	i doio i	-0. O= Q_\	0.100[0	1 register i leia Bescriptions
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power ON sequence order value for channel 6.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage rising level passes the UV_LF[N] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.34 SEQ\_ON\_LOG[7] Register (Address = 0x56) [Reset = 0xX0]

SEQ\_ON\_LOG[7] is shown in Table 7-44.

Return to the Summary Table.

Channel N Power ON sequence order value (ACT/ SLEEP 0 to 1).

### Table 7-44. SEQ\_ON\_LOG[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R		This register stores the Power ON sequence order value for channel 7. The sequence order value is the tag assigned to the channel during the sequence triggered by ACT. The tag is assigned when the voltage rising level passes the UV_LF[N] threshold. The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.35 SEQ\_ON\_LOG[8] Register (Address = 0x57) [Reset = 0xX0]

SEQ\_ON\_LOG[8] is shown in Table 7-45.

Return to the Summary Table.

Channel N Power ON sequence order value (ACT/ SLEEP 0 to 1).

# Table 7-45. SEQ\_ON\_LOG[8] Register Field Descriptions

	10.010		- · · • • [• .	i regiotor i iola zocomplicilo
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power ON sequence order value for channel 8.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage rising level passes the UV_LF[N] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.36 SEQ\_OFF\_LOG[1] Register (Address = 0x60) [Reset = 0xX0]

SEQ\_OFF\_LOG[1] is shown in Table 7-46.

Return to the Summary Table.

Channel N Power OFF sequence order value (ACT 1 to 0).



#### Table 7-46. SEQ\_OFF\_LOG[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power OFF sequence order value for channel 1.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.37 SEQ\_OFF\_LOG[2] Register (Address = 0x61) [Reset = 0xX0]

SEQ\_OFF\_LOG[2] is shown in Table 7-47.

Return to the Summary Table.

Channel N Power OFF sequence order value (ACT 1 to 0).

### Table 7-47. SEQ\_OFF\_LOG[2] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power OFF sequence order value for channel 2.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.38 SEQ\_OFF\_LOG[3] Register (Address = 0x62) [Reset = 0xX0]

SEQ\_OFF\_LOG[3] is shown in Table 7-48.

Return to the Summary Table.

Channel N Power OFF sequence order value (ACT 1 to 0).

#### Table 7-48, SEQ\_OFF\_LOG[3] Register Field Descriptions

			<u>_</u>	1 9.0.0
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power OFF sequence order value for channel 3.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.39 SEQ\_OFF\_LOG[4] Register (Address = 0x63) [Reset = 0xX0]

SEQ\_OFF\_LOG[4] is shown in Table 7-49.

Return to the Summary Table.

Channel N Power OFF sequence order value (ACT 1 to 0).

Table 7-49. SEQ\_OFF\_LOG[4] Register Field Descriptions

				1 regioter i ioia 2 cooribació
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power OFF sequence order value for channel 4.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.40 SEQ\_OFF\_LOG[5] Register (Address = 0x64) [Reset = 0xX0]

SEQ\_OFF\_LOG[5] is shown in Table 7-50.

Return to the Summary Table.

Channel N Power OFF sequence order value (ACT 1 to 0).

### Table 7-50. SEQ\_OFF\_LOG[5] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power OFF sequence order value for channel 5.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.41 SEQ\_OFF\_LOG[6] Register (Address = 0x65) [Reset = 0xX0]

SEQ\_OFF\_LOG[6] is shown in Table 7-51.

Return to the Summary Table.

Channel N Power OFF sequence order value (ACT 1 to 0).

### Table 7-51. SEQ\_OFF\_LOG[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power OFF sequence order value for channel 6.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.42 SEQ\_OFF\_LOG[7] Register (Address = 0x66) [Reset = 0xX0]

SEQ\_OFF\_LOG[7] is shown in Table 7-52.

Return to the Summary Table.

Channel N Power OFF sequence order value (ACT 1 to 0).



#### Table 7-52. SEQ\_OFF\_LOG[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power OFF sequence order value for channel 7.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.43 SEQ\_OFF\_LOG[8] Register (Address = 0x67) [Reset = 0xX0]

SEQ\_OFF\_LOG[8] is shown in Table 7-53.

Return to the Summary Table.

Channel N Power OFF sequence order value (ACT 1 to 0).

### Table 7-53. SEQ\_OFF\_LOG[8] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Power OFF sequence order value for channel 8.  The sequence order value is the tag assigned to the channel during the sequence triggered by ACT.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.44 SEQ\_EXS\_LOG[1] Register (Address = 0x70) [Reset = 0xX0]

SEQ\_EXS\_LOG[1] is shown in Table 7-54.

Return to the Summary Table.

Channel N Sleep Exit sequence order value (SLEEP 0 to 1).

### Table 7-54. SEQ\_EXS\_LOG[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Exit sequence order value for channel 1.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage rising level passes the UV_LF[1] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.45 SEQ\_EXS\_LOG[2] Register (Address = 0x71) [Reset = 0xX0]

SEQ\_EXS\_LOG[2] is shown in Table 7-55.

Return to the Summary Table.

Channel N Sleep Exit sequence order value (SLEEP 0 to 1).

Table 7-55. SEQ\_EXS\_LOG[2] Register Field Descriptions

	Tubic 1	OO. OL Q_L		1 register i leia Descriptions
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Exit sequence order value for channel 2.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage rising level passes the UV_LF[2] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.46 SEQ\_EXS\_LOG[3] Register (Address = 0x72) [Reset = 0xX0]

SEQ\_EXS\_LOG[3] is shown in Table 7-56.

Return to the Summary Table.

Channel N Sleep Exit sequence order value (SLEEP 0 to 1).

### Table 7-56. SEQ\_EXS\_LOG[3] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Exit sequence order value for channel 3.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage rising level passes the UV_LF[3] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.47 SEQ\_EXS\_LOG[4] Register (Address = 0x73) [Reset = 0xX0]

SEQ\_EXS\_LOG[4] is shown in Table 7-57.

Return to the Summary Table.

Channel N Sleep Exit sequence order value (SLEEP 0 to 1).

### Table 7-57. SEQ\_EXS\_LOG[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Exit sequence order value for channel 4.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage rising level passes the UV_LF[4] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.48 SEQ\_EXS\_LOG[5] Register (Address = 0x74) [Reset = 0xX0]

SEQ\_EXS\_LOG[5] is shown in Table 7-58.

Return to the Summary Table.

Channel N Sleep Exit sequence order value (SLEEP 0 to 1).



Table 7-58. SEQ\_EXS\_LOG[5] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Exit sequence order value for channel 5.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage rising level passes the UV_LF[5] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.49 SEQ\_EXS\_LOG[6] Register (Address = 0x75) [Reset = 0xX0]

SEQ\_EXS\_LOG[6] is shown in Table 7-59.

Return to the Summary Table.

Channel N Sleep Exit sequence order value (SLEEP 0 to 1).

### Table 7-59. SEQ\_EXS\_LOG[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Exit sequence order value for channel 6.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage rising level passes the UV_LF[6] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.50 SEQ\_EXS\_LOG[7] Register (Address = 0x76) [Reset = 0xX0]

SEQ\_EXS\_LOG[7] is shown in Table 7-60.

Return to the Summary Table.

Channel N Sleep Exit sequence order value (SLEEP 0 to 1).

### Table 7-60. SEQ\_EXS\_LOG[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Exit sequence order value for channel 7.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage rising level passes the UV_LF[5] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.51 SEQ\_EXS\_LOG[8] Register (Address = 0x77) [Reset = 0xX0]

SEQ\_EXS\_LOG[8] is shown in Table 7-61.

Return to the Summary Table.

Channel N Sleep Exit sequence order value (SLEEP 0 to 1).

Table 7-61. SEQ\_EXS\_LOG[8] Register Field Descriptions

	Tubic 1	UI. OLQ_L		1 register ricia Descriptions
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Exit sequence order value for channel 8.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage rising level passes the UV_LF[6] threshold.  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.52 SEQ\_ENS\_LOG[1] Register (Address = 0x80) [Reset = 0xX0]

SEQ\_ENS\_LOG[1] is shown in Table 7-62.

Return to the Summary Table.

Channel N Sleep Entry sequence order value (SLEEP 1 to 0).

### Table 7-62. SEQ\_ENS\_LOG[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Entry sequence order value for channel 1.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.53 SEQ\_ENS\_LOG[2] Register (Address = 0x81) [Reset = 0xX0]

SEQ\_ENS\_LOG[2] is shown in Table 7-63.

Return to the Summary Table.

Channel N Sleep Entry sequence order value (SLEEP 1 to 0).

### Table 7-63. SEQ\_ENS\_LOG[2] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R		This register stores the Sleep Entry sequence order value for channel 2.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.54 SEQ\_ENS\_LOG[3] Register (Address = 0x82) [Reset = 0xX0]

SEQ\_ENS\_LOG[3] is shown in Table 7-64.

Return to the Summary Table.

Channel N Sleep Entry sequence order value (SLEEP 1 to 0).



#### Table 7-64. SEQ\_ENS\_LOG[3] Register Field Descriptions

				1 9
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Entry sequence order value for channel 3.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.55 SEQ\_ENS\_LOG[4] Register (Address = 0x83) [Reset = 0xX0]

SEQ\_ENS\_LOG[4] is shown in Table 7-65.

Return to the Summary Table.

Channel N Sleep Entry sequence order value (SLEEP 1 to 0).

### Table 7-65. SEQ\_ENS\_LOG[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Entry sequence order value for channel 4.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.56 SEQ\_ENS\_LOG[5] Register (Address = 0x84) [Reset = 0xX0]

SEQ\_ENS\_LOG[5] is shown in Table 7-66.

Return to the Summary Table.

Channel N Sleep Entry sequence order value (SLEEP 1 to 0).

### Table 7-66. SEQ\_ENS\_LOG[5] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R		This register stores the Sleep Entry sequence order value for channel 5.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.57 SEQ\_ENS\_LOG[6] Register (Address = 0x85) [Reset = 0xX0]

SEQ\_ENS\_LOG[6] is shown in Table 7-67.

Return to the Summary Table.

Channel N Sleep Entry sequence order value (SLEEP 1 to 0).

Table 7-67. SEQ\_ENS\_LOG[6] Register Field Descriptions

143.0 : 0:: 0=4_=:10_=00[				1 9
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Entry sequence order value for channel 6.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.58 SEQ\_ENS\_LOG[7] Register (Address = 0x86) [Reset = 0xX0]

SEQ\_ENS\_LOG[7] is shown in Table 7-68.

Return to the Summary Table.

Channel N Sleep Entry sequence order value (SLEEP 1 to 0).

### Table 7-68. SEQ\_ENS\_LOG[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R	xxxxb	This register stores the Sleep Entry sequence order value for channel 7.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.59 SEQ\_ENS\_LOG[8] Register (Address = 0x87) [Reset = 0xX0]

SEQ\_ENS\_LOG[8] is shown in Table 7-69.

Return to the Summary Table.

Channel N Sleep Entry sequence order value (SLEEP 1 to 0).

### Table 7-69. SEQ\_ENS\_LOG[8] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R		This register stores the Sleep Entry sequence order value for channel 8.  The sequence order value is the tag assigned to the channel during the sequence triggered by SLEEP.  The tag is assigned when the voltage falling level passes the OFF threshold (200mV).  The tag value is the SYNC_ORD_COUNT at the time the threshold is passed.

### 7.5.1.60 SEQ\_TIME\_MSB[1] Register (Address = 0x90) [Reset = 0xX0]

SEQ\_TIME\_MSB[1] is shown in Table 7-70.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).



### Table 7-70. SEQ\_TIME\_MSB[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the MSB of the sequence timestamp for channel 1.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[1] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

### 7.5.1.61 SEQ\_TIME\_LSB[1] Register (Address = 0x91) [Reset = 0xX0]

SEQ\_TIME\_LSB[1] is shown in Table 7-71.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-71. SEQ\_TIME\_LSB[1] Register Field Descriptions

_			· · · · • = • <u>-</u> ·		1 Regioter Flora Becomptions
	Bit	Field	Туре	Reset	Description
	7:0	CLOCK[7:0]	R	xxxxb	This register stores the LSB of the sequence timestamp for channel 1.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[1] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

#### 7.5.1.62 SEQ\_TIME\_MSB[2] Register (Address = 0x92) [Reset = 0xX0]

SEQ\_TIME\_MSB[2] is shown in Table 7-72.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

#### Table 7-72. SEQ\_TIME\_MSB[2] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the MSB of the sequence timestamp for channel 2.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[2] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

### 7.5.1.63 SEQ\_TIME\_LSB[2] Register (Address = 0x93) [Reset = 0xX0]

SEQ\_TIME\_LSB[2] is shown in Table 7-73.



Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

#### Table 7-73. SEQ\_TIME\_LSB[2] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the LSB of the sequence timestamp for channel 2.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[2] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

### 7.5.1.64 SEQ\_TIME\_MSB[3] Register (Address = 0x94) [Reset = 0xX0]

SEQ TIME MSB[3] is shown in Table 7-74.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-74. SEQ TIME MSB[3] Register Field Descriptions

Table 1-14. OE & Time Mobile I Register Field Descriptions							
	Bit	Field	Туре	Reset	Description		
	7:0	CLOCK[7:0]	R	xxxxb	This register stores the MSB of the sequence timestamp for channel 3.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[3] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).		

### 7.5.1.65 SEQ\_TIME\_LSB[3] Register (Address = 0x95) [Reset = 0xX0]

SEQ TIME LSB[3] is shown in Table 7-75.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-75. SEQ\_TIME\_LSB[3] Register Field Descriptions

E	3it	Field	Туре	Reset	Description
7	7:0	CLOCK[7:0]	R	xxxxb	This register stores the LSB of the sequence timestamp for channel 3.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[3] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

### 7.5.1.66 SEQ\_TIME\_MSB[4] Register (Address = 0x96) [Reset = 0xX0]

SEQ\_TIME\_MSB[4] is shown in Table 7-76.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

#### Table 7-76. SEQ\_TIME\_MSB[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the MSB of the sequence timestamp for channel 4.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[4] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

#### 7.5.1.67 SEQ\_TIME\_LSB[4] Register (Address = 0x97) [Reset = 0xX0]

SEQ\_TIME\_LSB[4] is shown in Table 7-77.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

#### Table 7-77. SEQ\_TIME\_LSB[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the LSB of the sequence timestamp for channel 4.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[4] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power 200mVd Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

#### 7.5.1.68 SEQ\_TIME\_MSB[5] Register (Address = 0x98) [Reset = 0xX0]

SEQ\_TIME\_MSB[5] is shown in Table 7-78.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-78. SEQ\_TIME\_MSB[5] Register Field Descriptions

				2] . tog.otoo.a 2000paoo
Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the MSB of the sequence timestamp for channel 5.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[5] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

### 7.5.1.69 SEQ\_TIME\_LSB[5] Register (Address = 0x99) [Reset = 0xX0]

SEQ\_TIME\_LSB[5] is shown in Table 7-79.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-79. SEQ\_TIME\_LSB[5] Register Field Descriptions

	Tubic 1	<i>,</i> o. o. u		of Itegister Freid Descriptions
Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the LSB of the sequence timestamp for channel 5.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[5] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

### 7.5.1.70 SEQ\_TIME\_MSB[6] Register (Address = 0x9A) [Reset = 0xX0]

SEQ\_TIME\_MSB[6] is shown in Table 7-80.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

### Table 7-80. SEQ\_TIME\_MSB[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the MSB of the sequence timestamp for channel 6.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[6] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

### 7.5.1.71 SEQ\_TIME\_LSB[6] Register (Address = 0x9B) [Reset = 0xX0]

SEQ\_TIME\_LSB[6] is shown in Table 7-81.



Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-81. SEQ\_TIME\_LSB[6] Register Field Descriptions

E	Bit	Field	Туре	Reset	Description
7	7:0	CLOCK[7:0]	R	xxxxb	This register stores the LSB of the sequence timestamp for channel 6.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[6] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

### 7.5.1.72 SEQ\_TIME\_MSB[7] Register (Address = 0x9C) [Reset = 0xX0]

SEQ TIME MSB[7] is shown in Table 7-82.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-82. SEQ\_TIME\_MSB[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the MSB of the sequence timestamp for channel 7.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[7] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

## 7.5.1.73 SEQ\_TIME\_LSB[7] Register (Address = 0x9D) [Reset = 0xX0]

SEQ TIME LSB[7] is shown in Table 7-83.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

Table 7-83. SEQ\_TIME\_LSB[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the LSB of the sequence timestamp for channel 7.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[7] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

### 7.5.1.74 SEQ\_TIME\_MSB[8] Register (Address = 0x9E) [Reset = 0xX0]

SEQ\_TIME\_MSB[8] is shown in Table 7-84.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

#### Table 7-84. SEQ TIME MSB[8] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the MSB of the sequence timestamp for channel 8.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[8] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

#### 7.5.1.75 SEQ\_TIME\_LSB[8] Register (Address = 0x9F) [Reset = 0xX0]

SEQ\_TIME\_LSB[8] is shown in Table 7-85.

Return to the Summary Table.

Channel N Sequence timestamp value MSB and LSB (all sequences).

#### Table 7-85. SEQ TIME LSB[8] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	CLOCK[7:0]	R	xxxxb	This register stores the LSB of the sequence timestamp for channel 8.  The sequence timer value is the time assigned to the channel during the sequence triggered by ACT or SLEEP.  The timestamp is stored when the voltage rising level passes the UV_LF[8] threshold for Power ON and Sleep Exit sequences (ACT 01 or SLEEP 01).  The timestamp is stored when the voltage falling level passes the OFF threshold (200mV) for Power OFF and Sleep Entry sequences (ACT 10 or SLEEP 10).  The least significant bit corresponds to 50µs (equal to tSEQ_LSB).

#### 7.5.1.76 BANK\_SEL Register (Address = 0xF0) [Reset = 0x00]

BANK\_SEL is shown in Table 7-86.

Return to the Summary Table.

Bank select=0 for Bank 0 and 1 for Bank 1

# Table 7-86. BANK\_SEL Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:1	RESERVED	R	b	Reserved
0	BANK SELECTION	R/W	b	Register Bank selection number.

### 7.5.1.77 PROT1 Register (Address = 0xF1) [Reset = 0x00]

PROT1 is shown in Table 7-87.

Return to the Summary Table.

Protection selection registers. To write-protect a register group, the host must set the relevant bit in both registers. For security, registers PROT1 and PROT2 need to have POR value = 0x00 and become read-only once set until power cycle. Once set to 1, the bit cannot be cleared to 0 by the host. They can be cleared (and allow writing different VMON registers configurations) through: A power cycle A reset through VMON\_CTL.RESET BIST executed on exiting Sequence 2 (if TEST\_CFG.AT\_SHDN=1).

Table 7-87. PROT1 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:6	RESERVED	R	b	Reserved
5	WRKC	R/W	b	0b 0 = Control Working (WRKC) registers are writeable. 0b 1 = Writes to control working registers are ignored.
4	WRKS	R/W	b	0b 0 = Sequence Working (WRKS) registers are writeable. 0b 1 = Writes to sequence working registers are ignored.
3	CFG	R/W	b	0b 0 = Configuration (CFG) registers are writeable. 0b 1 = Writes to configuration registers are ignored.
2	IEN	R/W	b	0b 0 = Interrupt Enable (IEN) registers are writeable. 0b 1 = Writes to interrupt enable registers are ignored.
1	MON	R/W	b	0b 0 = Monitor (MON[N]) registers are writeable. 0b 1 = Writes to monitor registers selected in PROT_MON 1 register are ignored.
0	SEQ	R/W	b	0b 0 = Sequence (SEQ) Registers are writeable. 0b 1 = Writes to sequence registers are ignored.

#### 7.5.1.78 PROT2 Register (Address = 0xF2) [Reset = 0x00]

PROT2 is shown in Table 7-88.

Return to the Summary Table.

Protection selection registers. To write-protect a register group, the host must set the relevant bit in both registers. For security, registers PROT1 and PROT2 need to have POR value = 0x00 and become read-only once set until power cycle. Once set to 1, the bit cannot be cleared to 0 by the host. They can be cleared (and allow writing different VMON registers configurations) through: A power cycle A reset through VMON\_CTL.RESET BIST executed on exiting Sequence 2 (if TEST\_CFG.AT\_SHDN=1).

Table 7-88. PROT2 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:6	RESERVED	R	b	Reserved
5	WRKC	R/W	b	0b 0 = Control Working (WRKC) registers are writeable. 0b 1 = Writes to control working registers are ignored.

Table 7-88. PROT2 Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
4	WRKS	R/W	b	0b 0 = Sequence Working (WRKS) registers are writeable. 0b 1 = Writes to sequence working registers are ignored.
3	CFG	R/W	b	0b 0 = Configuration (CFG) registers are writeable. 0b 1 = Writes to configuration registers are ignored.
2	IEN	R/W	b	0b 0 = Interrupt Enable (IEN) registers are writeable. 0b 1 = Writes to interrupt enable registers are ignored.
1	MON	R/W	b	0b 0 = Monitor (MON[N]) registers are writeable. 0b 1 = Writes to monitor registers selected in PROT_MON 1 register are ignored.
0	SEQ	R/W	b	0b 0 = Sequence (SEQ) Registers are writeable. 0b 1 = Writes to sequence registers are ignored.

# 7.5.1.79 PROT\_MON2 Register (Address = 0xF3) [Reset = 0xC1]

PROT MON2 is shown in Table 7-89.

Return to the Summary Table.

Monitor channels configuration protection.

Table 7-89. PROT\_MON2 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:6	RESERVED	R	b	Reserved
5:0	MON[N]	R/W	1b	This register selects the monitor channels configurations that will be protected once PROT  1, PROT  2 registers are written to protect the MON group.  0 = Monitor configuration registers for channel N are writeable.  1 = Writes to monitor configuration registers for channel N are ignored.

# 7.5.1.80 I2CADDR Register (Address = 0xF9) [Reset = 0xX0]

I2CADDR is shown in Table 7-90.

Return to the Summary Table.

3 LSB bits are decided based on resistor value and 5 MSB bits are based on OTP NVM. ADDR\_NVM has default value of 30 (Factory default setting)

Table 7-90. I2CADDR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	RESERVED	R	b	Reserved
6:3	ADDR_NVM[3:0]	R	xb	I2C address four most significant bits. Set in NVM.
2:0	ADDR_STRAP[2:0]	R	xxxb	I2C address three least significant bits. Set by the strap level detected on ADDR pin, from 000b to 111b.



# 7.5.1.81 DEV\_CFG Register (Address = 0xFA) [Reset = 0xX0]

DEV\_CFG is shown in Table 7-91.

Return to the Summary Table.

Status of I2C interface voltage levels, 0 for 3.3V I/F and 1 for 1.2/1.8V interface (Factory default setting)

# Table 7-91. DEV\_CFG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:1	RESERVED	R	b	Reserved
0	SOC_IF	R	xb	Host SoC Interface (includes I 2C, ACT, SLEEP, and SYNC).  0 = 3. 3V 1 = 1. 2V/ 1. 8V



# 7.5.2 BANK1 Registers

Table 7-92 lists the memory-mapped registers for the BANK1 registers. All register offset addresses not listed in Table 7-92 should be considered as reserved locations and the register contents should not be modified.

Table 7-92. BANK1 Registers

	Table 7-92. BANK1 Registers								
Addres s	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	VMON_CTL	DIAG_EN	I_SCALE	SLP_PWR	RESERVED	RESET_PR OT	SYNC_RST	FORCE_SY NC	FORCE_NI RQ
0x11	VMON_MISC		RESE	RVED		EN_TS_OW	EN_SEQ_O W	REQ_PEC	EN_PEC
0x12	TEST_CFG		RESE	RVED		AT_SHDN	RESERVED	AT_	POR
0x13	IEN_UVHF				MO	N[N]			
0x14	IEN_UVLF				MO	N[N]			
0x15	IEN_OVHF				MO	N[N]			
0x16	IEN_OVLF				MO	N[N]			
0x17	IEN_SEQ_ON	RESE	RVED			MO	N[N]		
0x18	IEN_SEQ_OFF	RESE	RVED			MO	N[N]		
0x19	IEN_SEQ_EXS	RESE	RVED			MO	N[N]		
0x1A	IEN_SEQ_ENS	RESE	RVED			MO	N[N]		
0x1B	IEN_CONTROL		RESERVED		RT_CRC Int	RESERVED	TSD Int	SYNC Int	PEC Int
0x1C	IEN_TEST		RESE	RVED		ECC_SEC	RESERVED	BIST_Compl ete_INT	BIST_Fail_I NT
0x1D	IEN_VENDOR				RESERVED				RESERVED
0x1E	MON_CH_EN				MO	N[N]			
0x1F	VRANGE_MULT				MO	N[N]			
0x20	UV_HF[1]				THRESH	IOLD[7:0]			
0x21	OV_HF[1]				THRESH	IOLD[7:0]			
0x22	UV_LF[1]				THRESH	IOLD[7:0]			
0x23	OV_LF[1]				THRESH	IOLD[7:0]			
0x24	FLT_HF[1]		OV_DI	EB[3:0]			UV_DI	EB[3:0]	
0x25	FC_LF[1]		RESERVED		UV_HF_1	1 to NRST THRESHOLD[2:0]			
0x30	UV_HF[2]				THRESH	IOLD[7:0]			
0x31	OV_HF[2]				THRESH	IOLD[7:0]			
0x32	UV_LF[2]				THRESH	IOLD[7:0]			
0x33	OV_LF[2]				THRESH	IOLD[7:0]			
0x34	FLT_HF[2]		OV_DI	EB[3:0]			UV_DI	EB[3:0]	
0x35	FC_LF[2]		RESERVED		UV_HF_2	2 to NRST	TH	HRESHOLD[2	:0]
0x40	UV_HF[3]				THRESH	IOLD[7:0]			
0x41	OV_HF[3]				THRESH	IOLD[7:0]			
0x42	UV_LF[3]		THRESHOLD[7:0]						
0x43	OV_LF[3]	THRESHOLD[7:0]							
0x44	FLT_HF[3]	OV_DEB[3:0] UV_DEB[3:0]							
0x45	FC_LF[3]		RESERVED		UV_HF_3	3 to NRST	TH	HRESHOLD[2	:0]
0x50	UV_HF[4]				THRESH	IOLD[7:0]			
0x51	OV_HF[4]				THRESH	IOLD[7:0]			
0x52	UV_LF[4]				THRESH	IOLD[7:0]			
0x53	OV_LF[4]				THRESH	IOLD[7:0]			
0x54	FLT_HF[4]		OV_DI	EB[3:0]			UV_DI	EB[3:0]	



Table 7-92. BANK1 Registers (continued)

			Table 1-32	. DANKI F	kegisters (d	,onunueu)				
Addres s	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x55	FC_LF[4]		RESERVED		UV_HF_4	to NRST	TI	HRESHOLD[2	:0]	
0x60	UV_HF[5]		THRESHOLD[7:0]							
0x61	OV_HF[5]		THRESHOLD[7:0]							
0x62	UV_LF[5]	THRESHOLD[7:0]								
0x63	OV_LF[5]				THRESH	IOLD[7:0]				
0x64	FLT_HF[5]		OV_DI	EB[3:0]			UV_DI	EB[3:0]		
0x65	FC_LF[5]		RESERVED		UV_HF_	to NRST	TI	HRESHOLD[2	:0]	
0x70	UV_HF[6]				THRESH	IOLD[7:0]				
0x71	OV_HF[6]				THRESH	IOLD[7:0]				
0x72	UV_LF[6]				THRESH	IOLD[7:0]				
0x73	OV_LF[6]				THRESH	IOLD[7:0]				
0x74	FLT_HF[6]		OV_DI	EB[3:0]			UV_D	EB[3:0]		
0x75	FC_LF[6]		RESERVED		UV_HF_6	6 to NRST	TI	HRESHOLD[2	:0]	
0x80	UV_HF[7]				THRESH	IOLD[7:0]				
0x81	OV_HF[7]				THRESH	IOLD[7:0]				
0x82	UV_LF[7]				THRESH	IOLD[7:0]				
0x83	OV_LF[7]				THRESH	IOLD[7:0]				
0x84	FLT_HF[7]		OV_DI	EB[3:0]			UV_D	EB[3:0]		
0x85	FC_LF[7]			RESERVED			TI	HRESHOLD[2	:0]	
0x90	UV_HF[8]				THRESH	IOLD[7:0]				
0x91	OV_HF[8]				THRESH	IOLD[7:0]				
0x92	UV_LF[8]				THRESH	IOLD[7:0]				
0x93	OV_LF[8]				THRESH	IOLD[7:0]				
0x94	FLT_HF8]		OV_DI	EB[3:0]			UV_D	EB[3:0]		
0x95	FC_LF[8]			RESERVED			TI	HRESHOLD[2	:0]	
0x9F	TI_CONTROL	ENTER_BIS T	RSVD	Manual Reset	RESE	RVED	F	Reset delay tin	ne	
0xA0	SEQ_REC_CTL	REC_STAR T	SEQ	[1:0]	TS_ACK	SEQ_ON_A CK	SEQ_OFF_ ACK	SEQ_EXS_ ACK	SEQ_ENS_ ACK	
0xA1	AMSK_ON				MO	N[N]				
0xA2	AMSK_OFF				MO	N[N]				
0xA3	AMSK_EXS				MO	N[N]				
0xA4	AMSK_ENS				MO	N[N]				
0xA5	SEQ_TOUT_MS B				MILLIS	EC[7:0]				
0xA6	SEQ_TOUT_LS B				MILLIS	EC[7:0]				
0xA7	SEQ_SYNC	PULSE_WIDTH[7:0]								
0xA8	SEQ_UP_THLD		MON[N]							
0xA9	SEQ_DN_THLD				МО	N[N]				
0xB0	SEQ_ON_EXP[1				ORDE	ER[7:0]				
0xB1	SEQ_ON_EXP[2 ]				ORDE	ER[7:0]				
0xB2	SEQ_ON_EXP[3				ORDE	ER[7:0]				
L	1	L.								



Table 7-92. BANK1 Registers (continued)

			Table 7-94	L BANKT R	Registers (d	continuea)			
Addres s	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xB3	SEQ_ON_EXP[4				ORDE	R[7:0]			
0xB4	SEQ_ON_EXP[5				ORDE	R[7:0]			
0xB5	SEQ_ON_EXP[6				ORDE	R[7:0]			
0xB6	SEQ_ON_EXP[7				ORDE	ER[7:0]			
0xB7	SEQ_ON_EXP[8				ORDE	ER[7:0]			
0xC0	SEQ_OFF_EXP[ 1]				ORDE	ER[7:0]			
0xC1	SEQ_OFF_EXP[				ORDE	ER[7:0]			
0xC2	SEQ_OFF_EXP[				ORDE	ER[7:0]			
0xC3	SEQ_OFF_EXP[ 4]				ORDE	R[7:0]			
0xC4	SEQ_OFF_EXP[ 5]				ORDE	ER[7:0]			
0xC5	SEQ_OFF_EXP[ 6]				ORDE	ER[7:0]			
0xC6	SEQ_OFF_EXP[				ORDE	ER[7:0]			
0xC7	SEQ_OFF_EXP[ 8]				ORDE	ER[7:0]			
0xD0	SEQ_EXS_EXP[ 1]				ORDE	R[7:0]			
0xD1	SEQ_EXS_EXP[ 2]				ORDE	R[7:0]			
0xD2	SEQ_EXS_EXP[				ORDE	ER[7:0]			
0xD3	SEQ_EXS_EXP[ 4]				ORDE	R[7:0]			
0xD4	SEQ_EXS_EXP[ 5]				ORDE	ER[7:0]			
0xD5	SEQ_EXS_EXP[ 6]				ORDE	ER[7:0]			
0xD6	SEQ_EXS_EXP[ 7]				ORDE	ER[7:0]			
0xD7	SEQ_EXS_EXP[ 8]				ORDE	ER[7:0]			
0xE0	SEQ_ENS_EXP[ 1]				ORDE	ER[7:0]			
0xE1	SEQ_ENS_EXP[ 2]				ORDE	ER[7:0]			
0xE2	SEQ_ENS_EXP[ 3]				ORDE	ER[7:0]			
0xE3	SEQ_ENS_EXP[ 4]				ORDE	ER[7:0]			
0xE4	SEQ_ENS_EXP[ 5]				ORDE	ER[7:0]			
	-								



Table 7-92. BANK1 Registers (continued)

					- 3 1 -	,			
Addres s	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xE5	SEQ_ENS_EXP[ 6]		ORDER[7:0]						
0xE6	SEQ_ENS_EXP[ 7]		ORDER[7:0]						
0xE7	SEQ_ENS_EXP[ 8]				ORDE	R[7:0]			

Complex bit access types are encoded to fit into small table cells. Table 7-93 shows the codes that are used for access types in this section.

Table 7-93. BANK1 Access Type Codes

Access Type	Code	Description						
Read Type								
R	R	Read						
Write Type	Write Type							
W	W	Write						
Reset or Default	Reset or Default Value							
-n		Value after reset or the default value						

# 7.5.2.1 VMON\_CTL Register (Address = 0x10) [Reset = 0xX0]

VMON\_CTL is shown in Table 7-94.

Return to the Summary Table.

Voltage Monitor device control register.

Table 7-94. VMON\_CTL Register Field Descriptions

D:4				Description
Bit	Field	Туре	Reset	Description
7:6	DIAG_EN_SCALE	R/W	b	Diag EN Scale 00 = No force on GAINSEL of SVS COMPs 01 = Forced to 1x 10 = Forced to 2x 11 = Forced to 4x
5	SLP_PWR	R/W	b	Sleep Power Bit 0 = Sleep low power mode 1 = Sleep high power mode
4	RESERVED	R	b	Reserved
3	RESET_PROT	R/W	b	Reset 0 = Always reads 0 1 = Full device Reset
2	SYNC_RST	R/W	b	SYNC counter reset (SEQ_ORD_STAT.SYNC_COUNT).  0 = Always reads  0  1 = Reset SYNC counter
1	FORCE_SYNC	R/W	b	Force SYNC assertion  0 = SYNC pin is de-asserted and controlled by the sequence monitoring logic.  1 = SYNC pin is asserted (forced low)

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Table 7-94. VMON\_CTL Register Field Descriptions (continued)

E	Bit	Field	Туре	Reset	Description
	0	FORCE_NIRQ	R/W	b	Force NIRQ assertion 0 = NIRQ pin is de-asserted and controlled by interrupt registers faults 1 = NIRQ pin is asserted (forced low)

# 7.5.2.2 VMON\_MISC Register (Address = 0x11) [Reset = 0x0C]

VMON\_MISC is shown in Table 7-95.

Return to the Summary Table.

Miscellaneous voltage monitoring configurations.

#### Table 7-95. VMON MISC Register Field Descriptions

			_	Register Field Descriptions
Bit	Field	Туре	Reset	Description
7:4	RESERVED	R	b	Reserved
3	EN_TS_OW	R/W	1b	Allow Timestamp recording overwrite  0 = Disabled.  If sequence timestamp data is available in the SEQ_TIME_xSB[N] registers and the SEQ_REC_STAT.TS_RDY bit is set (data not read yet), a new sequence does not overwrite the existing data.  1 = Enabled (default).  Sequence timestamp data is overwritten with a new sequence, irrelevant of the SEQ_REC_STAT.TS_RDY bit.
2	EN_SEQ_OW	R/W	1b	Allow Sequence Order recording overwrite  0 = Disabled.  If sequence order data is available in the  SEQ_ON_LOG[N], SEQ_OFF_LOG[N], SEQ_EXS_LOG[N], or SEQ_ENS_LOG[N] registers, and the respective  SEQ_REC_STAT.SEQ_ON_RDY, SEQ_REC_STAT.SEQ_OFF_RDY, SEQ_REC_STAT.SEQ_EXS_RDY, or  SEQ_REC_STAT.SEQ_ENS_RDY bit is set (data not read yet), a new sequence does not overwrite the existing data.  1 = Enabled (default).  Sequence order data is overwritten with a new sequence, regradless of the  SEQ_REC_STAT.SEQ_ON_RDY, SEQ_REC_STAT.SEQ_OFF_RDY, SEQ_REC_STAT.SEQ_EXS_RDY, or  SEQ_REC_STAT.SEQ_EXS_RDY bit.
1	REQ_PEC	R/W	b	Require PEC byte (valid only if EN_PEC is 1): 0 = missing PEC byte is treated as good PEC 1 = missing PEC byte is treated as bad PEC, triggering a fault
0	EN_PEC	R/W	b	PEC: 0 = PEC disabled (default) 1 = PEC enabled

# 7.5.2.3 TEST\_CFG Register (Address = 0x12) [Reset = 0xX0]

TEST\_CFG is shown in Table 7-96.

Return to the Summary Table.

Built-In Self Test BIST execution configuration.

Table 7-96. TEST\_CFG Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:4	RESERVED	R	b	Reserved



Table 7-96. TEST\_CFG Register Field Descriptions (continued)

	i i ioi a 2000 i più oi io (con i i i ao a)			
Bit	Field	Туре	Reset	Description
3	AT_SHDN	R/W	xb	Run BIST when exiting ACTIVE state due to ACT transitioning 1 to 0. Device ready after tCFG_WB. This bit cannot be set in OTP/NVM. Always defaults to 0 when loading configuration from OTP/NVM.
2	RESERVED	R	b	
1:0	AT_POR	R/W	xxb	Run BIST at POR. Device ready after tCFG_WB.  00b = Valid OTP configuration, skip BIST at POR  01b = Corrupt OTP configuration, run BIST at POR  10b = Corrupt OTP configuration, run BIST at POR  11b = Valid OTP configuration, run BIST at POR

#### 7.5.2.4 IEN\_UVHF Register (Address = 0x13) [Reset = 0x00]

IEN\_UVHF is shown in Table 7-97.

Return to the Summary Table.

High Frequency channel Undervoltage Interrupt Enable register.

Table 7-97. IEN\_UVHF Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	MON[N]	R/W		Undervoltage High Frequency fault Interrupt Enable for VIN channel N ( 1 through 8). 0 = Interrupt disabled 1 = Interrupt enabled

#### 7.5.2.5 IEN\_UVLF Register (Address = 0x14) [Reset = 0x00]

IEN\_UVLF is shown in Table 7-98.

Return to the Summary Table.

Low Frequency channel Undervoltage Interrupt Enable register.

Table 7-98. IEN\_UVLF Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	MON[N]	R/W		Undervoltage Low Frequency fault Interrupt Enable for VIN channel N ( 1 through 8). 0 = Interrupt disabled 1 = Interrupt enabled

# 7.5.2.6 IEN\_OVHF Register (Address = 0x15) [Reset = 0x00]

IEN\_OVHF is shown in Table 7-99.

Return to the Summary Table.

High Frequency channel Overvoltage Interrupt Enable register.

Table 7-99. IEN OVHF Register Field Descriptions

	Table 7 00: 1214_0 viii Register Field Besonptions						
Bit	Field	Туре	Reset	Description			
7:0	MON[N]	R/W	b	Overvoltage High Frequency fault Interrupt Enable for VIN channel N ( 1 through 8). 0 = Interrupt disabled 1 = Interrupt enabled			

#### 7.5.2.7 IEN\_OVLF Register (Address = 0x16) [Reset = 0x00]

IEN\_OVLF is shown in Table 7-100.

Return to the Summary Table.

Low Frequency channel Overvoltage Interrupt Enable register.

Table 7-100. IEN\_OVLF Register Field Descriptions

_					<u> </u>
	Bit	Field	Туре	Reset	Description
	7:0	MON[N]	R/W		Overvoltage Low Frequency fault Interrupt Enable for VIN channel N ( 1 through 8). 0 = Interrupt disabled 1 = Interrupt enabled

# 7.5.2.8 IEN\_SEQ\_ON Register (Address = 0x17) [Reset = 0x00]

IEN SEQ ON is shown in Table 7-101.

Return to the Summary Table.

Power ON Sequence ACT transition 0 to 1 Interrupt Enable register.

# Table 7-101. IEN\_SEQ\_ON Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:6	RESERVED	R	b	Reserved
5:0	MON[N]	R/W	b	Power ON Sequence Fault Interrupt Enable for VIN channel N ( 1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled

#### 7.5.2.9 IEN\_SEQ\_OFF Register (Address = 0x18) [Reset = 0x00]

IEN\_SEQ\_OFF is shown in Table 7-102.

Return to the Summary Table.

Power OFF Sequence ACT transition 1 to 0 Interrupt Enable register.

#### Table 7-102. IEN\_SEQ\_OFF Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:6	RESERVED	R	b	Reserved
5:0	MON[N]	R/W	b	Power OFF Sequence Fault Interrupt Enable for VIN channel N ( 1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled

# 7.5.2.10 IEN\_SEQ\_EXS Register (Address = 0x19) [Reset = 0x00]

IEN\_SEQ\_EXS is shown in Table 7-103.

Return to the Summary Table.

Exit Sleep Sequence SLEEP transition 0 to 1 Interrupt Enable register.

# Table 7-103. IEN\_SEQ\_EXS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:6	RESERVED	R	b	Reserved
5:0	MON[N]	R/W	b	Exit Sleep Sequence Fault Interrupt Enable for VIN channel N ( 1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled

# 7.5.2.11 IEN\_SEQ\_ENS Register (Address = 0x1A) [Reset = 0x00]

IEN\_SEQ\_ENS is shown in Table 7-104.

Return to the Summary Table.

Entry Sleep Sequence SLEEP transition 1 to 0 Interrupt Enable register.

# Table 7-104. IEN\_SEQ\_ENS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:6	RESERVED	R	b	Reserved
5:0	MON[N]	R/W	b	Entry Sleep Sequence Fault Interrupt Enable for VIN channel N ( 1 through 6). 0 = Interrupt disabled 1 = Interrupt enabled

#### 7.5.2.12 IEN\_CONTROL Register (Address = 0x1B) [Reset = 0x0X]

IEN\_CONTROL is shown in Table 7-105.

Return to the Summary Table.

Control and Communication Fault Interrupt Enable register.

# Table 7-105. IEN\_CONTROL Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:5	RESERVED	R	b	Reserved
4	RT_CRC Int	R/W	b	Runtime register Cyclic Redundancy Check (CRC) fault interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled
3	RESERVED	R	b	Reserved
2	TSD Int	R/W	b	Thermal Shutdown fault interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled
1	SYNC Int	R/W	b	SYNC pin fault (short to supply or ground detected on SYNC pin) interrupt enable:  0 = Interrupt disabled  1 = Interrupt enabled

Table 7-105. IEN\_CONTROL Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
0	PEC Int	R/W		PEC fault (mismatch) interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled

# 7.5.2.13 IEN\_TEST Register (Address = 0x1C) [Reset = 0x0X]

IEN\_TEST is shown in Table 7-106.

Return to the Summary Table.

Internal Test and Configuration Load Fault Interrupt Enable register.

# Table 7-106. IEN\_TEST Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:4	RESERVED	R	b	Reserved
3	ECC_SEC	R/W	b	ECC single-error correction fault (on OTP load) interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled
2	RESERVED	R	b	Reserved
1	BIST_Complete_INT	R/W	b	Built-In Self-Test complete interrupt enable: 0 = Interrupt disabled 1 = Interrupt enabled
0	BIST_Fail_INT	R/W	b	Built-In Self-Test fault interrupt enable:  0 = Interrupt disabled  1 = Interrupt enabled Although expected to be always enabled, it is desirable to have the option to disable the interrupt.

#### 7.5.2.14 IEN\_VENDOR Register (Address = 0x1D) [Reset = 0xX0]

IEN\_VENDOR is shown in Table 7-107.

Return to the Summary Table.

Vendor Specific Internal Interrupt Enable register.

#### Table 7-107. IEN VENDOR Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	RESERVED	R	b	Reserved

# 7.5.2.15 MON\_CH\_EN Register (Address = 0x1E) [Reset = 0x00]

MON\_CH\_EN is shown in Table 7-108.

Return to the Summary Table.

Channel 1-8 Voltage Monitoring Enable register.

# Table 7-108. MON\_CH\_EN Register Field Descriptions

Bit	Field	Туре	Reset	Description			
7:0	MON[N]	R/W	b	Voltage Monitoring Enable for VIN channel N ( 1 through 8). 0 = Channel Monitor disabled 1 = Channel Monitor enabled			

# 7.5.2.16 VRANGE\_MULT Register (Address = 0x1F) [Reset = 0x00]

VRANGE\_MULT is shown in Table 7-109.

Return to the Summary Table.

Channel 1-8 Voltage Monitoring Range/Scaling register.

#### Table 7-109. VRANGE\_MULT Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	MON[N]	R/W	b	Voltage Monitoring Range/Scaling for VIN channel N (
				1 through
				8).
				0 =
				1x scaling (
				0.
				2V to
				1.
				475V with
				5mV steps)
				1 =
				4x scaling (
				0.
				8V to
				5.
				9V with
				20mV steps)

#### 7.5.2.17 UV\_HF[1] Register (Address = 0x20) [Reset = 0x00]

UV\_HF[1] is shown in Table 7-110.

Return to the Summary Table.

Channel 1 High Frequency channel Undervoltage threshold.

#### Table 7-110. UV\_HF[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV.  With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

#### 7.5.2.18 OV\_HF[1] Register (Address = 0x21) [Reset = 0xFF]

OV\_HF[1] is shown in Table 7-111.

Return to the Summary Table.

Channel 1 High Frequency channel Overvoltage threshold.

Table 7-111. OV\_HF[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.19 UV\_LF[1] Register (Address = 0x22) [Reset = 0x00]

UV\_LF[1] is shown in Table 7-112.

Return to the Summary Table.

Channel 1 Low Frequency channel Undervoltage threshold.

#### Table 7-112. UV\_LF[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV.  With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# $7.5.2.20 \text{ OV}_{LF[1]} \text{ Register (Address = 0x23) [Reset = 0xFF]}$

OV\_LF[1] is shown in Table 7-113.

Return to the Summary Table.

Channel 1 Low Frequency channel Overvoltage threshold.

#### Table 7-113. OV LF[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.21 FLT\_HF[1] Register (Address = 0x24) [Reset = 0x00]

FLT\_HF[1] is shown in Table 7-114.

Return to the Summary Table.

Channel 1 debounce filter for High Frequency Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.



#### Table 7-114. FLT\_HF[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:4	OV_DEB[3:0]	R/W	b	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	b	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

#### 7.5.2.22 FC\_LF[1] Register (Address = 0x25) [Reset = 0x14]

FC\_LF[1] is shown in Table 7-115.

Return to the Summary Table.

Channel 1 Low Frequency Path Cutoff Frequency 3dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies. The register also sets the mapping for OV\_HF[1]/UV\_HF[1] faults to the Reset pin

Table 7-115. FC\_LF[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:5	RESERVED	R	b	Reserved
4:3	UV_HF_1 to NRST	R/W	10b	Mapping to NRST  00 = HF faults not mapped  01 = UV_HF 1 mapped  10 = OV_HF 1 mapped  11 = UV_HF 1 and OV_HF 1 mapped
2:0	THRESHOLD[2:0]	R/W	100ь	Low frequency cutoff. 000b = Invalid 001b = Invalid 010b = 250Hz 011b = 500Hz 100b = 1kHz (default) 101b = 2kHz 110b = 4kHz 111b = Invalid

# 7.5.2.23 UV\_HF[2] Register (Address = 0x30) [Reset = 0x00]

UV\_HF[2] is shown in Table 7-116.

Return to the Summary Table.

Channel 2 High Frequency channel Undervoltage threshold.

Table 7-116. UV\_HF[2] Register Field Descriptions

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	Bit	Field	Туре	Reset	Description
	7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# $7.5.2.24 \text{ OV}_{\text{HF}[2]} \text{ Register (Address = 0x31) [Reset = 0xFF]}$

OV\_HF[2] is shown in Table 7-117.

Return to the Summary Table.

Channel 2 High Frequency channel Overvoltage threshold.

#### Table 7-117. OV\_HF[2] Register Field Descriptions

_					<u></u>
	Bit	Field	Туре	Reset	Description
	7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.25 UV\_LF[2] Register (Address = 0x32) [Reset = 0x00]

UV\_LF[2] is shown in Table 7-118.

Return to the Summary Table.

Channel 2 Low Frequency channel Undervoltage threshold.

# Table 7-118. UV\_LF[2] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.26 OV\_LF[2] Register (Address = 0x33) [Reset = 0xFF]

OV\_LF[2] is shown in Table 7-119.

Return to the Summary Table.

Channel 2 Low Frequency channel Overvoltage threshold.



#### Table 7-119. OV\_LF[2] Register Field Descriptions

				•
Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.27 FLT\_HF[2] Register (Address = 0x34) [Reset = 0x00]

FLT\_HF[2] is shown in Table 7-120.

Return to the Summary Table.

Channel 2 debounce filter for HF Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

#### Table 7-120. FLT\_HF[2] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:4	OV_DEB[3:0]	R/W	b	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	b	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

#### 7.5.2.28 FC\_LF[2] Register (Address = 0x35) [Reset = 0x14]

FC\_LF[2] is shown in Table 7-121.

Return to the Summary Table.

Channel 2 Low Frequency Path Cutoff Frequency 3dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies. The register also sets the mapping for OV\_HF[2]/UV\_HF[2] faults to the Reset pin

# Table 7-121. FC\_LF[2] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:5	RESERVED	R	b	Reserved
4:3	UV_HF_2 to NRST	R/W		Mapping to NRST  00 = HF faults not mapped  01 = UV_HF_ 2 mapped  10 = OV_HF_ 2 mapped  11 = UV_HF_ 2 and OV_HF_ 2 mapped

Table 7-121. FC\_LF[2] Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description
2:0	THRESHOLD[2:0]	R/W	100b	000b = Invalid 001b = Invalid 010b = 250Hz 011b = 500Hz 100b = 1kHz (default) 101b = 2kHz 110b = 4kHz 111b = Invalid

# 7.5.2.29 UV\_HF[3] Register (Address = 0x40) [Reset = 0x00]

UV\_HF[3] is shown in Table 7-122.

Return to the Summary Table.

Channel 3 High Frequency channel Undervoltage threshold.

#### Table 7-122. UV HF[3] Register Field Descriptions

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	Bit	Field	Туре	Reset	Description
	7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.30 OV\_HF[3] Register (Address = 0x41) [Reset = 0xFF]

OV\_HF[3] is shown in Table 7-123.

Return to the Summary Table.

Channel 3 High Frequency channel Overvoltage threshold.

#### Table 7-123. OV HF[3] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.31 UV\_LF[3] Register (Address = 0x42) [Reset = 0x00]

UV\_LF[3] is shown in Table 7-124.

Return to the Summary Table.

Channel 3 Low Frequency channel Undervoltage threshold.



# Table 7-124. UV\_LF[3] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.32 OV\_LF[3] Register (Address = 0x43) [Reset = 0xFF]

OV\_LF[3] is shown in Table 7-125.

Return to the Summary Table.

Channel 3 Low Frequency channel Overvoltage threshold.

# Table 7-125. OV\_LF[3] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.33 FLT\_HF[3] Register (Address = 0x44) [Reset = 0x00]

FLT\_HF[3] is shown in Table 7-126.

Return to the Summary Table.

Channel 3 debounce filter for HF Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

#### Table 7-126, FLT HF[3] Register Field Descriptions

idato : izo: z z z z z z z z z z z z z z z z z z							
Bit	Field	Туре	Reset	Description			
7:4	OV_DEB[3:0]	R/W	b	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs			
3:0	UV_DEB[3:0]	R/W	b	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs			

# 7.5.2.34 FC\_LF[3] Register (Address = 0x45) [Reset = 0x14]

FC\_LF[3] is shown in Table 7-127.

Return to the Summary Table.



Channel 3 Low Frequency Path Cutoff Frequency 3dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies. The register also sets the mapping for OV\_HF[3]/UV\_HF[3] faults to the Reset pin

Table 7-127. FC\_LF[3] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:5	RESERVED	R	b	Reserved
4:3	UV_HF_3 to NRST	R/W	10b	Mapping to NRST  00 = HF faults not mapped  01 = UV_HF 3 mapped  10 = OV_HF 3 mapped  11 = UV_HF 3 and OV_HF 3 mapped
2:0	THRESHOLD[2:0]	R/W	100ь	000b = Invalid 001b = Invalid 010b = 250Hz 011b = 500Hz 100b = 1kHz (default) 101b = 2kHz 110b = 4kHz 111b = Invalid

#### 7.5.2.35 UV\_HF[4] Register (Address = 0x50) [Reset = 0x00]

UV\_HF[4] is shown in Table 7-128.

Return to the Summary Table.

Channel 4 High Frequency channel Undervoltage threshold.

Table 7-128. UV\_HF[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.36 OV\_HF[4] Register (Address = 0x51) [Reset = 0xFF]

OV HF[4] is shown in Table 7-129.

Return to the Summary Table.

Channel 4 High Frequency channel Overvoltage threshold.

# Table 7-129. OV\_HF[4] Register Field Descriptions

_					<u> </u>
	Bit	Field	Туре	Reset	Description
	7:0	THRESHOLD[7:0]	R/W	111111111b	Overvoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.37 UV\_LF[4] Register (Address = 0x52) [Reset = 0x00]

UV\_LF[4] is shown in Table 7-130.

Return to the Summary Table.

Channel 4 Low Frequency channel Undervoltage threshold.

#### Table 7-130. UV\_LF[4] Register Field Descriptions

				•
Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# $7.5.2.38 \text{ OV}_{LF}[4] \text{ Register (Address = 0x53) [Reset = 0xFF]}$

OV\_LF[4] is shown in Table 7-131.

Return to the Summary Table.

Channel 4 Low Frequency channel Overvoltage threshold.

#### Table 7-131. OV\_LF[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.39 FLT\_HF[4] Register (Address = 0x54) [Reset = 0x00]

FLT\_HF[4] is shown in Table 7-132.

Return to the Summary Table.

Channel 4 debounce filter for HF Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

# Table 7-132. FLT\_HF[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:4	OV_DEB[3:0]	R/W	b	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	b	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs



# 7.5.2.40 FC\_LF[4] Register (Address = 0x55) [Reset = 0x14]

FC\_LF[4] is shown in Table 7-133.

Return to the Summary Table.

Channel 4 Low Frequency Path Cutoff Frequency 3dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies. The register also sets the mapping for OV\_HF[4]/UV\_HF[4] faults to the Reset pin

Table 7-133. FC LF[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:5	RESERVED	R	b	Reserved
4:3	UV_HF_4 to NRST	R/W	10b	Mapping to NRST  00 = HF faults not mapped  01 = UV_HF 4 mapped  10 = OV_HF 4 mapped  11 = UV_HF 4 and OV_HF 4 mapped
2:0	THRESHOLD[2:0]	R/W	100ь	000b = Invalid 001b = Invalid 010b = 250Hz 011b = 500Hz 100b = 1kHz (default) 101b = 2kHz 110b = 4kHz 111b = Invalid

#### 7.5.2.41 UV\_HF[5] Register (Address = 0x60) [Reset = 0x00]

UV HF[5] is shown in Table 7-134.

Return to the Summary Table.

Channel 5 High Frequency channel Undervoltage threshold.

Table 7-134. UV\_HF[5] Register Field Descriptions

_					<u> </u>
	Bit	Field	Туре	Reset	Description
	7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.42 OV\_HF[5] Register (Address = 0x61) [Reset = 0xFF]

OV\_HF[5] is shown in Table 7-135.

Return to the Summary Table.

Channel 5 High Frequency channel Overvoltage threshold.



# Table 7-135. OV\_HF[5] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.43 UV\_LF[5] Register (Address = 0x62) [Reset = 0x00]

UV\_LF[5] is shown in Table 7-136.

Return to the Summary Table.

Channel 5 Low Frequency channel Undervoltage threshold.

#### Table 7-136. UV\_LF[5] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# $7.5.2.44 \text{ OV}_{LF[5]} \text{ Register (Address = 0x63) [Reset = 0xFF]}$

OV\_LF[5] is shown in Table 7-137.

Return to the Summary Table.

Channel 5 Low Frequency channel Overvoltage threshold.

#### Table 7-137. OV\_LF[5] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W		Overvoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

#### 7.5.2.45 FLT\_HF[5] Register (Address = 0x64) [Reset = 0x00]

FLT\_HF[5] is shown in Table 7-138.

Return to the Summary Table.

Channel 5 debounce filter for HF Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

Table 7-138. FLT\_HF[5] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:4	OV_DEB[3:0]	R/W	b	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	b	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

#### 7.5.2.46 FC\_LF[5] Register (Address = 0x65) [Reset = 0x14]

FC\_LF[5] is shown in Table 7-139.

Return to the Summary Table.

Channel 5 Low Frequency Path Cutoff Frequency 3dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies. The register also sets the mapping for OV\_HF[5]/UV\_HF[5] faults to the Reset pin for parts with reset pin

Table 7-139. FC\_LF[5] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:5	RESERVED	R	b	Reserved
4:3	UV_HF_5 to NRST	R/W	10b	Mapping to NRST  00 = HF faults not mapped  01 = UV_HF 5 mapped  10 = OV_HF 5 mapped  11 = UV_HF 5 and OV_HF 5 mapped
2:0	THRESHOLD[2:0]	R/W	100Ь	000b = Invalid 001b = Invalid 010b = 250Hz 011b = 500Hz 100b = 1kHz (default) 101b = 2kHz 110b = 4kHz 111b = Invalid

#### 7.5.2.47 UV\_HF[6] Register (Address = 0x70) [Reset = 0x00]

UV\_HF[6] is shown in Table 7-140.

Return to the Summary Table.

Channel 6 High Frequency channel Undervoltage threshold.



#### Table 7-140. UV\_HF[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.48 OV\_HF[6] Register (Address = 0x71) [Reset = 0xFF]

OV\_HF[6] is shown in Table 7-141.

Return to the Summary Table.

Channel 6 High Frequency channel Overvoltage threshold.

#### Table 7-141. OV\_HF[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.49 UV\_LF[6] Register (Address = 0x72) [Reset = 0x00]

UV\_LF[6] is shown in Table 7-142.

Return to the Summary Table.

Channel 6 Low Frequency channel Undervoltage threshold.

# Table 7-142. UV\_LF[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

#### 7.5.2.50 OV\_LF[6] Register (Address = 0x73) [Reset = 0xFF]

OV\_LF[6] is shown in Table 7-143.

Return to the Summary Table.

Channel 6 Low Frequency channel Overvoltage threshold.

Table 7-143. OV\_LF[6] Register Field Descriptions

				. Э
Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.51 FLT\_HF[6] Register (Address = 0x74) [Reset = 0x00]

FLT\_HF[6] is shown in Table 7-144.

Return to the Summary Table.

Channel 6 debounce filter for HF Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

Table 7-144. FLT\_HF[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:4	OV_DEB[3:0]	R/W	b	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	b	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

#### 7.5.2.52 FC\_LF[6] Register (Address = 0x75) [Reset = 0x14]

FC\_LF[6] is shown in Table 7-145.

Return to the Summary Table.

Channel 6 Low Frequency Path Cutoff Frequency 3dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies. The register also sets the mapping for OV\_HF[6]/UV\_HF[6] faults to the Reset pin for parts with reset pin

Table 7-145. FC\_LF[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:5	RESERVED	R	b	Reserved
4:3	UV_HF_6 to NRST	R/W	10b	Mapping to NRST  00 = HF faults not mapped  01 = UV_HF_ 6 mapped  10 = OV_HF_ 6 mapped  11 = UV_HF_ 6 and OV_HF_ 6 mapped



# Table 7-145. FC\_LF[6] Register Field Descriptions (continued)

			1 - 5	
Bit	Field	Туре	Reset	Description
2:0	THRESHOLD[2:0]	R/W	100b	000b = Invalid 001b = Invalid
				010b = 250Hz   011b = 500Hz
				100b = 1kHz (default)
				101b = 2kHz
				110b = 4kHz
				111b = Invalid

# 7.5.2.53 UV\_HF[7] Register (Address = 0x80) [Reset = 0x00]

UV\_HF[7] is shown in Table 7-146.

Return to the Summary Table.

Channel 7 High Frequency channel Undervoltage threshold.

# Table 7-146. UV\_HF[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.54 OV\_HF[7] Register (Address = 0x81) [Reset = 0xFF]

OV\_HF[7] is shown in Table 7-147.

Return to the Summary Table.

Channel 7 High Frequency channel Overvoltage threshold.

#### Table 7-147. OV HF[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.55 UV\_LF[7] Register (Address = 0x82) [Reset = 0x00]

UV\_LF[7] is shown in Table 7-148.

Return to the Summary Table.

Channel 7 Low Frequency channel Undervoltage threshold.

Table 7-148. UV\_LF[7] Register Field Descriptions

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	Bit	Field	Туре	Reset	Description
	7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.56 OV\_LF[7] Register (Address = 0x83) [Reset = 0xFF]

OV\_LF[7] is shown in Table 7-149.

Return to the Summary Table.

Channel 7 Low Frequency channel Overvoltage threshold.

#### Table 7-149. OV\_LF[7] Register Field Descriptions

				<u>.                                      </u>
Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.57 FLT\_HF[7] Register (Address = 0x84) [Reset = 0x00]

FLT\_HF[7] is shown in Table 7-150.

Return to the Summary Table.

Channel 7 debounce filter for HF Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

# Table 7-150. FLT\_HF[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:4	OV_DEB[3:0]	R/W	b	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	b	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

# 7.5.2.58 FC\_LF[7] Register (Address = 0x85) [Reset = 0x14]

FC\_LF[7] is shown in Table 7-151.

Return to the Summary Table.



Channel 7 Low Frequency Path Cutoff Frequency 3dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies. The register also sets the mapping for OV\_HF[6]/UV\_HF[6] faults to the Reset pin for parts with reset pin

Table 7-151. FC\_LF[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:3	RESERVED	R	b	Reserved
2:0	THRESHOLD[2:0]	R/W	100ь	000b = Invalid 001b = Invalid 010b = 250Hz 011b = 500Hz 100b = 1kHz (default) 101b = 2kHz 110b = 4kHz 111b = Invalid

#### 7.5.2.59 UV\_HF[8] Register (Address = 0x90) [Reset = 0x00]

UV HF[8] is shown in Table 7-152.

Return to the Summary Table.

Channel 8 High Frequency channel Undervoltage threshold.

Table 7-152. UV\_HF[8] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

#### 7.5.2.60 OV\_HF[8] Register (Address = 0x91) [Reset = 0xFF]

OV HF[8] is shown in Table 7-153.

Return to the Summary Table.

Channel 8 High Frequency channel Overvoltage threshold.

#### Table 7-153. OV\_HF[8] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for High Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

#### 7.5.2.61 UV\_LF[8] Register (Address = 0x92) [Reset = 0x00]

UV\_LF[8] is shown in Table 7-154.

Return to the Summary Table.

Channel 8 Low Frequency channel Undervoltage threshold.

Table 7-154. UV\_LF[8] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	b	Undervoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.62 OV\_LF[8] Register (Address = 0x93) [Reset = 0xFF]

OV\_LF[8] is shown in Table 7-155.

Return to the Summary Table.

Channel 8 Low Frequency channel Overvoltage threshold.

#### Table 7-155. OV\_LF[8] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	THRESHOLD[7:0]	R/W	11111111b	Overvoltage threshold for Low Frequency component of monitored channel.  The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT.  With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

# 7.5.2.63 FLT\_HF8] Register (Address = 0x94) [Reset = 0x00]

FLT\_HF8] is shown in Table 7-156.

Return to the Summary Table.

Channel 8 debounce filter for HF Fault. The smallest value supported is 0.4 us, The largest is 102.4 us.

#### Table 7-156. FLT HF81 Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:4	OV_DEB[3:0]	R/W	b	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	b	Undervoltage comparator output debounce time (don't assert until output is stable for debounce time) for High Frequency monitoring path.  0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

# 7.5.2.64 FC\_LF[8] Register (Address = 0x95) [Reset = 0x14]

FC\_LF[8] is shown in Table 7-157.

Return to the Summary Table.



Channel 8 Low Frequency Path Cutoff Frequency 3dB point. The register changes the filter properties of the programmable LPF such that the total frequency response meets these cutoff frequencies. The register also sets the mapping for OV\_HF[6]/UV\_HF[6] faults to the Reset pin for parts with reset pin

Table 7-157. FC\_LF[8] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:3	RESERVED	R	b	Reserved
2:0	THRESHOLD[2:0]	R/W	100ь	000b = Invalid 001b = Invalid 010b = 250Hz 011b = 500Hz 100b = 1kHz (default) 101b = 2kHz 110b = 4kHz 111b = Invalid

#### 7.5.2.65 TI\_CONTROL Register (Address = 0x9F) [Reset = 0x02]

TI CONTROL is shown in Table 7-158.

Return to the Summary Table.

Manual BIST entry and Reset delay setting register.

Table 7-158. TI CONTROL Register Field Descriptions

			1	Trogister i leia Descriptions
Bit	Field	Туре	Reset	Description
7	ENTER_BIST	R/W	b	Manual BIST 1= Enter BIST
6	RSVD	R/W	b	RSVD
5	Manual Reset	R/W	b	Manual Reset: 0 = Reset not asserted 1 = Reset asserted
4:3	RESERVED	R	b	Reserved
2:0	Reset delay time	R/W	10b	Reset delay time 000b = 200µs 001b = 1ms 010b = 10ms (default) 011b = 16ms 100b = 20ms 101b = 70ms 110b = 100ms 111b = 200ms

#### 7.5.2.66 SEQ\_REC\_CTL Register (Address = 0xA0) [Reset = 0x00]

SEQ\_REC\_CTL is shown in Table 7-159.

Return to the Summary Table.

Sequence control register.

Table 7-159. SEQ\_REC\_CTL Register Field Descriptions

Bit	Field	Туре	Reset	Description
7	REC_START	R/W		Software start sequence logging (recording):  0 = Always read 0  1 = Initiate power sequence (selected by SEQ[1:0]) recording.

Table 7-159. SEQ\_REC\_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description Descriptions (continued)
6:5	SEQ[1:0]	R/W	b	Sequence to record (and compare for faults to corresponding expected sequence order registers):  00b = Power ON (same as ACT 0 to 1)  01b = Power OFF (ACT 1 to 0)  10b = Sleep Exit (SLEEP 0 to 1)  11b = Sleep Entry (SLEEP 1 to 0)
4	TS_ACK	R/W	b	Timestamp data OK to overwrite.  Valid and used only if VMON_MISC.EN_TS_OW=0.  00b = Always read 0  01b = Acknowledge Timestamp data and OK to overwrite.  SEQ_REC_STAT.TS_RDY and SEQ_OW_STAT.TS_OW are cleared.
3	SEQ_ON_ACK	R/W	b	Power ON sequence data OK to overwrite.  Valid and used only if VMON_MISC.EN_SEQ_OW=0.  00b = Always read 0  01b = Acknowledge Power ON sequence data and OK to overwrite.  SEQ_REC_STAT.SEQ_ON_RDY and  SEQ_OW_STAT.SEQ_ON_OW are cleared.
2	SEQ_OFF_ACK	R/W	b	Power OFF sequence data OK to overwrite.  Valid and used only if VMON_MISC.EN_SEQ_OW=0.  00b = Always read 0  01b = Acknowledge Power OFF sequence data and OK to overwrite.  SEQ_REC_STAT.SEQ_OFF_RDY and  SEQ_OW_STAT.SEQ_OFF_OW are cleared.
1	SEQ_EXS_ACK	R/W	b	Sleep Exit sequence data OK to overwrite.  Valid and used only if VMON_MISC.EN_SEQ_OW=0.  00b = Always read 0  01b = Acknowledge Sleep Exit sequence data and OK to overwrite.  SEQ_REC_STAT.SEQ_EXS_RDY and  SEQ_OW_STAT.SEQ_EXS_OW are cleared.
0	SEQ_ENS_ACK	R/W	b	Sleep Entry sequence data OK to overwrite.  Valid and used only if VMON_MISC.EN_SEQ_OW=0.  00b = Always read 0  01b = Acknowledge Sleep Entry sequence data and OK to overwrite.  SEQ_REC_STAT.SEQ_ENS_RDY and  SEQ_OW_STAT.SEQ_ENS_OW are cleared.

# 7.5.2.67 AMSK\_ON Register (Address = 0xA1) [Reset = 0xFF]

AMSK\_ON is shown in Table 7-160.

Return to the Summary Table.

Auto-mask ON register. This register is used to mask UVLF, UVHF, and OVHF interrupts on ACT transition 0 to 1 transitions.

Table 7-160. AMSK\_ON Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	MON[N]	R/W		Auto-mask on ACT 0 to 1 transition for IEN_UVLF, IEN_UVHF, and IEN_OVHF for VIN channel N (1 through 8).  00b = Channel interrupts not auto-masked  01b = Channel interrupts auto-masked

# 7.5.2.68 AMSK\_OFF Register (Address = 0xA2) [Reset = 0xFF]

AMSK\_OFF is shown in Table 7-161.

Return to the Summary Table.



Auto-mask OFF register. This register is used to mask UVLF, UVHF, and OVHF interrupts on ACT transition 1 to 0 transitions.

#### Table 7-161. AMSK\_OFF Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	MON[N]	R/W		Auto-mask on ACT 1 to 0 transition for IEN_UVLF, IEN_UVHF, and IEN_OVHF for VIN channel N (1 through 8).  00b = Channel interrupts not auto-masked  01b = Channel interrupts auto-masked

# 7.5.2.69 AMSK\_EXS Register (Address = 0xA3) [Reset = 0xFF]

AMSK EXS is shown in Table 7-162.

Return to the Summary Table.

Auto-mask EXIT register. This register is used to mask UVLF, UVHF, and OVHF interrupts on SLEEP transition 0 to 1 transitions.

# Table 7-162. AMSK\_EXS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	MON[N]	R/W		Auto-mask on SLEEP 0 to 1 transition for IEN_UVLF, IEN_UVHF, and IEN_OVHF for VIN channel N (1 through 8).  00b = Channel interrupts not auto-masked  01b = Channel interrupts auto-masked

#### 7.5.2.70 AMSK\_ENS Register (Address = 0xA4) [Reset = 0xFF]

AMSK\_ENS is shown in Table 7-163.

Return to the Summary Table.

Auto-mask ENTRY register. This register is used to mask UVLF, UVHF, and OVHF interrupts on SLEEP transition 1 to 0 transitions.

#### Table 7-163. AMSK\_ENS Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	MON[N]	R/W		Auto-mask on SLEEP 1 to 0 transition for IEN_UVLF, IEN_UVHF, and IEN_OVHF for VIN channel N (1 through 8).  00b = Channel interrupts not auto-masked  01b = Channel interrupts auto-masked

# 7.5.2.71 SEQ\_TOUT\_MSB Register (Address = 0xA5) [Reset = 0x00]

SEQ\_TOUT\_MSB is shown in Table 7-164.

Return to the Summary Table.

Sequence timeout most significant bits register.

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Table 7-164. SEQ\_TOUT\_MSB Register Field Descriptions

_					2 regional riola 2000 phone
	Bit	Field	Туре	Reset	Description
	7:0	MILLISEC[7:0]	R/W	b	ACT and SLEEP transition sequence timeout.  After the timeout, the auto-masks (AMSK_xxx) are released and the IEN_xVxF interrupts become active.  0x0  000 =  1ms  0x0  001 =  2ms  While the max value is not specified, it is desirable to be able to set this timeout up to 4s, and at least 256ms (using only the lower byte at address 0xA 6).

# 7.5.2.72 SEQ\_TOUT\_LSB Register (Address = 0xA6) [Reset = 0x00]

SEQ\_TOUT\_LSB is shown in Table 7-165.

Return to the Summary Table.

Sequence timeout least significant bits register.

# Table 7-165. SEQ\_TOUT\_LSB Register Field Descriptions

П			_	_	1 register i leia bescriptions
	Bit	Field	Туре	Reset	Description
	7:0	MILLISEC[7:0]	R/W	b	ACT and SLEEP transition sequence timeout.  After the timeout, the auto-masks (AMSK_xxx) are released and the IEN_xVxF interrupts become active.  0x0  000 = 1ms  0x0  001 = 2ms  While the max value is not specified, it is desirable to be able to set this timeout up to 4s, and at least 256ms (using only the lower byte at address 0xA 6).

# 7.5.2.73 SEQ\_SYNC Register (Address = 0xA7) [Reset = 0x00]

SEQ\_SYNC is shown in Table 7-166.

Return to the Summary Table.

Sequence SYNC pulse duration from 50 us to 2600 us.

# Table 7-166. SEQ\_SYNC Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	PULSE_WIDTH[7:0]	R/W	b	Pulse width for SYNC synchronization pulse.  00000000b = 50μs 00000001b = 60μs 00000010b = 70μs  111111101b = 2580μs 11111110b = 2590μs 111111111b = 2600μs

# 7.5.2.74 SEQ\_UP\_THLD Register (Address = 0xA8) [Reset = 0x1F]

SEQ\_UP\_THLD is shown in Table 7-167.



Return to the Summary Table.

Threshold selection register for up sequence tagging ACT and SLEEP transition 0 to 1 transitions.

#### Table 7-167. SEQ\_UP\_THLD Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	MON[N]	R/W		OFF (200 mV) or UV (UV_LF[N] register) threshold selection for Power ON and Exit Sleep sequence tagging:  00b = Use OFF threshold (200 mV)  01b = Use UV threshold (UV_LF[N] register)  0b = OFF  1b = UVLF

#### 7.5.2.75 SEQ\_DN\_THLD Register (Address = 0xA9) [Reset = 0x00]

SEQ DN THLD is shown in Table 7-168.

Return to the Summary Table.

Threshold selection register for down sequence tagging ACT and SLEEP transition 1 to 0 transitions.

#### Table 7-168. SEQ\_DN\_THLD Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	MON[N]	R/W	b	OFF (200 mV) or UV (UV_LF[N] register) threshold selection for Power OFF and Enter Sleep sequence tagging: 00b = Use OFF threshold (200 mV) 01b = Use UV threshold (UV_LF[N] register) 0b = OFF 1b = UVLF

#### 7.5.2.76 SEQ\_ON\_EXP[1] Register (Address = 0xB0) [Reset = 0x00]

SEQ\_ON\_EXP[1] is shown in Table 7-169.

Return to the Summary Table.

Channel 1 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 1.

#### Table 7-169. SEQ\_ON\_EXP[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W		Expected Power ON sequence order value for channel 1.  This sequence order value is compared with the SEQ_ON_LOG[1] register assigned to the channel during the sequence triggered by ACT.

#### 7.5.2.77 SEQ\_ON\_EXP[2] Register (Address = 0xB1) [Reset = 0x00]

SEQ\_ON\_EXP[2] is shown in Table 7-170.

Return to the Summary Table.

Channel 2 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 2.

Table 7-170. SEQ\_ON\_EXP[2] Register Field Descriptions

_			·		1
	Bit	Field	Туре	Reset	Description
	7:0	ORDER[7:0]	R/W		Expected Power ON sequence order value for channel 2. This sequence order value is compared with the SEQ_ON_LOG[2] register assigned to the channel during the sequence triggered by ACT.

# 7.5.2.78 SEQ\_ON\_EXP[3] Register (Address = 0xB2) [Reset = 0x00]

SEQ\_ON\_EXP[3] is shown in Table 7-171.

Return to the Summary Table.

Channel 3 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 3

Table 7-171. SEQ ON EXP[3] Register Field Descriptions

_			·		<u>.                                      </u>
	Bit	Field	Туре	Reset	Description
	7:0	ORDER[7:0]	R/W	b	Expected Power ON sequence order value for channel 3. This sequence order value is compared with the SEQ_ON_LOG[3] register assigned to the channel during the sequence triggered by ACT.

#### 7.5.2.79 SEQ\_ON\_EXP[4] Register (Address = 0xB3) [Reset = 0x00]

SEQ\_ON\_EXP[4] is shown in Table 7-172.

Return to the Summary Table.

Channel 4 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 4.

Table 7-172. SEQ\_ON\_EXP[4] Register Field Descriptions

_		· · · · · · · · · · · · · · · · · · ·						
	Bit	Field	Туре	Reset	Description			
	7:0	ORDER[7:0]	R/W		Expected Power ON sequence order value for channel 4. This sequence order value is compared with the SEQ_ON_LOG[4] register assigned to the channel during the sequence triggered by ACT.			

#### 7.5.2.80 SEQ\_ON\_EXP[5] Register (Address = 0xB4) [Reset = 0x00]

SEQ\_ON\_EXP[5] is shown in Table 7-173.

Return to the Summary Table.

Channel 5 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 5.

Table 7-173. SEQ\_ON\_EXP[5] Register Field Descriptions

-			·		
	Bit	Field	Туре	Reset	Description
	7:0	ORDER[7:0]	R/W	b	Expected Power ON sequence order value for channel 5. This sequence order value is compared with the SEQ_ON_LOG[5] register assigned to the channel during the sequence triggered by ACT.

#### 7.5.2.81 SEQ\_ON\_EXP[6] Register (Address = 0xB5) [Reset = 0x00]

SEQ\_ON\_EXP[6] is shown in Table 7-174.



Return to the Summary Table.

Channel 6 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 6.

Table 7-174. SEQ\_ON\_EXP[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Power ON sequence order value for channel 6. This sequence order value is compared with the SEQ_ON_LOG[6] register assigned to the channel during the sequence triggered by ACT.

# 7.5.2.82 SEQ\_ON\_EXP[7] Register (Address = 0xB6) [Reset = 0x00]

SEQ\_ON\_EXP[7] is shown in Table 7-175.

Return to the Summary Table.

Channel 7 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 7.

Table 7-175. SEQ\_ON\_EXP[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W		Expected Power ON sequence order value for channel 7. This sequence order value is compared with the SEQ_ON_LOG[5] register assigned to the channel during the sequence triggered by ACT.

# 7.5.2.83 SEQ\_ON\_EXP[8] Register (Address = 0xB7) [Reset = 0x00]

SEQ ON EXP[8] is shown in Table 7-176.

Return to the Summary Table.

Channel 8 Power ON sequence order expected value register. This register is used to set the value of the expected power-on sequence order for channel 8.

Table 7-176. SEQ\_ON\_EXP[8] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Power ON sequence order value for channel 8.  This sequence order value is compared with the SEQ_ON_LOG[6] register assigned to the channel during the sequence triggered by ACT.

#### 7.5.2.84 SEQ\_OFF\_EXP[1] Register (Address = 0xC0) [Reset = 0x00]

SEQ OFF EXP[1] is shown in Table 7-177.

Return to the Summary Table.

Channel 1 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 1.

Table 7-177. SEQ OFF EXP[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Power OFF sequence order value for channel 1. This sequence order value is compared with the SEQ_OFF_LOG[1] register assigned to the channel during the sequence triggered by ACT

## 7.5.2.85 SEQ\_OFF\_EXP[2] Register (Address = 0xC1) [Reset = 0x00]

SEQ\_OFF\_EXP[2] is shown in Table 7-178.

Return to the Summary Table.

Channel 2 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 2.

Table 7-178. SEQ\_OFF\_EXP[2] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W		Expected Power OFF sequence order value for channel 2. This sequence order value is compared with the SEQ_OFF_LOG[2] register assigned to the channel during the sequence triggered by ACT

## 7.5.2.86 SEQ\_OFF\_EXP[3] Register (Address = 0xC2) [Reset = 0x00]

SEQ\_OFF\_EXP[3] is shown in Table 7-179.

Return to the Summary Table.

Channel 3 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 3.

Table 7-179. SEQ\_OFF\_EXP[3] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Power OFF sequence order value for channel 3.  This sequence order value is compared with the SEQ_OFF_LOG[3] register assigned to the channel during the sequence triggered by ACT

### 7.5.2.87 SEQ\_OFF\_EXP[4] Register (Address = 0xC3) [Reset = 0x00]

SEQ\_OFF\_EXP[4] is shown in Table 7-180.

Return to the Summary Table.

Channel 4 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 4.

Table 7-180. SEQ\_OFF\_EXP[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W		Expected Power OFF sequence order value for channel 4. This sequence order value is compared with the SEQ_OFF_LOG[4] register assigned to the channel during the sequence triggered by ACT

# 7.5.2.88 SEQ\_OFF\_EXP[5] Register (Address = 0xC4) [Reset = 0x00]

SEQ\_OFF\_EXP[5] is shown in Table 7-181.

Return to the Summary Table.

Channel 5 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 5.



Table 7-181. SEQ\_OFF\_EXP[5] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W		Expected Power OFF sequence order value for channel 5. This sequence order value is compared with the SEQ_OFF_LOG[5] register assigned to the channel during the sequence triggered by ACT

## 7.5.2.89 SEQ\_OFF\_EXP[6] Register (Address = 0xC5) [Reset = 0x00]

SEQ OFF EXP[6] is shown in Table 7-182.

Return to the Summary Table.

Channel 6 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 6.

Table 7-182. SEQ\_OFF\_EXP[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Power OFF sequence order value for channel 6. This sequence order value is compared with the SEQ_OFF_LOG[6] register assigned to the channel during the sequence triggered by ACT

## 7.5.2.90 SEQ\_OFF\_EXP[7] Register (Address = 0xC6) [Reset = 0x00]

SEQ\_OFF\_EXP[7] is shown in Table 7-183.

Return to the Summary Table.

Channel 7 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 7.

Table 7-183, SEQ OFF EXP[7] Register Field Descriptions

_					1 -9
	Bit	Field	Туре	Reset	Description
	7:0	ORDER[7:0]	R/W	b	Expected Power OFF sequence order value for channel 7. This sequence order value is compared with the SEQ_OFF_LOG[5] register assigned to the channel during the sequence triggered by ACT

### 7.5.2.91 SEQ\_OFF\_EXP[8] Register (Address = 0xC7) [Reset = 0x00]

SEQ OFF EXP[8] is shown in Table 7-184.

Return to the Summary Table.

Channel 8 Power OFF sequence order expected value register. This register is used to set the value of the expected power-off sequence order for channel 8.

Table 7-184. SEQ OFF EXP[8] Register Field Descriptions

-					
	Bit	Field	Туре	Reset	Description
	7:0	ORDER[7:0]	R/W	b	Expected Power OFF sequence order value for channel 8. This sequence order value is compared with the SEQ_OFF_LOG[6] register assigned to the channel during the sequence triggered by ACT

## 7.5.2.92 SEQ\_EXS\_EXP[1] Register (Address = 0xD0) [Reset = 0x00]

SEQ\_EXS\_EXP[1] is shown in Table 7-185.



Return to the Summary Table.

Channel 1 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 1

Table 7-185. SEQ\_EXS\_EXP[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Sleep Exit sequence order value for channel 1.  This sequence order value is compared with the SEQ_EXS_LOG[1] register assigned to the channel during the sequence triggered by ACT/ SLEEP.

### $7.5.2.93 \text{ SEQ\_EXS\_EXP[2]} \text{ Register (Address = 0xD1) [Reset = 0x00]}$

SEQ\_EXS\_EXP[2] is shown in Table 7-186.

Return to the Summary Table.

Channel 2 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 2

Table 7-186. SEQ\_EXS\_EXP[2] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Sleep Exit sequence order value for channel 2. This sequence order value is compared with the SEQ_EXS_LOG[2] register assigned to the channel during the sequence triggered by ACT/ SLEEP.

## 7.5.2.94 SEQ\_EXS\_EXP[3] Register (Address = 0xD2) [Reset = 0x00]

SEQ EXS EXP[3] is shown in Table 7-187.

Return to the Summary Table.

Channel 3 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 3

Table 7-187. SEQ\_EXS\_EXP[3] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Sleep Exit sequence order value for channel 3.  This sequence order value is compared with the SEQ_EXS_LOG[3] register assigned to the channel during the sequence triggered by ACT/ SLEEP.

### 7.5.2.95 SEQ\_EXS\_EXP[4] Register (Address = 0xD3) [Reset = 0x00]

SEQ\_EXS\_EXP[4] is shown in Table 7-188.

Return to the Summary Table.

Channel 4 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 4

Table 7-188. SEQ EXS EXP[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Sleep Exit sequence order value for channel 4.  This sequence order value is compared with the SEQ_EXS_LOG[4] register assigned to the channel during the sequence triggered by ACT/ SLEEP.

## 7.5.2.96 SEQ\_EXS\_EXP[5] Register (Address = 0xD4) [Reset = 0x00]

SEQ\_EXS\_EXP[5] is shown in Table 7-189.

Return to the Summary Table.

Channel 5 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 5

Table 7-189, SEQ EXS EXP[5] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W		Expected Sleep Exit sequence order value for channel 5. This sequence order value is compared with the SEQ_EXS_LOG[5] register assigned to the channel during the sequence triggered by ACT/ SLEEP.

## 7.5.2.97 SEQ\_EXS\_EXP[6] Register (Address = 0xD5) [Reset = 0x00]

SEQ\_EXS\_EXP[6] is shown in Table 7-190.

Return to the Summary Table.

Channel 6 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 6

Table 7-190. SEQ\_EXS\_EXP[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Sleep Exit sequence order value for channel 6. This sequence order value is compared with the SEQ_EXS_LOG[6] register assigned to the channel during the sequence triggered by ACT/ SLEEP.

### 7.5.2.98 SEQ\_EXS\_EXP[7] Register (Address = 0xD6) [Reset = 0x00]

SEQ\_EXS\_EXP[7] is shown in Table 7-191.

Return to the Summary Table.

Channel 7 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 7

Table 7-191. SEQ\_EXS\_EXP[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W		Expected Sleep Exit sequence order value for channel 7. This sequence order value is compared with the SEQ_EXS_LOG[5] register assigned to the channel during the sequence triggered by ACT/ SLEEP.

## 7.5.2.99 SEQ\_EXS\_EXP[8] Register (Address = 0xD7) [Reset = 0x00]

SEQ\_EXS\_EXP[8] is shown in Table 7-192.

Return to the Summary Table.

Channel 8 Sleep Exit sequence order expected value register. This register is used to set the value of the expected sleep exit sequence order for channel 8

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Table 7-192. SEQ\_EXS\_EXP[8] Register Field Descriptions

				1
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W		Expected Sleep Exit sequence order value for channel 8.  This sequence order value is compared with the SEQ_EXS_LOG[6] register assigned to the channel during the sequence triggered by ACT/ SLEEP.

## 7.5.2.100 SEQ\_ENS\_EXP[1] Register (Address = 0xE0) [Reset = 0x00]

SEQ\_ENS\_EXP[1] is shown in Table 7-193.

Return to the Summary Table.

Channel 1 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 1

Table 7-193. SEQ\_ENS\_EXP[1] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W		Expected Sleep Entry sequence order value for channel 1. This sequence order value is compared with the SEQ_ENS_LOG[1] register assigned to the channel during the sequence triggered by SLEEP.

## 7.5.2.101 SEQ\_ENS\_EXP[2] Register (Address = 0xE1) [Reset = 0x00]

SEQ\_ENS\_EXP[2] is shown in Table 7-194.

Return to the Summary Table.

Channel 2 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 2

Table 7-194, SEQ\_ENS\_EXP[2] Register Field Descriptions

Bit	Field	Туре	Reset	Description						
7:0	ORDER[7:0]	R/W		Expected Sleep Entry sequence order value for channel 2. This sequence order value is compared with the SEQ_ENS_LOG[2] register assigned to the channel during the sequence triggered by SLEEP.						

### 7.5.2.102 SEQ\_ENS\_EXP[3] Register (Address = 0xE2) [Reset = 0x00]

SEQ\_ENS\_EXP[3] is shown in Table 7-195.

Return to the Summary Table.

Channel 3 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 3

Table 7-195. SEQ\_ENS\_EXP[3] Register Field Descriptions

				1
Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Sleep Entry sequence order value for channel 3. This sequence order value is compared with the SEQ_ENS_LOG[3] register assigned to the channel during the sequence triggered by SLEEP.

## 7.5.2.103 SEQ\_ENS\_EXP[4] Register (Address = 0xE3) [Reset = 0x00]

SEQ\_ENS\_EXP[4] is shown in Table 7-196.



Return to the Summary Table.

Channel 4 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 4

Table 7-196. SEQ\_ENS\_EXP[4] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Sleep Entry sequence order value for channel 4. This sequence order value is compared with the SEQ_ENS_LOG[4] register assigned to the channel during the sequence triggered by SLEEP.

## 7.5.2.104 SEQ\_ENS\_EXP[5] Register (Address = 0xE4) [Reset = 0x00]

SEQ\_ENS\_EXP[5] is shown in Table 7-197.

Return to the Summary Table.

Channel 5 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 5

Table 7-197. SEQ\_ENS\_EXP[5] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Sleep Entry sequence order value for channel 5. This sequence order value is compared with the SEQ_ENS_LOG[5] register assigned to the channel during the sequence triggered by SLEEP.

## 7.5.2.105 SEQ\_ENS\_EXP[6] Register (Address = 0xE5) [Reset = 0x00]

SEQ ENS EXP[6] is shown in Table 7-198.

Return to the Summary Table.

Channel 6 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 6

Table 7-198. SEQ\_ENS\_EXP[6] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W		Expected Sleep Entry sequence order value for channel 6. This sequence order value is compared with the SEQ_ENS_LOG[6] register assigned to the channel during the sequence triggered by SLEEP.

### 7.5.2.106 SEQ\_ENS\_EXP[7] Register (Address = 0xE6) [Reset = 0x00]

SEQ ENS EXP[7] is shown in Table 7-199.

Return to the Summary Table.

Channel 7 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 7

Table 7-199. SEQ ENS EXP[7] Register Field Descriptions

Bit	Field	Туре	Reset	Description
7:0	ORDER[7:0]	R/W	b	Expected Sleep Entry sequence order value for channel 7. This sequence order value is compared with the SEQ_ENS_LOG[5] register assigned to the channel during the sequence triggered by SLEEP.



# 7.5.2.107 SEQ\_ENS\_EXP[8] Register (Address = 0xE7) [Reset = 0x00]

SEQ\_ENS\_EXP[8] is shown in Table 7-200.

Return to the Summary Table.

Channel 8 Sleep Entry sequence order expected value register. This register is used to set the value of the expected sleep entry sequence order for channel 8

Table 7-200. SEQ\_ENS\_EXP[8] Register Field Descriptions

_										
	Bit	Field	Туре	Reset	Description					
	7:0	ORDER[7:0]	R/W		Expected Sleep Entry sequence order value for channel 8.  This sequence order value is compared with the SEQ_ENS_LOG[6] register assigned to the channel during the sequence triggered by SLEEP.					



## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for design purposes. Customers should validate and test their design implementation to confirm system functionality.

## **8.1 Application Information**

Modern SOC and FPGA devices typically have multiple power rails to provide power to the different blocks within the IC. Accurate voltage level and timing requirements are common and must be met in order to ensure proper operation of these devices. By utilizing TPS389006-Q1 along with a multichannel voltage sequencer, the power up and power down sequencing requirements as well as the core voltage requirements of the target SOC or FPGA device can be met. This design focuses on meeting the timing requirements for an SOC by using the TPS389006-Q1.

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## 8.2 Typical Application

### 8.2.1 Multichannel Sequencer and Monitor

A typical application for the TPS389006 is shown in Figure 8-1. TPS389006 is used to provide the proper voltage monitoring for the target SOC device. A multichannel voltage monitor TPS389006 is used to monitor the voltage rails as these rails power up and power down to make sure that the correct sequence occurs in both occasions. A safety microcontroller is also used to provide ACT, SLEEP, and I<sup>2</sup>C commands to the TPS389006 monitor the NIRQ pin for active faults. The ACT signal from the safety microcontroller determines when the TPS389006 enters into ACTIVE or IDLE states while the NIRQ pin of the TPS389006 acts as a latched interrupt pin that is set when a fault has occurred. The host microcontroller can clear the fault by writing 1 to the affected registers. The power rails for the safety microcontroller are not shown in Figure 8-1 for simplicity.

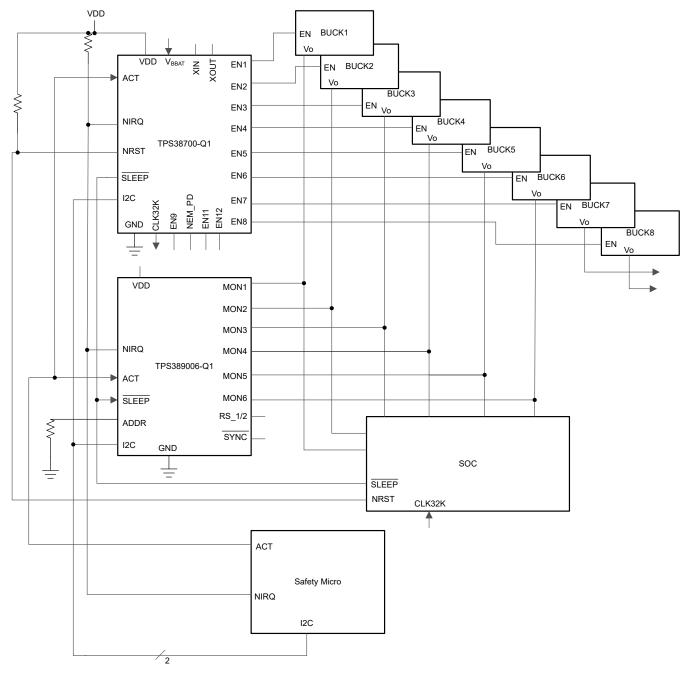


Figure 8-1. TPS389006 Voltage Monitor Design Block Diagram



## 8.2.2 Design Requirements

Six different voltage rails supplied by DC/DC converters need to be properly monitored in this design. All detected failures in sequencing will be reported via an external hardware interrupt signal. All detected failures will be logged in internal registers and be accessible to an external processor via I<sup>2</sup>C.

## 8.2.3 Detailed Design Procedure

TPS389006-Q1 device option comes preprogrammed with default values for over voltage, under voltage, expected sequences on power up and down. Please follow the design requirements outlined below.

- NIRQ pin requires a pull up resistor in the range of  $10k\Omega$  to  $100k\Omega$ .
- SDA and SCL lines require pull up resistors in the range of 10kΩ.
- The ACT pin is driven by an external safety microcontroller. When the ACT pin is driven high, the device enters into ACTIVE mode. When the ACT pin is driven low, the device enters into SLEEP mode.
- The safety microcontroller is used to clear fault interrupts reported through the NIRQ interrupt pin and the INT\_SCR1 and INT\_SCR2 registers. The interrupt flags can only be cleared by the host microcontroller with a write-1-to-clear operation; interrupt flags are not automatically cleared if the fault condition is no longer present.

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## 8.2.4 Application Curves

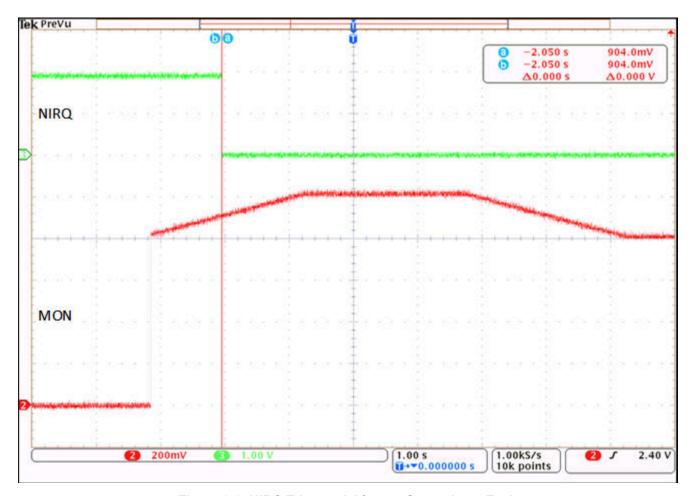


Figure 8-2. NIRQ Triggered After an Overvoltage Fault



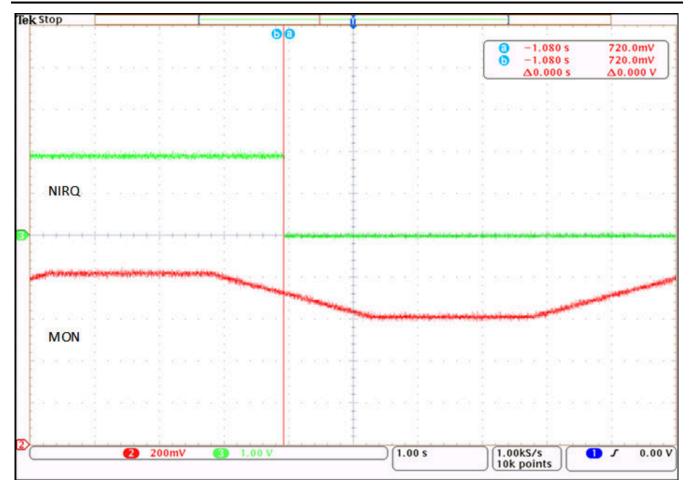


Figure 8-3. NIRQ Triggered After an Undervoltage Fault

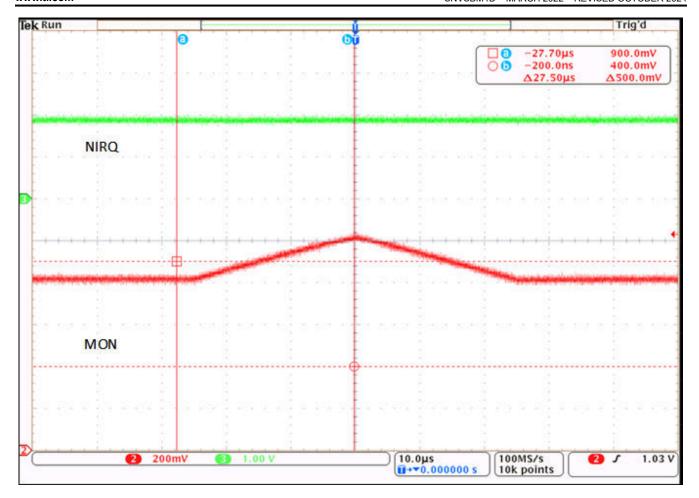


Figure 8-4. NIRQ Not Triggered on Overvoltage Fault with 51.2us OV Debounce Filter



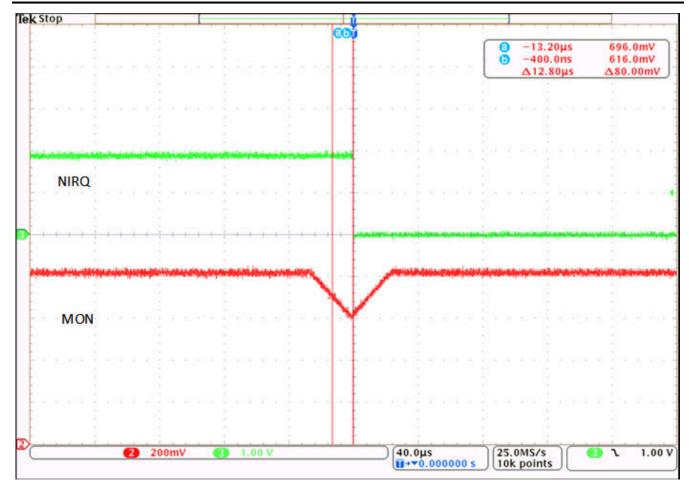


Figure 8-5. NIRQ Triggered on Undervoltage Fault with 12.8us UV Debounce Filter

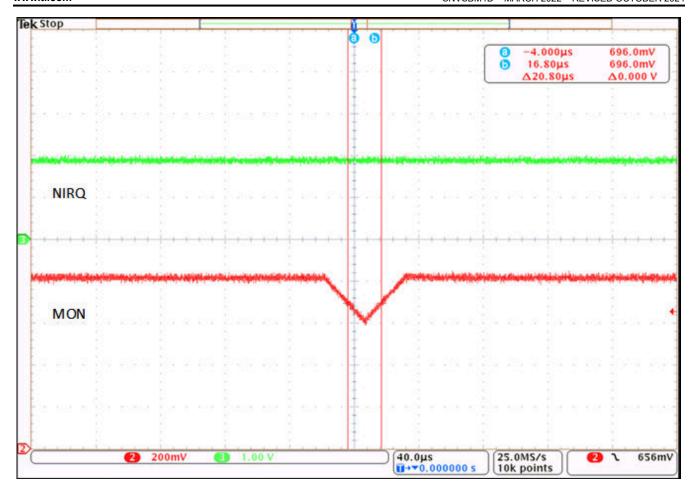


Figure 8-6. NIRQ Not Triggered on Undervoltage Fault with 25us UV Debounce Filter



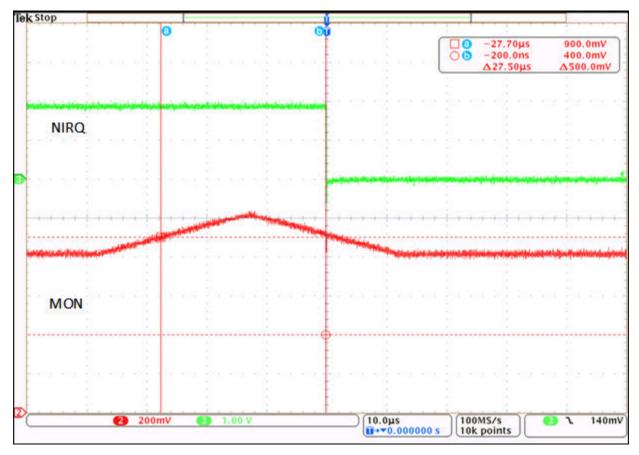


Figure 8-7. NIRQ Triggered on Overvoltage Fault with 25us OV Debounce Filter



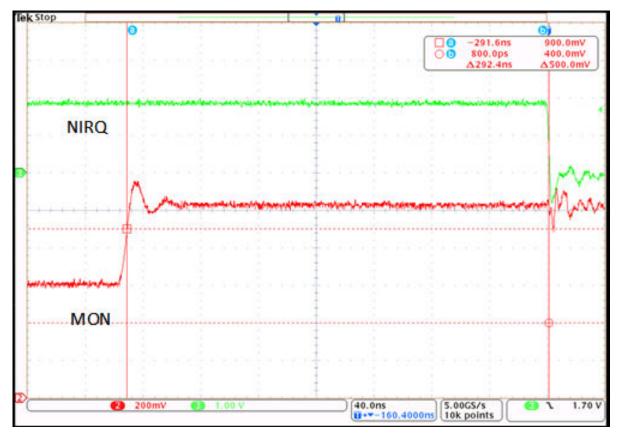


Figure 8-8. NIRQ Propagation Delay Resulting from Overvoltage Fault



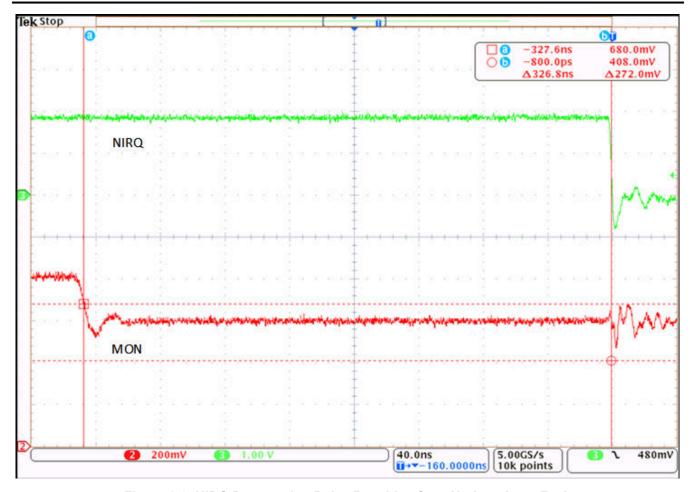


Figure 8-9. NIRQ Propagation Delay Resulting from Undervoltage Fault

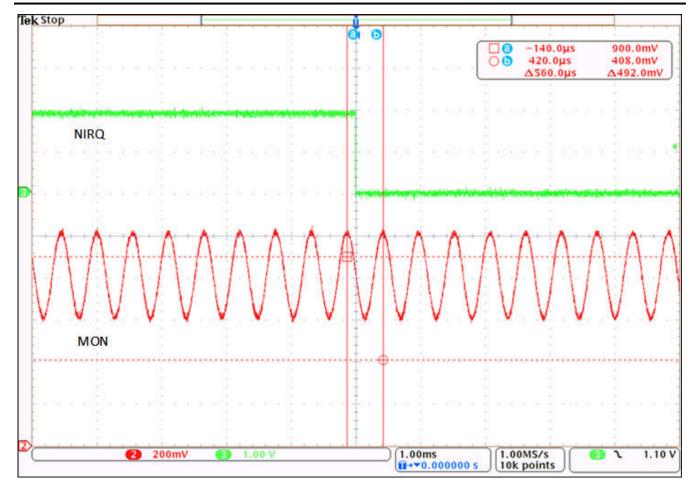


Figure 8-10. 1kHz Low Pass Filter Setting. NIRQ Triggered at 1.8kHz Signal with a 0.8V DC Component and 200mVp-p AC Signal. OV and UV Thresholds Set to 0.9V and 0.7V. Reduced the Frequency From 2kHz Until the NIRQ Pin Went Low.



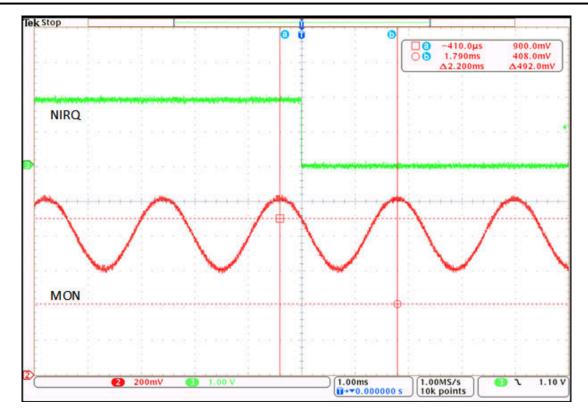


Figure 8-11. 250Hz Low Pass Filter setting. NIRQ Triggered at 455Hz Signal With a 0.8V DC Component and 200mVp-p AC Signal. OV and UV Thresholds Set to 0.9V and 0.7V. Reduced the Frequency From 500Hz Until the NIRQ Pin Went Low.

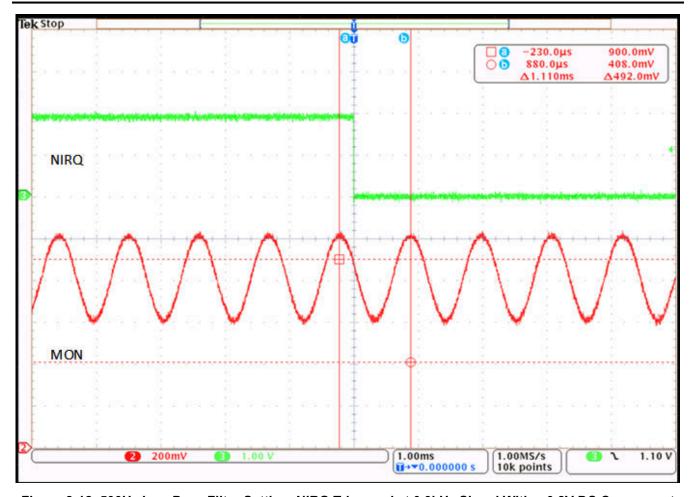


Figure 8-12. 500Hz Low Pass Filter Setting. NIRQ Triggered at 0.9kHz Signal With a 0.8V DC Component and 200mVp-p AC Signal. OV and UV Thresholds Set to 0.9V and 0.7V. Reduced the Frequency From 1kHz Until the NIRQ Pin Went Low.

### 8.3 Power Supply Recommendations

## 8.3.1 Power Supply Guidelines

This device is designed to operate from an input supply with a voltage range between 2.5V to 5.5V. The device has a 6V absolute maximum rating on the VDD pin. Good analog practice is to place a  $0.1\mu F$  to  $1\mu F$  capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the voltage supply providing power to VDD is susceptible to any large voltage transient that exceed maximum specifications, additional precautions must be taken. See SNVA849 for more information.

### 8.4 Layout

### 8.4.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.
- Avoid using long traces of voltage to the MON pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.
- If differential voltage sensing is required for MON1 and/or MON2, route RS\_1/2 pin to the point of measurement



• Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

## 8.4.2 Layout Example

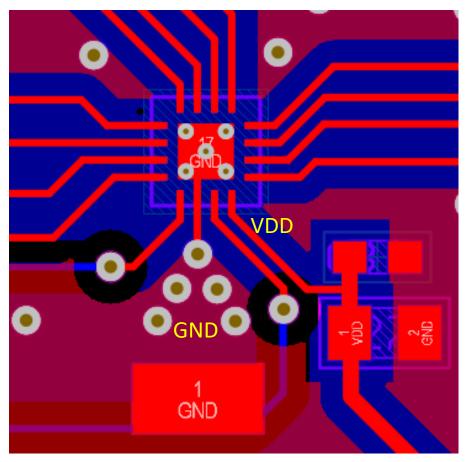


Figure 8-13. Recommended Layout



# **9 Device and Documentation Support**

## 9.1 Device Nomenclature

Table 9-1 Table 9-2 and Table 9-3 show how to decode the function of the device based on the part number.

## Table 9-1. Device Thresholds TPS389006-Q1,TPS389R06-Q1

ORDERING CODE	Thresholds	VMON1 (V)	VMON2 (V)	VMON3 (V)	VMON4 (V)	VMON5 (V)	VMON6 (V)
TPS389006ADJRTER	UV_HF/OV_HF	0.47/0.53	0.47/0.53	0.66/0.74	0.66/0.74	0.66/0.74	0.66/0.74
	UV_LF/OV_LF	0.5/0.7	0.5/0.7	0.5/0.7	0.5/0.7	0.5/0.7	0.5/0.7
TPS389006007RTER	UV_HF/OV_HF	1.4/2.1	1.4/2.1	1.4/2.1	1.4/2.1	1.4/2.1	1.4/2.1
	UV_LF/OV_LF	1.4/2.1	1.4/2.1	1.4/2.1	1.4/2.1	1.4/2.1	1.4/2.1
TPS389R06ADJRTER	UV_HF/OV_HF	0.705/0.795	0.705/0.795	0.705/0.795	0.705/0.795	3.1/3.5	4.7/5.3
Preview	UV_LF/OV_LF	0.705/0.795	0.705/0.795	0.705/0.795	0.705/0.795	3.1/3.5	4.7/5.3

## Table 9-2. Device Thresholds TPS389008-Q1

ORDERING CODE	Thresholds	VMON1 (V)	VMON2 (V)	VMON3 (V)	VMON4 (V)	VMON5 (V)	VMON6 (V)	VMON7 (V)	VMON8 (V)
TPS389008M6HRTER	UV_HF/OV_HF	0.83/0.91	1.68/1.92	1.68/1.92	0.81/0.91	0.70/0.80	1.005/1.09	0.46/0.535	1.68/1.92
Preview	UV_LF/OV_LF								
TPS389008M62RTER	UV_HF/OV_HF	0.705/0.80	0.805/0.90	1.05/1.18	1.13/1.27	0.70/0.80	1.035/1.165	3.1/3.5	2.24/2.56
Preview	UV_LF/OV_LF								
TPS389008M67RTER	UV_HF/OV_HF	0.775/0.825	1.165/1.235	0.775/0.825	1.165/1.235	0.815/0.865	1.165/1.235	1.74/1.86	4.74/5.26
Preview	UV_LF/OV_LF								
TPS389008M64RTER	UV_HF/OV_HF	0.755/0.845	0.5/1.0	1.05/1.18	0.80/0.90	1.68/1.92	0.755/0.845	1.68/1.92	1.05/1.15
Preview	UV_LF/OV_LF	1							
TPS389008M66RTER	UV_HF/OV_HF	1.03/1.155	4.7/5.3	1.13/1.27	1.12/1.25	0.755/0.845	3.1/3.5	1.03/1.155	4.74/5.26
Preview	UV_LF/OV_LF	1							

# **Table 9-3. Device Configuration Table**

ORDERING CODE	FUNCTIONS	SCALING	OV/UV DEBOUNCE	LF CUTOFF	I <sup>2</sup> C ADDRESS	BIST	SEQ TIMEOUT/ RESET DELAY	PEC <sup>(1)</sup>	I <sup>2</sup> C PULL-UP VOLTAGE (V)	ACT/SLEEP
TPS389006ADJRTER	Monitor LF/HF	1/1/1/1/1/1	102.4µsec	1kHz	Resistor strap	at POR	25ms/NA	Disable	3.3	Level
TPS389006007RTER	Monitor LF/HF	4/4/4/4/4	25.6µsec	1kH	Resistor Strap	At POR	100ms/NA	Disable	3.3	Level
TPS389R06ADJRTER Preview	Monitor LF/HF	1/1/1/1/4/4	51.2µsec	1kH	Resistor Strap	At POR	50ms/20ms	Disable	3.3	Level



**Table 9-3. Device Configuration Table (continued)** 

ORDERING CODE	FUNCTIONS	SCALING	OV/UV DEBOUNCE	LF CUTOFF	I <sup>2</sup> C ADDRESS	BIST	SEQ TIMEOUT/ RESET DELAY	PEC <sup>(1)</sup>	I <sup>2</sup> C PULL-UP VOLTAGE (V)	ACT/SLEEP	
TPS389008M6xRTER Preview	Monitor LF/HF	1 or 4 based on thresholds	51.2µsec	1kH	Resistor Strap	At POR	100ms/NA	Disable	3.3	Level	

## (1) For parts with PEC enabled:

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- a. PEC calculation is based on initializing to 0x00.
- b. In case of a PEC violation there needs to be a subsequent I<sup>2</sup>C transaction before NIRQ is asserted.
- c. If incorrect PEC device asserts NIRQ.
- d. If there is an extra byte after successfully writing the correct PEC byte, NIRQ is asserted and the write fails.

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## 9.2 Documentation Support

## 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.4 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

### 9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

#### 

Updated pinout and ordering code nomenclature	4
Added pinout and pin description for TPS389008-Q1 and TPS389R0-Q1	
<ul> <li>Updated Abs max for ACT,SLEEP,SCL,SDA from VDD+0.3V to 6V and added NRST to Abs ma</li> </ul>	
Recommended Operating Conditions	
Updated abs max to 6V from VDD+0.3	
Pin current max updated	8
Updated recommended operating max to 5.5V from VDD	8
Added electrical characteristics for NRST pin	9
Added electrical characteristic for NRST pin	
Added timing characteristics for NRST pin	
<ul> <li>Removed max numbers for t<sub>HD:DAT</sub> to confirm to I<sup>2</sup>C standard</li> </ul>	
NRST pin description added	



С	Changes from Revision A (March 2022) to Revision B (May 2023)	Page
•	Initial Public Release	1

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: TPS389006-Q1 TPS389R0-Q1



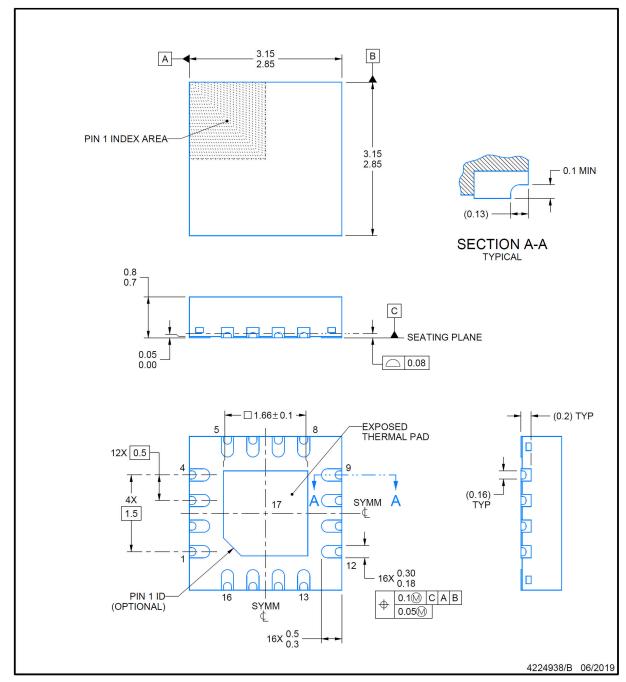
# **RTE0016K**



# **PACKAGE OUTLINE**

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
   This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

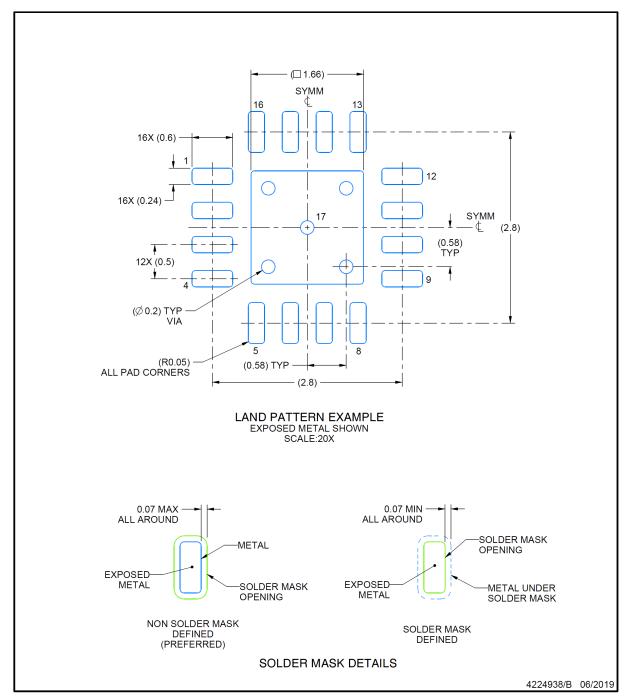


## **EXAMPLE BOARD LAYOUT**

## **RTE0016K**

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

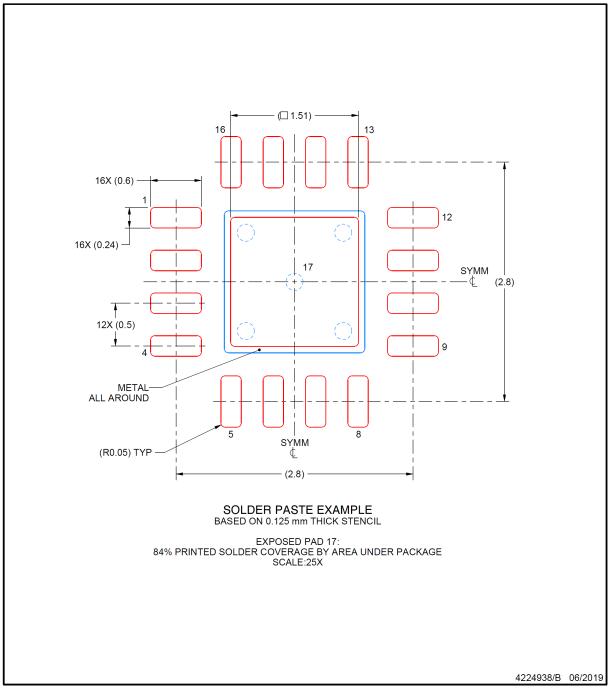


# **EXAMPLE STENCIL DESIGN**

# **RTE0016K**

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations. www.ti.com 25-Nov-2025

### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
PPS389R06ADJRTERQ1	Active	Preproduction	WQFN (RTE)   16	3000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
PPS389R06ADJRTERQ1.A	Active	Preproduction	WQFN (RTE)   16	3000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS389006004RTERQ1	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6004Q
TPS389006004RTERQ1.A	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6004Q
TPS38900603NRTERQ1	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0603Q
TPS38900603NRTERQ1.A	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	0603Q
TPS389006ADJRTERQ1	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6ADJQ
TPS389006ADJRTERQ1.A	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6ADJQ
TPS389008M64RTERQ1	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TM64Q
TPS389008M67RTERQ1	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TM67Q
TPS389008M68RTERQ1	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TM68Q
TPS389008M69RTERQ1	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TM69Q
TPS389008M70RTERQ1	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TM70Q

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF TPS389006-Q1:

Catalog: TPS389006

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product



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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS389006004RTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS38900603NRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS389006ADJRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS389008M64RTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS389008M67RTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS389008M68RTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS389008M69RTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS389008M70RTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS389006004RTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS38900603NRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS389006ADJRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS389008M64RTERQ1	WQFN	RTE	16	3000	360.0	360.0	36.0
TPS389008M67RTERQ1	WQFN	RTE	16	3000	360.0	360.0	36.0
TPS389008M68RTERQ1	WQFN	RTE	16	3000	360.0	360.0	36.0
TPS389008M69RTERQ1	WQFN	RTE	16	3000	360.0	360.0	36.0
TPS389008M70RTERQ1	WQFN	RTE	16	3000	360.0	360.0	36.0

3 x 3, 0.5 mm pitch

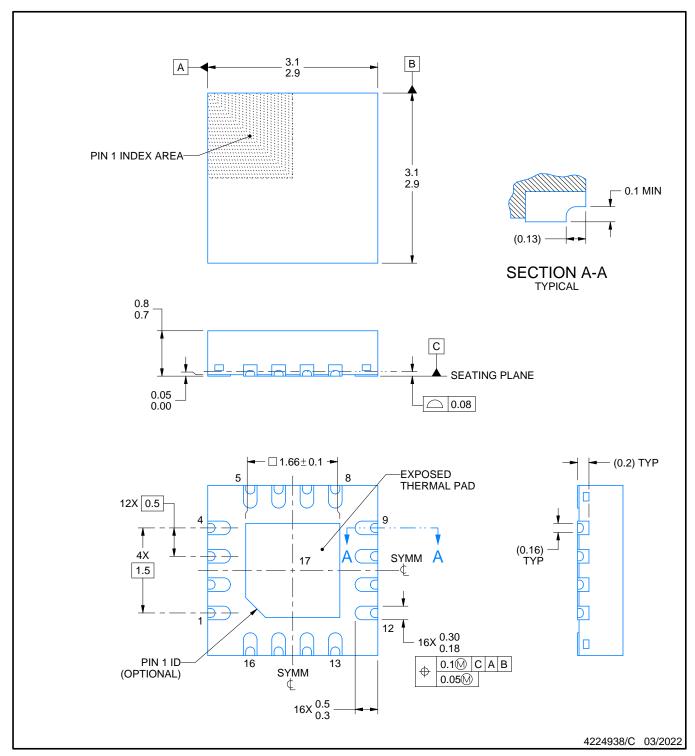
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC QUAD FLATPACK - NO LEAD

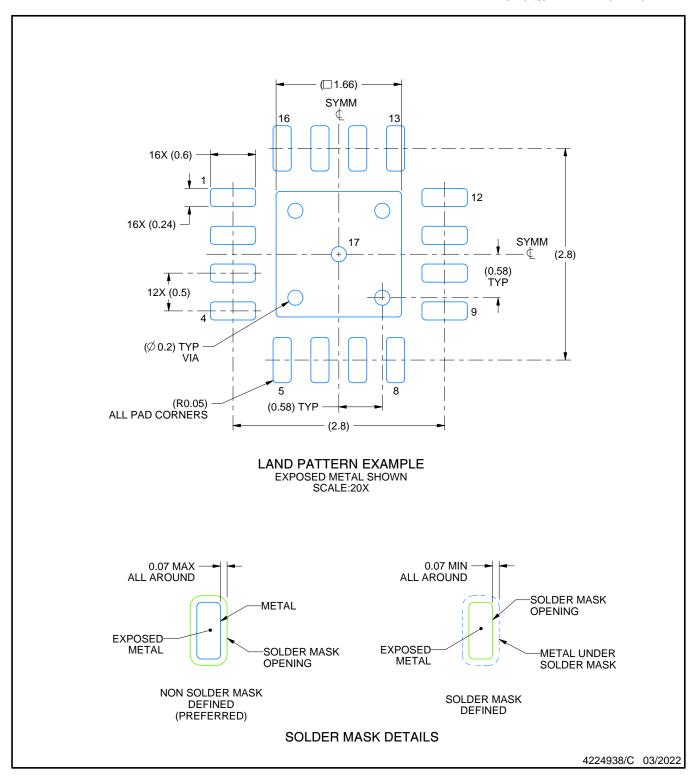


### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

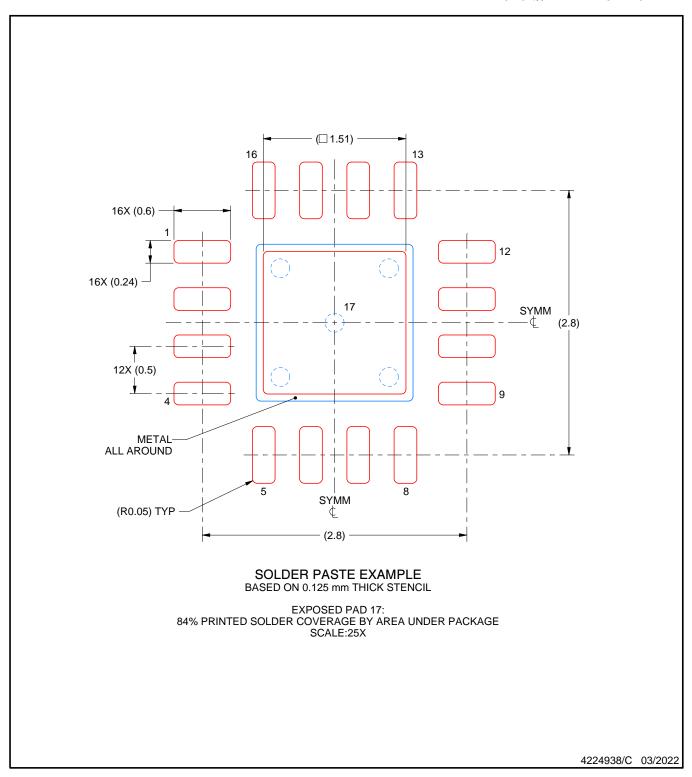


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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