Support &



# **TPS3850 Precision Voltage Supervisor with Programmable Window Watchdog Timer**

Technical

documentation

#### 1 Features

- Input voltage range: VDD = 1.6 V to 6.5 V
- 0.8% Voltage threshold accuracy
- Low supply current:  $I_{DD} = 10 \mu A$  (typical)
- User-programmable watchdog timeout
- User-programmable reset delay
- · Factory-programmed precision watchdog and reset timers
- Open-drain outputs
- Precision over- and undervoltage monitoring:
  - Supports common rails from 0.9 V to 5.0 V
  - ±4% and ±7% Fault windows available
  - 0.5% Hysteresis
- Watchdog disable feature
- Available in a small 3-mm × 3-mm, 10-Pin VSON package
- Junction operating temperature range: -40°C to +125°C

# 2 Applications

- Ultrasound scanner
- Storage area network
- Active Antenna System mMIMO (AAS)
- Robot servo drive
- Infusion pump
- **HVAC** controller

# 3 Description

🥦 Design & development

The TPS3850 combines a precision voltage supervisor with a programmable window watchdog timer. The TPS3850 window comparator achieves accuracy (-40°C to +125°C) for both overvoltage  $(V_{IT+(OV)})$  and undervoltage  $(V_{IT-(UV)})$ thresholds on the SENSE pin. The TPS3850 also includes accurate hysteresis on both thresholds, making the device ideal for use with tight tolerance systems. The supervisor RESET delay can be set by factory-programmed default delay settings, or programmed by an external capacitor. The factoryprogrammed RESET delay features a 9.5% accuracy, high-precision delay timing.

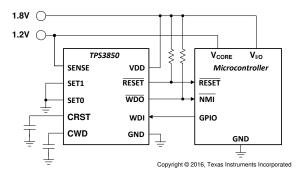
The TPS3850 includes a programmable window watchdog timer for a wide variety of applications. The dedicated watchdog output ( WDO) enables increased resolution to help determine the nature of fault conditions. The window watchdog timeouts can be set by factory-programmed default delay settings, or programmed by an external capacitor. The watchdog can be disabled via logic pins to avoid undesired watchdog timeouts during the development process.

The TPS3850 is available in a small 3.00-mm × 3.00-mm, 10-pin VSON package.

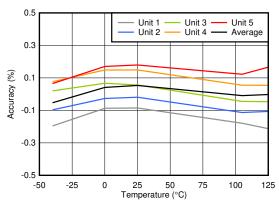
#### **Device Information**

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TPS3850	VSON (10)	3.00 mm × 3.00 mm

For all available packages, see the orderable addendum at the end of the data sheet.



**Fully Integrated Microcontroller Supervisory** Circuit



Overvoltage Threshold (V<sub>IT+(OV)</sub>) Accuracy vs **Temperature** 



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# **4 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision A (November 2016) to Revision B (September 2021)	Page
•	Updated the numbering format for tables, figures, and cross-references throughout the document	1
•	Removed "±15% Accurate WDT and RST Delays"	1
•	Updated Applications to include link to the website	1
•	Added "on the SENSE pin"	
•	Changed V <sub>ESD</sub> values to ±4000 V and ±1000 V	5
•	Changed I <sub>CWD</sub> min and max spec	
•	Changed V <sub>CWD</sub> min and max spec	6
•	Added a footnote to for t <sub>INIT</sub>	<mark>7</mark>
•	Changed minimum and maximum specifications of 2nd, 5th, 6th, and 8th rows of t <sub>WDL</sub> parameter	<mark>7</mark>
•	Changed minimum and maximum specifications of 2nd and last rows of two parameter	
•	Added new section "Disabling the Watchdog Timer When Using the CRST Capacitor"	
•	Changed 0.000381 to 0.000324 and 0.000438 in Equation 4 and Equation 5, respectively	24
•	Changed minimum and maximum specifications in 100 pF and 1 nF rows of Reset Delay Time for Com	
	Ideal Capacitor Values table	24
•	Changed minimum and maximum specifications for NC SETx 01 setting for both upper and lower watch	ıdog
	boundaries, 10 k $\Omega$ to VDD SETx 00 and 01 settings for lower watchdog boundary, and 10 k $\Omega$ to VDD S	ETx
	11 setting for both upper and lower watchdog boundaries in Factory-Programmed Watchdog Timing tal	
•	Changed minimum and maximum limits on two and added explanation.	25
•	Changed 0.000381 to 0.000324 in Equation 11	
•	Changed description of factory-programmed timing options and values of two two and two two in Sett	
	the Watchdog Window section	
•	Changed 0.85 to 0.905 in Equation 14	33
•	Changed Equation 17 and Equation 18 so that I <sub>SENSE</sub> is no longer in the denominator	34
C	hanges from Revision * (October 2016) to Revision A (November 2016)	Page
•	Changed units in I <sub>SENSE</sub> parameter and footnote 1 in <i>Electrical Characteristics</i> table	6
•	Added correct operation state to Figure 2	
•	Changed Figure 3 so the SET pins do not bring the watchdog into the disabled state before going to the	e 1:2
	ratio	<b>7</b>
•	Changed Figure 11 so it no longer has VDD and Vorsion tied together	11



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•	Changed Figure 26 so it no longer goes through watchdog disabled	18
	Added correct operation state to Figure 27	
	Changed RESET to WDO in description of WDO assertion in WDO Functionality section	

# **5 Pin Configuration and Functions**

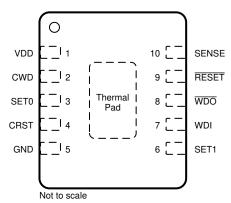


Figure 5-1. DRC Package: TPS3850 3-mm × 3-mm VSON-10 Top View

**Table 5-1. Pin Functions** 

	PIN		DECODINE
NAME	NO.	I/O	DESCRIPTION
CRST	4	I	Programmable reset timeout pin. Connect a capacitor between this pin and GND to program the reset timeout period. This pin can also be connected by a $10-k\Omega$ pullup resistor to VDD, or left unconnected (NC) for various factory programmed reset timeout options; see the <i>Section 8.1.1</i> section. When using an external capacitor, use Equation 3 to determine the reset timeout.
CWD	2	I	Programmable watchdog timeout input. Watchdog timeout is set by connecting a capacitor between this pin and ground. Furthermore, this pin can also be connected by a 10-kΩ resistor to VDD, or leaving unconnected (NC) further enables the selection of the preset watchdog timeouts; see the <i>Section 6.6</i> table. When using a capacitor, the TPS3850 determines the window watchdog upper boundary with Equation 6. The lower watchdog boundary is set by the SET pins, see Table 8-5 and the <i>Section 8.1.2</i> section for additional information.
GND	5	_	Ground pin
RESET	9	0	Reset output. Connect $\overline{RESET}$ using a 1-k $\Omega$ to 100-k $\Omega$ resistor to VDD. $\overline{RESET}$ goes low when the voltage at the SENSE pin goes below the undervoltage threshold (V <sub>IT-(UV)</sub> ) or above the overvoltage threshold (V <sub>IT+(OV)</sub> ). When the voltage level at the SENSE pin is within the normal operating range, the $\overline{RESET}$ timeout counter starts. At timer completion, $\overline{RESET}$ goes high. During startup, the state of $\overline{RESET}$ is undefined below the specified power-on reset voltage (V <sub>POR</sub> ). Above V <sub>POR</sub> , $\overline{RESET}$ goes low and remains low until the monitored voltage is within the correct operating range (between V <sub>IT-(UV)</sub> and V <sub>IT(+OV)</sub> ) and the $\overline{RESET}$ timeout is complete.
SENSE	10	I	SENSE input to monitor voltage rail. Connect this pin to the supply rail that must be monitored.
SET0	3	I	Logic input. SET0, SET1, and CWD select the watchdog window ratios, timeouts, and disable the watchdog; see the <i>Section 6.6</i> table.
SET1	6	I	Logic input. SET0, SET1, and CWD select the watchdog window ratios, timeouts, and disable the watchdog; see the <i>Section 6.6</i> table.
VDD	1	ı	Supply voltage pin. For noisy systems, connecting a 0.1-µF bypass capacitor is recommended.
WDI	7	ı	Watchdog input. A falling transition (edge) must occur at this pin between the lower $(t_{WDL(max)})$ and upper $(t_{WDU(min)})$ window boundaries in order for $\overline{WDO}$ to not assert. When the watchdog is not in use, the SET pins can be used to disable the watchdog. The input at WDI is ignored when $\overline{RESET}$ or $\overline{WDO}$ are low (asserted) and also when the watchdog is disabled. If the watchdog is disabled, then WDI cannot be left unconnected and must be driven to either VDD or GND.
WDO	8	0	Watchdog output. Connect $\overline{WDO}$ with a 1-k $\Omega$ to 100-k $\Omega$ resistor to VDD. $\overline{WDO}$ goes low (asserts) when a watchdog timeout occurs. $\overline{WDO}$ only asserts when $\overline{RESET}$ is high. When a watchdog timeout occurs, $\overline{WDO}$ goes low (asserts) for the set $\overline{RESET}$ timeout delay (t <sub>RST</sub> ). When $\overline{RESET}$ goes low, $\overline{WDO}$ is in a high-impedance state.
Thermal pa	ad	_	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

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# **6 Specifications**

# **6.1 Absolute Maximum Ratings**

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	VDD	-0.3	7	V
Output voltage range	RESET, WDO	-0.3	7	V
Voltago rangos	SET0, SET1, WDI, SENSE	-0.3	7	V
Voltage ranges	CWD, CRST	-0.3	VDD + 0.3 <sup>(3)</sup>	V
Output pin current	RESET, WDO		±20	mA
Input current (all pins)	·		±20	mA
Continuous total power dissipation		See S	Section 6.4	
	Operating junction, T <sub>J</sub> <sup>(2)</sup>	-40	150	
Temperature	Operating free-air temperature, T <sub>A</sub> <sup>(2)</sup>	-40	150	°C
	Storage, T <sub>stg</sub>	-65	150	

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

				VALUE	UNIT
V		Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
\ \ \ \ \ \ (E	SD)	Liectiostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply pin voltage	1.6		6.5	V
V <sub>SENSE</sub>	Input pin voltage	0		6.5	V
V <sub>SET0</sub>	SET0 pin voltage	0		6.5	V
V <sub>SET1</sub>	SET1 pin voltage	0		6.5	V
C <sub>CRST</sub>	RESET delay capacitor	0.1(1)		1000(1)	nF
CRST	Pullup resistor to VDD	9	10	11	kΩ
C <sub>CWD</sub>	Watchdog timing capacitor	0.1(2)		1000(2)	nF
CWD	Pullup resistor to VDD	9	10	11	kΩ
R <sub>PU</sub>	Pullup resistor, RESET and WDO	1	10	100	kΩ
I <sub>RST</sub>	RESET pin current			10	mA
I <sub>WDO</sub>	Watchdog output current			10	mA
TJ	Junction Temperature	-40		125	°C

<sup>(1)</sup> Using a C<sub>CRST</sub> capacitor of 0.1 nF or 1000 nF gives a reset delay of 703 μs or 3.22 seconds, respectively.

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<sup>(2)</sup>  $T_J = T_A$  as a result of the low dissipated power in this device.

<sup>(3)</sup> The absolute maximum rating is V<sub>DD</sub> + 0.3 V or 7.0 V, whichever is smaller.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

<sup>(2)</sup> Using a C<sub>CWD</sub> capacitor of 0.1 nF or 1000 nF gives a t<sub>WDU(typ)</sub> of 62.74 ms or 77.45 seconds, respectively.



### **6.4 Thermal Information**

		TPS3850	
	THERMAL METRIC <sup>(1)</sup>	DRC (VSON)	UNIT
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.3	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	59.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	26.1	°C/W
ΨЈТ	Junction-to-top characterization parameter	1.7	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	26.0	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	9.7	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application

### 6.5 Electrical Characteristics

at 1.6 V  $\leq$  V<sub>DD</sub>  $\leq$  6.5 V over the operating temperature range of  $-40^{\circ}$ C  $\leq$  T<sub>J</sub>  $\leq$  +125 $^{\circ}$ C (unless otherwise noted); the open-drain pullup resistors are 10 k $\Omega$  for each output; typical values are at T<sub>J</sub> = 25 $^{\circ}$ C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL C	HARACTERISTICS			'	-	
V <sub>DD</sub> (1) (2) (3)	Supply voltage		1.6		6.5	V
I <sub>DD</sub>	Supply current			10	19	μA
RESET FUN	CTION				,	
V <sub>POR</sub> (2)	Power-on reset voltage	I <sub>RESET</sub> = 15 μA, V <sub>OL(MAX)</sub> = 0.25 V			0.8	V
V <sub>UVLO</sub> (1)	Undervoltage lockout voltage			1.35		V
V <sub>IT+(OV)</sub>	Overvoltage SENSE threshold accuracy, entering RESET		V <sub>IT+(nom)</sub> -0.8%		V <sub>IT+(nom)</sub> +0.8%	
V <sub>IT-(UV)</sub>	Undervoltage SENSE threshold accuracy, entering RESET		V <sub>IT-(nom)</sub> -0.8%		V <sub>IT-(nom)</sub> +0.8%	
V <sub>IT(ADJ)</sub>	Falling SENSE threshold voltage, adjustable version only		0.3968	0.4	0.4032	V
V <sub>HYST</sub>	Hysteresis voltage		0.2%	0.5%	0.8%	
I <sub>CRST</sub>	CRST pin charge current	CRST = 0.5 V	347	375	403	nA
V <sub>CRST</sub>	CRST pin threshold voltage		1.196	1.21	1.224	V
WINDOW W	ATCHDOG FUNCTION					
I <sub>CWD</sub>	CWD pin charge current	CWD = 0.5 V	347	375	403	nA
V <sub>CWD</sub>	CWD pin threshold voltage		1.196	1.21	1.224	V
V <sub>OL</sub>	RESET, WDO output low	VDD = 5 V, I <sub>SINK</sub> = 3 mA			0.4	V
I <sub>D</sub>	RESET, WDO output leakage current	VDD = 1.6 V, V <sub>RESET</sub> , = V <sub>WDO</sub> = 6.5 V			1	μA
V <sub>IL</sub>	Low-level input voltage (SET0, SET1)				0.25	V
V <sub>IH</sub>	High-level input voltage (SET0, SET1)		0.8			V
V <sub>IL(WDI)</sub>	Low-level input voltage (WDI)				0.3 × V <sub>DD</sub>	V
V <sub>IH(WDI)</sub>	High-level input voltage (WDI)		0.8 × V <sub>DD</sub>			V
	SENSE pin idle current	TPS3850Xyy(y), V <sub>SENSE</sub> = 5.0 V, VDD = 3.3 V		2.1	2.5	μA
ISENSE	SENSE più luie current	TPS3850H01 only, V <sub>SENSE</sub> = 5.0 V, VDD = 3.3 V	-50		50	nA

- When  $V_{DD}$  falls below  $V_{UVLO}$ ,  $\overline{RESET}$  is driven low. When  $V_{DD}$  falls below  $V_{POR}$ ,  $\overline{RESET}$  and  $\overline{WDO}$  are undefined.
- (3) During power-on, V<sub>DD</sub> must be a minimum 1.6 V for at least 300 µs before the output corresponds to the SENSE voltage.



# 6.6 Timing Requirements

			MIN	TYP	MAX	UNIT
GENERA	L				-	
t <sub>INIT</sub>	CWD, CRST pin evaluation	period <sup>(1)</sup>		381		μs
t <sub>SET</sub>	Time required between chan	ging SET0 and SET1 pins		500		μs
	SET0, SET1 pin setup time			1		μs
	Startup delay <sup>(2)</sup>			300		μs
RESET F	UNCTION				1	
	Deset time sout a sais d	CRST = NC	170	200	230	ms
<sup>L</sup> RST	Reset timeout period	CRST = 10 kΩ to VDD	8.5	10	11.5	ms
	V to DECET deleve	VDD = 5 V, V <sub>SENSE</sub> = V <sub>IT+(OV)</sub> + 2.5%		35		
<sup>L</sup> RST-DEL	V <sub>SENSE</sub> to RESET delay	VDD = 5 V, V <sub>SENSE</sub> = V <sub>IT-(UV)</sub> - 2.5%		17		μs
WINDOW	WATCHDOG FUNCTION				1	
	Window watchdog ratio of	CWD = programmable, SET0 = 0, SET1 = 0 <sup>(3)</sup>		1/8		
WD ratio	lower boundary to upper boundary	CWD = programmable, SET0 = 1, SET1 = 1 <sup>(3)</sup>		1/2		
		CWD = programmable, SET0 = 0, SET1 = 1 <sup>(3)</sup> (4)		3/4		
	Window watchdog lower	CWD = NC, SET0 = 0, SET1 = 0	19.1	22.5	25.9	ms
		CWD = NC, SET0 = 0, SET1 = 1	1.48	1.85	2.22	ms
		CWD = NC, SET0 = 1, SET1 = 0	Watchdog disabled		ed	
		CWD = NC, SET0 = 1, SET1 = 1	680	800	920	ms
t <sub>WDL</sub>	boundary	CWD = 10 k $\Omega$ to VDD, SET0 = 0, SET1 = 0	7.65	9.0	10.35	ms
		CWD = 10 k $\Omega$ to VDD, SET0 = 0, SET1 = 1	7.65 9.0 1		10.35	ms
		CWD = 10 k $\Omega$ to VDD, SET0 = 1, SET1 = 0	Watchdog disabled		ed	
		CWD = 10 k $\Omega$ to VDD, SET0 = 1, SET1 = 1	1.48	1.85	2.22	ms
		CWD = NC, SET0 = 0, SET1 = 0	46.8	55.0	63.3	ms
		CWD = NC, SET0 = 0, SET1 = 1	23.375	27.5	31.625	ms
		CWD = NC, SET0 = 1, SET1 = 0	Watch	dog disable	ed	
	Window watchdog upper	CWD = NC, SET0 = 1, SET1 = 1	1360	1600	1840	ms
rMDU	boundary	CWD = 10 k $\Omega$ to VDD, SET0 = 0, SET1 = 0	92.7	109.0	125.4	ms
		CWD = 10 k $\Omega$ to VDD, SET0 = 0, SET1 = 1	165.8	195.0	224.3	ms
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 0	Watch	dog disable	ed	
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 1	9.35	11.0	12.65	ms
t <sub>WD-setup</sub>	Setup time required for device	e to respond to changes on WDI after being enabled	d to changes on WDI after being enabled 150			μs
·	Minimum WDI pulse duration	1		50		ns
t <sub>WD-del</sub>	WDI to WDO delay			50		ns

<sup>(1)</sup> Please refer to Section 8.1.1.2

During power-on,  $V_{DD}$  must be a minimum 1.6 V for at least 300 µs before the output corresponds to the SENSE voltage. 0 refers to  $V_{SET} \le V_{IL}$ , 1 refers to  $V_{SET} \ge V_{IH}$ . If this watchdog ratio is used, then  $t_{WDL(max)}$  can overlap  $t_{WDU(min)}$ . (2) (3) (4)



# **6.7 Timing Diagrams**

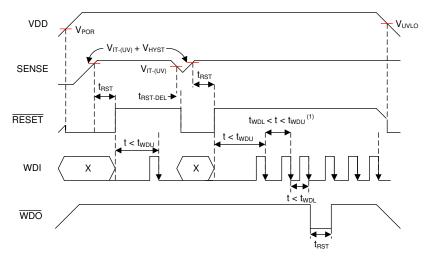


Figure 6-1. Timing Diagram

A. See Figure 6-2 for WDI timing requirements.



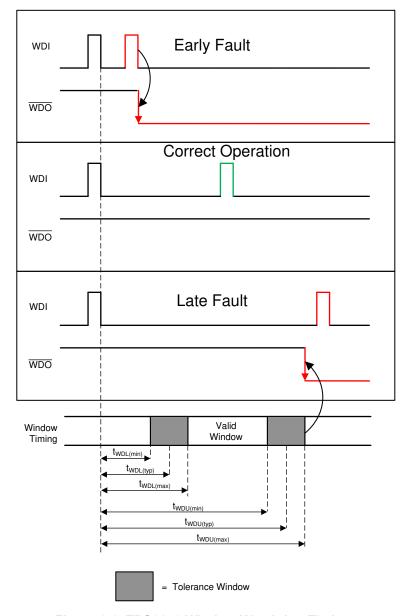


Figure 6-2. TPS3850 Window Watchdog Timing



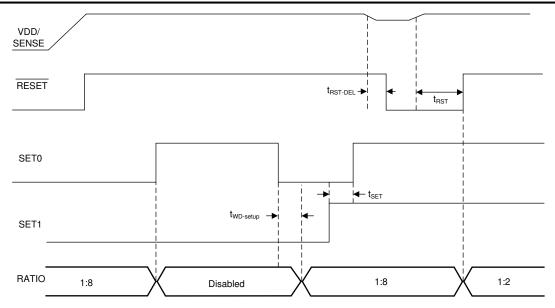
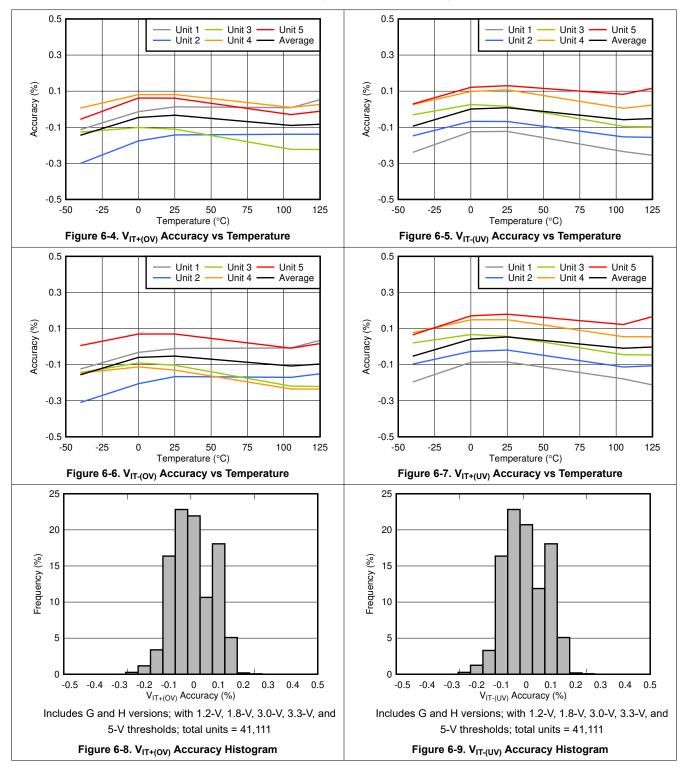


Figure 6-3. Changing SET0 and SET1 Pins

## **6.8 Typical Characteristics**

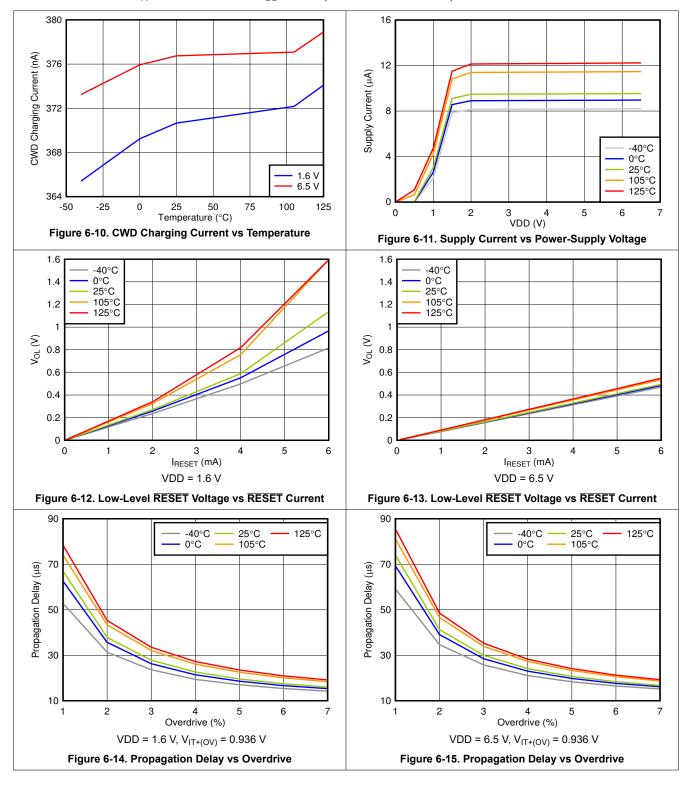
all curves are taken at T<sub>A</sub> = 25°C with 1.6 V ≤ V<sub>DD</sub> ≤ 6.5 V (unless otherwise noted)





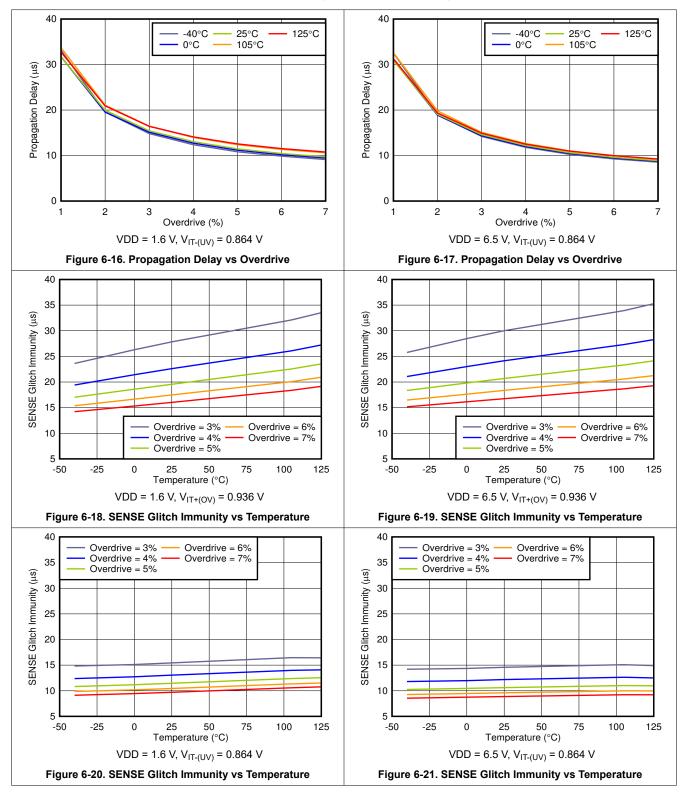
# **6.8 Typical Characteristics (continued)**

all curves are taken at  $T_A$  = 25°C with 1.6 V  $\leq$  V<sub>DD</sub>  $\leq$  6.5 V (unless otherwise noted)



# **6.8 Typical Characteristics (continued)**

all curves are taken at T<sub>A</sub> = 25°C with 1.6 V ≤ V<sub>DD</sub> ≤ 6.5 V (unless otherwise noted)



# 7 Detailed Description

# 7.1 Overview

The TPS3850 is a high-accuracy voltage supervisor with an integrated watchdog timer. This device includes a precision voltage supervisor with both overvoltage ( $V_{\text{IT+(OV)}}$ ) and undervoltage ( $V_{\text{IT-(UV)}}$ ) thresholds that achieve 0.8% accuracy over the specified temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . In addition, the TPS3850 includes accurate hysteresis on both thresholds, making the device ideal for use with tight tolerance systems where voltage supervisors must ensure a  $\overline{\text{RESET}}$  before the minimum and maximum supply tolerance of the microprocessor or system-on-a-chip (SoC) is reached.

# 7.2 Functional Block Diagrams

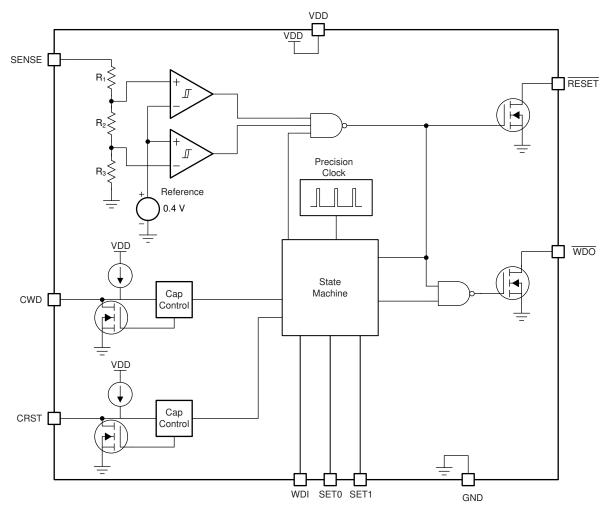


Figure 7-1. Fixed Version Block Diagram

 $R_{TOTAL}$  =  $R_1$  +  $R_2$  +  $R_3$  = 4.5  $M\Omega$ .



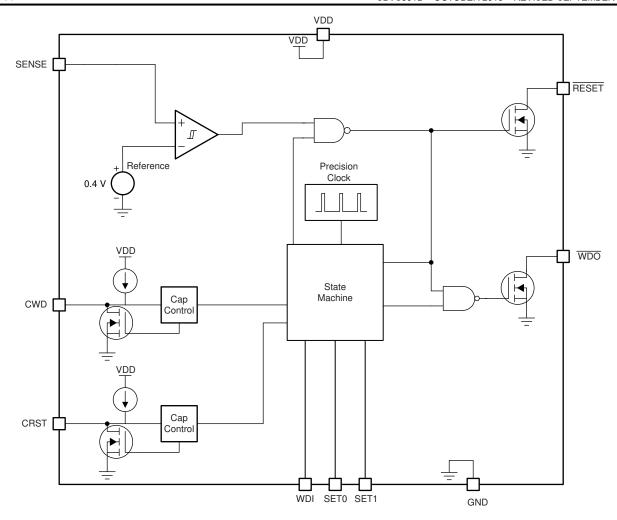


Figure 7-2. Adjustable Version Block Diagram

# 7.3 Feature Description

### 7.3.1 CRST

The CRST pin provides the user the functionality of both high-precision, factory-programmed, reset delay timing options and user-programmable, reset delay timing. The CRST pin can be pulled up to VDD through a resistor, have an external capacitor to ground, or can be left unconnected. The configuration of the CRST pin is re-evaluated by the device every time the voltage on the SENSE line enters the valid window ( $V_{IT+(UV)} < V_{SENSE} < V_{IT-(OV)}$ ). The pin evaluation is controlled by an internal state machine that determines which option is connected to the CRST pin. The sequence of events takes 381 µs ( $t_{INIT}$ ) to determine if the CRST pin is left unconnected, pulled up through a resistor, or connected to a capacitor. If the CRST pin is being pulled up to VDD, then a 10-k $\Omega$  pullup resistor is required.

### **7.3.2 RESET**

The  $\overline{\text{RESET}}$  pin features a programmable reset delay time that can be adjusted from 703 µs to 3.22 seconds when using adjustable capacitor timing.  $\overline{\text{RESET}}$  is an open-drain output that should be pulled up through a 1-k $\Omega$  to 100-k $\Omega$  pullup resistor. When  $V_{DD}$  is above  $V_{DD}$  (min),  $\overline{\text{RESET}}$  remains high (not asserted) when the SENSE voltage is between the positive threshold  $(V_{IT+(OV)})$  and the negative threshold  $(V_{IT-(UV)})$ . If SENSE falls below  $V_{IT-(UV)}$  or rises above  $V_{IT+(OV)}$ , then  $\overline{\text{RESET}}$  is asserted, driving the  $\overline{\text{RESET}}$  pin to a low-impedance state. When SENSE comes back into the valid window, a  $\overline{\text{RESET}}$  delay circuit is enabled that holds  $\overline{\text{RESET}}$  low for a specified reset delay period ( $t_{RST}$ ). This  $t_{RST}$  period is determined by what is connected to the CRST pin; see Figure 8-1. When the reset delay has elapsed, the  $\overline{\text{RESET}}$  pin goes to a high-impedance state and uses a pullup resistor to hold  $\overline{\text{RESET}}$  high. The pullup resistor must be connected to the proper voltage rail

to allow other devices to be connected at the correct interface voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by output logic low voltage ( $V_{OL}$ ), capacitive loading, and leakage current ( $I_D$ ); see the *Section 8.1.1* section for more information.

#### 7.3.3 Over- and Undervoltage Fault Detection

The TPS3850 features both overvoltage detection and undervoltage detection. This detection is achieved through the combination of two comparators with a precision voltage reference and a trimmed resistor divider (fixed versions only). The SENSE pin is used to monitor the critical voltage rail; this configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Both comparators also include built-in hysteresis that provides some noise immunity and ensures stable operation. If the voltage on the SENSE pin drops below  $V_{\text{IT-(UV)}}$ , then  $\overline{\text{RESET}}$  is asserted (driven low). When the voltage on the SENSE pin is between the positive and negative threshold voltages,  $\overline{\text{RESET}}$  deasserts after the user-defined  $\overline{\text{RESET}}$  delay time, as shown in Figure 7-3.

The SENSE input can vary from GND to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, for noisy applications, good analog-design practice is to place a 1-nF to 10-nF bypass capacitor at the SENSE pin to reduce sensitivity to transient voltages on the monitored signal.

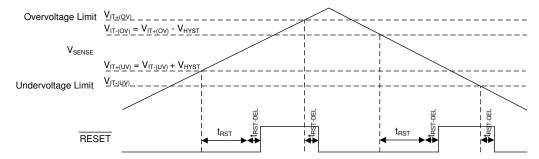


Figure 7-3. Window Comparator Timing Diagram

### 7.3.4 Adjustable Operation Using the TPS3850H01

The adjustable version (TPS3850H01) can be used to monitor any voltage rail down to 0.4 V using the circuit illustrated in Figure 7-4. When using the TPS3850H01, the device does not function as a window comparator; instead, the device only monitors the undervoltage threshold. To monitor a user-defined voltage, the target threshold voltage for the monitored supply  $(V_{MON})$  and the resistor divider values can be calculated by using Equation 1 and Equation 2, respectively:

$$V_{MON} = V_{IT(ADJ)} \times \left(1 + \frac{R_1}{R_2}\right) \tag{1}$$

Equation 1 can be used to calculate either the negative threshold or the positive threshold by replacing  $V_{ITx}$  with either  $V_{ITN}$  or  $V_{ITN} + V_{HYST}$ , respectively.

$$R_{TOTAL} = R_1 + R_2 \tag{2}$$

Large resistor values minimize current consumption; however, the input bias current of the device degrades accuracy if the current through the resistors is too low. Therefore, choosing an  $R_{TOTAL}$  value so that the current through the resistor divider is at least 100 times larger than the maximum SENSE pin current ( $I_{SENSE}$ ) ensures a good degree of accuracy; see the  $I_Q$  vs Accuracy Tradeoff In Designing Resistor Divider Input To A Voltage Supervisor (SLVA450) application report for more details on sizing input resistors.

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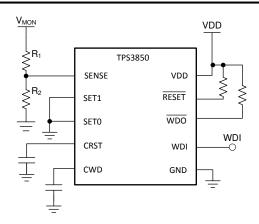


Figure 7-4. Adjustable Voltage Monitor

# 7.3.5 Window Watchdog

#### 7.3.5.1 SET0 and SET1

When changing the SET0 or SET1 pins, there are two cases to consider: enabling and disabling the watchdog, and changing the SET0 or SET1 pins when the watchdog is enabled. In case 1 where the watchdog is being enabled or disabled, the changes take effect immediately. However, in case 2, a RESET event must occur in order for the changes to take place.

### 7.3.5.1.1 Enabling the Window Watchdog

The TPS3850 features the ability to enable and disable the watchdog timer. This feature allows the user to start with the watchdog timer disabled and then enable the watchdog timer using the SET0 and SET1 pins. The ability to enable and disable the watchdog is useful to avoid undesired watchdog trips during initialization and shutdown. When the SETx pins are changed to disable the watchdog timer, changes on the pins are responded to immediately (as shown in Figure 7-5). When the watchdog goes from disabled to enabled, there is a 150 µs (t<sub>WD-setup</sub>) transition period where the device does not respond to changes on WDI. After this 150-µs period, the device begins to respond to changes on WDI again.

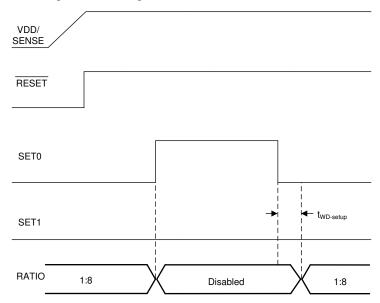
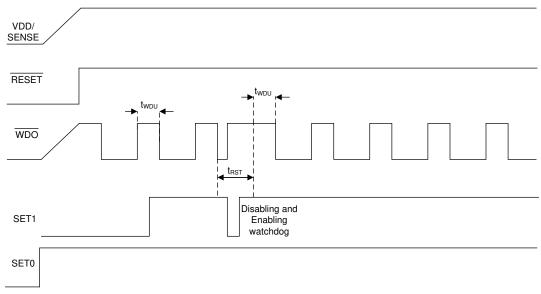


Figure 7-5. Enabling the Watchdog Timer

# 7.3.5.1.2 Disabling the Watchdog Timer When Using the CRST Capacitor

When using the TPS3850-Q1 with fixed timing options, if the watchdog is disabled and reenabled while  $\overline{WDO}$  is asserted (logic low) the watchdog performs as described in the Section 7.3.5.1.1 section. However, if there is a capacitor on the CRST pin, and the watchdog is disabled and reenabled when  $\overline{WDO}$  is asserted (logic low), then the watchdog behaves as shown in Figure 7-6. When the watchdog is disabled,  $\overline{WDO}$  goes high impedance (logic high). However, when the watchdog is enabled again, the  $t_{RST}$  period must expire before the watchdog resumes normal operation.



There is no WDI signal in this figure, WDI is always at GND.

Figure 7-6. Enabling and Disabling the Watchdog Timer During a WDO Reset Event

#### 7.3.5.1.3 SET0 and SET1 During Normal Watchdog Operation

The SET0 and SET1 pins can be used to control the window watchdog ratio of the lower boundary to the upper boundary. There are four possible modes for the watchdog (see Table 8-5): disabled, 1:8 ratio, 3:4 ratio, and 1:2 ratio. If SET0 = 1 and SET1 = 0, then the watchdog is disabled. When the watchdog is disabled  $\overline{\text{WDO}}$  does not assert, and the TPS3850 functions as a normal supervisor. The SET0 and SET1 pins can be changed when the device is operational, but cannot be changed at the same time. If these pins are changed when the device is operational, then there must be a 500- $\mu$ s ( $t_{\text{SET}}$ ) delay between switching the two pins. If the SET0 and SET1 are used to change the reset timing, then a reset event must occur before the new timing condition is latched. This reset can be triggered by SENSE rising above  $V_{\text{IT+(OV)}}$  or below  $V_{\text{IT-(UV)}}$ , or by bringing  $V_{\text{DD}}$  below  $V_{\text{UVLO}}$ . Figure 7-7 shows how the SET0 and SET1 pins do not change the watchdog timing option until a reset event has occurred.



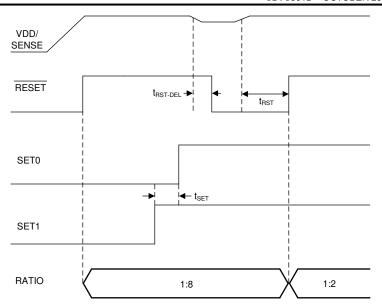


Figure 7-7. Changing SET0 and SET1 Pins

## 7.3.6 Window Watchdog Timer

This section provides information for the window watchdog modes of operation. A window watchdog is typically employed in safety critical applications where a traditional watchdog timer is inadequate. In a traditional watchdog, there is a maximum time in which a pulse must be issued to prevent the reset from occurring. However, in a window watchdog the pulse must be issued between a maximum lower window time  $(t_{WDL(max)})$  and the minimum upper window time  $(t_{WDU(min)})$  set by the CWD pin and the SET0 and SET1 pins. Table 8-5 describes how  $t_{WDU}$  can be used to calculate the timing of  $t_{WDL}$ . The  $t_{WDL}$  timing can also be changed by adjusting the SET0 and SET1 pins. Figure 7-8 shows the valid region for a WDI pulse to be issued to prevent the  $\overline{WDO}$  from being triggered and being pulled low.

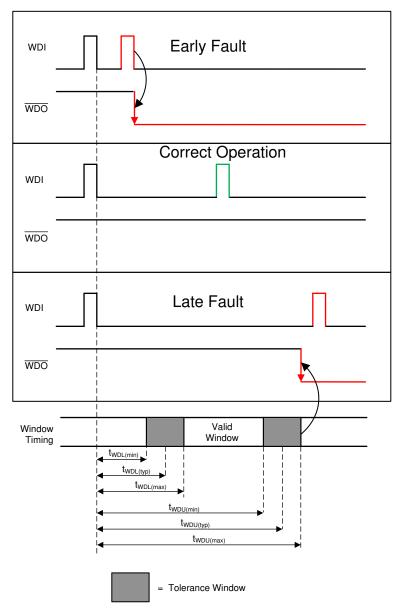


Figure 7-8. TPS3850 Window Watchdog Timing

#### 7.3.6.1 CWD

The CWD pin provides the user the functionality of both high-precision, factory-programmed watchdog timing options and user-programmable watchdog timing. The TPS3850 features three options for setting the watchdog window: connecting a capacitor to the CWD pin, connecting a pullup resistor to VDD, and leaving the CWD pin unconnected. The configuration of the CWD pin is evaluated by the device every time  $V_{SENSE}$  enters the valid window  $(V_{IT+(UV)} < V_{SENSE} < V_{IT-(OV)})$ . The pin evaluation is controlled by an internal state machine that determines which option is connected to the CWD pin. The sequence of events takes 381  $\mu$ s ( $t_{INIT}$ ) to determine if the CWD pin is left unconnected, pulled up through a resistor, or connected to a capacitor. If the CWD pin is being pulled up to VDD using a pullup resistor, then a 10-k $\Omega$  resistor is required.

### 7.3.6.2 WDI Functionality

WDI is the watchdog timer input that controls the  $\overline{WDO}$  output. The WDI input is triggered by the falling edge of the input signal. For the first pulse, the watchdog acts as a traditional watchdog timer; thus, the first pulse must be issued before  $t_{WDU(min)}$ . After the first pulse, to ensure proper functionality of the watchdog timer, always issue the WDI pulse within the window of  $t_{WDL(max)}$  and  $t_{WDU(min)}$ . If the pulse is issued in this region, then  $\overline{WDO}$  remains unasserted. Otherwise, the device asserts  $\overline{WDO}$ , putting the  $\overline{WDO}$  pin into a low-impedance state.

The watchdog input (WDI) is a digital pin. To ensure there is no increase in  $I_{DD}$ , drive the WDI pin to either VDD or GND at all times. Putting the pin to an intermediate voltage can cause an increase in supply current ( $I_{DD}$ ) because of the architecture of the digital logic gates. When  $\overline{RESET}$  is asserted, the watchdog is disabled and all signals input to WDI are ignored. When  $\overline{RESET}$  is no longer asserted, the device resumes normal operation and no longer ignores the signal on WDI. If the watchdog is disabled, drive the WDI pin to either VDD or GND.

# 7.3.6.3 WDO Functionality

The TPS3850 features a window watchdog timer with an independent watchdog output ( $\overline{WDO}$ ). The independent watchdog output provides the flexibility to flag a fault in the watchdog timing without performing an entire system reset. When  $\overline{RESET}$  is not asserted (high), the  $\overline{WDO}$  signal maintains normal operation. When asserted,  $\overline{WDO}$  remains down for  $\overline{t_{RST}}$ . When the  $\overline{RESET}$  signal is asserted (low), the  $\overline{WDO}$  pin goes to a high-impedance state. When  $\overline{RESET}$  is unasserted, the window watchdog timer resumes normal operation and  $\overline{WDO}$  can be used again.

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#### 7.4 Device Functional Modes

Table 7-1 summarizes the functional modes of the TPS3850.

Table 7-1. Device Functional Modes

VDD	WDI	WDO	SENSE	RESET
V <sub>DD</sub> < V <sub>POR</sub>	_	_	_	Undefined
$V_{POR} \le V_{DD} < V_{UVLO}$	Ignored	High	_	Low
	Ignored	High	V <sub>SENSE</sub> < V <sub>IT+(UV)</sub> (1)	Low
	Ignored	High	V <sub>SENSE</sub> > V <sub>IT-(OV)</sub> (1)	Low
V <sub>DD</sub> ≥ V <sub>DD (min)</sub>	$t_{\text{WDL(max)}} \le t_{\text{pulse}} \stackrel{(3)}{\le} t_{\text{WDU(min)}}$	High	$V_{IT-(UV)} < V_{SENSE} < V_{IT+(OV)}$ (2)	High
	$t_{WDL(max)} > t_{pulse}$ (3)	Low	$V_{IT-(UV)} < V_{SENSE} < V_{IT+(OV)}$ (2)	High
	$t_{\text{WDU(min)}} < t_{\text{pulse}}$ (3)	Low	$V_{\text{IT-(UV)}} < V_{\text{SENSE}} < V_{\text{IT+(OV)}}$ (2)	High

- (1) When V<sub>SENSE</sub> has not entered the valid window.
- (2) When  $V_{SENSE}$  is in the valid window.
- (3) Where t<sub>pulse</sub> is the time between falling edges on WDI.

# 7.4.1 $V_{DD}$ is Below $V_{POR}$ ( $V_{DD} < V_{POR}$ )

When  $V_{DD}$  is less than  $V_{POR}$ ,  $\overline{RESET}$  is undefined and can be either high or low. The state of  $\overline{RESET}$  largely depends on the load that the  $\overline{RESET}$  pin is experiencing.

# 7.4.2 Above Power-On-Reset But Less Than UVLO $(V_{POR} \le V_{DD} < V_{UVLO})$

When  $V_{DD}$  is less than  $V_{UVLO}$ , and greater than or equal to  $V_{POR}$ , the  $\overline{RESET}$  signal is asserted (logic low) regardless of the voltage on the SENSE pin. When  $\overline{RESET}$  is asserted, the watchdog output  $\overline{WDO}$  is in a high-impedance state regardless of the WDI signal that is input to the device.

# 7.4.3 Above UVLO But Less Than $V_{DD (min)}$ ( $V_{UVLO} \le V_{DD} < V_{DD (min)}$ )

When  $V_{DD}$  is less than  $V_{DD\ (min)}$  and greater than or equal to  $V_{UVLO}$ , the  $\overline{RESET}$  signal responds to changes on the SENSE pin, but the accuracy can be degraded.

# 7.4.4 Normal Operation (V<sub>DD</sub> ≥ V<sub>DD (min)</sub>)

When  $V_{DD}$  is greater than or equal to  $V_{DD~(min)}$ , the  $\overline{RESET}$  signal is determined by  $V_{SENSE}$ . When  $\overline{RESET}$  is asserted,  $\overline{WDO}$  goes to a high-impedance state.  $\overline{WDO}$  is then pulled high through the pullup resistor.

Product Folder Links: TPS3850

# 8 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

# 8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

### 8.1.1 CRST Delay

The TPS3850 features three options for setting the reset delay ( $t_{RST}$ ): connecting a capacitor to the CRST pin, connecting a pullup resistor to VDD, and leaving the CRST pin unconnected. Figure 8-1 shows a schematic drawing of all three options. To determine which option is connected to the CRST pin, an internal state machine controls the internal pulldown device and measures the pin voltage. This sequence of events takes 381  $\mu$ s ( $t_{INIT}$ ) to determine which timing option is used. Every time  $\overline{RESET}$  is asserted, the state machine determines what is connected to the pin.

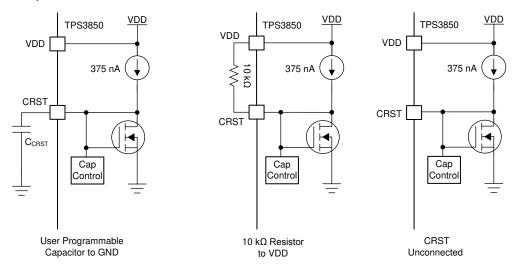


Figure 8-1. CRST Charging Circuit

# 8.1.1.1 Factory-Programmed Reset Delay Timing

To use the factory-programmed timing options, the CRST pin must either be left unconnected or pulled up to VDD through a  $10-k\Omega$  pullup resistor. Using these options enables a high-precision, 15% accurate reset delay timing, as shown in Table 8-1.

Table 8-1. Reset Delay Time for Factory-Programmed Reset Delay Timing

CRST	RES	UNIT		
CROT	MIN	TYP	MAX	ONT
NC	170	200	230	ms
10 kΩ to VDD	8.5	10	11.5	ms

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### 8.1.1.2 Programmable Reset Delay-Timing

The TPS3850 uses a CRST pin charging current ( $I_{CRST}$ ) of 375 nA. When using an external capacitor, the rising RESET delay time can be set to any value between 700 µs ( $C_{CRST}$  = 100 pF) and 3.2 seconds ( $C_{CRST}$  = 1 µF). The typical ideal capacitor value needed for a given delay time can be calculated using Equation 3, where  $C_{CRST}$  is in microfarads and  $I_{RST}$  is in seconds:

$$t_{RST} = 3.22 \times C_{CRST} + 0.000381$$
 (3)

To calculate the minimum and maximum-reset delay time use Equation 4 and Equation 5, respectively.

$$t_{RST(min)} = 2.8862 \times C_{CRST} + 0.000324$$
 (4)

$$t_{RST(max)} = 3.64392 \times C_{CRST} + 0.000438$$
 (5)

The slope of Equation 3 is determined by the time the CRST charging current ( $I_{CRST}$ ) takes to charge the external capacitor up to the CRST comparator threshold voltage ( $V_{CRST}$ ). When  $\overline{RESET}$  is asserted, the capacitor is discharged through the internal CRST pulldown resistor. When the  $\overline{RESET}$  conditions are cleared, the internal precision current source is enabled and begins to charge the external capacitor; when  $V_{CRST} = 1.21$  V,  $\overline{RESET}$  is unasserted. Note that to minimize the difference between the calculated  $\overline{RESET}$  delay time and the actual  $\overline{RESET}$  delay time, use a use a high-quality ceramic dielectric COG, X5R, or X7R capacitor and minimize parasitic board capacitance around this pin. Table 8-2 lists the reset delay time ideal capacitor values for  $C_{CRST}$ .

Table 8-2. Reset Delay Time for Common Ideal Capacitor Values

C <sub>CRST</sub>	RESET D	UNIT		
	MIN <sup>(1)</sup>	TYP	MAX <sup>(1)</sup>	ONT
100 pF	0.61	0.70	0.8	ms
1 nF	3.21	3.61	4.08	ms
10 nF	29.2	32.6	36.8	ms
100 nF	289	323	364	ms
1 μF	2886	3227	3644	ms

<sup>(1)</sup> Minimum and maximum values are calculated using ideal capacitors.

### 8.1.2 CWD Functionality

The TPS3850 features three options for setting the watchdog window: connecting a capacitor to the CWD pin, connecting a pullup resistor to VDD, and leaving the CWD pin unconnected. Figure 8-2 shows a schematic drawing of all three options. If this pin is connected to VDD through a  $10-k\Omega$  pullup resistor or left unconnected (high impedance), then the factory-programmed watchdog timeouts are enabled; see the *Section 6.6* table. Otherwise, the watchdog timeout can be adjusted by placing a capacitor from the CWD pin to ground.

Product Folder Links: TPS3850

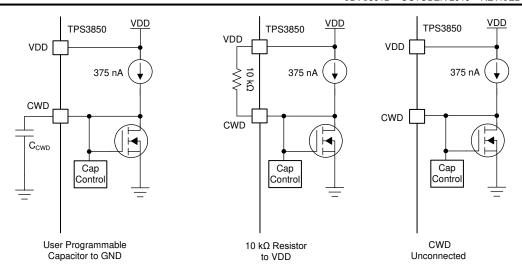


Figure 8-2. CWD Charging Circuit

# 8.1.2.1 Factory-Programmed Timing Options

If using the factory-programmed timing options (listed in Table 8-3), the CWD pin must either be unconnected or pulled up to VDD through a  $10-k\Omega$  pullup resistor. Using these options enables high-precision, factory-programmed watchdog timing.

Table 8-3. Factory-Programmed Watchdog Timing

INPUT			WATCHDOG LOWER BOUNDARY (t <sub>WDL</sub> )			WATCHDOG UPPER BOUNDARY (t <sub>WDU</sub> )			LIMIT	
CWD	SET0	SET1	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
NC	0	0	19.1	22.5	25.9	46.8	55.0	63.3	ms	
	0	1	1.48	1.85	2.22	23.375	27.5	31.625	ms	
	1	0	Watchdog disabled			Watchdog disabled				
	1	1	680	800	920	1360	1600	1840	ms	
	0	0	7.65	9.0	10.35	92.7	109.0	125.4	ms	
10 kΩ to VDD	0	1	7.65	9.0	10.35	165.8	195.0	224.3	ms	
	1	0	Watch	dog disabled		Watch	idog disabled			
	1	1	1.48	1.85	2.22	9.35	11.0	12.65	ms	

#### 8.1.2.2 Adjustable Capacitor Timing

Adjustable capacitor timing is achievable by connecting a capacitor to the CWD pin. If a capacitor is connected to CWD, then a 375-nA constant-current source charges  $C_{CWD}$  until  $V_{CWD}$  = 1.21 V. The TPS3850 determines the window watchdog upper boundary with the formula given in Equation 6, where  $C_{CWD}$  is in microfarads and  $t_{WDLI}$  is in seconds.

$$t_{WDU(typ)} = 77.4 \times C_{CWD} + 0.055$$
 (6)

The TPS3850 is designed and tested using  $C_{CWD}$  capacitors between 100 pF and 1  $\mu$ F. Note that Equation 6 is for ideal capacitors. Capacitor tolerances cause the actual device timing to vary such that the minimum of  $t_{WDU}$  can decrease and the maximum of  $t_{WDU}$  can increase by the capacitor tolerance. To allow for a valid watchdog window, choose a capacitor with tolerance such that  $t_{WDU(min)}$  and  $t_{WDL(max)}$  do not overlap. For the most accurate timing, use ceramic capacitors with COG dielectric material. As shown in Table 8-4, when using the minimum capacitor of 100 pF, the watchdog upper boundary is 62.74 ms; whereas with a 1- $\mu$ F capacitor, the watchdog upper boundary is 77.455 seconds. If a  $C_{CWD}$  capacitor is used, Equation 6 can be used to set  $t_{WDU}$  the window watchdog upper boundary. The window watchdog lower boundary is dependent on the SET0 and SET1 pins because these pins set the window watchdog ratio of the lower boundary to upper boundary; Table 8-5 shows how  $t_{WDU}$  can be used to calculate  $t_{WDL}$  based on the SET0 and SET1 pins.

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6	WATCHDOG	UNIT		
C <sub>CWD</sub>	MIN <sup>(1)</sup>	TYP	MAX <sup>(1)</sup>	ONIT
100 pF	56.77	62.74	68.7	ms
1 nF	119.82	132.4	144.98	ms
10 nF	750	829	908	ms
100 nF	7054	7795	8536	ms
1 μF	70096	77455	84814	ms

(1) Minimum and maximum values are calculated using ideal capacitors.

### Table 8-5. Programmable CWD Timing

INF	TUT		WATCHDOG	LOWER BOUN	DARY (t <sub>WDL</sub> )	WATCHDOG UPPER BOUNDARY (t <sub>WDU</sub> )			UNIT
CWD	SET0	SET1	MIN	TYP	MAX	MIN <sup>(2)</sup>	TYP <sup>(1)</sup>	MAX <sup>(2)</sup>	ONIT
	0	0	t <sub>WDU(min)</sub> x 0.125	t <sub>WDU</sub> x 0.125	t <sub>WDU(max)</sub> x 0.125	0.905 x t <sub>WDU(typ)</sub>	t <sub>WDU(typ)</sub>	1.095 x t <sub>WDU(typ)</sub>	s
C <sub>CWD</sub>	0	1	t <sub>WDU(min)</sub> x 0.75	t <sub>WDU</sub> x 0.75	$t_{WDU(max)} \times 0.75$	0.905 x t <sub>WDU(typ)</sub>	t <sub>WDU(typ)</sub>	1.095 x t <sub>WDU(typ)</sub>	s
CCMD	1	0	W	atchdog disable	d	Wato	hdog disabled		
	1	1	t <sub>WDU(min)</sub> x 0.5	t <sub>WDU</sub> x 0.5	t <sub>WDU(max)</sub> x 0.5	0.905 x t <sub>WDU(typ)</sub>	t <sub>WDU(typ)</sub>	1.095 x t <sub>WDU(typ)</sub>	s

- (1) Calculated from Equation 6 using ideal capacitors.
- (2) The  $t_{WDU(min)}$  and  $t_{WDU(max)}$  include  $I_{CWD}$  and  $V_{CWD}$  minimum to maximum variation

### 8.1.3 Adjustable SENSE Configuration

The TPS3850H01 has an undervoltage supervisor that can monitor voltage rails greater than 0.4 V. Table 8-6 contains 1% resistor values for creating a voltage divider to monitor common rails from 0.5 V to 12 V with a threshold of 4% and 10%. These resistor values can be scaled to decrease the amount of current flowing through the resistor divider, but increasing the resistor values also decreases the accuracy of the resistor divider. General practice is for the current flowing through the resistor divider to be 100 times greater than the current going into the SENSE pin. This practice ensures the highest possible accuracy. Equation 7 can be used to calculate the resistors required in the resistor divider. Figure 8-3 shows the block diagram for adjustable operation.

$$V_{MON} = V_{IT(ADJ)} \times \left(1 + \frac{R_1}{R_2}\right)$$
 (7)

Table 8-6. SENSE Resistor Divider Values

		4% THRESHOLD		10% THRESHOLD			
INPUT VOLTAGE (V)	R <sub>1</sub> (kΩ)	R <sub>2</sub> (kΩ)	THRESHOLD VOLTAGE (V)	R <sub>1</sub> (kΩ)	R <sub>2</sub> (kΩ)	THRESHOLD VOLTAGE (V)	
0.5	16.2	80.6	0.48	10	80.6	0.45	
0.8	75	80.6	0.77	64.9	80.6	0.72	
0.9	93.1	80.6	0.86	82.5	80.6	0.81	
1.2	150	80.6	1.14	137	80.6	1.08	
1.8	267	80.6	1.73	249	80.6	1.64	
2.5	402	80.6	2.40	374	80.6	2.26	
3	499	80.6	2.88	464	80.6	2.70	
3.3	562	80.6	3.19	523	80.6	2.99	
5	887	80.6	4.80	825	80.6	4.49	
12	2260	80.6	11.62	2100	80.6	10.82	

Product Folder Links: TPS3850



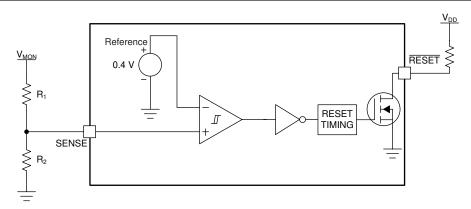


Figure 8-3. Adjustable Voltage Divider

#### 8.1.4 Overdrive on the SENSE Pin

The propagation delay from exceeding the threshold to  $\overline{RESET}$  being asserted is dependent on two conditions: the amplitude of the voltage on the SENSE pin relative to the threshold, ( $\Delta V_1$  and  $\Delta V_2$ ), and the length of time that the voltage is above or below the trip point ( $t_1$  and  $t_2$ ). If the voltage is just over the trip point for a long period of time, then  $\overline{RESET}$  asserts and the output is pulled low. However, if the SENSE voltage is just over the trip point for a few nanoseconds, then the  $\overline{RESET}$  does not assert and the output remains high. The time required for  $\overline{RESET}$  to assert can be changed by increasing the time that the SENSE voltage goes over the trip point. Equation 8 shows how to calculate the percentage overdrive.

Overdrive = 
$$|(V_{SENSE}/V_{ITx} - 1) \times 100\%|$$
 (8)

In Equation 8,  $V_{ITx}$  corresponds to the SENSE threshold trip point. If  $V_{SENSE}$  exceeds the positive threshold, then  $V_{IT+(OV)}$  is used.  $V_{IT-(UV)}$  is used when  $V_{SENSE}$  falls below the negative threshold. In Figure 8-4,  $t_1$  and  $t_2$  correspond to the amount of time that the SENSE voltage is over the threshold. The response time versus overdrive for  $V_{IT+(OV)}$  and  $V_{IT-(UV)}$  is illustrated in Figure 6-14 and Figure 6-17, respectively.

The TPS3850 is relatively immune to short positive and negative transients on the SENSE pin because of the overdrive voltage curve; see Figure 6-20 and Figure 6-21.

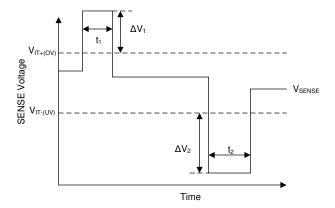


Figure 8-4. Overdrive Voltage on the SENSE Pin

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## 8.2 Typical Applications

## 8.2.1 Design 1: Monitoring a 1.2-V Rail with Factory-Programmable Watchdog Timing

A typical application for the TPS3850 is shown in Figure 8-5. The TPS3850G12 is used to monitor the 1.2-V,  $V_{CORE}$  rail powering the microcontroller.

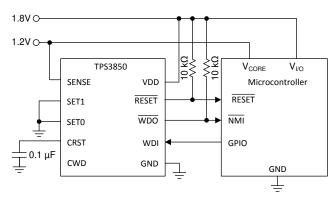


Figure 8-5. Monitoring Supply Voltage and Watchdog Supervision of a Microcontroller

### 8.2.1.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Reset delay	Minimum reset delay of 250 ms	Minimum reset delay of 260 ms, reset delay of 322 ms (typical)
Watchdog window	Functions with a 200-Hz pulse-width modulation (PWM) signal with a 50% duty cycle	Leaving the CWD pin unconnected with SET0 = 0 and SET1 = 1 produces a window with a t <sub>WDL(max)</sub> of 2.2 ms and a t <sub>WDU(min)</sub> of 22 ms
Output logic voltage	1.8-V CMOS	1.8-V CMOS
Monitored rail	1.2 V within ±5%	Worst-case V <sub>IT+(OV)</sub> 1.257 V (4.8%)
Monitored rail	1.2 V WIUIIII ±3%	Worst-case V <sub>IT-(UV)</sub> 1.142 V (4.7%)
Maximum device current consumption	200 μΑ	10 μA of current consumption, typical worst-case of 199 μA when WDO or RESET is asserted

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Monitoring the 1.2-V Rail

The window comparator allows for precise voltage supervision of common rails between 0.9 V and 5.0 V. This application calls for very tight monitoring of the rail with only  $\pm 5\%$  of variation allowed on the rail. To ensure this requirement is met, the TPS3850G12 was chosen for its  $\pm 4\%$  thresholds. To calculate the worst-case for  $V_{\text{IT+(OV)}}$  and  $V_{\text{IT-(UV)}}$ , the accuracy must also be taken into account. The worst-case for  $V_{\text{IT+(OV)}}$  can be calculated by Equation 9:

$$V_{\text{IT+(OV)(Worst-Case)}} = V_{\text{IT+(OV)typ}} \times 1.048 = 1.2 \times 1.048 = 1.257 \text{ V}$$
 (9)

The worst case for  $V_{IT-(UV)}$  can be calculated using Equation 10:

$$V_{\text{IT-(UV)(Worst-Case)}} = V_{\text{IT-(UV)typ}} \times 0.952 = 1.2 \times 0.952 = 1.142 \text{ V}$$
(10)

#### 8.2.1.2.2 Meeting the Minimum Reset Delay

The TPS3850 features three options for setting the reset delay: connecting a capacitor to the CRST pin, connecting a pullup resistor, and leaving the CRST pin unconnected. If the CRST pin is either unconnected or pulled up the minimum timing requirement cannot be met, thus an external capacitor must be connected to the CRST pin. Because a minimum time is required, the worst-case scenario is a supervisor with a high CRST charging current ( $I_{CRST}$ ) and a low CRST comparator threshold ( $V_{CRST}$ ). For applications with ambient temperatures ranging from  $-40^{\circ}$ C to  $+125^{\circ}$ C,  $C_{CRST}$  can be calculated using  $I_{CRST(MAX)}$ ,  $V_{CRST(MIN)}$ , and solving for  $C_{CRST}$  in Equation 11:

$$C_{RST(min)\_ideal} = \frac{t_{RST(min)} - 0.000324}{2.8862} = \frac{0.25 - 0.000324}{2.8862}$$
(11)

When solving Equation 11, the minimum capacitance required at the CRST pin is  $0.086 \mu F$ . If standard capacitors with  $\pm 10\%$  tolerances are used, then the minimum CRST capacitor required can be found in Equation 12:

$$C_{RST(min)} = \frac{C_{RST(min)\_ideal}}{1 - C_{tolerance}} = \frac{0.086 \ \mu F}{1 - 0.1} \tag{12}$$

Solving Equation 12 where  $C_{tolerance}$  is 0.1 or 10%, the minimum  $C_{CRST}$  capacitor is 0.096  $\mu$ F. This value is then rounded up to the nearest standard capacitor value, so a 0.1- $\mu$ F capacitor must be used to achieve this reset delay timing. If voltage and temperature derating are being considered, then also include these values in  $C_{tolerance}$ .

#### 8.2.1.2.3 Setting the Watchdog Window

In this application, the window watchdog timing options are based on the PWM signal that is provided to the TPS3850. A window watchdog setting must be chosen such that the falling edge of the PWM signal always falls within the window. A nominal window must be designed with  $t_{WDL(max)}$  less than 5 ms and  $t_{WDU(min)}$  greater than 5 ms. There are several options that satisfy this window option. An external capacitor can be placed on the CWD pin and calculated to have a sufficient window. Another option is to use one of the factory-programmed timing options. An additional advantage of choosing one of the factory-programmed options is the ability to reduce the number of components required, thus reducing overall BOM cost. Leaving the CWD pin unconnected (NC) with SET0 = 0 and SET1 = 1 produces a  $t_{WDL(max)}$  of 2.22 ms and a  $t_{WDU(min)}$  of 23.375 ms; see Figure 8-10.

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# 8.2.1.2.4 Calculating the RESET and WDO Pullup Resistor

The TPS3850 uses an open-drain configuration for the  $\overline{RESET}$  circuit, as shown in Figure 8-6. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that  $V_{OL}$  is below its maximum value. To choose the proper pullup resistor, there are three key specifications to keep in mind: the pullup voltage ( $V_{PU}$ ), the recommended maximum  $\overline{RESET}$  pin current ( $I_{RST}$ ), and  $V_{OL}$ . The maximum  $V_{OL}$  is 0.4 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.4 V with  $I_{RST}$  kept below 10 mA. For this example, with a  $V_{PU}$  of 1.8 V, a resistor must be chosen to keep  $I_{RST}$  below 200  $\mu$ A because this value is the maximum consumption current allowed. To ensure this specification is met, a pullup resistor value of 10 k $\Omega$  was selected, which sinks a maximum of 180  $\mu$ A when  $\overline{RESET}$  or  $\overline{WDO}$  is asserted. As illustrated in Figure 6-12, the  $\overline{RESET}$  current is at 180  $\mu$ A and the low-level output voltage is approximately zero.

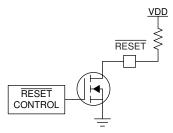
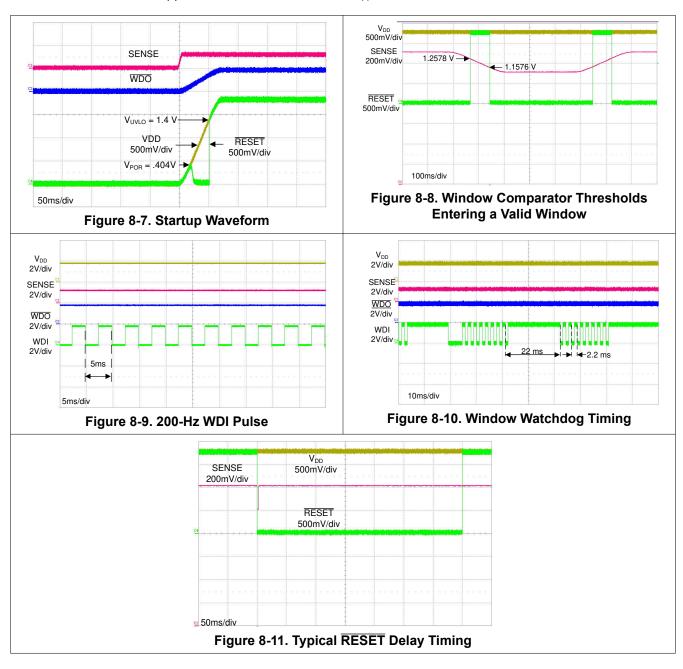


Figure 8-6. Open-Drain RESET Configuration



## 8.2.1.3 Application Curves

Unless otherwise stated, application curves were taken at T<sub>A</sub> = 25°C.



# 8.2.2 Design 2: Using TPS3850H01 to monitor a 0.7-V Rail With an Adjustable Window Watchdog Timing

A typical application for the TPS3850H01 is shown in Figure 8-12.

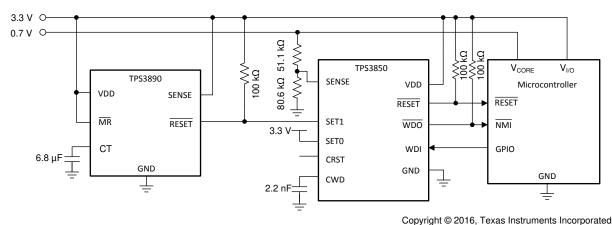


Figure 8-12. Monitoring Supply Voltage and Watchdog Supervision of a Microcontroller

### 8.2.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT		
Reset delay	Minimum RESET delay of 150 ms	Minimum RESET delay of 170 ms		
Watchdog disable for initialization period	Watchdog must remain disabled for 7 seconds until logic enables the watchdog timer	7.21 seconds (typ)		
Watchdog window	250 ms, maximum	t <sub>WDL(max)</sub> = 135 ms, t <sub>WDU(min)</sub> = 181 ms		
Output logic voltage	3.3-V CMOS	3.3-V CMOS		
		V <sub>ITN (max)</sub> 0.667 V (-4.7%)		
Monitored rail	0.7 V, with 7% threshold	V <sub>ITN (typ)</sub> 0.65 V (-6.6%)		
		V <sub>ITN (min)</sub> 0.641 V (-8.5%)		
Maximum device current consumption	50 μΑ	10 $\mu A$ of current consumption typical, worst-case of 52 $\mu A$ when $\overline{WDO}$ or $\overline{RESET}$ is asserted <sup>(1)</sup>		

<sup>(1)</sup> Only includes the current consumption of the TPS3850.

#### 8.2.2.2 Detailed Design Procedure

### 8.2.2.2.1 Meeting the Minimum Reset Delay

The design goal for the  $\overline{\text{RESET}}$  delay time can be achieved by either using an external capacitor or the CRST pin can be left unconnected. To minimize component count, the CRST pin is left unconnected. For CRST = NC, the minimum delay is 170 ms, which is greater than the minimum required  $\overline{\text{RESET}}$  delay of 150 ms.

### 8.2.2.2 Setting the Window Watchdog

As illustrated in Figure 8-2, there are three options for setting the window watchdog. The design specifications in this application require the programmable timing option (external capacitor connected to CWD). When a capacitor is connected to the CWD pin, the window is governed by Equation 13. Equation 13 is only valid for ideal capacitors, any temperature or voltage derating must be accounted for separately.

$$C_{CWD}\left(\mu\text{F}\right) = \frac{t_{WDU} - 0.055}{77.4} = \frac{0.25 - 0.055}{77.4} = 0.0025 \ \mu\text{F} \tag{13}$$

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The nearest standard capacitor value to 2.5 nF is 2.2 nF. Selecting 2.2 nF for the C<sub>CWD</sub> capacitor gives the following minimum and maximum timing parameters:

$$t_{WDU(MIN)} = 0.905 \times t_{WDU(TYP)} = 0.905 \times \left(77.4 \times 2.2 \times 10^{-3} + 0.055\right) = 203.88 \text{ ms} \tag{14}$$

$$t_{WDL(MAX)} = 0.5 \times t_{WDU(MAX)} = 0.5 \times \left[1.05 \times \left(77.4 \times 2.2 \times 10^{-3} + 0.055\right)\right] = 118 \text{ ms} \tag{15}$$

Capacitor tolerance also influence  $t_{WDU(MIN)}$  and  $t_{WDL(MAX)}$ . Select a ceramic COG dielectric capacitor for high accuracy. For 2.2 nF, COG capacitors are readily available with a 5% tolerance, which results in a 5% decrease in  $t_{WDU(MIN)}$  and a 5% increase in  $t_{WDL(MAX)}$ , giving 181 ms and 135 ms, respectively. A falling edge must be issued within this window.

### 8.2.2.2.3 Watchdog Disabled During the Initialization Period

The watchdog is often needed to be disabled during startup to allow for an initialization period. When the initialization period is over, the watchdog timer is turned back on to allow the microcontroller to be monitored by the TPS3850. To achieve this setup, SET0 must start at VDD and SET1 must start at GND. In this design, SET0 is simply tied to VDD and SET1 is controlled by a TPS3890 supervisor. In this application, the TPS3890 was chosen to monitor  $V_{DD}$  as well, which means that RESET on the TPS3890 stays low until  $V_{DD}$  rises above  $V_{ITN}$ . When  $V_{DD}$  comes up, the delay time can be adjusted through the CT capacitor on the TPS3890. With this approach, the RESET delay can be adjusted from a minimum of 25  $\mu$ s to a maximum of 30 seconds. For this design, a minimum delay of 7 seconds is needed until the watchdog timer is enabled. The CT capacitor calculation (see the TPS3890 data sheet) yields an ideal capacitance of 6.59  $\mu$ F, giving a closest standard ceramic capacitor value of 6.8  $\mu$ F. When connecting a 6.8- $\mu$ F capacitor from CT to GND, the typical delay time is 7.21 seconds. Figure 8-13 illustrates the typical startup waveform for this circuit when the watchdog input is off. Figure 8-13 illustrates that when the watchdog is disabled, the  $\overline{WDO}$  output remains high. See the TPS3890 data sheet for detailed information on the TPS3890.

#### 8.2.2.2.4 Calculating the Sense Resistor

There are three key specifications to keep in mind when calculating the resistor divider values ( $R_1$  and  $R_2$ , see Figure 7-4 or Figure 8-3): voltage threshold ( $V_{IT(ADJ)}$ ), resistor tolerance, and the SENSE pin current ( $I_{SENSE}$ ). To ensure that no accuracy is lost because of  $I_{SENSE}$ , the current through the resistor divider must be 100 times greater than  $I_{SENSE}$ . Starting with  $R_2$  = 80.6 k $\Omega$  provides a 5- $\mu$ A resistor divider current when  $V_{SENSE}$  = 0.4 V. To calculate the nominal resistor values, use Equation 16:

$$V_{ITN} = V_{IT(ADJ)} + R_1 \frac{V_{IT(ADJ)}}{R_2}$$
(16)

#### where

- V<sub>ITN</sub> is the monitored falling threshold voltage and
- V<sub>IT(ADJ)</sub> is the threshold voltage on the SENSE pin

Solving Equation 16 for  $R_1$  gives the nearest 1% resistor of 51.1 k $\Omega$ . Now, plug  $R_1$  back into Equation 16 to get the monitored threshold. With these resistor values, the nominal threshold is 0.65 V or 6.6%.

Product Folder Links: TPS3850

To calculate the minimum and maximum threshold variation including the tolerances of the resistors, threshold voltage, and sense current, use Equation 17 and Equation 18.

$$V_{ITN(min)} = V_{IT(ADJ)min} + R_{1(min)} \left( \frac{V_{IT(ADJ)min}}{R_{2(max)}} + I_{SENSE(min)} \right) = 0.641 \text{ V}$$

$$(17)$$

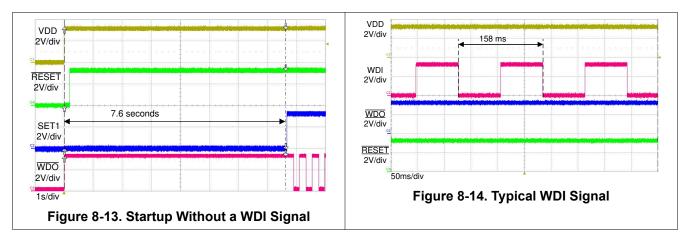
$$V_{ITN(max)} = V_{IT(ADJ)max} + R_{1(max)} \left( \frac{V_{IT(ADJ)max}}{R_{2(min)}} + I_{SENSE(max)} \right) = 0.667 \text{ V}$$
(18)

#### where

- V<sub>ITN</sub> is the falling monitored threshold voltage
- V<sub>IT(ADJ)</sub> is the sense voltage threshold and
- I<sub>SENSE</sub> is the sense pin current

The calculated tolerance on  $R_1$  and  $R_2$  is 1%.

# 8.2.2.3 Application Curves



# 9 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1.6 V and 6.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin.

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# 10 Layout

# 10.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a 0.1- $\mu$ F ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CRST pin, then minimize parasitic capacitance on this pin so the  $\overline{\text{RESET}}$  delay time is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-μF ceramic capacitor as near as possible to the VDD pin.
- If a C<sub>CRST</sub> capacitor or pullup resistor is used, place these components as close as possible to the CRST pin. If the CRST pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin.
- If a C<sub>CWD</sub> capacitor or pullup resistor is used, place these components as close as possible to the CWD pin. If the CWD pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin.
- Place the pullup resistors on RESET and WDO as close to the pin as possible.

### 10.2 Layout Example

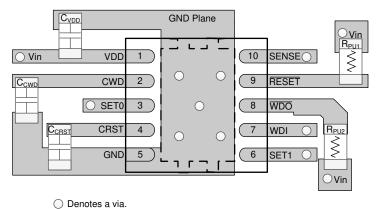


Figure 10-1. Typical Layout for the TPS3850

Product Folder Links: TPS3850

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Device Nomenclature

**Table 11-1. Device Nomenclature** 

DESCRIPTION	NOMENCLATURE	VALUE
TPS3850 (high-accuracy supervisor with window watchdog)	_	_
X	G	$V_{IT+(OV)} = 4\%; V_{IT-(UV)} = -4\%$
(nominal thresholds as a percent of the nominal monitored voltage)	Н	V <sub>IT+(OV)</sub> = 7%; V <sub>IT-(UV)</sub> = -7%
	01	0.4 V
	09	0.9 V
	115	1.15 V
	12	1.2 V
yy(y) (nominal monitored voltage option)	18	1.8 V
(nonmal morniored voltage option)	25	2.5 V
	30	3.0 V
	33	3.3 V
	50	5.0 V

### 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation see the following:

- TPS3890 Low Quiescent Current, 1% Accurate Supervisor with Programmable Delay
- · Optimizing Resistor Dividers at a Comparator Input
- TPS3850EVM-781 Evaluation Module

# 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.4 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.5 Trademarks

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#### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.7 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.



# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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# **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TPS3850G12DRCR	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850CA
TPS3850G12DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850CA
TPS3850G12DRCT	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850CA
TPS3850G12DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850CA
TPS3850G18DRCR	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850DA
TPS3850G18DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850DA
TPS3850G18DRCT	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850DA
TPS3850G18DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850DA
TPS3850G30DRCR	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850FA
TPS3850G30DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850FA
TPS3850G30DRCT	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850FA
TPS3850G30DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850FA
TPS3850G33DRCR	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850GA
TPS3850G33DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850GA
TPS3850G33DRCT	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850GA
TPS3850G33DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850GA
TPS3850G50DRCR	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850HA
TPS3850G50DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850HA
TPS3850G50DRCT	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850HA
TPS3850G50DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850HA
TPS3850H01DRCR	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850AA
TPS3850H01DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850AA
TPS3850H01DRCT	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850AA
TPS3850H01DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850AA
TPS3850H12DRCR	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850KA
TPS3850H12DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850KA
TPS3850H12DRCT	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850KA
TPS3850H12DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850KA
TPS3850H18DRCR	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850LA



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Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
TPS3850H18DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850LA
TPS3850H18DRCT	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850LA
TPS3850H18DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850LA
TPS3850H30DRCR	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850NA
TPS3850H30DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850NA
TPS3850H30DRCT	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850NA
TPS3850H30DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850NA
TPS3850H33DRCR	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850PA
TPS3850H33DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850PA
TPS3850H33DRCT	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850PA
TPS3850H33DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850PA
TPS3850H50DRCR	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850RA
TPS3850H50DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	850RA
TPS3850H50DRCT	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850RA
TPS3850H50DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	850RA

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE OPTION ADDENDUM**

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF TPS3850:

Automotive: TPS3850-Q1

NOTE: Qualified Version Definitions:

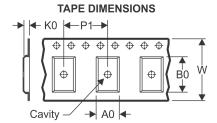
Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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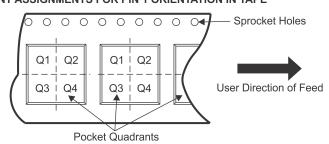
### TAPE AND REEL INFORMATION





	Α0	Dimension designed to accommodate the component width
	B0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
г	D1	Pitch between successive cavity centers

# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

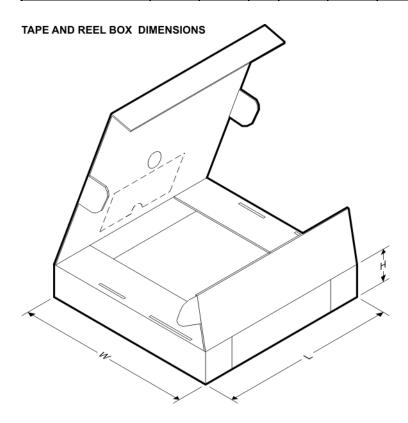
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3850G12DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G12DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G18DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G18DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G30DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G30DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G33DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G33DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G50DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850G50DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H01DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H01DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H12DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H12DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H18DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H18DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H30DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H30DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2





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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3850H33DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H33DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H50DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3850H50DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3850G12DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850G12DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS3850G18DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850G18DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS3850G30DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850G30DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS3850G33DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850G33DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS3850G50DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850G50DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS3850H01DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H01DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS3850H12DRCR	VSON	DRC	10	3000	367.0	367.0	35.0



# **PACKAGE MATERIALS INFORMATION**

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3850H12DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS3850H18DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H18DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS3850H30DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H30DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS3850H33DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H33DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS3850H50DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS3850H50DRCT	VSON	DRC	10	250	210.0	185.0	35.0

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC SMALL OUTLINE - NO LEAD



### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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