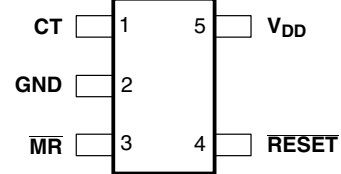


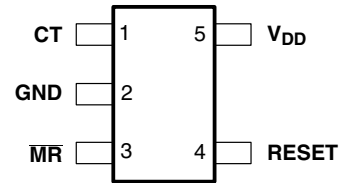
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Supply Current of 220 nA (Typ)
- Precision Supply Voltage Supervision Range: 1.8 V, 2.5 V, 3.0 V, 3.3 V
- Power-On Reset Generator With Selectable Delay Time of 10 ms or 200 ms
- Push/Pull $\overline{\text{RESET}}$ Output (TPS3836), RESET Output (TPS3837), or Open-Drain $\overline{\text{RESET}}$ Output (TPS3838)
- Manual Reset
- 5-Pin SOT-23 Package
- Temperature Range: -40°C to 125°C

- Applications Include
 - Applications Using Automotive Low-Power DSPs, Microcontrollers, or Microprocessors
 - Battery-Powered Equipment
 - Intelligent Instruments
 - Wireless Communication Systems
 - Automotive Systems

TPS3836, TPS3838
 DBV PACKAGE
 (TOP VIEW)



TPS3837
 DBV PACKAGE
 (TOP VIEW)



description

The TPS3836, TPS3837, TPS3838 families of supervisory circuits provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage V_{IT} . An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after V_{DD} has risen above the threshold voltage V_{IT} .

When CT is connected to GND a fixed delay time of typical 10 ms is asserted. When connected to V_{DD} the delay time is typically 200 ms.

When the supply voltage drops below the threshold voltage V_{IT} , the output becomes active (low) again.

All the devices of this family have a fixed-sense threshold voltage V_{IT} set by an internal voltage divider.

The TPS3836 has an active-low push-pull $\overline{\text{RESET}}$ output. The TPS3837 has active-high push-pull RESET, and TPS3838 integrates an active-low open-drain $\overline{\text{RESET}}$ output.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
 INSTRUMENTS**

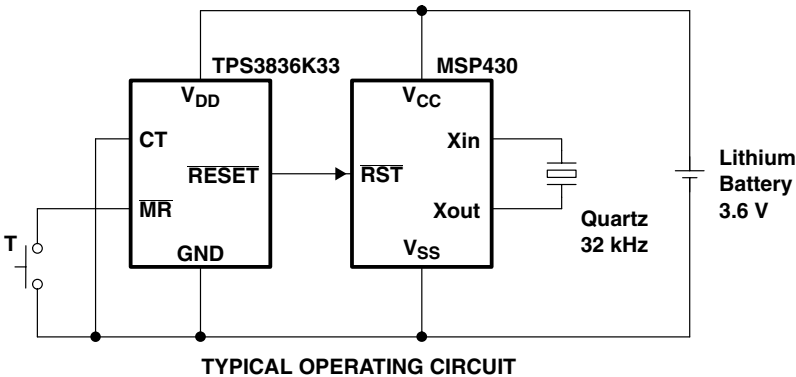
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TPS3836E18-Q1 / J25-Q1 / H30-Q1 / L30-Q1 / K33-Q1
 TPS3837E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1, TPS3838E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1
 NANOPOWER SUPERVISORY CIRCUITS

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description (continued)



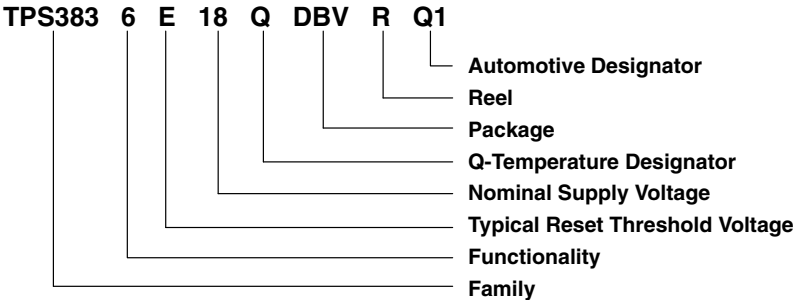
The product spectrum is designed for supply voltages of 1.8 V, 2.5 V, 3 V, and 3.3 V. The circuits are available in a 5-pin SOT-23 package. The TPS3836-Q-Q1, TPS3837-Q-Q1, TPS3838-Q-Q1 families are characterized for operation over a temperature range of –40°C to 125°C.

PACKAGE INFORMATION

T _A	DEVICE NAME	THRESHOLD VOLTAGE	SYMBOL
–40°C to 125°C	TPS3836E18QDBVRQ1†	1.71 V	PDNQ
	TPS3836J25QDBVRQ1†	2.25 V	PDSQ
	TPS3836H30QDBVRQ1†	2.79 V	PHRQ
	TPS3836L30QDBVRQ1†	2.64 V	PCAQ
	TPS3836K33QDBVRQ1†	2.93 V	PDTQ
	TPS3837E18QDBVRQ1†	1.71 V	PDOQ
	TPS3837J25QDBVRQ1†	2.25 V	PDRQ
	TPS3837L30QDBVRQ1†	2.64 V	PCBQ
	TPS3837K33QDBVRQ1†	2.93 V	PDUQ
	TPS3838E18QDBVRQ1†	1.71 V	PDQQ
	TPS3838J25QDBVRQ1†	2.25 V	PDPQ
	TPS3838L30QDBVRQ1†	2.64 V	PCCQ
	TPS3838K33QDBVRQ1†	2.93 V	PDVQ

† DBVR indicates tape and reel of 3000 parts.

ORDERING INFORMATION

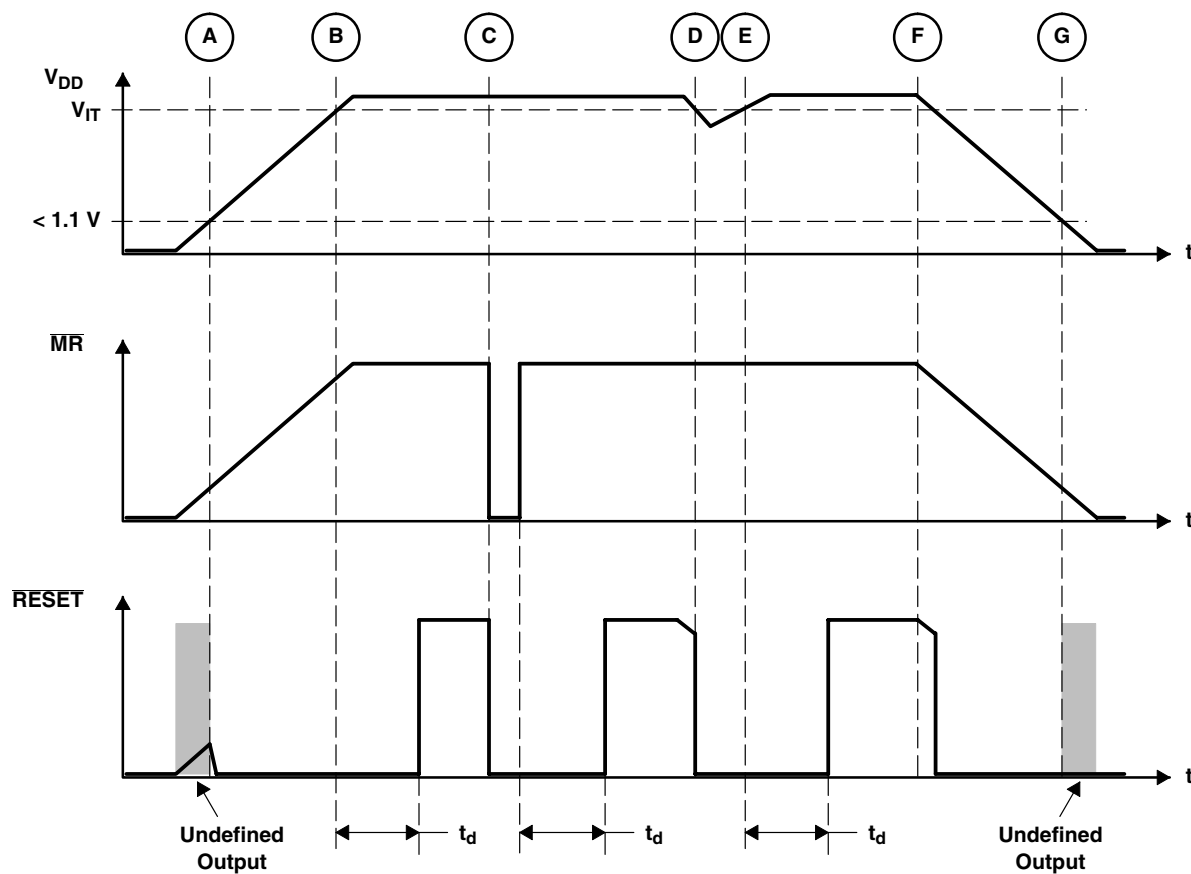


MR	$V_{DD} > V_{IT}$	RESET [†]	RESET [‡]
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

‡ TPS3837

The schematic diagram illustrates the reset circuit for the TPS3836. It features a Band-Gap Reference connected to a network of resistors (R1, R2, R3) and capacitors (C1, C2, C3). The MR pin is connected to this network. The output of the reset logic is connected to the Reset pin (TPS3836-Push-Pull) and the Reset pin (TPS3838-Open-Drain). The Refresh Timer is connected to the Refresh pin (TPS3836-Open-Drain).

timing diagram



TPS3836E18-Q1 / J25-Q1 / H30-Q1 / L30-Q1 / K33-Q1
TPS3837E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1, TPS3838E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1
NANOPOWER SUPERVISORY CIRCUITS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	7 V
All other pins (see Note 1)	–0.3 V to 7 V
Maximum low output current, I_{OL}	5 mA
Maximum high output current, I_{OH}	–5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Soldering temperature	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation, the device must not be operated at 7 V for more than $t=1000$ h continuously

DISSIPATION RATING TABLE

PACKAGE	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW	87 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.6	6	V
Input voltage, V_I	0	$V_{DD} + 0.3$	V
High-level input voltage, V_{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage, V_{IL}		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$		100	ns/V
Operating free-air temperature range, T_A	–40	125	°C



electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITION		MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	RESET (TPS3836)	V _{DD} = 3.3 V,	I _{OH} = −2 mA	0.8 × V _{DD}			V
			V _{DD} = 6 V,	I _{OH} = −3 mA				
		RESET (TPS3837)	V _{DD} = 1.8 V,	I _{OH} = −1 mA				
			V _{DD} = 3.3 V,	I _{OL} = −2 mA				
V _{OL}	Low-level output voltage	RESET (TPS3836/8)	V _{DD} = 1.8 V,	I _{OL} = 1 mA			0.4	V
			V _{DD} = 3.3 V,	I _{OL} = 2 mA				
		RESET (TPS3837)	V _{DD} = 3.3 V,	I _{OL} = 2 mA				
			V _{DD} = 6 V,	I _{OL} = 3 mA				
	Power-up reset voltage (see Note 2)	TPS3836/8	V _{DD} ≥ 1.1 V,	I _{OL} = 50 μA			0.2	V
		TPS3837	V _{DD} ≥ 1.1 V,	I _{OH} = −50 μA	0.8 × V _{DD}			
V _{IT}	Negative-going input threshold voltage (see Note 3)	TPS383xE18			1.64	1.71	1.76	V
		TPS383xJ25			2.16	2.25	2.30	
		TPS383xH30			2.70	2.79	2.85	
		TPS383xL30			2.54	2.64	2.71	
		TPS383xK33			2.82	2.93	3.10	
V _{hys}	Hysteresis at V _{DD} input	1.7 V < V _{IT} < 2.5 V		30			mV	
		2.5 V < V _{IT} < 3.5 V		40				
		3.5 V < V _{IT} < 5 V		50				
I _{IH}	High-level input current	MR (see Note 4)	MR = 0.7 × V _{DD} ,	V _{DD} = 6 V	−40	−60	−100	μA
		CT	CT = V _{DD} = 6 V		−25		25	nA
I _{IL}	Low-level input current	MR (see Note 4)	MR = 0 V,	V _{DD} = 6 V	−130	−200	−340	μA
		CT	CT = 0 V,		−25		25	nA
I _{OH}	High-level output current	TPS3838	V _{DD} = V _{IT} + 0.2 V,	V _{OH} = V _{DD}			25	nA
I _{DD}	Supply current	V _{DD} > V _{IT} ,		V _{DD} < 3 V	220	500	nA	
		V _{DD} > V _{IT} ,		V _{DD} > 3 V	250	550		
		V _{DD} < V _{IT}			10	25	μA	
Internal pullup resistor at MR					30			kΩ
C _I	Input capacitance at MR, CT		V _I = 0 V to V _{DD}		5			pF

NOTES: 2. The lowest voltage at which RESET output becomes active. t_r , $V_{DD} \geq 15\text{ }\mu\text{s/V}$

3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, $0.1\text{ }\mu\text{F}$) should be placed near the supply terminal.

4. If manual reset is unused, MR should be connected to V_{DD} to minimize current consumption.

TPS3836E18-Q1 / J25-Q1 / H30-Q1 / L30-Q1 / K33-Q1
TPS3837E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1, TPS3838E18-Q1 / J25-Q1 / L30-Q1 / K33-Q1
NANOPOWER SUPERVISORY CIRCUITS

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timing requirements at $R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	at V_{DD} $V_{IH} = V_{IT} + 0.2\text{ V}$, $V_{IL} = V_{IT} - 0.2\text{ V}$	6			μs
		at $\overline{\text{MR}}$ $V_{DD} \geq V_{IT} + 0.2\text{ V}$, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	1			μs

switching characteristics at $R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time	$V_{DD} \geq V_{IT} + 0.2\text{ V}$, $\overline{\text{MR}} = 0.7 \times V_{DD}$, $\text{CT} = \text{GND}$, See timing diagram	5	10	15	ms
		$V_{DD} \geq V_{IT} + 0.2\text{ V}$, $\overline{\text{MR}} = 0.7 \times V_{DD}$, $\text{CT} = V_{DD}$, See timing diagram	100	200	300	
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to RESET delay (TPS3836, TPS3838) $V_{IL} = V_{IT} - 0.2\text{ V}$, $V_{IH} = V_{IT} + 0.2\text{ V}$			10	μs
		$V_{IL} = 1.6\text{ V}$			50	
t_{PLH}	Propagation (delay) time, low-to-high-level output	V_{DD} to RESET delay (TPS3837) $V_{IL} = V_{IT} - 0.2\text{ V}$, $V_{IH} = V_{IT} + 0.2\text{ V}$			10	μs
		$V_{IL} = 1.6\text{ V}$			50	
t_{PHL}	Propagation (delay) time, high-to-low-level output	$\overline{\text{MR}}$ to RESET delay (TPS3836, TPS3838) $V_{DD} \geq V_{IT} + 0.2\text{ V}$, $V_{IL} = 0.3 \times V_{DD}$			0.1	μs
t_{PLH}	Propagation (delay) time, low-to-high-level output	$\overline{\text{MR}}$ to RESET delay (TPS3837) $V_{IL} = 0.7 \times V_{DD}$			0.1	μs

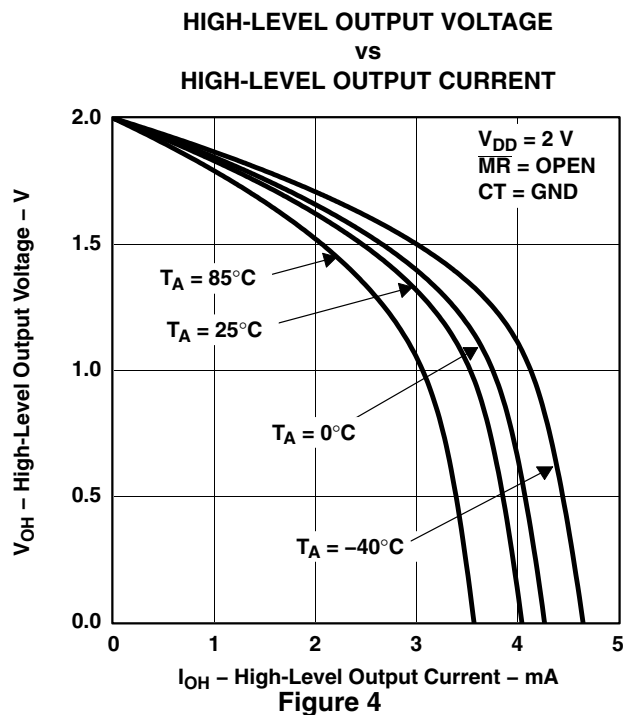
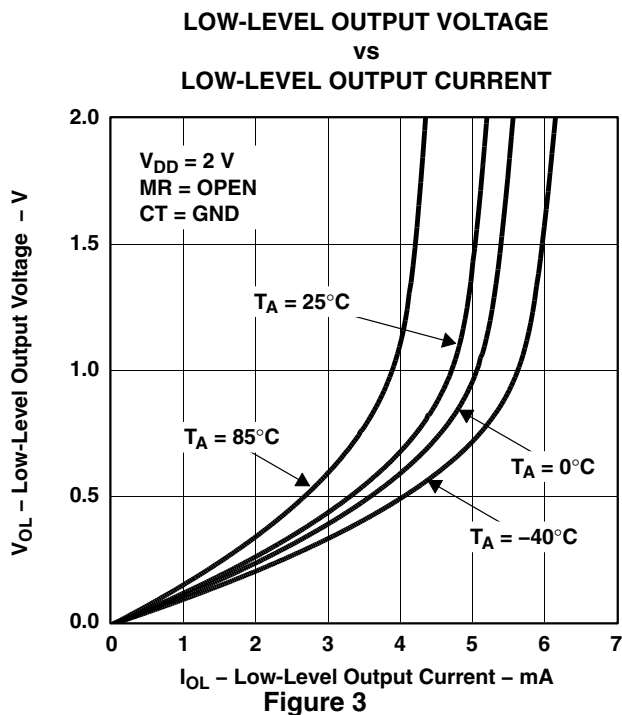
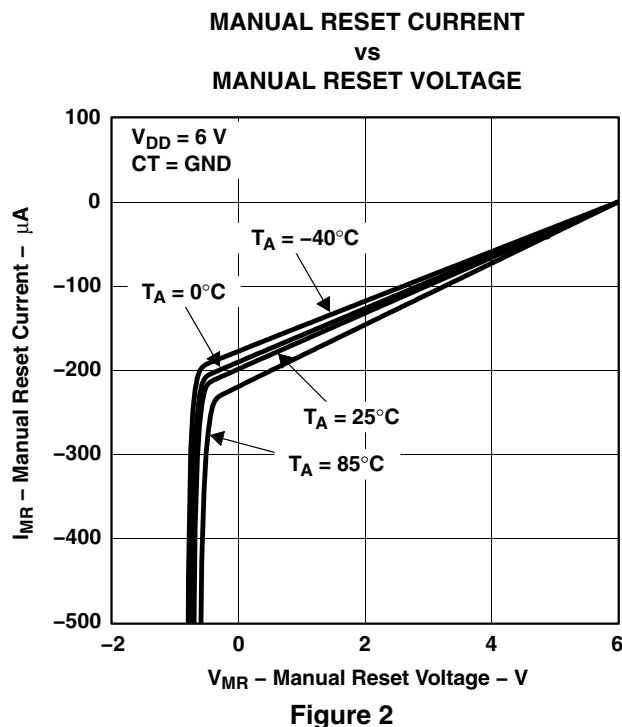
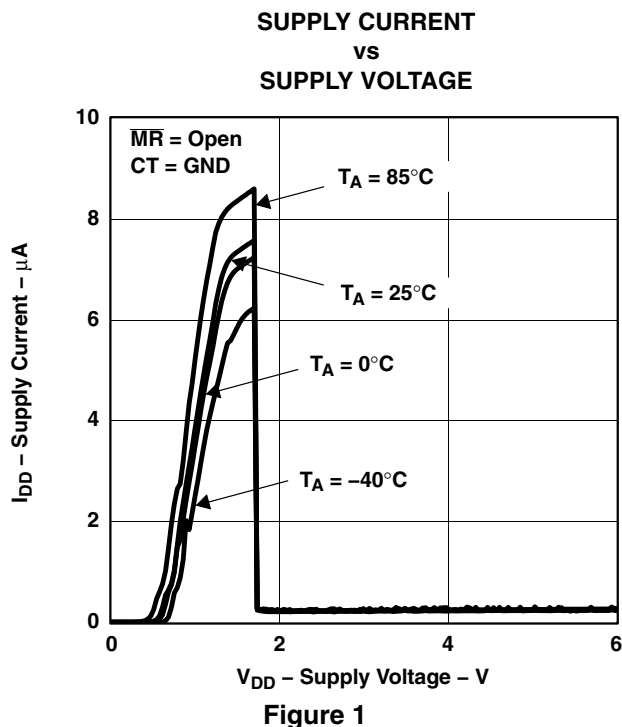
TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{DD}	Supply current	vs Supply voltage	1
I_{MR}	Manual reset current	vs Manual reset voltage	2
V_{OL}	Low-level output voltage	vs Low-level output current	3
V_{OH}	High-level output voltage	vs High-level output current	4
	Normalized reset threshold voltage	vs Free-air temperature	5
	Minimum pulse duration at V_{DD}	vs V_{DD} Threshold overdrive	6



TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

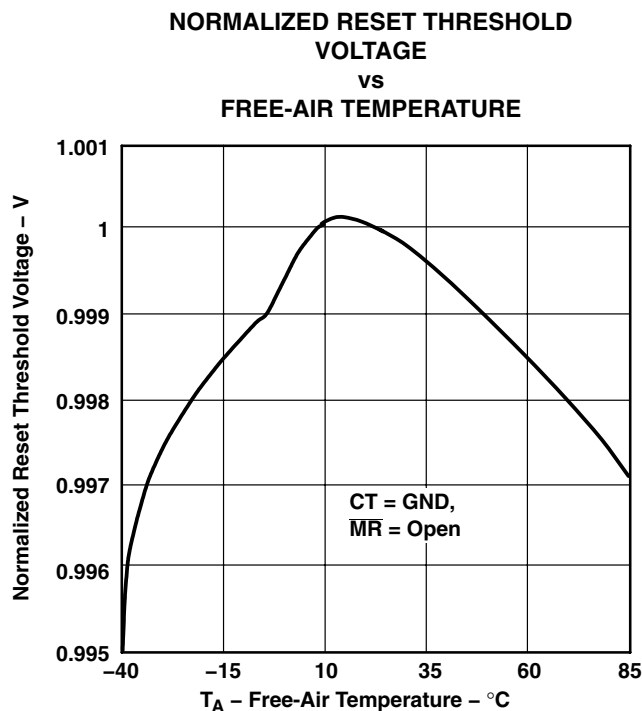


Figure 5

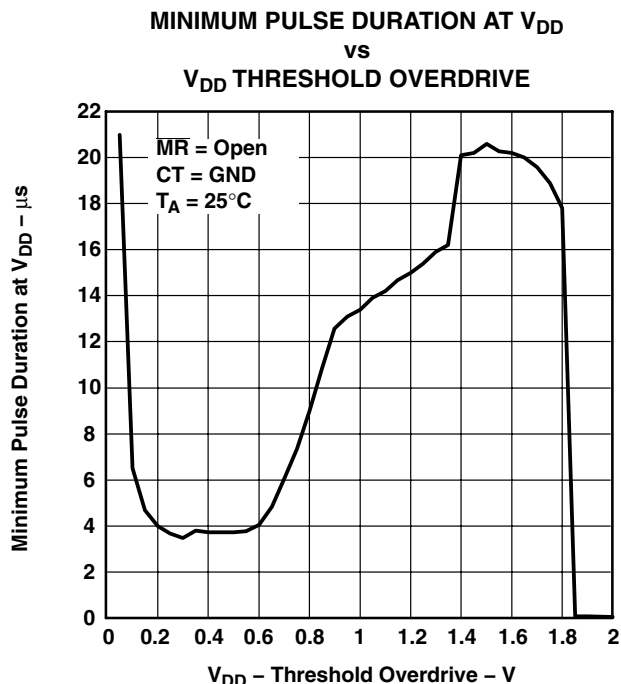


Figure 6

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3836J25QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	PDSQ
TPS3836J25QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PDSQ
TPS3836K33QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PDTQ
TPS3836K33QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PDTQ
TPS3836L30QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	PCAQ
TPS3836L30QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PCAQ
TPS3838K33QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	PDVQ
TPS3838K33QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PDVQ
TPS3838K33QDBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PDVQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS3836-Q1, TPS3838-Q1 :

- Catalog : [TPS3836](#), [TPS3838](#)
- Enhanced Product : [TPS3836-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3836J25QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3836J25QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3836K33QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3836L30QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS3836L30QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3838K33QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

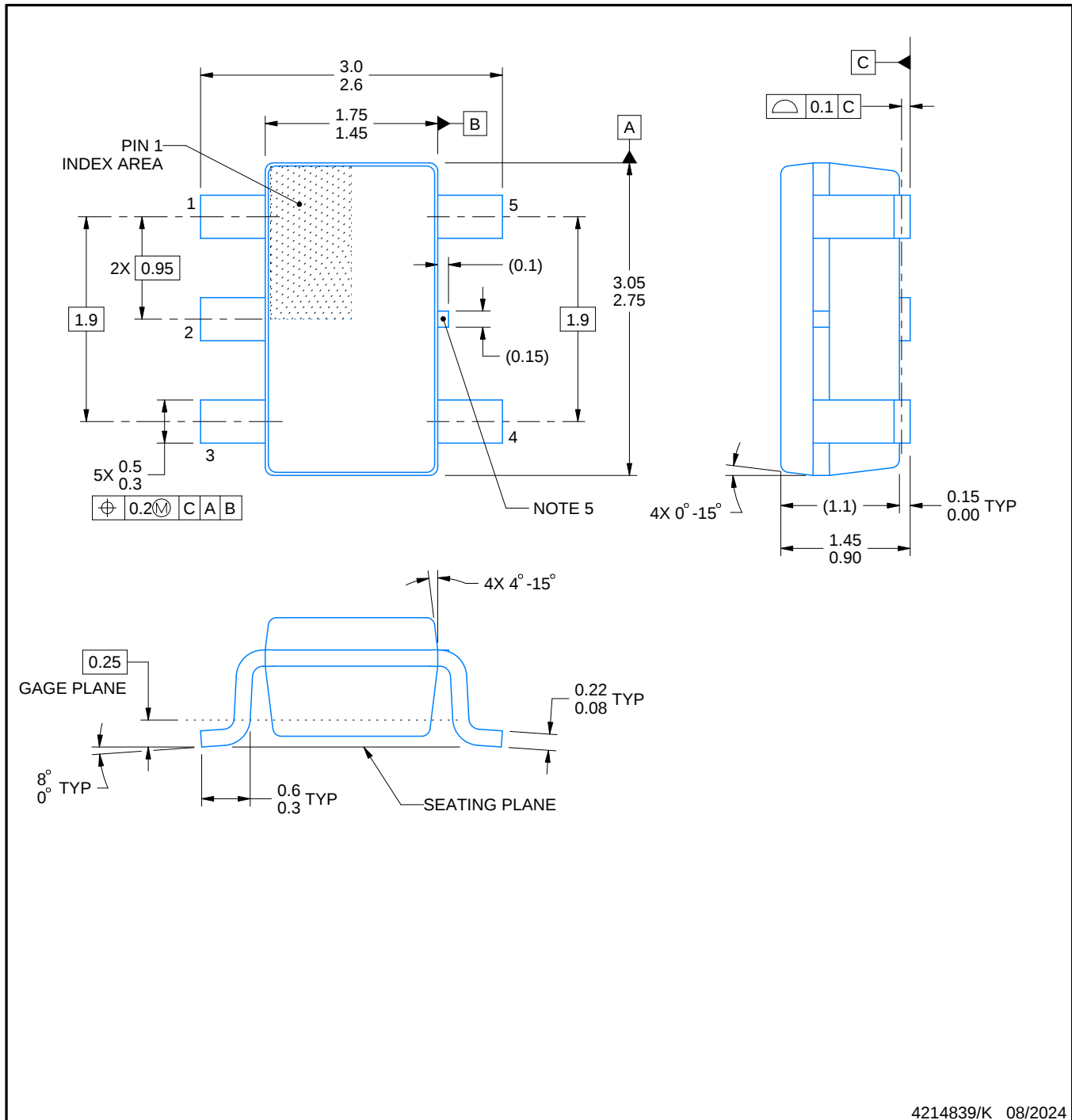


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3836J25QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3836J25QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3836K33QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3836L30QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS3836L30QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3838K33QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR

**NOTES:**

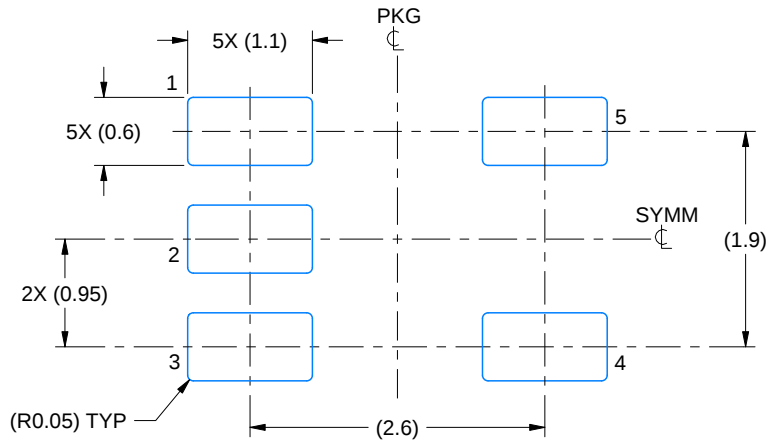
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

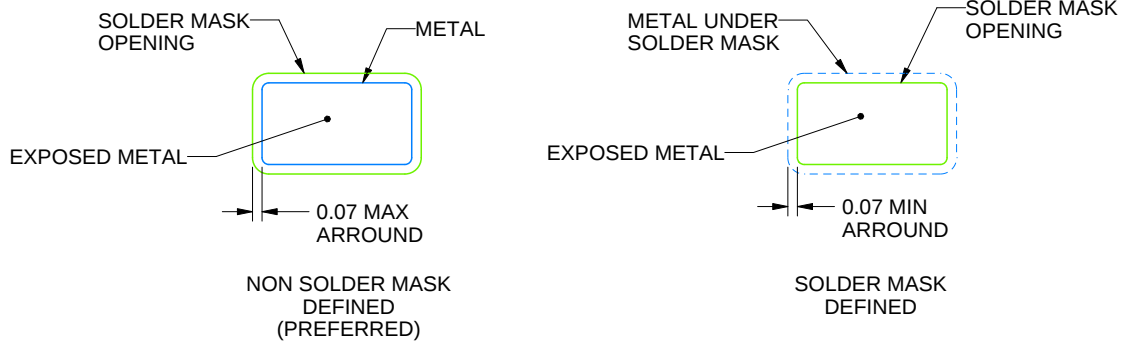
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

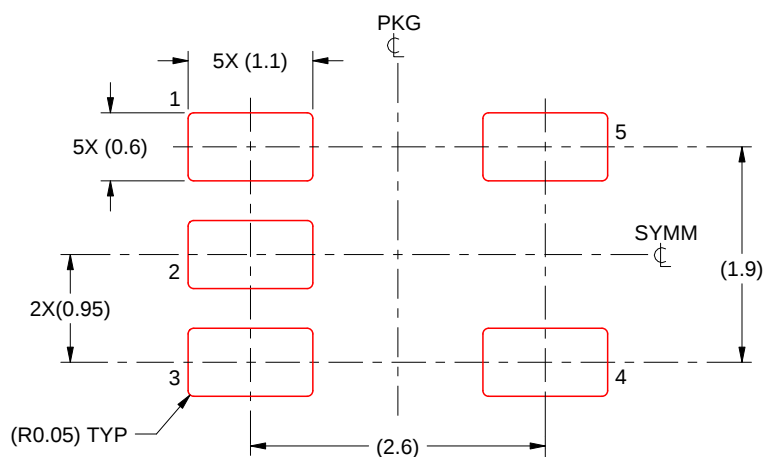
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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