

TPS3762 65 V Window (OV & UV) Supervisor with Built-In Self-Test and Latch

1 Features

- SIL-3 Functional Safety-compliant product targeted
 - Documentation to aid IEC 61508 system design
 - Systematic capability up to SIL-3 targeted
 - Hardware capability up to SIL-3 targeted
- Device flexibility to meet design requirements
 - Wide voltage threshold range: 2.7 V to 60 V
 - 800mV option - use with external resistor divider to set threshold
 - Built-in hysteresis (2 %, 5 %, and 10 % options)
 - Fixed and programmable reset time delay
 - Fixed and programmable detection delay
- Monitor high voltage power rails
 - Wide input voltage range: 2.7 V to 65 V
 - Reverse polarity protection on sense pin -65 V
 - No external components required to power off of high voltage rail
- Fast UV/OV protection in 12/24/48 V systems
 - Output reset latching feature
 - Ultra-fast detection time delay option(<5 μ s)
 - Built-In Self-Test

2 Applications

- [Single & Multiaxis Servo Drive](#)
- [Industrial & Collaborative Robot](#)
- [Avionics](#)
- [PLC, DCS & PAC](#)

3 Description

The TPS3762 is a 65 V input voltage supervisor with 4 μ A I_{DD} , 0.9% accuracy, fast detection time, and a Built-In Self-Test feature. This device can be connected directly to 12 V / 24 V industrial SELV power rails for continuous monitoring of overvoltage (OV) and undervoltage (UV) conditions; with its internal resistor divider, TPS3762 offers the smallest total solution size. Wide hysteresis voltage options are available to ignore large voltage transients. Built-in hysteresis on the SENSE pin prevents false reset signals when monitoring a supply voltage rail.

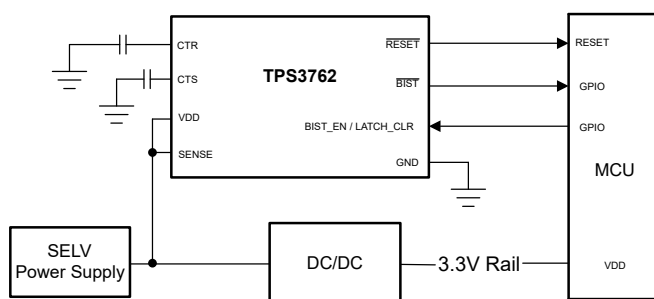
The separate VDD and SENSE pins allow redundancy sought by high-reliability systems and SENSE can monitor higher and lower voltages than VDD. Optional use of external resistors are supported by the high impedance input of the SENSE pin. CTS and CTR pins allow delay adjustability on the falling and rising edges of the RESET signal. The CTS functions as a debouncer by ignoring voltage glitches on the monitored voltage rails.

The TPS3762 is available in a 2.9 mm $\times$ 1.6 mm SOT23 8-pin package. TPS3762 operates over -40°C to +150°C T_A .

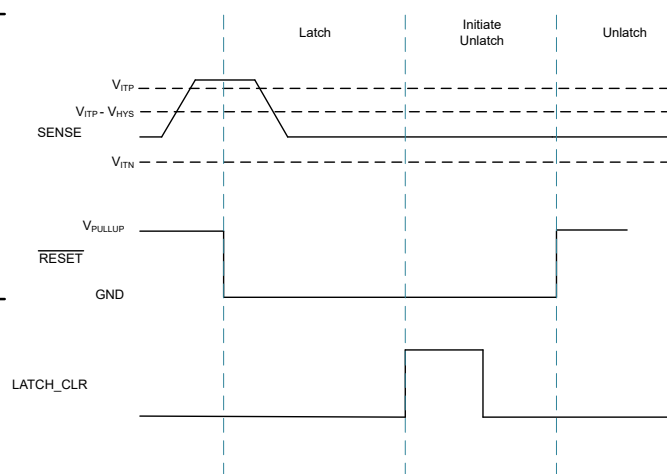
Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
TPS3762	SOT-23 (8) (DDF)	2.9 mm x 1.6 mm

(1) For package details, see the mechanical drawing addendum at the end of the data sheet.



Typical Application Circuit



Latch Functionality Waveform



Table of Contents

1 Features	1	7.3 Feature Description.....	15
2 Applications	1	7.4 Device Functional Modes.....	26
3 Description	1	8 Application and Implementation	27
4 Device Comparison	3	8.1 Application Information.....	27
5 Pin Configuration and Functions	4	8.2 Adjustable Voltage Thresholds.....	27
6 Specifications	5	8.3 Typical Application.....	28
6.1 Specifications.....	5	8.4 Power Supply Recommendations.....	32
6.2 Absolute Maximum Ratings.....	5	8.5 Layout.....	32
6.3 Recommended Operating Conditions.....	5	9 Device and Documentation Support	34
6.4 Thermal Information	5	9.1 Device Nomenclature.....	34
6.5 Electrical Characteristics.....	6	9.2 Receiving Notification of Documentation Updates....	34
6.6 Switching Requirements.....	8	9.3 Support Resources.....	34
6.7 Timing Requirements.....	9	9.4 Trademarks.....	34
6.8 Timing Diagrams	10	9.5 Electrostatic Discharge Caution.....	34
6.9 Typical Characteristic.....	12	9.6 Glossary.....	34
7 Detailed Description	14	10 Revision History	34
7.1 Overview.....	14	11 Mechanical, Packaging, and Orderable Information	34
7.2 Functional Block Diagram.....	14		

4 Device Comparison

Device Decoder shows some of the device naming nomenclature of the TPS3762. Not all device namings will follow this nomenclature table. For a detailed breakdown of every device part number by threshold voltage options, BIST configurations, Latch configurations, CTR options, CTS options, and UVbypass, see [Section 9.1](#) for more details. Contact TI sales representatives or on [TI's E2E forum](#) for detail and availability of other options.

Overvoltage Undervoltage
VITP VITN

TPS3762 X XX XX XXX X

Topology				
Suffix	CTR	CTS	Latch / UV Bypass	BIST RESET Trigger
A	ADJ	ADJ	Disabled	Yes
B	ADJ	ADJ	Latch	Yes
C	ADJ	ADJ	UVBypass	Yes
D	ADJ	ADJ	Both	Yes
E	ADJ	5 μ s	Disabled	Yes
F	ADJ	5 μ s	Latch	Yes
G	ADJ	5 μ s	UVBypass	Yes
H	ADJ	5 μ s	Both	Yes
I	ADJ	ADJ	Disabled	No
J	ADJ	ADJ	Latch	No
K	ADJ	ADJ	UVBypass	No
L	ADJ	ADJ	Both	No
M	ADJ	5 μ s	Disabled	No
N	ADJ	5 μ s	Latch	No
O	ADJ	5 μ s	UVBypass	No
P	ADJ	5 μ s	Both	No
Q	200ms	5 μ s	Disabled	Yes
R	200ms	5 μ s	Latch	Yes

Threshold Voltage			
2% Hysteresis Option			
Suffix	VIT	Suffix	VIT
02	800mV	D7	8.5V
A7	2.7V	D8	9V
A8	2.8V	D9	9.5V
A9	2.9V	E0	10V
B0	3V	E1	11V
B1	3.1V	E2	12V
B2	3.2V	E3	13V
B3	3.3V	E4	14V
B4	3.4V	E5	15V
B5	3.5V	E6	16V
B6	3.6V	E7	17V
B7	3.7V	E8	18V
B8	3.8V	E9	20V
B9	3.9V	F0	22V
C0	4V	F1	24V
C1	4.1V	F2	26V
C2	4.2V	F3	28V
C3	4.3V	F4	30V
C4	4.4V	F5	32V
C5	4.5V	F6	34V
C6	4.6V	F7	36V
C7	4.7V	F8	38V
C8	4.8V	F9	40V
C9	4.9V	G0	42V
D0	5V	G1	46V
D1	5.5V	G2	48V
D2	6V	G3	50V
D3	6.5V	G4	54V
D4	7V	G5	57V
D5	7.5V	G6	58V
D6	8V	G7	60V
W7	+/-7%		
UV	UV Only	OV	OV Only

Threshold Voltage			
5% Hysteresis Option			
Suffix	VIT	Suffix	VIT
05	800mV	K7	8.5V
H7	2.7V	K8	9V
H8	2.8V	K9	9.5V
H9	2.9V	L0	10V
I0	3V	L1	11V
I1	3.1V	L2	12V
I2	3.2V	L3	13V
I3	3.3V	L4	14V
I4	3.4V	L5	15V
I5	3.5V	L6	16V
I6	3.6V	L7	17V
I7	3.7V	L8	18V
I8	3.8V	L9	20V
I9	3.9V	M0	22V
J0	4V	M1	24V
J1	4.1V	M2	26V
J2	4.2V	M3	28V
J3	4.3V	M4	30V
J4	4.4V	M5	32V
J5	4.5V	M6	34V
J6	4.6V	M7	36V
J7	4.7V	M8	38V
J8	4.8V	M9	40V
J9	4.9V	N0	42V
K0	5V	N1	46V
K1	5.5V	N2	48V
K2	6V	N3	50V
K3	6.5V	N4	54V
K4	7V	N5	57V
K5	7.5V	N6	58V
K6	8V	N7	60V

Package	
Suffix	Name
DDF	SOT-23

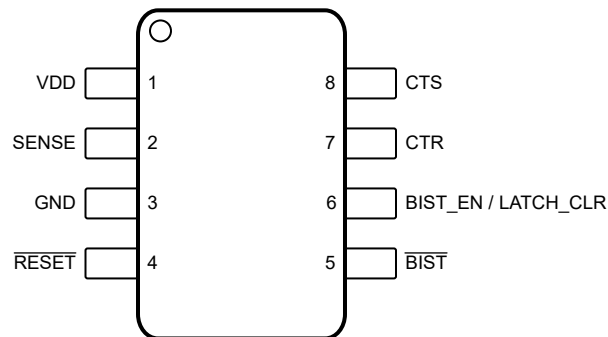
Reel	
Suffix	Name
R	Large

10% Hysteresis Option			
Suffix	VIT	Suffix	VIT
10	800mV	Q1	4.1V
O7	2.7V	Q2	4.2V
O8	2.8V	Q3	4.3V
O9	2.9V	Q4	4.4V
P0	3V	Q5	4.5V
P1	3.1V	Q6	4.6V
P2	3.2V	Q7	4.7V
P3	3.3V	Q8	4.8V
P4	3.4V	Q9	4.9V
P5	3.5V	R0	5V
P6	3.6V	R1	5.5V
P7	3.7V	R2	6V
P8	3.8V	R3	6.5V
P9	3.9V	R4	7V
Q0	4V	R5	7.5V

10% Hysteresis Option			
Suffix	VIT	Suffix	VIT
R6	8V	T2	26V
R7	8.5V	T3	28V
R8	9V	T4	30V
R9	9.5V	T5	32V
S0	10V	T6	34V
S1	11V	T7	36V
S2	12V	T8	38V
S3	13V	T9	40V
S4	14V	U0	42V
S5	15V	U1	46V
S6	16V	U2	48V
S7	17V	U3	50V
S8	18V	U4	54V
S9	20V	U5	57V
T0	22V	U6	58V
T1	24V	U7	60V

- Suffix 02, 05, and 10 with VIT of 800mV corresponds to the adjustable variant, do not have internal voltage divider
- Not all TPS3762 devices can be decoded by this table. Refer to [Section 9.1](#) for a decoding table by part number.

5 Pin Configuration and Functions



**Figure 5-1. DDF Package,
8-Pin SOT-23,
TPS3762 (Top View)**

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1	I	Input Supply Voltage: Supply voltage pin. For noisy systems, bypass with a 0.1 μ F capacitor to GND.
SENSE	2	I	Sense Voltage: Connect this pin to the supply rail that must be monitored. See SENSE for more details. Sensing Topology: Overvoltage (OV), Undervoltage (UV), or Window (OV + UV)
GND	3	-	Ground. Ground pin. All GND pins must be electrically connected to the board ground.
RESET	4	O	Output Reset Signal: RESET asserts when SENSE crosses the voltage threshold after the sense time delay, set by CTS and remains asserted for the reset time delay period after SENSE transitions out of a fault condition. For latch variants RESET remains asserted until the latch is cleared. The active low open-drain reset output requires an external pullup resistor. See Section 7.3.3 for more details. Output topology: Open-Drain Active-Low
BIST	5	O	Built-In Self-Test: BIST asserts when a logic high input occurs on the BIST_EN / LATCH_CLR or BIST_EN pin, this initiates the internal BIST testing. BIST recovers after t_{BIST} to signify BIST completed successfully. BIST will remain asserted for a time period longer than t_{BIST} if there is a failure during BIST. BIST active-low open-drain output requires an external pullup resistor. See Section 7.3.6 for more details.
BIST_EN / LATCH_CLR	6	I	Built-In Self-Test Enable and Latch Clear: A logic high input must occur on the BIST_EN / LATCH_CLR to initiate BIST and clear a latched OV/UV fault. See Section 7.3.6 and Section 7.3.3.3 for more details.
CTR	7	O	RESET Time Delay: User-programmable reset time delay for RESET. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Section 7.3.4 for more details.
CTS	8	O	SENSE Time Delay: User-programmable sense time delay for SENSE. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Section 7.3.5 for more details.

6 Specifications

6.1 Specifications

6.2 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted ⁽¹⁾

		MIN	MAX	UNIT
Voltage	V_{DD} , $V_{SENSE(Adjustable)}$, V_{RESET}	−0.3	70	V
Voltage	$V_{SENSE(Fixed)}$	−65	70	V
Voltage	V_{CTS} , V_{CTR}	−0.3	6	V
Voltage	V_{BIST} , V_{BIST_EN} , $V_{BIST_EN/LATCH_CLR}$	−0.3	6	V
Current	I_{RESET} , I_{BIST}		10	mA
Temperature ⁽²⁾	Operating junction temperature, T_J	−40	150	°C
Temperature ⁽²⁾	Operating Ambient temperature, T_A	−40	150	°C
Temperature ⁽²⁾	Storage, T_{stg}	−65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	V_{DD}	2.7		65	V
Voltage	V_{SENSE} , V_{RESET}	0		65	V
Voltage	V_{CTS} , V_{CTR}	0		5.5	V
Voltage	V_{BIST} , V_{BIST_EN} , $V_{BIST_EN/LATCH_CLR}$	0		5.5	V
Current	I_{RESET} , I_{BIST}	0		5	mA
T_J ⁽¹⁾	Junction temperature (free air temperature)	−40		125	°C

- (1) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3762	UNIT
		DDF	
		8-PIN	
R _{θJA}	Junction-to-ambient thermal resistance	154.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	77.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	73.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	4.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	72.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, CTR = CTS = open, output $\overline{\text{RESET}}$ pull-up resistor $R_{PU} = 10 \text{ k}\Omega$, voltage $V_{PU} = 5.5 \text{ V}$, output $\overline{\text{BIST}}$ pull-up resistor $R_{PU \text{ BIST}} = 10 \text{ k}\Omega$, voltage $V_{PU \text{ BIST}} = 5.5 \text{ V}$, and load $C_{LOAD} = 10 \text{ pF}$. The operating free-air temperature range $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$ and $V_{DD} = 12 \text{ V}$ and $V_{IT} = 6.5 \text{ V}$ (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
POWER SUPPLY						
V _{DD}	Supply Voltage		2.7	65	V	
UVLO ⁽¹⁾	Undervoltage Lockout	V _{DD} rising above V _{DD (MIN)}		2.6	V	
UVLO(HYS) ⁽¹⁾	Undervoltage Lockout Hysteresis	V _{DD} falling below V _{DD (MIN)}	500		mV	
V _{POR(RESET)}	Power on Reset Voltage ⁽²⁾ RESET, Active Low (Open-Drain)	V _{OL(MAX)} = 300 mV I _{OUT (Sink)} = 15 μA		1.4	V	
V _{POR(BIST)}	Power on Reset Voltage ⁽²⁾ BIST, Active Low (Open-Drain)	V _{OL(MAX)} = 300 mV I _{OUT (Sink)} = 15 μA		1.4	V	
I _{DD}	Supply current into V _{DD} pin	V _{IT} = 800 mV V _{DD (MIN)} ≤ V _{DD} ≤ V _{DD (MAX)}	4	8.1	μA	
SENSE (Input)						
I _{SENSE}	Input current	V _{IT} = 800 mV		200	nA	
V _{ITN}	Input Threshold Negative (Undervoltage)	V _{IT} = 800 mV ⁽³⁾	-0.9	0.9	%	
V _{ITP}	Input Threshold Positive (Overvoltage)	V _{IT} = 800 mV ⁽³⁾	-0.9	0.9	%	
V _{HYS}	Hysteresis Accuracy ⁽⁴⁾	V _{IT} = 0.8 V V _{HYS} Range = 2%	1.5	2	2.5	%
RESET (Output)						
I _{lkg(OD)}	Open-Drain leakage	V _{RESET} = 5.5 V V _{ITN} < V _{SENSE} < V _{ITP}		300	nA	
I _{lkg(OD)}	Open-Drain leakage	V _{RESET} = 65 V V _{ITN} < V _{SENSE} < V _{ITP}		300	nA	
V _{OL} ⁽⁵⁾	Low level output voltage	2.7 V ≤ V _{DD} ≤ 65 V I _{RESET} = 2.7 mA		350	mV	

6.5 Electrical Characteristics (continued)

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, CTR = CTS = open, output $\overline{RESET}$ pull-up resistor $R_{PU} = 10\text{ k}\Omega$, voltage $V_{PU} = 5.5\text{ V}$, output BIST pull-up resistor $R_{PU_BIST} = 10\text{ k}\Omega$, voltage $V_{PU_BIST} = 5.5\text{ V}$, and load $C_{LOAD} = 10\text{ pF}$. The operating free-air temperature range $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$ and $V_{DD} = 12\text{ V}$ and $V_{IT} = 6.5\text{ V}$ (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitor Timing (CTS, CTR)						
R_{CTR}	Internal resistance (CTR)		3.2	4	4.8	$\text{M}\Omega$
R_{CTS}	Internal resistance (CTS)		3.2	4	4.8	$\text{M}\Omega$
Built-in Self-test						
$I_{kg(BIST)}$	Open-Drain leakage	$V_{BIST} = 5.5\text{ V}$ $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
$I_{kg(BIST)}$	Open-Drain leakage	$V_{BIST} = 3.3\text{ V}$ $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
V_{BIST_OL}	Low level output voltage	$2.7\text{ V} \leq V_{DD} \leq 65\text{ V}$ $I_{BIST} = 5\text{ mA}$			300	mV
V_{BIST_EN}	BIST_EN pin logic low input				500	mV
V_{BIST_EN}	BIST_EN pin logic high input		1300			mV
$V_{BIST_EN}/$ $LATCH_CLR$	LATCH_CLR pin logic low input				500	mV
$V_{BIST_EN}/$ $LATCH_CLR$	LATCH_CLR pin logic high input		1300			mV

- (1) When V_{DD} voltage falls below UVLO, $\overline{RESET}$ is asserted. V_{DD} slew rate $\leq 100\text{ mV} / \mu\text{s}$
- (2) V_{POR} is the minimum V_{DD} voltage for a controlled output state. Below V_{POR} , the output cannot be determined. V_{DD} slew rate $\leq 100\text{ mV}/\mu\text{s}$
- (3) For adjustable voltage guidelines and resistor selection refer to **Adjustable Voltage Thresholds** in **Application and Implementation section**
- (4) Hysteresis is with respect to V_{ITP} and V_{ITN} voltage threshold. V_{ITP} has negative hysteresis and V_{ITN} has positive hysteresis.
- (5) For V_{OH} and V_{OL} relation to output variants refer to **Timing Figures after the Timing Requirement Table**

6.6 Switching Requirements

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, CTR = CTS = open and enabled, output $\overline{\text{RESET}}$ pull-up resistor $R_{PU} = 10 \text{ k}\Omega$, voltage $V_{PU} = 5.5 \text{ V}$, output $\overline{\text{BIST}}$ pull-up resistor $R_{PU_BIST} = 10 \text{ k}\Omega$, voltage $V_{PU_BIST} = 5.5 \text{ V}$, and load $C_{LOAD} = 10 \text{ pF}$. The operating free-air temperature range $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$ and $V_{DD} = 12 \text{ V}$ and $V_{IT} = 6.5 \text{ V}$ (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common Switching Requirements						
t _{CTR} (No Cap)	RESET release time delay (CTR) ⁽¹⁾	VIT = 800 mV C _{CTR} = Open 20% Overdrive from Hysteresis		350	600	μs
t _{CTS} (No Cap)	Sense detect time delay (CTS) ⁽²⁾	VIT = 800 mV C _{CTS} = Open 20% Overdrive from V _{IT}		85	100	μs
t _{SD}	Startup Delay ⁽³⁾	C _{CTR} = Open		1		ms
BIST Switching Requirements						
t _{BIST_en_pd}	Rising edge of BIST_EN to BIST asserting			2.3		μs
t _{BIST_en_pd}	Rising edge of BIST_EN to RESET asserting			2.3		μs
t _{BIST_recover}	Rising edge of BIST to SENSE input valid	C _{CTR} = Open, BIST = Enabled		350	600	μs
t _{BIST}	BIST run time				3.5	ms
t _{SD+BIST}	Startup time with BIST run time				4.5	ms
LATCH Switching Requirements						
t _{BIST_EN/LATCH_CLR_R ecover}	Rising edge of BIST to SENSE input valid	C _{CTR} = Open, BIST = Disabled		10		μs

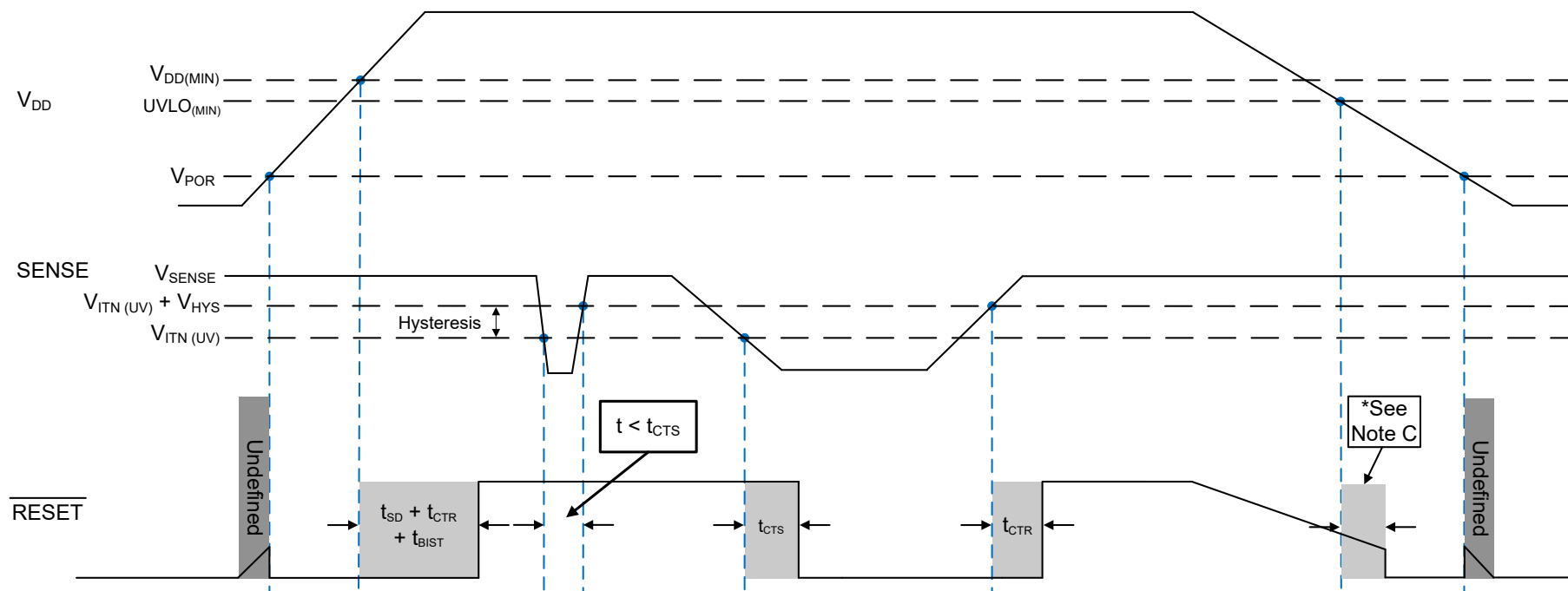
- (1) **CTR Reset detect time delay:**
 Overvoltage active-low output is measure from $V_{ITP-HYS}$ to V_{OH}
 Undervoltage active-low output is measure from $V_{ITN+HYS}$ to V_{OH}
- (2) **CTS Sense detect time delay:**
 Overvoltage active-low output is measure from V_{ITP} to V_{OL}
 Undervoltage active-low output is measure from V_{ITN} to V_{OL}
- (3) During the power-on sequence, V_{DD} must be at or above $V_{DD(MIN)}$ for at least $t_{SD+BIST} + t_{CTR}$ before the output is in the correct state based on V_{SENSE} .
 t_{SD} time includes the propagation delay (C_{CTR} = Open). Capacitor on CTR will add time to t_{SD} .

6.7 Timing Requirements

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, CTR = CTS = open and enabled, output $\overline{RESET}$ pull-up resistor $R_{PU} = 10\text{ k}\Omega$, voltage $V_{PU} = 5.5\text{ V}$, output $\overline{BIST}$ pull-up resistor $R_{PU_BIST} = 10\text{ k}\Omega$, voltage $V_{PU_BIST} = 5.5\text{ V}$, and load $C_{LOAD} = 10\text{ pF}$. The operating free-air temperature range $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$ and $V_{DD} = 12\text{ V}$ and $V_{IT} = 6.5\text{ V}$ (V_{IT} refers to V_{ITN} or V_{ITP}).

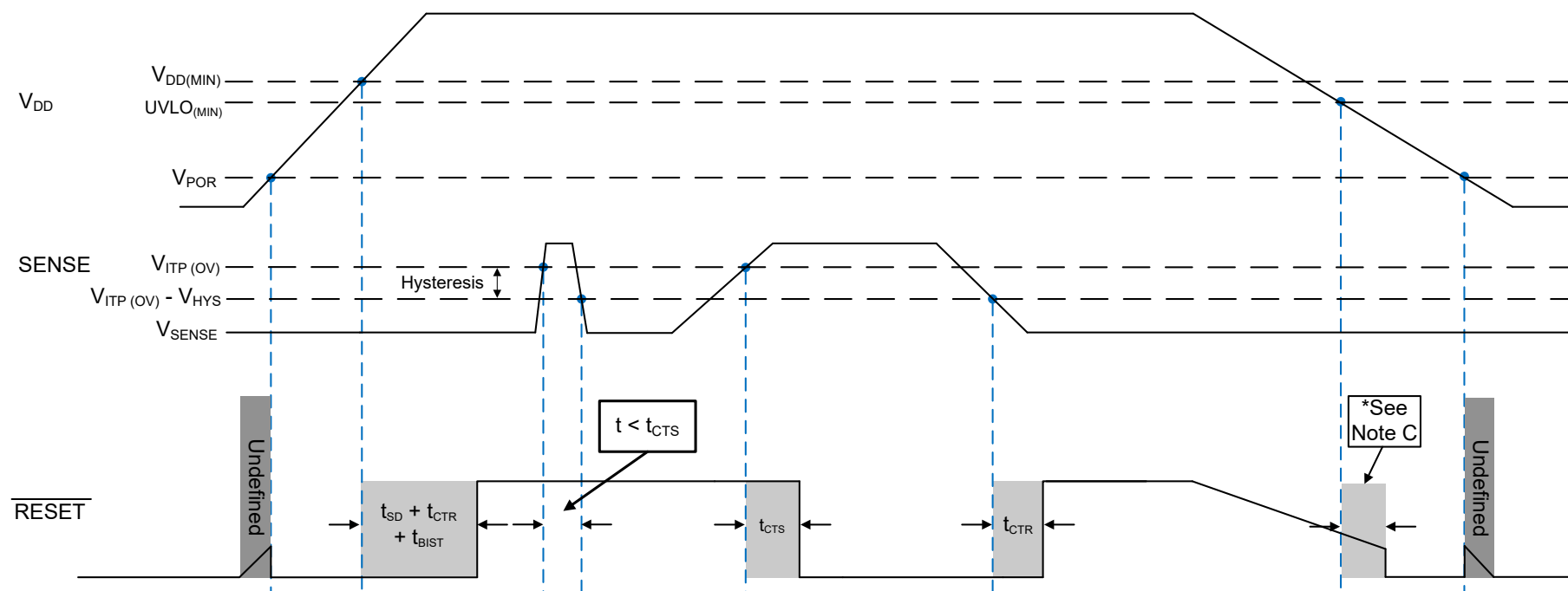
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common timing parameters					
BIST timing parameters					
$t_{BIST_en\text{ Glitch}}$	BIST_EN Glitch immunity		1.1		μs
t_{BIST_en}	Minimum BIST_EN input width to initiate BIST		1.2	8	μs
LATCH timing parameters					
$t_{BIST_EN/LATCH_CLR\text{ Glitch}}$	Latch Glitch immunity		1.5		μs
$t_{BIST_EN/LATCH_CLR}$	Latch input width to clear latch		1.6		μs

6.8 Timing Diagrams



- A. The timing diagram assumes the open-drain output $RESET$ pin is connected via an external pull-up resistor to V_{DD} .
- B. Be advised that [Figure 6-1](#) shows the V_{DD} falling slew rate is slow or the V_{DD} decay time is much larger than the propagation detect delay (t_{CTR}) time.
- C. $RESET$ is asserted when V_{DD} goes below the $UVLO_{(MIN)}$ threshold after the time delay, t_{CTR} , is reached.

Figure 6-1. SENSE Undervoltage (UV) Timing Diagram



- A. The timing diagram assumes the open-drain output RESET pin is connected via an external pull-up resistor to VDD.
- B. Be advised that Figure 6-2 shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay (t_{CTR}) time.
- C. RESET is asserted when VDD goes below the $UVLO_{(MIN)}$ threshold after the time delay, t_{CTR} , is reached.

Figure 6-2. SENSE Overvoltage (OV) Timing Diagram

6.9 Typical Characteristic

Typical characteristics show the typical performance of the TPS3762 device. Test conditions are $T_A = 25^\circ\text{C}$, unless otherwise noted.

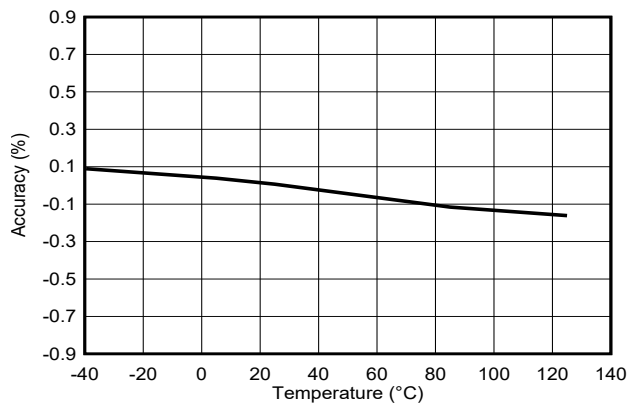


Figure 6-3. Undervoltage Accuracy vs Temperature ($V_{IT} = 0.8\text{ V}$)

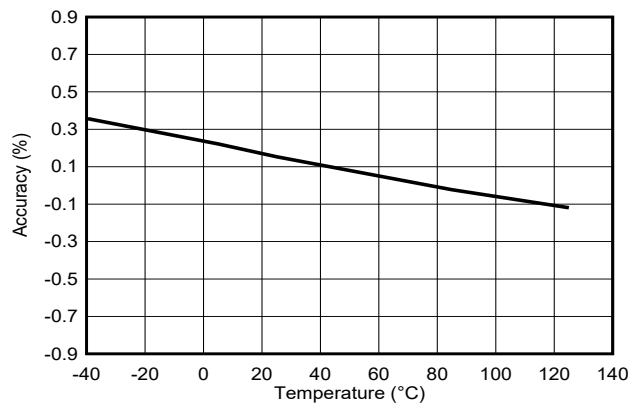


Figure 6-4. Overvoltage Accuracy vs Temperature ($V_{IT} = 0.8\text{ V}$)

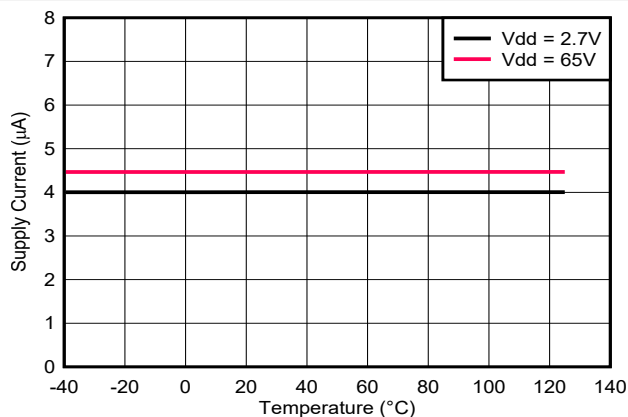


Figure 6-5. I_{DD} vs Temperature (RESET = High, $V_{IT} = 0.8\text{ V}$)

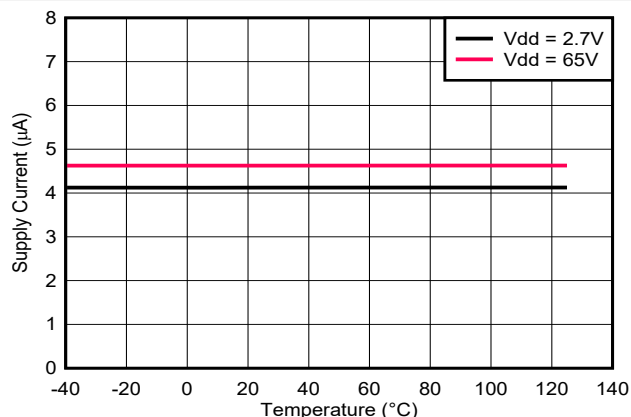


Figure 6-6. I_{DD} vs Temperature (RESET = Low, $V_{IT} = 0.8\text{ V}$)

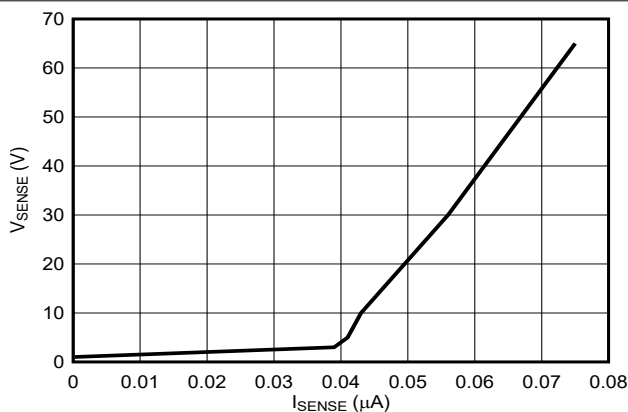


Figure 6-7. V_{SENSE} vs I_{SENSE} ($V_{DD} = 2.7\text{ V}$)

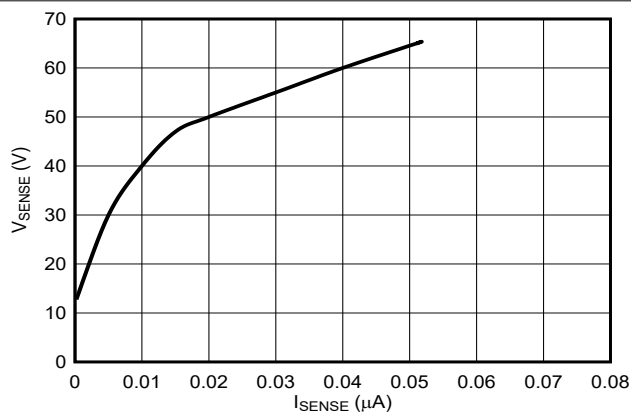


Figure 6-8. V_{SENSE} vs I_{SENSE} ($V_{DD} = 65\text{ V}$)

6.9 Typical Characteristic (continued)

Typical characteristics show the typical performance of the TPS3762 device. Test conditions are $T_A = 25^\circ\text{C}$, unless otherwise noted.

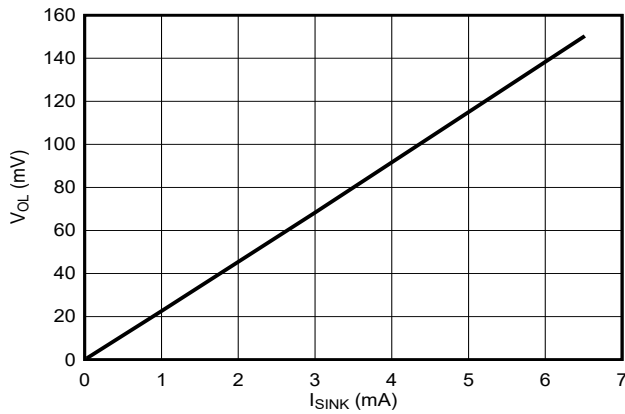


Figure 6-9. Open-Drain Active Low V_{OL} vs I_{RESET} ($V_{\text{DD}} = 2.7 \text{ V}$)

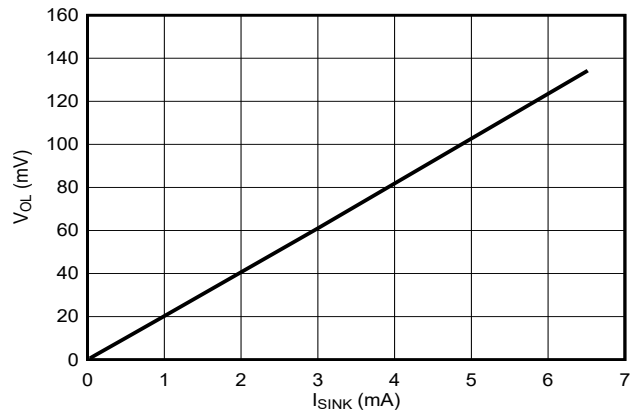


Figure 6-10. Open-Drain Active Low V_{OL} vs I_{RESET} ($V_{\text{DD}} = 65 \text{ V}$)

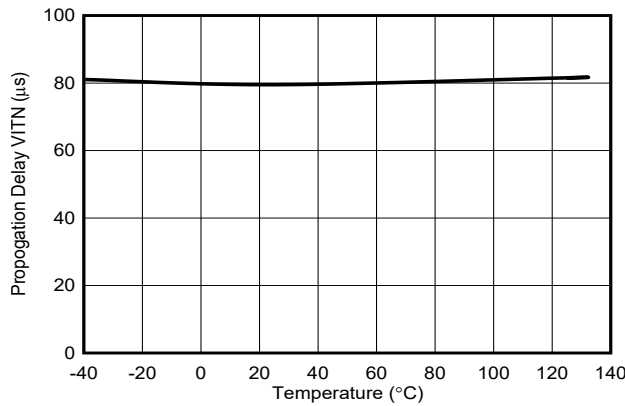


Figure 6-11. Propagation Delay (Undervoltage) vs Temperature ($V_{\text{IT}} = 0.8 \text{ V}$, CTS = Enabled = 50 pF)

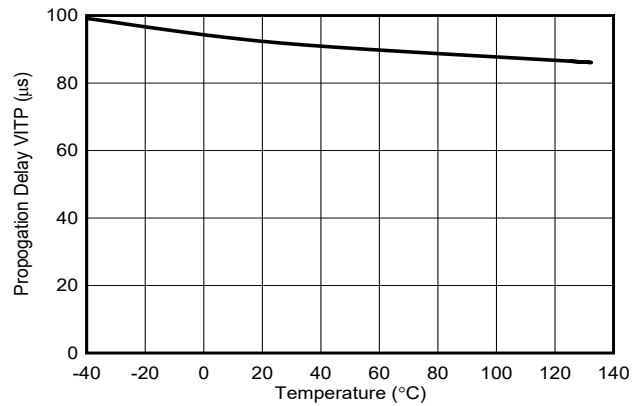


Figure 6-12. Propagation Delay (Overvoltage) vs Temperature ($V_{\text{IT}} = 0.8 \text{ V}$, CTS = Enabled = 50 pF)

7 Detailed Description

7.1 Overview

The TPS3762 is a family of high voltage and low quiescent current voltage supervisors with overvoltage and undervoltage threshold voltage options, delay timings, Built-In Self-Test, and latch. The TPS3762 over and undervoltage thresholds are device specific and are offered in either adjustable thresholds or fixed thresholds. The adjustable threshold option uses an external resistor ladder to make a voltage divider on SENSE pin which uses the internal 800 mV threshold to trigger overvoltage and undervoltage faults. The benefit of using an adjustable option with external resistors is the faster reaction speed compared to a fixed internal threshold variant. The TPS3762 fixed threshold option utilizes an integrated voltage divider to eliminate the need for external resistors and provides a lower system leakage current.

VDD, SENSE and $\overline{\text{RESET}}$ pins can support 65 V continuous operation. SENSE has -65 V reverse polarity protection. Both VDD and SENSE voltage levels can be independent of each other. TPS3762 includes a reset output latching feature that holds the output active to help system achieve safe state. Fixed and programmable sense and reset delay are available to avoid false resets and false reset releases.

7.2 Functional Block Diagram

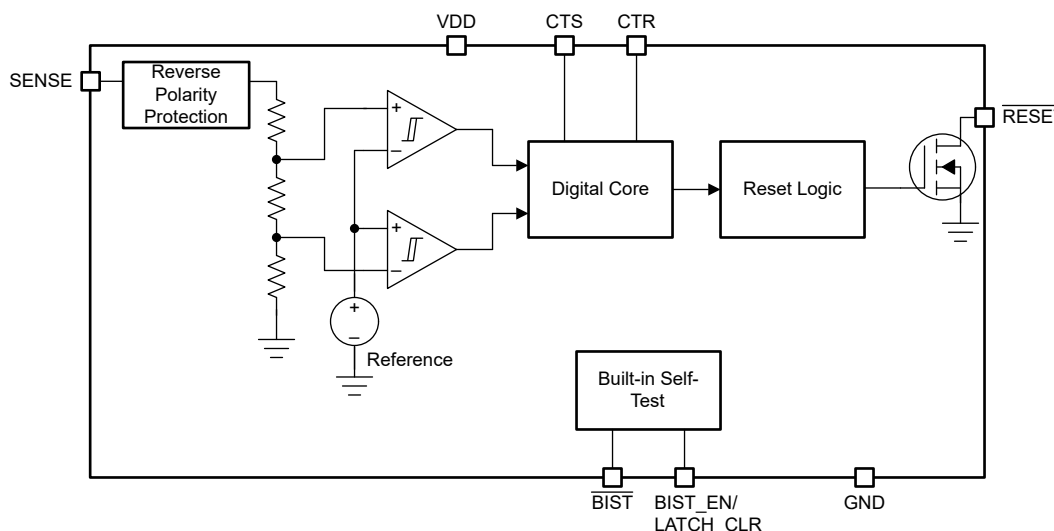


Figure 7-1. Fixed Threshold Functional Block Diagram

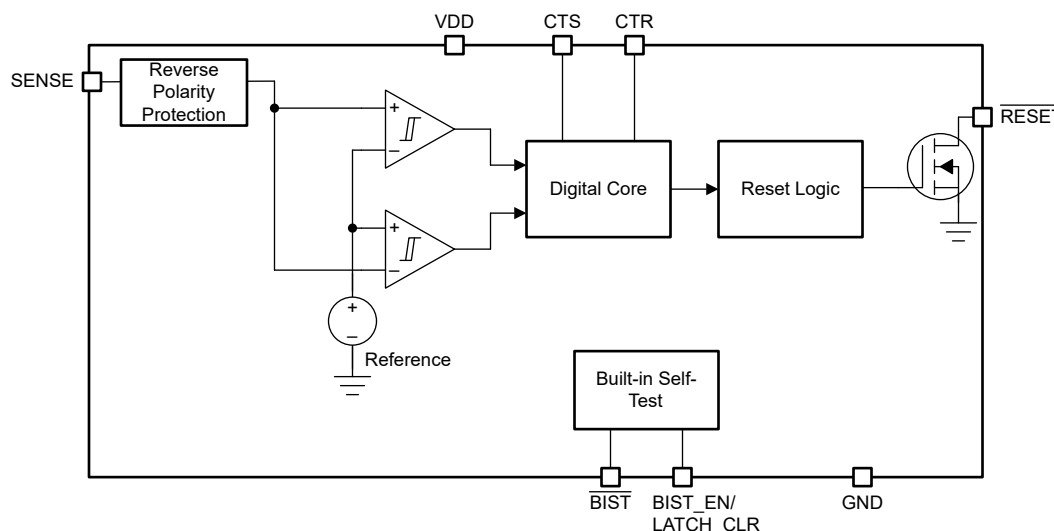


Figure 7-2. Adjustable Threshold Functional Block Diagram

7.3 Feature Description

7.3.1 Input Voltage (VDD)

VDD operating voltage ranges from 2.7 V to 65 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1 μ F capacitor between the VDD and GND.

VDD needs to be at or above $V_{DD(MIN)}$ for at least the start-up time delay (t_{SD}) for the device to be fully functional.

VDD voltage is independent of V_{SENSE} and V_{RESET} , meaning that VDD can be higher or lower than the other pins.

7.3.1.1 Undervoltage Lockout ($V_{POR} < V_{DD} < UVLO$)

When the voltage on VDD is less than the UVLO voltage, but greater than the power-on reset voltage (V_{POR}), the $\overline{RESET}$ and BIST pins will be asserted, regardless of the voltage at SENSE pins.

7.3.1.2 Power-On Reset ($V_{DD} < V_{POR}$)

When the voltage on VDD is lower than the power on reset voltage (V_{POR}), the output signal is undefined and is not to be relied upon for proper device function.

Note: Figure 7-3 and Figure 7-4 assume an external pull-up resistor is connected the reset pin to VDD.

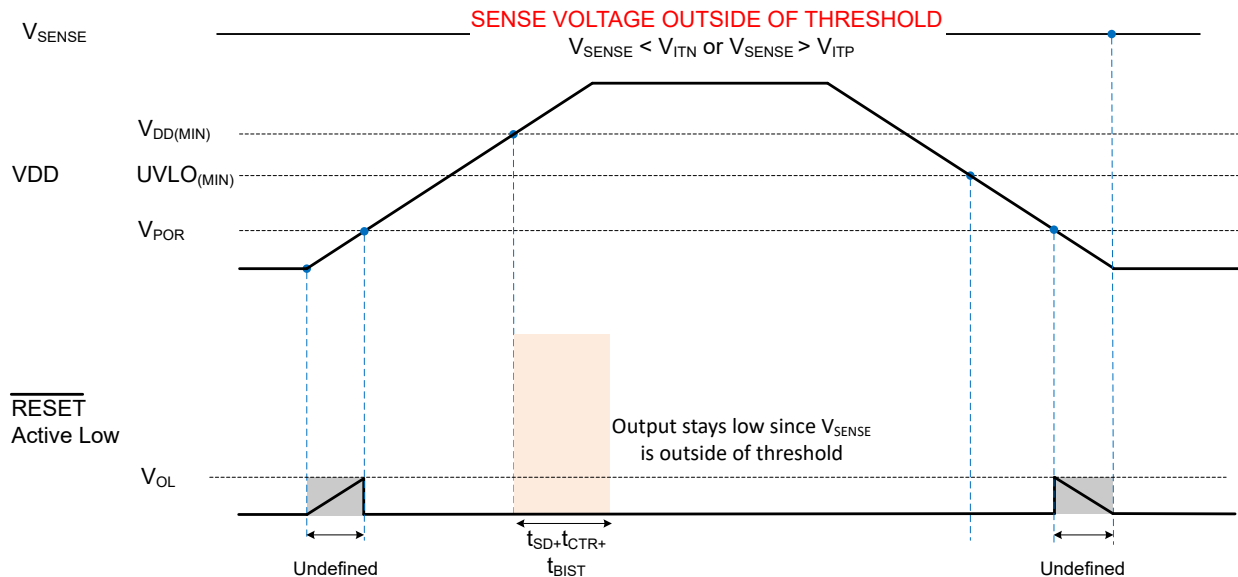


Figure 7-3. Power Cycle (SENSE Outside of Nominal Voltage)

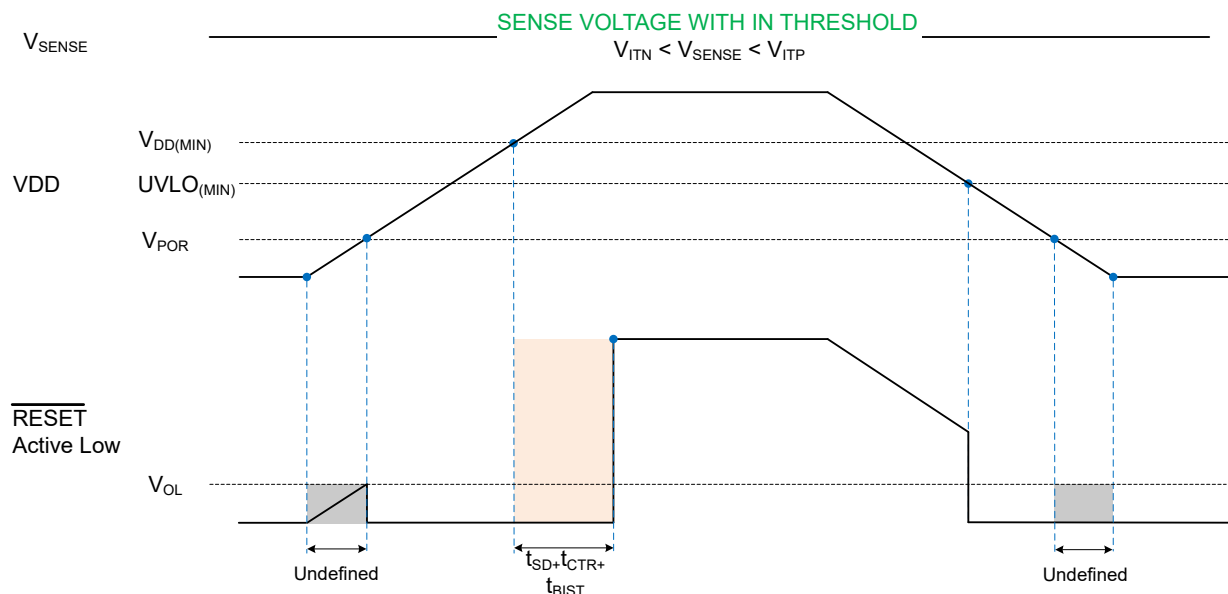


Figure 7-4. Power Cycle (SENSE Within Nominal Voltage)

7.3.2 SENSE

The SENSE pin connects to the supply rail that is to be monitored. The sense pin on each device is configured to monitor either overvoltage (OV), undervoltage (UV), and window (OV&UV) conditions. TPS3762 device offers built-in hysteresis that provides noise immunity and maintains stable operation.

Although not required in most cases, for noisy applications good analog design practice is to place a 10 nF to 100 nF bypass capacitor at the SENSE inputs to reduce sensitivity to transient voltages on the monitored signal. SENSE can be connected directly to VDD pin.

7.3.2.1 Reverse Polarity Protection

The TPS3762 has reverse polarity protection on the sense pin up to -65 V. This allows the TPS3762 to support accidental or test simulated reverse connections without damaging the device. This protection permits the TPS3762 to connect directly off of the supply prior to any reverse polarity protection diodes for accurate voltage measurement.

7.3.2.2 SENSE Hysteresis

TPS3762 device offers built-in hysteresis around the UV and OV thresholds to avoid erroneous $\overline{\text{RESET}}$ deassert. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold (V_{ITP}), for undervoltage options hysteresis is added to the negative threshold (V_{ITN}).

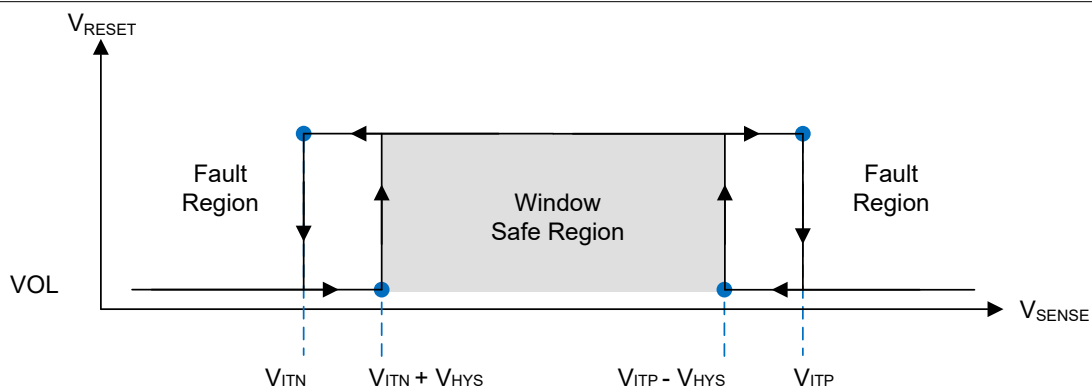


Figure 7-5. Hysteresis (Undervoltage & Overvoltage Active-Low)

Table 7-1. Common Adjustable Hysteresis Lookup Table

ADJUSTABLE THRESHOLD	TARGET		DEVICE ACTUAL HYSTERESIS OPTION
	TOPOLOGY	RELEASE VOLTAGE (V)	
800 mV	Overvoltage	784 mV	-2%
800 mV	Overvoltage	760 mV	-5%
800 mV	Overvoltage	720 mV	-10%
800 mV	Undervoltage	816 mV	2%
800 mV	Undervoltage	840 mV	5%
800 mV	Undervoltage	880 mV	10%

Table 7-1 shows a sample of hysteresis for the 800 mV adjustable variant for the TPS3762.

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is ($V_{ITN} + V_{HYS}$) and for the overvoltage (OV) channel is ($V_{ITP} - V_{HYS}$).

Undervoltage (UV) Channel

$$V_{ITN} = 800 \text{ mV}$$

$$\text{Voltage Hysteresis } (V_{HYS}) = 2\% = 16 \text{ mV}$$

$$\text{Hysteresis Accuracy} = +1.5\% \text{ to } +2.5\% = 16.24 \text{ mV to } 16.4 \text{ mV}$$

$$\text{Release Voltage} = V_{ITN} + V_{HYS} = 816.24 \text{ mV to } 816.4 \text{ mV}$$

Overvoltage (OV) Channel

$$V_{ITP} = 800 \text{ mV}$$

$$\text{Voltage Hysteresis } (V_{HYS}) = 2\% = 16 \text{ mV}$$

$$\text{Hysteresis Accuracy} = +1.5\% \text{ to } +2.5\% = 16.24 \text{ mV to } 16.4 \text{ mV}$$

$$\text{Release Voltage} = V_{ITP} - V_{HYS} = 783.6 \text{ mV to } 783.76 \text{ mV}$$

7.3.3 Output Logic Configurations

TPS3762 is a single channel device that has a single input sense pin and a single reset pin. The single reset is available with open drain topology.

7.3.3.1 Open-Drain

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels.

To select the right pull-up resistor consider system V_{OH} and the Open-Drain Leakage Current (I_{lk}) provided in the electrical characteristics, high resistors values will have a higher voltage drop affecting the output voltage high. The open-drain output can be connected as a wired-AND logic with other open-drain signals such as another TPS3762 open-drain output pin.

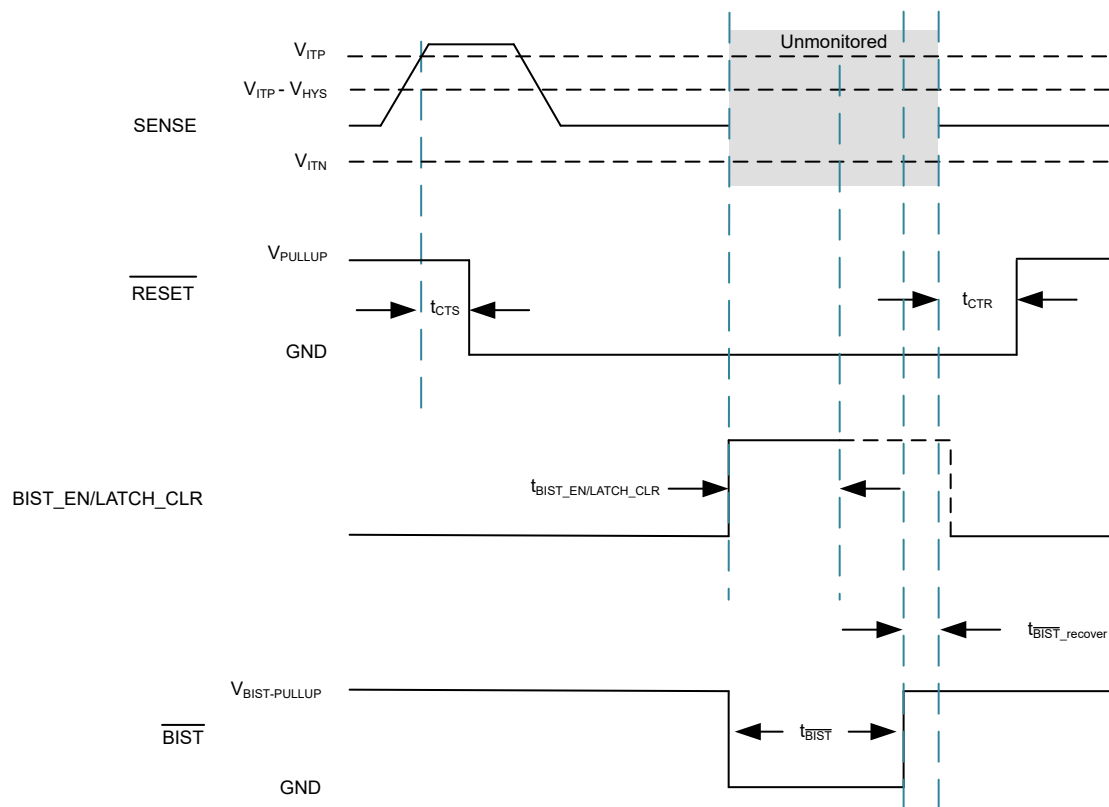
7.3.3.2 Active-Low ($\overline{RESET}$)

$\overline{RESET}$ (active low) denoted with a bar above the pin label. $\overline{RESET}$ remains high voltage (V_{OH} , deasserted) (open-drain variant V_{OH} is measured against the pullup voltage) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary (V_{ITP}).

7.3.3.3 Latching

The TPS3762 comes with the optional output reset latching feature for the window (OV & UV) and OV variants, check the [Section 4](#) to verify variant specific latch functionality. When using a variant with latch enabled ($V_{BIST_EN/LATCH_CLR} < 0.5$ V), whenever a fault, OV or UV, occurs $\overline{RESET}$ asserts and goes low and remains low until cleared by a logic high input ($V_{BIST_EN/LATCH_CLR} > 1.3$ V) on the BIST_EN / LATCH_CLR pin. If the SENSE pin is in a safe region and latch is disabled, the $\overline{RESET}$ will deassert after a delay. This delay is dependent on BIST and CTR timing. See [Section 7.3.6](#) for more details. While $V_{BIST_EN/LATCH_CLR} > 1.3$ V, the device is in latch disabled mode and the $\overline{RESET}$ will not latch for OV and UV on SENSE pin. While the device is in latch disabled mode the $\overline{RESET}$ will still assert for OV and UV faults. When $V_{BIST_EN/LATCH_CLR} < 0.5$ V, latch mode will be enabled.

Figure 7-6. $\overline{\text{RESET}}$ Latch & Unlatch

7.3.4 User-Programmable Reset Time Delay

TPS3762 has adjustable reset release time delay with external capacitors.

- A capacitor on CTR programs the reset time delay of the output.
- No capacitor on this pin gives the fastest reset delay time indicated by t_{CTR} in [Section 6.7](#).
- Variants such as TPS3762Q use a fixed internal time delay. check the [Section 4](#) to verify variant specific timing.

7.3.4.1 Reset Time Delay Configuration

The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR pin and GND.

The relationship between external capacitor $C_{CTR_EXT (typ)}$ and the time delay $t_{CTR (typ)}$ is given by [Equation 1](#).

$$t_{CTR (typ)} = R_{CTR (typ)} \times C_{CTR_EXT (typ)} + t_{CTR (no\ cap)} \quad (1)$$

$R_{CTR (typ)}$ = is in kilo ohms (k Ω)

$C_{CTR_EXT (typ)}$ = is given in microfarads (μ F)

$t_{CTR (typ)}$ = is the reset time delay (ms)

The reset delay varies according to three variables: the external capacitor (C_{CTR_EXT}), CTR pin internal resistance (R_{CTR}) provided in [Section 6](#), and a constant. The minimum and maximum variance due to the constant is show in [Equation 2](#) and [Equation 3](#):

$$t_{CTR (min)} = R_{CTR (min)} \times C_{CTR_EXT (min)} + t_{CTR (no\ cap (min))} \quad (2)$$

$$t_{CTR (max)} = R_{CTR (max)} \times C_{CTR_EXT (max)} + t_{CTR (no\ cap (max))} \quad (3)$$

There is no limit to the capacitor on CTR pin. Having a too large of a capacitor value can cause very slow charge up (rise times) due to capacitor leakage and system noise can cause the internal circuit to hold $\overline{RESET}$ active.

* Leakages on the capacitor can effect accuracy of reset time delay.

7.3.5 User-Programmable Sense Delay

TPS3762 has adjustable sense release time delay with external capacitors.

- A capacitor in CTS programs the excursion detection on SENSE.
- No capacitor on this pin gives the fastest sense delay time indicated by t_{CTS} in [Section 6.7](#).
- The TPS3762 comes with an optional fixed internal time delay that ignores the capacitor value at the CTS pin, check the [Section 4](#) to verify variant specific functionality.

7.3.5.1 Sense Time Delay Configuration

The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTS pin and GND.

The relationship between external capacitor $C_{CTS_EXT (typ)}$ and the time delay $t_{CTS (typ)}$ is given by [Equation 4](#).

$$t_{CTS (typ)} = R_{CTS (typ)} \times C_{CTS_EXT (typ)} + t_{CTS (no\ cap)} \quad (4)$$

R_{CTS} = is in kilo ohms (k Ω)

C_{CTS_EXT} = is given in microfarads (μ F)

t_{CTS} = is the sense time delay (ms)

The sense delay varies according to three variables: the external capacitor (C_{CTS_EXT}), CTS pin internal resistance (R_{CTS}) provided in Electrical Characteristics, and a constant. The minimum and maximum variance due to the constant is show in [Equation 5](#) and [Equation 6](#):

$$t_{CTS (min)} = R_{CTS (min)} \times C_{CTS_EXT (min)} + t_{CTS (no\ cap (min))} \quad (5)$$

$$t_{CTR (max)} = R_{CTS (max)} \times C_{CTS_EXT (max)} + t_{CTSx (no\ cap (max))} \quad (6)$$

The recommended maximum sense delay capacitor for the TPS3762 is limited to 10 μ F as this makes sure enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

* Leakages on the capacitor can effect accuracy of sense time delay.

7.3.6 Built-In Self-Test

The TPS3762 has a Built-In Self-Test (BIST) feature that runs diagnostics internally in the device. During power-up BIST is initiated automatically after crossing $V_{DD(min)}$. During BIST the $BIST$ pin and $RESET$ output asserts low and deasserts if the $BIST$ test completes successfully indicating no internal faults in the device. The length of the BIST and $BIST$ assertion is specified by t_{BIST} . If BIST is not successful, the $BIST$ pin will say asserted low signifying an internal fault. The $RESET$ output will stay assert on $BIST$ failure. During BIST, the device is not monitoring the SENSE pin for faults and the $RESET$ is not dependent on the SENSE pin voltage. The $BIST$ sequence of internal tests verifies the internal signal chain of the device by checking for faults on the internal comparators on the SENSE pin, bandgap voltage, and the $RESET$ output. See [Figure 7-7](#) for more details.

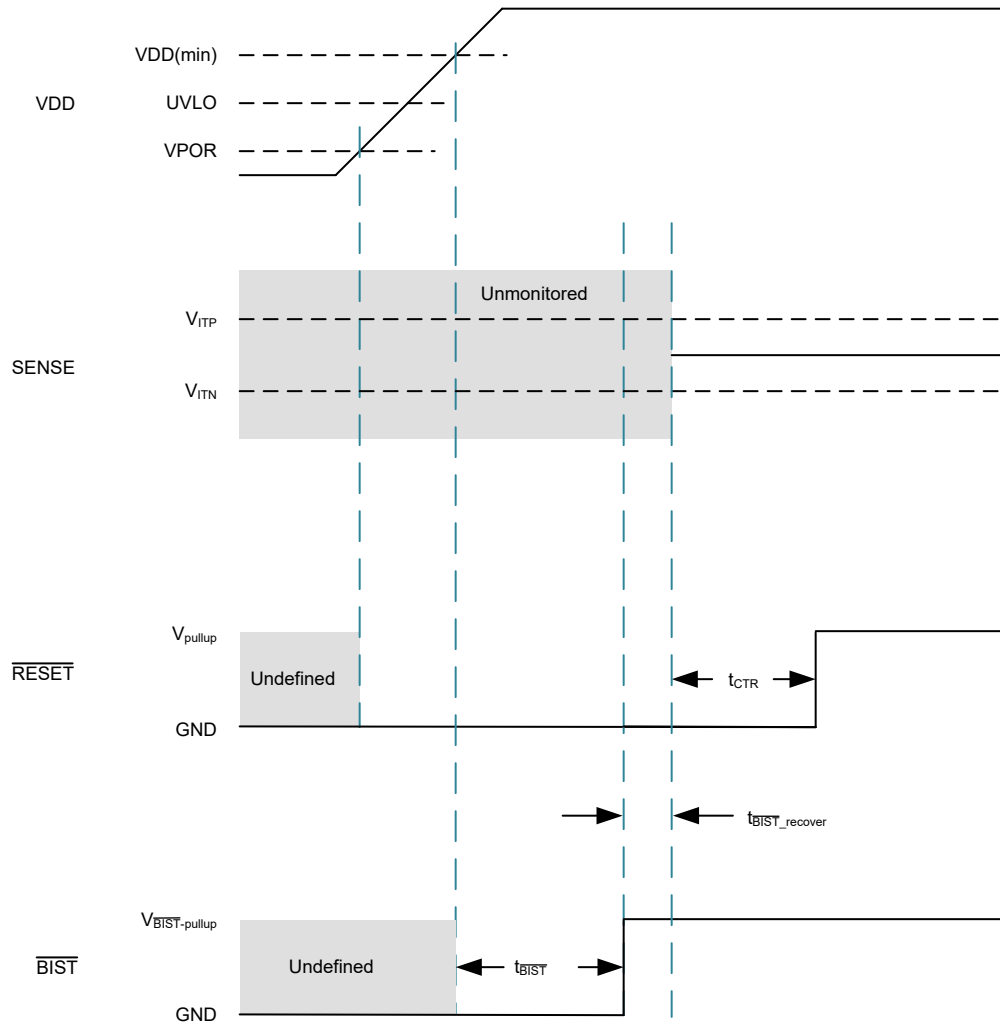
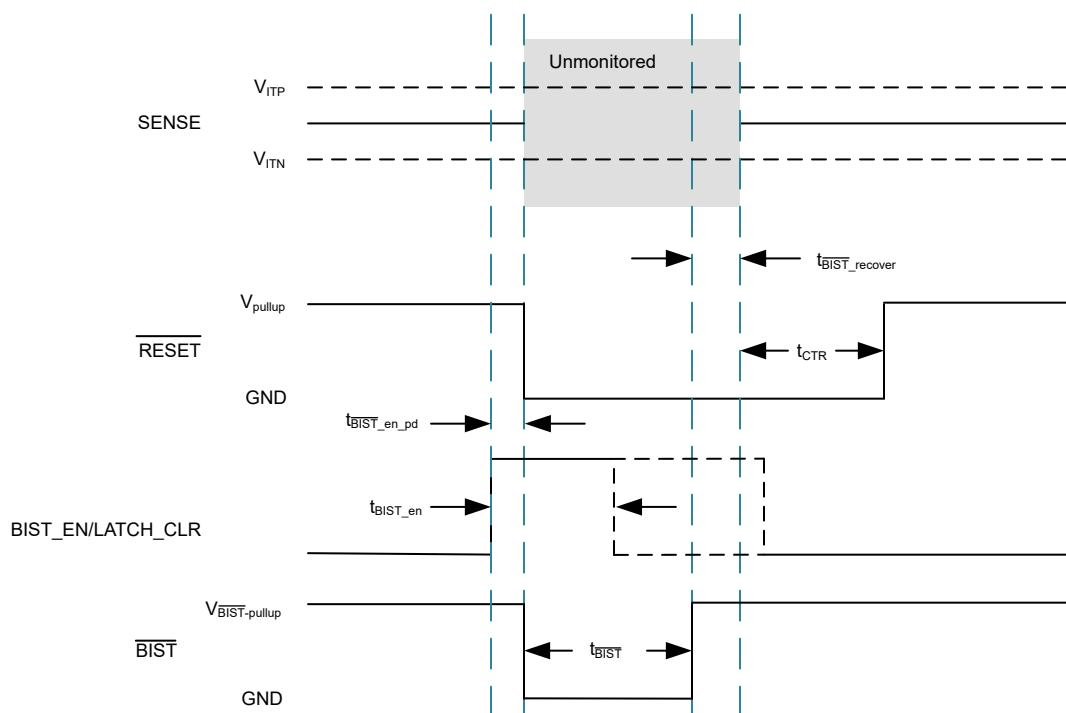
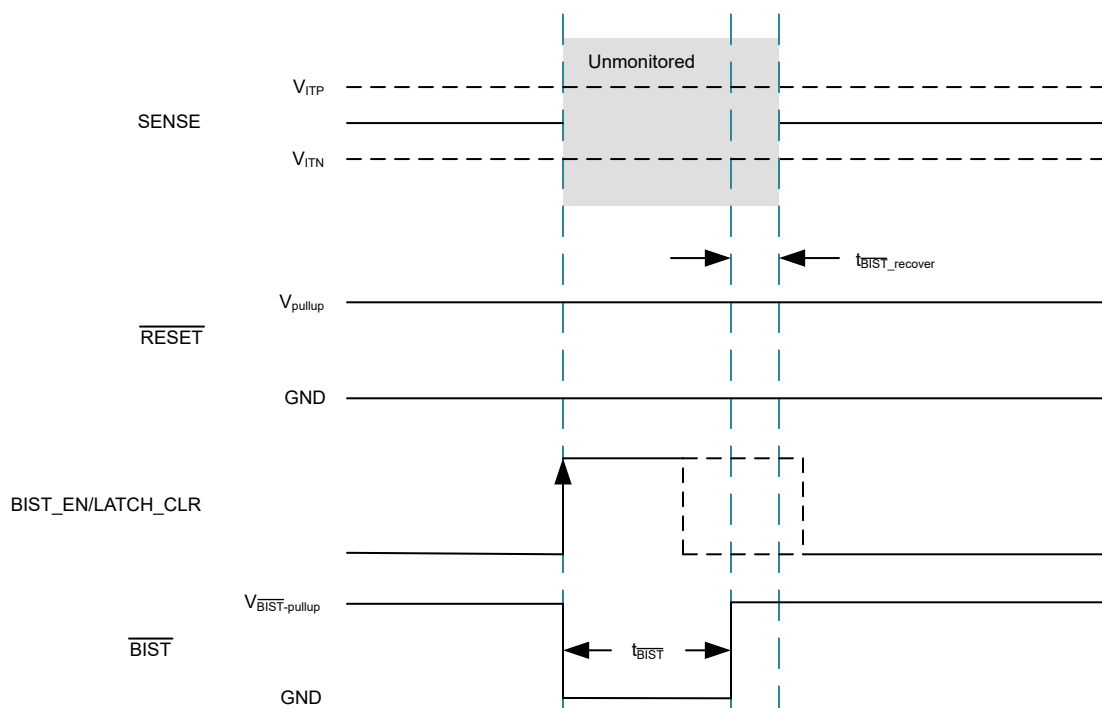


Figure 7-7. TPS3762 Start-Up Sequence

After a successful power-up sequence, BIST can be initiated any time with a logic high input (V_{BIST_EN} or $V_{BIST_EN/LATCH_CLR} > 1.3\text{ V}$) on the BIST_EN / LATCH_CLR pin. BIST initiates and the $\overline{BIST}$ pin asserts only if the SENSE pin is not in a overvoltage or undervoltage fault mode. During this BIST test time period, t_{BIST} , $\overline{BIST}$ pin asserts low to signify that $\overline{BIST}$ has started and $\overline{RESET}$ assertion is dependent on the device variant. Upon a successful BIST the $\overline{BIST}$ pin and $\overline{RESET}$ pin are deasserted. If BIST is not successful due to the internal device not working properly, the $\overline{RESET}$ pin and $\overline{BIST}$ pin remain asserted low signifying a fault internal to the device. See [Figure 7-8](#) and for [Figure 7-9](#) more details.

Figure 7-8. BIST With $\overline{\text{RESET}}$ AssertionFigure 7-9. BIST With No $\overline{\text{RESET}}$ Assertion

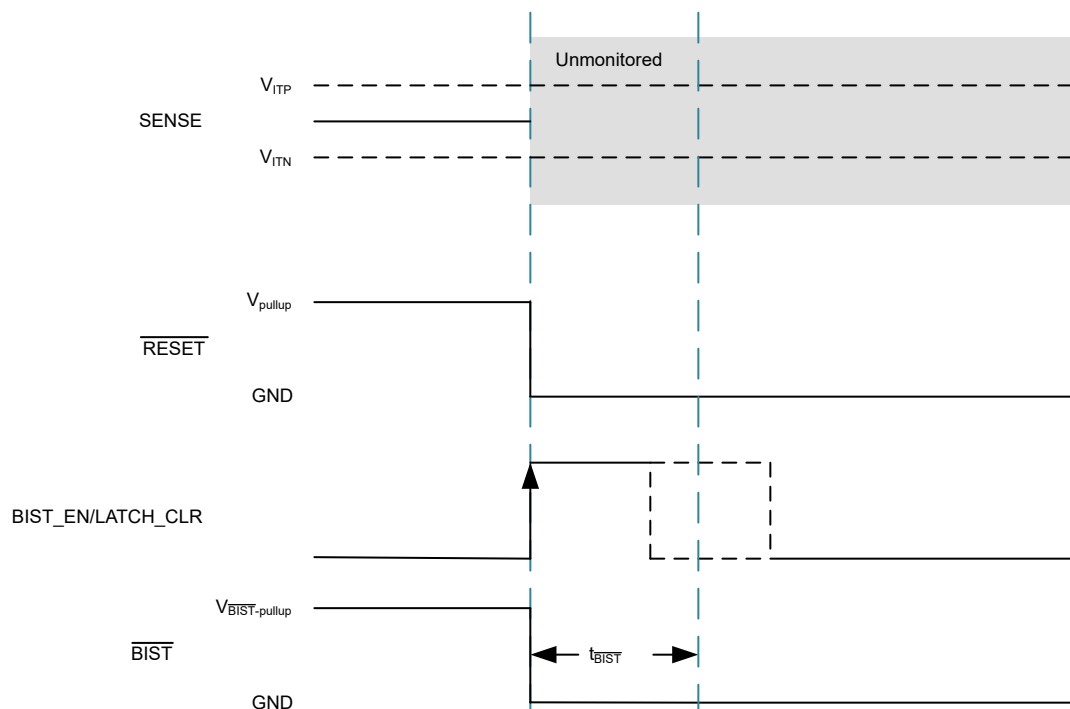


Figure 7-10. BIST Fail With $\overline{\text{RESET}}$ Assertion

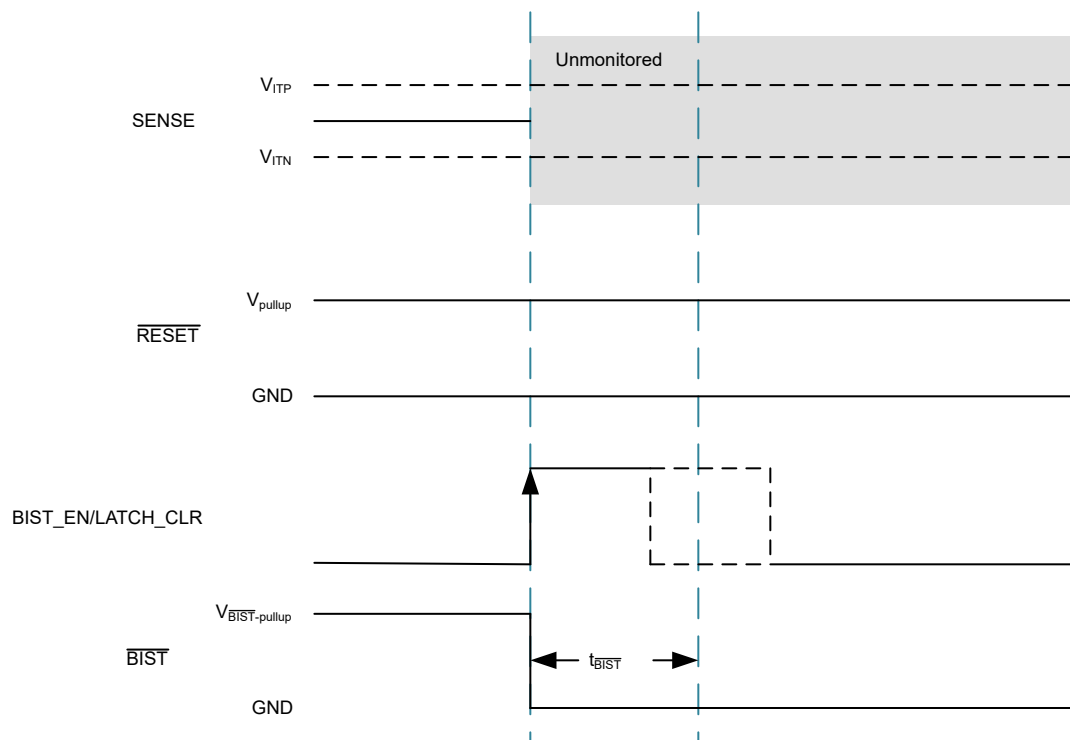


Figure 7-11. BIST Fail With No $\overline{\text{RESET}}$ Assertion

7.4 Device Functional Modes

Table 7-2. Undervoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR ⁽¹⁾	VDD PIN	OUTPUT ⁽²⁾ (RESET PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	$SENSE > V_{ITN}$	$SENSE > V_{ITN}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Undervoltage Detection	$SENSE > V_{ITN}$	$SENSE < V_{ITN}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Undervoltage Detection	$SENSE < V_{ITN}$	$SENSE > V_{ITN}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Normal Operation	$SENSE < V_{ITN}$	$SENSE > V_{ITN} + HYS$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
UVLO Engaged	$SENSE > V_{ITN}$	$SENSE > V_{ITN}$	Open or capacitor connected	$V_{POR} < V_{DD} < V_{DD(MIN)}$	Low
Below V_{POR} , Undefined Output	$SENSE > V_{ITN}$	$SENSE > V_{ITN}$	Open or capacitor connected	$V_{DD} < V_{POR}$	Undefined

(1) Reset time delay is ignored in the truth table.

(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

Table 7-3. Overvoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR ⁽¹⁾	VDD PIN	OUTPUT ⁽²⁾ (RESET PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	$SENSE < V_{ITN}$	$SENSE < V_{ITN}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Overvoltage Detection	$SENSE < V_{ITN}$	$SENSE > V_{ITN}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Overvoltage Detection	$SENSE > V_{ITN}$	$SENSE < V_{ITN}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Normal Operation	$SENSE > V_{ITN}$	$SENSE < V_{ITN} - HYS$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
UVLO Engaged	$SENSE < V_{ITN}$	$SENSE < V_{ITN}$	Open or capacitor connected	$V_{POR} < V_{DD} < UVLO$	Low
Below V_{POR} , Undefined Output	$SENSE < V_{ITN}$	$SENSE < V_{ITN}$	Open or capacitor connected	$V_{DD} < V_{POR}$	Undefined

(1) Reset time delay is ignored in the truth table.

(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.2 Adjustable Voltage Thresholds

[Figure 8-1](#) illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8 V voltage threshold device when using an adjustable voltage variant. This variant bypasses the internal resistor ladder.

For example, consider a 12 V rail, V_{MON} , being monitored for overvoltage (OV) using of the TPS3762D02OVDDFR variant, as shown in [Figure 8-1](#). The monitored OV threshold, denoted as V_{MON+} , is the desired voltage where the device asserts the reset. For this example $V_{MON+} = 35$ V. To assert an overvoltage reset the voltage at the sense pin, V_{SENSE} , needs to be equal to the input threshold positive, V_{ITP} . For this example variant $V_{SENSE} = V_{ITP} = 0.8$ V. Using R_1 and R_2 the correlation between V_{MON+} and V_{SENSE} can be seen in [Equation 8](#). Assuming $R_2 = 10$ k Ω , and R_1 can be calculated as $R_1 = 427.5$ k Ω .

$$V_{SENSE} = V_{MON+} \times (R_2 \div (R_1 + R_2)) \quad (7)$$

The TPS3762D02OVDDFR comes with variant specific 2 %, 5 %, or 10 % voltage threshold hysteresis. For the reset signal to become deasserted, V_{MON} must go below $V_{ITP} - V_{HYS}$. For this example variant a 2 % voltage threshold hysteresis was selected. Therefore, V_{MON} equals 34.3 V when the reset signal becomes deasserted.

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that can affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for the design specifications. The internal SENSE resistance (R_{SENSE}) can be calculated by the SENSE voltage (V_{SENSE}) divided by the SENSE current (I_{SENSE}) as shown in [Equation 9](#). V_{SENSE} can be calculated using [Equation 7](#) depending on the resistor divider and monitored voltage. I_{SENSE} can be calculated using [Equation 8](#).

$$I_{SENSE} = [(V_{MON} - V_{SENSE}) \div R_1] - (V_{SENSE} \div R_2) \quad (8)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (9)$$

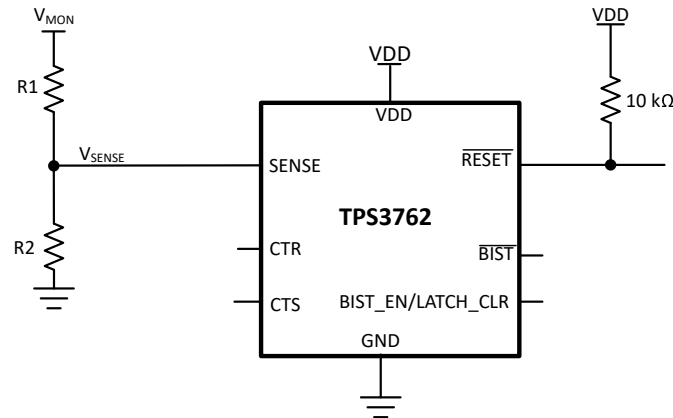


Figure 8-1. Adjustable Voltage Threshold with External Resistor Dividers

8.3 Typical Application

8.3.1 Design 1: SELV Power Supply Monitoring

This application is intended for the initial power stage in applications with 24 V SELV power rails. The TPS3762 utilizes high-voltage SENSE and V_{DD} inputs to monitor a 24 V SELV power rail.

[Figure 8-6](#) illustrates an example of how the TPS3762 is monitoring the rail voltage while being powered by it, as well.

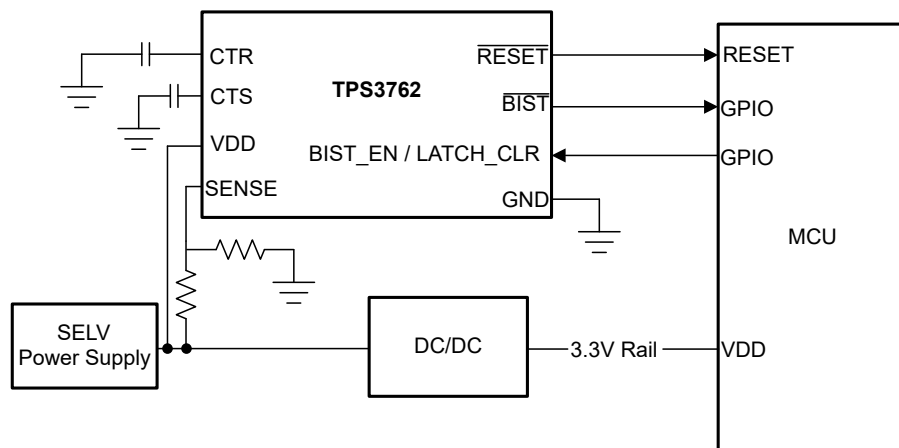


Figure 8-2. TPS3762 Overvoltage Supervisor with SELV Monitoring

8.3.1.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Voltage Threshold	Typical OV voltage threshold 30V.
Maximum Input Power	Operate with power supply input up to 65V
Output logic	Open-Drain
SENSE delay	>100ms
RESET delay	>300ms
Output Features	Output latching and built-in self-test

8.3.1.2 Detailed Design Procedure

The TPS3762 utilizes high-voltage SENSE and V_{DD} inputs to monitor a 24V SELV power rail.

In this design example TPS3762D02OVDDFR is used.

8.3.1.2.1 Setting Voltage Threshold

The positive-going threshold voltage, V_{ITP} , is set by the device variant. In this example, the nominal supply voltage from the SELV supply is 24 V. Setting a overvoltage threshold of 30 V (~25% buffer) makes sure that the device resets before supply voltage violates the allowed boundary. The adjustable voltage variant is chosen and R_1 and R_2 are adusted to meet the threshold. Assuming R_2 equal to 10 k Ω and R_1 is calculated as 365 k Ω . For additional information on selecting resistor values see [Section 8.2](#). TPS3762 also supports fixed voltage threshold variants. Threshold voltage decoding can be found in [Device Decoder](#).

8.3.1.2.2 Meeting the Sense and Reset Delay

The TPS3762 features both reset assertion (sense) delay, t_{CTS} , and reset deassertion (reset) delay, t_{CTR} . The TPS3762 features two options for selecting sense and reset delays: fixed delays and capacitor-programmable delays. For the device variant used in this design, TPS3762D02OVDDFR, the capacitor programmable delay is chosen. [Section 7.3.5](#) and [Section 7.3.4](#) show how to set the timings for the capacitor-programmable delays. The application requires greater than 100 ms sense delay, thus a 0.033 μ F capacitor is used. The application requires greater than 300 ms reset delay, thus a 0.1 μ F capacitor is used.

8.3.1.2.3 Setting Supply Voltage

Setting the supply voltage is done by connecting the V_{DD} input directly to the 24V rail without the need for external circuitry. The device being able to handle 65 V on V_{DD} means the monitored voltage rail can handle any voltage transience up to 65 V. Good analog design practice recommends using a 0.1 μ F capacitor on the V_{DD} pin.

8.3.1.2.4 Initiating Built-In Self-Test and Clearing Latch

Built-In Self-Test (BIST) is asserted on device power-up, as outlined in [Figure 7-7](#). BIST can also be initiated any time by a rising edge that crosses the voltage logic high input (V_{BIST_EN} or $V_{BIST_EN/LATCH_CLR} > 1.3$ V) on the BIST_EN / LATCH_CLR pin, as outlined in [Figure 7-8](#). Output reset latching is set by the device variant. For the device variant used in this design, TPS3762D02OVDDFR, the output has latch. Device specific output reset latching feature can be found in [#none#](#). In order to clear the latch a logic high input on the BIST_EN / LATCH_CLR pin is required. When clearing latch, BIST is initiated and the $\overline{RESET}$ returns logic level high once $t_{BIST} + t_{BIST_recover} + t_{CTR}$ has expired, outlined in [Figure 7-6](#). While $V_{BIST_EN/LATCH_CLR} > 1.3$ V, the device is in latch disabled mode and the $\overline{RESET}$ will not latch for OV and UV on SENSE pin. While the device is in latch disabled mode the $\overline{RESET}$ will still assert for OV and UV faults.

8.3.1.3 Application Curves

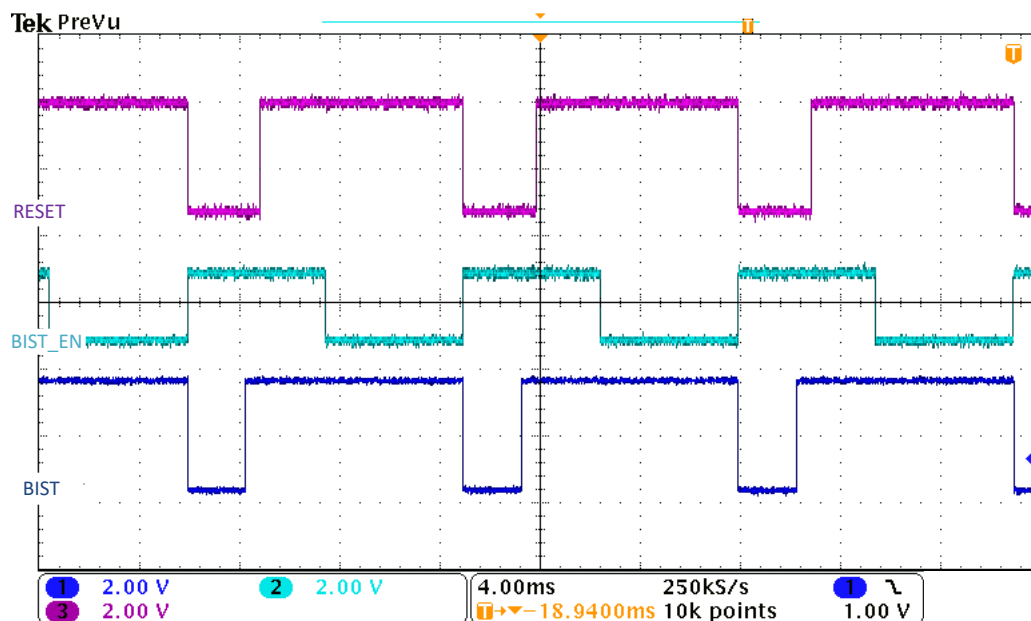


Figure 8-3. $\overline{\text{BIST}}$ with $\overline{\text{RESET}}$ Assertion Waveform

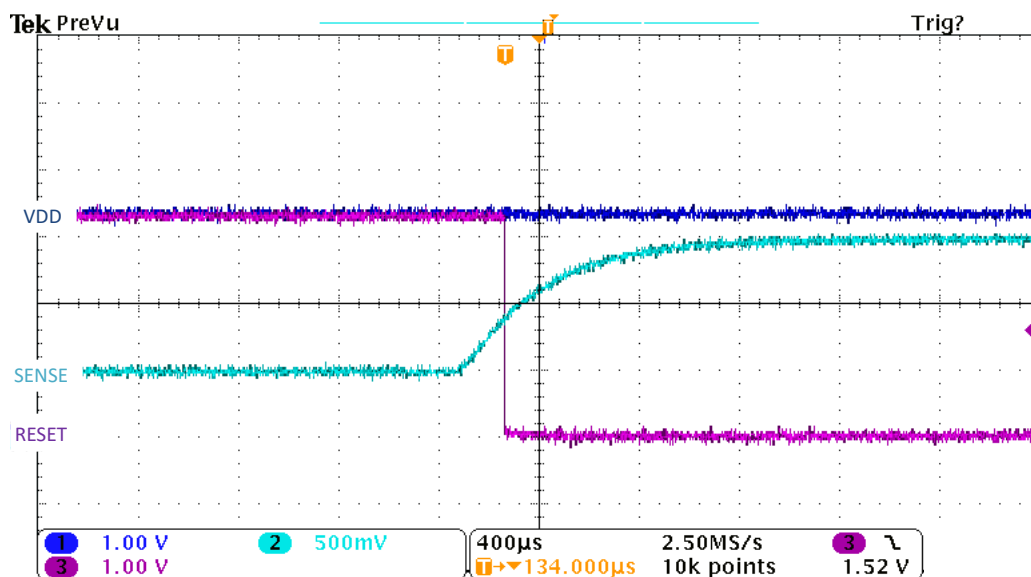


Figure 8-4. Overvoltage $\overline{\text{RESET}}$ Latching Waveform

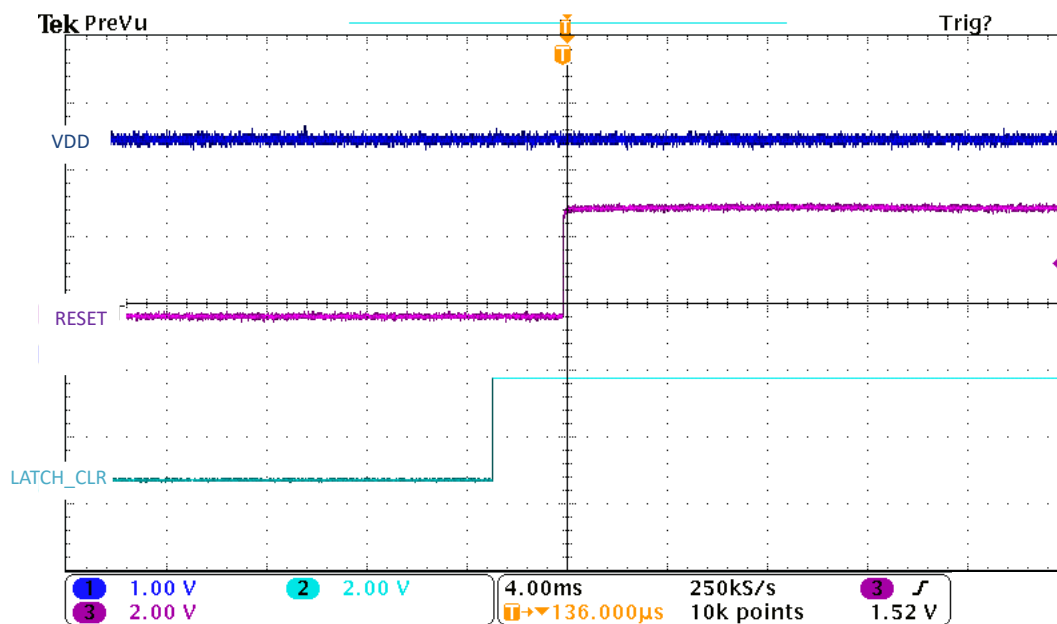


Figure 8-5. Overvoltage $\overline{\text{RESET}}$ Unlatching Waveform

8.4 Power Supply Recommendations

TPS3762 is designed to operate from an input supply with a V_{DD} voltage between 2.7 V (minimum operation) to 65 V (maximum operation). Good analog design practice recommends placing a minimum 0.1 μ F ceramic capacitor as near as possible to the V_{DD} pin.

8.4.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuous allowable power dissipation for the device in a given package can be calculated using Equation 10:

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \quad (10)$$

The actual power being dissipated in the device can be represented by Equation 11:

$$P_D = V_{DD} \times I_{DD} + P_{RESET} \quad (11)$$

P_{RESET} is calculated by Equation 12 or Equation 13

$$P_{RESET} (PUSH/PULL) = V_{DD} - V_{RESET} \times I_{RESET} \quad (12)$$

$$P_{RESET} (OPEN-DRAIN) = V_{RESET} \times I_{RESET} \quad (13)$$

Equation 10 and Equation 11 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature (T_{A-MAX}) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature (T_{A-MAX}) may have to be de-rated. T_{A-MAX} is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum allowable power dissipation in the device package in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by Equation 14:

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (14)$$

8.5 Layout

8.5.1 Layout Guidelines

- Make sure that the connection to the V_{DD} pin is low impedance. Good analog design practice is to place a greater than 0.1 μ F ceramic capacitor as near as possible to the V_{DD} pin.
- To further improve the noise immunity on the SENSE pins, placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.
- If a capacitor is used on CTS or CTR, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 5 pF.
- Place the pull-up resistors on $\overline{RESET}$ as close to the pin as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible. If high and low voltage traces need to run close by, spacing between traces should be greater than 20 mils (0.5 mm).

- Do not have high voltage metal pads or traces closer than 20 mils (0.5 mm) to the low voltage metal pads or traces.

8.5.2 Layout Example

The layout example in [Figure 8-6](#) shows how the TPS3762 is laid out on a printed circuit board (PCB) with user-defined delays.

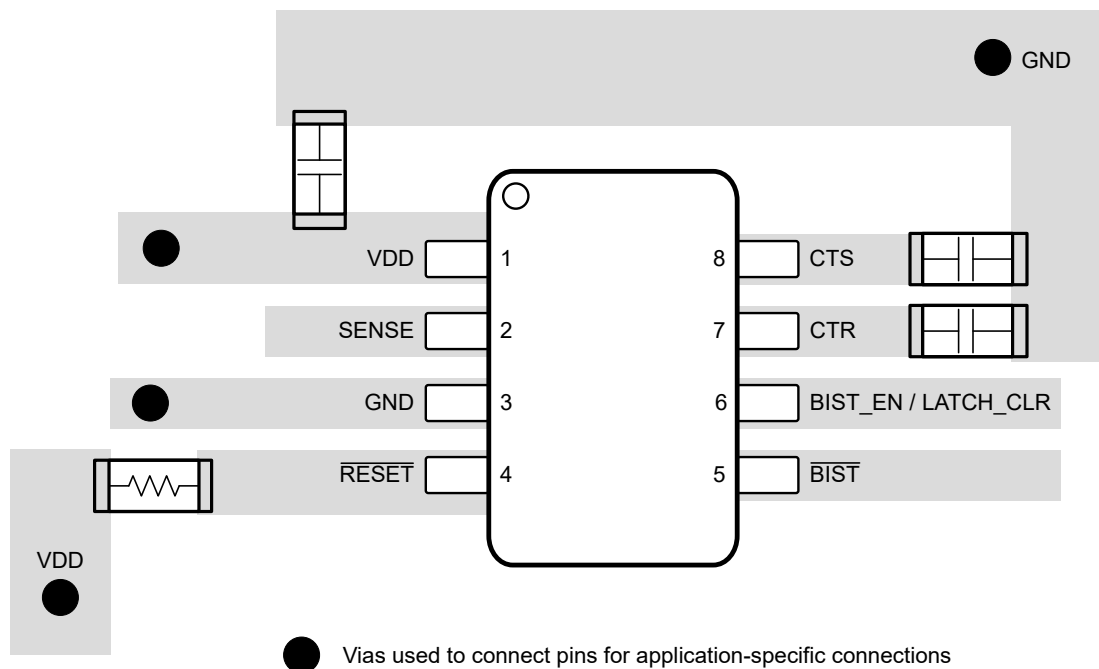


Figure 8-6. TPS3762 Recommended Layout

9 Device and Documentation Support

9.1 Device Nomenclature

[Device Decoder](#) in [Section 4](#) describe how to decode certain device function of the device based on its part number. Not all part numbers follow this nomenclature. Use [Table 9-1](#) as the part number decoding table for all devices.

Table 9-1. Device Configuration Table

ORDERABLE PART NAME	Overvoltage (V _{ITP})	Overvoltage Hysteresis	Undervoltage (V _{ITN})	Undervoltage Hysteresis	CTR / CTS	Latch / UVbypass	BIST RESETTrigger
TPS3762D02OVDDFR	800mV	2%	N/A	N/A	ADJ / ADJ	Both Enabled	Yes

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2023) to Revision A (December 2023)	Page
• Production Data Release.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3762D02OVDDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62D02
TPS3762D02OVDDFR.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62D02

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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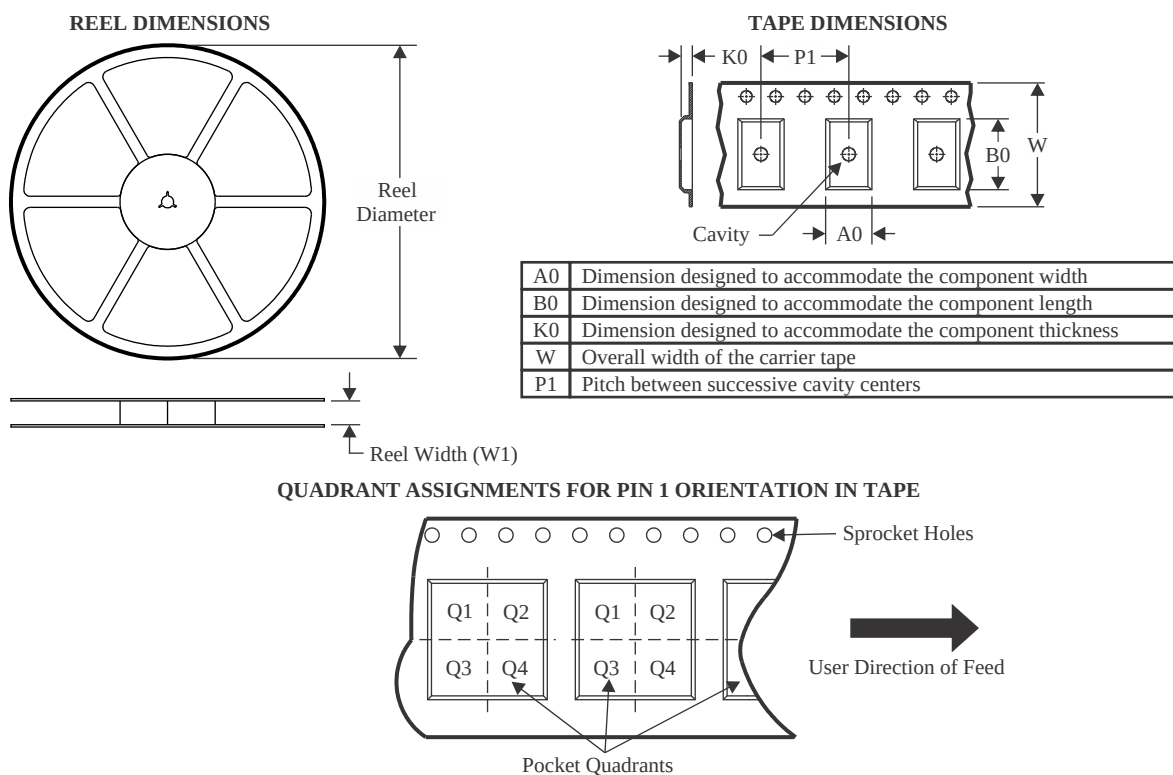
OTHER QUALIFIED VERSIONS OF TPS3762 :

- Automotive : [TPS3762-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

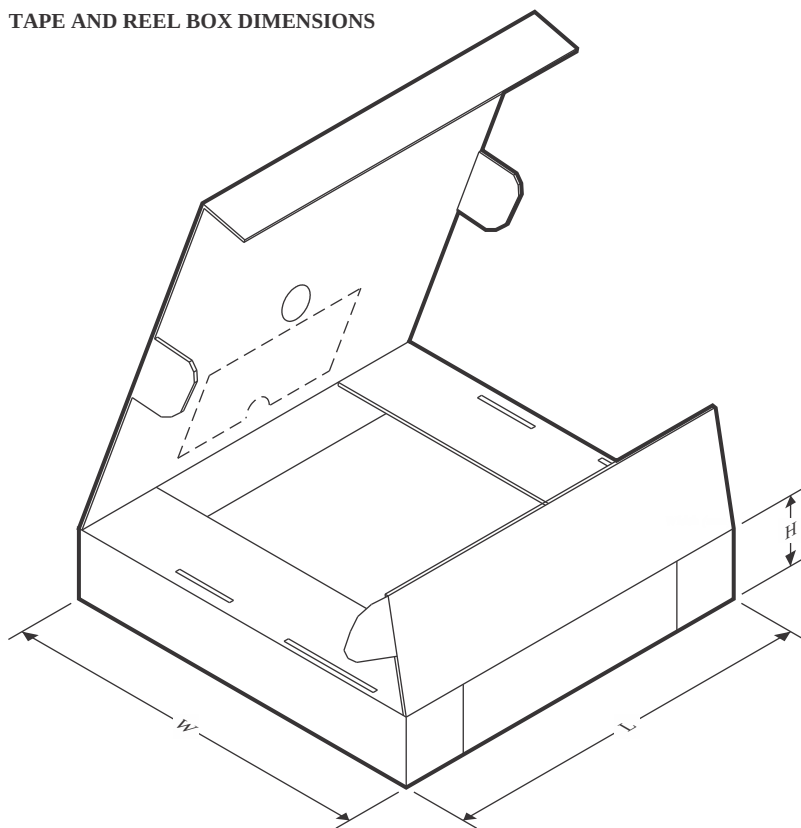
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3762D02OVDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

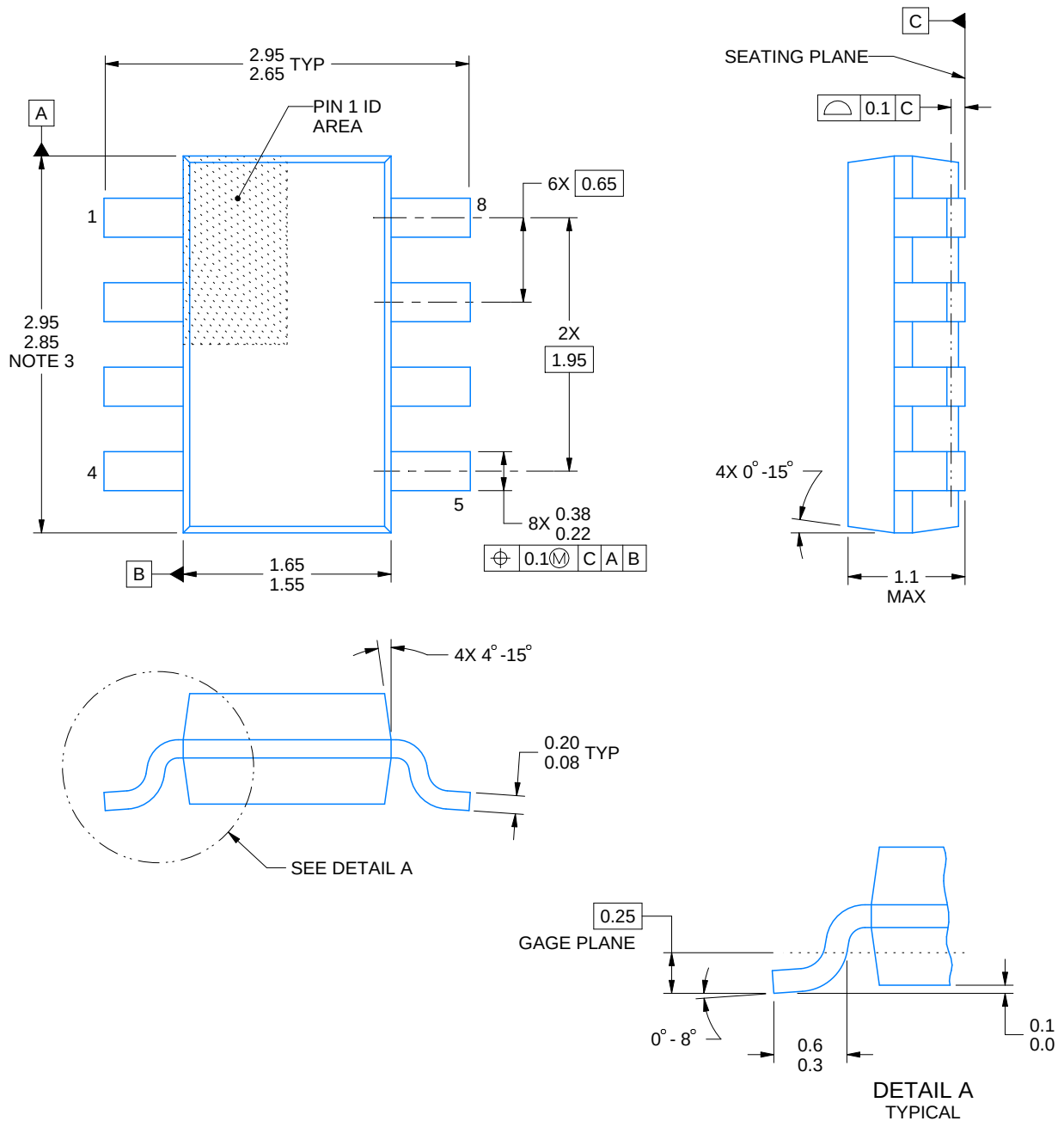


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3762D02OVDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

DDF0008A**PACKAGE OUTLINE****SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



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NOTES:

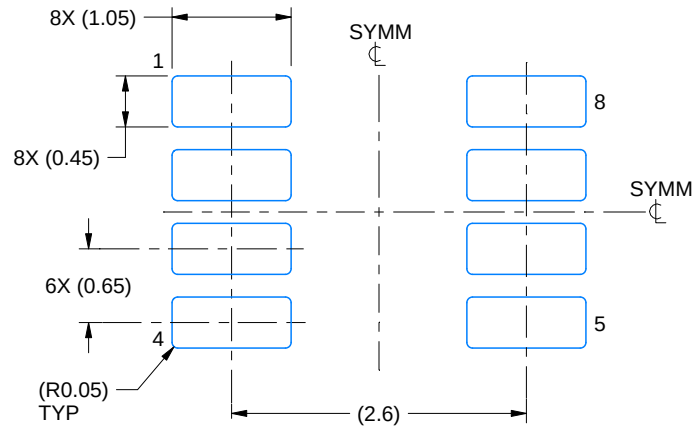
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

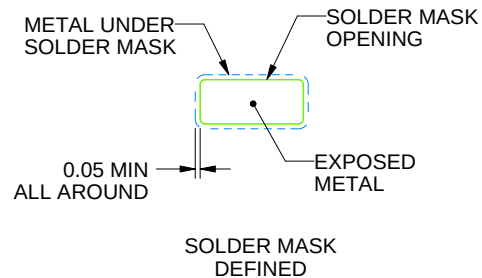
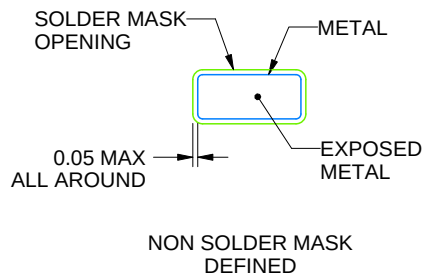
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

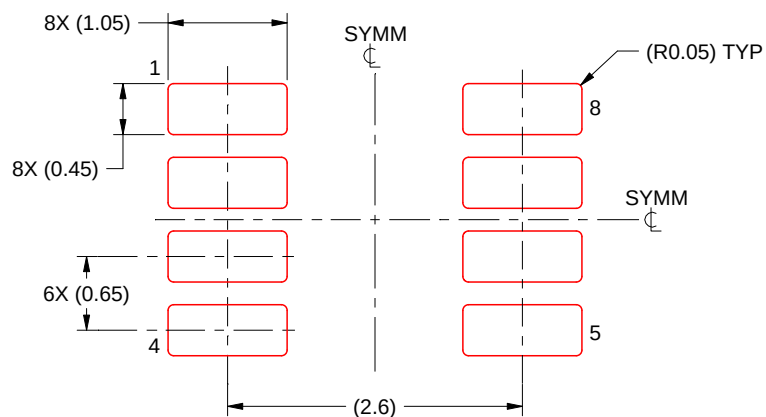
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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