TPS2HC08-Q1 9.4mΩ Dual-Channel Automotive Smart High-Side Switch

1 Features

- Dual-Channel smart high-side switch with full diagnostics
  - Control using GPIO pins
  - Open-drain status output
  - Current sense analog output, <±2.5% at ≥ 1A
- Wide operating voltage 3V to 28V
- Low R_{ON}: 9.4mΩ typical, 19mΩ max
- Ultra-low standby current, <1.5µA
- Adjustable current limit with and without thermal regulation
  - Current limit range: 7.5A to 30A
- Protection
  - Overload and short-circuit protection
  - Undervoltage lockout (UVLO)
  - Thermal shutdown and swing with self recovery
  - Integrated output clamp to demagnetize inductive loads
  - Loss-of-GND, loss-of-battery, and reverse battery protection
- Diagnostics
  - Global fault report for fast interrupt
  - Overcurrent and short-to-ground detection
  - Open-load and short-to-battery detection
- Qualified for automotive applications
  - AEC-Q100 qualified with the following results:
    - Temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Electrical transient disturbance immunity certification of ISO7637-2 and ISO16750-2
- Small footprint: 11-pin QFN 2.2mm × 3.6mm, 0.55mm pitch

2 Applications

- Incandescent and LED lighting
- Body control module
- Zone control module

3 Description

TPS2HC08-Q1 is a dual-channel, smart high-side switch, with integrated NMOS power FETs and charge pump, designed to meet the requirements of 12V automotive battery systems. The low RON (9.4mΩ) minimizes device power dissipation when driving a wide range of output load current up to 7.5A DC when both channels are enabled or 10A DC when only one channel is enabled.

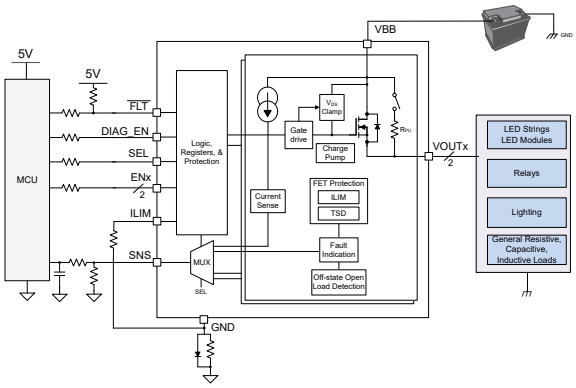
The device integrates protection features such as thermal shutdown, output clamp, and current limit. TPS2HC08-Q1 implements an adjustable current limiting circuit that improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current. The adjustable current limit can be adjusted from (7.5A to 30A) using an external resistor on the ILIM pin. The devices offers current limit settings with and without thermal regulation. The thermal regulated current limit can be useful when charging large capacitors at start-up. The current limit setting without thermal regulation is useful for loads such motor stall currents or bulb loads.

The device also provides an accurate load current sense that allows for improved load diagnostics such as overload and open-load detection enabling better predictive maintenance. TPS2HC08-Q1 is available in a 11-pin, 2.2mm × 3.6mm QFN leaded package with 0.55mm pin pitch minimizing the PCB footprint.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS2HC08-Q1	VAH (QFN, 11)	2.2mm × 3.6mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

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4 Device Comparison Table

Part Number	Current Limit	Current Limit Range	Current Limit with ILIM = GND	Overcurrent behavior
TPS2HC08-Q1	adjustable through external resistor	7.5A - 30A	30A	Current limiting with thermal regulation when external resistor is used on ILIM pin
				Current limiting with no thermal regulation when ILIM pin = GND

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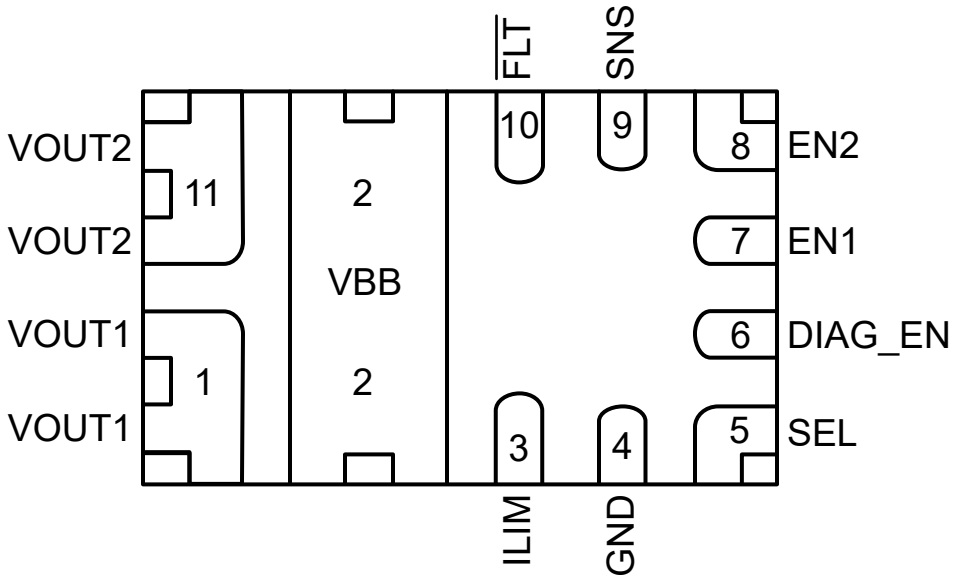
5 Pin Configuration and Functions



NC – No internal connection

Figure 5-1. VAH Package, TPS2HC08-Q1 (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VOUT1	Power	Channel 1 output, connect to load.
2	VBB	Power	Power supply.
3	ILIM	Output	Adjustable current limit. Connect R_{LIM} to GND to set the current limit.
4	GND	Power	Ground of device. Connect to resistor-diode ground network to have reverse battery protection.
5	SEL	Input	Selects the channel to output on the SNS pin.
6	DIAG_EN	Input	Enable-disable pin for diagnostics, internal pulldown.
7	EN1	Input	Input control for channel 1 activation, internal pulldown.
8	EN2	Input	Input control for channel 2 activation, internal pulldown.
9	SNS	Output	Analog current sense output corresponding to load current. Connect R_{SNS} to ground to convert to a voltage. Also shows fault status by going high.
10	$\overline{FLT}$	Output	Open drain global fault output. Referred to FAULT, FLT, or fault pin.
11	VOUT2	Power	Channel 2 output, connect to load.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum continuous supply voltage, V_{BB}			28	V
Load dump voltage, V_{LD}	ISO16750-2:2010(E)		35	V
Reverse Polarity Voltage	Maximum duration of 3 minutes and with the application circuit	–18		V
Enable pin current, I_{ENx}		–1	20	mA
Enable pin voltage, V_{ENx}		–1	7	V
Diagnostic Enable pin current, I_{DIAG_EN}		–1	20	mA
Diagnostic Enable pin voltage, V_{DIAG_EN}		–1	7	V
SEL pin current, I_{SEL}		–1	20	mA
SEL pin voltage, V_{SEL}		–1	7	V
Sense pin current, I_{SNS}		–100	10	mA
Sense pin voltage, V_{SNS}		–1	7	V
FLT pin current, I_{FLT}		-30	10	mA
FLT pin voltage, V_{FLT}		–0.3	7	V
Reverse ground current, I_{GND}	V_{BB} < 0V		–50	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per AEC Q100-002 Classification Level 2(2)	All pins except VBB and VOUT	±2000	V
			VBB and VOUT	±4000	
		Charged-device model (CDM), per AEC Q100-011 Classification Level C5	All pins	±750	

(1) All ESD strikes are with reference from the pin mentioned to GND
(2) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{VBB_NOM}	Nominal supply voltage (1)	4	18	V
V_{VBB_EXT}	Extended supply voltage(2)	3	28	V
V_{VBB_SC}	Short circuit supply voltage capability		26	V
V_{ENx}	Enable voltage	–1	5.5	V
V_{DIAG_EN}	Diagnostic Enable voltage	–1	5.5	V
V_{SEL}	Select voltage	–1	5.5	V
V_{SNS}	Sense voltage	–1	5.5	V

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6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	125	°C

(1) All operating voltage conditions are measured with respect to device GND
(2) Device functions within extended operating range, however some timing parametric values does not always apply. See the respective sections for what voltages are used. Additionally more explanation can be found in the Power Supply Recommendations.

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS2HC08-Q1 VAH 11 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.8	°C/W

(1) For more information about traditional and new thermal metrics, see the SPRA953 application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

6.5 Electrical Characteristics

V_{BB} = 6V to 18V, T_J = –40°C to 150°C (unless otherwise noted); Typical application is 13.5V, RILIM=Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
V_{UVLO}	V_{BB} undervoltage lockout	Measured with respect to device GND pin	V_{BB} rising threshold	3.7	3.85	4.0	V
			V_{BB} falling threshold	2.8	2.9	3.0	V
V_{DET1}	V_{BB} detection 1 threshold	Sleep state	V_{BB} rising threshold	20	22	24	V
		Active, diagnostic, or standby state		20	22	24	V
		Active, diagnostic, or standby state	V_{BB} falling threshold	18.5	19.5	20.5	V
V_{Clamp}	VDS clamp voltage	$V_{BB} \geq V_{DET1}$	T_J= 25°C	35		37	V
			T_J = –40°C to 150°C	31		42	V
		$V_{BB} < V_{DET1}$	T_J = –40°C to 150°C	24		33	V
I_{SLEEP}	Standby current (total device leakage including both MOSFET channels)	V_{ENx} = V_{DIAG_EN} = 0V, V_{OUT} = 0V	T_J = 25°C			1.2	µA
			T_J = 85°C			1.5	µA
			T_J = 150°C			20	µA
$I_{OUT(SLEEP)}$	Output leakage current per channel	V_{EN} = V_{DIAG_EN} = 0V, V_{OUT} = 0V	T_J = 25°C		0.01	0.2	µA
			T_J = 85°C			0.5	µA
I_{DIAG}	Diagnostic state current consumption	V_{ENx} = 0V, V_{DIAG_EN} = 5V, V_{OUT} = 0V, I_{SNS} = 0mA			1.9	3	mA
I_Q	Quiescent current	V_{ENx} = V_{DIAG_EN} = 5V, I_{OUTx} = 0A			2	3	mA

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6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, T_J = –40°C to 150°C (unless otherwise noted); Typical application is 13.5V, RILIM=Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{HV_R}	VBB high voltage wakeup threshold	V_{BB} voltage to transition from sleep to standby state	V_{BB} rising threshold	19	23	27	V
V_{HV_F}		V_{BB} voltage to transition from standby to sleep state	V_{BB} falling threshold	18			V
t_{STBY}	Standby mode delay time	V_{ENx} = V_{DIAG_EN} = 0V, V_{BB} < V_{HV_F} to standby			16		ms
RON CHARACTERISTICS							
R_{ON}	On-resistance	6V ≤ V_{BB} ≤ 28V, I_{OUT}= 1A	T_J = 25°C		9.4	10.5	mΩ
			T_J = 150°C			19	mΩ
		3V ≤ V_{BB} ≤ 6V, I_{OUT} =1A	T_J = 25°C		9.8	11	mΩ
			T_J = 150°C			20	mΩ
ΔR_{ON}	Delta On-resistance between channels	6V ≤ V_{BB} ≤ 28V, I_{OUT}= 1A	T_J= -40°C to 150°C		5		%
$R_{ON(REV)}$	On-resistance during reverse polarity	-18V ≤ V_{BB} ≤ -6V	T_J = 25°C		10	13	mΩ
			T_J = 150°C			20	mΩ
IL_{NOM}	Continuous load current, per channel	Two channels enabled, T_{AMB} = 85°C			7.5		A
		One channel enabled, T_{AMB} = 85°C			10		A
CURRENT SENSE CHARACTERISTICS							
V_{BB_ISNS}	V_{BB} headroom needed for full current sense and fault functionality	V_{DIAG_EN} = 3.3V		5.3			V
		V_{DIAG_EN} = 5V		6.5			V
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS}	I_{OUT} = 1A			3000		
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 10A		3007		
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 10A	-1.8		0.9	%
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 5A		3004		
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 5A	-1.8		0.8	%
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 2A		3001		
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 2A	-1.9		0.9	%
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 1A		3000		
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 1A	-2.2		1.5	%
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 500mA		2994		
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 500mA	-3.1		3.1	%
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 200mA		2975		
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 200mA	-6.8		7.7	%
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 100mA		2950		

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6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, T_J = –40°C to 150°C (unless otherwise noted); Typical application is 13.5V, RILIM=Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 100mA	-12.5		16.5	%
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 50mA		2909		
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 50mA	-26		36	%
$I_{SNSleak}$	I_{SNS} leakage	V_{DIAG_EN} = 5V, I_{OUT} = 0mA	T_J = 25°C			0.5	µA
			T_J = 125°C			1	µA
I_{SNSFH}	I_{SNS} fault high-level	V_{DIAG_EN} > $V_{IH,DIAG\_EN}$		5.2	7.4	10.5	mA
CURRENT LIMIT CHARACTERISTICS							
R_{ILIM}	R_{ILIM} Short Circuit Detection Range				16.66		kΩ
	R_{ILIM} Open Detection Range				66.66		kΩ
K_{CL}	Current Limit Ratio(1)	T_J = –40°C to 150°C	R_{ILIM} = 16.9kΩ	425	500	575	A × kΩ
			R_{ILIM} = 33.2kΩ	425	500	575	A × kΩ
			R_{ILIM} = 66.5kΩ	425	500	575	A × kΩ
I_{CL}	I_{CL} Current Limit Threshold	T_J = –40°C to 150°C	R_{ILIM} = GND		30		A
			R_{ILIM} = OPEN		7.5		A
I_{CB}	Peak current threshold when short is applied while switch enabled	R_{ILIM} = 16.9kΩ to 66.5kΩ	T_J = –40°C	23			A
			T_J = 25°C		25		A
			T_J = 150°C	22			A
V_{DET2}	VBB detection 2 threshold	active state	V_{BB} rising threshold	25.2	26.5	27.8	V
			V_{BB} falling threshold	23	24.3	25.5	V
I_{CL_HV}	I_{CL} current limit derating at high voltage	T_J = –40°C to 150°C	V_{BB} < V_{DET1}		I_{CL}		A
			V_{DET1} ≤ V_{BB} < V_{DET2}		I_{CL}	20	
			V_{BB} ≥ V_{DET2}		I_{CL}	10	
I_{CL_LNPK}	Linear mode peak	T_J = –40°C to 150°C	R_{ILIM} ≥ 24.9kΩ			1.45 × I_{CL}	A
			R_{ILIM} < 24.9kΩ		1.45 × I_{CL}	I_{CB}	A
FAULT CHARACTERISTICS							
V_{OL}	Open-load detection voltage (VDS voltage)	V_{EN} = 0V, V_{DIAG_EN} = 5V, diagnostic state		1.5	2	2.5	V
R_{VOL}	Open-load (OL) detection internal pull-up resistor per channel	V_{EN} = 0V, V_{DIAG_EN} = 5V, diagnostic state			75		kΩ
t_{OL}	Open-load (OL) detection deglitch time	V_{EN} = 0V, V_{DIAG_EN} = 5V, When V_{BB} – V_{OUT} < V_{OL}, duration longer than t_{OL}		150		500	µs
t_{OL1}	OL and STB indication-time from EN falling	V_{EN} = 5V to 0V, V_{DIAG_EN} = 5V I_{OUT} = 0mA, V_{OUT} = V_{BB} - V_{OL}		150		500	µs
t_{OL2}	OL and STB indication-time from DIAG_EN rising	V_{EN} = 0V, V_{DIAG_EN} = 0V to 5V I_{OUT} = 0mA, V_{OUT} = V_{BB} - V_{OL}		150		3200	µs
t_{OL3}	OL and STB indication-time from V_{OUT} rising	V_{EN} = 0V, V_{DIAG_EN} = 5V, I_{OUT} = 0mA, V_{OUT} = 0V to V_{BB} - V_{OL}		150		1600	µs
T_{ABS}	Thermal shutdown			150	165	187	°C
T_{REL}	Relative thermal shutdown				85		°C

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6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, T_J = –40°C to 150°C (unless otherwise noted); Typical application is 13.5V, RILIM=Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{HYS}	Thermal shutdown hysteresis			28		°C
V_{FLT}	$\overline{FLT}$ low output voltage	$I_{\overline{FLT}}$ = 2.5mA			0.2	V
t_{FAULT_FLT}	Fault indication-time	V_{DIAG_EN} = 5V, time between fault and $\overline{FLT}$ asserting			20	µs
t_{FAULT_SNS}	Fault indication-time	V_{DIAG_EN} = 5V, time between fault and I_{SNS} settling at V_{SNSFH}			30	µs
t_{RETRY_WINDOW}	Initial retry time window			50		ms
$t_{RETRY, INT}$	Retry time in initial retry window	Time from thermal shutdown to switch re-enable	100	200	300	µs
$t_{RETRY,EXTD}$	Retry time in extended overcurrent window		50	100	150	ms
$n_{RETRY,EXTD}$	Number of retry cycles in extended overcurrent window			7		
EN PIN CHARACTERISTICS						
$V_{IL, ENx}$	Input voltage low-level	No GND Network			0.8	V
$V_{IH, ENx}$	Input voltage high-level		1.5			V
$V_{IHYS, ENx}$	Input voltage hysteresis			280		mV
R_{ENx}	Internal pulldown resistor		150	250	500	kΩ
$I_{IL,\_ENx}$	Input current low-level	V_{ENx} = 0.8V	1.6	2.2	4	µA
$I_{IH, ENx}$	Input current high-level	V_{ENx} = 5V	19	25	35	µA
DIAG_EN PIN CHARACTERISTICS						
$V_{IL, DIAG\_EN}$	Input voltage low-level	No GND Network			0.8	V
$V_{IH, DIAG\_EN}$	Input voltage high-level		1.5			V
$V_{IHYS, DIAG\_EN}$	Input voltage hysteresis			280		mV
R_{DIAG_EN}	Internal pulldown resistor		100	250	500	kΩ
$I_{IL, DIAG\_EN}$	Input current low-level	V_{DIAG_EN} = 0.8V	3	4	7.5	µA
$I_{IH, DIAG\_EN}$	Input current high-level	V_{DIAG_EN} = 5V	19	25	35	µA
SEL PIN CHARACTERISTIC						
$V_{IL, SEL}$	Input voltage low-level	No GND Network			0.8	V
$V_{IH, SEL}$	Input voltage high-level		1.5			V
$V_{IHYS, SEL}$	Input voltage hysteresis			280		mV
R_{SEL}	Internal pulldown resistor		100	250	500	kΩ
$I_{IL, SEL}$	Input current low-level	V_{SEL} = 0.8V	1.8	2.3	3	µA
$I_{IH, SEL}$	Input current high-level	V_{SEL} = 5V	11	15	20	µA

(1) To calculate I_{CL} from K_{CL} use equation $I_{CL} = K_{CL} / R_{ILIM}$

6.6 SNS Timing Characteristics

V_{BB} = 6V to 18V, V_{ENx} = 5V, V_{DIAG_EN} = 5V, R_{SNS} = 1kΩ, T_J = –40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNS TIMING - CURRENT SENSE						
$t_{SNSION1}$	Settling time from rising edge of DIAG_EN	V_{DIAG_EN} = 0V to 5V, I_{OUTx} = 1A			15	µs
		V_{DIAG_EN} = 0V to 5V, I_{OUTx} = 50mA			15	µs

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6.6 SNS Timing Characteristics (continued)

V_{BB} = 6V to 18V, V_{ENx} = 5V, V_{DIAG_EN} = 5V, R_{SNS} = 1kΩ, T_J = –40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SNSION2}$	Settling time from rising edge of EN and DIAG_EN, 50% of V_{DIAG_EN}, V_{EN} to 90% of I_{SNS}	V_{EN} = V_{DIAG_EN} = 0V to 5V, I_{OUTx} = 1A			230	µs
$t_{SNSION3}$	Settling time from rising edge of EN with DIAG_EN = HI, 50% of V_{EN} to 90% of I_{SNS}	V_{ENx} = 0V to 5V, V_{DIAG_EN} = 5V, I_{OUTx} = 1A			150	µs
$t_{SNSIOFF}$	Settling time from falling edge of DIAG_EN, 50% of V_{DIAG_EN} to 5% of I_{SNS}	V_{ENx} = 5V, V_{DIAG_EN} = 5V to 0V , I_{OUTx} = 1A			10	µs
$t_{SETTLEH}$	Settling time from rising edge of load step	I_{OUTx} = 50mA to 1A			10	µs
$t_{SETTLEL}$	Settling time from falling edge of load step	I_{OUTx} = 1A to 50mA			10	µs
t_{MUX}	Settling time from switching from CHx to CHy	V_{SEL} = 0V to 5V, I_{OUT1} = 50mA, I_{OUT2} = 1A			20	µs
t_{MUX}	Settling time from switching from CHx to CHy with an open load fault	V_{EN1} = 5V, V_{EN2} = 0V, V_{SEL} = 0V to 5V, I_{OUT1} = 1A, CH2 = I_{SNSFH}			20	µs

6.7 Switching Characteristics

V_{BB} = 13.5V, R_L = 10Ω, T_J = –40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Channel Turn-on delay time	50% of ENx to 20% of VOUTx from standby state	6	20	45	µs
		50% of ENx to 20% of VOUTx from sleep state	10	55	90	µs
t_{DF}	Channel Turn-off delay time	50% of ENx to 80% of VOUTx	40	70	105	µs
SR_R	VOUT rising slew rate	20% to 80% of VOUT, OTP = 1b, 1.3 Ω load	0.02	0.06	0.1	V/µs
SR_R	VOUT rising slew rate	20% to 80% of VOUTx, OTP = 0b, 1.3 Ω load	0.3	0.45	0.61	V/µs
SR_F	VOUT falling slew rate	80% to 20% of VOUT, OTP = 1b, 1.3 Ω load	0.02	0.06	0.1	V/µs
SR_F	VOUT falling slew rate	80% to 20% of VOUT, OTP = 0b, 1.3 Ω load	0.3	0.4	0.8	V/µs
t_{ON}	Channel Turn-on time	50% of EN to 80% of VOUT, from standby state	20	45	90	µs
t_{OFF}	Channel Turn-off time	50% of EN to 20% of VOUT	50	90	130	µs
$t_{ON} – t_{OFF}$	Turn-on and off matching	1ms enable pulse	–75		40	µs
		200µs enable pulse	–75		40	µs
Δ_{PWM}	PWM accuracy - average load current	200µs enable pulse (1ms period)	–35		25	%
		≤500Hz, 50% Duty cycle	–12		12	%
E_{ON}	Switching energy losses during turn-on	V_{BB} = 18V, R_L = 3.3Ω, 10% to 90% of VOUT		0.576		mJ
E_{OFF}	Switching energy losses during turn-off	V_{BB} = 18V, R_L = 3.3Ω, 10% to 90% of VOUT		0.584		mJ

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7 Parameter Measurement Information

For reference purposes throughout the data sheet, current directions on the respective pins are as shown by the arrows in Figure 7-1. All voltages are measured relative to the ground plane.

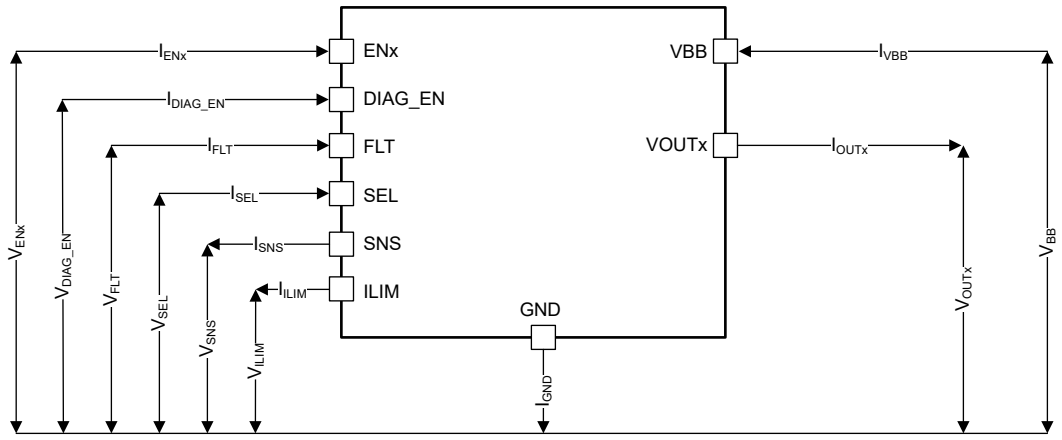
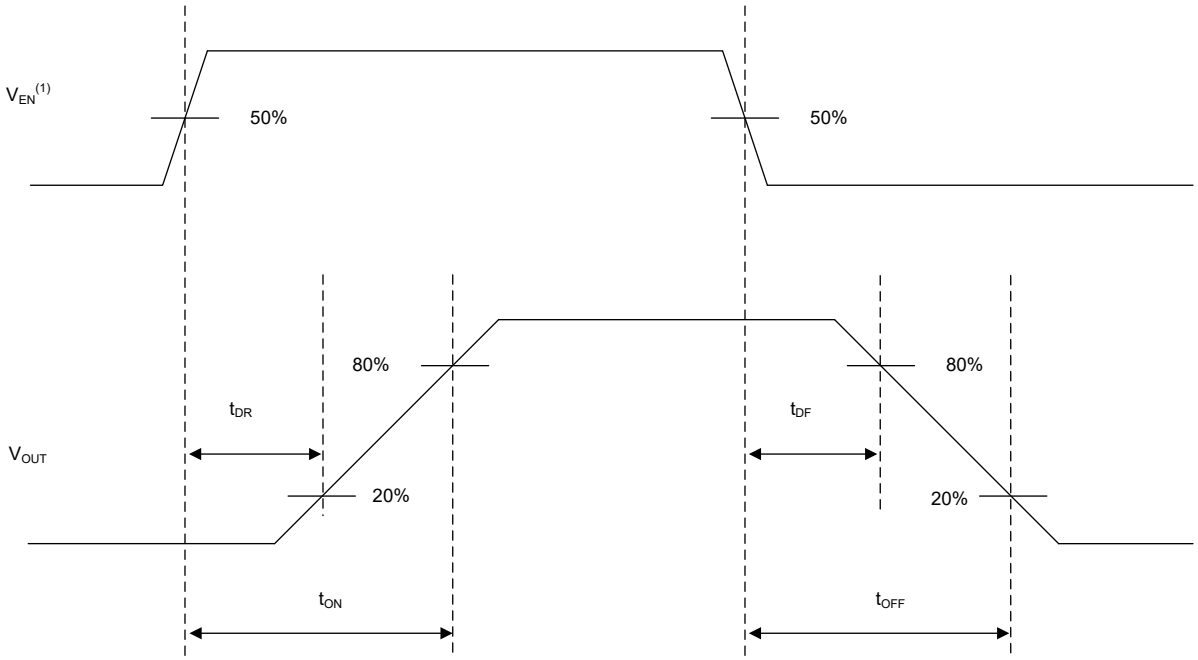


Figure 7-1. Voltage and Current Conventions



Rise and fall time of VEN is 100 ns.

Figure 7-2. Switching Characteristics Definitions

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8 Detailed Description

8.1 Overview

The TPS2HC08-Q1 is a dual-channel, fully-protected, high side power switch with an integrated NMOS power FETs and charge pump. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The device offers two pins to support both digital status and analog current-sense output. The current-sense output can be set to high-impedance state when diagnostics are disabled, which can enable multiplexing of the MCU analog interface between multiple devices.

The device has logic pins to enable each of the four channels and a separate pin to enable the diagnostic output with two pins to select the channel to be output on the analog current SNS pin. The device also implements a global FLT pin to be used as an interrupt to the MCU. The global FLT is implemented with an open-drain structure. When a fault condition occurs, the pin is pulled down to GND. An external pullup is required to match the microcontroller supply level.

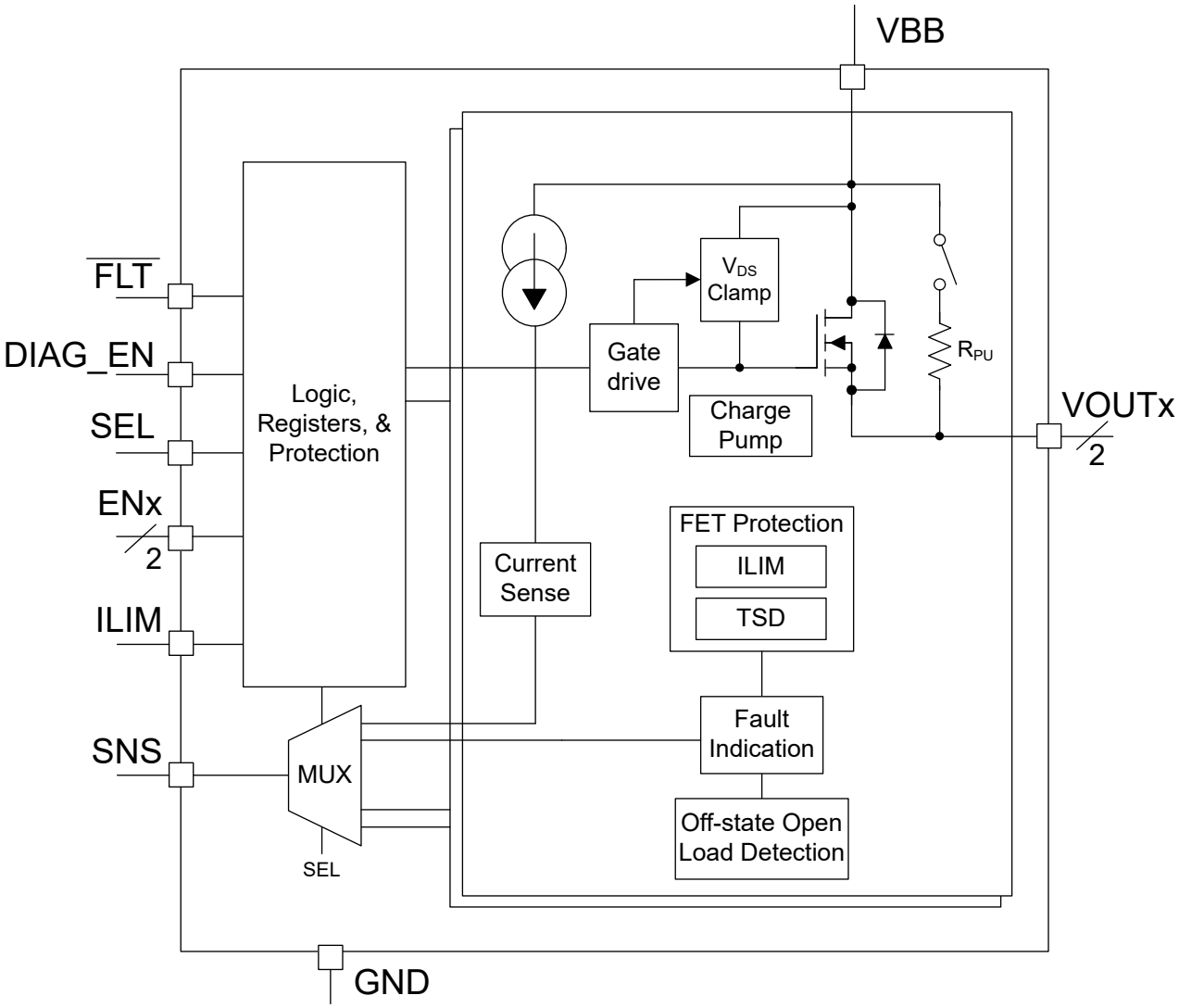
High-accuracy current sensing allows for better real-time monitoring and more-accurate diagnostics without additional in-line calibration. A current mirror is used to source 1 / K_{SNS} of the load current, which is reflected as voltage across a resistor on the SNS pin. K_{SNS} is a constant value across the temperature and supply voltage. The SNS pin can also report a fault by forcing a voltage of V_{SNSFH} that scales with the diagnostic enable voltage so that the maximum voltage seen by the system ADC is within an acceptable value. This action removes the need for an external Zener diode or resistor divider on the SNS pin.

The device also offers a programmable current-limit function which greatly improves the reliability of the whole system. The current limit highly improves the reliability of the system by clamping the inrush current effectively under start-up when charging large capacitances or during short-circuit conditions. The high-accuracy current limit of the device can be set using an external resistor to 7.5A to 30A. An internal current limit is also implemented in this device when the ILIM pin is connected to ground through a resistor. The devices also offers current limit settings with and without thermal regulation. The thermal regulated current limit can be useful when charging large capacitors at startup. The current limit setting without thermal regulation is useful for loads such high motor stall currents or bulb loads.

A voltage clamp is built in to address switching off the energy of inductive loads, such as relays, solenoids, pumps, motors, and so forth. During the inductive switching-off cycle, both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high side power switch. With the benefits of process technology and excellent IC layout, the TPS2HC08-Q1 device can achieve excellent power dissipation capacity, which can help save the external free-wheeling circuitry in most cases. For more details, see Inductive-Load Switching-Off Clamp.

The TPS2HC08-Q1 device can be used as a high side power switch for a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, and heaters.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Accurate Current Sense

The high-accuracy current-sense function is internally implemented, which allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source 1 / K_{SNS} of the load current, flowing out to the external resistor between the SNS pin and GND, and reflected as voltage on the SNS pin.

K_{SNS} is the ratio of the output current and the sense current. The accuracy values of K_{SNS} quoted in the electrical characteristics do take into consideration temperature and supply voltage. Each device is internally calibrated while in production, so post-calibration by users is not required in most cases.

The sense resistor value, R_{SNS}, can be chosen to maximize the range of currents needed to be measured by the system. The R_{SNS} value must be chosen based on application need. The minimum R_{SNS} value is bounded by the ADC minimum acceptable voltage, $V_{ADC,min}$, for the smallest load current needed to be measured by the system, $I_{LOAD,min}$. The maximum R_{SNS} value is chosen to verify that the V_{SNS} voltage is below the V_{SNSFH} value so that the system can determine faults from normal load currents. This difference between the maximum readable current through the SNS pin, $I_{LOAD,max} \times R_{SNS}$, and the V_{SNSFH} is called the headroom voltage, V_{HR}. The headroom voltage is determined by the system but is important so that there is a difference between the

maximum readable current and a fault condition. Therefore, the maximum R_{SNS} value has to be the V_{SNSFH} minus the V_{HR} times the sense current ratio, K_{SNS} divided by the maximum load current the system must measure, $I_{LOAD,max}$. Use the following equation to see the boundary equation.

$$V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \leq R_{SNS} \leq (V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \quad (1)$$

In some applications, where there is a higher load current range the above boundary equation can only satisfy either the lower or upper bound. In these cases, more emphasis can be put on the lower measurable current values which increases R_{SNS}. Likewise, if the higher currents are of more interest the R_{SNS} can be decreased.

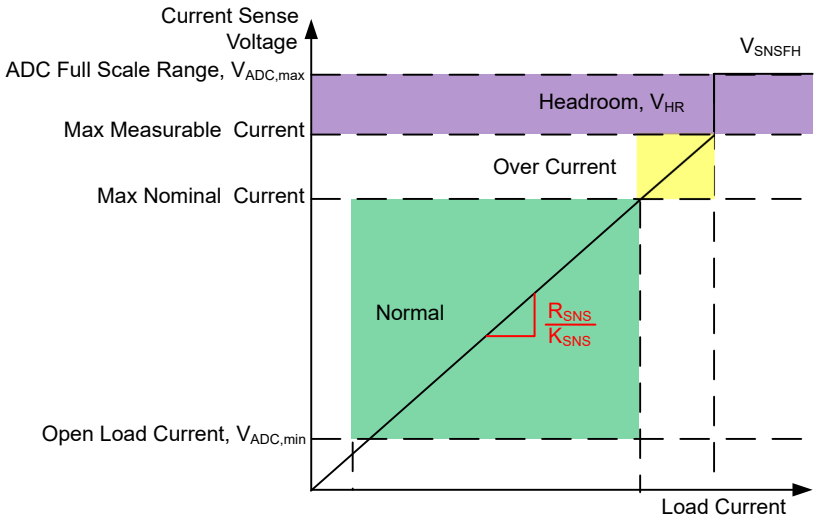

Figure 8-1. Voltage Indication on the Current-Sense Pin

The maximum current the system wants to read, $I_{LOAD,max}$, must be below the current-limit threshold because after the current-limit threshold is tripped the V_{SNS} value goes to V_{SNSFH}.

8.3.2 Overcurrent Protection

The TPS2HC08-Q1 provides thermal shutdown and current limiting protection during overcurrent events to protect the internal power MOSFETs. These protection functions are enabled when the device is in the active state. Each channel has an independent thermal shutdown and current limiting circuitry.

8.3.2.1 Thermal Shutdown

The device includes a temperature sensor on each power FET and within the controller portion of the device to monitor the temperature of each FET ($T_{J,FET}$) and the temperature of the controller ($T_{J,CONTROLLER}$). There are two cases that the device considers to be a thermal shutdown fault:

- **Relative thermal shutdown (T_{REL}):** $T_{J,FET} - T_{J,CONTROLLER} > T_{REL}$
- **Absolute thermal shutdown (T_{ABS}):** $T_{J,FET} > T_{ABS}$

If either the above faults occur, the relevant switch is turned off. Each channel is turned off based on the measurement of the temperature sensor for that channel. As result, if the thermal fault is detected on only one channel, the other channel continues operation.

8.3.2.1.1 Relative Thermal Shutdown

A relative thermal shutdown event can occur when there is a large peak power event such as a short-to-ground event where the FET temperature ($T_{J,FET}$) quickly rises relative to the controller temperature ($T_{J,CONTROLLER}$). Once the relative temperature ($T_{J,FET} - T_{J,CONTROLLER}$) exceeds T_{REL} the relevant channel is turned off.

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8.3.2.1.2 Absolute Thermal Shutdown

An absolute thermal shutdown occurs when the FET temperature ($T_{J,FET}$) rises above T_{ABS}. This can occur when a channel is subjected to long durations of overcurrent such as a permanent short use case. Once the FET temperature ($T_{J,FET}$) exceeds T_{ABS} the relevant channel is turned off.

8.3.2.2 Adjustable Current Limit

The TPS2HC08-Q1 offers a high accuracy, adjustable current which enables higher reliability and provides protection to the power supply during a short circuit or power up with large capacitance. An adjustable current limit can also save system costs by reducing PCB traces, connector size, and the capacity of the preceding power stage by setting the current limit at a lower level.

The current limit of the device can be adjusted via an external resistor on the ILIM pin. The value which is set by the ILIM pin is applied to both the channels. The device provides ILIM settings with a thermal regulated current limit which adjusts the current limit level based on the relative temperature of the FET and the controller to enable the device to charge up large capacitors at startup. The device also offers ILIM settings without thermal regulation where the device limits the current at the set ILIM value. Table 8-1 details the different settings that are possible based on the ILIM pin configuration.

Table 8-1. Current Limit settings through ILIM pin

R_{ILIM} Value	Typ ILIM	Thermal Regulation
GND (< 16.66kΩ)	30A	Disabled
16.9kΩ	30A	Enabled
66.5kΩ	7.5A	Enabled
Open (> 66.66kΩ)	7.5A	Enabled

The device also offers a fast-trip circuit breaker function which is used when a short-circuit occurs while a channel is enabled which is also known as a hot-short. Once the I_{CB} threshold is reached, the device quickly turns off the channel to protect the internal MOSFET. Additionally, the device provides a current limit foldback function at higher voltages to help protect the internal power MOSFETs during high V_{DS} events.

The different overcurrent events that can occur in a system are:

- hot-short
- enable into short
- current overload (slow creep)

A hot-short occurs when a channel is enabled and a short-circuit condition is applied to the output of a channel. Enabling in to short occurs when there is already a short on the output of the MOSFET and the channel is enabled into the short-circuit condition. Current overload or also known as slow creep can occur if there is a slow rising overcurrent event at the output.

The next sections describe how the current limiting with thermal regulation and without thermal regulation work along with the circuit breaker and thermal shutdown functions to help protect against the various overcurrent conditions that can occur.

8.3.2.2.1 Current Limiting With Thermal Regulation

Based on the ILIM setting the device can be configured to limit current with thermal regulation. The thermal regulation works by monitoring the relative temperature of the MOSFET ($T_{J,FET}$) to the temperature of controller ($T_{J,CONTROLLER}$) and reducing the current limit based on the relative temperature.

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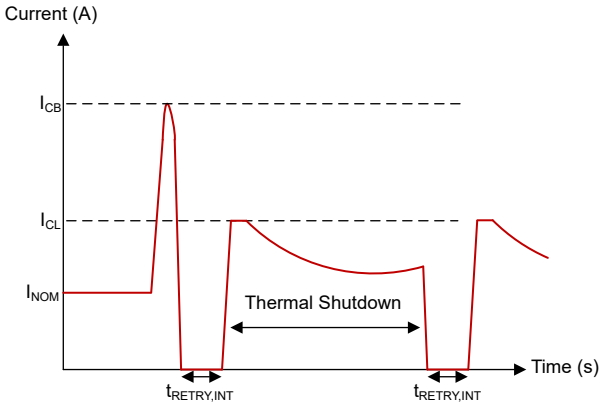

Figure 8-2. On-state Short-circuit Behavior With Thermal Regulation

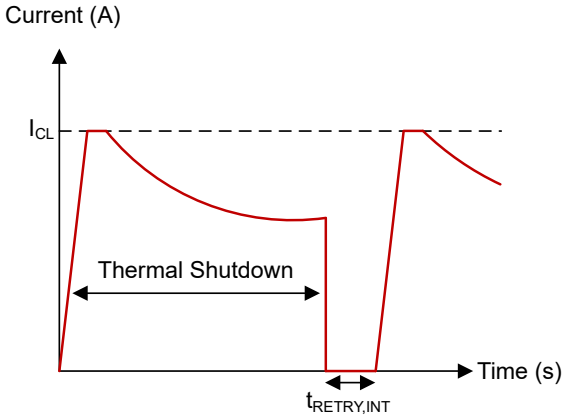

Figure 8-3. Enable Into Short With Thermal Regulation

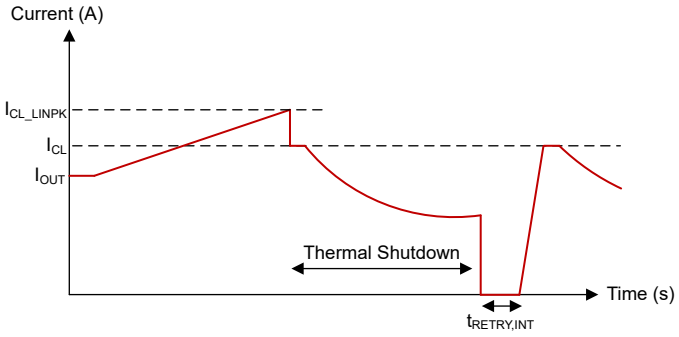

Figure 8-4. Overload Behavior (Current Creep) With Thermal Regulation

8.3.2.2.2 Current Limiting With No Thermal Regulation

Based on the ILIM setting, the device can be configured to limit current without thermal regulation. The device limits the current based on the setting at the ILIM pin. Applications where this can be used are bulb loads and motor loads with high stall currents.

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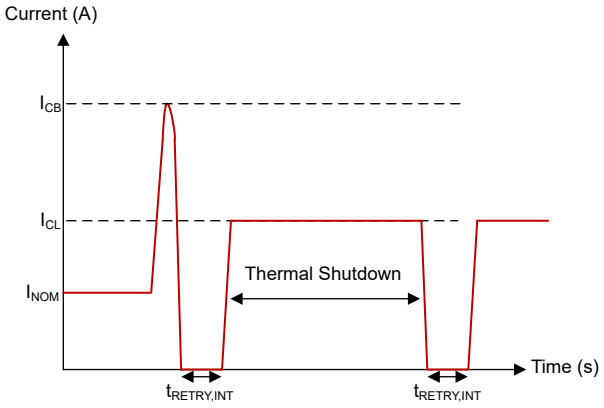

Figure 8-5. On-state Short-circuit Behavior With No Thermal Regulation

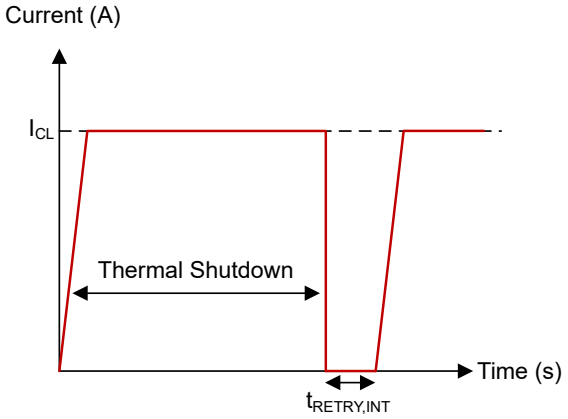

Figure 8-6. Enable Into Short With No Thermal Regulation

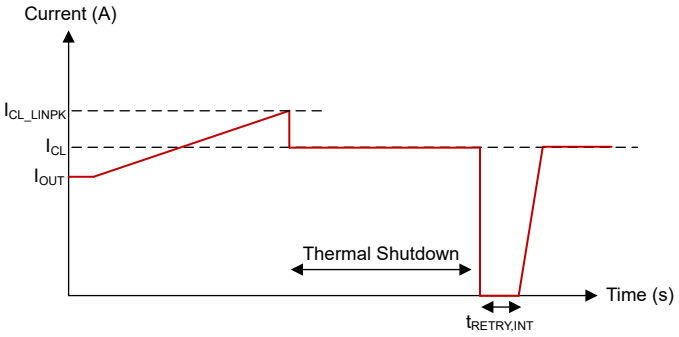

Figure 8-7. Overload Behavior (Current Creep) With No Thermal Regulation

8.3.2.2.3 Current Limit Foldback

To protect the MOSFET from overcurrent at high V_{DS} voltages the device offers a current limit foldback mechanism. If the ILIM is set to greater than 20A and the V_{BB} voltage is greater than V_{DET1} then the current limit folds back to 20A. If the V_{BB} voltage is above V_{DET2}, the current limit folds back 10A if the ILIM setting is greater than 10A.

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8.3.3 Retry From Thermal Shutdown

When a thermal shutdown occurs on a channel, the device can respond using three methods depending on the duration of the overcurrent event. Table 8-2 explains how the affected channel responds depending on the time in overcurrent and the number of retries that occur.

Table 8-2. Response To Thermal Shutdown

Conditions		Retry time
$t < t_{RETRY\_WINDOW}$		200µs (typical)
$t > t_{RETRY\_WINDOW}$	$n_{RETRY,EXTD} < 7$	100ms (typical)
	$n_{RETRY,EXTD} > 7$	Latch-off

In any of the above retry cases the relevant channel must wait for the t_{retry} interval and the T_{ABS} or T_{REL} to recover below the T_{HYS} level to restart the device. If the retry timer has expired and the temperature of T_{ABS} or T_{REL} has not recovered below the T_{HYS} level, the channel does not retry until the temperature falls below the T_{HYS} level.

Once a channel latches off due to an extended overcurrent event, the ENx pin can be brought from high to low to clear the thermal shutdown fault. The FLT pin is pulled high and the SNS pin no longer outputs I_{SNSFH} or V_{SNSFH}. The output of the channel then follows the ENx pin after the initial toggle from high to low. Figure 8-8 and Figure 8-9 below shows how the device retries after a hot-short on VOUT1 with and without thermal regulation, respectively.

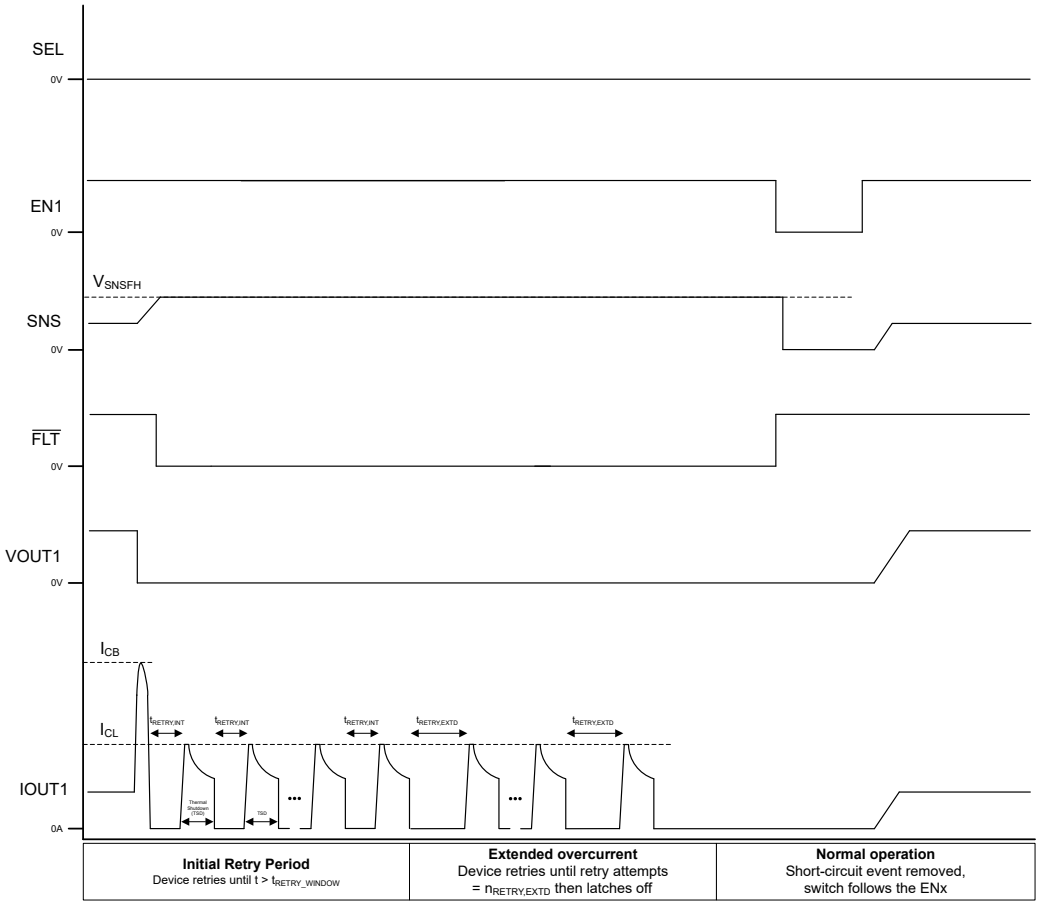

Figure 8-8. Retry Behavior After Hot-short With Thermal Regulation

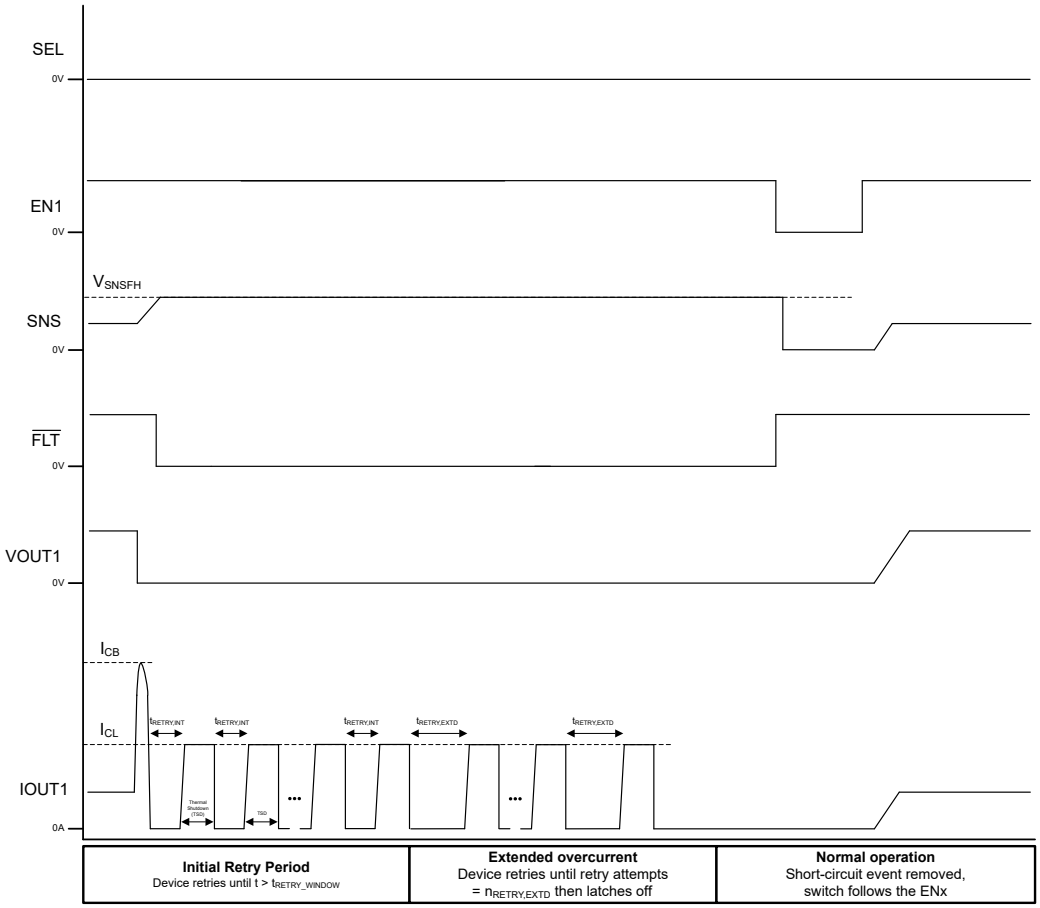

Figure 8-9. Retry Behavior After Hot-short With No Thermal Regulation

8.3.4 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage can cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

$$V_{DS(clamp)} = V_{VS} - V_{OUT} \quad (2)$$

During the period of demagnetization (t_{decay}), the power FET is turned on for inductance-energy dissipation. The total energy is dissipated in the high-side switch. Total energy includes the energy of the power supply ($E_{(VS)}$) and the energy of the load ($E_{(load)}$). If resistance is in series with inductance, some of the load energy is dissipated on the resistance.

$$E_{(HSS)} = E_{(VS)} + E_{(load)} = E_{(VS)} + E_{(L)} - E_{(R)} \quad (3)$$

When an inductive load switches off, $E_{(HSS)}$ causes high thermal stressing on the device.. The upper limit of the power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

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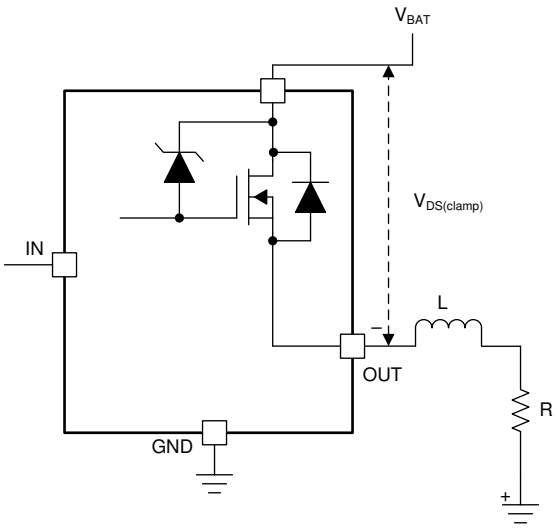

Figure 8-10. Drain-to-Source Clamping Structure

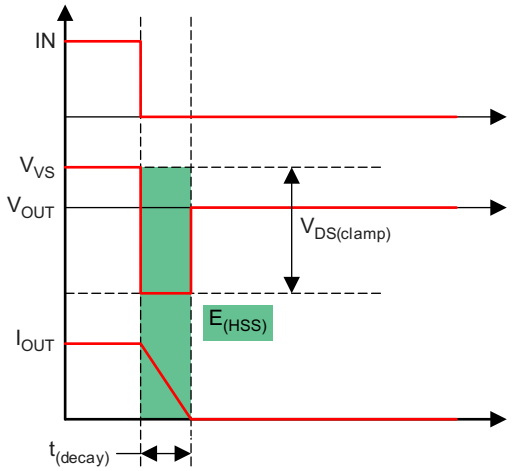

Figure 8-11. Inductive Load Switching-Off Diagram

From the perspective of the high-side switch, $E_{(HSS)}$ equals the integration value during the demagnetization period.

$$E_{(HSS)} = \int_0^{t_{(decay)}} V_{DS(clamp)} \times I_{OUT}(t)dt$$

$$t_{(decay)} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)$$

$$E_{(HSS)} = L \times \frac{V_{VS} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(max)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \quad (4)$$

When R approximately equals 0, $E_{(HSD)}$ can be given simply as:

$$E_{(HSS)} = \frac{1}{2} \times L \times I_{OUT(max)}^2 \frac{V_{VS} + |V_{OUT}|}{|V_{OUT}|} \quad (5)$$

Note that for PWM-controlled inductive loads, adding the external freewheeling circuitry as shown in Figure 8-12 is recommended to protect the device from repetitive power stressing. TVS is used to achieve the fast decay. See Figure 8-12 for more details.

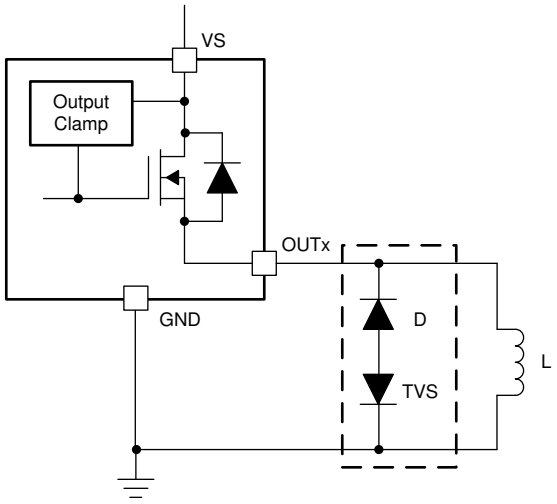

Figure 8-12. Protection With External Circuitry

8.3.5 Fault Detection and Reporting

8.3.5.1 Diagnostic Enable Function

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the MCU can use GPIOs to set DIAG_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and ENx low.

8.3.5.2 Multiplexing of Current Sense

The SEL pin is used to multiplex the shared current-sense function among the two channels. Pulling the SEL pin high or low sets the corresponding channel to be output on the SNS pin if DIAG_EN is high. $\overline{\text{FLT}}$ still represents a global interrupt that goes low if a fault occurs on any channel.

Table 8-3. Diagnosis Configuration Table

DIAG_EN	ENx	SEL	SNS ACTIVATED CHANNEL	SNS	$\overline{\text{FLT}}$	PROTECTIONS AND DIAGNOSTICS
L	H	—	—	High impedance	See Table 8-4	SNS disabled, $\overline{\text{FLT}}$ reporting, full protection
	L				High impedance	Diagnostics disabled, no protection
H	—	0	Channel 1	See Table 8-4	See Table 8-4	See Table 8-4
		1	Channel 2			

8.3.5.3 $\overline{\text{FAULT}}$ Reporting

The global $\overline{\text{FLT}}$ pin is used to monitor the global fault condition among the two channels. When a fault condition occurs on any channel, the $\overline{\text{FLT}}$ pin is pulled down to GND. A 3.3V or 5V external pullup is required to match the supply level of the microcontroller.

After the $\overline{\text{FAULT}}$ report, the microcontroller can check and identify the channel in fault status by the multiplexed current sensing. The SNS pin also works as a fault report with an internal pullup voltage, V_{SNSFH} if DIAG_EN is high.

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8.3.5.4 Fault Table

Table 8-4 below shows the response of the FLT and SNS pins when DIAG_EN = HIGH during different conditions.

Table 8-4. Fault Table

CONDITIONS	ENx	OUTx	CRITERION	SNS	$\overline{FLT}$	FAULT RECOVERY
Normal	L	L	—	0	H	—
	H	H	—	In linear region	H	—
Overload, short to ground	H	L	Current limit triggered	V_{SNSFH}	L	Auto
Open load, short to battery, reverse polarity	L	H	$V_{VS} - V_{OUTx} < V_{(ol,off)}$	V_{SNSFH}	L	Auto
Absolute Thermal shutdown	H	—	T_{ABS} triggered	V_{SNSFH}	L	Auto-retry or latch, see Section 8.3.3
Relative Thermal Shutdown	H	—	T_{REL} triggered	V_{SNSFH}	L	Auto-retry or latch, see Section 8.3.3

8.3.6 Full Diagnostics

8.3.6.1 Open-Load Detection

8.3.6.1.1 Channel On

If a channel is on and the DIAG_EN = HI, then the high accuracy current sense of the device can be used to detect open-loads in the on state through an external ADC. Please note there is no detection reported on the $\overline{FAULT}$ pin. Determination of an open-load while a channel is on must be made by the user or system.

8.3.6.1.2 Channel Off

Open load detection is available in the off state if DIAG_EN = HI. If a channel is off and a load is connected to the relevant channel, the output voltage is pulled low to ≅0V by the load. In the case of an open load on the channel, the output voltage is close to the supply voltage, $V_{BB} - V_{OUT} < V_{ol,off}$. The FLT pin goes low to indicate a fault to the MCU. If the particular channel experiencing the open load fault is selected through the SEL pin, then the SNS pin outputs I_{SNSFH} or clamps the voltage to V_{SNSFH}. If the channel is not selected through the SEL pin then the SNS pin does not show I_{SNSFH} until the channel is selected through the SEL pin. There is always a leakage current Iol,off present on the output, due to the internal logic control path or external humidity, corrosion, and so forth. Thus, the device implements an internal pullup resistor (RPU) on each channel to offset the leakage current. This pullup current must be less than the output load current to avoid false detection in the normal operation mode. To reduce the standby current, the device implements a switch and pullup resistor on each channel which is controlled by the DIAG_EN pin and the EN pin for that channel.

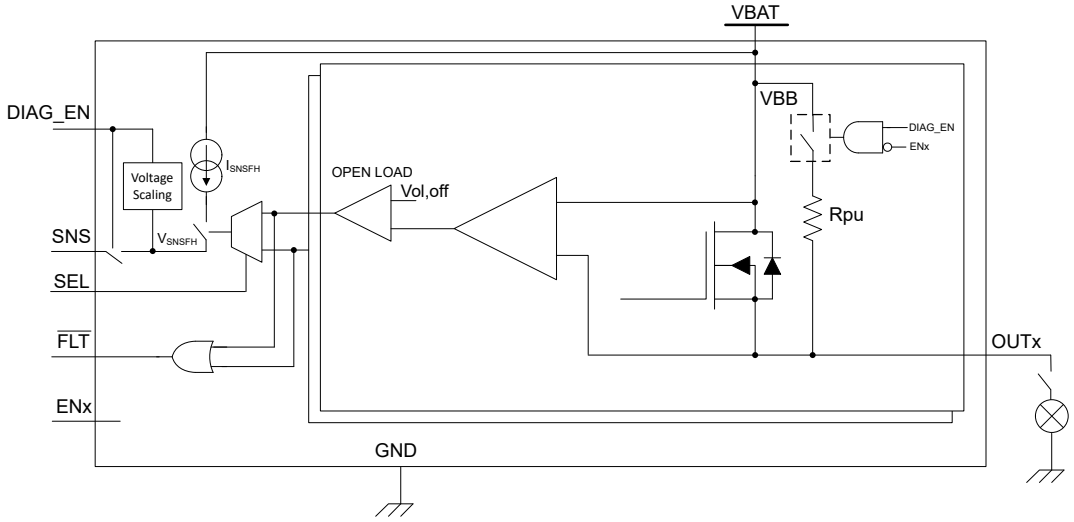


Figure 8-13. Open-Load Detection in Off-State

8.3.6.2 Short-to-Battery Detection

Short-to-battery detection has the same detection mechanism and behavior as open-load detection, both in the on-state and off-state. The device is not able to differentiate between open load and short-to-battery, the device does detect the short-to-battery fault and can signal the fault to the system. See Table 8-4 for more details.

8.3.6.3 Reverse-Polarity and Battery Protection

Reverse-polarity, commonly referred to as reverse battery, occurs when the ground of the device goes to the battery potential, $V_{GND} = V_{BAT}$, and the supply pin goes to ground, V_{BB} = 0V. In this case, if the EN pin has a path to the *ground* plane, then the FET turns on to lower the power dissipation through the main channel and prevent current flow through the body diode. Note that the resistor/diode ground network (if there is not a central blocking diode on the supply) must be present for the device to protect the device during a reverse battery event.

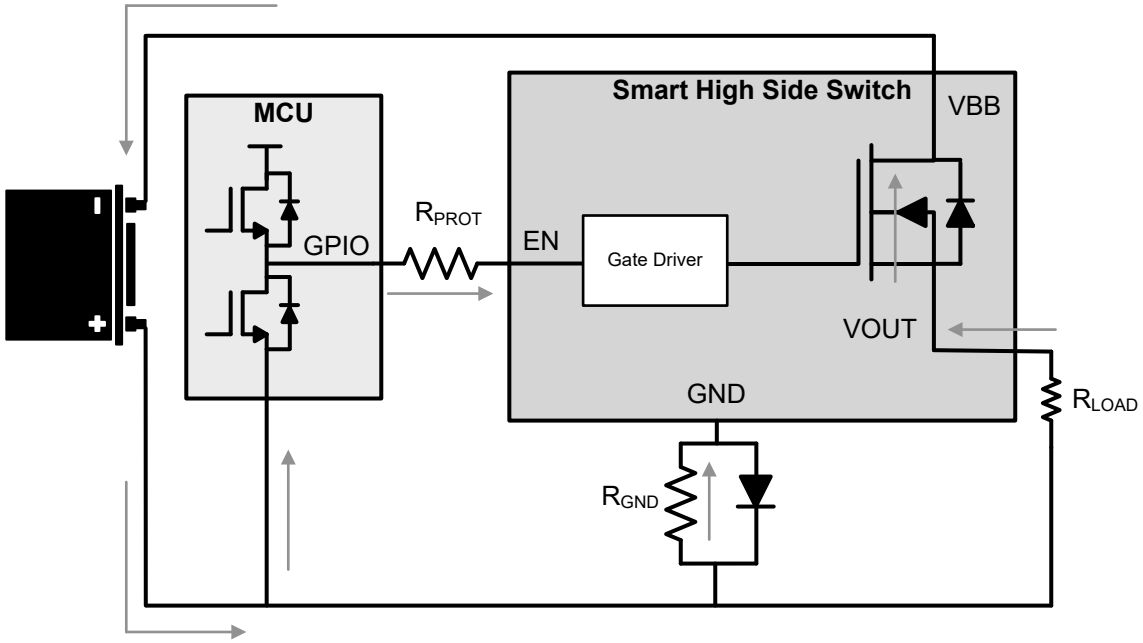


Figure 8-14. Reverse Battery Circuit

For more external protection circuitry information, see *Reverse Current Protection*. See the fault truth table for more details.

8.3.7 Full Protections

8.3.7.1 UVLO Protection

The device monitors the supply voltage V_{VBB}, to prevent unpredicted behaviors when V_{VBB} is too low. When V_{VBB} falls down to V_{UVLOF}, the device shuts down. When V_{VBB} rises up to V_{UVLOR}, the device turns on.

ADVANCE INFORMATION

8.3.7.2 Loss of GND Protection

When loss of GND occurs, output is turned off regardless of whether the input signal is high or low.

Case 1 (loss of device GND): loss of GND protection is active when the thermal pad (Tab), I_{C_GND}, and current limit ground are one trace connected to the system ground, as shown in Figure 8-15.

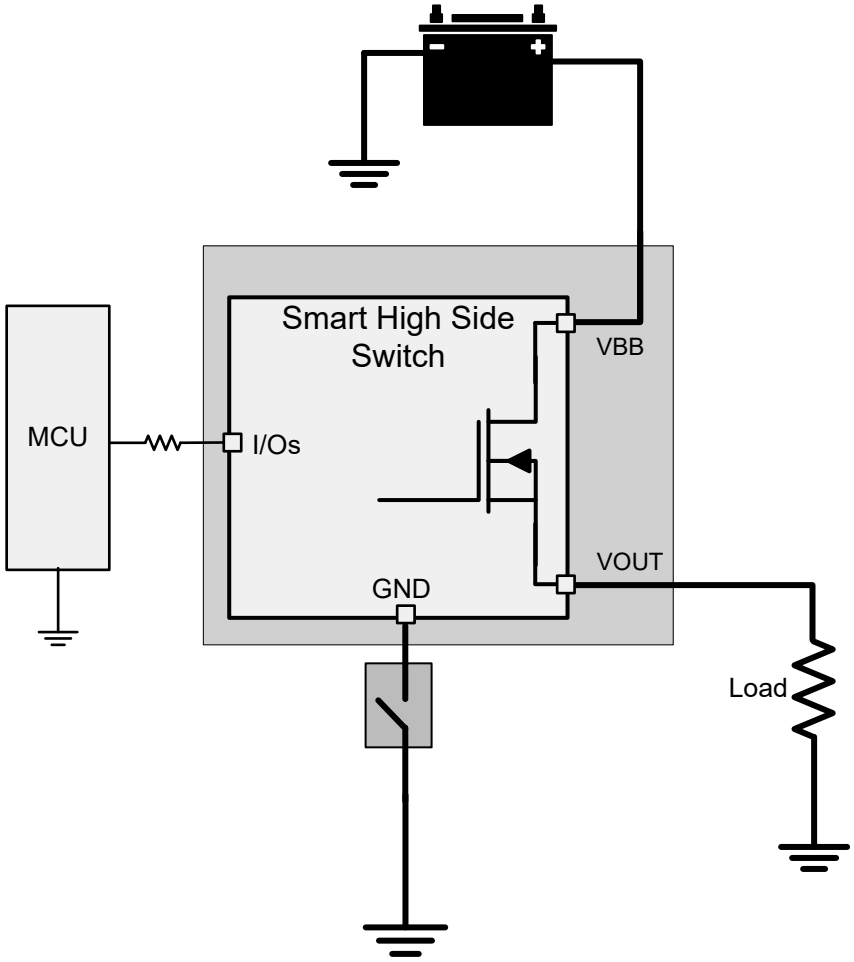


Figure 8-15. Loss of Device GND

Case 2 (loss of module GND): when the whole ECU module GND is lost, protections are also active. At this condition, the load GND remains connected.

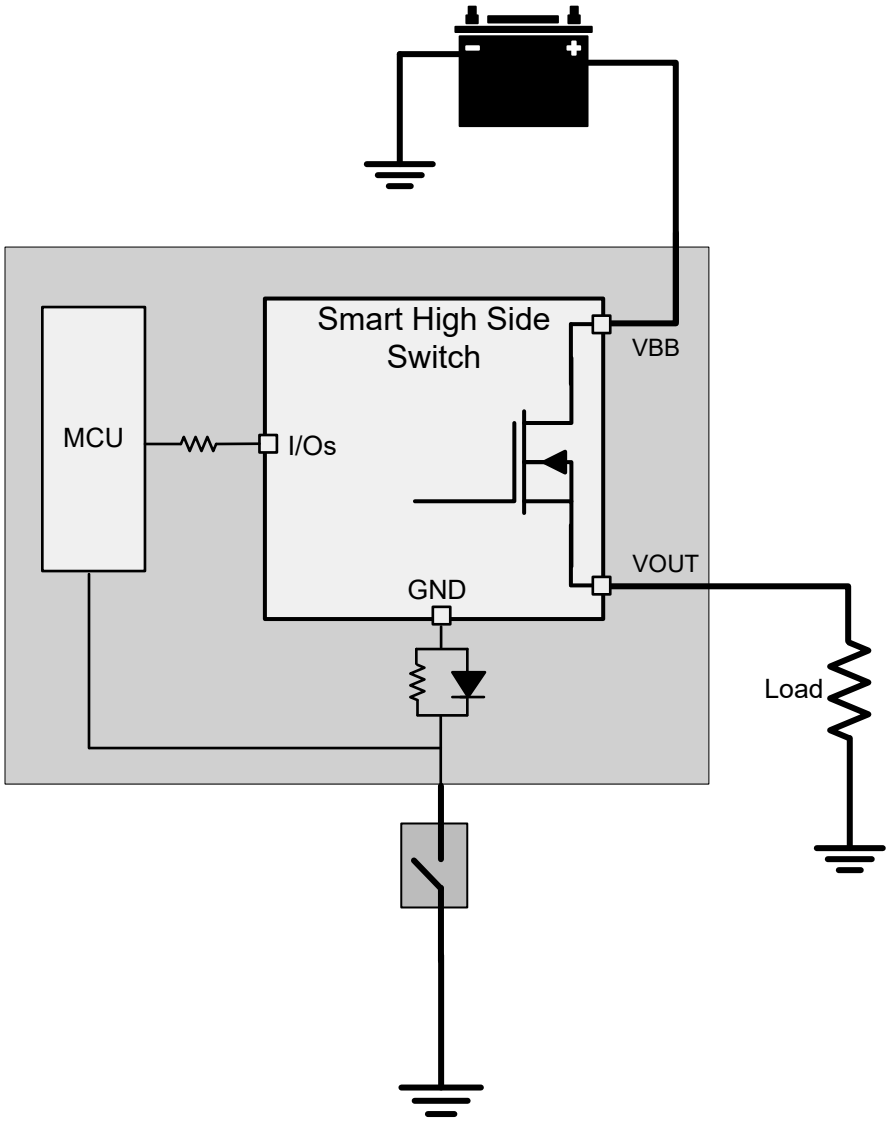


Figure 8-16. Loss of Module GND

8.3.7.3 Loss of Power Supply Protection

When loss of supply occurs, output is turned off regardless of whether the input is high or low. For a resistive or capacitive load, loss of supply protection is easy to achieve due to no more power. The worst case is a charged inductive load. In this case, the current is driven from all of the IOs to maintain the inductance output loop. TI recommends either the MCU serial resistor plus the GND network (diode and resistor in parallel) or external free-wheeling circuitry.

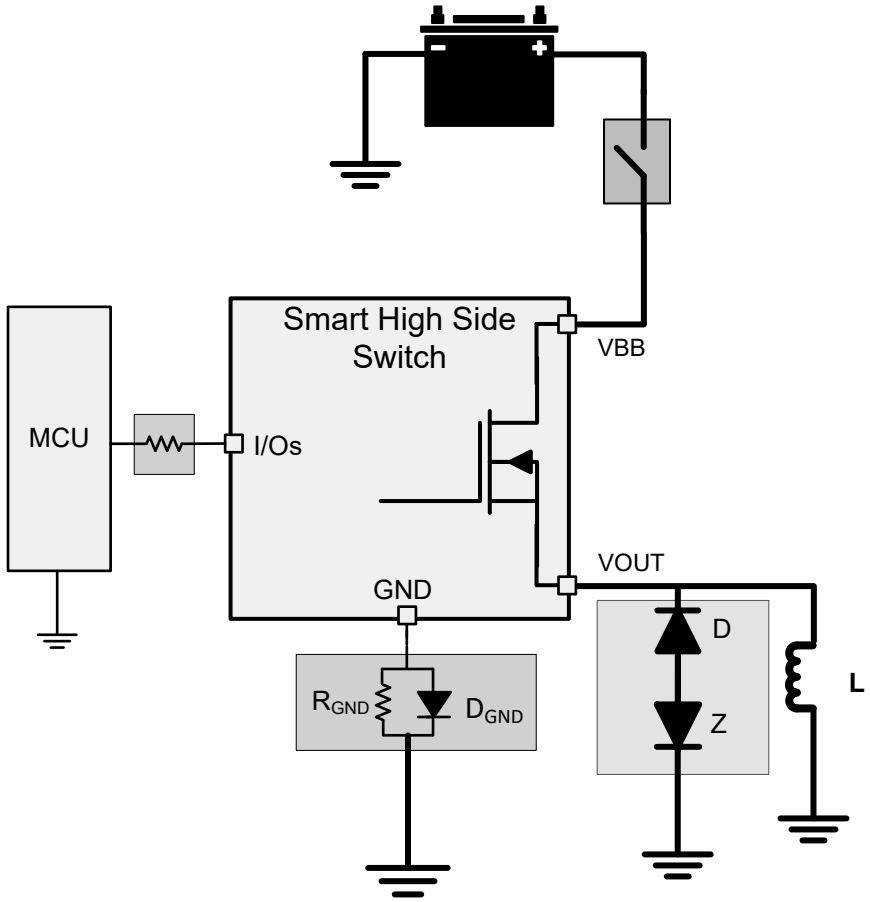


Figure 8-17. Loss of Battery

8.3.7.4 Reverse Current Protection

Method 1: block diode connected with V_{BB}. Both the device and load are protected when in reverse polarity. The blocking diode does not allow any of the current to flow during reverse battery condition.

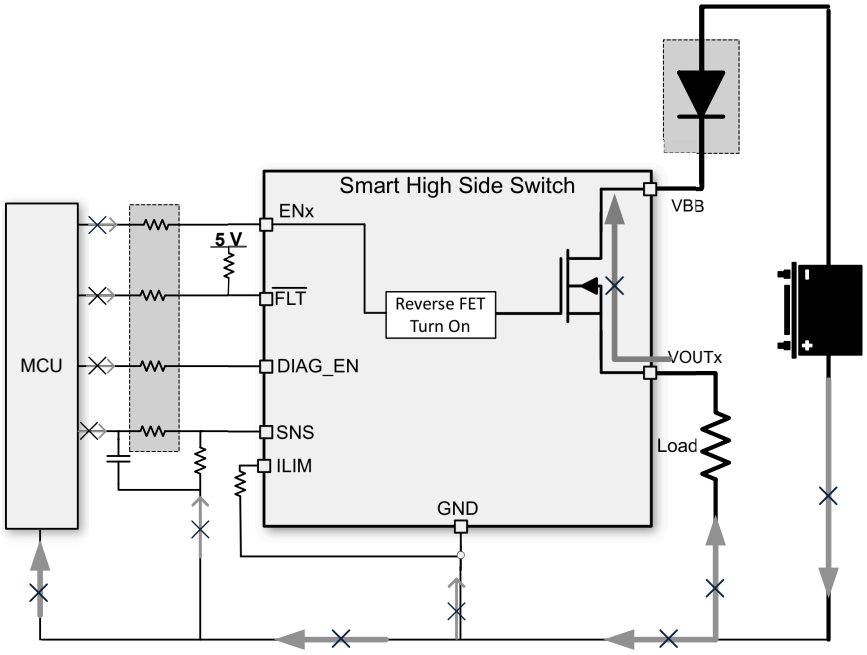


Figure 8-18. Reverse Protection With Block Diode

Method 2 (GND network protection): only the high-side device is protected under this connection. The load reverse current is limited by the impedance of the load. When reverse polarity happens, the continuous reverse current through the power FET must not make the heat build up be greater than the absolute maximum junction temperature. This can be calculated using the $R_{ON(REV)}$ value and the $R_{\theta JA}$ specification. In the reverse battery condition, the FET must come on to lower the power dissipation. This action is achieved through the path from EN to system ground where the positive voltage is being applied. No matter what types of connection are between the device GND and the board GND, if a GND voltage shift happens, verify that the following proper connections for the normal operation:

- Connect the current limit programmable resistor to the device GND.

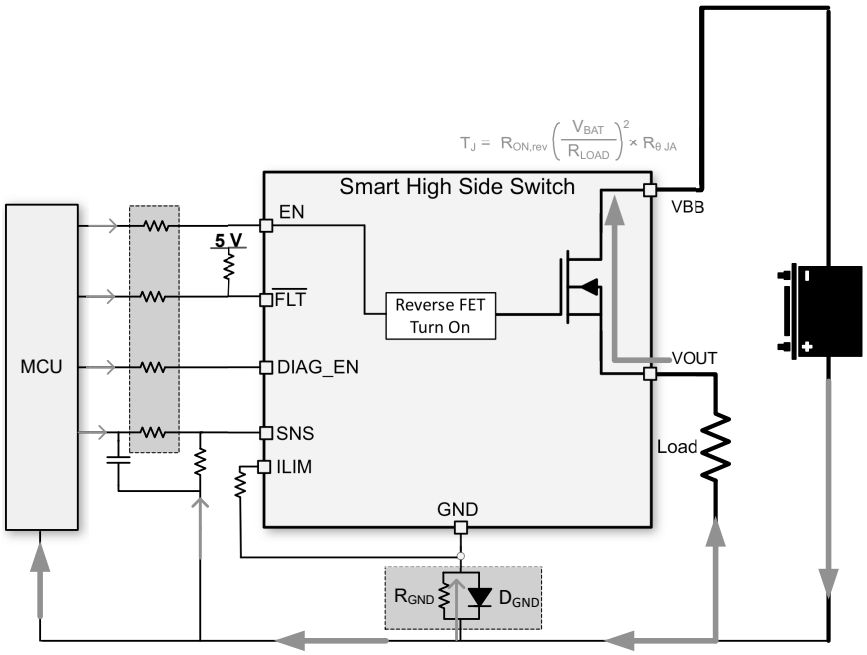


Figure 8-19. Reverse Protection With GND Network

- **Recommendation – resistor and diode in parallel:** a peak negative spike can occur when the inductive load is switching off, which can damage the HSD or the diode. So, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selection are a 1kΩ resistor in parallel with an I_F > 100mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices.

  If multiple high-side power switches are used, the resistor can be shared among devices.
- **Ground Resistor:** The higher resistor value contributes to a better current limit effect when the reverse battery or negative ISO pulses.

$$R_{GND} \geq \frac{(-V_{CC})}{(-I_{GND})} \quad (6)$$

  where

  – $-V_{CC}$ is the maximum reverse battery voltage (typically –16V).
  – $-I_{GND}$ is the maximum reverse current the ground pin can withstand, which is available in the *Absolute Maximum Ratings*.
- **Ground Diode:** A diode is needed to block the reverse voltage, which also brings a ground shift (≅600mV). Additionally, the diode must be ≅200V reverse voltage for the ISO 7637 pulse 1 testing so that the diode does not get biased.

ADVANCE INFORMATION

8.3.7.5 Protection for MCU I/Os

In many conditions, such as the negative ISO pulse, or the loss of battery with an inductive load, a negative potential on the device GND pin can damage the MCU I/O pins (more likely, the internal circuitry connected to the pins). Therefore, the serial resistors between MCU and HSS are required.

Also, for proper protection against loss of GND, TI recommends 10-kΩ resistance for the R_{PROT} resistors.

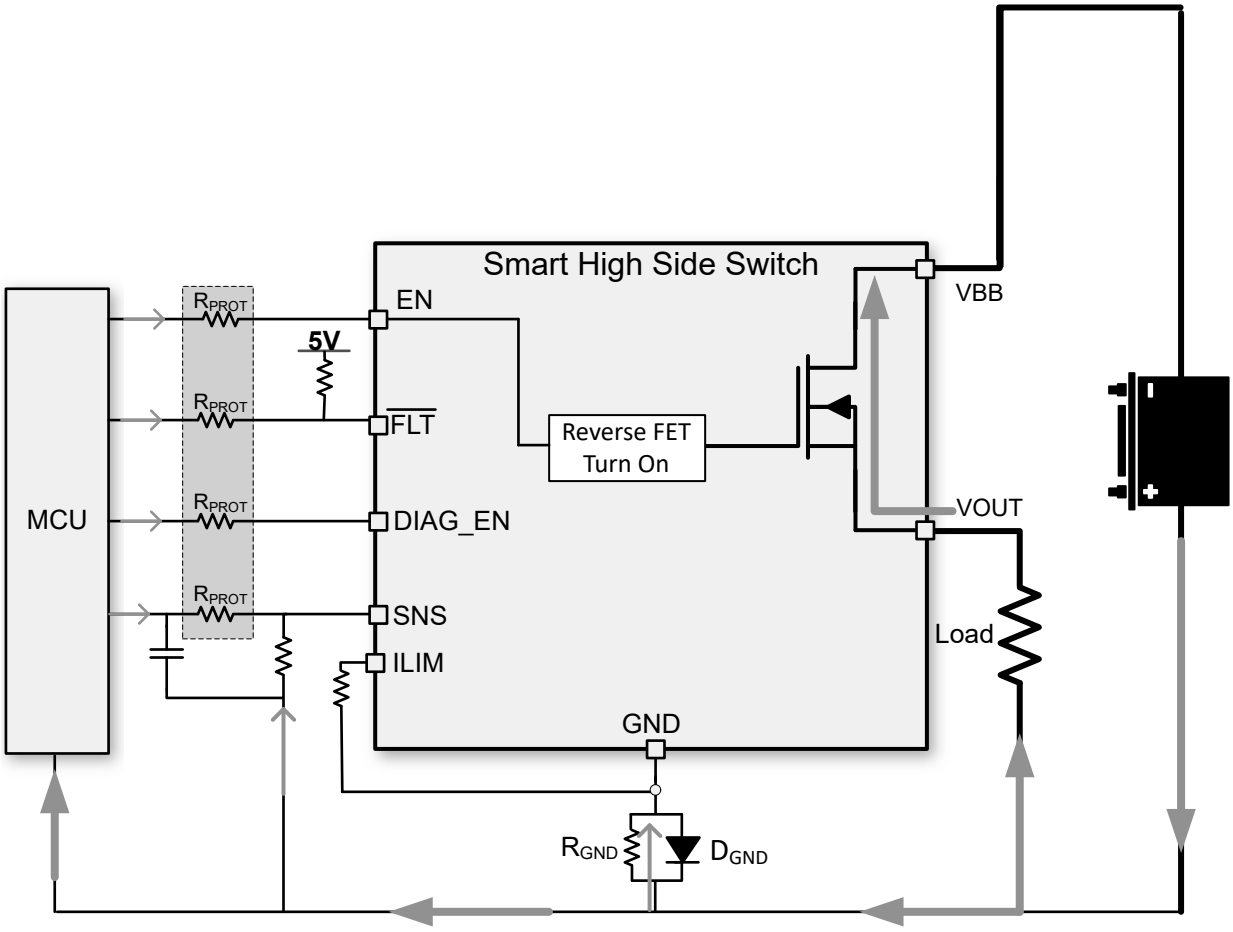


Figure 8-20. MCU I/O Protections

8.4 Device Functional Modes

The device has several states to transition into based on the ENx pin, DIAG_EN pin, and V_{BB} voltage. The different states are referenced throughout the data sheet.

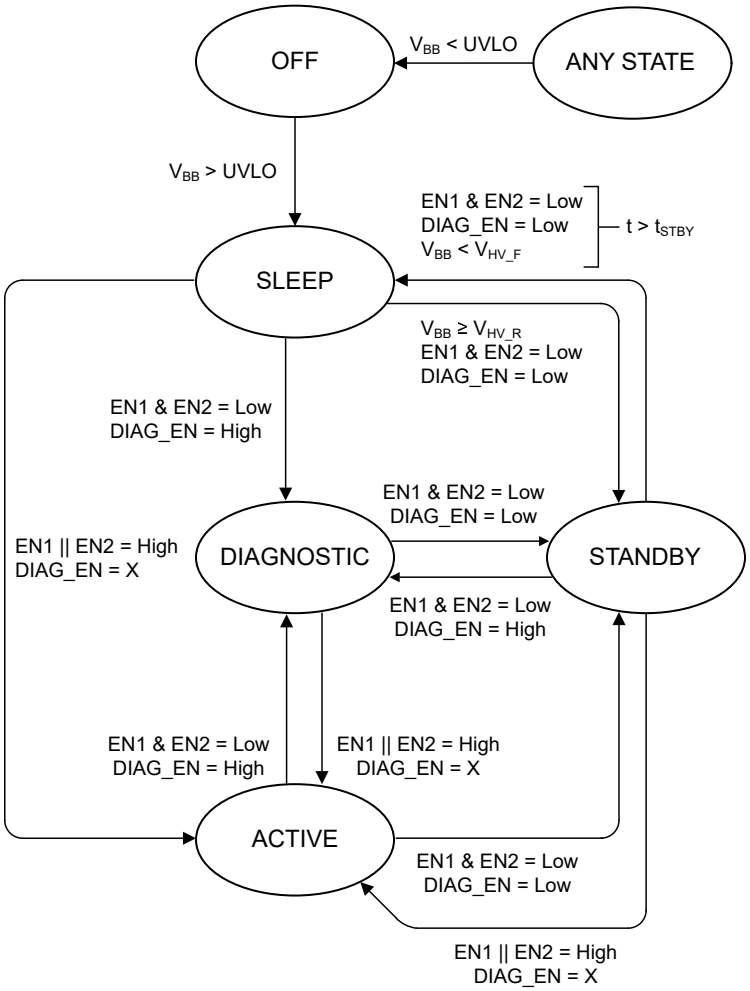


Figure 8-21. State Diagram

OFF

Off state occurs when the V_{BB} voltage of the device is below the V_{ULVO}.

SLEEP

In the SLEEP state, everything inside the device is turned off and the current into the V_{BB} is I_{SLEEP}. From SLEEP, the device can transfer into the ACTIVE state if any of the ENx pins are pulled high, the DIAGNOSTIC state if the DIAG_EN pin, without any of the ENx pins, goes high, or the STANDBY state if V_{BB} is greater than V_{HV_R}.

DIAGNOSTIC

Diagnostic state is entered when both ENx pins are low and the DIAG_EN pin is high. Open-load or short-to-battery can be diagnosed in this state. Both channels open load switches is enabled in this state. The device signals a $\overline{FLT}$ if any of the channels experience either an open-load or short-to-battery. The SNS pin output I_{SNSFH} or clamp the voltage to V_{SNSFH} if the channel that has a fault is selected through the SEL pin.

STANDBY

The STANDBY state is entered when the ENx pins are all low. Outputs are all turned off and the DIAG_EN pin is also low but there has not yet been t_{STBY} amount of time. This state is included so that the channel outputs can be modulated using PWM without any of the internal rails being cut off and put to SLEEP state. Once the device has waited t_{STBY} and V_{BB} is less than V_{HV_F}, the device completely shuts down and transitions into SLEEP state.

However, if the time is less than t_{STBY} and if either ENx pins were to go high, the device transitions into ACTIVE state. Similarly if the DIAG_EN goes high, the device transitions into DIAGNOSTIC state.

ACTIVE

The ACTIVE state is when any of the channel outputs are on by the associated ENx pin. In the ACTIVE state, the current limit value is set by the external resistor on the ILIM pin. If the DIAG_EN pin is pulled high while in the ACTIVE state, the SNS pin outputs a proportional current to the load current of the channel associated to the SEL pin configuration until a fault occurs on that channel. Additionally the $\overline{FLT}$ pin reports if there is a fault occurring on any channel. The device can transition out of the ACTIVE state by turning off all of the channels while DIAG_EN is high or low. If all of the channels turn off and DIAG_EN is high, the device transitions into the DIAGNOSTIC state. If all of the channels turn off and the DIAG_EN pin is low, then the device transitions into the STANDBY state.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS2HC08-Q1 device is capable of driving a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

9.1.1 Application Limitations

This section highlights limitations in the application that are identified from bench evaluation of the existing TPS2HC08-Q1 silicon on the evaluation module (EVM).

9.1.1.1 Short-circuit Protection

Testing has shown that during output short circuit at supply voltage level > 22V, the device damages. A design fix will be included in the final version of the IC to remove this limitation. This section will be removed in the production version of the datasheet.

9.2 Typical Application

The following figure shows an example of the external circuitry connections for TPS2HC08-Q1.

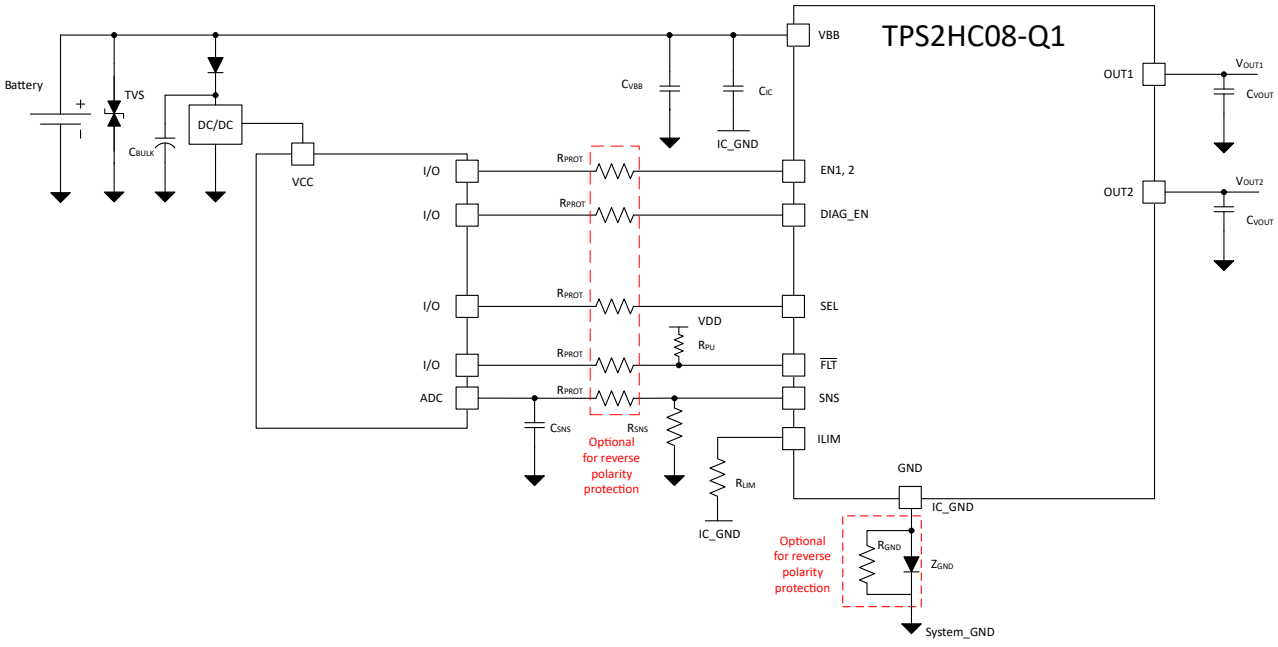


Figure 9-1. Typical Application Diagram

ADVANCE INFORMATION

9.2.1 Design Requirements

Table 9-1. Recommended Component Values

COMPONENT	DESCRIPTION	PURPOSE
TVS	SMBJ39CA	Filter voltage transients coming from battery (ISO7637-2)
C_{VBB}	220nF	Better EMI performance
C_{IC}	100nF	Minimal amount of capacitance on input for EMI mitigation
C_{BULK}	10µF	Help filter voltage transients on the supply rail
R_{PROT}	10kΩ	Protection resistor for microcontroller and device I/O pins
R_{LIM}	Values listed in Electrical Characteristics	Set current limit threshold
R_{SNS}	1kΩ	Translate the sense current into sense voltage
C_{FILTER}	100nF	Coupled with RPROT on the SNS line creates a low pass filter to filter out noise going into the ADC of the MCU
C_{VOUT}	22nF	Improves EMI performance, filtering of voltage transients
R_{PULLUP}	5kΩ	Pull up resistor for open-drain pins ($\overline{FLT}$ and LPM)
R_{GND}	1kΩ	Stabilize GND potential during turn-off of inductive load
D_{GND}	BAS21 Diode	Keeps GND close to system ground during normal operation

9.2.2 Detailed Design Procedure

To keep the maximum voltage on the SNS pin at an acceptable range for the system, calculate the R_{SNS} resistor using Equation 7. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$V_{ADC,\,min} \times K_{SNS} / I_{LOAD,\,min} \leq R_{SNS} \leq (V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,\,max} \quad (7)$$

Table 9-2. Typical Application

Parameter	Value
V_{DIAG_EN}	5V
$I_{LOAD,max}$	7.5A
$I_{LOAD,min}$	100mA
$V_{ADC,min}$	5mV
V_{HR}	1V
K_{SNS}	3000
K_{CL}	500

For this application, a R_{SNS} value of 1000Ω can be chosen to satisfy the equation requirements.

In other applications, where there is a higher dynamic current range either more emphasis can be put on the lower end measurable values which increases RSNS. Likewise, if the higher currents are of more interest the RSNS can be decreased.

To set the adjustable current limit value I_{CL}, use Equation 8 to select the R_{LIM} value.

$$R_{LIM} = K_{CL} / I_{CL} \quad (8)$$

TI recommends R_{PROT} = 10 kΩ for 5V MCU IO connections.

9.3 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12V automotive system. The supply voltage must be within the range specified in the *Recommended Operating Conditions*.

ADVANCE INFORMATION

Table 9-3. Voltage Operating Ranges

VBB VOLTAGE RANGE	NOTE
3V to 6V	Extended lower 12V automotive battery operation such as cold crank and start-stop. The device is fully functional and protected but some parametrics such as R_{ON}, current sense accuracy, current limit accuracy and timing parameters can deviate from specifications. Check the individual specifications in the *Electrical Characteristics* to confirm the voltage range.
6V to 18V	Nominal 12V automotive battery voltage range. All parametric specifications apply and the device is fully functional and protected.
18V to 28V	Extended upper 12V automotive battery operation such as double battery. The device is fully functional and protected but some parametrics such as R_{ON}, current sense accuracy, current limit accuracy, and timing parameters can deviate from specifications. Check the individual specifications in the *Electrical Characteristics* to confirm the voltage range.
35V	Load dump voltage. Device is operational and lets the pulse pass through without being damaged but does not protect against short circuits.

9.4 Layout

9.4.1 Layout Guidelines

To achieve good thermal performance, connect the VBB pad to a large copper pour. On the top PCB layer, the pour can extend beyond the package dimensions as shown in the layout examples below. In addition to this, having a VBB plane on one or more internal PCB layers and/or on the bottom layer is recommended. Vias must connect these planes to the top VBB pour. Connecting the VOUT1 and VOUT2 pads to large copper pours on the board can also help to achieve better thermal performance as the heat can transfer through the internal copper pillars to the large copper pours on the board.

TI recommends that the IO signals that connect to the microcontroller be routed to a via and then through an internal PCB layer.

If used in the design, the C_{IC} capacitor, must be placed as close as possible to the VBB and GND pins of the device. If a ground network is used for reverse battery protection, the C_{IC} capacitor must be connected from the VBB net to the IC_GND net. The C_{VBB} capacitor must be placed close to the VBB pin and connected to system ground to allow for best performance.

The R_{LIM} component must be placed close to the ILIM and GND pins of the device. If a ground network is used for reverse battery protection, the R_{LIM} must be connected from the ILIM pin to the IC_GND net for best current limit performance.

9.4.2 Layout Examples

9.4.2.1 Without a GND Network

Figure 9-2 below shows an example PCB layout without a GND network. TI recommends that the IO signals that connect to the microcontroller be routed to a via and then through an internal PCB layer.

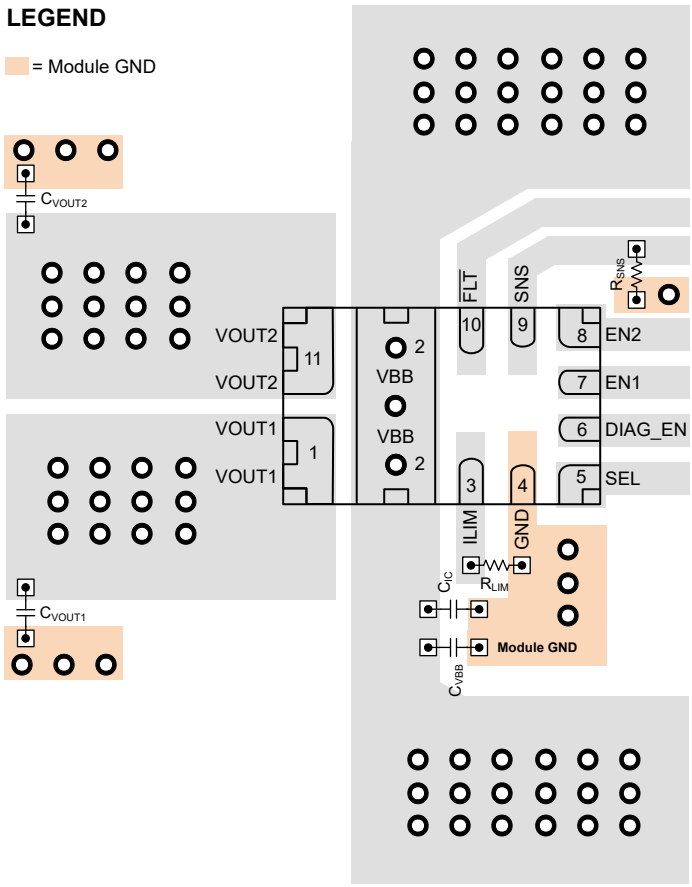


Figure 9-2. Layout Example Without a GND Network

ADVANCE INFORMATION

9.4.2.2 With a GND Network

Figure 9-3 below shows an example PCB layout with a GND network. TI recommends that the IO signals that connect to the microcontroller be routed to a via and then through an internal PCB layer.

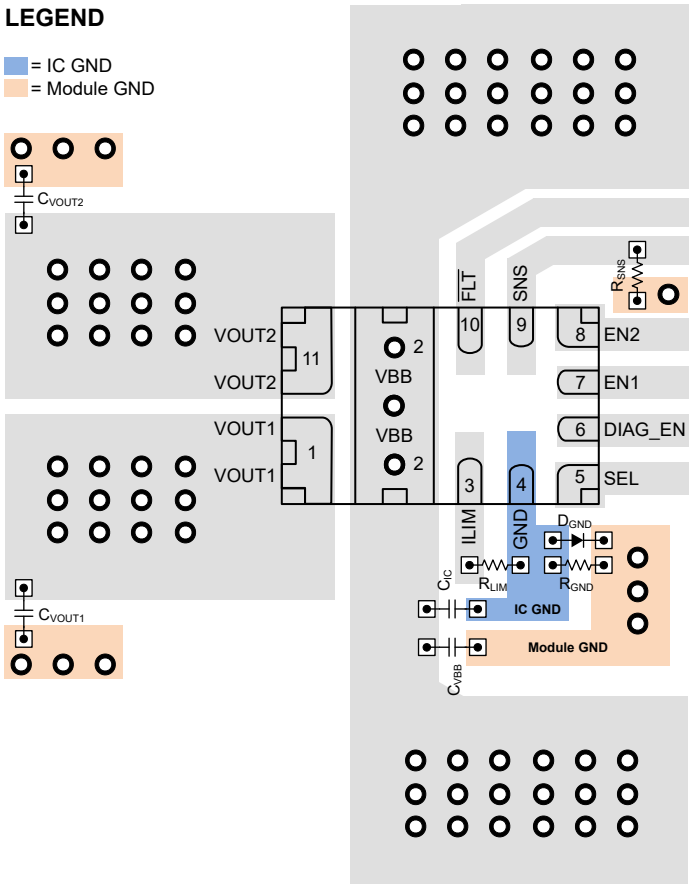


Figure 9-3. Layout Example With a GND Network

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

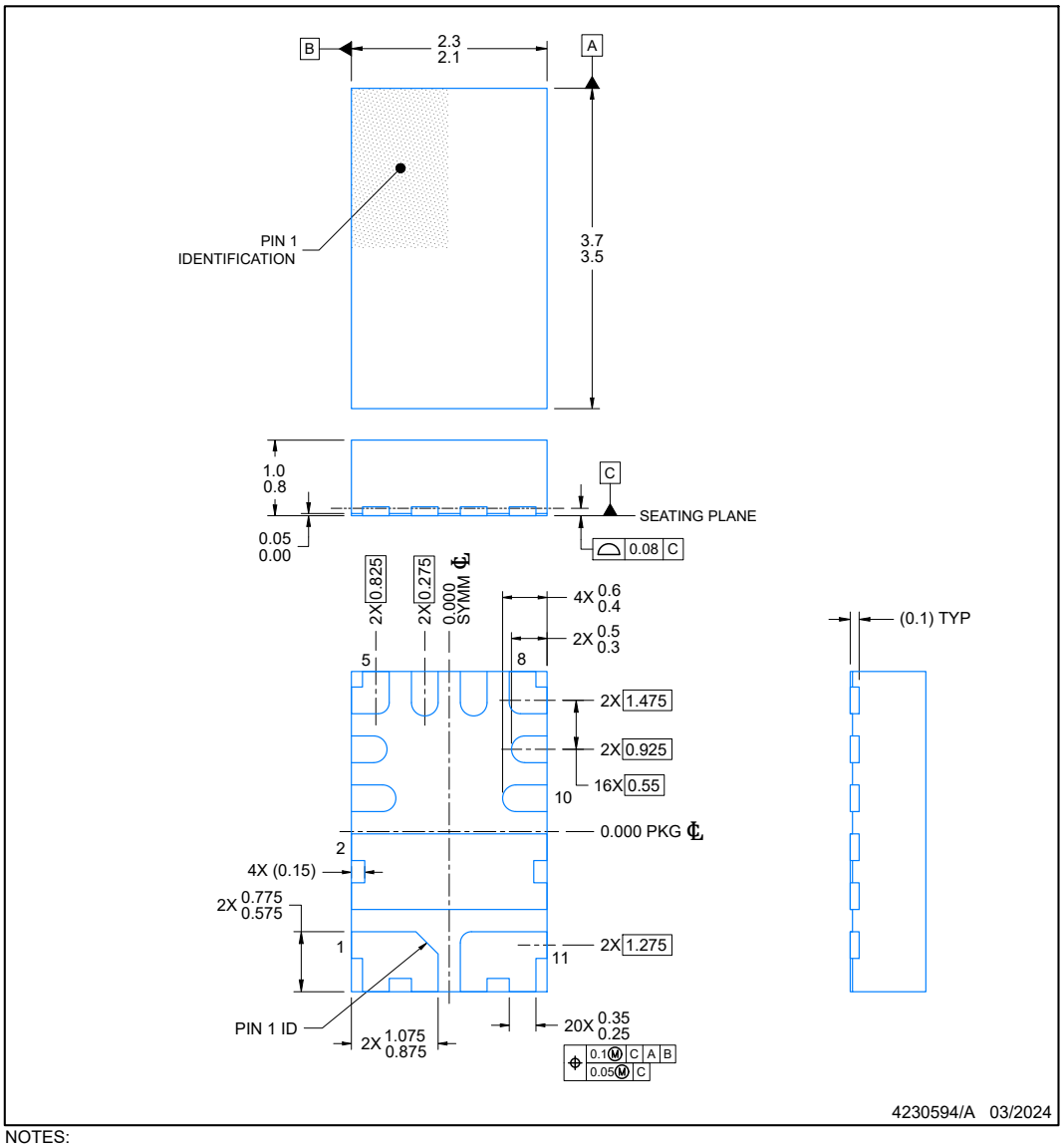
ADVANCE INFORMATION

ADVANCE INFORMATION

PACKAGE OUTLINE

VAH0011C — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



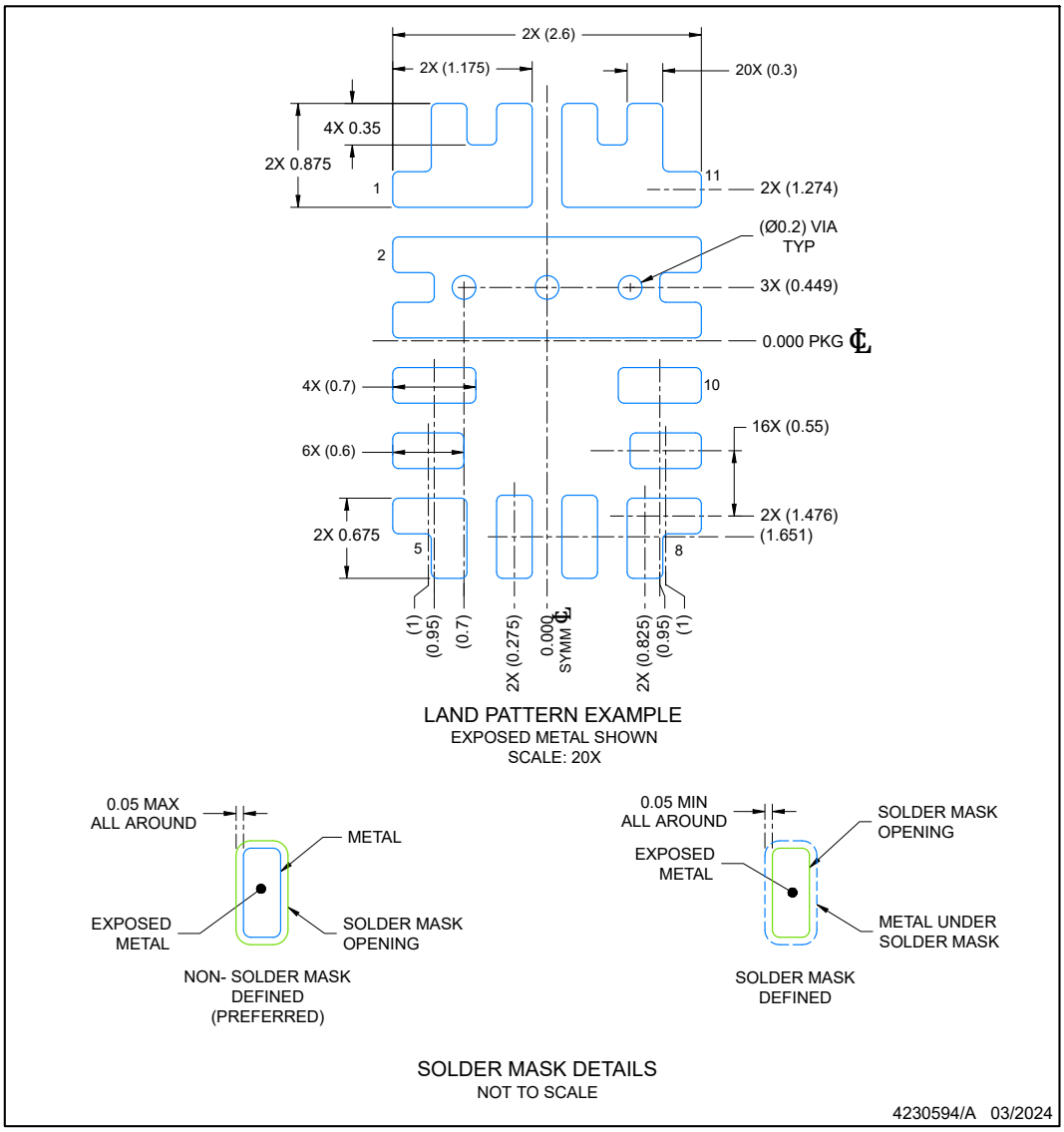
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

VAH0011C — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

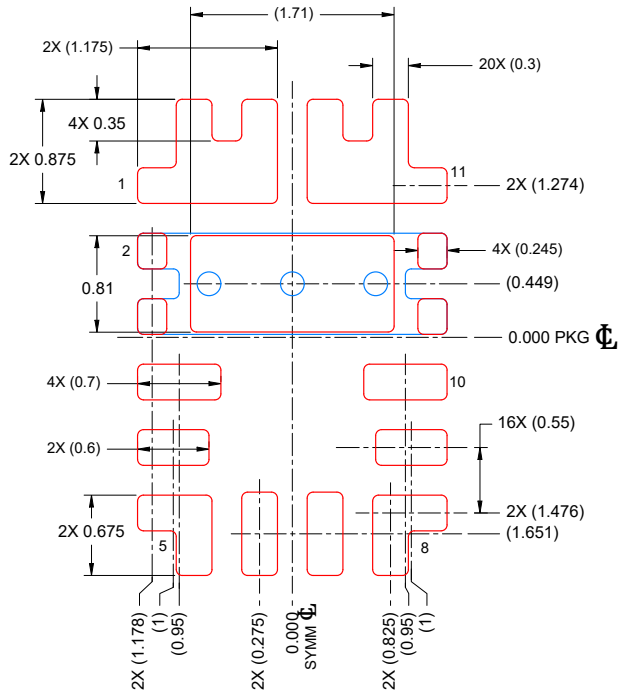
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

VAH0011C — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

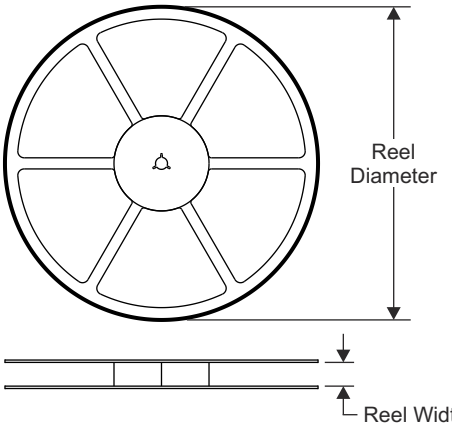
4230594/A 03/2024

NOTES: (continued)

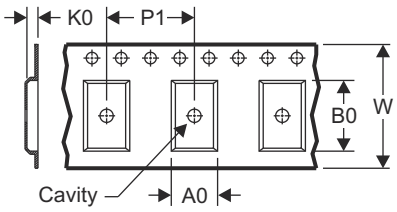
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12.1 Tape and Reel Information

REEL DIMENSIONS

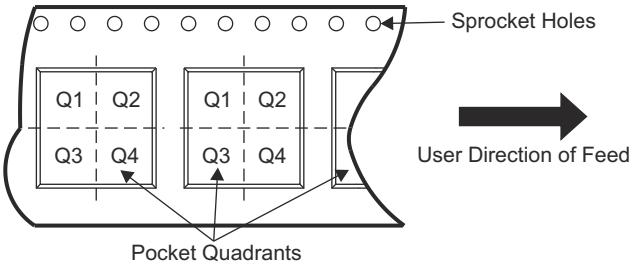


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

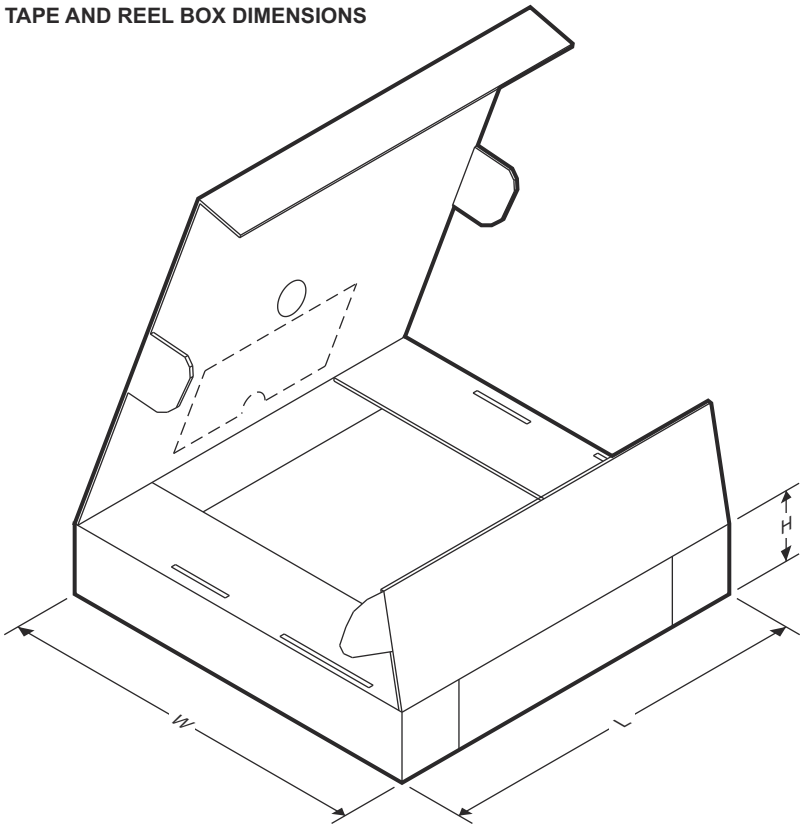


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2HC08PQVAHRQ1	VQFN-HR	VAH	11	3000	180	12.4	2.5	3.9	1.2	4	12	Q2

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2HC08PQVAHRQ1	VQFN-HR	VAH	11	3000	210	185	35

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS2HC08PQVAHRQ1	Active	Preproduction	VQFN-HR (VAH) | 11	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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