IEEE 802.3 PoE INTERFACE AND ISOLATED CONVERTER CONTROLLER

Check for Samples: TPS23753

FEATURES

- **Optimized for Isolated Converters**
- **Complete PoE Interface**
- **Adapter ORing Support**
- **12 V Adapter Support**
- **Programmable Frequency with Synch.**
- **Robust 100 V, 0.7 Ω Hotswap MOSFET**
- **Small TSSOP 14 Package**
- **15 kV / 8 kV System Level ESD Capable**
- **–40°C to 125°C Junction Temperature Range**
- **Design Procedure Application Note - SLVA305**
- **Adapter ORing Application Note - SLVA306**

APPLICATIONS

- **IEEE 802.3at Compliant Powered Devices**
- **VoIP Telephones**
- **Access Points**
- **Security Cameras**

DESCRIPTION

The TPS23753 is a combined Power over Ethernet (PoE) powered device (PD) interface and current-mode dc/dc controller optimized specifically for isolated converter designs. The PoE implementation supports the IEEE 802.3at standard as a 13 W, type 1 PD. The requirements for an IEEE 802.3at type 1 device are a superset of IEEE 802.3-2008 (originally 802.3af) requirements.

The TPS23753 supports a number of input-voltage ORing options including highest voltage, external adapter preference, and PoE preference.

The PoE interface features an external detection signature pin that can also be used to disable the internal hotswap MOSFET. This allows the PoE function to be turned off. Classification can be programmed to any of the defined types with a single resistor.

The dc/dc controller features a bootstrap startup mechanism with an internal, switched current source. This provides the advantages of cycling overload fault protection without the constant power loss of a pull up resistor.

The programmable oscillator may be synchronized to a higher-frequency external timing reference.

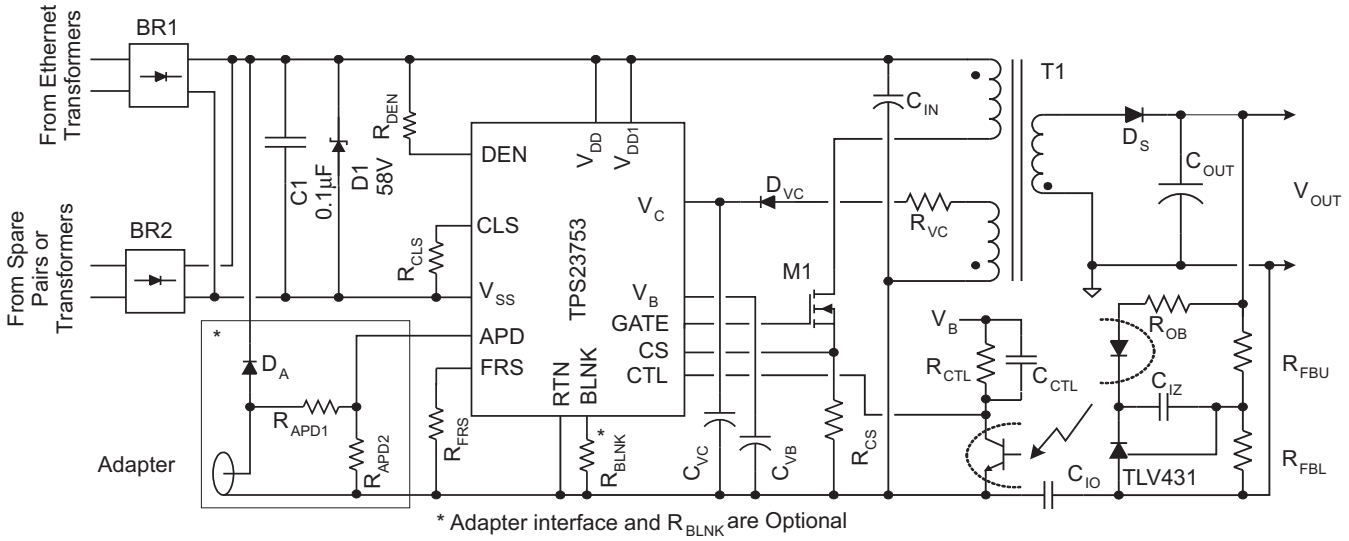


Figure 1. Basic TPS23753 Implementation

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT INFORMATION(1)

DEVICE	DUTY CYCLE	PoE UVLO ON / HYST.	PACKAGE	MARKING
TPS23753	0 – 80%	35/4.5	PW (TSSOP-14)	TP23753

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Voltages are with respect to V_{SS} (unless otherwise noted)

			VALUE	UNIT
V_I	Input voltage range	V_{DD}, V_{DD1}, DEN, RTN(2)	–0.3 to 100	V
		V_{DD1} to RTN	–0.3 to 100	V
		CLS(3)	–0.3 to 6.5	V
		[APD, BLNK(3), CTL, FRS(3), V_B (3)] to RTN	–0.3 to 6.5	V
		CS to RTN	–0.3 to V_B	V
		V_C to RTN	–0.3 to 19	V
		GATE to RTN	–0.3 to V_C + 0.3	V
	Sourcing current	V_B	Internally limited	mA
	Average sourcing or sinking current	GATE	25	mA_{RMS}
	ESD rating	HBM	2	kV
		CDM	500	V
	ESD – system level (contact/air)(4)		8/15	kV
T_J	Operating junction temperature range		–40 to Internally Limited	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) I_{RTN} = 0 for V_{RTN} > 80V.
(3) Do not apply voltage to these pins.
(4) Surges per EN61000-4-2, 1999 applied between RJ-45 and output ground and between adapter input and output ground of the TPS23753EVM-001 (HPA304-001) evaluation module (documentation available on the web). These were the test levels, not the failure threshold.

DISSIPATION RATINGS

PACKAGE	Ψ_{JT} (°C/W) (1)	θ_{JA} (°C/W)(2)	θ_{JA} (°C/W)(1)
PW (TSSOP-14)	0.97	173.6	99.3

(1) JEDEC method with high-k board (4 layers, 2 signal and 2 planes). $T_J = T_{TOP} + (\Psi_{JT} \times P_J)$. Use Ψ_{JT} to validate T_J from measurements.
(2) JEDEC method with low-k board (2 signal layers).

RECOMMENDED OPERATING CONDITIONS

Voltage with respect to V_{SS} (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage range, V_{DD}, V_{DD1}, RTN	0		57	V
	Input voltage range, V_{DD}, V_{DD1} to RTN	0		57	V
	Input voltage range, V_C to RTN	0		18	V
	Input voltage range, APD, CTL to RTN	0		V_B	V
	Input voltage range, CS to RTN	0		2	V
	RTN current ($T_J \le 125°C$)			350	mA
	V_B sourcing current	0	2.5	5	mA
	V_B capacitance	0.08	0.1	2.2	µF
R_{BLNK}		0		350	kΩ
	Synchronization pulse width input (when used)	25		150	ns
T_J	Operating junction temperature range	–40		125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: CS = APD = CTL = RTN, GATE open, R_{FRS} = 60.4 kΩ, R_{BLNK} = 249 kΩ, $C_{VB} = C_{VC}$ = 0.1 µF, R_{DEN} = 24.9 kΩ, R_{CLS} open, $V_{VDD-VSS}$ = 48 V, $V_{VDD1-RTN}$ = 48 V, 8.5 V ≤ V_{VC-RTN} ≤ 18 V, –40°C ≤ T_J ≤ 125°C

Controller Section Only

[V_{SS} = RTN and $V_{DD} = V_{DD1}$] or [V_{SS} = RTN = V_{DD}], all voltages referred to RTN. Typical specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C						
$UVLO_1$	Undervoltage lockout	V_C rising	8.65	9	9.3	V
$UVLO_H$		Hysteresis(1)	3.3	3.5	3.7	
	Operating current	V_C = 12 V, CTL = V_B	0.40	0.58	0.85	mA
t_{ST}	Startup time, C_{VC} = 22 µF	V_{DD1} = 10.2 V, $V_C(0)$ = 0 V	50	85	175	ms
		V_{DD1} = 35 V, $V_C(0)$ = 0 V	30	48	85	
	Startup current source - I_{VC}	V_{DD1} = 10.2 V, V_{VC} = 8.6 V	0.44	1.06	1.80	mA
		V_{DD1} = 48 V, V_{VC} = 0 V	2.5	4.3	6.0	
V_B						
	Voltage	6.5 V ≤ V_C ≤ 18 V, 0 ≤ I_{VB} ≤ 5 mA	4.75	5.10	5.25	V
FRS						
	Switching frequency	CTL= V_B, Measure GATE	223	248	273	kHz
		R_{FRS} = 60.4 kΩ				
D_{MAX}	Duty cycle	CTL= V_B, Measure GATE	76	78.5	81	%
V_{SYNC}	Synchronization	Input threshold	2.0	2.2	2.4	V
CTL						
V_{ZDC}	0% duty cycle threshold	V_{CTL} ↓ until GATE stops	1.3	1.5	1.7	V
	Softstart period	Interval from switching start to V_{CSMAX}	400	800		µs
	Input resistance		70	100	145	kΩ
BLNK						
	Blanking delay	In addition to t_1				ns
		BLNK = RTN	35	52	75	
		R_{BLNK} = 49.9 kΩ	41	52	63	

(1) The hysteresis tolerance tracks the rising threshold for a given device.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted: CS = APD = CTL = RTN, GATE open, R_{FRS} = 60.4 kΩ, R_{BLNK} = 249 kΩ, C_{VB} = C_{VC} = 0.1 µF, R_{DEN} = 24.9 kΩ, R_{CLS} open, $V_{VDD-VSS}$ = 48 V, $V_{VDD1-RTN}$ = 48 V, 8.5 V ≤ V_{VC-RTN} ≤ 18 V, –40°C ≤ T_J ≤ 125°C

Controller Section Only

[V_{SS} = RTN and V_{DD} = V_{DD1}] or [V_{SS} = RTN = V_{DD}], all voltages referred to RTN. Typical specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CS						
V_{CSMAX}	Maximum threshold voltage	V_{CTL} = V_B, V_{CS} ↑ until GATE duty cycle drops	0.50	0.55	0.60	V
t_1	Turn off delay	V_{CS} = 0.65 V	25	41	60	ns
V_{SLOPE}	Internal slope compensation voltage	Peak voltage at maximum duty cycle, referred to CS	90	118	142	mV
I_{SL_EX}	Peak slope compensation current	V_{CTL} = V_B, I_{CS} at maximum duty cycle (ac component)	30	42	54	µA
	Bias current (sourcing)	Gate high, dc component of CS current	2	3	4.2	µA
GATE						
	Source current	V_{CTL} = V_B, V_C = 12 V, GATE high, Pulsed measurement	0.30	0.46	0.60	A
	Sink current	V_{CTL} = V_B, V_C = 12 V, GATE low, Pulsed measurement	0.50	0.79	1.1	A
APD						
V_{APDEN}	Threshold voltage	V_{APD}↑	1.42	1.5	1.58	V
V_{APDH}		Hysteresis(2)	0.28	0.3	0.32	
THERMAL SHUTDOWN						
	Turn off temperature		135	145	155	°C
	Hysteresis(3)			20		°C

(2) The hysteresis tolerance tracks the rising threshold for a given device.
(3) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS

PoE and Control

[V_{DD} = V_{DD1}] or [V_{DD1}] = RTN, V_{VC-RTN} = 0 V, all voltages referred to V_{SS}. Typical specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEN (DETECTION)		**(V_{DD} = V_{DD1} = RTN = V_{SUPPLY} positive)**				
	Detection current	Measure I_{SUPPLY}				µA
		V_{DD} = 1.6 V	62	64.3	66.5	
		V_{DD} = 10 V	399	406	413	
	Detection bias current	V_{DD} = 10 V, DEN open, Measure I_{SUPPLY}		5.2	12	µA
V_{PD_DIS}	Hotswap disable threshold		3	4	5	V
I_{lkg}	DEN leakage current	V_{DEN} = V_{DD} = 57 V, Float V_{DD1} and RTN, Measure I_{DEN}		0.1	5	µA
CLS (CLASSIFICATION)		**(V_{DD} = V_{DD1} = RTN = V_{SUPPLY} positive)**				
I_{CLS}	Classification current	13 V ≤ V_{DD} ≤ 21 V, Measure I_{SUPPLY}				mA
		R_{CLS} = 1270 Ω	1.8	2.14	2.4	
		R_{CLS} = 243 Ω	9.9	10.6	11.3	
		R_{CLS} = 137 Ω	17.6	18.6	19.4	
		R_{CLS} = 90.9 Ω	26.5	27.9	29.3	
		R_{CLS} = 63.4 Ω	38	39.9	42	
V_{CL_ON}	Classification regulator lower threshold	Regulator turns on, V_{DD} rising	10	11.7	13	V
V_{CL_HYS}		Hysteresis(1)	1.9	2.05	2.2	
V_{CU_OFF}	Classification regulator upper threshold	Regulator turns off, V_{DD} rising	21	22	23	V
V_{CU_HYS}		Hysteresis(1)	0.5	0.77	1	
I_{lkg}	Leakage current	V_{DD} = 57 V, V_{CLS} = 0 V, DEN = V_{SS}, Measure I_{CLS}			1	µA

(1) The hysteresis tolerance tracks the rising threshold for a given device.

ELECTRICAL CHARACTERISTICS (continued)

PoE and Control

[V_{DD} = V_{DD1}] or [V_{DD1}] = RTN, V_{VC-RTN} = 0 V, all voltages referred to V_{SS}. Typical specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RTN (PASS DEVICE)		**(V_{DD1} = RTN)**				
	On resistance			0.7	1.2	Ω
	Current limit	V_{RTN} = 1.5 V, V_{DD} = 48 V, Pulsed Measurement	405	450	505	mA
	Inrush limit	V_{RTN} = 2 V, V_{DD}: 0 V → 48 V, Pulsed Measurement	100	140	180	mA
	Foldback voltage threshold	V_{DD} rising	11	12.3	13.6	V
I_{lkg}	Leakage current	V_{DD} = V_{RTN} = 100 V, DEN = V_{SS}			40	µA
UVLO						
UVLO_R	Undervoltage lockout threshold	V_{DD} rising	33.9	35	36.1	V
UVLO_H		Hysteresis (2)	4.40	4.55	4.70	
THERMAL SHUTDOWN						
	Turn off temperature		135	145	155	°C
	Hysteresis (3)			20		°C

(2) The hysteresis tolerance tracks the rising threshold for a given device.
(3) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

DEVICE INFORMATION

TOP VIEW

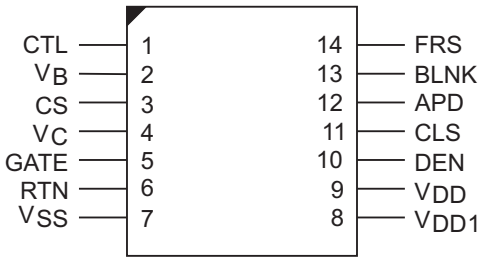


Table 1. Terminal Functions

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
1	CTL	I	The control loop input to the PWM (pulse width modulator). Use V_B as a pull up for CTL.
2	V_B	O	5 V bias rail for dc/dc control circuits. Apply a 0.1 µF to RTN. V_B may be used to bias an external optocoupler for feedback.
3	CS	I	Dc/dc converter switching MOSFET current sense input. Connect CS to the high side of the RTN-referenced current sense resistor.
4	V_C	I/O	Dc/dc converter bias voltage. The internal startup current source and converter bias winding output power this pin. Connect a 0.22 µF minimum ceramic capacitor to RTN, and a larger capacitor to facilitate startup.
5	GATE	O	Gate drive output for the dc/dc converter switching MOSFET.
6	RTN		RTN is the negative rail input to the dc/dc converter and output of the PoE hotswap.
7	V_{SS}		Negative power rail derived from the PoE source.
8	V_{DD1}		Source of dc/dc converter startup current. Connect to V_{DD} for most applications.
9	V_{DD}		Positive input power rail for PoE interface circuit. Derived from the PoE source.
10	DEN	I/O	Connect a 24.9 kΩ resistor from DEN to V_{DD} to provide the PoE detection signature. Pulling this pin to V_{SS} during powered operation causes the internal hotswap MOSFET to turn off.
11	CLS	O	Connect a resistor from CLS to V_{SS} to program the classification current per Table 2.
12	APD	I	Pull APD above 1.5 V to disable the internal PD hotswap switch, forcing power to come from an external adapter. Connect to the adapter through a resistor divider.
13	BLNK	I/O	Connect to RTN to utilize the internally set blanking period or connect through a resistor to RTN to program the blanking period.
14	FRS	I/O	Connect a resistor from FRS to RTN to program the converter switching frequency.

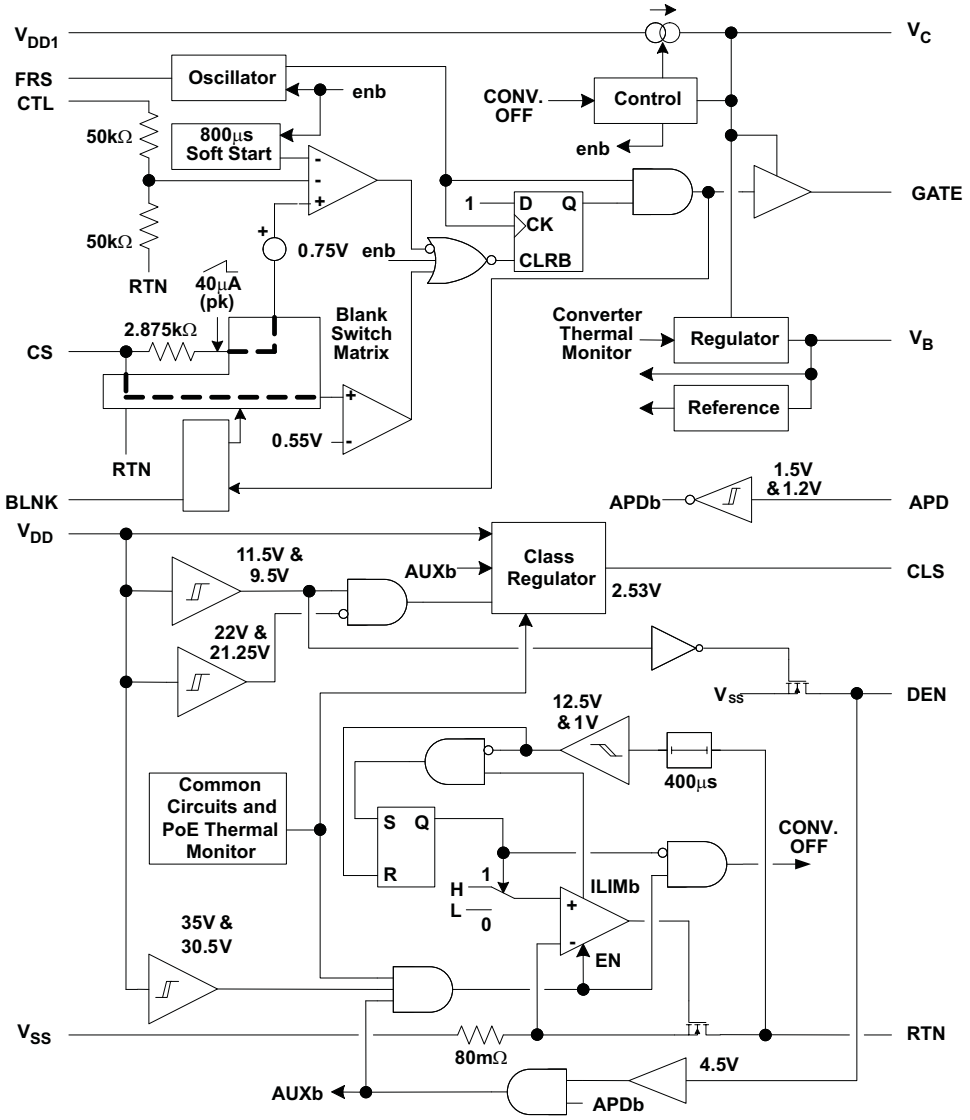


Figure 2. TPS23753 Functional Block Diagram

Pin Description

Refer to Figure 1 for component reference designators ®$_{CS}$ for example), and the Electrical Characteristics table for values denoted by reference (V_{CSMAX} for example). Electrical Characteristic values take precedence over any numerical values used in the following sections.

APD

APD forces power to come from an external adapter connected from V_{DD1} to RTN by opening the hotswap switch. A resistor divider is recommended on APD when it is connected to an external adapter. The divider provides ESD protection, leakage discharge for the adapter ORing diode, and input voltage qualification. Voltage qualification assures the adapter can support the PD before the PoE current is cut off.

Select the APD divider resistors per the following equations where $V_{ADPTR-ON}$ is the desired adapter voltage that enables the APD function as adapter voltage rises.

$$R_{APD1} = R_{APD2} \cdot \left(V_{ADPTR\_ON} - V_{APDEN}\right) / V_{APDEN} \quad (1)$$

$$V_{ADPTR\_OFF} = \frac{R_{APD1} + R_{APD2}}{R_{APD2}} \cdot \left(V_{APDEN} - V_{APDH}\right) \quad (2)$$

The CLS output is disabled when a voltage above V_{APDEN} is applied to the APD pin.

Place the APD pull-down resistor adjacent to the APD pin.

APD should be tied to RTN when not used.

BLNK

Blanking provides an interval between the gate drive going high and the current comparator on CS actively monitoring the input. This delay allows the normal turn-on current transient (spike) to subside before the comparator is active, preventing undesired short duty cycles and premature current limiting.

Connect BLNK to RTN to obtain the internally set blanking period. Connect a resistor from BLNK to RTN for a programmable blanking period. The relationship between the desired blanking period and the programming resistor is defined by the following equation.

$$R_{BLNK}\left(k\Omega\right) = t_{BLNK}\left(ns\right) \quad (3)$$

Place the resistor adjacent to the BLNK pin when it is used.

CLS

Connect a resistor from CLS to V_{SS} to program the classification current per IEEE 802.3at. The PD power ranges and corresponding resistor values are listed in Table 2. The power assigned should correspond to the maximum average power drawn by the PD during operation. The TPS23753 supports class 0 – 3 power levels.

CS

The current sense input for the dc/dc converter should be connected to the high side of the switching MOSFET's current sense resistor. The current-limit threshold, V_{CSMAX}, defines the voltage on CS above which the GATE ON time will be terminated regardless of the voltage on CTL.

The TPS23753 provides internal slope compensation to stabilize the current mode control loop. If the provided slope is not sufficient, the effective slope may be increased by addition of R_S per Figure 22.

Routing between the current-sense resistor and the CS pin should be short to minimize cross-talk from noisy traces such as the gate drive signal.

CTL

CTL is the voltage control loop input to the PWM (pulse width modulator). Pulling V_{CTL} below V_{ZDC} causes GATE to stop switching. Increasing V_{CTL} above V_{ZDC} raises the switching MOSFET programmed peak current. The maximum (peak) current is requested at approximately V_{ZDC} + (2 × V_{CSMAX}). The ac gain from CTL to the PWM comparator is 0.5.

Use V_B as a pull up source for CTL.

DEN

Connect a 24.9 kΩ resistor from DEN to V_{DD} to provide the PoE detection signature. DEN goes to a high impedance state when not in the detection voltage range. Pulling DEN to V_{SS} during powered operation causes the internal hotswap MOSFET and class regulator to turn off.

FRS

Connect a resistor from FRS to RTN to program the converter switching frequency. Select the resistor per the following relationship.

$$R_{FRS}(k\Omega) = \frac{15000}{f_{SW}(kHz)} \quad (4)$$

The converter may be synchronized to a frequency above its maximum free-running frequency by applying short ac-coupled pulses into the FRS pin. More information is provided in the Applications section.

The FRS pin is high impedance. Keep the connections short and apart from potential noise sources.

GATE

Gate drive output for the dc/dc converter switching MOSFET.

RTN

RTN is internally connected to the drain of the PoE hotswap MOSFET, and the dc/dc controller return. RTN should be treated as a local reference plane (ground plane) for the dc/dc controller and converter primary to maintain signal integrity.

V_B

V_B is an internal 5V control rail that should be bypassed by a 0.1 µF capacitor to RTN. V_B should be used to bias the feedback optocoupler.

V_C

V_C is the bias supply for the dc/dc controller. The MOSFET gate driver runs directly from V_C. V_B is regulated down from V_C, and is the bias voltage for the rest of the converter control. A startup current source from V_{DD1} to V_C is controlled by a comparator with hysteresis to implement a bootstrap startup of the converter. V_C must be connected to a bias source, such as a converter auxiliary output, during normal operation.

A minimum 0.22 µF capacitor, located adjacent to the V_C pin, should be connected from V_C to RTN to bypass the gate driver. A larger total capacitance is required for startup.

V_{DD}

Positive input power rail for PoE control that is derived from the PoE. V_{DD} should be bypassed to V_{SS} with a 0.1 µF (X7R,10%) capacitor as required by the standard. A transient suppressor (Zener) diode, should be connected from V_{DD} to V_{SS} to protect against overvoltage transients.

V_{DD1}

Source of dc/dc converter startup current. Connect to V_{DD} for most applications. V_{DD1} may be isolated by a diode from V_{DD} to support PoE priority operation.

V_{SS}

V_{SS} is the PoE input-power return side. It is the reference for the PoE interface circuits, and has a current-limited hotswap switch that connects it to RTN. V_{SS} is clamped to a diode drop above RTN by the hotswap switch. A local V_{SS} reference plane should be used to connect the input components and the V_{SS} pin.

TYPICAL CHARACTERISTICS

DETECTION BIAS CURRENT vs VOLTAGE

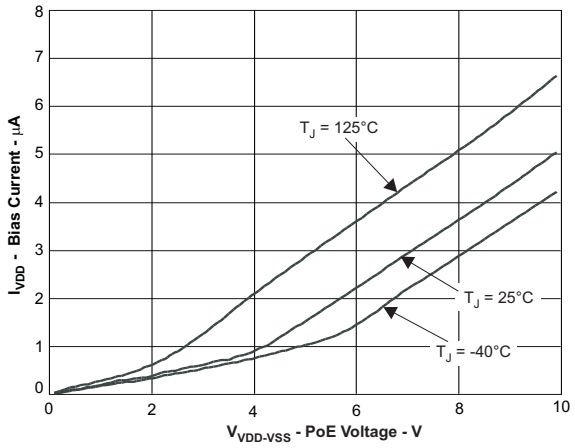


Figure 3.

PoE CURRENT LIMIT vs TEMPERATURE

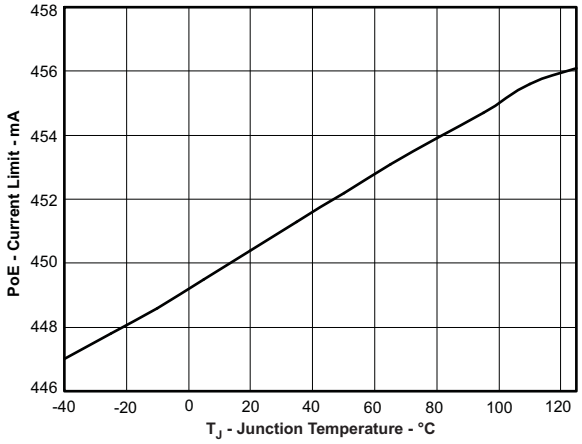


Figure 4.

CONVERTER START TIME vs TEMPERATURE

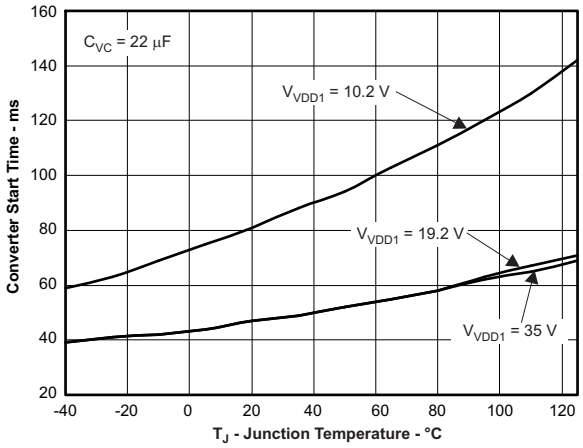


Figure 5.

CONVERTER STARTUP SOURCE CURRENT vs V_{VDD1}

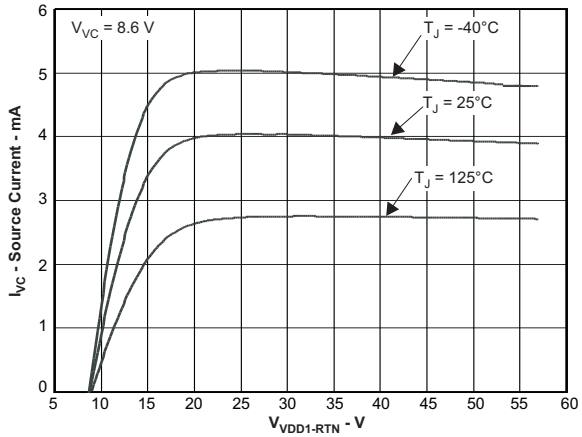


Figure 6.

TYPICAL CHARACTERISTICS (continued)

CONTROLLER BIAS CURRENT vs TEMPERATURE

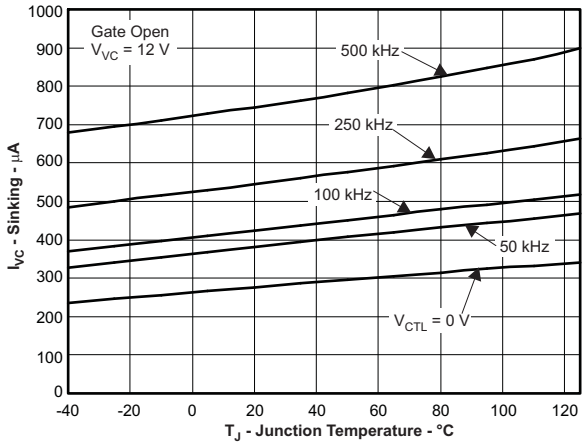


Figure 7.

CONTROLLER BIAS CURRENT vs VOLTAGE

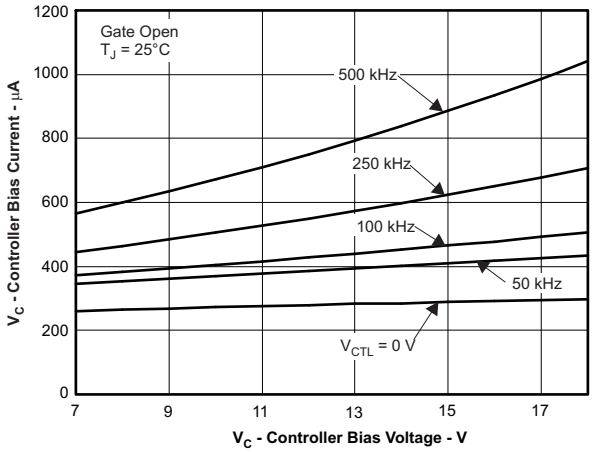


Figure 8.

SWITCHING FREQUENCY vs TEMPERATURE

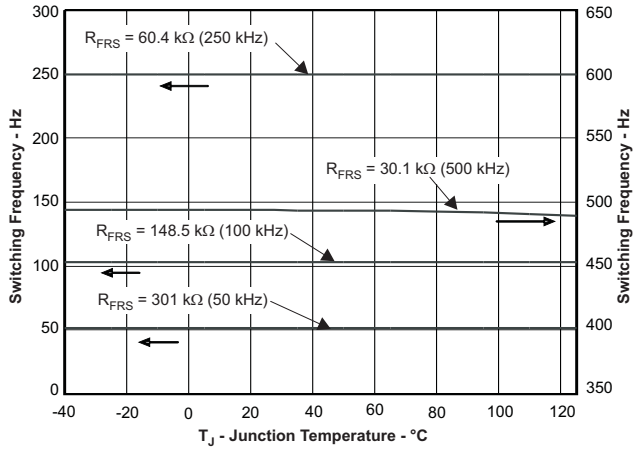


Figure 9.

SWITCHING FREQUENCY vs PROGRAMMED RESISTANCE

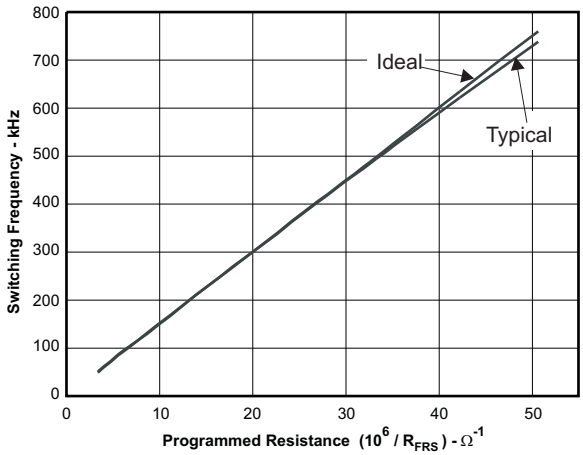


Figure 10.

TYPICAL CHARACTERISTICS (continued)

MAXIMUM DUTY CYCLE vs TEMPERATURE

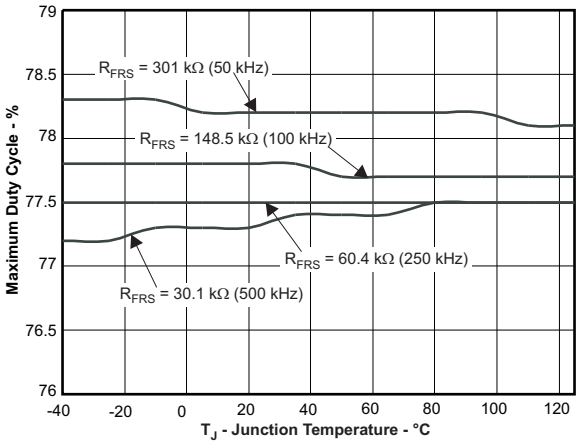


Figure 11.

CURRENT SLOPE COMPENSATION VOLTAGE vs TEMPERATURE

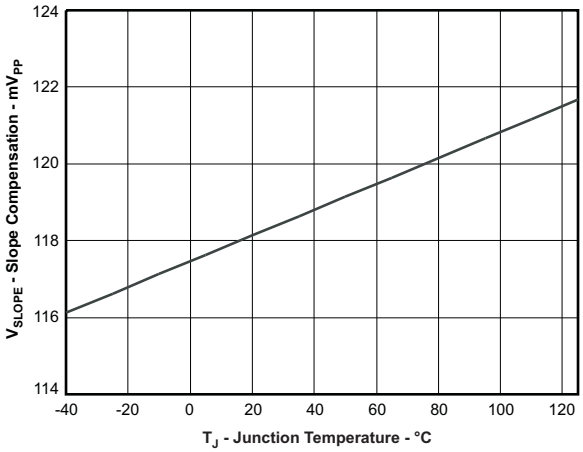


Figure 12.

CURRENT SLOPE COMPENSATION CURRENT vs TEMPERATURE

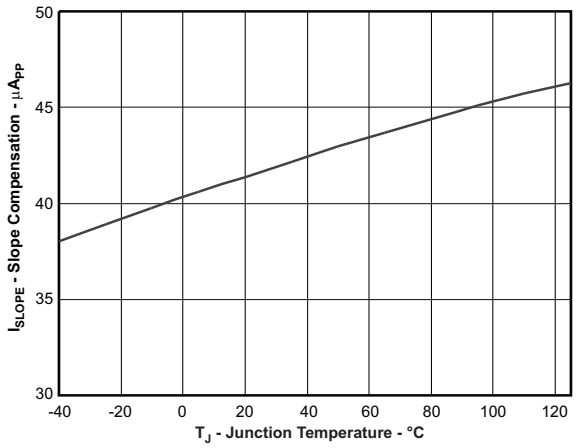


Figure 13.

BLANKING PERIOD vs TEMPERATURE

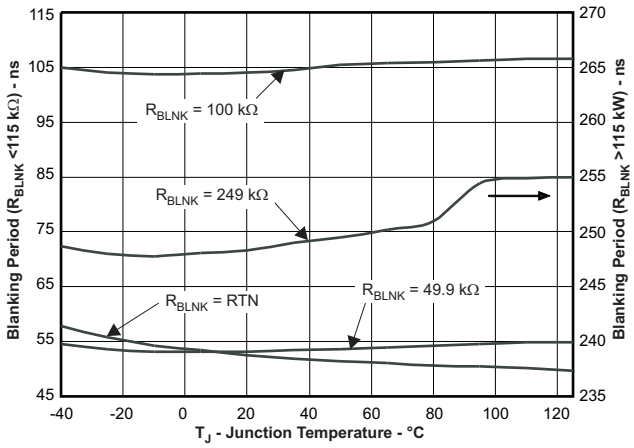


Figure 14.

TYPICAL CHARACTERISTICS (continued)

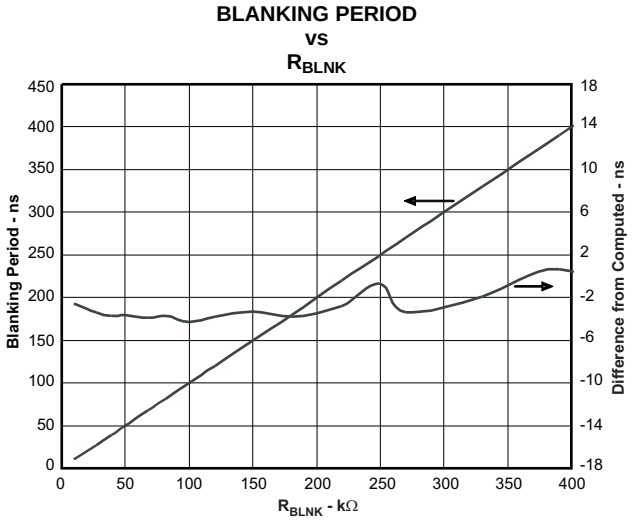


Figure 15.

APPLICATIONS

Classic PoE Overview

The following text is intended as an aid in understanding the operation of the TPS23753 but not as a substitute for the actual IEEE 802.3at standard. The IEEE 802.3at standard is an update to IEEE 802.3-2008 clause 33 (PoE), adding high-power options and enhanced classification. Generally speaking, a device compliant to IEEE 802.3-2008 will be referred to as a Type 1 device, and devices with high power or enhanced classification will be referred to as Type 2 devices. Standards change and should always be referenced when making design decisions.

The IEEE 802.3at standard defines a method of safely powering a PD (powered device) over a cable, and then removing power if a PD is disconnected. The process proceeds through an idle state and three operational states of detection, classification, and operation. The PSE leaves the cable unpowered (idle state) while it periodically looks to see if something has been plugged in; this is referred to as detection. The low power levels used during detection are unlikely to damage devices not designed for PoE. If a valid PD signature is present, the PSE may inquire how much power the PD requires; this is referred to as classification. Type 2 PSEs are required to do hardware classification. The PD may return the default 13W current-encoded class, or one of four other choices. The PSE may then power the PD if it has adequate capacity. Once started, the PD must present the maintain power signature (MPS) to assure the PSE that it is still present. The PSE monitors its output for a valid MPS, and turns the port off if it loses the MPS. Loss of the MPS returns the PSE to the idle state. Figure 16 shows the operational states as a function of PD input voltage.

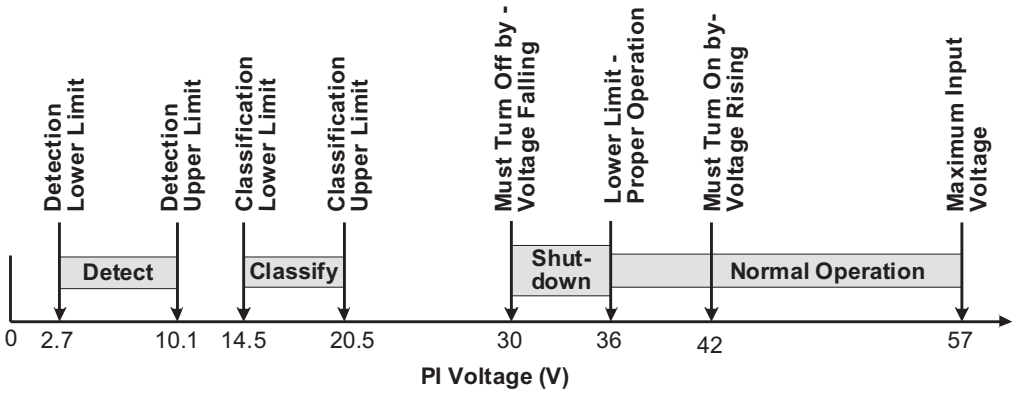


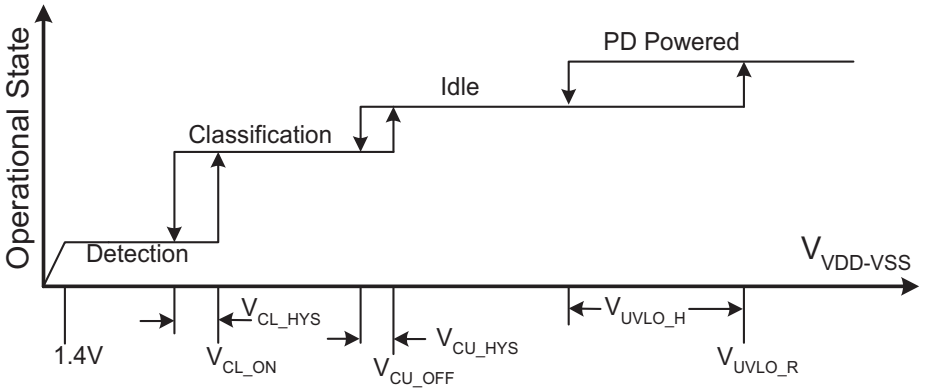
Figure 16. IEEE 802.3at (Type 1) Operational States

The PD input is typically an RJ-45 eight-lead connector which is referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops in the cable and operating margin. The IEEE 802.3at standard uses a cable resistance of 20 Ω (for type 1 devices) to derive the voltage limits at the PD based on the PSE output voltage requirements. Although the standard specifies an output power of 15.4 W at the PSE, only 13 W is available at the PI due to the worst-case power loss in the cable. The PSE can apply voltage either between the RX and TX pairs (pins 1–2 and 3–6 for 10baseT or 100baseT), or between the two spare pairs (4–5 and 7–8). The PSE may only apply voltage to one set of pairs at a time. The PD uses input diode bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges create a difference between the standard limits at the PI and the TPS23753 specifications.

The PSE is permitted to disconnect a PD if it draws more than its maximum class power over a one second interval. A type 1 PSE compliant to IEEE 802.3at is required to limit current to between 400 mA and an upper-bound template (IEEE 802.3-2008 was 450 mA) during powered operation. The PSE must disconnect the PD if it draws this current for more than 75 ms. Class 0 and 3 PDs may draw up to 400 mA peak currents for up to 50 ms. The PSE may set lower output current limits based on the PD's declared power requirements.

Threshold Voltages

The TPS23753 has a number of internal comparators with hysteresis for stable switching between the various states as shown in Figure 16. Figure 17 relates the parameters in the Electrical Characteristics section to the PoE states. The mode labeled idle between classification and operation implies that the DEN, CLS, and RTN pins are all high impedance.



Note: Variable names refer to Electrical Characteristic Table parameters

Figure 17. Threshold Voltages

PoE Startup Sequence

The waveforms of Figure 18 demonstrate detection, classification, and startup from a type 1 PSE. The key waveforms shown are $V_{VDD-VSS}$, $V_{RTN-VSS}$, and I_{PI}. IEEE 802.3at requires a minimum of two detection levels; however; four levels are shown in this example. Four levels guard against misdetection of a device when plugged in during the detection sequence.

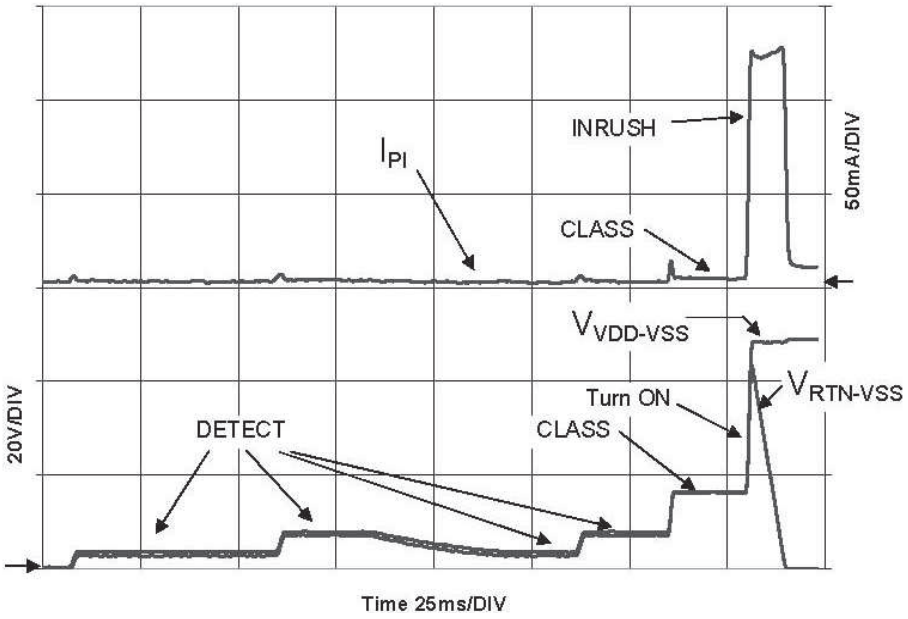


Figure 18. PoE Startup Sequence

Detection

The TPS23753 is in detection mode whenever $V_{VDD-V\ SS}$ is below the lower classification threshold. When the input voltage rises above V_{CL_ON}, the DEN pin goes to an open-drain condition to conserve power. While in detection, RTN is high impedance, almost all the internal circuits are disabled, and the DEN pin is pulled to V_{SS}. An R_{DEN} of 24.9 kΩ (1%), presents the correct signature. It may be a small, low-power resistor since it only sees a stress of about 5 mW. A valid PD detection signature is an incremental resistance between 23.75 kΩ and 26.25 kΩ at the PI.

The detection resistance seen by the PSE at the PI is the result of the input bridge resistance in series with the parallel combination of R_{DEN} and the TPS23753 bias loading. The input diode bridge's incremental resistance may be hundreds of Ohms at the very low currents drawn when 2.7 V is applied to the PI. The input bridge resistance is partially cancelled by the TPS23753's effective resistance during detection.

Hardware Classification

Hardware classification allows a PSE to determine a PD's power requirements before starting and helps with power management once power is applied. The maximum power entries in Table 2 determine the class the PD must advertise. A Type 1 PD may not advertise Class 4. The PSE may disconnect a PD if it draws more than its stated Class power. The standard permits the PD to draw limited current peaks, however the average power requirement always applies.

Voltage between 14.5 V and 20.5 V is applied to the PD for up to 75 ms during hardware Classification. A fixed output voltage is sourced by the CLS pin, causing a fixed current to be drawn from V_{DD} through R_{CLS}. The total current drawn from the PSE during classification is the sum of bias and R_{CLS} currents. PD current is measured and decoded by the PSE to determine which of the five available classes is advertised (see Table 2). The TPS23753 disables classification above V_{CU_OFF} to avoid excessive power dissipation. CLS voltage is turned off during PD thermal limit or when APD or DEN are active. The CLS output is inherently current limited, but should not be shorted to V_{SS} for long periods of time.

Table 2. Class Resistor Selection

CLASS	POWER AT PD PI		Class Current Requirement		RESISTOR (Ω)	NOTES
	MINIMUM (W)	MAXIMUM (W)	MINIMUM (mA)	MAXIMUM (mA)		
0	0.44	12.95	0	4	1270	
1	0.44	3.84	9	12	243	
2	3.84	6.49	17	20	137	
3	6.49	12.95	26	30	90.9	
4	12.95	25.5	36	44	63.4	Only permitted for type 2 devices

Maintain Power Signature (MPS)

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. A valid MPS consists of a minimum dc current of 10 mA (at a duty cycle of at least 75 ms on every 225 ms) and an ac impedance lower than 26.25 kΩ in parallel with 0.05 µF. The ac impedance is usually accomplished by the minimum C_{IN} requirement of 5 µF. When APD or DEN are used to force the hotswap switch off, the dc MPS will not be met. A PSE that monitors the dc MPS will remove power from the PD when this occurs. A PSE that monitors only the ac MPS may remove power from the PD.

TPS23753 Operation

Startup and Converter Operation

The internal PoE UVLO (Under Voltage Lock Out) circuit holds the hotswap switch off before the PSE provides full voltage to the PD. This prevents the converter circuits from loading the PoE input during detection and classification. The converter circuits will discharge C_{IN}, C_{VC}, and C_{VB} while the PD is unpowered. Thus $V_{RTN-VDD}$ will be a small voltage just after full voltage is applied to the PD, as seen in Figure 18.

The PSE drives the PI voltage to the operating range once it has decided to power up the PD. When V_{DD} rises above the UVLO turn-on threshold (V_{UVLO-R}, ~35 V) with RTN high, the TPS23753 enables the hotswap MOSFET with a ~140 mA (inrush) current limit. Refer to the waveforms of Figure 19 for an example. Converter switching is disabled while C_{IN} charges and V_{RTN} falls from V_{DD} to nearly V_{SS}, however the converter startup circuit is allowed to charge C_{VC}. Once the inrush current falls about 10% below the inrush current limit, the PD control switches to the operational level (~450 mA) and converter switching is permitted.

Converter switching is allowed if the PD is not in inrush and the V_C under-voltage lock out (UVLO) permits it. Continuing the startup sequence shown in Figure 19, V_{VC} rises as the startup current source charges C_{VC} and M1 switching is inhibited by the status of the V_C UVLO. The V_B regulator powers the internal converter circuits as V_{VC} rises. Startup current is turned off, converter switching is enabled, and a softstart cycle starts when V_{VC} exceeds $UVLO_1$ (~9 V). V_{VC} falls as it powers both the internal circuits and the switching MOSFET gate. If the converter control-bias output rises to support V_{VC} before it falls to $UVLO_1 – UVLO_{1H}$ (~5.5 V), a successful startup occurs. Figure 19 shows a small droop in V_{VC} while the output voltage rises smoothly and a successful startup occurs.

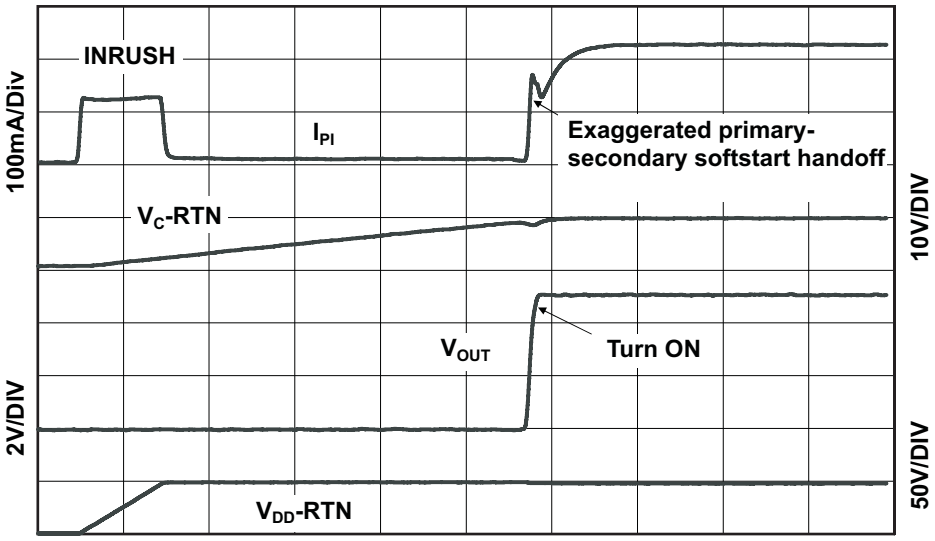


Figure 19. Power Up and Start

If $V_{VDD-VSS}$ drops below the lower PoE UVLO ($UVLO_R – UVLO_H$, ~30.5 V), the hotswap MOSFET is turned off, but the converter will still run. The converter will stop if V_{VC} falls below the converter UVLO ($UVLO_1 – UVLO_H$, ~5.5 V), the hotswap is in inrush current limit, or 0% duty cycle is demanded by V_{CTL} ($V_{CTL} < V_{ZDC}$, ~1.5 V), or the converter is in thermal shutdown.

PD Interface Features

The PD section has the following functions, with the first four covered above.

- Detection
- Classification
- V_{DD} to V_{SS} UVLO
- Orderly sequencing of C_{IN} charge and converter operation
- Hotswap switch current limit
- Hotswap switch foldback
- Hotswap thermal protection

The internal hotswap MOSFET is protected against output faults with a current limit and deglitched foldback. The PSE output cannot be relied on to protect the PD MOSFET against transient conditions, so the PD implements its own protection. High stress conditions include converter output shorts, shorts from V_{DD} to RTN, or transients on the input line. An overload on the pass MOSFET engages the current limit, with $V_{RTN-VSS}$ rising as a result. If V_{RTN} rises above ~12 V for longer than ~400 µs, the current limit reverts to the inrush limit, and turns the converter off. The 400 µs deglitch feature prevents momentary transients from causing a PD reset, provided that recovery lies within the bounds of the hotswap and PSE protection. Figure 20 shows an example of recovery from a 15 V PSE rising voltage step. The hotswap MOSFET goes into current limit, overshooting to a relatively low current, recovers to 420 mA full current limit, and charges the input capacitor while the converter continues to run. The MOSFET did not go into foldback because $V_{RTN-VSS}$ was below 12 V after the 400 µs deglitch.

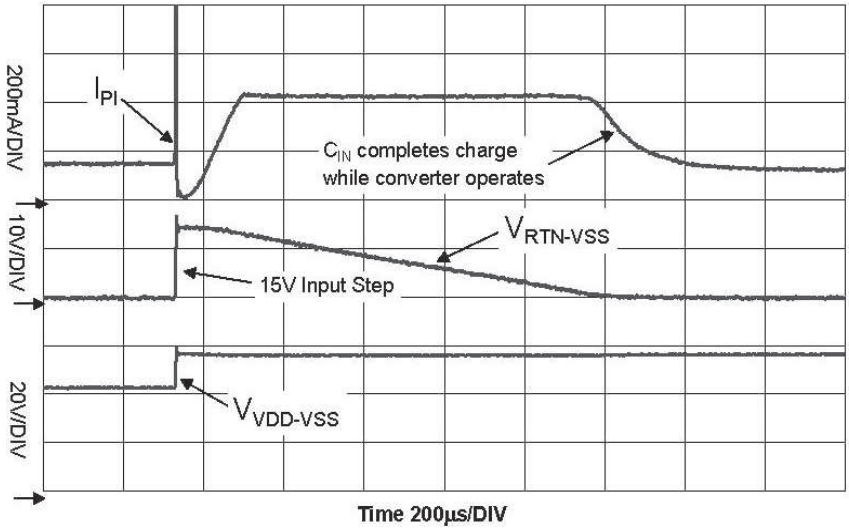


Figure 20. Response to PSE Step Voltage

The PD control has a thermal sensor that protects the internal hotswap MOSFET. Conditions like startup or operation into a V_{DD} to RTN short cause high power dissipation in the MOSFET. An overtemperature shutdown (OTSD) turns off the hotswap MOSFET and class regulator, which are restarted after the device cools. The PD state machine will always restart in inrush current limit when exiting from a PD overtemperature event.

Pulling DEN to V_{SS} during powered operation causes the internal hotswap MOSFET to turn off. This feature allows a PD with secondary-side adapter ORing to achieve adapter priority. Care must be taken with synchronous converter topologies that can deliver power in both directions.

The hotswap switch will be forced off under the following conditions:

- V_{APD} above V_{APDEN} (~1.5 V)
- $V_{DE\ N} \leq V_{PD\_DIS}$ when $V_{VDD-VSS}$ is in the operational range
- PD over temperature
- $V_{VDD-VSS}$ < PoE UVLO (~30.5 V).

Converter Controller Features

The TPS23753 dc/dc controller implements a typical current-mode control as shown in Figure 2. Features include oscillator, overcurrent and PWM comparators, current-sense blanker, softstart, and gate driver. In addition, an internal current-compensation ramp generator, frequency synchronization logic, thermal shutdown, and startup current source with control are provided.

The TPS23753 is optimized for isolated converters, and does not provide an internal error amplifier. Instead, the optocoupler feedback is directly fed to the CTL pin which serves as a current-demand control for the PWM and converter. There is an offset of V_{ZDC} (~1.5 V) and 2:1 resistor divider between the CTL pin and the PWM. A V_{CTL} below V_{ZDC} will stop converter switching, while voltages above (V_{ZDC} + 2 × V_{CSMAX}) will not increase the requested peak current in the switching MOSFET. Optocoupler biasing design is eased by this limited control range.

The internal startup current source and control logic implement a bootstrap-type startup. The startup current source charges C_{VC} from V_{DD1} when the converter is disabled (either by the PD control or the V_C control), while operational power must come from a converter (bias winding) output. Loading on V_C and V_B must be minimal while C_{VC} charges, otherwise the converter may never start. The optocoupler will not load V_B when the converter is off. The converter will shut off when V_C falls below its lower UVLO. This can happen when power is removed from the PD, or during a fault on a converter output rail. When one output is shorted, all the outputs fall in voltage including the one that powers V_C. The control circuit discharges V_C until it hits the lower UVLO and turns off. A restart will initiate as described in "Startup and Converter Operation" if the converter turns off and there is sufficient V_{DD1} voltage. This type of operation is sometimes referred to as “hiccup mode,” which provides robust output short protection by providing time-average heating reduction of the output rectifier.

Care in design of the transformer and V_C bias circuit is required to obtain hiccup overload protection. Leading-edge voltage overshoot on the bias winding may cause V_C to peak-charge, preventing the expected tracking with output voltage. R_{VC} (Figure 1) is often required slow the peak charging. Good transformer bias-to-output-winding coupling results in reduced overshoot and better voltage tracking.

The startup current source transitions to a resistance as (V_{DD1} - V_C) falls below 7 V, but will start the converter from 12 V adapters within t_{ST} (V_{DD1} ≥ 10.2, V~85 ms). The bootstrap source provides reliable startup from widely varying input voltages, and eliminates the continual power loss of external resistors. The startup current source will not charge above the maximum recommended V_{VC} if the converter is disabled and there is sufficient V_{DD1} to charge higher.

The peak current limit does not have duty cycle dependency unless R_S is used as shown in Figure 22 to increase slope compensation. This makes it easier to design the current limit to a fixed value.

The TPS23753 blanker timing is precise enough that the traditional R-C filters on CS can be eliminated. This avoids current-sense waveform distortion, which tends to get worse at light output loads. While the internally set blanking period is relatively precise, almost all converters will require their own blanking period. The TPS23753 provides the BLNK pin to allow this programming. There may be some situations or designers that prefer an R-C approach. The TPS23753 provides a pull-down on CS during the GATE off time to improve sensing when an R-C filter must be used. The CS input signal should be protected from nearby noisy signals like GATE drive and the MOSFET drain.

Converters require a softstart on the voltage error amplifier to prevent output overshoot on startup. Figure 21 shows a common implementation of a secondary-side softstart that works with the typical TL431 error amplifier shown in Figure 1. This secondary-side error amplifier will not become active until there is sufficient voltage on the secondary. The TPS23753 provides a primary-side softstart which persists long enough (~800 µs) for secondary side voltage-loop softstart to take over. The primary-side current-loop softstart controls the switching MOSFET peak current by applying a slowly rising ramp voltage to a second PWM control input. Figure 19 shows an exaggerated handoff between the primary and secondary-side softstart that is most easily seen in the I_{PI} waveform. The output voltage rises in a smooth monotonic fashion with no overshoot. This handoff can be optimized by decreasing the secondary-side softstart period.

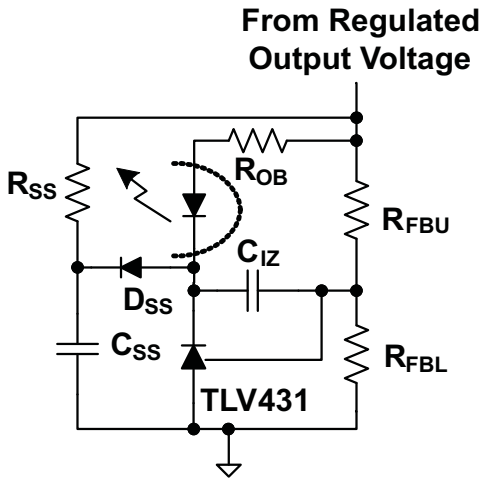


Figure 21. Example of Softstart Circuit Added to Error Amplifier

The dc/dc controller has an OTSD that can be triggered by heat sources including the V_B regulator, GATE driver, bootstrap current source, and bias currents. The controller OTSD turns off V_B, the GATE driver, resets the softstart generator, and forces the V_C control into an under-voltage state.

Special Switching MOSFET Considerations

Special care must be used in selecting the converter switching MOSFET. The TPS23753 converter section has minimum V_C operating voltage of ~5.5 V, which is reflected in the applied gate voltage. This will occur during an output overload, or towards the end of a (failed) bootstrap startup. The MOSFET must be able to carry the anticipated peak fault current at this gate voltage.

Thermal Considerations

Sources of nearby local PCB heating should be considered during the thermal design. Typical calculations assume that the TPS23753 is the only heat source contributing to the PCB temperature rise. It is possible for a normally operating TPS23753 device to experience an OTSD event if it is excessively heated by a nearby device.

Blanking – R_{BLNK}

The TPS23753 BLNK feature permits programming of the blanking period with specified tolerance. Selection of the blanking period is often empirical because it is affected by parasitics and thermal effects of every device between the gate-driver and output capacitors.

There is a critical range of blanking period that is bounded on the short side by erratic operation, and on the long side by potentially harmful switching-MOSFET and output rectifier currents during a short circuit. The minimum blanking period prevents the current limit and PWM comparators from being falsely triggered by the inherent current “spike” that occurs when the switching MOSFET turns on. The maximum blanking period is bounded by the output rectifier's ability to withstand the currents experienced during a converter output short. A short on the flyback transformer secondary will cause very large peak MOSFET currents that are worsened by longer blanking periods. A long blanking time also increases the minimum load required before cycle skipping occurs in a non-synchronous converter.

The TPS23753 provides a choice between internal fixed and programmable blanking periods. The blanking period is specified as an increase in the minimum GATE on time over the inherent gate driver and comparator delays. The default period (see the Electrical Characteristics table) is selected by connecting BLNK to RTN, and the programmable period is set with a resistor from BLNK to RTN per the following equation.

$$R_{BLNK}\left(k\Omega\right) = t_{BLNK}\left(ns\right) \tag{5}$$

For example, a 100 ns period is programmed by a 100 kΩ resistor. For a brand-new design, it is recommended that an initial blanking period of 125 ns be designed in. This period should be tuned once the converter is operational.

Current Slope Compensation

Current-mode control requires addition of a compensation ramp to the sensed inductor (flyback transformer) current for stability at duty cycles near and over 50%. The TPS23753 has a maximum duty cycle limit of 80%, permitting the design of wide input-range flyback converters with a lower voltage stress on the output rectifiers. While the maximum duty cycle is 80%, converters may be designed that run at duty cycles well below 80% for a narrower, 36 V to 57 V range. The TPS23753 provides a fixed internal compensation ramp that suffices for most applications. R_S (see Figure 22) may be used if the internally provided slope compensation is not enough. It works with ramp current (I_{PK} = I_{SL-EX}, ~40 µA) that flows out of the CS pin when the MOSFET is on. The I_{PK} specification does not include the ~3 µA fixed current that flows out of the CS pin.

Most current-mode control papers and application notes define the slope values in terms of V_{PP}/T_S (peak ramp voltage / switching period), however the electrical characteristics table specifies the slope peak (V_{SLOPE}) based on an 80% duty cycle. Assuming that the desired slope, $V_{SLOPE-D}$ (in mV/period), is based on the full period, compute R_S per the following equation where V_{SLOPE}, D_{MAX}, and I_{SL-EX} are from the electrical characteristics table with voltages in mV, current in µA, and the duty cycle is unitless (e.g. D_{MAX} = 0.8).

$$R_S(\Omega) = \frac{\left[V_{SLOPE\_D}(mV) - \left(V_{SLOPE}(mV) \middle/ D_{MAX}\right)\right]}{I_{SL\_EX}(\mu A)} \cdot 1000 \tag{6}$$

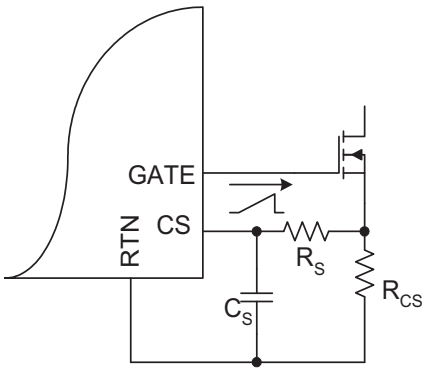


Figure 22. Additional Slope Compensation

C_S may be required if the presence of R_S causes increased noise, due to adjacent signals like the gate drive, to appear at the C_S pin. The TPS23753 has an internal pull-down on C_S (~500 Ω) while the MOSFET is OFF to reduce cycle-to-cycle carry-over voltage on C_S.

FRS and Synchronization

The FRS pin programs the (free-running) oscillator frequency, and may also be used to synchronize the TPS23753 converter to a higher frequency. The internal oscillator sets the maximum duty cycle at 80% and controls the current-compensation ramp circuit. R_{FRS} should be selected per the following equation.

$$R_{FRS}(k\Omega) = \frac{15000}{f_{SW}(kHz)} \quad (7)$$

The TPS23753 may be synchronized to an external clock to eliminate beat frequencies from a sampled system, or to place emission spectrum away from an RF input frequency. Synchronization may be accomplished by applying a short pulse (> 25 ns) of magnitude V_{SYNC} to FRS as shown in Figure 23. R_{FRS} should be chosen so that the maximum free-running frequency is just below the desired synchronization frequency. The synchronization pulse terminates the potential on-time period, and the off-time period doesn't begin until the pulse terminates. A short pulse is preferred to avoid reducing the potential on-time.

Figure 23 shows examples of non-isolated and transformer-coupled synchronization circuits The pulse at the FRS pin should reach between 2.5 V and V_B, with a minimum width of 22 ns (above 2.5 V) and rise/fall times less than 10 ns. The FRS node should be protected from noise because it is high-impedance.

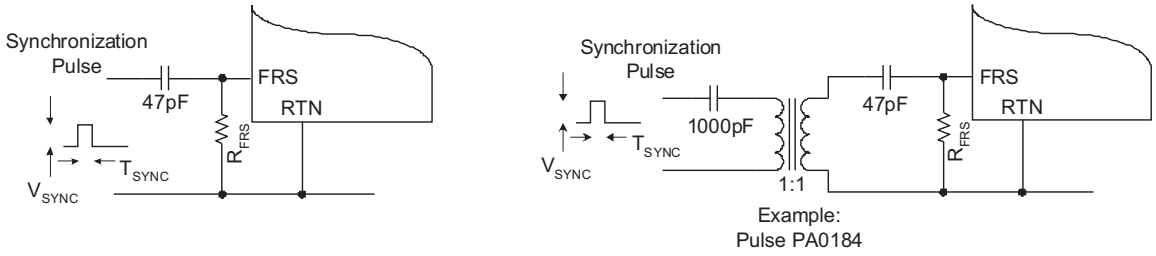


Figure 23. Synchronization

Adapter ORing

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used if PoE is not available in a particular installation. While most applications only require that the PD operate when both sources are present, the TPS23753 supports forced operation from either of the power sources. Figure 24 illustrates three options for

diode ORing external power into a PD. Only one option would be used in any particular design. Option 1 applies power to the TPS23753 PoE input, option 2 applies power between the TPS23753 PoE section and the power circuit, and option 3 applies power to the output side of the converter. Each of these options has advantages and disadvantages. A detailed discussion of the TPS23753 and ORing solutions is covered in application note *Advanced Adapter ORing Solutions using the TPS23753*, literature number SLVA306.

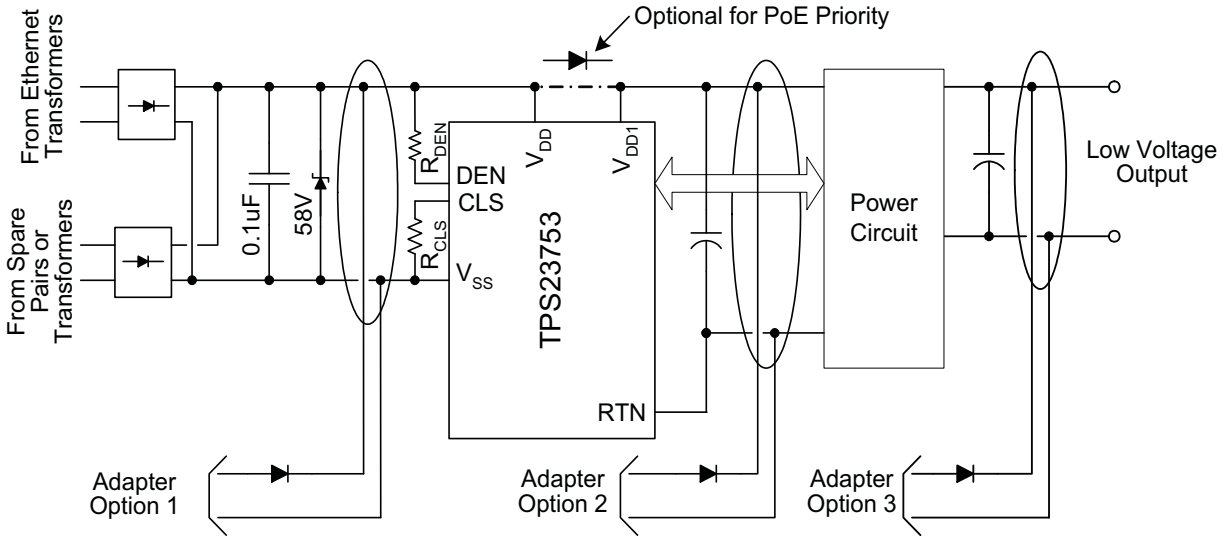


Figure 24. ORing Configurations

Preference of one power source presents a number of challenges. Combinations of adapter output voltage (nominal and tolerance), power insertion point, and which source is preferred determine solution complexity. Several factors which add to the complexity are the natural high-voltage selection of diode ORing (the simplest method of combining sources), the current limit implicit in the PSE, and PD inrush and protection circuits (necessary for operation and reliability). Creating simple and seamless solutions is difficult if not impossible for many of the combinations. However the TPS23753 offers several built-in features that simplify some combinations.

Several examples will demonstrate the limitations inherent in ORing solutions. Diode ORing a 48 V adapter with PoE (option 1) presents the problem that either source might be higher. A blocking switch would be required to assure which source was active. A second example is combining a 12 V adapter with PoE using option 2. The converter will draw approximately four times the current at 12 V from the adapter than it does from PoE at 48 V. Transition from adapter power to PoE may demand more current than can be supplied by the PSE. The converter must be turned off while C_{IN} capacitance charges, with a subsequent converter restart at the higher voltage and lower input current. A third example is use of a 12 V adapter with ORing option 1. The PD hotswap would have to handle four times the current, and have 1/16 the resistance (be 16 times larger) to dissipate equal power. A fourth example is that MPS is lost when running from the adapter, causing the PSE to remove power from the PD. If ac power is then lost, the PD will stop operating until the PSE detects and powers the PD.

The most popular preferential ORing scheme is option 2 with adapter priority. The hotswap MOSFET is disabled when the adapter is used to pull APD high, blocking the PoE source from powering the output. This solution works well with a wide range of adapter voltages, is simple, and requires few external parts. When the ac power fails, or the adapter is removed, the hotswap switch is enabled. In the simplest implementation, the PD will momentarily loose power until the PSE completes its startup cycle.

The DEN pin can be used to disable the PoE input when ORing with option 3. This is an adapter priority implementation. Pulling DEN low, while creating an invalid detection signature, disables the hotswap MOSFET and prevents the PD from redetecting. This would typically be accomplished with an optocoupler that is driven from the secondary side of the converter.

The least popular technique is PoE priority. It is implemented by placing a diode between the PD supply voltage, V_{DD}, and the dc/dc controller bias voltage, V_{DD1}. The diode prevents reverse biasing of the PoE input diode bridges when option 2 adapter ORing is used. The PSE may then detect, classify, and provide power to the PD while a live adapter is connected. As long as the PoE voltage is greater than the adapter voltage, the PSE will power the load. The APD function is not used in this technique.

The IEEE standards require that the Ethernet cable be isolated from ground and all other system potentials. The adapter must meet a minimum 1500 Vac dielectric withstand test between the output and all other connections for options 1 and 2. The adapter only needs this isolation for option 3 if it is not provided by the converter.

Adapter ORing diodes are shown for all the options to protect against a reverse voltage adapter, a short on the adapter input pins, and damage to a low-voltage adapter. ORing is sometimes accomplished with a MOSFET in option 3.

Protection

A TVS across the rectified PoE voltage per Figure 1 must be used. An SMAJ58A, or a part with equal to or better performance, is recommended for general indoor applications. If an adapter is connected from V_{DD1} to RTN, as in ORing option 2 above, voltage transients caused by the input cable inductance ringing with the internal PD capacitance can occur. Adequate capacitive filtering or a TVS must limit this voltage to be within the absolute maximum ratings. Configurations that use D_{VDD} as in Figure 25 may require additional protection against ESD transients that would turn D_{VDD} off and force all the voltage to appear across the internal hotswap MOSFET. C_{VDD} and D_{RTN} per Figure 25 provide this additional protection.

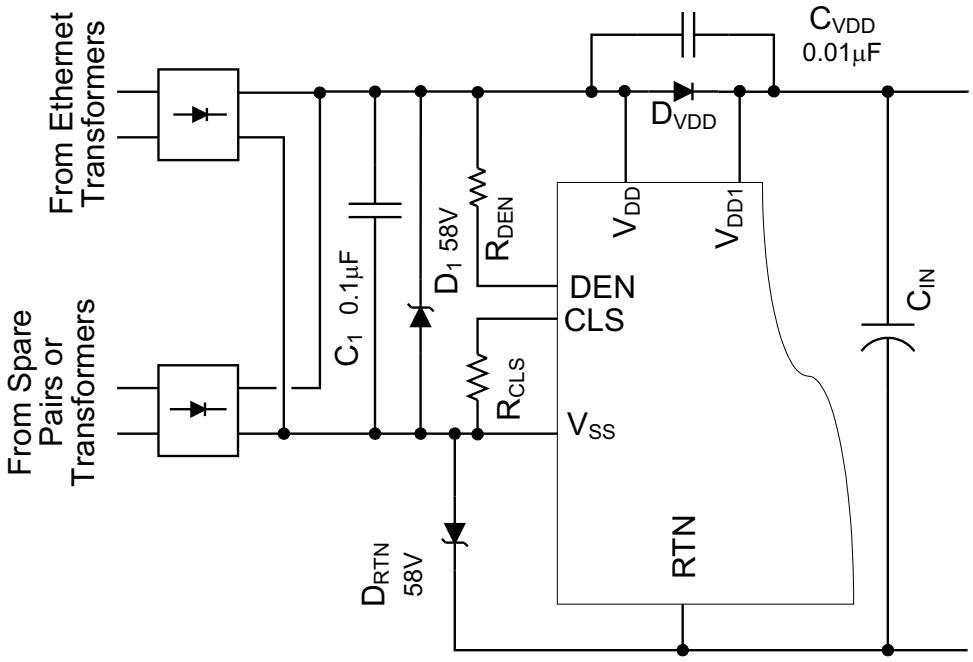


Figure 25.

Outdoor applications require more extensive protection to lightning standards.

Frequency Dithering for Conducted Emissions Control

The international standard CISPR 22 (and adopted versions) is often used as a requirement for conducted emissions. Ethernet cables are covered as a telecommunication port under section 5.2 for conducted emissions. Meeting EMI requirements is often a challenge, with the lower limits of Class B being especially hard. Circuit board layout, filtering, and snubbing various nodes in the power circuit are the first layer of control techniques. A more detailed discussion of EMI control is presented in *Practical Guidelines to Designing an EMI Compliant PoE Powered Device With Isolated Flyback*, TI literature number SLUA469. Additionally, IEEE802.3at section 33.4 has requirements for noise injected onto the Ethernet cable based on compatibility with data transmission.

Occasionally, a technique referred to as frequency dithering is utilized to provide additional EMI measurement reduction. The switching frequency is modulated to spread the narrowband individual harmonics across a wider bandwidth, thus lowering peak measurements. The circuit of Figure 26 modulates the switching frequency by feeding a small ac signal into the FRS pin. These values may be adapted to suit individual needs.

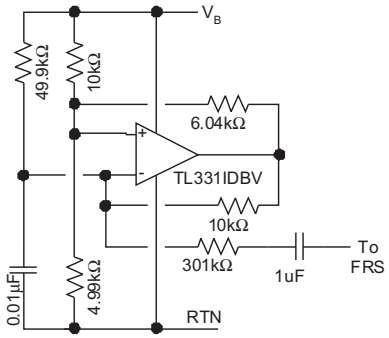


Figure 26. Frequency Dithering

Design Procedure

A detailed design procedure for PDs using the TPS23753 is covered in *Designing with the TPS23753 Powered Device and Power Supply Controller* , literature number SLVA305.

References

IEEE Standard for Information Technology … Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications, IEEE Computer Society, IEEE 802.3™at (Clause 33)

Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement, International Electrotechnical Commission, CISPR 22 Edition 5.2, 2006-03

Designing with the TPS23753 Powered Device and Power Supply Controller, Eric Wright, TI, SLVA305

Advanced Adapter ORing Solutions using the TPS23753, Eric Wright, TI, SLVA306

Practical Guidelines to Designing an EMI-Compliant PoE Powered Device With Isolated Flyback, Donald V. Comiskey, TI, SLUA469

REVISION HISTORY

Changes from Original (June 2008) to Revision A **Page**

- Changed data sheet From: Product Preview To: Production 1
- Changed the TPS23753 Functional Block Diagram. 6
- Added the Typical Characteristics section. 9

Changes from Revision A (June 2008) to Revision B **Page**

- Changed the ESDS statement. 2

Changes from Revision B (September 2009) to Revision C **Page**

- Changed From: IEEE 802.3-2005 To: IEEE 802.3 throughout the data sheet. 1
- Changed the 1st paragraph in the Description From: The PoE implementation supports the IEEE 802.3-2005 (previously 802.3af) standard, 12.95 W (13 W) PD. To: The PoE implementation supports the IEEE 802.3-2005. An IEEE802.3at type 1 device is equivalent to IEEE802.3-2008 (originally 802.3af) standard as a 13 W type 1 PD. 1
- Changed Note 1 in the Dissipations Ratings table to include additional information. 2
- Changed section Classic PoE Overview second paragraph: From: The PD may return the default 12.95W (often referred to as 13W) current-encoded class, or one of four other choices. To: The PD may return the default 13W current-encoded class, or one of four other choices 13
- Changed Table 2 - Notes for the Class 4 row 15
- Added text and Figure 25 to the Protection section 22

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS23753PW	NRND	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TP23753
TPS23753PW.A	NRND	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TP23753
TPS23753PWG4	NRND	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TP23753
TPS23753PWR	NRND	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TP23753
TPS23753PWR.A	NRND	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TP23753

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

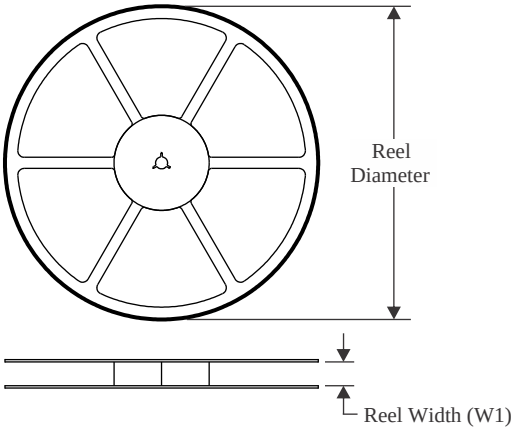
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

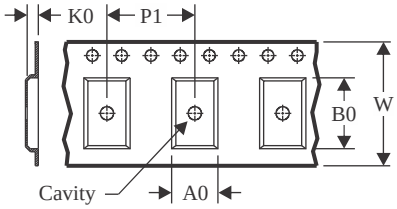
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

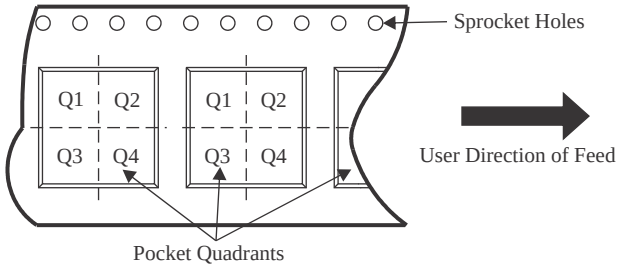


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

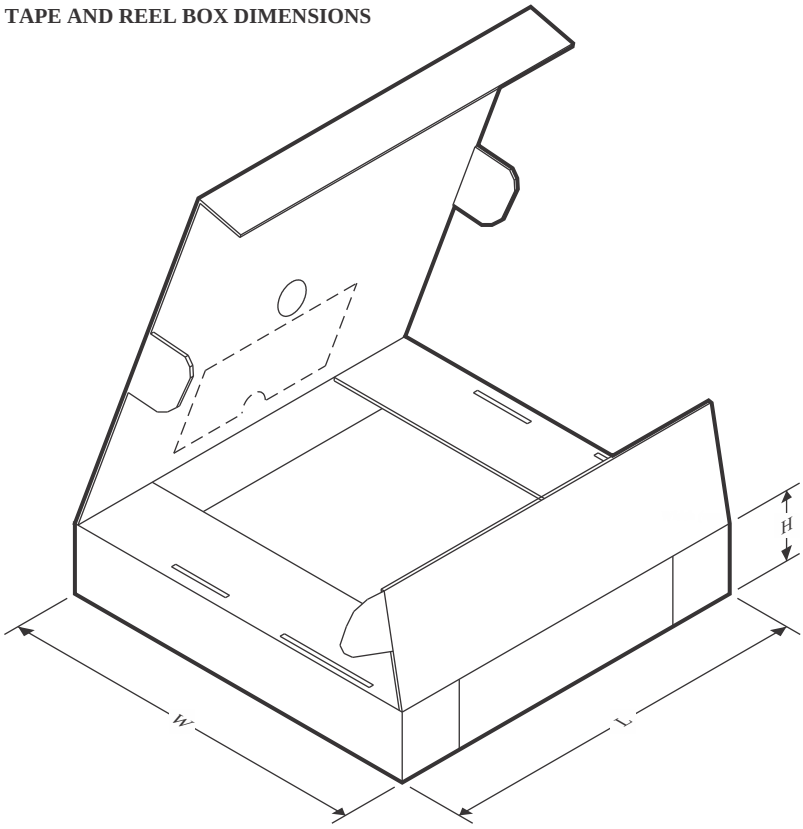
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS23753PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

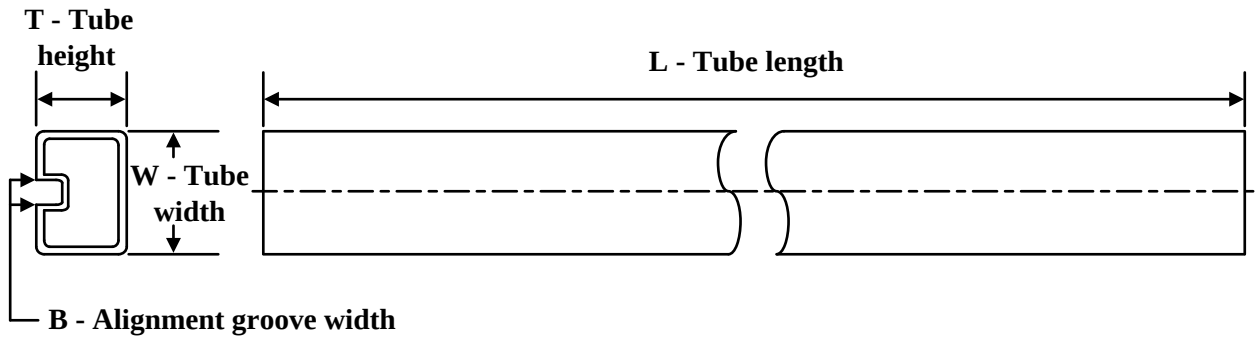
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS23753PWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

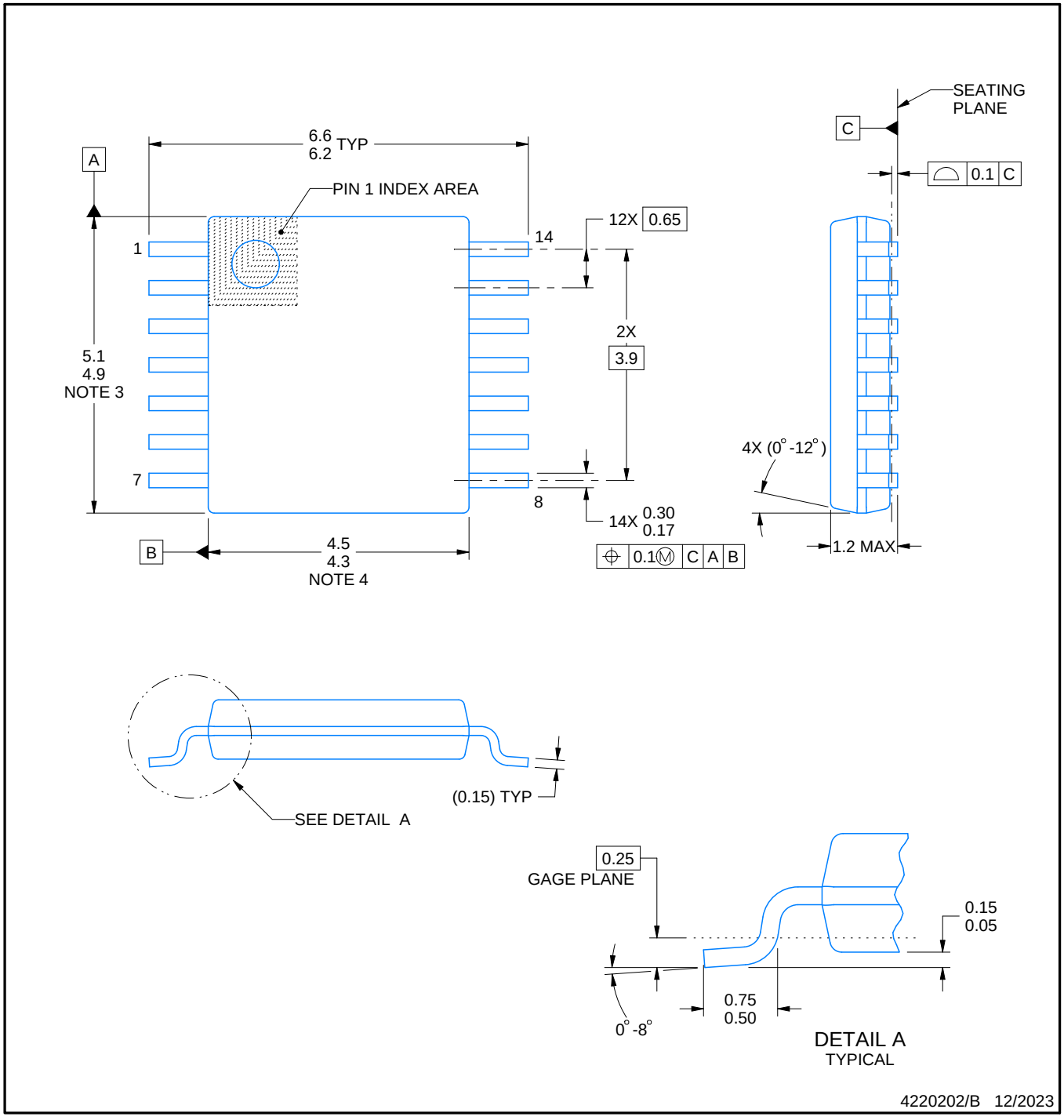
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS23753PW	PW	TSSOP	14	90	530	10.2	3600	3.5
TPS23753PW.A	PW	TSSOP	14	90	530	10.2	3600	3.5
TPS23753PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

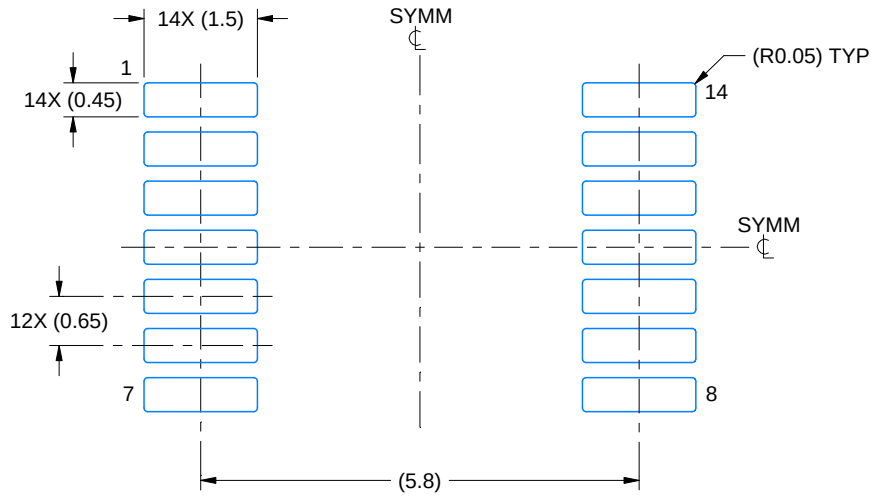
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

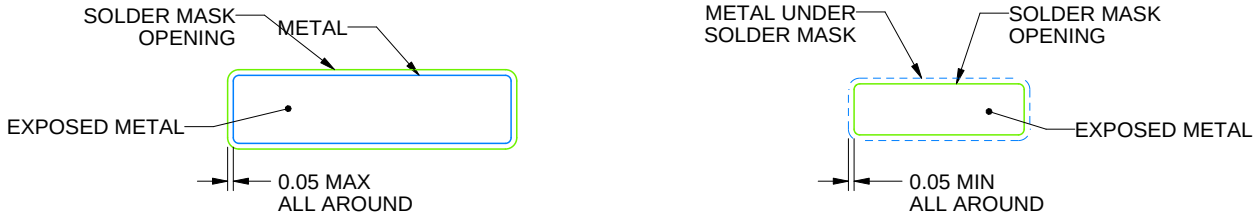


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

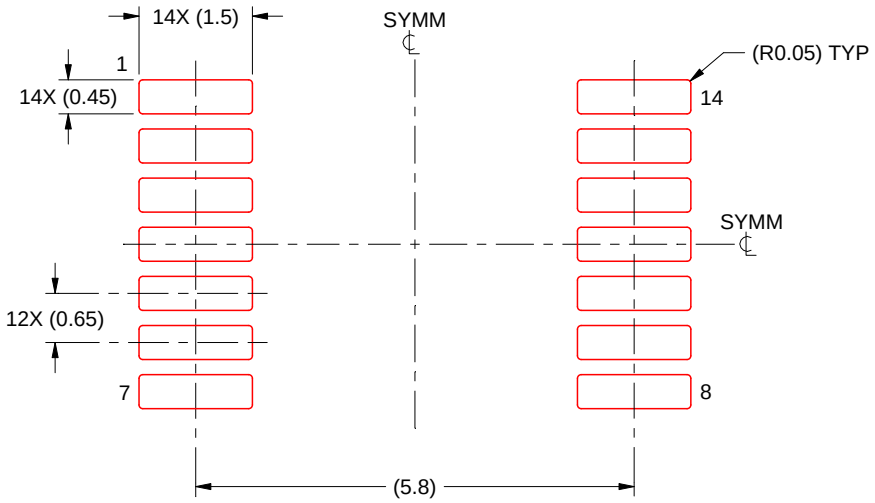


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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