











SLVSBJ0F-AUGUST 2012-REVISED AUGUST 2016

**TPS22965** 

# TPS22965 5.7-V, 6-A, 16-m $\Omega$ On-Resistance Load Switch

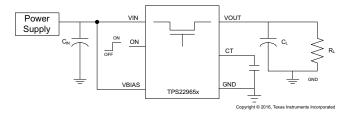
#### **Features**

- Integrated Single Channel Load Switch
- Input Voltage Range: 0.8 V to 5.7 V
- Ultra-Low On Resistance (R<sub>ON</sub>)
  - $R_{ON} = 16 \text{ m}\Omega$  at VIN = 5 V (VBIAS = 5 V)
  - $R_{ON} = 16 \text{ m}\Omega$  at VIN = 3.6 V (VBIAS = 5 V)
  - $R_{ON}$  = 16 mΩ at VIN = 1.8 V (VBIAS = 5 V)
- 6-A Maximum Continuous Switch Current
- Low Quiescent Current (50 µA)
- Low Control Input Threshold Enables Use of 1.2-, 1.8-, 2.5-, and 3.3-V Logic
- Configurable Rise Time
- Quick Output Discharge (QOD) (Optional)
- SON 8-pin Package With Thermal Pad
- ESD Performance Tested per JESD 22
  - 2000-V HBM and 1000-V CDM

# **Applications**

- Ultrabook™
- Notebooks and Netbooks
- Tablet PC
- Consumer Electronics
- Set-top Boxes and Residential Gateways
- **Telecom Systems**
- Solid State Drives (SSDs)

#### Simplified Schematic



# 3 Description

The TPS22965x is a single channel load switch that provides configurable rise time to minimize inrush current. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.8 V to 5.7 V and can support a maximum continuous current of 6 A. The switch is controlled by an on and off input (ON), which is capable of interfacing directly with low-voltage control signals. In the TPS22965, a 225- $\Omega$  on-chip load resistor is added for quick output discharge when switch is turned off.

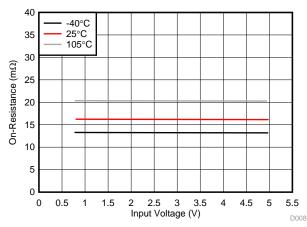
The TPS22965x is available in a small, space-saving 2-mm × 2-mm 8-pin SON package (DSG) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of -40°C to +105°C.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
TPS22965 TPS22965N	WSON (8)	2.00 mm × 2.00 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### On-Resistance vs Input Voltage $(V_{BIAS} = 5 \text{ V}, I_{OUT} = -200 \text{ mA})$





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Changes from Revision E (May 2016) to Revision F	Page
Updated all Typical Characteristics Graphs	
Changes from Revision D (March 2015) to Revision E	Page
Changed QOD from "TPS22965 Only" to "Optional" in Features section	
Changes from Revision C (February 2015) to Revision D	Pago
Added TPS22965N part number	
Updated Thermal Information table	(
Updated typical AC timing parameters (tables, graphs and scope captures)	1
Changes from Revision B (June 2014) to Revision C	Page
Extended Recommended Operating free-air temperature range maximum to 105°C	
• Added temperature operations to <i>Electrical Characteristics</i> , V <sub>BIAS</sub> = 5 V	(
Added temperature operations to <i>Electrical Characteristics</i> , V <sub>BIAS</sub> = 2.5 V	
Changes from Revision A (August 2013) to Revision B	Page
Added Device Information table	onal Modes

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Application and Implementation section, Power Supply Recommendations section, Layout section, Device and



w	/ww.ti.com	A Page
•	Added Thermal Information table	6
С	Changes from Original (August 2012) to Revision A	Page
•	Updated VON MAX value to fix typo that restricted operating range. Chawith rest of document.	



# 5 Device Comparison Table

DEVICE	R <sub>ON</sub> AT 3.3 V (TYP)	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22965	16 m $\Omega$	Yes	6 A	Active high
TPS22965N	16 mΩ	No	6 A	Active high

# 6 Pin Configuration and Functions



#### **Pin Functions**

	PIN				
No.	NAME	I/O	DESCRIPTION		
1 2	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V <sub>IN</sub> dip. Must be connected to Pin 1 and Pin 2. See the <i>Application and Implementation</i> section for more information		
3	ON	I	ive high switch control input. Do not leave floating		
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.7 V. See the <i>Application and Implementation</i> section for more information		
5	GND	_	Device ground		
6	СТ	0	Switch slew rate control. Can be left floating. See the <i>Adjustable Rise Time</i> section for more information		
7	VOLIT	0	Contract and and		
8	VOUT	0	Switch output		
_	Thermal Pad	_	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the <i>Layout Example</i> section for layout guidelines		



# 7 Specifications

#### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	-0.3	6	V
V <sub>OUT</sub>	Output voltage	-0.3	6	V
$V_{BIAS}$	Bias voltage	-0.3	6	V
V <sub>ON</sub>	On voltage	-0.3	6	V
I <sub>MAX</sub>	Maximum continuous switch current		6	Α
I <sub>PLS</sub>	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		8	Α
$T_{J}$	Maximum junction temperature		125	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### 7.2 ESD Ratings

			VALUE	UNIT
V Florensets discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V	
V(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

#### 7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{IN}$	Input voltage		0.8	$V_{BIAS}$	V
$V_{BIAS}$	Bias voltage		2.5	5.7	V
$V_{ON}$	ON voltage		0	5.7	V
V <sub>OUT</sub>	Output voltage			$V_{IN}$	V
$V_{IH}$	High-level input voltage, ON	$V_{BIAS} = 2.5 \text{ V to } 5.7 \text{ V}$	1.1	5.7	V
$V_{IL}$	Low-level input voltage, ON	$V_{BIAS} = 2.5 \text{ V to } 5.7 \text{ V}$	0	0.5	V
C <sub>IN</sub>	Input capacitor		1 <sup>(1)</sup>		μF
$T_A$	Operating free-air temperature	2)	-40	105	°C

<sup>(1)</sup> See the Application Information section.

<sup>(2)</sup> All voltage values are with respect to network ground pin.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

<sup>(2)</sup> In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T<sub>A(max)</sub>] is dependent on the maximum operating junction temperature [T<sub>J(max)</sub>], the maximum power dissipation of the device in the application [P<sub>D(max)</sub>], and the junction-to-ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the equation: T<sub>A (max)</sub> = T<sub>J(max)</sub> - (θ<sub>JA</sub> × P<sub>D(max)</sub>)



#### 7.4 Thermal Information

		TPS22965x	
	THERMAL METRIC <sup>(1)</sup>		UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	°C/W
ΨЈТ	Junction-to-top characterization parameter	3.3	°C/W
ΨЈВ	Junction-to-board characterization parameter	42.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.2	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

# 7.5 Electrical Characteristics—V<sub>BIAS</sub> = 5 V

Unless otherwise noted, the specification in the following table applies where  $V_{BIAS} = 5 \text{ V}$ . Typical values are for  $T_A = 25 \text{ °C}$ .

	PARAMETER	TEST CON	IDITIONS	T <sub>A</sub>	MIN TYP	MAX	UNIT
POWER SI	UPPLIES AND CURRENTS	"					
I <sub>Q</sub> V <sub>VBIAS</sub>	V <sub>BIAS</sub> quiescent current	$I_{OUT} = 0 \text{ mA},$ $V_{IN} = V_{ON} = V_{BIAS} = 5 \text{ N}$	V	-40°C to +105°C	50	75	μΑ
$I_{SD} V_{BIAS}$	V <sub>BIAS</sub> shutdown current	$V_{ON} = GND, V_{OUT} = 0$	V	-40°C to +105°C		2	μA
			V <sub>IN</sub> = 5 V	-40°C to +105°C	0.005	5	
1 1/	V <sub>IN</sub> off-state supply current	V <sub>ON</sub> = GND,	$V_{IN} = 3.3 \ V$	-40°C to +105°C	0.002	3	
$I_{SD} V_{IN}$	V <sub>IN</sub> oil-state supply current	$V_{OUT} = 0 V$	V <sub>IN</sub> = 1.8 V	-40°C to +105°C	0.002	2	μΑ
			V <sub>IN</sub> = 0.8 V	-40°C to +105°C	0.001	1	
I <sub>ON</sub>	ON pin input leakage current	V <sub>ON</sub> = 5.5 V		-40°C to +105°C		0.5	μΑ
RESISTAN	CE CHARACTERISTICS						
				25°C	16	21	
			$V_{IN} = 5 V$	-40°C to +85°C		23	mΩ
				-40°C to +105°C		25	
				25°C	16	21	mΩ
			$V_{IN} = 3.3 \text{ V}$	-40°C to +85°C		23	
				-40°C to +105°C		25	
				25°C	16	21	mΩ
			V <sub>IN</sub> = 1.8 V	-40°C to +85°C		23	
Б.	011	$I_{OUT} = -200 \text{ mA},$		-40°C to +105°C		25	
R <sub>ON</sub>	ON-state resistance	V <sub>BIAS</sub> = 5 V		25°C	16	21	
			V <sub>IN</sub> = 1.5 V	-40°C to +85°C		23	$m\Omega$
				-40°C to +105°C		25	
				25°C	16	21	-
			V <sub>IN</sub> = 1.2 V	-40°C to +85°C		23	mΩ
				-40°C to +105°C		25	1
				25°C	16	21	
			V <sub>IN</sub> = 0.8 V	-40°C to +85°C		23	mΩ
				-40°C to +105°C		25	
R <sub>PD</sub> <sup>(1)</sup>	Output pulldown resistance	V <sub>IN</sub> = 5 V, V <sub>ON</sub> = 0 V, I <sub>O</sub>	OUT = 15 mA	-40°C to +105°C	225	300	Ω

(1) TPS22965 only



# 7.6 Electrical Characteristics— $V_{BIAS} = 2.5 \text{ V}$

Unless otherwise noted, the specification in the following table applies where  $V_{BIAS} = 2.5 \text{ V}$ . Typical values are for  $T_A = 25 \text{ °C}$ .

	PARAMETER	TEST CONDITIONS		T <sub>A</sub>	MIN	TYP	MAX	UNIT
POWER SI	JPPLIES AND CURRENTS							
I <sub>Q</sub> V <sub>VBIAS</sub>	V <sub>BIAS</sub> quiescent current	$I_{OUT} = 0 \text{ mA},$ $V_{IN} = V_{ON} = V_{BIAS} = 2.$	5 V	-40°C to +105°C		20	30	μA
I <sub>SD</sub> V <sub>BIAS</sub>	V <sub>BIAS</sub> shutdown current	$V_{ON} = GND, V_{OUT} = 0$	V	-40°C to +105°C			2	μA
			V <sub>IN</sub> = 2.5 V	-40°C to +105°C		0.005	3	
1 1/	V <sub>IN</sub> off-state supply current	$V_{ON} = GND,$	$V_{IN} = 1.8 \text{ V}$	-40°C to +105°C		0.002	2	
$I_{SD} V_{IN}$	V <sub>IN</sub> on-state supply current	$V_{OUT} = 0 V$	V <sub>IN</sub> = 1.2 V	-40°C to +105°C		0.002	2	μA
			$V_{IN} = 0.8 \text{ V}$	-40°C to +105°C		0.001	1	
I <sub>ON</sub>	ON pin input leakage current	V <sub>ON</sub> = 5.5 V		-40°C to +105°C			0.5	μΑ
RESISTAN	CE CHARACTERISTICS							
				25°C		20	24	
			V <sub>IN</sub> = 2.5 V	-40°C to +85°C			27	mΩ
				-40°C to +105°C			28	
			V <sub>IN</sub> = 1.8 V	25°C		19	23	mΩ
				-40°C to +85°C			26	
				-40°C to +105°C			28	
			V <sub>IN</sub> = 1.5 V	25°C		18	23	
R <sub>ON</sub>	ON-state resistance	$I_{OUT} = -200 \text{ mA},$ $V_{BIAS} = 2.5 \text{ V}$		-40°C to +85°C			25	
		V BIAS — 2.0 V		-40°C to +105°C			27	
				25°C	0	18	23	
			$V_{IN} = 1.2 \text{ V}$	-40°C to +85°C			25	mΩ
				-40°C to +105°C			27	
				25°C		17	22	
			$V_{IN} = 0.8 \text{ V}$	-40°C to +85°C			25	mΩ
				-40°C to +105°C			27	
R <sub>PD</sub> <sup>(1)</sup>	Output pulldown resistance	$V_{IN} = 2.5 \text{ V}, V_{ON} = 0 \text{ V}$	, I <sub>OUT</sub> = 1 mA	-40°C to +105°C		275	325	Ω

<sup>(1)</sup> TPS22965 only

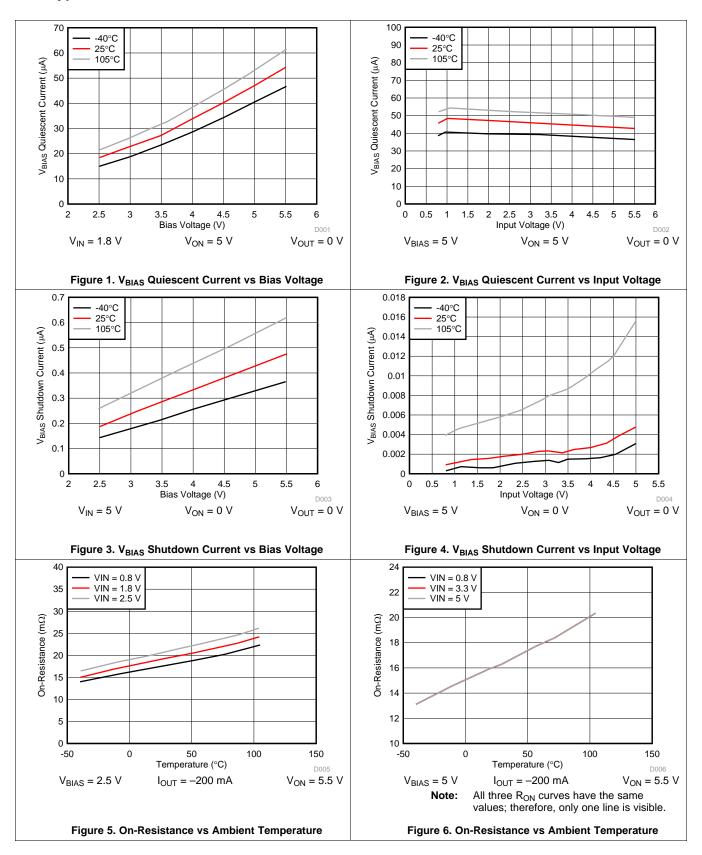


# 7.7 Switching Characteristics

	PARAMETER	TEST CONDITION	MIN TYP	MAX UNIT
V <sub>IN</sub> = \	V <sub>ON</sub> = V <sub>BIAS</sub> = 5 V, T <sub>A</sub> = 2	5ºC (unless otherwise noted)		
t <sub>ON</sub>	Turnon time	$R_L = 10 \Omega$ , $C_L = 0.1 \mu F$ , $C_T = 1000 pF$	1600	
t <sub>OFF</sub>	Turnoff time	$R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ C_T = 1000 \ pF$	9	
t <sub>R</sub>	V <sub>OUT</sub> rise time	$R_L = 10 \Omega$ , $C_L = 0.1 \mu F$ , $C_T = 1000 pF$	1985	μs
t <sub>F</sub>	V <sub>OUT</sub> fall time	$R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ C_T = 1000 \ pF$	3	
$t_D$	ON delay time	$R_L = 10 \Omega$ , $C_L = 0.1 \mu F$ , $C_T = 1000 pF$	660	
$V_{IN} = 0$	$0.8 \text{ V}, \text{ V}_{ON} = \text{V}_{BIAS} = 5 \text{ V},$	T <sub>A</sub> = 25°C (unless otherwise noted)	•	*
t <sub>ON</sub>	Turnon time	$R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ C_T = 1000 \ pF$	730	
t <sub>OFF</sub>	Turnoff time	$R_L = 10 \Omega$ , $C_L = 0.1 \mu F$ , $C_T = 1000 pF$	100	
$t_R$	V <sub>OUT</sub> rise time	$R_L = 10 \Omega$ , $C_L = 0.1 \mu F$ , $C_T = 1000 pF$	380	μs
t <sub>F</sub>	V <sub>OUT</sub> fall time	$R_L = 10 \Omega$ , $C_L = 0.1 \mu F$ , $C_T = 1000 pF$	8	
$t_D$	ON delay time	$R_L = 10~\Omega,~C_L = 0.1~\mu F,~C_T = 1000~pF$	560	
V <sub>IN</sub> = 2	2.5 V, V <sub>ON</sub> = 5 V, V <sub>BIAS</sub> =	2.5 V, T <sub>A</sub> = 25°C (unless otherwise noted)		
$t_{ON}$	Turnon time	$R_L = 10 \Omega$ , $C_L = 0.1 \mu F$ , $C_T = 1000 pF$	2435	
t <sub>OFF</sub>	Turnoff time	$R_L = 10 \Omega$ , $C_L = 0.1 \mu F$ , $C_T = 1000 pF$	9	
$t_R$	V <sub>OUT</sub> rise time	$R_L = 10 \Omega$ , $C_L = 0.1 \mu F$ , $C_T = 1000 pF$	2515	μs
t <sub>F</sub>	V <sub>OUT</sub> fall time	$R_L = 10 \Omega$ , $C_L = 0.1 \mu F$ , $C_T = 1000 pF$	4	
$t_D$	ON delay time	$R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ C_T = 1000 \ pF$	1230	
$V_{IN} = 0$	0.8 V, $V_{ON} = 5$ V, $V_{BIAS} =$	2.5 V, T <sub>A</sub> = 25°C (unless otherwise noted)		
t <sub>ON</sub>	Turnon time	$R_L$ = 10 $\Omega$ , $C_L$ = 0.1 $\mu$ F, $C_T$ = 1000 $p$ F	1565	
t <sub>OFF</sub>	Turnoff time	$R_L$ = 10 $\Omega$ , $C_L$ = 0.1 $\mu$ F, $C_T$ = 1000 $p$ F	70	
t <sub>R</sub>	V <sub>OUT</sub> rise time	$R_L$ = 10 $\Omega$ , $C_L$ = 0.1 $\mu$ F, $C_T$ = 1000 $p$ F	930	μs
t <sub>F</sub>	V <sub>OUT</sub> fall time	$R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F, \ C_T = 1000 \ pF$	8	
$t_D$	ON delay time	$R_L = 10 \Omega$ , $C_L = 0.1 \mu F$ , $C_T = 1000 pF$	1110	



# 7.8 Typical DC Characteristics

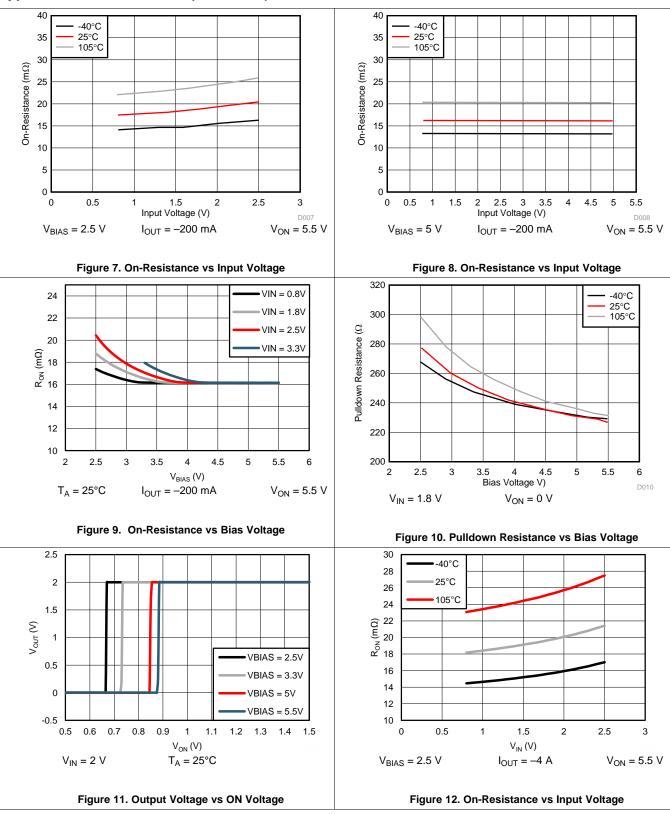


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# **Typical DC Characteristics (continued)**

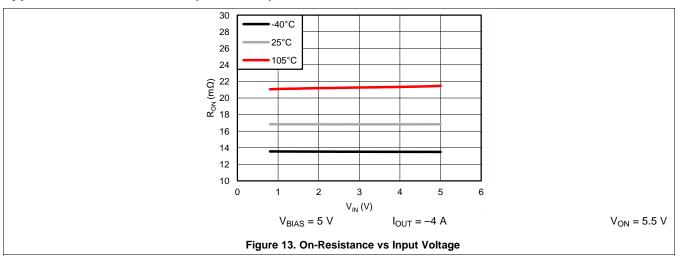


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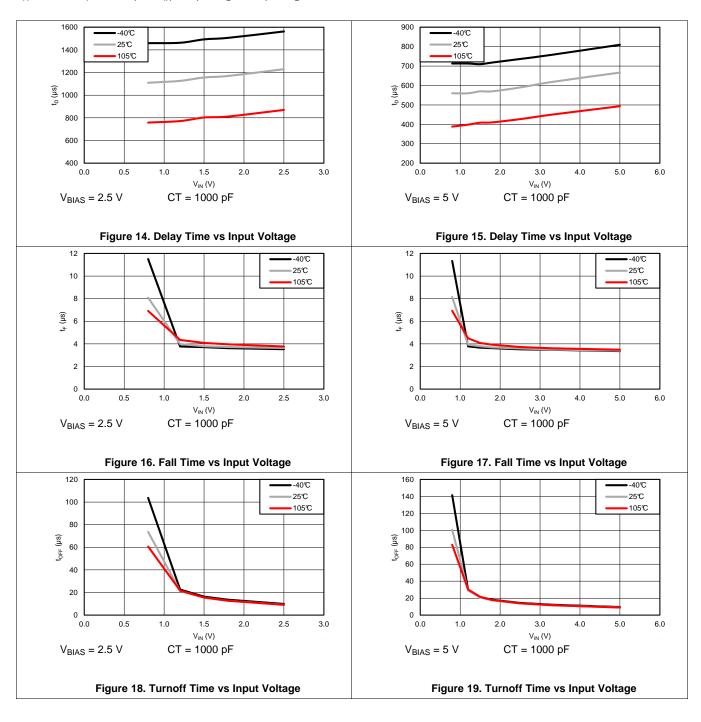
# **Typical DC Characteristics (continued)**



# TEXAS INSTRUMENTS

# 7.9 Typical Switching Characteristics

 $T_A$  = 25°C,  $C_T$  = 1000 pF,  $C_{IN}$  = 1  $\mu F,~C_L$  = 0.1  $\mu F,~R_L$  = 10  $\Omega$ 

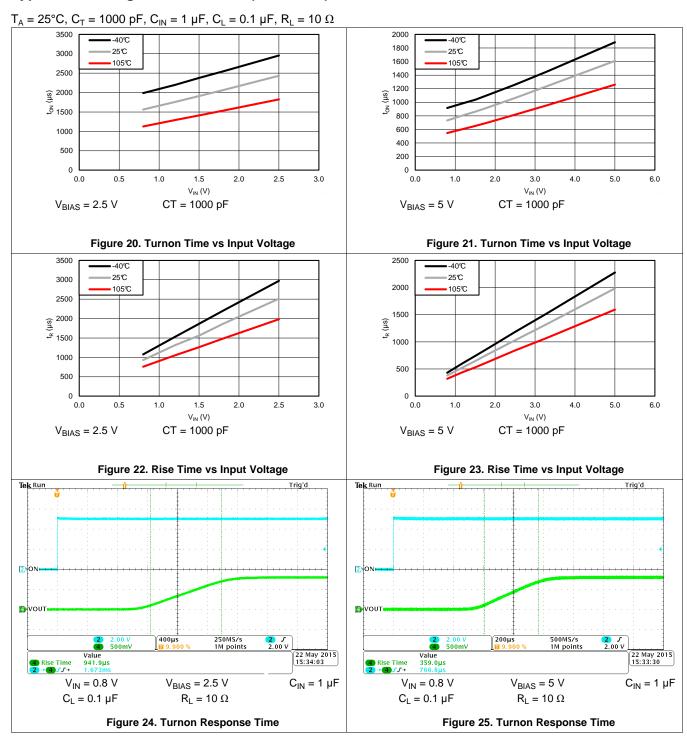


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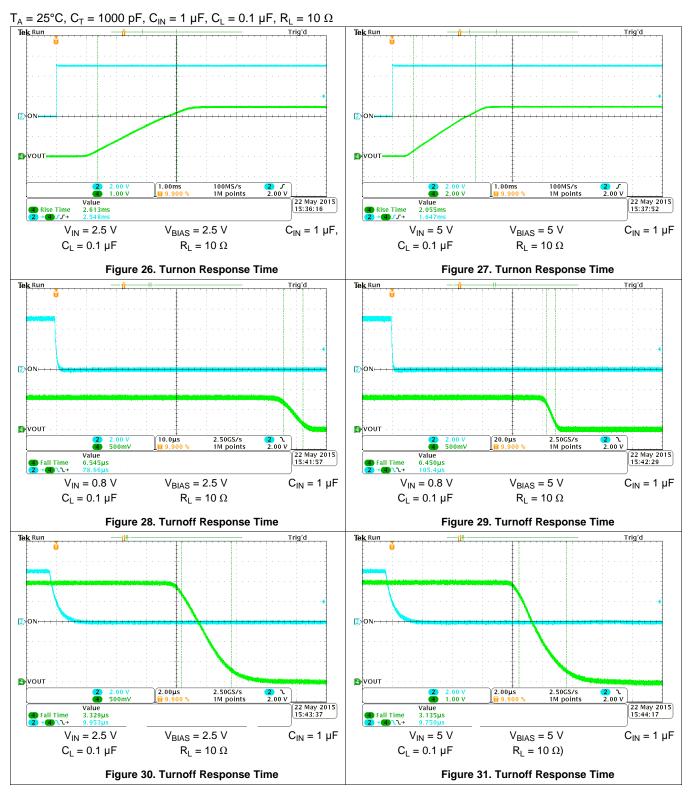


# **Typical Switching Characteristics (continued)**



# TEXAS INSTRUMENTS

# Typical Switching Characteristics (continued)

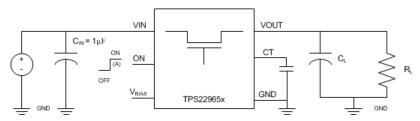


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# 8 Parameter Measurement Information



A. Rise and fall times of the control signal is 100 ns.

Figure 32. Test Circuit

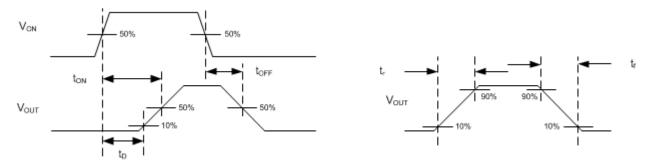


Figure 33.  $\,t_{\text{ON}}$  and  $t_{\text{OFF}}$  Waveforms



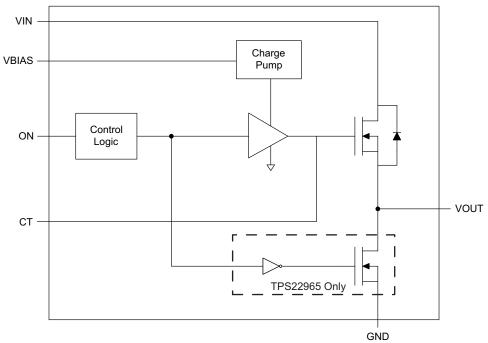
#### 9 Detailed Description

#### 9.1 Overview

The TPS22965x device is a single channel, 6-A load switch in an 8-pin SON package. To reduce the voltage drop in high current rails, the device implements an ultra-low resistance N-channel MOSFET. The device has a programmable slew rate for applications that require specific rise-time.

The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

#### 9.2 Functional Block Diagram



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#### 9.3 Feature Description

#### 9.3.1 Adjustable Rise Time

A capacitor to GND on the CT pin sets the slew rate. The voltage on the CT pin can be as high as 12 V; therefore, the minimum voltage rating for the CT capacitor must be 25 V for optimal performance. An approximate formula for the relationship between CT and slew rate when  $V_{BIAS}$  is set to 5 V is shown in Equation 1. This equation accounts for 10% to 90% measurement on  $V_{OUT}$  and does **NOT** apply for CT = 0 pF. Use Table 1 to determine rise times for when CT = 0 pF.

$$SR = 0.38 \times CT + 34$$

where

- SR is the slew rate (in µs/V)
- CT is the the capacitance value on the CT pin (in pF)
- The units for the constant 34 are  $\mu$ s/V. The units for the constant 0.38 are  $\mu$ s/(V × pF). (1)

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device. Rise times shown in Table 1 are only valid for the power-up sequence where  $V_{IN}$  and  $V_{BIAS}$  are already in steady state condition before the ON pin is asserted high.

				о . сыр									
OT (F)	TYPICAL VALUES at 25°C with a 25 V X7R 10% CERAMIC CAPACITOR on CT <sup>(1)</sup>												
CT (pF)	VIN = 5 V	VIN = 3.3 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 1.05 V	VIN = 0.8 V						
0	180	136	94	84	74	70	60						
220	547	378	232	202	173	157	129						
470	962	654	386	333	282	252	206						
1000	1983	1330	765	647	533	476	382						
2200	4013	2693	1537	1310	1077	959	766						
4700	8207	5490	3137	2693	2200	1970	1590						
10000	17700	11767	6697	5683	4657	4151	3350						

Table 1. Rise Time vs CT Capacitor

#### 9.3.2 Quick Output Discharge (QOD) (Optional)

The TPS22965 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 225  $\Omega$  and prevents the output from floating while the switch is disabled.

#### 9.3.3 Low Power Consumption During Off State

The  $I_{SD}$   $V_{IN}$  supply current is 0.01  $\mu A$  typical at 1.8 VIN. Typically, the downstream loads must have a significantly higher off-state leakage current. The load switch allows system standby power consumption to be reduced.

#### 9.4 Device Functional Modes

The Table 2 lists the VOUT pin states as determined by the ON pin.

**Table 2. VOUT Connection** 

ON	TPS22965	TPS22965N
L	GND	Open
Н	VIN	VIN

<sup>(1)</sup> Rise time ( $\mu$ s) 10% - 90%,  $C_L$  = 0.1  $\mu$ F,  $C_{IN}$  = 1  $\mu$ F,  $R_L$  = 10  $\Omega$ ,  $V_{BIAS}$  = 5 V



# 10 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 10.1 Application Information

#### 10.1.1 ON and OFF Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

#### 10.1.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1- $\mu$ F ceramic capacitor,  $C_{IN}$ , placed close to the pins, is usually sufficient. Higher values of  $C_{IN}$  can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

#### 10.1.3 Output Capacitor (Optional)

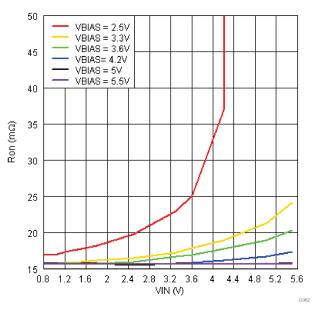
Becuase of the integrated body diode in the NMOS switch, a  $C_{IN}$  greater than  $C_{L}$  is highly recommended. A  $C_{L}$  greater than  $C_{IN}$  can cause  $V_{OUT}$  to exceed  $V_{IN}$  when the system supply is removed. This could result in current flow through the body diode from  $V_{OUT}$  to  $V_{IN}$ . A  $C_{IN}$  to  $C_{L}$  ratio of 10 to 1 is recommended for minimizing  $V_{IN}$  dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more  $V_{IN}$  dip upon turn-on due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see the *Adjustable Rise Time* section).

#### 10.1.4 V<sub>IN</sub> and V<sub>BIAS</sub> Voltage Range

For optimal  $R_{ON}$  performance, make sure  $V_{IN} \le V_{BIAS}$ . The device is still functional if  $V_{IN} > V_{BIAS}$  but it exhibits  $R_{ON}$  greater than what is listed in the *Electrical Characteristics—V\_{BIAS} = 5 V* table. See Figure 34 for an example of a typical device. Notice the increasing  $R_{ON}$  as  $V_{IN}$  exceeds  $V_{BIAS}$  voltage. Never exceed the maximum voltage rating for  $V_{IN}$  and  $V_{BIAS}$ .



# **Application Information (continued)**



 $T_A = 25 \, ^{\circ}C$ 

 $I_{OUT} = -200 \text{ mA}$ 

Figure 34. R<sub>ON</sub> vs V<sub>IN</sub>

# 10.2 Typical Application

This application demonstrates how the TPS22965x can be used to power downstream modules.

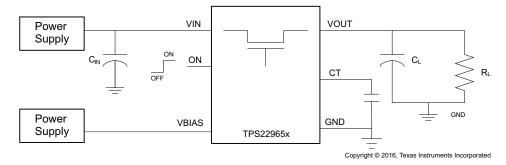


Figure 35. Powering a Downstream Module

#### 10.2.1 Design Requirements

Table 3 shows the design parameters.

**Table 3. Design Parameters** 

DESIGN PARAMETER	EXAMPLE VALUE
V <sub>IN</sub>	3.3 V
V <sub>BIAS</sub>	5 V
C <sub>L</sub>	22 μF
Maximum Acceptable Inrush Current	400 mA



#### 10.2.2 Detailed Design Procedure

#### 10.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 2.

Inrush Current =  $C \times dV/dt$ 

#### where

- · C is the output capacitance
- dV is the output voltage
- dt is the rise time (2)

The TPS22965x offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turn-on. The appropriate rise time can be calculated using the design requirements and the inrush current equation. See Equation 3 and Equation 4.

$$400 \text{ mA} = 22 \mu\text{F} \times 3.3 \text{ V/dt}$$
 (3)

$$dt = 181.5 \,\mu s$$
 (4)

To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 181.5 µs. See the oscilloscope captures in the *Application Curves* section for an example of how the CT capacitor can be used to reduce inrush current.

#### 10.2.2.2 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation,  $P_{D(max)}$  for a given output current and ambient temperature, use Equation 5 as a guideline:

$$P_{\text{D(max)}} = \frac{T_{\text{J(max)}} - T_{\text{A}}}{\theta_{\text{JA}}}$$

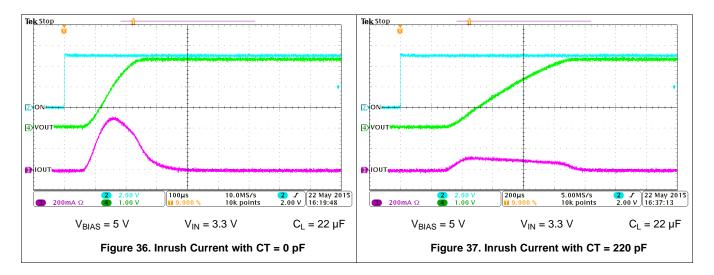
#### where

- P<sub>D(max)</sub> is the maximum allowable power dissipation
- T<sub>J(max)</sub> is the maximum allowable junction temperature (125°C for the TPS22965x)
- T<sub>A</sub> is the ambient temperature of the device
- Θ<sub>JA</sub> = junction to air thermal impedance. See the *Thermal Information* table. This parameter is highly dependent upon board layout.

See Figure 38, notice that the thermal vias are located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.



#### 10.2.3 Application Curves



# 11 Power Supply Recommendations

The device is designed to operate from a VBIAS range of 2.5 V to 5.7 V and a VIN range of 0.8 V to VBIAS.



# 12 Layout

# 12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace must be as short as possible to avoid parasitic capacitance.

# 12.2 Layout Example

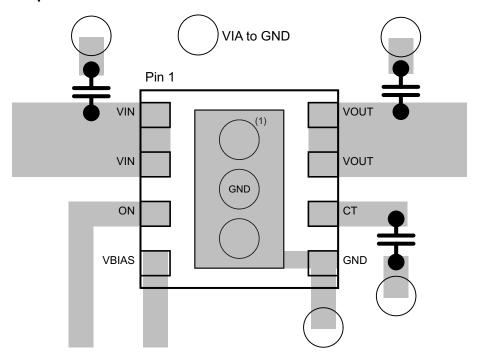


Figure 38. Layout Recommendation



# 13 Device and Documentation Support

#### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation see the following:

- Managing Inrush Current
- TPS22965EVM-023 Single 6A Load Switch
- Load Switch Thermal Considerations
- TPS22965NEVM User's Guide
- TPS22965WDSGQ1EVM User's Guide

#### 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 13.4 Trademarks

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#### 13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 13.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TPS22965DSGR	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZSA0
TPS22965DSGR.A	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZSA0
TPS22965DSGRG4	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZSA0
TPS22965DSGRG4.A	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZSA0
TPS22965DSGT	Active	Production	WSON (DSG)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZSA0
TPS22965DSGT.A	Active	Production	WSON (DSG)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZSA0
TPS22965NDSGR	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZDVI
TPS22965NDSGR.A	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZDVI
TPS22965NDSGRG4	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZDVI
TPS22965NDSGRG4.A	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZDVI

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF TPS22965:

Automotive: TPS22965-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# **PACKAGE MATERIALS INFORMATION**

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#### TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22965DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965NDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965NDSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2



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#### \*All dimensions are nominal

7 III GIII I GII I GI GI GI GI GI GI GI G							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22965DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22965DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22965DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS22965NDSGR	WSON	DSG	8	3000	182.0	182.0	20.0
TPS22965NDSGRG4	WSON	DSG	8	3000	182.0	182.0	20.0

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC SMALL OUTLINE - NO LEAD



#### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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