











TPS22925

SLVS840D - NOVEMBER 2015 - REVISED AUGUST 2016

TPS22925 3.6-V, 3-A, 9-m Ω On-Resistance Load Switch

Features

- Input Voltage Range: 0.65 V to 3.6 V
- On-Resistance
 - R_{ON} = 9.2 mΩ at V_{IN} = 3.6 V
 - R_{ON} = 9.2 mΩ at V_{IN} = 1.8 V
 - R_{ON} = 10.2 m Ω at V_{IN} = 1 V
 - R_{ON} = 13.1 mΩ at V_{IN} = 0.65 V
- 3-A Maximum Continuous Switch Current
- Quiescent Current, $I_{Q,VIN} = 29 \mu A$ at $V_{IN} = 3.6 \text{ V}$
- Low Control Input Threshold Enables 1.5-, 1.8-, 2.5-, or 3.3-V Logic
- Controlled Slew Rate
 - t_R = 97 µs at V_{IN} = 3.6 V (TPS22925Bx)
 - t_R = 810 µs at V_{IN} = 3.6 V (TPS22925Cx)
- Reverse Current Blocking (When Disabled)
- Quick Output Discharge (QOD) (TPS22925B and TPS22925C only)
- Wafer Chip Scale Package:
 - 0.9 mm x 1.4 mm, 0.5-mm Pitch, 0.4-mm
- ESD Performance Tested per JESD 22
 - 2-kV HBM and 1-kV CDM

Applications

- Computing
- SSD
- **Tablets**
- Wearables
- **EPOS**

3 Description

The TPS22925 product family consists of four devices: TPS22925B, TPS22925BN, TPS22925C, and TPS22925CN. Each device is a 9-m Ω , singlechannel load switch with a controlled slew rate.

The devices contain an N-channel MOSFET that can operate over an input voltage range of 0.65 V to 3.6 V and can support a maximum continuous current of 3 A. This continuous current enables the devices to be used across multiple designs and end equipments. Each of the TPS22925 devices provides reverse current blocking when disabled allowing for power supply protection and power multiplexing capabilities.

The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. When operating with an input voltage of 3.6 V, the TPS22925Bx devices feature a 97 μs rise time and the TPS22925Cx devices feature an 810 µs rise time.

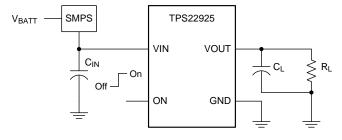
The TPS22925 family of devices can help reduce the total solution size by offering an optional integrated, 150- Ω pull-down resistor for quick output discharge (QOD) when the switch is turned off. Each of the TPS22925 devices is available in a 0.9 mm x 1.4 mm, 0.5-mm pitch, 0.4-mm height 6-pin wafer chip scale package (WCSP) allowing for smaller, more integrated designs. The WCSP and 9 m Ω of onresistance allow use in space constrained, battery powered applications. The device is characterized for operation over the free-air temperature range of -40°C to +105°C.

Device Information⁽¹⁾

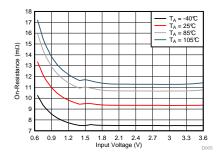
PART NUMBER	PACKAGE	BODY SIZE (NOM)		
TPS22925B	D0D0 ((0)	0.00 4.40		
TPS22925BN				
TPS22925C	DSBGA (6)	0.90 mm × 1.40 mm		
TPS22925CN				

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application



On-Resistance vs Input Voltage



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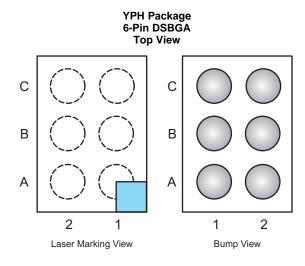
Changes from Original (November 2015) to Revision A



5 Device Comparison Table

DEVICE	QOD	R_{ON} (m Ω) at $V_{IN} = 3.6 \text{ V}$	t _R (μs) at V _{IN} = 3.6 V	MAXIMUM OUTPUT CURRENT I _{MAX} (A)	ENABLE (ON PIN)
TPS22925B	Yes		97		
TPS22925BN	No	0.2	97	2	A ativa I liab
TPS22925C	Yes	9.2		3	Active High
TPS22925CN	22925CN No 810				

6 Pin Configuration and Functions



Pin Assignments

	3						
С	GND	ON					
В	VOUT	VIN					
Α	VOUT	VIN					
	1	2					

Pin Functions

PIN		TYPE	DESCRIPTION		
NAME	NO.	ITPE	DESCRIPTION		
GND	C1	GND	Ground		
ON	C2	1	Switch control input. Active high. Do not leave floating.		
VIN	A2	1	Switch input; bypass this input with a ceramic capacitor to ground. See the <i>Application</i>		
VIIN	B2	1	Information section for more detail.		
VOLIT	A1	0	Switch output		
VOUT	B1	0	Switch output		



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VIN, ON	Input voltage	-0.3	4	V
VOUT	Output voltage	-0.3	4	V
I _{MAX}	Maximum continuous switch current at T _A = 60°C		3	Α
I _{PLS}	Maximum pulsed switch current, 100-μs pulse, 2% duty cycle		4	Α
TJ	Junction temperature		125	°C
T _{stg}	Storage temperature	-65	150	°C

⁽¹⁾ Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute—maximum—rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
\/		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	\/
۱) ۷	Electrostatic discharge	Charged–device model (CDM), per JEDEC specification JESD22–C101 (2)	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500–V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500–V HBM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	0.65	3.6	V
V _{OUT}	Output voltage	0	3.6	V
V_{IH}	High-level input voltage, ON	0.9	3.6	V
V_{IL}	Low-level input voltage, ON	0	0.45	V
C _{IN}	Input capacitance	1		μF
T _A	Operating free-air temperature	-40	105	°C

7.4 Thermal Information

	THERMAL METRIC ⁽¹⁾	TPS22925xx YPH (DSBGA)	UNIT
		6 PINS	_
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	0.8	°C/W
ΨЈВ	Junction-to-board characterization parameter	30.4	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

⁽²⁾ JEDEC document JEP157 states that 250–V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250–V CDM is possible with the necessary precautions.



7.5 Electrical Characteristics

over operating free–air temperature range (unless otherwise noted). Typical values are for $T_A = 25$ °C.

P	PARAMETER	TEST CO	NDITIONS	T _A	MIN TYP	MAX	UNIT
			V - 26 V	-40°C to +85°C	29	71	
			$V_{IN} = 3.6 \text{ V}$	-40°C to +105°C		84	
			V 25V	-40°C to +85°C	28	67	
			$V_{IN} = 2.5 \text{ V}$	-40°C to +105°C		79	
			V 40V	-40°C to +85°C	26	65	
	0	V _{ON} = 3.6 V,	$V_{IN} = 1.8 \text{ V}$	-40°C to +105°C		76	
$I_{Q,VIN}$	Quiescent current	$I_{OUT} = 0 A$		-40°C to +85°C	20	55	μA
			V _{IN} = 1.2 V	-40°C to +105°C		66	
			., .,,	-40°C to +85°C	16	50	
			$V_{IN} = 1 V$	-40°C to +105°C		60	
			V 0.05.V	-40°C to +85°C	10	39	
			$V_{IN} = 0.65 \text{ V}$	-40°C to +105°C		49	
			V 00V	-40°C to +85°C	0.5	5	
			$V_{IN} = 3.6 \text{ V}$	-40°C to +105°C		9	
			V 0.5.V	-40°C to +85°C	0.5	4	
			$V_{IN} = 2.5 \text{ V}$	-40°C to +105°C		6	
			V 40V	-40°C to +85°C	0.5	4	
	VIN shutdown	$V_{ON} = 0 V$	$V_{IN} = 1.8 \text{ V}$	-40°C to +105°C		6	
SD,VIN	current	V _{OUT} = 0 V	.,	-40°C to +85°C	0.5	3	μΑ
			$V_{IN} = 1.2 \text{ V}$	-40°C to +105°C		5	
			V _{IN} = 1 V	-40°C to +85°C	0.5	3	
				-40°C to +105°C		5	
			V _{IN} = 0.65 V	-40°C to +85°C	0.5	3	
				-40°C to +105°C		5	
ON	ON pin input leakage current	0.9 V ≤ V _{ON} ≤ 3.6	V	-40°C to +105°C		0.1	μΑ
	Reverse current	\\ \\\ \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\		-40°C to +85°C	-0.2	-2.5	μА
RC,VIN	when disabled	$V_{IN} = V_{ON} = 0 V, V$	V _{OUT} = 3.6 V	-40°C to +105°C		-6	
			V _{IN} = 3.6 V	25°C	9.2	13	
				-40°C to +85°C		15	
				-40°C to +105°C		16	
				25°C	9.2	13	
			V _{IN} = 2.5 V	-40°C to +85°C		15	
				-40°C to +105°C		16	
				25°C	9.2	13	
			V _{IN} = 1.8 V	-40°C to +85°C		15	
	0			-40°C to +105°C		16	
R _{ON}	On-resistance	$I_{OUT} = -200 \text{ mA}$		25°C	9.5	14	mΩ
			V _{IN} = 1.2 V	-40°C to +85°C		16	
				-40°C to +105°C		17	
				25°C	10.2	15	
			V _{IN} = 1 V	-40°C to +85°C		17	-
				-40°C to +105°C		18	
				25°C	13.1	20	
			V _{IN} = 0.65 V	-40°C to +85°C		23	
			V IN - 0.00 V	-40°C to +105°C		25	

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Electrical Characteristics (continued)

over operating free–air temperature range (unless otherwise noted). Typical values are for $T_A = 25$ °C.

	PARAMETER	TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
V _{HYS}		$V_{IN} = 3.6 \text{ V}$			86		mV
		$V_{IN} = 2.5 \text{ V}$	25°C		83		
	ON pin hysteresis	$V_{IN} = 1.8 \ V$			82		
	ON pill hysteresis	V _{IN} = 1.2 V			80		
		$V_{IN} = 1 V$			79		
		V _{IN} = 0.65 V			79		
R _{PD} ⁽¹⁾	Output pull-down	Output pull-down $V_{IN} = V_{OLIT} = 3.6 \text{ V}$	-40°C to +85°C		150	205	0
L'AD(,,)	resistance	Output pull-down resistance $V_{IN} = V_{OUT} = 3.6 \text{ V},$ -40°C to -40°C to				215	Ω

⁽¹⁾ Applies to TPS22925B and TPS22925C only.

7.6 Switching Characteristics⁽¹⁾

over operating free-air temperature range (unless otherwise noted) V_{ON} = 3.6 V, R_L = 10 Ω , C_{IN} = 1 μF , C_L = 0.1 μF , T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP (TPS22925Bx)	TYP (TPS22925Cx)	UNIT
		V _{IN} = 3.6 V	110	900	
t _{ON}	Turnon time	V _{IN} = 1.8 V	94	730	μs
		V _{IN} = 0.65 V	86	620	
		V _{IN} = 3.6 V	3	3	
t _{OFF}	Turnoff time	V _{IN} = 1.8 V	2.7	2.7	μs
		V _{IN} = 0.65 V	10.9	10.9	
		V _{IN} = 3.6 V	97	810	
t _R	Output voltage rise time	V _{IN} = 1.8 V	61	520	μs
		V _{IN} = 0.65 V	36	300	
		V _{IN} = 3.6 V	2.2	2.2	
t _F	Output voltage fall time	V _{IN} = 1.8 V	2.1	2.1	μs
		V _{IN} = 0.65 V	3.6	3.6	
		V _{IN} = 3.6 V	64	500	
t _D	Delay time	V _{IN} = 1.8 V	66	490	μs
		V _{IN} = 0.65 V	68	470	

⁽¹⁾ Turn-off time and fall time are dependent on the time constant at the load. For TPS22925BN and TPS22925CN, there is no QOD. The time constant is $R_L \times C_L$. For TPS22925B and TPS22925C, internal pull-down resistor R_{PD} is enabled when the switch is disabled. The time constant is $(R_{PD} \parallel R_L) \times C_L$.



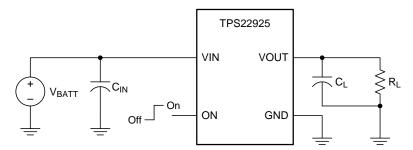
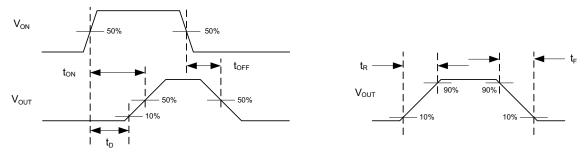


Figure 1. Timing Test Circuit

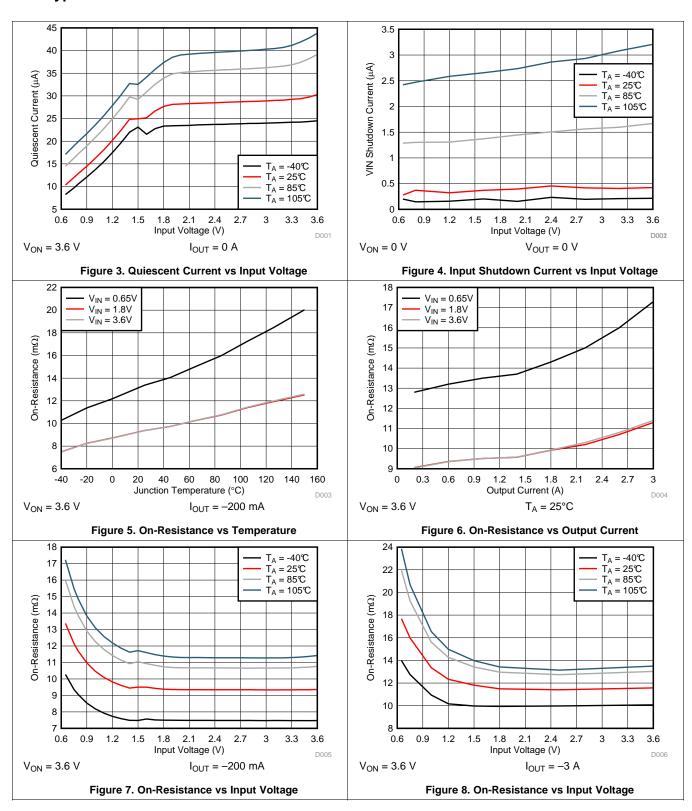


Rise times and fall times of the control signal is 100 ns.

Figure 2. Timing Waveforms

TEXAS INSTRUMENTS

7.7 Typical Characteristics

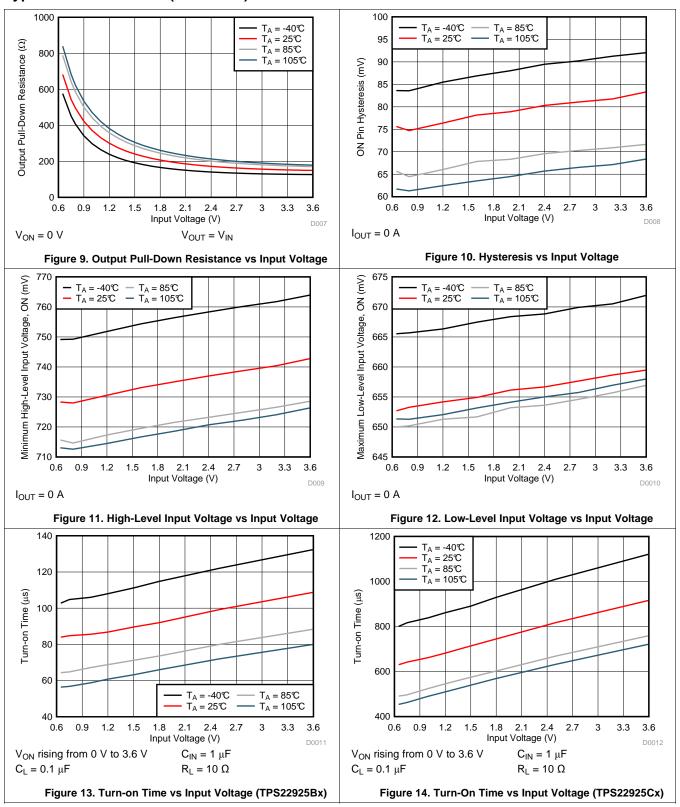


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Typical Characteristics (continued)

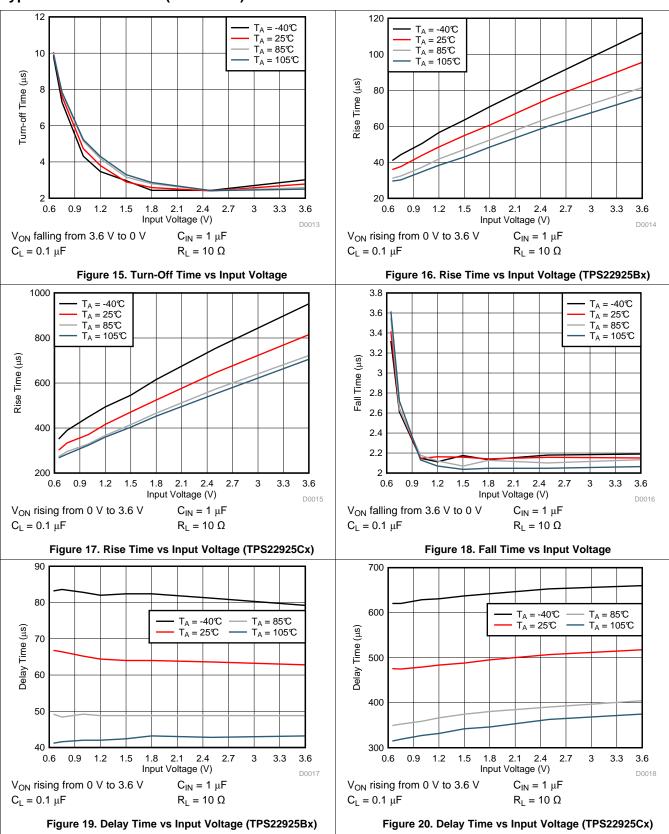


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Typical Characteristics (continued)



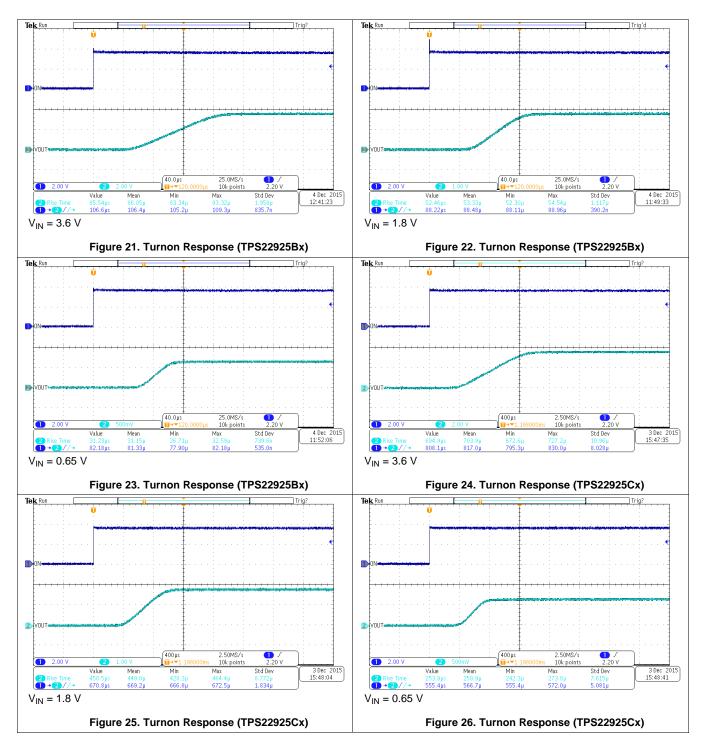
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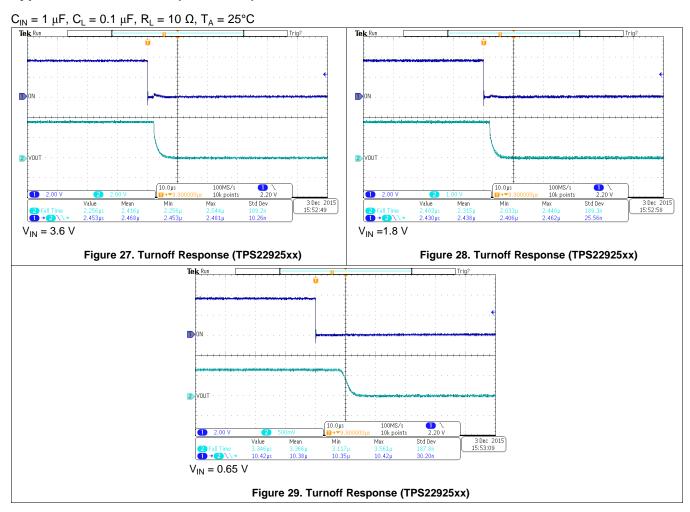
7.8 Typical Characteristics

 C_{IN} = 1 μF , C_{L} = 0.1 μF , R_{L} = 10 Ω , T_{A} = 25°C



TEXAS INSTRUMENTS

Typical Characteristics (continued)



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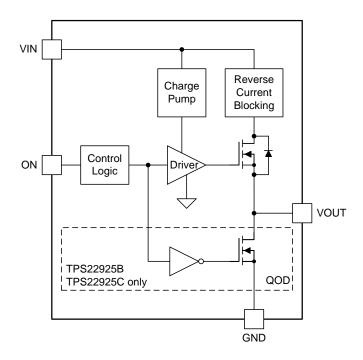


8 Detailed Description

8.1 Overview

The TPS22925 is a single channel, 3-A load switch in a WCSP-6 package. This device implements an N-channel MOSFET with a controlled rise time for applications that need to limit inrush current. The device is also designed to have low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. The TPS22925 provides reverse current blocking when the power switch is disabled. Integrated control logic, driver, and output discharge FET eliminates the need for additional external components, which reduces solution size and bill of material (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ON and OFF Control

The ON pin controls the state of the switch. Asserting the ON pin high enables the switch. The ON pin is compatible with GPIOs of 1.5 V and above.

8.3.2 Quick Output Discharge (QOD) (TPS22925B and TPS22925C Only)

When the switch is disabled, a discharge path is enabled between the output and ground with a typical resistance of 150 Ω . The resistance pulls down the output and prevents it from floating when the device is disabled.



Feature Description (continued)

8.3.3 Reverse Current Blocking

The reverse current blocking feature prevents current flow from the VOUT pin to the VIN pin when the TPS22925 devices are disabled. This feature is particularly useful when the output of the device needs to be driven by another voltage source after TPS22925 is disabled (for example in a power multiplexer application). In order for this feature to work, the TPS22925 must be disabled and either of the following conditions must be met:

- $V_{IN} \ge 0.65 \text{ V or}$
- V_{OUT} ≥ 0.65 V

Figure 30 describes the ideal behavior of reverse current blocking circuit in TPS22925 devices where

- I_{VIN} is the current through the VIN pin
- V_{SRC} is the input voltage applied to the device
- V_{FORCE} is the external voltage source forced at the VOUT pin
- I_{OUT} is the output load current

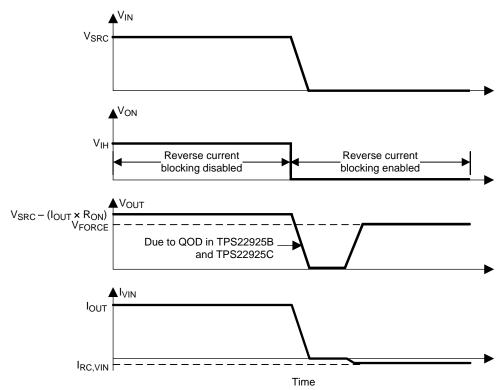


Figure 30. Reverse Current Blocking

After the device is disabled via the ON pin and VOUT is forced to an external voltage (V_{FORCE}), less than 6 μ A of current flows from the VOUT pin to the VIN pin. This limitation prevents any extra current loading on the voltage source supplying the V_{FORCE} voltage.



8.4 Device Functional Modes

Table 1 shows the function table for the TPS22925xx devices.

Table 1. Function Table

ON	VIN to VOUT	OUTPUT DISCHARGE ⁽¹⁾
L	OFF	ENABLED
Н	ON	DISABLED

(1) This feature is in the TPS22925B and TPS22925C only (not in the TPS22925BN and TPS22925CN).

(1)



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS22925 device is a 9-m Ω , single-channel load switch with a controlled slew rate. This design example describes a device containing an N-channel MOSFET that operates at an input voltage range of 3.6 V and supports a maximum continuous current of 3 A. The devices provides reverse current blocking when disabled allowing for power supply protection and power multiplexing capabilities.

9.1.1 VIN to VOUT Voltage Drop

The VIN pin to VOUT pin voltage drop in the device is determined by the R_{ON} of the device and the load current. The on-resistance of the device depends upon the VIN condition of the device. See the on-resistance specification in the *Electrical Characteristics* table. After the on-resistance of the device is determined based upon the input voltage conditions, use Equation 1 to calculate the VIN-to-VOUT voltage drop.

$$\Delta V = I_L \times R_{ON}$$

where

- ΔV is the voltage drop from the VIN pin to the VOUT pin
- I_I is the load current
- R_{ON} is the on-resistance of the device for a specific input voltage
- Choose an appropriate I_L so that the maximum current (I_{MAX}) specification of the device is not violated

9.1.2 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, place a capacitor between VIN and GND close to the pins. A 1- μ F ceramic capacitor, C_{IN}, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

9.1.3 Load Capacitor (C₁)

A C_{IN} to C_L ratio of 10-to-1 is recommended for minimizing the input voltage dip caused by inrush currents during startup.



Application Information (continued)

9.1.4 Standby Power Reduction

Any end equipment that is being powered from the battery has a need to reduce current consumption in order to maintain the battery charge for a longer time. TPS22925 devices help to accomplish this reduction by turning off the supply to the modules that are in standby state and hence significantly reducing the leakage current overhead of the standby modules. See Figure 31.

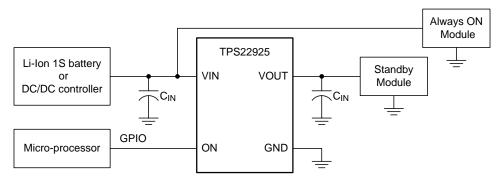


Figure 31. Standby Power Reduction

9.1.5 Power Multiplexing

Figure 32 shows a power multiplexing application using two TPS22925xN devices. Use the non-QOD version in order to maintain the output voltage. Configure the GPIO control from the microprocessor unit as break-before-make (BBM).

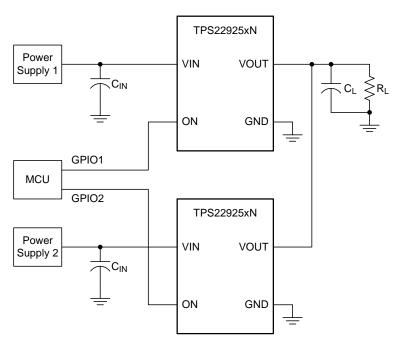


Figure 32. Power Multiplexing with Two TPS22925xN Devices



Application Information (continued)

9.1.6 Thermal Considerations

Restrict the maximum junction temperature lower than 125° C. Use Equation 2 to calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output load current and ambient temperature.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

where

- P_{D(max)} is the maximum allowable power dissipation
- T_{J(max)} is the maximum allowable junction temperature
- T_A is the ambient temperature of the device
- R_{θJA} is the junction-to-air thermal impedance

(2)

NOTE

The $R_{\theta JA}$ parameter is highly dependent upon board layout. (See the *Thermal Information* table)

9.2 Typical Application

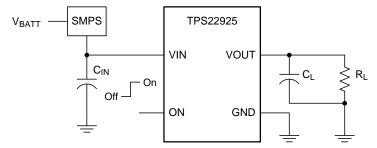


Figure 33. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.6 V
C_L	1 μF
Maximum Acceptable Inrush Current	40 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Managing Inrush Current

When the switch is enabled, the V_{IN} capacitors must be charged up from 0 V to V_{IN} . This charge arrives in the form of inrush current. Calculate the inrush current using Equation 3.

$$I_{INRUSH} = C_L \times \frac{dv}{dt}$$

where

- I_{INRUSH} is the inrush current
- C_L is the load capacitance
- dv/dt is the output slew rate

(3)

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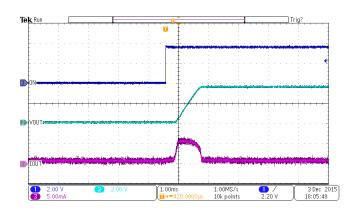


The TPS22925Bx and TPS22925Cx have different controlled rise time. TPS22925Bx has shorter rise time than TPS22925Cx. In the application where fast rise time is required and higher inrush current can be tolerated, consider using the TPS22925Bx. For an application that requires a longer rise time and lower inrush current, consider using the TPS22925Cx. Calculate the maximum acceptable slew rate using the design requirements and Equation 4.

$$\frac{dv}{dt} = \frac{I_{INRUSH}}{C_L} = \frac{40 \text{ mA}}{1.0 \text{ }\mu\text{F}} = 40 \text{ V/ms}$$
(4)

The TPS22925Bx has a typical rise time of 97 μs at 3.6 V. This results in a slew rate of 29.7 V/ms which meets the above design requirements. The TPS22925Cx has a typical rise time of 810 μs at 3.6 V. This results in a slew rate of 3.6 V/ms which also meets the above design requirements. Base on inrush current requirement, either devices can be used.

9.2.3 Application Curve



$$C_L = 1 \mu F$$

Figure 34. Inrush Current (TPS22925C)

10 Power Supply Recommendations

This family of devices is designed to operate with a VIN range of 0.65 V to 3.6 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1 μ F bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 μ F may be sufficient.



11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and load capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

VIA to Power Ground Plane

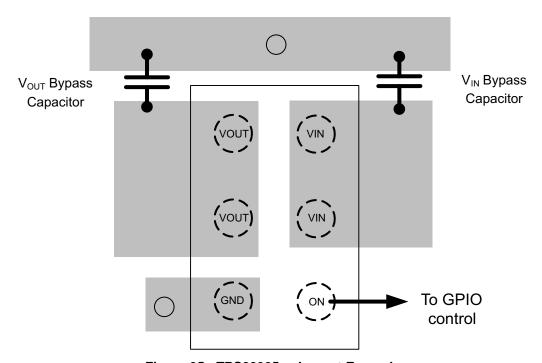


Figure 35. TPS22925xx Layout Example



12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Reverse Current Protection in Load Switches
- Quiescent Current vs Shutdown Current for Load Switch Power Consumption
- TPS22925EVM User's Guide

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — TI Glossarv.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser–based versions of this data sheet, refer to the left–hand navigation.





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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(0)	(4)	(5)		(6)
TPS22925BNYPHR	Active	Production	DSBGA (YPH) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12D9
TPS22925BNYPHR.B	Active	Production	DSBGA (YPH) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12D9
TPS22925BNYPHT	Active	Production	DSBGA (YPH) 6	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12D9
TPS22925BNYPHT.B	Active	Production	DSBGA (YPH) 6	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12D9
TPS22925BYPHR	Active	Production	DSBGA (YPH) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12A8
TPS22925BYPHR.B	Active	Production	DSBGA (YPH) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12A8
TPS22925BYPHT	Active	Production	DSBGA (YPH) 6	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12A8
TPS22925BYPHT.B	Active	Production	DSBGA (YPH) 6	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12A8
TPS22925CNYPHR	Active	Production	DSBGA (YPH) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12C9
TPS22925CNYPHR.B	Active	Production	DSBGA (YPH) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12C9
TPS22925CNYPHT	Active	Production	DSBGA (YPH) 6	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12C9
TPS22925CNYPHT.B	Active	Production	DSBGA (YPH) 6	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12C9
TPS22925CYPHR	Active	Production	DSBGA (YPH) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12B9
TPS22925CYPHR.B	Active	Production	DSBGA (YPH) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12B9
TPS22925CYPHT	Active	Production	DSBGA (YPH) 6	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12B9
TPS22925CYPHT.B	Active	Production	DSBGA (YPH) 6	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	12B9

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22925BNYPHR	DSBGA	YPH	6	3000	180.0	8.4	0.96	1.46	0.42	4.0	8.0	Q1
TPS22925BNYPHT	DSBGA	YPH	6	250	180.0	8.4	0.96	1.46	0.42	4.0	8.0	Q1
TPS22925BYPHR	DSBGA	YPH	6	3000	180.0	8.4	0.96	1.46	0.42	4.0	8.0	Q1
TPS22925BYPHT	DSBGA	YPH	6	250	180.0	8.4	0.96	1.46	0.42	4.0	8.0	Q1
TPS22925CNYPHR	DSBGA	YPH	6	3000	180.0	8.4	0.96	1.46	0.42	4.0	8.0	Q1
TPS22925CNYPHT	DSBGA	YPH	6	250	180.0	8.4	0.96	1.46	0.42	4.0	8.0	Q1
TPS22925CYPHR	DSBGA	YPH	6	3000	180.0	8.4	0.96	1.46	0.42	4.0	8.0	Q1
TPS22925CYPHT	DSBGA	YPH	6	250	180.0	8.4	0.96	1.46	0.42	4.0	8.0	Q1



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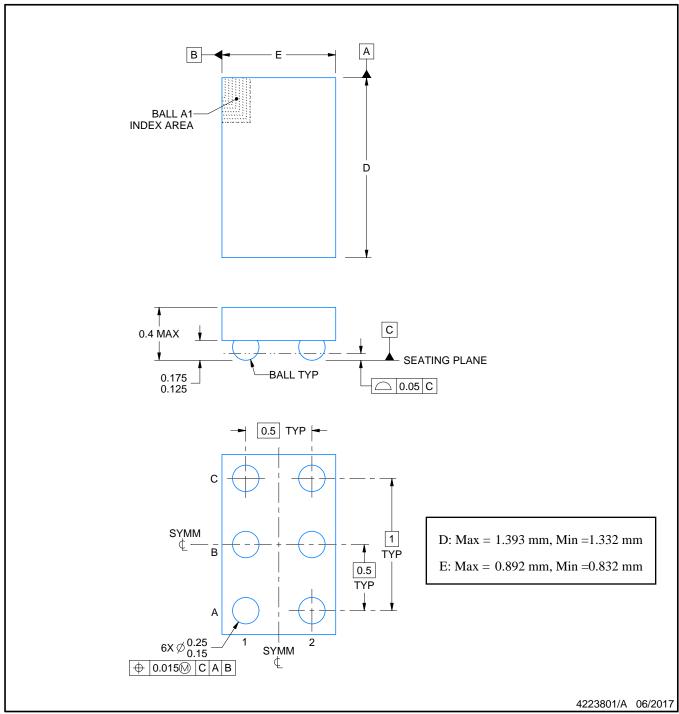


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22925BNYPHR	DSBGA	YPH	6	3000	182.0	182.0	20.0
TPS22925BNYPHT	DSBGA	YPH	6	250	182.0	182.0	20.0
TPS22925BYPHR	DSBGA	YPH	6	3000	182.0	182.0	20.0
TPS22925BYPHT	DSBGA	YPH	6	250	182.0	182.0	20.0
TPS22925CNYPHR	DSBGA	YPH	6	3000	182.0	182.0	20.0
TPS22925CNYPHT	DSBGA	YPH	6	250	182.0	182.0	20.0
TPS22925CYPHR	DSBGA	YPH	6	3000	182.0	182.0	20.0
TPS22925CYPHT	DSBGA	YPH	6	250	182.0	182.0	20.0



DIE SIZE BALL GRID ARRAY



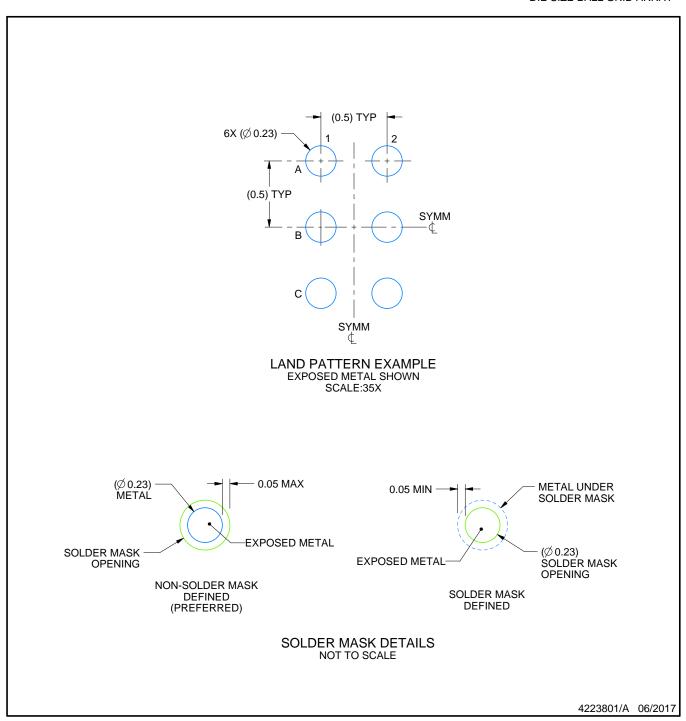
NOTES:

NanoFree Is a trademark of Texas Instruments.

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
- 3. NanoFree[™] package configuration.



DIE SIZE BALL GRID ARRAY

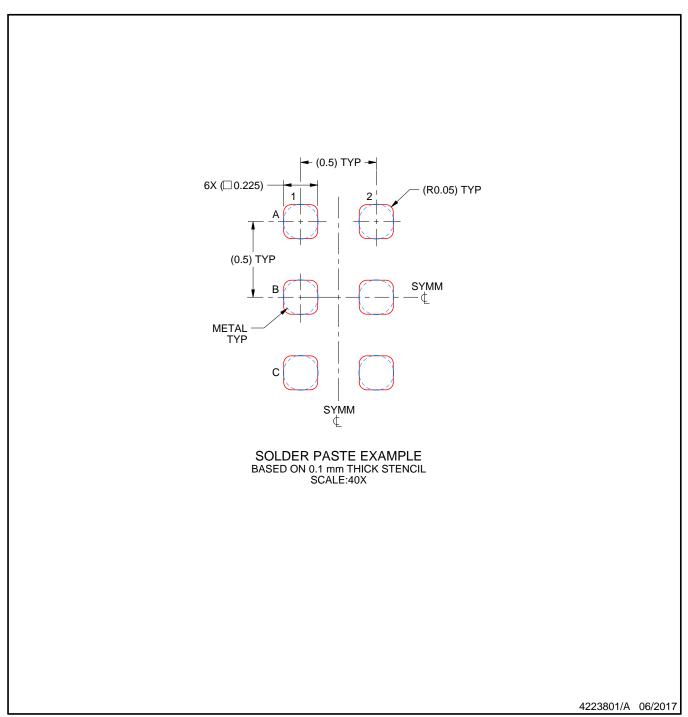


NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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