

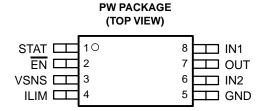
AUTOSWITCHING POWER MUX

FEATURES

- Two-Input, One-Output Power Multiplexer With Low r_{DS(on)} Switches:
 - 84 m Ω Typ (TPS2113)
 - 120 m Ω Typ (TPS2112)
- Reverse and Cross-Conduction Blocking
- Wide Operating Voltage Range 2.8 V to 5.5 V
- Low Standby Current 0.5-μA Typ
- Low Operating Current 55-μA Typ
- Adjustable Current Limit
- Controlled Output Voltage Transition Times, Limits Inrush Current and Minimizes Output Voltage Hold-Up Capacitance
- CMOS and TTL Compatible Control Inputs
- Auto-Switching Operating Mode
- Thermal Shutdown
- Available in a TSSOP-8 Package

APPLICATIONS

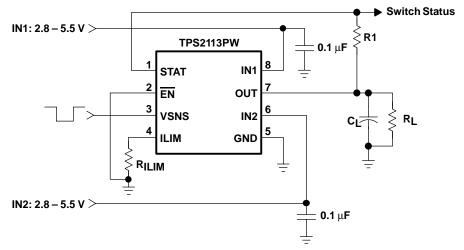
- PCs
- PDAs
- Digital Cameras
- Modems
- Cell phones
- Digital Radios
- MP3 Players



DESCRIPTION

The TPS211x family of power multiplexers enables seamless transition between two power supplies, such as a battery and a wall adapter, each operating at 2.8–5.5 V and delivering up to 1 A. The TPS211x family includes extensive protection circuitry, including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

TYPICAL APPLICATION



A

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

FEATURE		TPS2110	TPS2111	TPS2112	TPS2113	TPS2114	TPS2115
Current Limit Adjustment Range		0.31-0.75A	0.63-1.25A	0.31-0.75A	0.63-1.25A	0.31-0.75A	0.63-1.25A
Consistability of the state of	Manual	Yes	Yes	No	No	Yes	Yes
Switching modes	Automatic	Yes	Yes	Yes	Yes	Yes	Yes
Switch Status Output Automatic		No	No	Yes	Yes	Yes	Yes
Package		TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8

ORDERING INFORMATION

TA	PACKAGE	ORDERING NUMBER(1)	MARKINGS
4000 1- 0500	TSSOD 8 (DW)	TPS2112PW	2112
-40°C to 85°C	TSSOP-8 (PW)	TPS2113PW	2113

⁽¹⁾ The PW package is available taped and reeled. Add an R suffix to the device type (e.g., TPS2112PWR) to indicate tape and reel.

PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE	T _A ≤ 25°C	T _A = 70°C	T _A = 85°C
	T _A = 25°C	POWER RATING	POWER RATING	POWER RATING
TSSOP-8 (PW)	3.87 mW/°C	386.84 mW	212.76 mW	154.73 mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS2112, TPS2113
Input voltage range at pins IN1, IN2,	EN, VSNS, ILIM ⁽²⁾	−0.3 V to 6 V
Output voltage range, VO(OUT), VO	(STAT) ⁽²⁾	−0.3 V to 6 V
Output sink current, IO(STAT)		5 mA
Continuous sutmit surrent 1-	TPS2112	0.9 A
Continuous output current, IO	TPS2113	1.5 A
Continuous total power dissipation		See Dissipation Rating Table
Operating virtual junction temperatur	e range, TJ	-40°C to 125°C
Storage temperature range, T _{Stg}		−65°C to 150°C
Lead temperature soldering 1,6 mm	(1/16 inch) from case for 10 seconds	260°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIM	I MAX	UNIT
	V _{I(IN2)} ≥ 2.8 V	1.5	5.5	.,
Input voltage at IN1, V _I (IN1)	V _{I(IN2)} < 2.8 V	2.8	5.5	V
landarkan at NO V	V _{I(IN1)} ≥ 2.8 V	1.5	1.5 5.5 2.8 5.5 1.5 5.5 2.8 5.5 0 5.5 0.31 0.75 0.63 1.25	.,
Input voltage at IN2, V _{I(IN2)}	V _{I(IN1)} < 2.8 V	2.8	5.5	V
Input voltage, VI(EN), VI(VSNS)		(5.5	V
	TPS2112	0.3	0.75	_
Current limit adjustment range, IO(OUT)	TPS2113	0.63	3 1.25	A
Operating virtual junction temperature, TJ	•	-40) 125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model		2	kV
CDM		500	V

⁽²⁾ All voltages are with respect to GND.



ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5 \text{ V}$, $R_{ILIM} = 400 \Omega$ (unless otherwise noted)

PARAMETER TEST		T-0.T	CONDITIONS	TPS2112		TPS2112 TPS2113			LINUT	
		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
POWER SW	/ITCH									
		T 0500	$V_{I(IN1)} = V_{I(IN2)} = 5.0 \text{ V}$		120	140		84	110	
		T _J = 25°C, I _I = 500 mA	$V_{I(IN1)} = V_{I(IN2)} = 3.3 \text{ V}$		120	140		84	110	$m\Omega$
rac()(1)	Drain-source on-state resistance	1 <u>L</u> = 300 m/A	$V_{I(IN1)} = V_{I(IN2)} = 2.8 \text{ V}$		120	140		84	84 110 84 110	
r _{DS(on)} (1)	(INx-OUT)	T 40500	$V_{I(IN1)} = V_{I(IN2)} = 5.0 \text{ V}$			220			150	
	(/	T _J = 125°C, I _I = 500 mA	$V_{I(IN1)} = V_{I(IN2)} = 3.3 \text{ V}$			220			150	$m\Omega$
		1 <u>L</u> = 000 IIIA	$V_{I(IN1)} = V_{I(IN2)} = 2.8 \text{ V}$		•	220		•	150	

⁽¹⁾ The TPS211x can switch a voltage as low as 1.5 V as long as there is a minimum of 2.8 V at one of the input power pins. In this specific case, the lower supply voltage has no effect on the IN1 and IN2 switch on-resistances.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUTS (EN)				•	
VIH High-level input voltage		2			V
V _{IL} Low-level input voltage				0.7	V
Inputourrant	EN = High, sink current			1	^
Input current	EN = Low, source current	0.5	1.4	5	μΑ
SUPPLY AND LEAKAGE CURRE	-				
	$V_{I(VSNS)} = 1.5 \text{ V}, \overline{EN} = \text{Low (IN1 active)}, V_{I(IN1)} = 5.5 \text{ V}, V_{I(IN2)} = 3.3 \text{ V}, I_{O(OUT)} = 0 \text{ A}$		55	90	
Supply current from IN1	$V_{I(VSNS)} = 1.5 \text{ V}, \overline{EN} = \text{Low (IN1 active)}, V_{I(IN1)} = 3.3 \text{ V}, V_{I(IN2)} = 5.5 \text{ V}, I_{O(OUT)} = 0 \text{ A}$		1	12	
(operating)	$V_{I(VSNS)} = 0 \text{ V}, \overline{EN} = \text{Low (IN2 active)}, V_{I(IN1)} = 5.5 \text{ V}, V_{I(IN2)} = 3.3 \text{ V}, I_{O(OUT)} = 0 \text{ A}$			75	μΑ
	$V_{I(VSNS)} = 0 \text{ V}, \overline{EN} = \text{Low (IN2 active)}, V_{I(IN1)} = 3.3 \text{ V}, V_{I(IN2)} = 5.5 \text{ V}, I_{O(OUT)} = 0 \text{ A}$			1	
	$V_{I(VSNS)} = 1.5 \text{ V}, \overline{EN} = \text{Low (IN1 active)}, V_{I(IN1)} = 5.5 \text{ V}, V_{I(IN2)} = 3.3 \text{ V}, I_{O(OUT)} = 0 \text{ A}$			1	
Supply current from IN2	$V_{I(VSNS)} = 1.5 \text{ V}, \overline{EN} = \text{Low (IN1 active)}, V_{I(IN1)} = 3.3 \text{ V}, V_{I(IN2)} = 5.5 \text{ V}, I_{O(OUT)} = 0 \text{ A}$			75	
(operating)	$V_{I(VSNS)} = 0 \text{ V}, \overline{EN} = \text{Low (IN2 active)}, V_{I(IN1)} = 5.5 \text{ V}, V_{I(IN2)} = 3.3 \text{ V}, I_{O(OUT)} = 0 \text{ A}$		1	12	μΑ
	$V_{I(VSNS)} = 0 \text{ V}, \overline{EN} = \text{Low (IN2 active)}, V_{I(IN1)} = 3.3 \text{ V}, V_{I(IN2)} = 5.5 \text{ V}, I_{O(OUT)} = 0 \text{ A}$		55	90	
Quiescent current from IN1	$\overline{\text{EN}}$ = High (inactive), $V_{\text{I(IN1)}}$ = 5.5 V, $V_{\text{I(IN2)}}$ = 3.3 V, $I_{\text{O(OUT)}}$ = 0 A		0.5	2	μΑ
(STANDBY)	$\overline{\text{EN}}$ = High (inactive), $V_{\text{I(IN1)}}$ = 3.3 V, $V_{\text{I(IN2)}}$ = 5.5 V, $I_{\text{O(OUT)}}$ = 0 A			1	μΛ
Quiescent current from IN2	$\overline{\text{EN}}$ = High (inactive), $V_{\text{I(IN1)}}$ = 5.5 V, $V_{\text{I(IN2)}}$ = 3.3 V, $I_{\text{O(OUT)}}$ = 0 A			1	μA
(STANDBY)	$\overline{\text{EN}}$ = High (inactive), $V_{\text{I}(\text{IN1})}$ = 3.3 V, $V_{\text{I}(\text{IN2})}$ = 5.5 V, $I_{\text{O}(\text{OUT})}$ = 0 A		0.5	2	
Forward leakage current from IN1 (measured from OUT to GND)	$\overline{\text{EN}}$ = High (inactive), $V_{\text{I}(\text{IN1})}$ = 5.5 V, IN2 open, $V_{\text{O}(\text{OUT})}$ = 0 V (shorted), T_{J} = 25°C		0.1	5	μΑ
Forward leakage current from IN2 (measured from OUT to GND)	$\overline{\text{EN}}$ = High (inactive), $V_{\text{I}(\text{IN2})}$ = 5.5 V, IN1 open, $V_{\text{O}(\text{OUT})}$ = 0 V (shorted), T_{J} = 25°C		0.1	5	μΑ
Reverse leakage current to INx (measured from INx to GND)	$\overline{\text{EN}} = \text{High (inactive)}, \ V_{\text{I(INX)}} = 0 \ \text{V}, \ V_{\text{O(OUT)}} = 5.5 \ \text{V}, \ T_{\text{J}} = 25^{\circ}\text{C}$		0.3	5	μΑ
STAT OUTPUT				•	
Leakage current	V _{O(STAT)} = 5.5 V		0.01	1	μΑ
Saturationvoltage	I _I (STAT) = 2 mA, IN1 switch is on		0.13	0.4	V
Deglitch time (falling edge only)			150		μs
	<u>.</u>				



ELECTRICAL CHARACTERISTICS (Continued) over recommended operating junction temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5 \text{ V}$, $R_{ILIM} = 400 \Omega$ (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURR	RENT LIMIT CIRCUIT						
	TPS2112	$R_{ILIM} = 400 \Omega$	0.51	0.63	0.80		
	Current limit accuracy	1752112	R _{ILIM} = 700 Ω	0.30	0.36	0.50	٨
	Current limit accuracy	TPS2113	$R_{ILIM} = 400 \Omega$	0.95	1.25	1.56	Α
		11732113	R _{ILIM} = 700 Ω	0.47	0.71	0.99	
^t d	Current limit settling time ⁽¹⁾		Time for short–circuit output current to settle within 10% of its steady state value.		1		ms
	Input current at ILIM		V _{I(ILIM)} = 0 V, I _{O(OUT)} = 0 A	-15		0	μΑ

⁽¹⁾ Not tested in production.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSNS COMPARATOR	•				
VONO the set of desire	V _I (VSNS) ↑	0.78	0.8	0.82	.,
VSNS threshold voltage	VI(VSNS) ↓	0.735	0.755	0.775	V
VSNS comparator hysteresis(1)		30		60	mV
Deglitch of VSNS comparator (both $\uparrow\downarrow$)(1)		90	150	220	μs
Input current	$0 \text{ V} \le \text{V}_{\text{I(VSNS)}} \le 5.5 \text{ V}$	-1		1	μΑ
UVLO	•				
	Fallingedge	1.15	1.25		.,
IN1 and IN2 UVLO	Rising edge		1.30	1.35	V
IN1 and IN2 UVLO hysteresis(1)		30	57	65	mV
Laterace IV LIVI O (the high and INI)	Fallingedge	2.4	2.53		.,
Internal V _{DD} UVLO (the higher of IN1 and IN2)	Rising edge		2.58	2.8	V
Internal V _{DD} UVLO hysteresis ⁽¹⁾		30	50	75	mV
UVLO deglitch for IN1, IN2 ⁽¹⁾	Fallingedge		110		μs

⁽¹⁾ Not tested in production.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
REVERSE CO	REVERSE CONDUCTION BLOCKING								
$\Delta V_{O(I_block)}$	Minimumoutput-to-inputvoltage difference to block switching	$\overline{\text{EN}}$ = high, $V_{\text{I(IN1)}}$ = 3.3 V and $V_{\text{I(IN2)}}$ = $V_{\text{I(VSNS)}}$ = 0 V. Connect OUT to a 5 V supply through a series 1-k Ω resistor. Let $\overline{\text{EN}}$ = low. Slowly decrease the supply voltage until OUT connects to IN1.	80	100	120	mV			

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
Thermal shutdown threshold(1)	TPS211x is in current limit.	135			
Recovery from thermal shutdown(1)	TPS211x is in current limit.	125			°C
Hysteresis(1)			10		
IN2-IN1 COMPARATORS	·				
Hysteresis of IN2–IN1 comparator		0.1		0.2	V
Deglitch of IN2–IN1 comparator, (both ↑↓)(1)		90	150	220	μs

⁽¹⁾ Not tested in production.



SWITCHING CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5 \text{ V}$, $R_{ILIM} = 400 \Omega$ (unless otherwise noted)

			Т	PS2112	2	Т				
	PARAMETER	TEST CO	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
POWE	R SWITCH									
t _r	Output rise time from an enable ⁽¹⁾	V _I (IN1) = V _I (IN2) = 5 V, V _I (VSNS) = 1.5 V	$T_J = 25^{\circ}C, C_L = 1 \mu F,$ $I_L = 500 \text{ mA},$ See Figure 1(a)	0.5	1.0	1.5	1	1.8	3	ms
tf	Output fall time from a disable ⁽¹⁾	V _I (IN1) = V _I (IN2) = 5 V, V _I (VSNS) = 1.5 V	$T_J = 25^{\circ}C, C_L = 1 \mu F,$ $I_L = 500 \text{ mA},$ See Figure 1(a)	0.35	0.5	0.7	0.5	1	2	ms
tt	Transition time(1)	IN1 to IN2 transition, $V_{I(IN1)} = 3.3 \text{ V},$ $V_{I(IN2)} = 5 \text{ V},$ $V_{I(EN)} = 0 \text{ V}$	T_J = 125°C, C_L = 10 μF, I_L = 500 mA [Measure transition time as 10–90% rise time or from 3.4 V to 4.8 V on VO(OUT)], See Figure 1(b)		40	60		40	60	με
^t PLH1	Turn-onpropagation delay from enable(1)	VI(IN1) = VI(IN2) = 5 V Measured from enable to 10% of VO(OUT), VI(VSNS) = 1.5 V	$T_J = 25$ °C, $C_L = 10 \mu F$, $I_L = 500 \text{ mA}$, See Figure 1(a)		0.5			1		ms
^t PHL1	Turn-off propagation delay from a disable ⁽¹⁾	VI(IN1) = VI(IN2) = 5 V, Measured from disable to 90% of VO(OUT), VI(VSNS) = 1.5 V	$T_J = 25$ °C, $C_L = 10 \mu F$, $I_L = 500 \text{ mA}$, See Figure 1(a)		3			5		ms
tPLH2	Switch-over rising propagation delay(1)	Logic 1 to Logic 0 transition on VSNS, VI(IN1) = 1.5 V, VI(<u>IN2</u>) = 5 V, VI(<u>EN</u>) = 0 V, Measured from VSNS to 10% of VO(OUT)	$T_J = 25$ °C, $C_L = 10 \mu F$, $I_L = 500 \text{ mA}$, See Figure 1(c)		0.17	1		0.17	1	ms
^t PHL2	Switch-overfalling propagation delay(1)	Logic 0 to Logic 1 transition on VSNS VI(IN1) = 1.5V, VI(IN2) = 5V, VI(EN) = 0 V, Measured from VSNS to 90% of VO(OUT)	$T_J = 25$ °C, $C_L = 10 \mu F$, $I_L = 500 \text{ mA}$, See Figure 1(c)	2	3	10	2	5	10	ms

⁽¹⁾ Not tested in production.



TRUTH TABLE

EN	V _{I(VSNS)} > 0.8V	V _{I(IN2)} > V _{I(IN1)}	STAT	OUT(1)
	Yes	X	0	IN1
0	No	No	0	IN1
	No	Yes	Hi-Z	IN2
1	Х	Х	0	Hi-Z

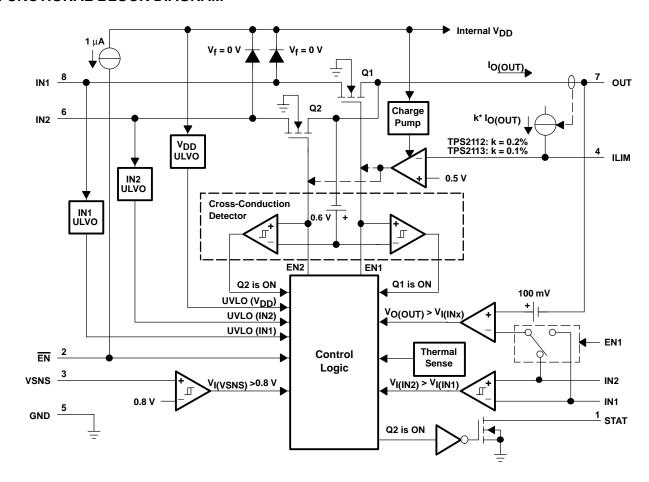
⁽¹⁾The under-voltage lockout circuit causes the output OUT to go Hi-Z if the selected power supply does not exceed the IN1/IN2 UVLO, or if neither of the supplies exceeds the internal $V_{\mbox{DD}}$ UVLO.

Terminal Functions

TERMI	NAL		DESCRIPTION						
NAME	NO.	1/0	DESCRIPTION						
EN	2	I	EN is a TTL and CMOS compatible input with a 1-μA pull-up. The truth table shown above illustrates the functionality of EN.						
GND	5	I	Ground						
IN1	8	I	Primary power switch input. The IN1 switch can be enabled only if the IN1 supply is above the UVLO threshold and at least one supply exceeds the internal V _{DD} UVLO.						
IN2	6	I	Secondary power switch input. The IN2 switch can be enabled only if the IN2 supply is above the UVLO threshold and at least one supply exceeds the internal V _{DD} UVLO.						
ILIM	4	I	A resistor R_{ILIM} from ILIM to GND sets the current limit I_L to $250/R_{ILIM}$ and $500/R_{ILIM}$ for the TPS2112 and TPS2113, respectively.						
OUT	7	0	Power switch output						
STAT	1	0	STAT is an open-drain output that is Hi-Z if the IN2 switch is ON. STAT pulls low if the IN1 switch is ON or if OUT is Hi-Z (i.e., EN is equal to logic 0)						
VSNS	3	I	An internal power FET connects OUT to IN1 if the VSNS voltage is greater than 0.8 V. Otherwise, the FET connects OUT to the higher of IN1 and IN2. The truth table shown above illustrates the functionality of VSNS.						



FUNCTIONAL BLOCK DIAGRAM





PARAMETER MEASUREMENT INFORMATION

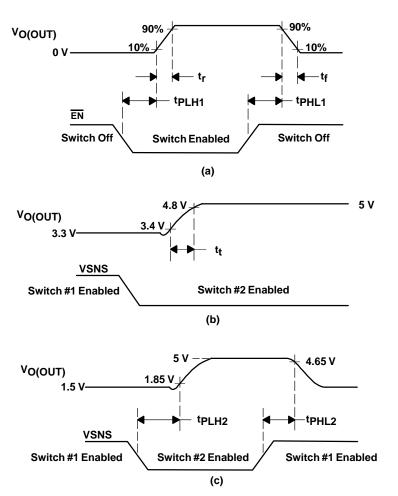


Figure 1. Propagation Delays and Transition Timing Waveforms



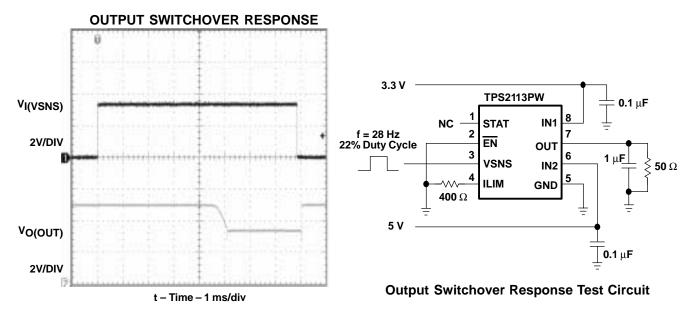


Figure 2

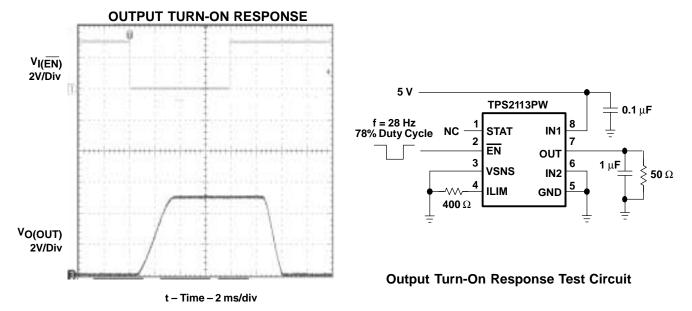
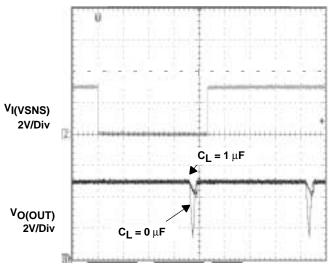


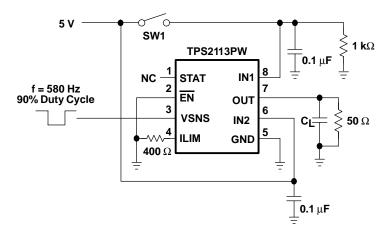
Figure 3



OUTPUT SWITCHOVER VOLTAGE DROOP



t – Time – 40 μ s/div



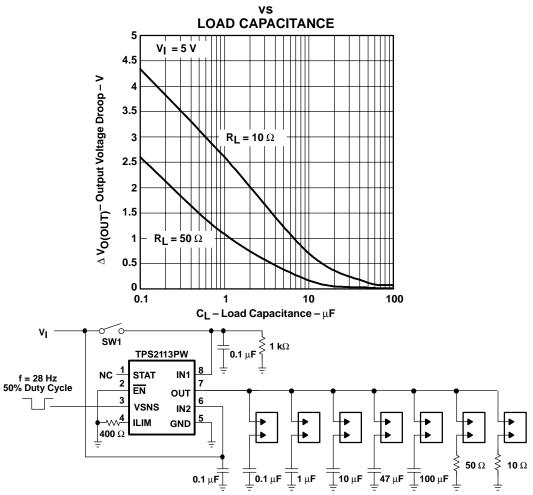
Output Switchover Voltage Droop Test Circuit

Figure 4

NOTE: To initialize the TPS2113 for this test, set input VSNS equal to 0 V, turn on the 5 V supply, and then turn on switch SW1.



OUTPUT SWITCHOVER VOLTAGE DROOP



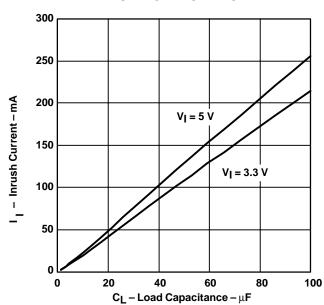
Output Switchover Voltage Droop Test Circuit

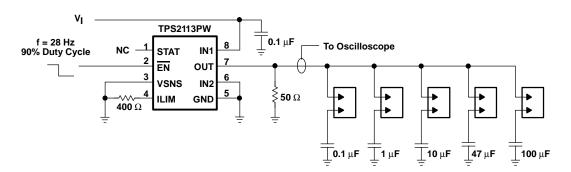
Figure 5

NOTE: To initialize the TPS2113 for this test, set input VSNS equal to 0 V, turn on the supply V_i , and then turn on switch SW1.



INRUSH CURRENT vs LOAD CAPACITANCE

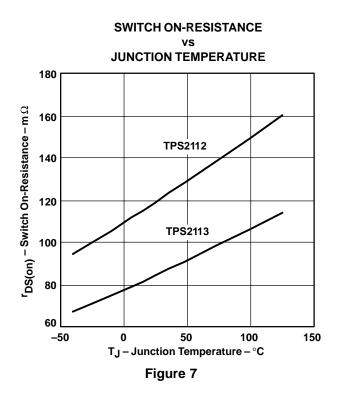


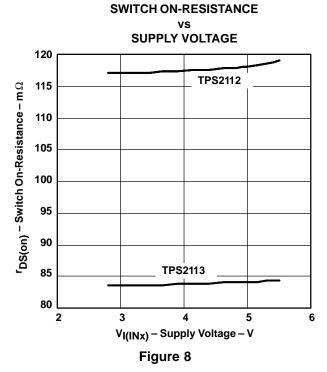


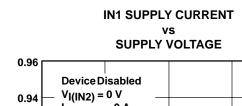
Output Capacitor Inrush Current Test Circuit

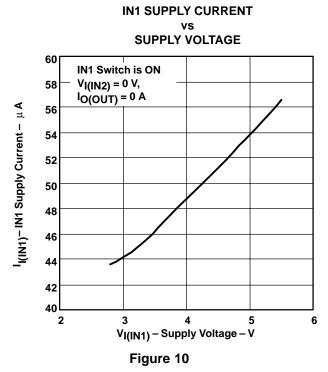
Figure 6

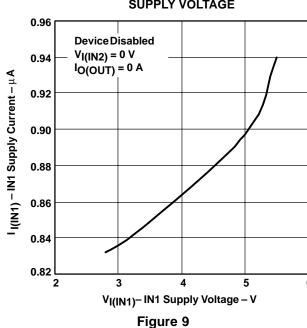




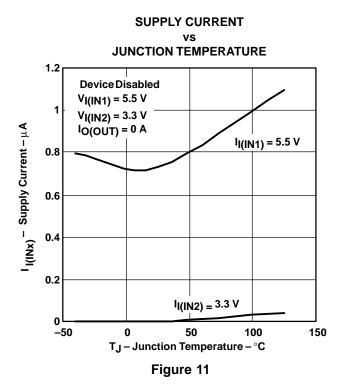


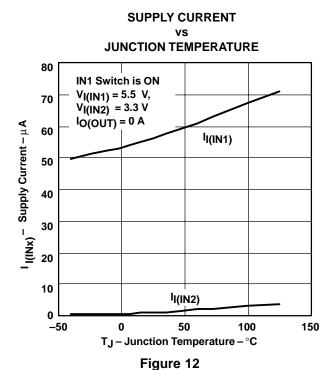














APPLICATION INFORMATION.

Some applications have two energy sources, one of which should be used in preference to another. Figure 13 shows a circuit that will connect IN1 to OUT until the voltage at IN1 falls below a user-specified threshold. Once the voltage on IN1 falls below this threshold, the TPS2112/3 will select the higher of the two supplies. This usually means that the TPS2112/3 will swap to IN2.

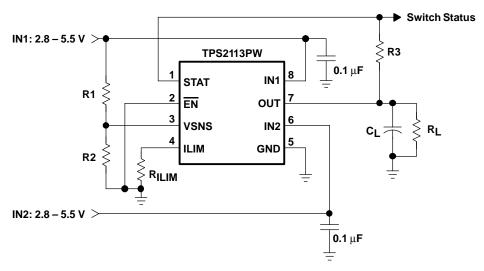


Figure 13. Auto-Selecting for a Dual Power Supply Application

In Figure 14, the multiplexer selects between two power supplies based upon the \overline{EN} logic signal. OUT connects to IN1 if \overline{EN} is logic 1, otherwise OUT connects to IN2. The logic thresholds for the \overline{EN} terminal are compatible with both TTL and CMOS logic.

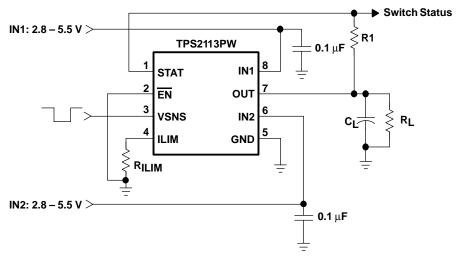


Figure 14. Manually Switching Power Sources



DETAILED DESCRIPTION

AUTO-SWITCHING MODE

The TPS2112/3 only supports the auto-switching mode. In this mode, OUT connects to IN1 if $V_{I(VSNS)}$ is greater than 0.8 V, otherwise OUT connects to the higher of IN1 and IN2.

The VSNS terminal includes hysteresis equal to 3.75–7.5% of the threshold selected for transition from the primary supply to the higher of the two supplies. This hysteresis helps avoid repeated switching from one supply to the other due to resistive drops.

N-CHANNEL MOSFETs

Two internal high-side power MOSFETs implement a single-pole double-throw (SPDT) switch. Digital logic selects the IN1 switch, IN2 switch, or no switch (Hi-Z state). The MOSFETs have no parallel diodes so output-to-input current cannot flow when the FET is off. An integrated comparator prevents turn-on of a FET switch if the output voltage is greater than the input voltage.

CROSS-CONDUCTION BLOCKING

The switching circuitry ensures that both power switches will never conduct at the same time. A comparator monitors the gate-to-source voltage of each power FET and allows a FET to turn on only if the gate-to-source voltage of the other FET is below the turn-on threshold voltage.

REVERSE-CONDUCTION BLOCKING

When the TPS211x switches from a higher-voltage supply to a lower-voltage supply, current can potentially flow back from the load capacitor into the lower-voltage supply. To minimize such reverse conduction, the TPS211x will not connect a supply to the output until the output voltage has fallen to within 100 mV of the supply voltage. Once a supply has been connected to the output, it will remain connected regardless of output voltage.

CHARGE PUMP

The higher of supplies IN1 and IN2 powers the internal charge pump. The charge pump provides power to the current limit amplifier and allows the output FET gate voltage to be higher than the IN1 and IN2 supply voltages. A gate voltage that is higher than the source voltage is necessary to turn on the N-channel FET.

CURRENT LIMITING

A resistor R_{ILIM} from ILIM to GND sets the current limit to 250/ R_{ILIM} and 500/R_{ILIM} for the TPS2112 and TPS2113, respectively. Setting resistor R_{ILIM} equal to zero is not recommended as that disables current limiting.

OUTPUT VOLTAGE SLEW-RATE CONTROL

The TPS2112/3 slews the output voltage at a slow rate when OUT switches to IN1 or IN2 from the Hi-Z state (see *Truth Table*).). A slow slew rate limits the inrush current into the load capacitor. High inrush currents can glitch the voltage bus and cause a system to hang up or reset. It can also cause reliability issues—like pit the connector power contacts, when hot plugging a load like a PCI card. The TPS2112/3 slews the output voltage at a much faster rate when OUT switches between IN1 and IN2. The fast rate minimizes the output voltage droop and reduces the output voltage hold-up capacitance requirement.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TPS2112PW	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2112
TPS2112PW.A	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2112
TPS2112PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2112
TPS2112PWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2112
TPS2113PW	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2113
TPS2113PW.A	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2113
TPS2113PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2113
TPS2113PWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2113

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS KO P1 BO W Cavity A0

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2112PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS2113PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2112PWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TPS2113PWR	TSSOP	PW	8	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2112PW	PW	TSSOP	8	150	530	10.2	3600	3.5
TPS2112PW.A	PW	TSSOP	8	150	530	10.2	3600	3.5
TPS2113PW	PW	TSSOP	8	150	530	10.2	3600	3.5
TPS2113PW.A	PW	TSSOP	8	150	530	10.2	3600	3.5



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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