











**TPS2065D** 

SLVSDQ4-DECEMBER 2016

# **TPS2065D Current Limited, Power-Distribution Switches**

#### **Features**

- Single Power Switch Family
- Rated currents of 1 A
- ±20% Accurate, Fixed, Constant Current Limit
- Fast Overcurrent Response: 2 µs
- **Deglitched Fault Reporting**
- **Output Discharge**
- Reverse Current Blocking
- **Built-in Soft Start**
- Ambient Temperature Range: -40°C to 85°C
- UL Listed and CB-File No. E169910

# Applications

- USB Ports/Hubs, Laptops, Desktops
- High-Definition Digital TVs
- Set Top Boxes
- Short Circuit Protection

# 3 Description

The TPS2065D power-distribution switch family is intended for applications such as USB where heavy capacitive loads and short circuits are likely to be encountered. The device can continuously deliver up to 1 A output current.

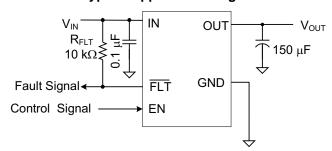
The TPS2065D limits the output current to a safe level by operating in a constant-current mode when the output load exceeds the current limit threshold. This provides a predictable fault current under all conditions. The fast overload response time eases the burden on the main 5-V supply to provide regulated power when the output is shorted. The power-switch rise and fall times are controlled to minimize current surges during turnon and turnoff.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2065D	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### **Typical Application Diagram**



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# 4 Revision History

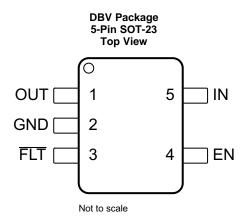
DATE	REVISION	NOTES
December 2016	*	Initial release.



# 5 Device Comparison Table

MAXIMUM OPERATING CURRENT	OUTPUT DISCHARGE	ENABLE
1 A	Υ	High

# 6 Pin Configuration and Functions



## **Pin Functions**

PIN			
NAME	NO.	1/0	DESCRIPTION
EN	4	- 1	Enable input, logic high turns on power switch
GND	2	_	Ground connection
IN	5	PWR	Input voltage and power-switch drain; connect a 0.1-µF or greater ceramic capacitor from IN to GND close to the IC
FLT	3	0	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions
OUT	1	PWR	Power-switch output, connect to load.

# 7 Specifications

#### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

	MIN	MAX	UNIT
Voltage range on IN, OUT, EN, FLT (4)	-0.3	6	V
Voltage range from IN to OUT	-6	6	V
Maximum junction temperature, T <sub>J</sub>	Internall	y Limited	
Storage temperature, T <sub>stg</sub>	-60	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Absolute maximum ratings apply over recommended junction temperature range.

3) Voltages are with respect to GND unless otherwise noted.

(4) See Input and Output Capacitance.

## 7.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	
V	Electrostatio discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	\/
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 contact discharge (3)	±8000	V
		IEC 61000-4-2 air-gap discharge	±15000	

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

# 7.3 Recommended Operating Conditions

		MIN	NOM MAX	UNIT
$V_{IN}$	Input voltage, IN	4.5	5.5	V
$V_{EN}$	Input voltage, EN	0	5.5	V
V <sub>IH</sub>	High-level input voltage, EN	2		V
V <sub>IL</sub>	Low-level input voltage, EN		0.7	V
I <sub>OUT</sub>	Continuous output current, OUT <sup>(1)</sup>		1 A	A
$T_{J}$	Operating junction temperature	-40	125	°C
IFLT	Sink current into FLT	0	5	mA mA

<sup>(1)</sup> Some package and current rating may request an ambient temperature derating of 85°C.

#### 7.4 Thermal Information

		TPS2065D	
	THERMAL METRIC(1)	DBV (SOT-23)	UNIT
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	224.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	95.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	6.6	°C/W
ΨЈВ	Junction-to-board characterization parameter	50.3	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W
$R_{\theta JA} Custom$	See Power Dissipation and Junction Temperature	139.3	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

<sup>(3)</sup> V<sub>OUT</sub> was surged on a pcb with input and output bypassing per Input and Output Capacitance (except input capacitor was 22 μF) with no device failures.



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# 7.5 Electrical Characteristics: $T_J = T_A = 25^{\circ}C^{(1)}$

Unless otherwise noted:  $V_{IN} = 5 \text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 0 \text{ A}$ . See *Device Comparison Table* for the rated current of each part number. Parametrics over a wider operational range are shown in *Electrical Characteristics:*  $-40^{\circ}\text{C} \le T_{J} \le 125^{\circ}\text{C}$ .

	PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
POWER	SWITCH		"			
		1-A rated output, 25°C DBV	′	96	110	mΩ
R <sub>DS(on)</sub>	Input – output resistance	1-A rated output, $-40^{\circ}\text{C} \le (\text{T}_{\text{J}}, \text{T}_{\text{A}}) \le 85^{\circ}\text{C}$	,	96	130	mΩ
CURRE	NT LIMIT					
I <sub>OS</sub> <sup>(2)</sup>	Current limit, See Figure 6	1-A rated output	1.3	1.55	1.8	Α
SUPPLY	CURRENT					
	Cumply ourment quitab disabled	I <sub>OUT</sub> = 0 A		0.01	1	
I <sub>SD</sub>	Supply current, switch disabled	$-40$ °C $\leq$ (T <sub>J</sub> , T <sub>A</sub> ) $\leq$ 85°C, V <sub>IN</sub> = 5.5 V, I <sub>OUT</sub> = 0	Α		1 2 70	μA
	Cumply gurrant quitab anablad	I <sub>OUT</sub> = 0 A		60	70	
I <sub>SE</sub>	Supply current, switch enabled	$-40$ °C $\leq$ (T <sub>J</sub> , T <sub>A</sub> ) $\leq$ 85°C, V <sub>IN</sub> = 5.5 V, I <sub>OUT</sub> = 0	Α		85	μA
		V <sub>OUT</sub> = 5 V, V <sub>IN</sub> = 0 V, measure I <sub>VOUT</sub>		0.1	1	
I <sub>REV</sub>	Reverse leakage current	$-40$ °C $\leq$ (T <sub>J</sub> , T <sub>A</sub> ) $\leq$ 85°C, V <sub>OUT</sub> = 5 V, V <sub>IN</sub> = 0 I <sub>VOUT</sub>	V, measure		1 2 70	μA
OUTPUT	DISCHARGE					
R <sub>PD</sub>	Output pulldown resistance (3)	V <sub>IN</sub> = V <sub>OUT</sub> = 5 V, disabled	400	470	600	Ω

<sup>(1)</sup> Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature

<sup>(2)</sup> See *Current Limit* section for explanation of this parameter.

<sup>(3)</sup> These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

# **TRUMENTS**

# 7.6 Electrical Characteristics: -40°C ≤ T<sub>J</sub> ≤ 125°C

Unless otherwise noted:4.5 V  $\leq$  V<sub>IN</sub>  $\leq$  5.5 V, V<sub>EN</sub> = V<sub>IN</sub>, I<sub>OUT</sub> = 0 A, typical values are at 5 V and 25°C. See *Device Comparison Table* for the rated current of each part number.

	PARAMETER	TEST CO	ONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
POWER	SWITCH	'	,				
R <sub>DS(ON)</sub>	Input – output resistance	1-A rated output	DBV		96	154	mΩ
	E INPUT (EN)	<u>'</u>					
	Threshold	Input rising		1	1.45	2	V
	Hysteresis			0.07	0.13	0.20	V
	Leakage current	(V <sub>EN</sub> ) = 0 V		-1	0	1	μA
CURRE	NT LIMIT						
I <sub>OS</sub> <sup>(2)</sup>	Current limit, See Figure 22	1-A rated output		1.2	1.55	1.9	Α
t <sub>iOS</sub>	Short circuit response time (3)	$V_{\text{IN}} = 5 \text{ V}$ (see Figure 6), One-half full load $\rightarrow$ R <sub>SHORT</sub> Measure from application to final value	= 50 m $\Omega$ , when current falls below 120% of		2		μs
SUPPLY	CURRENT						
I <sub>SD</sub>	Supply current, switch disabled	I <sub>OUT</sub> = 0 A			0.01	10	μΑ
I <sub>SE</sub>	Supply current, switch enabled	I <sub>OUT</sub> = 0 A			65	90	μA
I <sub>REV</sub>	Reverse leakage current	$V_{OUT} = 5.5 \text{ V}, V_{IN} = 0 \text{ V}, \text{ mea}$	asure I <sub>VOUT</sub>		0.2	20	μΑ
UNDER	VOLTAGE LOCKOUT					·	
V <sub>UVLO</sub>	Rising threshold	V <sub>IN</sub> ↑		3.5	3.75	4	V
	Hysteresis <sup>(3)</sup>	V <sub>IN</sub> ↓			0.14		V
FLT						·	
	Output low voltage, FLT	I <sub>FLT</sub> = 1 mA				0.2	V
	Off-state leakage	V <sub>FLT</sub> = 5.5 V				1	μΑ
t <sub>FLT</sub>	FLT deglitch	FLT assertion or deassertion	n deglitch	6	9	12	ms
OUTPU	T DISCHARGE						
D	Out-ut	V <sub>IN</sub> = 4 V, V <sub>OUT</sub> = 5 V, disabl	led	350	560	1200	Ω
R <sub>PD</sub>	Output pulldown resistance	V <sub>IN</sub> = 5 V, V <sub>OUT</sub> = 5 V, disabl	led	300	470	800	Ω
THERM	AL SHUTDOWN						
	Diging throughold (T.)	In current limit		135			
	Rising threshold (T <sub>J</sub> )	Not in current limit		155			°C
	Hysteresis (3)				20		

- (1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
- See *Current Limit* for explanation of this parameter.

  These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's

## 7.7 Timing Requirements: -40°C ≤ T₁ ≤ 125°C

			MIN	NOM	MAX	UNIT
t <sub>ON</sub>	Turnon time	$V_{IN}$ = 5 V, $C_L$ = 1 μF, $R_L$ = 100 $\Omega$ , EN ↑ or $\overline{EN}$ ↓. See Figure 1, Figure 3, and Figure 4 1 A Rated	1	1.4	1.8	ms
t <sub>OFF</sub>	Turnoff time	$V_{IN}$ = 5 V, $C_L$ = 1 μF, $R_L$ = 100 $\Omega$ , EN $\downarrow$ or $\overline{EN}$ $\uparrow$ . See Figure 1, Figure 3, and Figure 4 1 A Rated	1.3	1.65	2	ms
t <sub>R</sub>	Rise time, output	$C_L$ = 1 $\mu$ F, $R_L$ = 100 $\Omega$ , $V_{IN}$ = 5 V. See Figure 2 1 A Rated	0.4	0.55	0.7	ms
t <sub>F</sub>	Fall time, output	$C_L$ = 1 $\mu F,~R_L$ = 100 $\Omega,~V_{IN}$ = 5 V. See Figure 2 1 A Rated	0.25	0.35	0.45	ms

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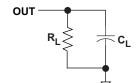


Figure 1. Output Rise and Fall Test Load



Figure 2. Power-On and Power-Off Timing

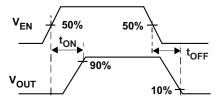


Figure 3. Enable Timing, Active High Enable

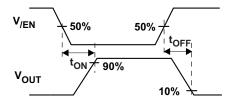


Figure 4. Enable Timing, Active Low Enable

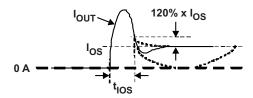


Figure 5. Output Short Circuit Parameters

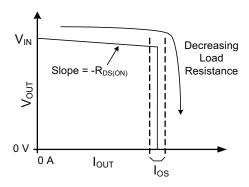
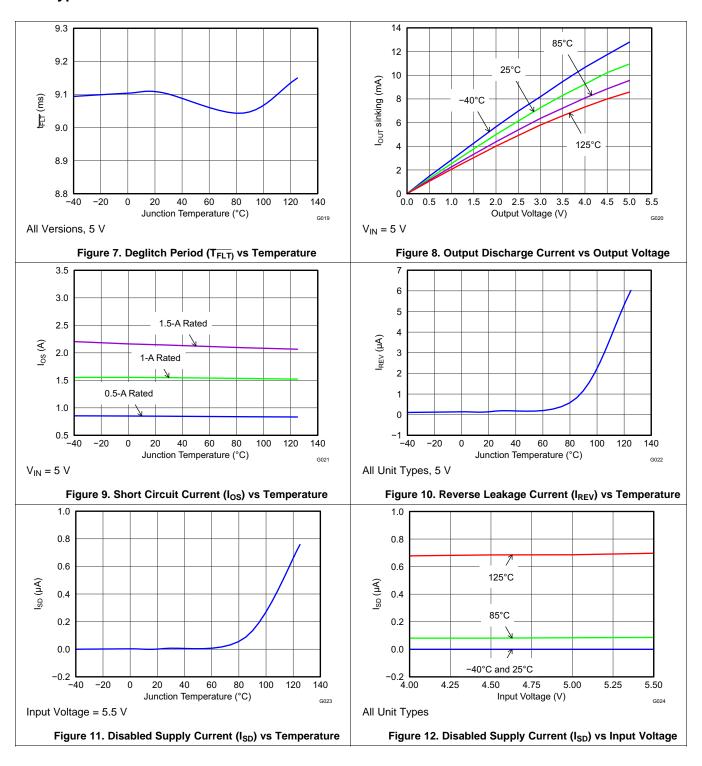


Figure 6. Output Characteristic Showing Current Limit

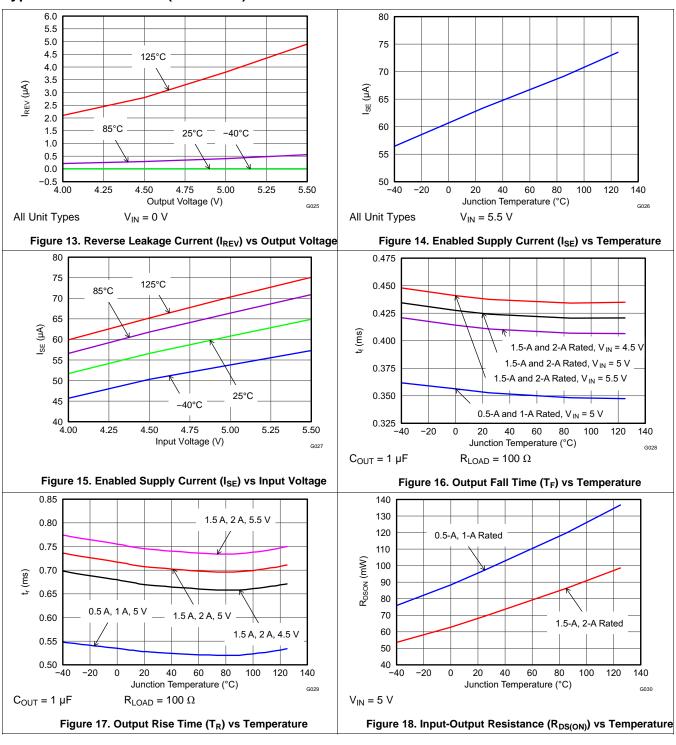
## 7.8 Typical Characteristics



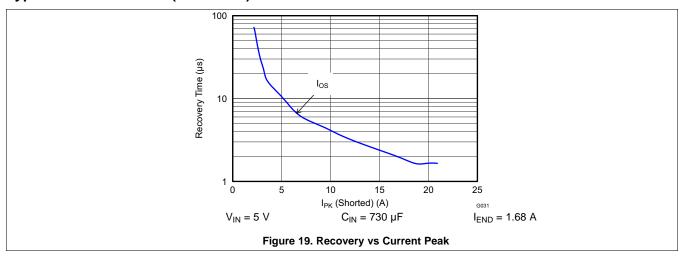


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## **Typical Characteristics (continued)**



# **Typical Characteristics (continued)**



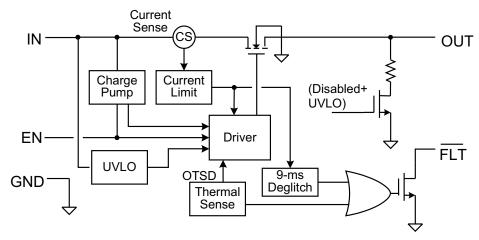
# 8 Detailed Description

#### 8.1 Overview

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The TPS2065D are current limited, power-distribution switches providing 1 A of continuous load current in 5-V circuits. These parts use N-channel MOSFETs for low resistance, maintaining voltage regulation to the load. They are designed for applications where short circuits or heavy capacitive loads are encountered. Device features include enable, reverse blocking when disabled, output discharge pulldown, overcurrent protection, overtemperature protection, and deglitched fault reporting.

## 8.2 Functional Block Diagrams



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Figure 20. Block Diagram

#### 8.3 Feature Description

## 8.3.1 Undervoltage Lockout

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted ON/OFF cycling due to input voltage drop from large current surges. FLT is high impedance when the TPS2065D is in UVLO.

#### 8.3.2 **Enable**

The logic enable input (EN), controls the power switch, bias for the charge pump, driver, and other circuits. The supply current is reduced to less than 1  $\mu$ A when the TPS2065D is disabled. Disabling the TPS2065D immediately clears an active  $\overline{FLT}$  indication. The enable input is compatible with both TTL and CMOS logic levels.

The turnon and turnoff times  $(t_{ON}, t_{OFF})$  are composed of a delay and a rise or fall time  $(t_R, t_F)$ . The delay times are internally controlled. The rise time is controlled by the device and the external loading (especially capacitance). TPS2065D fall time is controlled by the loading (R and C), and the output discharge  $(R_{PD})$ . An output load consisting of only a resistor will experience a fall time set by the device. An output load with parallel R and C elements experiences a fall time determined by the  $(R \times C)$  time constant if it is longer than the device  $t_F$ .

The enable should not be left open, and may be tied to VIN or GND depending on the device.

## **Feature Description (continued)**

#### 8.3.3 Internal Charge Pump

The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the gate driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionality. The MOSFET power switch will block current from OUT to IN when turned off by the UVLO or disabled.

#### 8.3.4 Current Limit

The TPS2065D responds to overloads by limiting output current to the static  $I_{OS}$  levels shown in *Electrical Characteristics:*  $T_J = T_A = 25^{\circ}C^{(1)}$ . When an overload condition is present, the device maintains a constant output current, with the output voltage determined by  $(I_{OS} \times R_{LOAD})$ . Two possible overload conditions can occur.

The first overload condition occurs when either: 1) input voltage is first applied, enable is true, and a short circuit is present (load which draws  $I_{OUT} > I_{OS}$ ), or 2) input voltage is present and the device is enabled into a short circuit. The output voltage is held near zero potential with respect to ground and the TPS2065D ramps the output current to  $I_{OS}$ . The device limits the current to  $I_{OS}$  until the overload condition is removed or the device begins to thermal cycle.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within  $t_{IOS}$  (Figure 5 and Figure 6) when the specified overload (see *Electrical Characteristics:*  $-40^{\circ}C \le T_{J} \le 125^{\circ}C$ ) is applied. The response speed and shape varies with the overload level, input circuit, and rate of application. The current limit response will vary between simply settling to  $I_{OS}$ , or turnoff and controlled return to  $I_{OS}$ . Similar to the previous case, the device limits the current to  $I_{OS}$  until the overload condition is removed or the device begins to thermal cycle.

The TPS2065D thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation  $[(V_{IN} - V_{OUT}) \times I_{OS}]$  driving the junction temperature up. The device turns off when the junction temperature exceeds 135°C (minimum) while in current limit. The device remains off until the junction temperature cools 20°C and then restarts.

There are two kinds of current limit profiles typically available in TI switch products similar to the TPS2065D. Many older designs have an output I vs V characteristic similar to the plot labeled **Current Limit with Peaking** in Figure 21. This type of limiting can be characterized by two parameters, the current limit corner ( $I_{OC}$ ), and the short circuit current ( $I_{OS}$ ).  $I_{OC}$  is often specified as a maximum value. The TPS2065D does not present noticeable peaking in the current limit, corresponding to the characteristic labeled **Flat Current Limit** in Figure 21. This is why the  $I_{OC}$  parameter is not present in *Electrical Characteristics:*  $-40^{\circ}C \le T_J \le 125^{\circ}C$ .

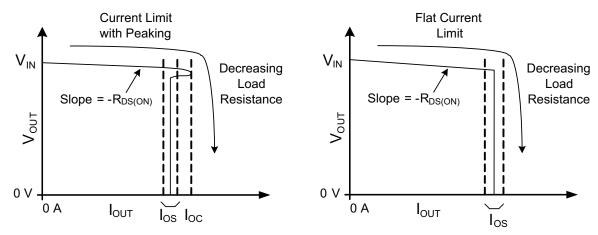


Figure 21. Current Limit Profiles

# **Feature Description (continued)**

#### 8.3.5 FLT

The FLT open-drain output is asserted (active low) during an overload or overtemperature condition. A 9-ms deglitch on both the rising and falling edges avoids false reporting at start-up and during transients. A current limit condition shorter than the deglitch period clears the internal timer upon termination. The deglitch timer will not integrate multiple short overloads and declare a fault. This is also true for exiting from a faulted state. An input voltage with excessive ripple and large output capacitance may interfere with operation of FLT around I<sub>OS</sub> as the ripple drives the device in and out of current limit.

If the TPS2065D is in current limit and the overtemperature circuit goes active, FLT goes true immediately; however, the exiting this condition is deglitched. FLT is tripped just as the knee of the constant-current limiting is entered. Disabling the device clears an active FLT as soon as the switch turns off. FLT is high impedance when the device is disabled or in undervoltage lockout (UVLO).

## 8.3.6 Output Discharge

A 470- $\Omega$  (typical) output discharge dissipates stored charge and leakage current on OUT when the TPS2065D is in UVLO or disabled. The pulldown circuit loses bias gradually as  $V_{IN}$  decreases, causing a rise in the discharge resistance as  $V_{IN}$  falls towards 0 V. The output is be controlled by an external loadings when the device is in ULVO or disabled.

#### 8.4 Device Functional Modes

There are no other functional modes.

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# TEXAS INSTRUMENTS

# 9 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

# 9.1 Application Information

The TPS2065D current limited power switch uses N-channel MOSFETs in applications requiring continuous load current. The device enters constant-current mode when the load exceeds the current limit threshold.

# 9.2 Typical Application

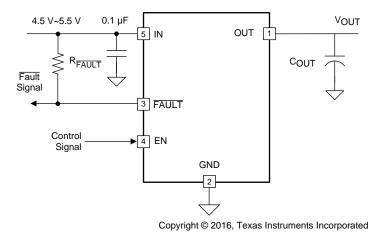


Figure 22. Typical Application Schematic

#### 9.2.1 Design Requirements

For this design example, use the following input parameters:

- 1. The TPS2065D operates from a 5 V±0.5V rail.
- 2. What is the normal operation current, for example, the maximum allowable current drawn by portable equipment for USB 3.0 port is 900 mA, so the normal operation current is 900 mA, and the minimum current limit of power switch must exceed 900 mA to avoid false trigger during normal operation. For the TPS2065D device, target 1 A continuous output current application.
- 3. What is the maximum allowable current provided by up-stream power, the maximum current limit of power switch that must lower it to ensure power switch can protect the up-stream power when overload is encountered at the output of power switch. For the TPS2065D device, the maximum I<sub>OS</sub> is 1.8 A.

# 9.2.2 Detailed Design Procedure

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- 1. Normal input operation voltage
- 2. Output continuous current
- 3. Maximum up-stream power supply output current



## **Typical Application (continued)**

#### 9.2.2.1 Input and Output Capacitance

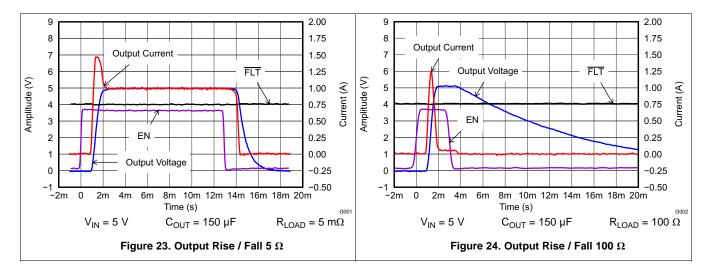
Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, TI recommends placing a 0.1-µF or greater ceramic bypass capacitor between IN and GND, as close to the device as possible for local noise decoupling.

All protection circuits such as the TPS2065D has the potential for input voltage overshoots and output voltage undershoots.

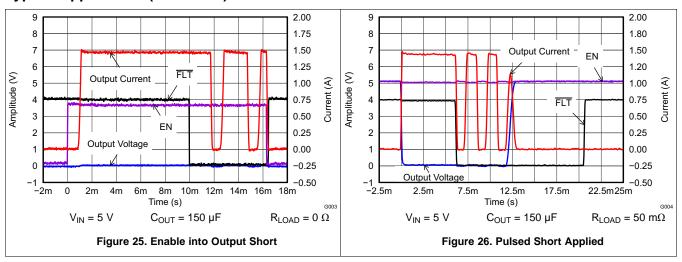
Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power bus inductance and input capacitance when the IN terminal is high impedance (before turnon). Theoretically, the peak voltage is 2x the applied. The second cause is due to the abrupt reduction of output short circuit current when the device turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the device output is shorted. Applications with large input inductance (for example, connecting the evaluation board to the bench power-supply through long cables) may require large input capacitance reduce the voltage overshoot from exceeding the absolute maximum voltage of the device. The fast current limit speed of the device to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1 µF to 22 µF adjacent to the device input aids in both speeding the response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5 V are permitted.

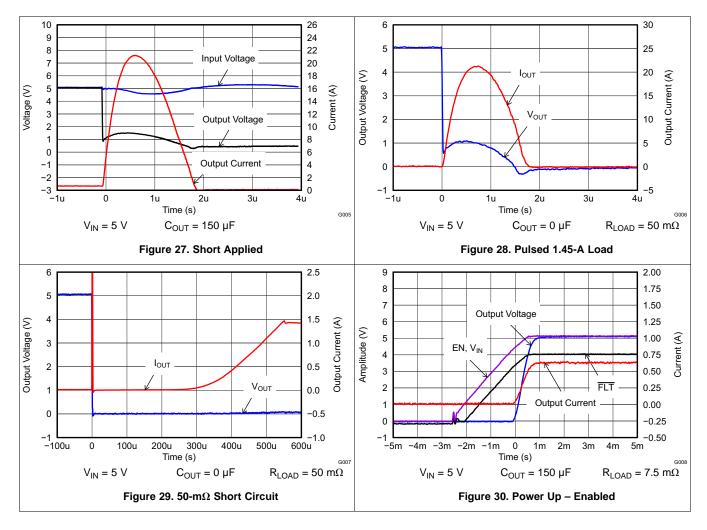
Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPS2065D has abruptly reduced OUT current. Energy stored in the inductance drives the OUT voltage down and potentially negative as it discharges. Applications with large output inductance (such as from a cable) benefit from use of a high-value output capacitor to control the voltage undershoot. When implementing USB standard applications, a 120 µF minimum output capacitance is required. Typically a 150-µF electrolytic capacitor is used, which is sufficient to control voltage undershoots. However, if the application does not require 120 µF of capacitance, and there is potential to drive the output negative, then TI recommends a minimum of 10-µF ceramic capacitance on the output. The voltage undershoot should be controlled to less than 1.5 V for 10 µs.

## 9.2.3 Application Curves



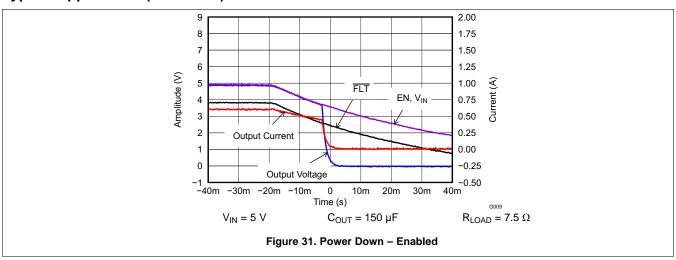
## **Typical Application (continued)**







# **Typical Application (continued)**



# 10 Power Supply Recommendations

Design of the devices is for operation from an input voltage supply range of 4.5 V to 5.5 V. The current capability of the power supply should exceed the maximum current limit of the power switch.

## 11 Layout

## 11.1 Layout Guidelines

- 1. Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low inductance trace.
- 2. Place at least 10-μF low ESR ceramic capacitor near the OUT and GND pins, and make the connections using a low inductance trace.
- 3. The PowerPAD™ should be directly connected to PCB ground plane using wide and short copper trace.

## 11.2 Layout Example

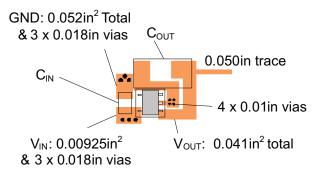


Figure 32. DBV Package PCB Layout Example

## 11.3 Power Dissipation and Junction Temperature

It is good design practice to estimate power dissipation and maximum expected junction temperature of the TPS2065D. The system designer can control choices of package, proximity to other power dissipating devices, and printed-circuit-board (PCB) design based on these calculations. These have a direct influence on maximum junction temperature. Other factors, such as airflow and maximum ambient temperature, are often determined by system considerations. It is important to remember that these calculations do not include the effects of adjacent heat sources, and enhanced or restricted air flow.

Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical. The lower junction temperatures achieved by soldering the pad improve the efficiency and reliability of both device parts and the system. The following examples were used to determine the  $\theta_{JA}$ Custom thermal impedances noted in *Thermal Information*. They were based on use of the JEDEC high-k circuit board construction (2 signal and 2 plane) with 4, 1-oz. copper weight, layers.

As shown in Equation 1, the following procedure requires iteration because power loss is due to the internal MOSFET  $I^2 \times R_{DS(ON)}$ , and  $R_{DS(ON)}$  is a function of the junction temperature. As an initial estimate, use the  $R_{DS(ON)}$  at 125°C from the *Typical Characteristics*, and the preferred package thermal resistance for the preferred board construction from the *Thermal Information* table.



# **Power Dissipation and Junction Temperature (continued)**

$$\mathsf{T}_\mathsf{J} = \mathsf{T}_\mathsf{A} + ((\mathsf{I}_\mathsf{OUT}^2 \times \mathsf{R}_\mathsf{DS(ON)}) \times \theta_\mathsf{JA})$$

where

- I<sub>OUT</sub> = rated OUT pin current (A)
- $R_{DS(ON)}$  = Power switch on-resistance at an assumed  $T_{J}(\Omega)$
- T<sub>A</sub> = Maximum ambient temperature (°C)
- T<sub>J</sub> = Maximum junction temperature (°C)
- $\theta_{JA}$  = Thermal resistance (°C/W)

(1)

If the calculated  $T_J$  is substantially different from the original assumption, estimate a new value of  $R_{DS(ON)}$  using the typical characteristic plot and recalculate.

If the resulting  $T_J$  is not less than 125°C, try a PCB construction and/or package with lower  $\theta_{JA}$ .

# 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

#### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

29-Nov-2025

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TPS2065DDBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	18OF
TPS2065DDBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	18OF
TPS2065DDBVR.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	18OF
TPS2065DDBVT	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	18OF
TPS2065DDBVT.A	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18OF
TPS2065DDBVT.B	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18OF

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

www.ti.com 29-Nov-2025

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 16-Oct-2024

## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2065DDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2065DDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2065DDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3



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## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2065DDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2065DDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2065DDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0



SMALL OUTLINE TRANSISTOR



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025