TPD2S017 2-Channel Ultra-Low Clamp Voltage ESD Solution With Series-Resistor Isolation

1 Features

- Ultra-low clamping voltage ensures the protection of ultra-low voltage core chipset during ESD events
- IEC 61000-4-2 ESD protection
- Matching of series resistor (R = 1 Ω) of ±8 mΩ (typical)
- Differential channel input capacitance matching of 0.02 pF (typical)
- High-speed data rate and EMI filter action at high frequencies (–3 dB bandwidth, ≠3 GHz)
- Available in 6-Pin small-outline transistor [SOT-23 (DBV)] package
- Easy straight-through routing packages

2 Applications

- Hi-speed USBs
- IEEE 1394 interfaces
- Low-voltage differential signaling (LVDS)
- Mobile display digital interfaces (MDDI) and mobile industry processor interfaces (MIPI)
- HS signals

3 Description

The TPD2S017 is a two channel electrostatic discharge (ESD) protection device. This protection product offers two-stage ESD transient voltage suppression (TVS) diodes in each line with a typically 1-Ω series resistor isolation. This architecture allows the device to clamp at a very low voltage during system level ESD strikes.

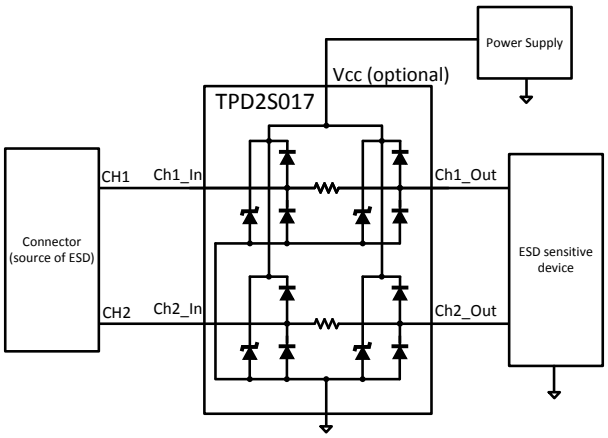
The TPD2S017 conforms to the IEC61000-4-2 ESD protection standard. Due to the series resistor component, the TPD2S017 provides a controlled filter roll-off for even greater spurious EMI suppression and signal integrity. The monolithic silicon technology allows good matching of the component values, including the clamp capacitances and the series resistors between the differential signal pairs. The tight matching of the line capacitance and series resistors ensures that the differential signal distortion due to added ESD clamp remains minimal, and it also allows the part to operate at high-speed differential data rate (in excess of 1.5 Gbps). The DBV package offers a flow-through pin mapping for ease of board layout.

Typical applications of this ESD protection device are circuit protection for USB data lines, IEEE 1394 Interfaces, LVDS, MDDI/MIPI and HS signals.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD2S017	DBV (SOT-23, 6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Application Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2015) to Revision C (Janurary 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the maximum IO voltage for V_{IO} from *5 V* to *6 V* in the *Absolute Maximum Ratings* section	4
• Updated the maximum operating voltage for V_{CC} from *5 V* to *5.5 V* in the *Recommended Operating Conditions* section	4

Changes from Revision A (July 2015) to Revision B (December 2015)	Page
• Added f = *10 MHz* to the test condition of *IO capacitance* in the *Electrical Characteristics* table	4

Changes from Revision * (September 2009) to Revision A (July 2015)	Page
• Added the *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

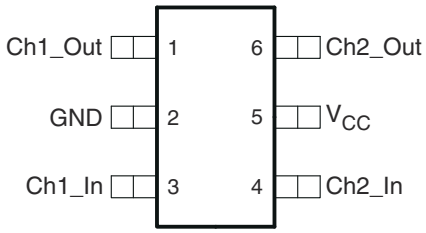


Figure 5-1. DBV Package
6-Pin SOT-23
Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Ch1_In	3	I	High-speed ESD clamp input
Ch2_In	4		
Ch1_Out	1	O	High-speed ESD clamp output
Ch2_Out	6		
GND	2	—	Ground
V_{CC}	5	—	Optional power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IO}	IO voltage	0	6	V
T_A	Operating temperature	–40	85	°C
T_{stg}	Storage temperature	–85	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±15000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		IEC 61000-4-2 Contact Discharge	±11000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A		–40		85	°C
Operating voltage	V_{CC}	0		5.5	V
	Ch1_In	0		V_{CC}	
	Ch2_In	0		V_{CC}	

6.4 Thermal Information

THERMAL METRIC(1)		TPD2S017 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	166.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	44.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R	Series resistor			1		Ω
I_{IO}	Current from I/O pins	V_{IO} = 3 V		0.01	0.1	µA

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔRS	Channel-to-channel resistance match	V_{IO} = 3 V		±8	±15	mΩ
V_D	Diode forward voltage for lower clamp	I_D = 8 mA	–0.6	–0.8	–0.95	V
R_{DYN}	Dynamic resistance (for I/O clamp)	I = 9 A		0.8		Ω
C_{IO}	IO capacitance	V_{IO} = 2.5 V; f = 10 MHz		1		pF
V_{BR}	Break-down voltage	I_O = 1 mA	11	12		V

6.6 Dissipation Ratings

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A \leq 25°C$	$T_A = 70°C$ POWER RATING
DBV	463.18 mW	–4.63 mW/C	254.75 mW

(1) Derating factor is defined as the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).

6.7 Typical Characteristics

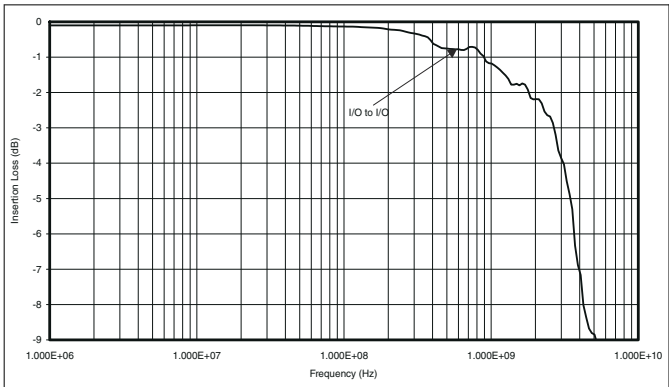


Figure 6-1. Insertion Loss Data (S21)

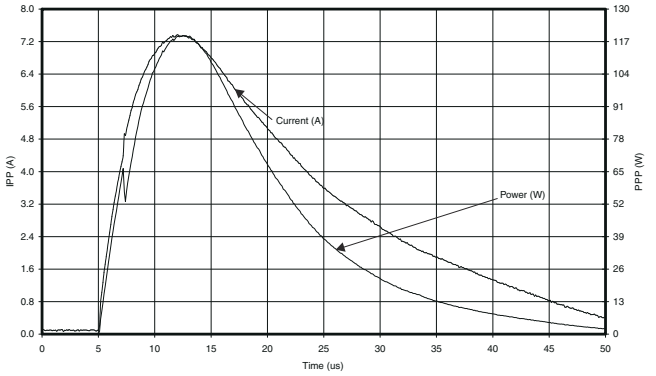


Figure 6-2. Peak Pulse Waveforms Ch1_Out, PUT with respect to GND, V_{CC} = 5 V

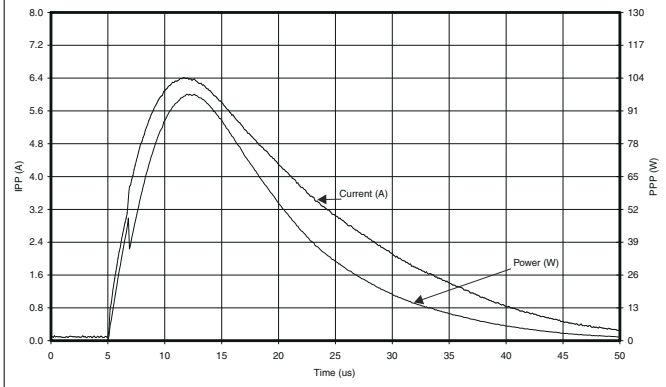


Figure 6-3. Peak Pulse Waveforms Ch2_In, PUT with respect to GND, V_{CC} = 5 V

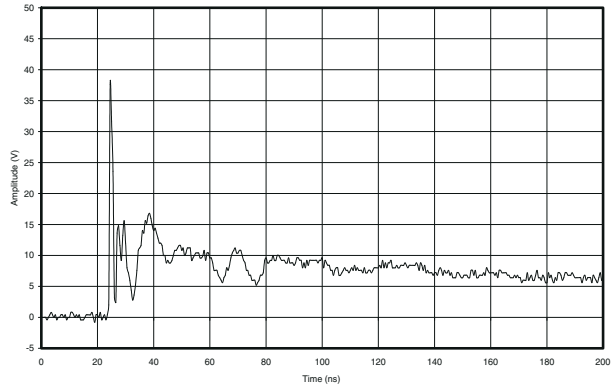


Figure 6-4. IEC Clamping Waveforms 8 kV Contact, 1 GHz Bandwidth

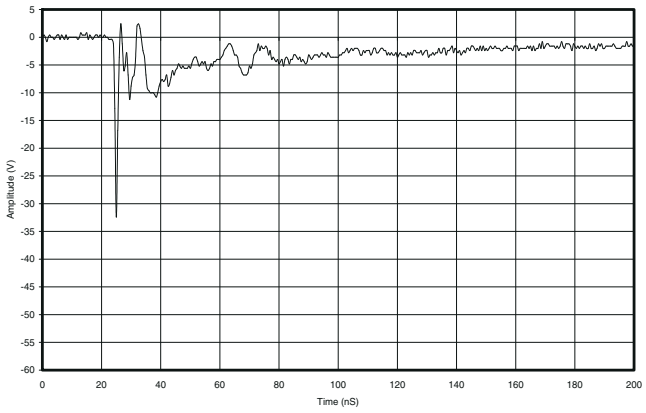


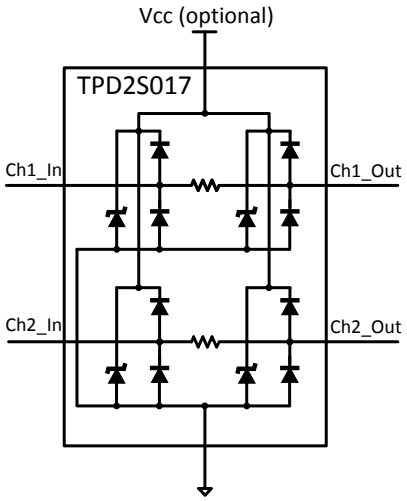
Figure 6-5. IEC Clamping Waveforms –8 kV Contact, 1 GHz Bandwidth

7 Detailed Description

7.1 Overview

The TPD2S017 is a two-channel ESD protection device. The two-stage ESD diodes and 1-Ω isolation resistor topology of the device gives the system very robust and good protection during ESD strikes. The TPD2S017 conforms to the IEC61000-4-2 ESD protection standard. The TPD2S017 provides a –3 dB frequency at almost 3 GHz which provides enough bandwidth for a vast majority of applications. Thanks to the monolithic silicon technology, the tight matching of the line capacitances and series resistances ensures a minimum distorted differential signal and a high operating differential data rate. The DBV package offers a flow-through pin mapping for ease of board layout.

7.2 Functional Block Diagram



7.3 Feature Description

Each channel of the TPD2S017 device has a topology of two-stage clamps with isolation resistor. This topology optimizes the clamping performance while supporting a high bandwidth. Due to the low clamping voltage, the down stream circuits that connect to the output of the channels are well-protected. The high IEC 61000-4-2 level ensures the system's robustness during the ESD events. The good matching of the resistor and capacitance values will yield minimal distortion of the signals. The low resistance and capacitance values make sure that this device supports a high differential data rate. The flow-through pinout ensures no additional layout burden on the printed circuit board (PCB).

7.4 Device Functional Modes

The TPD2S017 device stays passive and has low leakage during normal operation when the voltage at the input of each channel is from 0 V to V_{CC} and activates when that voltage exceeds one forward diode drop above V_{CC} or below ground. During IEC ESD events, contact transient voltages as high as ±11 kV can be suppressed. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

When a system contains a human interface connector, it becomes vulnerable to large system-level ESD strikes that standard ICs cannot survive. Protection products are typically used to suppress ESD at these connectors. TPD2S017 is a two-channel ESD protection device. In each channel, it contains two-stage TVS diodes and a resistor between the two clamping stages as an isolation. This implementation provides good clamping performance, minimal signal distortion and the support of high data speed.

8.2 Typical Application

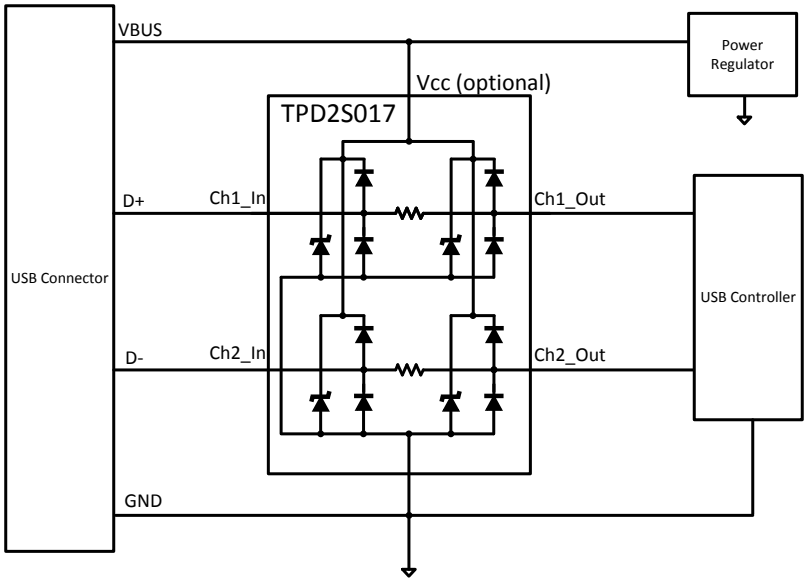


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, a TPD2S017 will be used to protect the USB 2.0 high-speed data lines. The following system parameters are known.

Table 8-1. Design Parameters

DESIGN PARAMETER	VALUE
High-speed mode high-level output voltage	400 mV ±10%
High-speed mode low-level output voltage	0 V ± 10 mV
USB 2.0 high-speed data rate	480 Mbps
Required IEC 61000-4-2 ESD Protection	±8 kV Contact

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer should make sure:

- Voltage range on the protected lines must not go beyond one forward diode drop above the V_{CC} and must no go below one forward diode drop below the ground.
- Operating frequency is supported by the IO capacitance C_{IO}.
- IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode.

For this application, a high speed USB 2.0 signal that ranges from –10 mV to 440 mV will be applied to each line. Connect a 5 V power supply to V_{CC} pin; therefore, the signal will not fall outside of the normal operation range and the TPD2S017 will stay passive and low leakage during normal operation.

Next, consider the data rate of this signal and ensure that the TVS I/O capacitance will not distort this signal by filtering it. The speed of a USB 2.0 high-speed signal is 480 Mbit/s. With TPD2S017's ultra low IO capacitance, this device can support 1.5 Gbit/s data rate and thus can pass USB 2.0 high-speed signal with minimal distortion.

Finally, TPD2S017 is rated for the IEC 61000-4-2 (Level 4) so it provides sufficient system-level ESD protection to the human interface in this application. See *Section 10.2* for instructions on properly laying out TPD2S017.

8.2.3 Application Curves

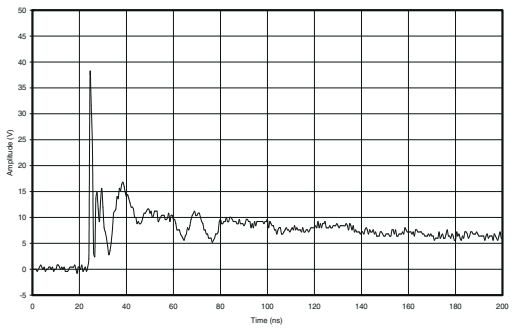


Figure 8-2. IEC Clamping Waveforms 8 kV Contact, 1 GHz Bandwidth

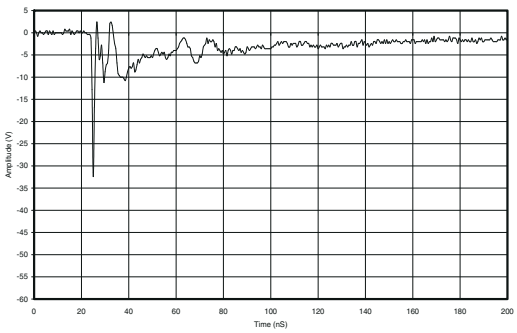


Figure 8-3. IEC Clamping Waveforms −8 kV Contact, 1 GHz Bandwidth

9 Power Supply Recommendations

The optional V_{CC} power supply bias is recommended to lower the I/O capacitances. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- Use thick and short traces for the power and ground paths.
- Run differential signal lines in pair with small distance to optimize signal integrity.

10.2 Layout Example

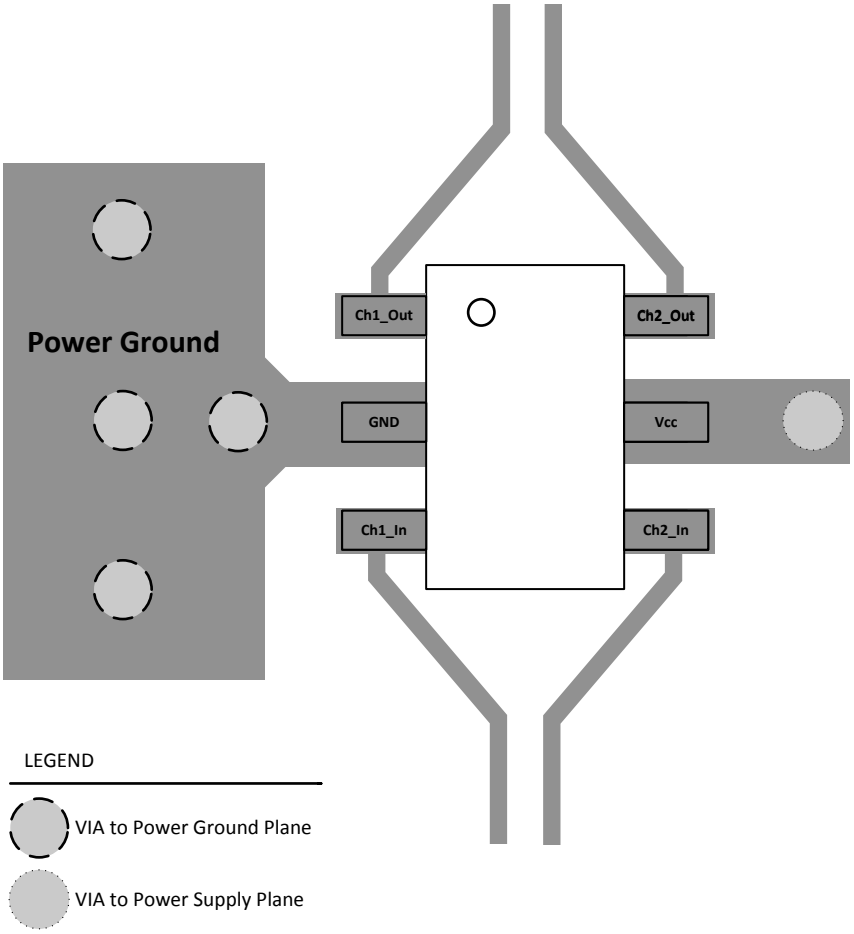


Figure 10-1. Layout Recommendation

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD2S017DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	NFT
TPD2S017DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	NFT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

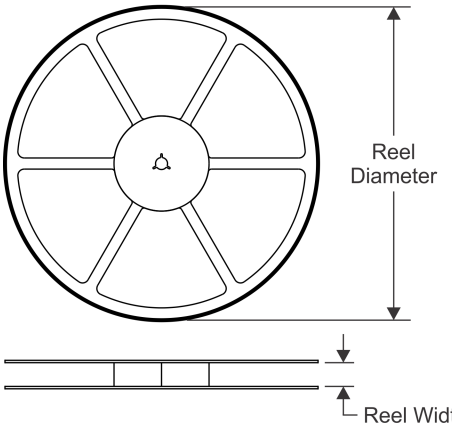
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

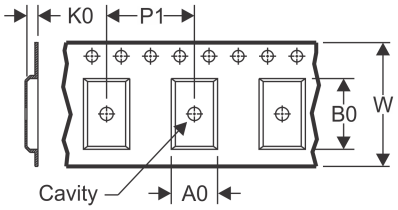
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

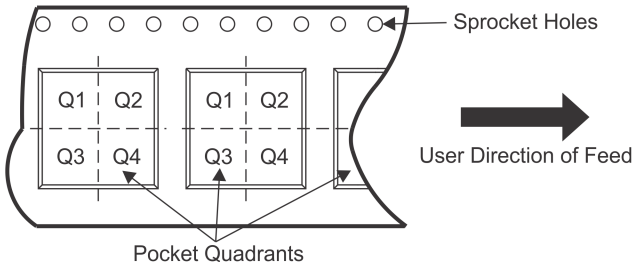


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

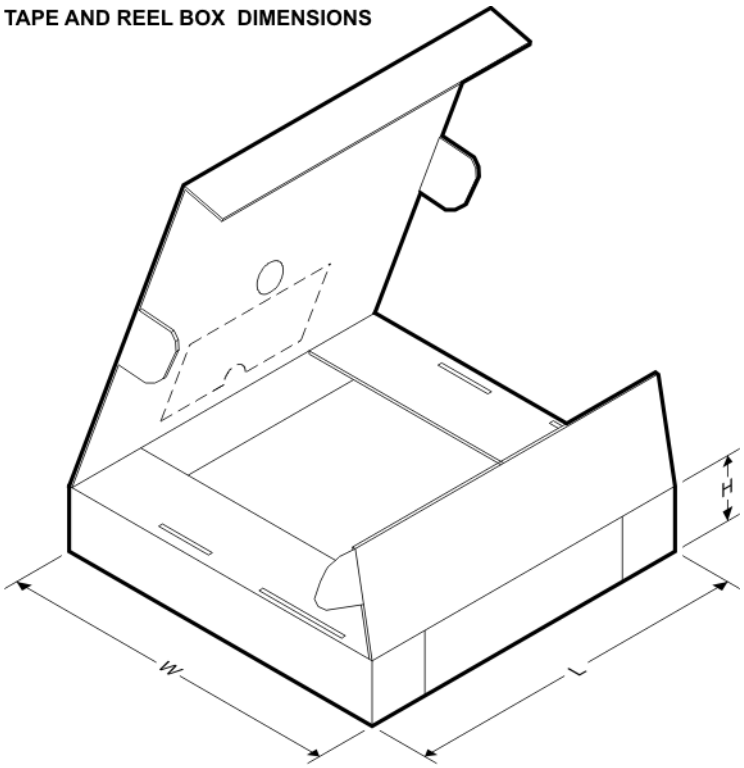
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2S017DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

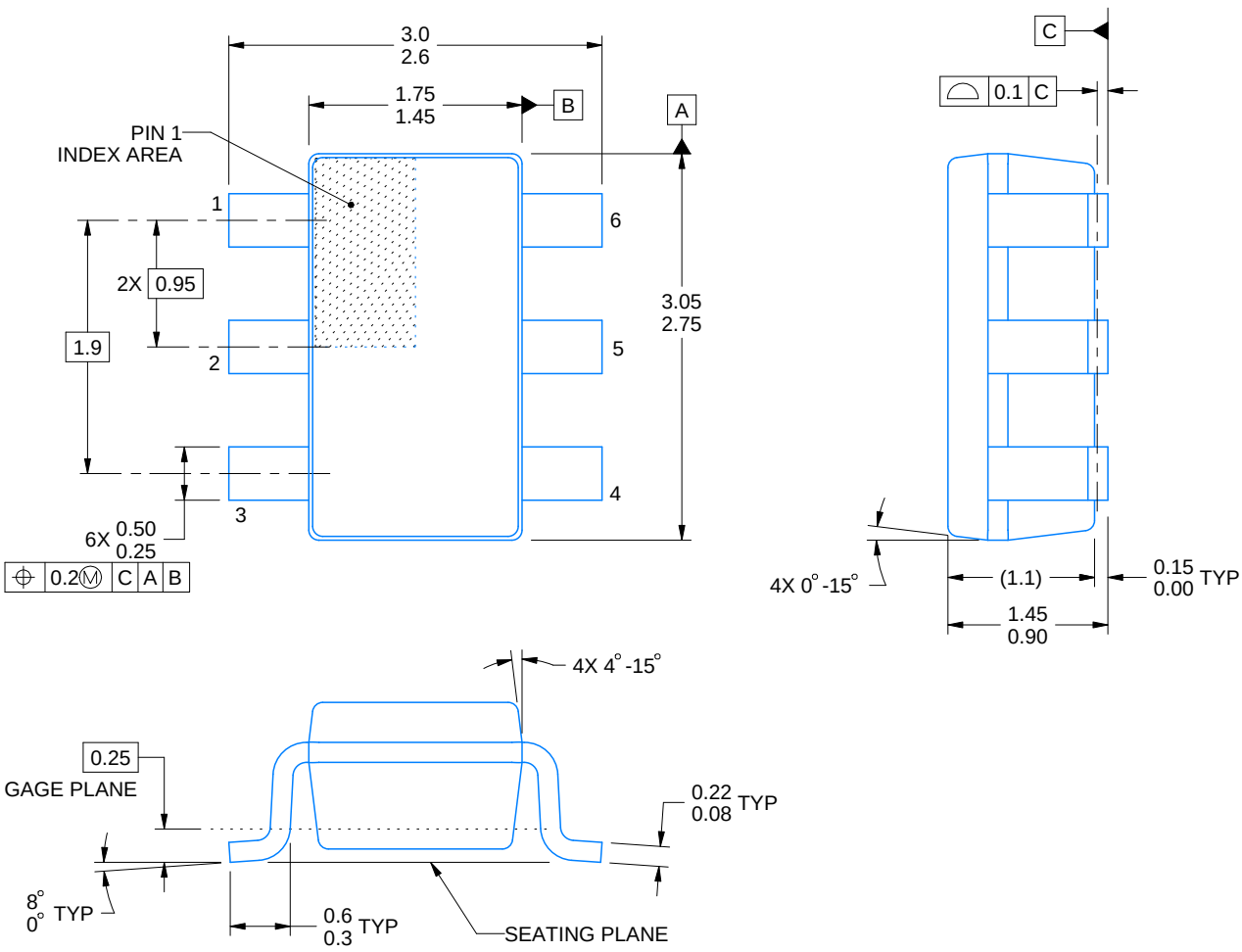
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2S017DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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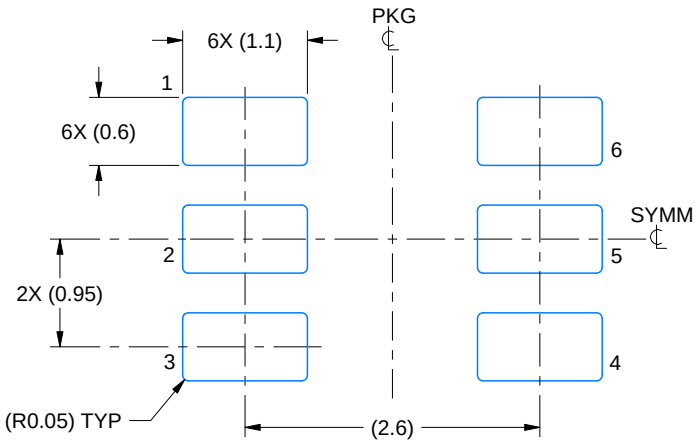
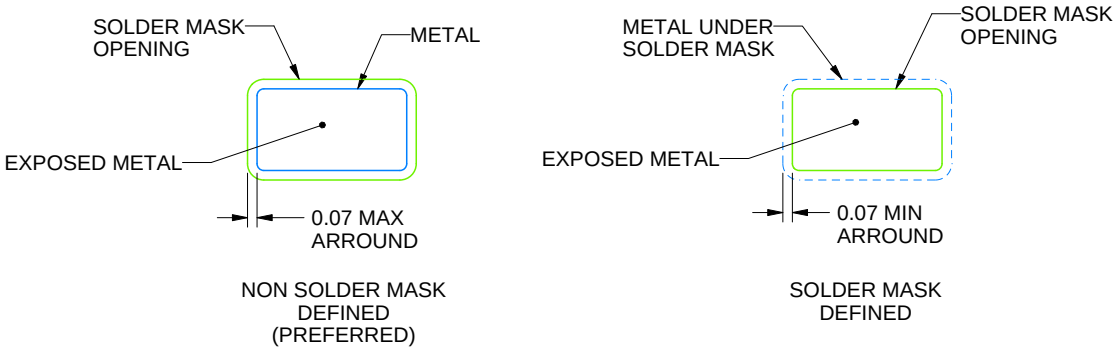
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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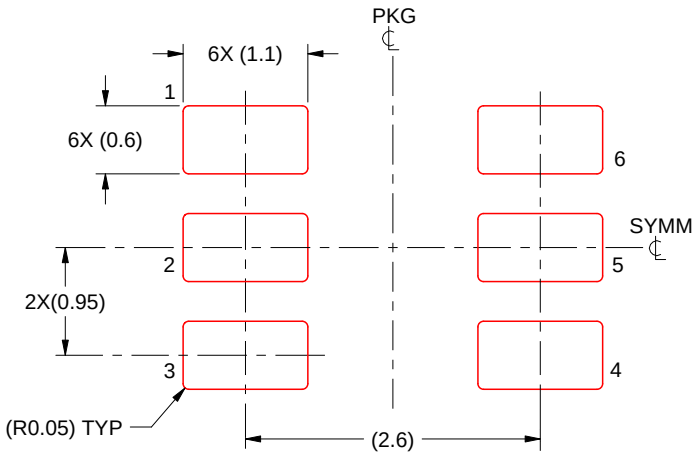
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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