

# TPD1S514x Family USB Charger Overvoltage, Surge and ESD Protection for $V_{BUS}$ PIN

## 1 Features

- Overvoltage Protection at  $V_{BUS\_CON}$  up to 30-V DC
- Precision OVP ( $< \pm 1\%$  Tolerance)
- Low  $R_{ON}$  nFET Switch Supports Host and Charging Mode
- Dedicated  $V_{BUS\_POWER}$  Pin Offers Flexible Power up Options Under Dead Battery Condition
- Transient Protection for  $V_{BUS}$  Line:
  - IEC 61000-4-2 Contact Discharge  $\pm 15$  kV
  - IEC 61000-4-2 Air Gap Discharge  $\pm 15$  kV
  - IEC 61000-4-5 Open Circuit Voltage 100 V
    - Precision Clamp Circuit Limits the  $V_{BUS\_SYS}$  Voltage  $< V_{OVP}$
- USB Inrush Current Compliant
- Thermal Shutdown (TSD) Feature

## 2 Applications

- Cell Phones
- Tablets
- eBook
- Portable Media Players
- 5-V, 9-V, and 12-V Power Rails

## 3 Description

The TPD1S514 Family consists of single-chip protection solutions for 5-V, 9-V or 12-V USB  $V_{BUS}$  lines, or other power buses. The bidirectional nFET switch ensures safe current flow in both charging and host mode while protecting the internal system circuits from any over voltage condition at the  $V_{BUS\_CON}$  pin. On the  $V_{BUS\_CON}$  pin, this device can handle over voltage protection up to 30-V DC. After the EN pin toggles low, any device in the TPD1S514 Family waits 20 ms before turning ON the nFET through a soft start delay.

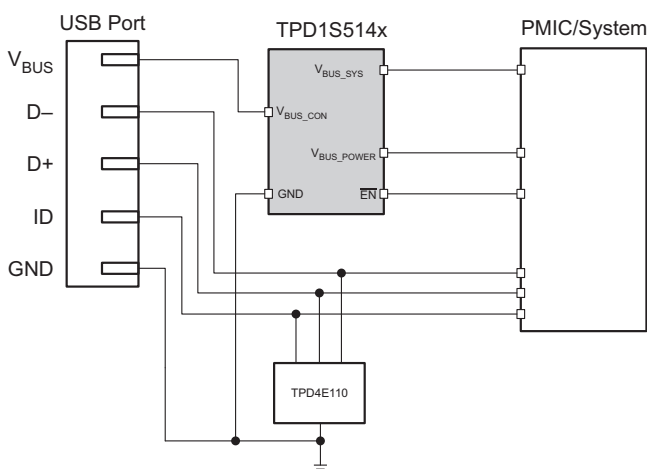
Typical application interfaces for the TPD1S514 Family are  $V_{BUS}$  lines in USB connectors typically found in cell phones, tablets, eBooks, and portable media players. The TPD1S514 Family can also be applied to any system using an interface for a 5-V, 9-V, or 12-V power rail.

### Device Information<sup>(1)</sup>

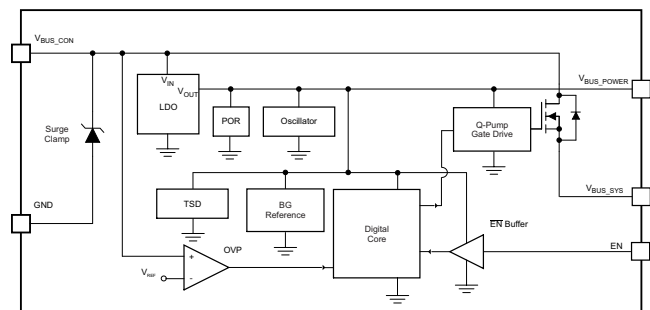
| DEVICE NAME | PACKAGE   | BODY SIZE (NOM)   |
|-------------|-----------|-------------------|
| TPD1S514x   | WCSP (12) | 1.29 mm × 1.99 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### TPD1S514 Family Circuit Protection Scheme



### TPD1S514 Family Block Diagram



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (October 2015) to Revision F                                                          | Page |
|---------------------------------------------------------------------------------------------------------------|------|
| • Changed $\text{I}_{\text{POWER}}$ from 1 mA to 10 mA in the <a href="#">Absolute Maximum Ratings</a> table. | 5    |

| Changes from Revision D (July 2015) to Revision E                                                                                       | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------|------|
| • Removed Preview status of TPD1S514-3.                                                                                                 | 1    |
| • Changed Max value of $\text{I}_{\text{VBUS\_SLEEP}}$ PARAMETER for TPD1S514-3 (Preview) from 308 $\mu\text{A}$ to 335 $\mu\text{A}$ . | 6    |
| • Updated TEST CONDITIONS for $\text{T}_{\text{OFF\_DELAY}}$ PARAMETER.                                                                 | 9    |

| Changes from Revision C (July 2015) to Revision D | Page |
|---------------------------------------------------|------|
| • Added TPD1S514 and TPD1S514-3 (Preview)         | 1    |

| Changes from Revision B (September 2014) to Revision C       | Page |
|--------------------------------------------------------------|------|
| • Removed Previewed TPD1S514-3 and Programmability Features. | 1    |

| Changes from Revision A (July 2014) to Revision B | Page |
|---------------------------------------------------|------|
| • Changed Body size to fix rounding error.        | 1    |

| Changes from Original (April 2014) to Revision A        | Page |
|---------------------------------------------------------|------|
| • Removed Preview status of TPD1S514-2.                 | 1    |
| • Updated Device Comparison table.                      | 4    |
| • Updated Electrical Characteristics OVP Circuit table. | 8    |

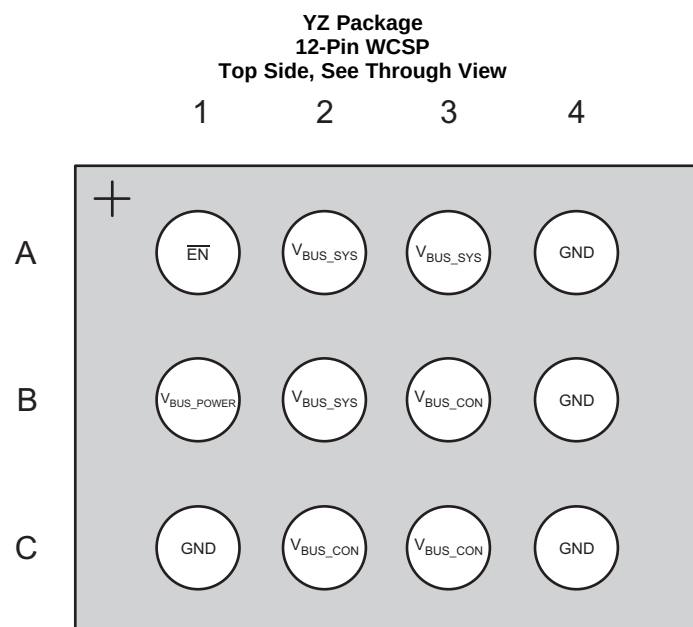


## 5 Device Comparison Table

| TPD1S514 Family | V <sub>OVP</sub> (V) |       |       | V <sub>OVP, HYS</sub> (mV) | V <sub>BUS_POWER</sub> (V) <sup>(1)</sup> |      | T <sub>Startup delay</sub> (ms) options | T <sub>Soft Start</sub> (ms) options |
|-----------------|----------------------|-------|-------|----------------------------|-------------------------------------------|------|-----------------------------------------|--------------------------------------|
|                 | MIN                  | TYP   | MAX   | TYP                        | MIN                                       | TYP  | TYP                                     | TYP                                  |
| TPD1S514-1      | 5.9                  | 5.95  | 5.99  | 100                        | 4.7                                       | 4.95 | 20                                      | 3.5                                  |
| TPD1S514-2      | 9.9                  | 9.98  | 10.05 | 100                        | 4.7                                       | 4.95 |                                         |                                      |
| TPD1S514-3      | 13.5                 | 13.75 | 14    | 100                        | 4.7                                       | 4.95 |                                         |                                      |
| TPD1S514        | 5.9                  | 5.95  | 5.99  | 20                         | 6.2                                       | 6.48 |                                         |                                      |

(1) With V<sub>BUS\_CON</sub> > 6.5V. See Sections [V<sub>BUS\\_POWER</sub>](#), [TPD1S514-1](#), [TPD1S514-2](#), [TPD1S514-3](#) and [V<sub>BUS\\_POWER</sub>](#), [TPD1S514](#) for full description.

## 6 Pin Configuration and Functions



**Pin Functions**

| PIN                    |                | I/O | DESCRIPTION                                                                                                                              |
|------------------------|----------------|-----|------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                   | NO.            |     |                                                                                                                                          |
| $\overline{\text{EN}}$ | A1             | I   | Enable Active-Low Input. Drive $\overline{\text{EN}}$ low to enable the switch. Drive $\overline{\text{EN}}$ high to disable the switch. |
| V <sub>BUS_POWER</sub> | B1             | O   | 5-V Power source controlled by V <sub>BUS_CON</sub> .                                                                                    |
| V <sub>BUS_SYS</sub>   | A2, A3, B2     | I/O | Connect to internal VBUS plane.                                                                                                          |
| V <sub>BUS_CON</sub>   | B3, C2, C3     | I/O | Connect to USB connector VBUS pin; IEC 61000-4-2 ESD protection and IEC 61000-4-5 Surge protection.                                      |
| GND                    | A4, B4, C1, C4 | G   | Connect to PCB ground plane.                                                                                                             |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

|                        |                                                                                          |                            | MIN  | MAX                | UNIT |
|------------------------|------------------------------------------------------------------------------------------|----------------------------|------|--------------------|------|
| V <sub>BUS_CON</sub>   | Supply voltage from USB connector                                                        |                            | −0.3 | 30                 | V    |
| V <sub>BUS_SYS</sub>   | Internal Supply DC voltage Rail on the PCB                                               |                            | −0.3 | 20                 | V    |
| I <sub>BUS</sub>       | Continuous input current on V <sub>BUS_CON</sub> pin <sup>(3)</sup>                      |                            |      | 3.5                | A    |
| I <sub>OUT</sub>       | Continuous output current on V <sub>BUS_CON</sub> pin <sup>(3)</sup>                     |                            |      | 3.5                | A    |
| I <sub>PEAK</sub>      | Peak Input and Output Current on V <sub>BUS_CON</sub> , V <sub>BUS_SYS</sub> pin (10 ms) |                            |      | 8                  | A    |
| I <sub>DIODE</sub>     | Continuous forward current through the FET body diode                                    |                            |      | 1                  | A    |
| I <sub>POWER</sub>     | Continuous current through V <sub>BUS_POWER</sub>                                        |                            |      | 10                 | mA   |
| V <sub>EN</sub>        | Voltage on Input pin ( $\overline{\text{EN}}$ )                                          |                            |      | 7                  | V    |
| V <sub>BUS_POWER</sub> | Continuous Voltage at V <sub>BUS_POWER</sub>                                             | TPD1S514-1                 |      | See <sup>(4)</sup> | V    |
|                        |                                                                                          | TPD1S514-2                 |      | See <sup>(4)</sup> |      |
|                        |                                                                                          | TPD1S514-3                 |      | See <sup>(4)</sup> |      |
|                        |                                                                                          | TPD1S514                   |      | See <sup>(4)</sup> |      |
|                        | IEC 61000-4-5 open circuit voltage (t <sub>p</sub> = 1.2/50 μs)                          | V <sub>BUS_CON</sub> pin   |      | 100                | V    |
|                        | IEC 61000-4-5 peak pulse current (t <sub>p</sub> = 8/20μs)                               | V <sub>BUS_CON</sub> pin   |      | 30                 | A    |
|                        | IEC 61000-4-5 peak pulse power (t <sub>p</sub> = 8/20μs)                                 | V <sub>BUS_CON</sub> pin   |      | 900                | W    |
| C <sub>LOAD</sub>      | Output load capacitance                                                                  | V <sub>BUS_SYS</sub> pin   | 0.1  | 100                | μF   |
| C <sub>CON</sub>       | Input capacitance                                                                        | V <sub>BUS_CON</sub> pin   | 0.1  | 50                 | μF   |
| C <sub>POW</sub>       | V <sub>BUS_POWER</sub> capacitance                                                       | V <sub>BUS_POWER</sub> pin | 0.1  | 4.7                | μF   |
| T <sub>A</sub>         | Operating free air temperature                                                           |                            | −40  | 85                 | °C   |
| T <sub>stg</sub>       | Storage temperature                                                                      |                            | −65  | 150                | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) Thermal limits and power dissipation limits must be observed.
- (4) 6.9 V or V<sub>BUS\_CON</sub> + 0.3 V, whichever is smaller.

### 7.2 ESD Ratings

|                    |                         |                                                                                | VALUE  | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|--------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000  | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500   |      |
|                    |                         | IEC 61000-4-2 Contact Discharge                                                | ±15000 |      |
|                    |                         | IEC 61000-4-2 Air-gap Discharge                                                | ±15000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                      |                                            |                            | MIN | NOM | MAX  | UNIT |
|----------------------|--------------------------------------------|----------------------------|-----|-----|------|------|
| V <sub>BUS_CON</sub> | Supply voltage from USB connector          | TPD1S514-1                 | 3.5 | 5   | 5.9  | V    |
|                      |                                            | TPD1S514-2                 | 3.5 | 9   | 9.9  |      |
|                      |                                            | TPD1S514-3                 | 3.5 | 12  | 13.5 |      |
|                      |                                            | TPD1S514                   | 3.5 | 5   | 5.9  |      |
| V <sub>BUS_SYS</sub> | Internal Supply DC voltage Rail on the PCB | TPD1S514-1                 | 3.9 | 5   | 5.9  | V    |
|                      |                                            | TPD1S514-2                 | 3.9 | 9   | 9.9  |      |
|                      |                                            | TPD1S514-3                 | 3.9 | 12  | 13.5 |      |
|                      |                                            | TPD1S514                   | 3.9 | 5   | 5.9  |      |
| C <sub>LOAD</sub>    | Output load capacitance                    | V <sub>BUS_SYS</sub> pin   |     | 2.2 |      | μF   |
| C <sub>CON</sub>     | Input capacitance                          | V <sub>BUS_CON</sub> pin   |     | 1   |      | μF   |
| C <sub>POWER</sub>   | Capacitance on V <sub>BUS_POWER</sub>      | V <sub>BUS_POWER</sub> pin |     | 1   |      | μF   |
| T <sub>A</sub>       | Operating free-air temperature             |                            | –40 |     | 85   | °C   |

## 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TPD1S514 Family | UNIT |
|-------------------------------|----------------------------------------------|-----------------|------|
|                               |                                              | YZ (WCSP)       |      |
|                               |                                              | 12 PINS         |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 89              | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 0.6             | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 16.3            | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 2.7             | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 16.2            | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Supply Current Consumption

over operating free-air temperature range (unless otherwise noted)

| PARAMETER               |                                                    | TEST CONDITIONS                                                             |                             | DEVICE NAME | TYP | MAX | UNIT |
|-------------------------|----------------------------------------------------|-----------------------------------------------------------------------------|-----------------------------|-------------|-----|-----|------|
| I <sub>VBUS_SLEEP</sub> | V <sub>BUS_CON</sub> Operating Current Consumption | Measured at V <sub>BUS_CON</sub> pin, EN = 5 V                              | V <sub>BUS_CON</sub> = 5 V  | TPD1S514-1  | 150 | 245 | μA   |
|                         |                                                    |                                                                             | V <sub>BUS_CON</sub> = 9 V  | TPD1S514-2  | 176 | 281 |      |
|                         |                                                    |                                                                             | V <sub>BUS_CON</sub> = 12 V | TPD1S514-3  | 195 | 335 |      |
|                         |                                                    |                                                                             | V <sub>BUS_CON</sub> = 5 V  | TPD1S514    | 150 | 245 |      |
| I <sub>VBUS</sub>       |                                                    | Measured at V <sub>BUS_CON</sub> pin, EN = 0 V and no load                  | V <sub>BUS_CON</sub> = 5 V  | TPD1S514-1  | 228 | 354 | μA   |
|                         |                                                    |                                                                             | V <sub>BUS_CON</sub> = 9 V  | TPD1S514-2  | 250 | 413 |      |
|                         |                                                    |                                                                             | V <sub>BUS_CON</sub> = 12 V | TPD1S514-3  | 270 | 456 |      |
|                         |                                                    |                                                                             | V <sub>BUS_CON</sub> = 5 V  | TPD1S514    | 228 | 354 |      |
| I <sub>VBUS_SYS</sub>   | V <sub>BUS_SYS</sub> operating current consumption | Measured at V <sub>BUS_SYS</sub> pin, V <sub>BUS_CON</sub> = Hi-Z, EN = 0 V | V <sub>BUS_SYS</sub> = 5 V  | TPD1S514-1  | 210 | 354 | μA   |
|                         |                                                    |                                                                             | V <sub>BUS_SYS</sub> = 9 V  | TPD1S514-2  | 250 | 424 |      |
|                         |                                                    |                                                                             | V <sub>BUS_SYS</sub> = 12 V | TPD1S514-3  | 333 | 461 |      |
|                         |                                                    |                                                                             | V <sub>BUS_SYS</sub> = 5 V  | TPD1S514    | 210 | 354 |      |
| I <sub>HOST_LEAK</sub>  | Host mode leakage current                          | Measured at V <sub>BUS_SYS</sub> pin, V <sub>BUS_CON</sub> = Hi-Z, EN = 5 V | V <sub>BUS_SYS</sub> = 5 V  | TPD1S514-1  | 90  | 218 | μA   |
|                         |                                                    |                                                                             | V <sub>BUS_SYS</sub> = 9 V  | TPD1S514-2  | 290 | 491 |      |
|                         |                                                    |                                                                             | V <sub>BUS_SYS</sub> = 12 V | TPD1S514-3  | 506 | 696 |      |
|                         |                                                    |                                                                             | V <sub>BUS_SYS</sub> = 5 V  | TPD1S514    | 90  | 218 |      |

## 7.6 Electrical Characteristics $\overline{\text{EN}}$ Pin

over operating free-air temperature range (unless otherwise noted)

| PARAMETER |                          |                        | TEST CONDITIONS                                                       | MIN | TYP | MAX | UNIT          |
|-----------|--------------------------|------------------------|-----------------------------------------------------------------------|-----|-----|-----|---------------|
| $V_{IH}$  | High-level input voltage | $\overline{\text{EN}}$ | $V_{BUS\_CON} = 5\text{ V}$                                           | 1.2 |     | 6   | V             |
| $V_{IL}$  | Low-level input voltage  | $\overline{\text{EN}}$ | $V_{BUS\_CON} = 5\text{ V}$                                           | 0   |     | 0.8 | V             |
| $I_{IL}$  | Input leakage current    | $\overline{\text{EN}}$ | $V_{\overline{\text{EN}}} = 0\text{ V}$ , $V_{BUS\_CON} = 5\text{ V}$ |     |     | 1   | $\mu\text{A}$ |
| $I_{IH}$  | Input leakage current    | $\overline{\text{EN}}$ | $V_{\overline{\text{EN}}} = 5\text{ V}$ , $V_{BUS\_CON} = 5\text{ V}$ |     |     | 10  | $\mu\text{A}$ |

## 7.7 Thermal Shutdown Feature

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                   |                  | TEST CONDITIONS                                                                                                                                                 | MIN | TYP | MAX | UNIT               |
|-----------------------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|--------------------|
| $T_{SHDN}$                  | Thermal shutdown | $V_{BUS\_CON} = 5\text{ V}$ , $\overline{\text{EN}} = 0\text{ V}$ , Junction temperature decreases from thermal shutdown level until the nFET switch turns off. |     | 145 |     | $^{\circ}\text{C}$ |
| Thermal shutdown hysteresis |                  | $V_{BUS\_CON} = 5\text{ V}$ , $\overline{\text{EN}} = 0\text{ V}$ , Junction temperature decreases from thermal shutdown level until the nFET switch turns on.  |     | 25  |     | $^{\circ}\text{C}$ |

## 7.8 Electrical Characteristics nFET Switch

$T = 25^{\circ}\text{C}$

| PARAMETER |                      | TEST CONDITIONS                                       |            | MIN | TYP | MAX | UNIT             |
|-----------|----------------------|-------------------------------------------------------|------------|-----|-----|-----|------------------|
| $R_{ON}$  | Switch ON resistance | $V_{BUS\_CON} = 5\text{ V}$ , $I_{OUT} = 1\text{ A}$  | TPD1S514-1 |     | 39  | 50  | $\text{m}\Omega$ |
|           |                      | $V_{BUS\_CON} = 9\text{ V}$ , $I_{OUT} = 1\text{ A}$  | TPD1S514-2 |     | 39  | 50  |                  |
|           |                      | $V_{BUS\_CON} = 12\text{ V}$ , $I_{OUT} = 1\text{ A}$ | TPD1S514-3 |     | 39  | 50  |                  |
|           |                      | $V_{BUS\_CON} = 5\text{ V}$ , $I_{OUT} = 1\text{ A}$  | TPD1S514   |     | 39  | 50  |                  |

## 7.9 Electrical Characteristics OVP Circuit

T = 25°C

| PARAMETER                     |                                           | TEST CONDITIONS      |                                                                               | MIN        | TYP  | MAX   | UNIT  |    |
|-------------------------------|-------------------------------------------|----------------------|-------------------------------------------------------------------------------|------------|------|-------|-------|----|
| V <sub>OVP</sub>              | Input voltage protection threshold        | V <sub>BUS_CON</sub> | V <sub>BUS_CON</sub> increasing from 0 V to 20 V                              | TPD1S514-1 | 5.90 | 5.95  | 5.99  | V  |
|                               |                                           |                      |                                                                               | TPD1S514-2 | 9.9  | 9.98  | 10.05 |    |
|                               |                                           |                      |                                                                               | TPD1S514-3 | 13.5 | 13.75 | 14    |    |
|                               |                                           |                      |                                                                               | TPD1S514   | 5.90 | 5.95  | 5.99  |    |
| V <sub>HYS_OVP</sub>          | Hysteresis on OVP                         | V <sub>BUS_CON</sub> | V <sub>BUS_CON</sub> decreasing from 20 V to 0 V                              | TPD1S514-1 |      | 100   | mV    |    |
|                               |                                           |                      |                                                                               | TPD1S514-2 |      | 100   |       |    |
|                               |                                           |                      |                                                                               | TPD1S514-3 |      | 100   |       |    |
|                               |                                           |                      |                                                                               | TPD1S514   |      | 20    |       |    |
| V <sub>UVLO</sub>             | Input under voltage lockout               | V <sub>BUS_CON</sub> | V <sub>BUS_CON</sub> voltage rising from 0 V to 5 V                           |            | 2.7  | 3.1   | 3.5   | V  |
| V <sub>HYS_UVLO</sub>         | Hysteresis on UVLO                        | V <sub>BUS_CON</sub> | Difference between rising and falling UVLO thresholds                         |            |      | 80    |       | mV |
| V <sub>UVLO_FALLING</sub>     | Input undervoltage lockout                | V <sub>BUS_CON</sub> | V <sub>BUS_CON</sub> voltage falling from 5 V to 0 V                          |            | 2.6  | 3.0   | 3.4   | V  |
| V <sub>UVLO_SYS</sub>         | V <sub>BUS_SYS</sub> undervoltage lockout | V <sub>BUS_SYS</sub> | V <sub>BUS_SYS</sub> voltage rising from 0 V to 5 V                           |            | 2.8  | 3.7   | 4.3   | V  |
| V <sub>HYS_UVLO_SYS</sub>     | V <sub>BUS_SYS</sub> UVLO Hysteresis      | V <sub>BUS_SYS</sub> | Difference between rising and falling UVLO thresholds on V <sub>BUS_SYS</sub> |            |      | 500   |       | mV |
| V <sub>UVLO_SYS_FALLING</sub> | V <sub>BUS_SYS</sub> undervoltage lockout | V <sub>BUS_SYS</sub> | V <sub>BUS_SYS</sub> voltage falling from 5 V to 0 V                          |            | 2.6  | 3.0   | 3.4   | V  |

## 7.10 Electrical Characteristics $V_{BUS\_POWER}$ Circuit

over operating free-air temperature range (unless otherwise noted)

| PARAMETER             |                                                            | TEST CONDITIONS                                                   |            | MIN | TYP  | MAX  | UNIT |
|-----------------------|------------------------------------------------------------|-------------------------------------------------------------------|------------|-----|------|------|------|
| $V_{CLAMP}$           | Output voltage on $V_{BUS\_POWER}$ during OVP              | $V_{BUS\_CON} = 20\text{ V}$                                      | TPD1S514-1 |     | 5.0  | 5.5  | V    |
|                       |                                                            |                                                                   | TPD1S514-2 |     | 5.0  | 5.5  |      |
|                       |                                                            |                                                                   | TPD1S514-3 |     | 5.0  | 5.5  |      |
|                       |                                                            |                                                                   | TPD1S514   |     | 6.48 | 6.68 |      |
| $V_{BUS\_POWER}$      | Output voltage on $V_{BUS\_POWER}$ during normal operation | $V_{BUS\_CON} = 5\text{ V}$ ,<br>$I_{BUS\_POWER} = 1\text{ mA}$ ; | TPD1S514-1 |     | 4.7  | 4.95 | V    |
|                       |                                                            |                                                                   | TPD1S514-2 |     | 4.7  | 4.95 |      |
|                       |                                                            |                                                                   | TPD1S514-3 |     | 4.7  | 4.95 |      |
|                       |                                                            |                                                                   | TPD1S514   |     | 4.7  | 4.98 |      |
| $I_{BUS\_POWER\_MAX}$ | Output current on $V_{BUS\_POWER}$                         | $V_{BUS\_CON} = 5\text{ V} - 15\text{ V}$                         |            |     |      | 3    | mA   |

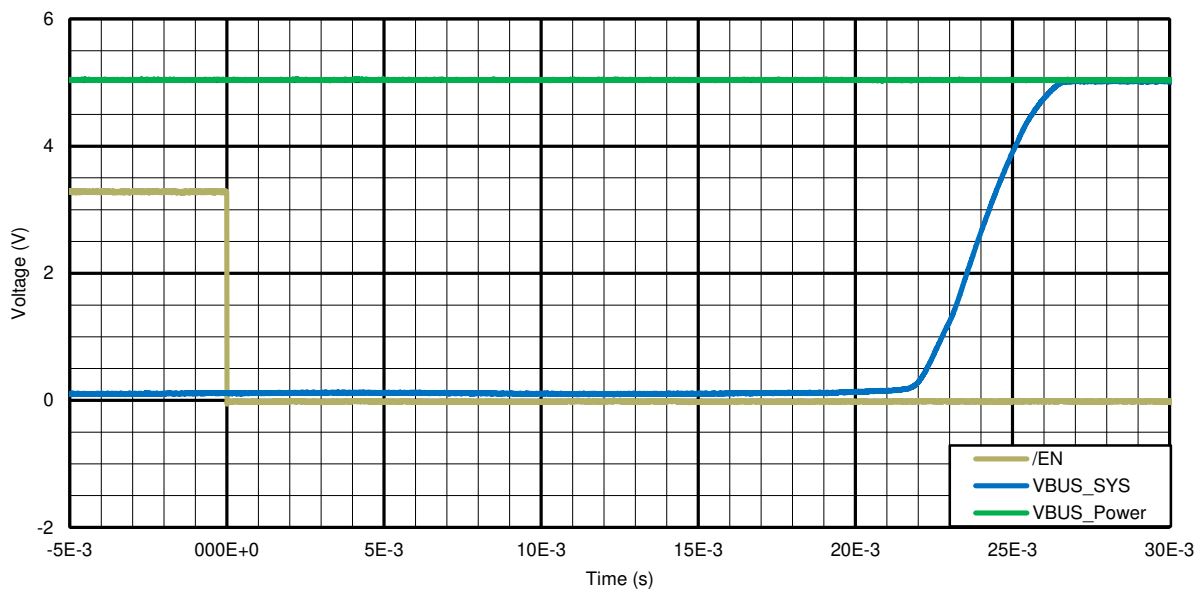


## 7.11 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                 |                                           | TEST CONDITIONS                                                                                                                                                          |            | MIN | TYP | MAX | UNIT |
|---------------------------|-------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|-----|-----|------|
| t <sub>DELAY</sub>        | USB charging turn-ON Delay                | Measured from $\overline{\text{EN}}$ asserted LOW to nFET begins to Turn ON, excludes soft-start time                                                                    | TPD1S514-1 | 20  |     |     | ms   |
|                           |                                           |                                                                                                                                                                          | TPD1S514-2 |     |     |     |      |
|                           |                                           |                                                                                                                                                                          | TPD1S514-3 |     |     |     |      |
|                           |                                           |                                                                                                                                                                          | TPD1S514   |     |     |     |      |
| t <sub>SS</sub>           | USB charging rise time (soft-start delay) | Force 5 V on VBUS_CON, measured from V <sub>BUS_SYS</sub> rises from 10% to 90% (with 1 MΩ load/ NO C <sub>LOAD</sub> )                                                  | TPD1S514-1 | 3.5 |     |     | ms   |
|                           |                                           |                                                                                                                                                                          | TPD1S514-2 |     |     |     |      |
|                           |                                           |                                                                                                                                                                          | TPD1S514-3 |     |     |     |      |
|                           |                                           |                                                                                                                                                                          | TPD1S514   |     |     |     |      |
| t <sub>OFF_DELAY</sub>    | USB charging turn-OFF time                | Measured from $\overline{\text{EN}}$ asserted High to V <sub>BUS_SYS</sub> falling to 10% with R <sub>LOAD</sub> = 10 Ω and No C <sub>LOAD</sub> on V <sub>BUS_SYS</sub> | TPD1S514-1 | 5.5 |     |     | μs   |
|                           |                                           |                                                                                                                                                                          | TPD1S514-2 |     |     |     |      |
|                           |                                           |                                                                                                                                                                          | TPD1S514-3 |     |     |     |      |
|                           |                                           |                                                                                                                                                                          | TPD1S514   |     |     |     |      |
| OVER VOLTAGE PROTECTION   |                                           |                                                                                                                                                                          |            |     |     |     |      |
| t <sub>OVP_response</sub> | OVP response time                         | Measured from OVP Condition to FET Turn OFF <sup>(1)</sup>                                                                                                               |            |     |     | 100 | ns   |

(1) Specified by design, not production tested



**Figure 1. TPD1S514-1 Response to Set  $\overline{\text{EN}}$  Low**

## 7.12 TPD1S514-1 Typical Characteristics

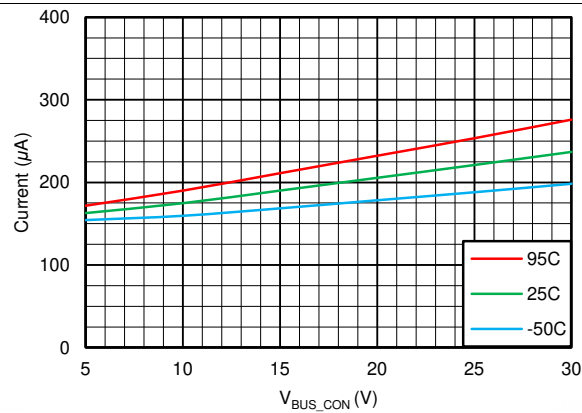


Figure 2. In Supply Current vs Supply Voltage

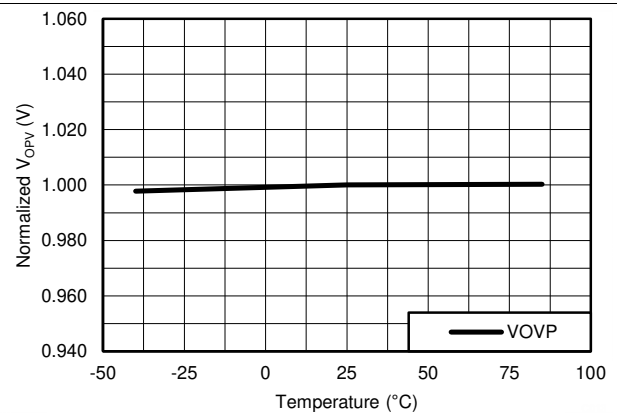


Figure 3. Normalized  $V_{OVP}$  vs Temperature

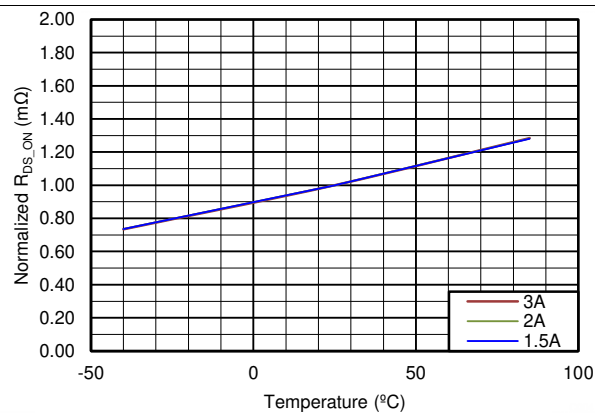


Figure 4. Normalized  $R_{ON}$  vs Temperature

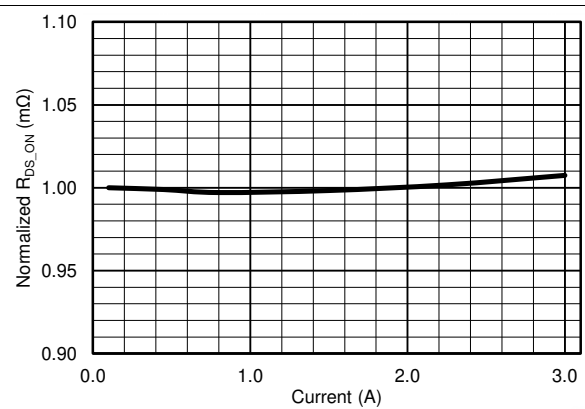


Figure 5. Normalized  $R_{ON}$  vs Output

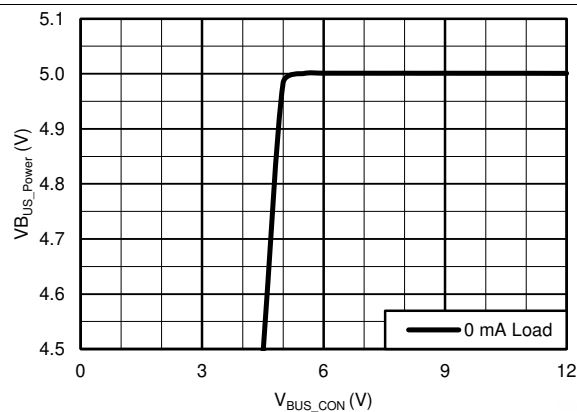


Figure 6.  $V_{BUS\_POWER}$  vs  $V_{BUS\_CON}$  With No Load

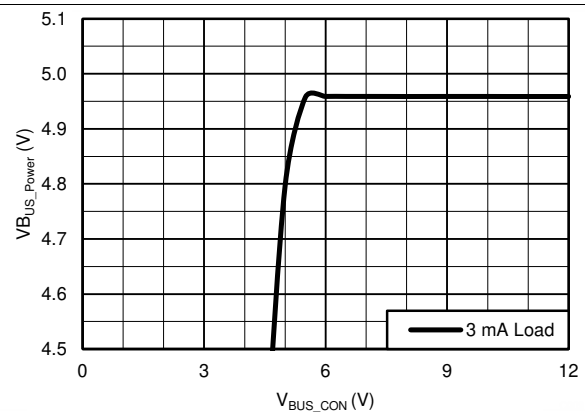
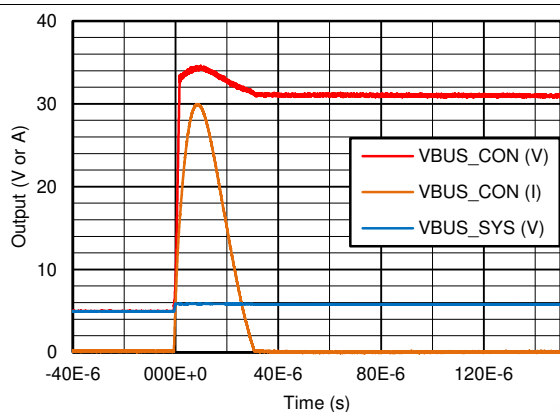
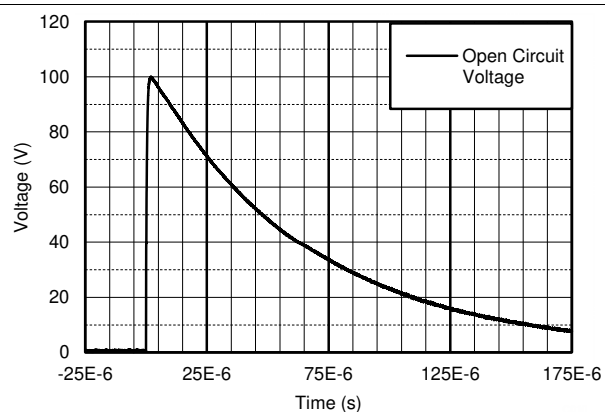


Figure 7.  $V_{BUS\_POWER}$  vs  $V_{BUS\_CON}$  With 3 mA Load

## TPD1S514-1 Typical Characteristics (continued)



**Figure 8. 100 V Surge With Device**



**Figure 9. 100 V Surge Without Device**

## 8 Detailed Description

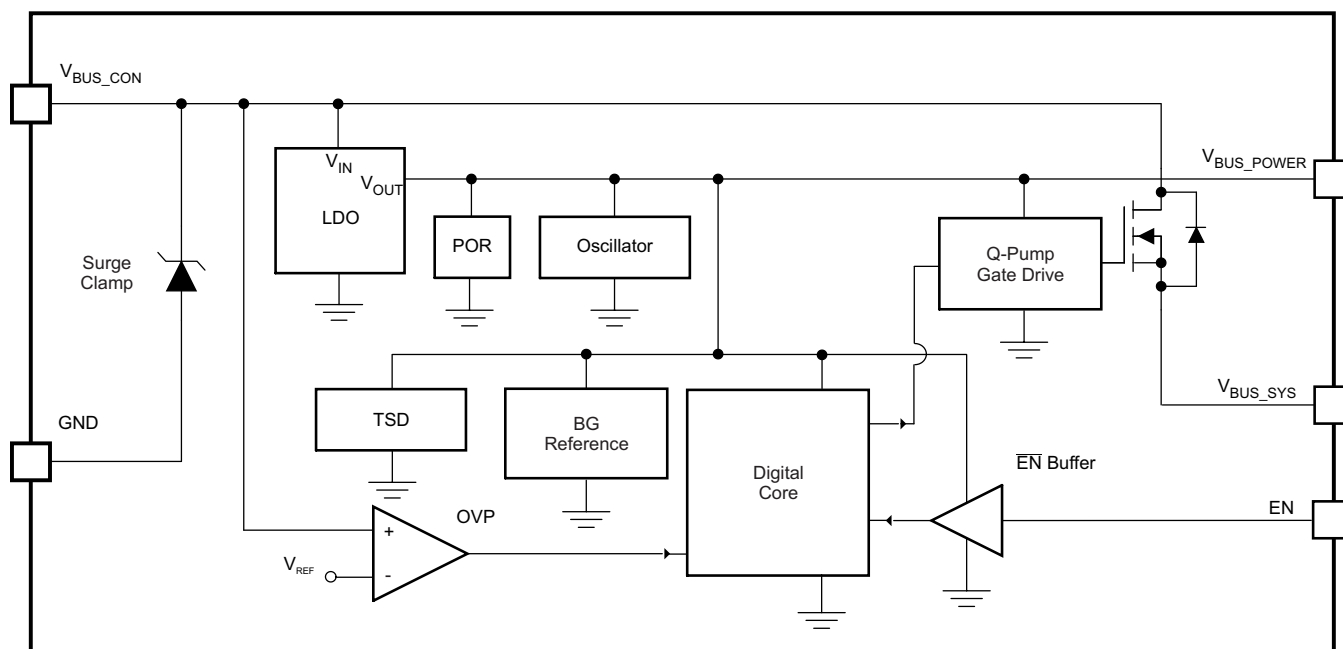
### 8.1 Overview

The TPD1S514 Family provides single-chip ESD, surge, and over voltage protection solutions for portable USB Charging and Host interfaces. Each device offers over voltage protection at the  $V_{BUS\_CON}$  pin up to 30-V DC. The TPD1S514 Family offers an ESD and Precision Clamp for the  $V_{BUS\_CON}$  pin, thus eliminating the need for external TVS clamp circuits in the application.

Each device has an internal oscillator and charge pump which controls turning ON the internal nFET switch. The internal oscillator controls the timers which enable the charge pump. If  $V_{BUS\_CON}$  is less than  $V_{OVP}$ , the internal charge pump is enabled. After a 20 ms internal delay, the charge-pump starts-up, and turns ON the internal nFET switch through a soft start. If at any time  $V_{BUS\_CON}$  rises above  $V_{OVP}$ , the nFET switch is turned OFF within 100 ns.

The TPD1S514 Family of devices also have a  $V_{BUS\_POWER}$  pin which follows  $V_{BUS\_CON}$  up to 4.9 V at 3 mA (except for TPD1S514, which follows  $V_{BUS\_CON}$  up to 6.48 V, after which it is regulated to that voltage) to power the system from  $V_{BUS\_CON}$ . In the case where the system battery state cannot power the system, voltage from an external charger can be provided to power the system.  $V_{BUS\_POWER}$  is supplied by an always on LDO regulator supplied by  $V_{BUS\_CON}$ .  $V_{BUS\_POWER}$  output voltage remains regulated to 4.9 V (except for TPD1S514, which follows  $V_{BUS\_CON}$  up to 6.48 V, after which it is regulated to that voltage) at up to 30-V DC on  $V_{BUS\_CON}$  and during IEC 61000-4-5 surge events of up to 100 V open circuit voltage on  $V_{BUS\_CON}$ .

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Over Voltage Protection on $V_{BUS\_CON}$ up to 30 V DC

When the  $V_{BUS\_CON}$  voltage rises above  $V_{OVP}$ , the internal nFET switch is turned OFF, removing power from the system side.  $V_{BUS\_CON}$  can tolerate up to 30-V DC. The response to over voltage is very rapid, with the nFET switch turning off in less than 100 ns. When the  $V_{BUS\_CON}$  voltage returns back to below  $V_{OVP} - V_{HYS\_OVP}$ , the nFET switch is turned ON again after an internal delay of  $t_{OVP\_RECOV}$  ( $t_{DELAY}$ ). This time delay ensures that the  $V_{BUS\_CON}$  supply has stabilized before turning the switch back on. After  $t_{OVP\_RECOV}$ , the TPD1S514 Family device turns on the nFET through a soft start. Once the OVP condition is cleared the nFET is turned completely ON.

## Feature Description (continued)

### 8.3.2 Precision OVP (< ±1% Tolerance)

1% OVP trip threshold accuracy allows use of the entire input charging range while protecting sensitive system-side components from over voltage conditions.

### 8.3.3 Low $R_{ON}$ nFET Switch Supports Host and Charging Mode

The nFET switch has a total on resistance ( $R_{ON}$ ) of 39 mΩ. This equates to a voltage drop of less than 140 mV when charging at the maximum 3.5 A current level. Such low  $R_{ON}$  helps provide maximum potential to the system as provided by an external charger or by the system when in Host Mode.

### 8.3.4 $V_{BUS\_POWER}$ , TPD1S514-1, TPD1S514-2, TPD1S514-3

The  $V_{BUS\_POWER}$  pin provides up to 3 mA and 5 V for powering the system using  $V_{BUS\_CON}$ .  $V_{BUS\_POWER}$  follows  $V_{BUS\_CON}$  after 3.5 V and up to the regulated 5 V. In the case where the system battery state cannot power the system, voltage from an external charger can power the system.  $V_{BUS\_POWER}$  is supplied by an always on LDO regulator supplied by  $V_{BUS\_CON}$ . The  $V_{BUS\_POWER}$  output voltage remains regulated to 5 V at up to 30-V DC on  $V_{BUS\_CON}$  and during IEC 61000-4-5 surge events of up to 100 V.

### 8.3.5 $V_{BUS\_POWER}$ , TPD1S514

The  $V_{BUS\_POWER}$  pin provides up to 3 mA and 6.48 V for powering the system using  $V_{BUS\_CON}$ .  $V_{BUS\_POWER}$  follows  $V_{BUS\_CON}$  after 3.5 V and up to the regulated 6.48 V. In the case where the system battery state cannot power the system, voltage from an external charger can be provided to power the system.  $V_{BUS\_POWER}$  is supplied by an always on LDO regulator supplied by  $V_{BUS\_CON}$ . The  $V_{BUS\_POWER}$  output voltage remains regulated to 6.48 V at up to 30-V DC on  $V_{BUS\_CON}$  and during IEC 61000-4-5 surge events of up to 100 V.

### 8.3.6 Powering the System When Battery is Discharged

There are two methods for powering the system under a dead battery condition. Case 1: The  $\overline{EN}$  pin can be tied to ground so that the nFET is always ON (when  $V_{UVLO} < V_{BUS\_CON} < V_{OVP}$ ) and an external charger can power  $V_{BUS}$ . Case 2: If  $\overline{EN}$  is controlled by a Power Management Unit (PMIC) or other logic,  $V_{BUS\_POWER}$  can be used to power the PMIC. In Case 2, once the device is enabled,  $t_{DELAY} + t_{SS}$ , work together to meet the USB Inrush Current compliance.

### 8.3.7 ±15 kV IEC 61000-4-2 Level 4 ESD Protection

The  $V_{BUS\_CON}$  pin can withstand ESD events up to ±15 kV Contact and Air-Gap. An ESD clamp diverts the current to ground.

### 8.3.8 100 V IEC 61000-4-5 μs Surge Protection

The  $V_{BUS\_CON}$  pin can withstand surge events up to 100 V open circuit voltage ( $V_{PP}$ ), or 900 W. A Precision Clamp diverts the current to ground and active circuitry switches OFF the nFET earlier than 100 ns before an over voltage can get through to  $V_{BYS\_SYS}$ . The ultra-fast response time of the TPD1S514 Family holds the voltage on  $V_{BUS\_SYS}$  to less than  $V_{OVP}$  during surge events of up to 100  $V_{PP}$ .

### 8.3.9 Startup and OVP Recovery Delay

Upon startup or recovering from an over voltage, the TPD1S514 Family of devices have a built in startup delay. An internal oscillator controls a charge pump to control the delay. Once a manufactured pre-programmed time,  $t_{DELAY}$ , has elapsed, the charge pump is enabled which turns ON the nFET. A manufactured pre-programmed soft start,  $t_{SS}$ , is used when turning ON the nFET. Once the device is enabled, these start delays,  $t_{DELAY} + t_{SS}$ , work together to meet the USB Inrush Current compliance.

### 8.3.10 Thermal Shutdown

The TPD1S514 Family has an over-temperature protection circuit to protect against system faults or improper use. The basic function of the thermal shutdown (TSD) circuit is to sense when the junction temperature has exceeded the absolute maximum rating and shuts down the device until the junction temperature has cooled to a safe level.

## 8.4 Device Functional Modes

### 8.4.1 Operation With $V_{BUS\_CON} < 3.5\text{ V}$ (Minimum $V_{BUS\_CON}$ )

The TPD1S514 Family operates normally (nFET ON) with input voltages above 3.5 V. The maximum UVLO voltage is 3.5 V and the device will operate at input voltages above 3.5 V. The typical UVLO voltage is 3.1 V and the device may operate at input voltages above that point. The device may also operate at input voltages as low as 2.7 V, the minimum UVLO. At input voltages between 0.6 V and 1.2 V, the state of output pins may not be controlled internally.

### 8.4.2 Operation With $V_{BUS\_CON} > V_{OVP}$

The TPD1S514 Family operates normally (nFET ON) with input voltages below  $V_{OVP\_min}$ . The typical OVP voltage is  $V_{OVP\_TYP}$  and the device may operate at input voltages below that point. The device may also operate at input voltages as high as  $V_{OVP\_MAX}$ .

**Table 1.  $V_{OVP}$  Values**

| DEVICE NAME | $V_{OVP}$ |       |       |
|-------------|-----------|-------|-------|
|             | MIN       | TYP   | MAX   |
| TPD1S514-1  | 5.9       | 5.95  | 5.99  |
| TPD1S514-2  | 9.9       | 9.98  | 10.05 |
| TPD1S514-3  | 13.5      | 13.75 | 14    |
| TPD1S514    | 5.9       | 5.95  | 5.99  |

### 8.4.3 OTG Mode

The TPD1S514 Family of devices UVLO and OVP voltages are referenced to  $V_{BUS\_CON}$  voltage. In OTG mode,  $V_{BUS\_SYS}$  is driving the  $V_{BUS\_CON}$ . Under this situation, initially  $V_{BUS\_CON}$  is powered through the body diode of the nFET by  $V_{BUS\_SYS}$ . Once the UVLO threshold on  $V_{BUS\_CON}$  is met, the nFET turns ON. If there is a short to ground on  $V_{BUS\_CON}$  the OTG supply is expected to limit the current.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPD1S514 Family of devices offer  $V_{BUS}$  port protection implementing UVLO and OVP, with an LDO supplied  $V_{BUS\_POWER}$  pin to regulate an output supply pin of 3 mA at 5 V (except for TPD1S514, which follows  $V_{BUS\_CON}$  up to 6.48 V, after which it is regulated to that voltage). The  $V_{BUS\_POWER}$  pin can be used to power the system from an external source on  $V_{BUS\_CON}$  in case the system's battery state cannot power the system.

### 9.2 Typical Applications

#### 9.2.1 TPD1S514-1 USB 2.0/3.0 Case 1: Always Enabled

The  $\overline{EN}$  pin can be tied to ground so that the nFET is ON when  $V_{UVLO} < V_{BUS\_CON} < V_{OVP}$  and an external charger can power  $V_{BUS}$ .  $V_{BUS\_POWER}$  should be tied to ground with a 1- $\mu$ F capacitor for LDO stability. USB Inrush Current compliance tests will need to be handled by the rest of the system since the start delays  $t_{DELAY}$  and  $t_{SS}$  implement only after the device changes from disabled to enabled, or after any UVLO or OVP event.

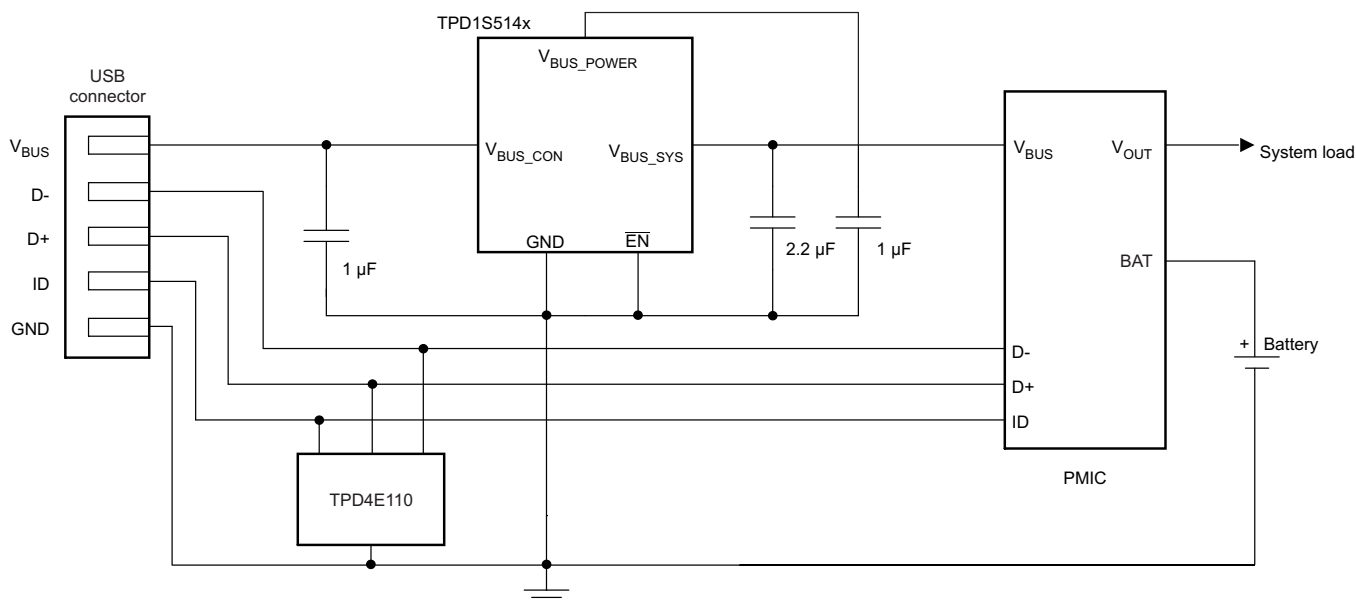


Figure 10. Always on, TPD1S514-1

#### 9.2.1.1 Design Requirements

For this example, use the following input parameters from Table 2.

Table 2. Design Parameters

| DESIGN PARAMETERS              | EXAMPLE VALUE              |
|--------------------------------|----------------------------|
| Signal range on $V_{BUS\_CON}$ | 3.5 V – 5.9 V              |
| Signal range on $V_{BUS\_SYS}$ | 3.9 V – 5.9 V              |
| Signal on $\overline{EN}$      | Tie to system ground plane |

### 9.2.1.2 Detailed Design Procedure

To begin the design process the designer needs to know the  $V_{BUS}$  voltage range.

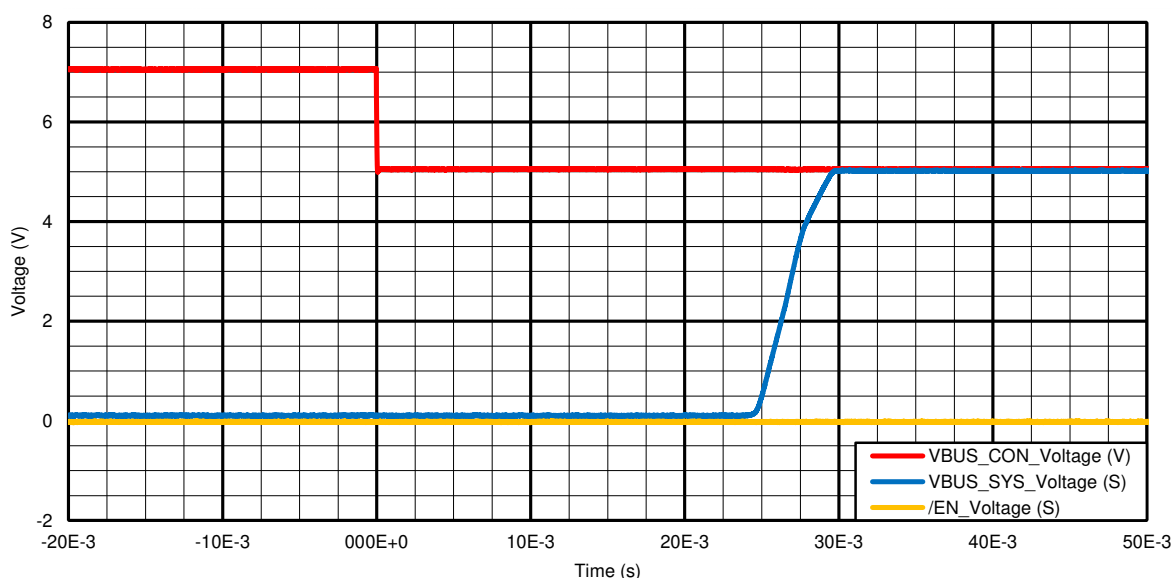
#### 9.2.1.2.1 $V_{BUS}$ Voltage Range

The UVLO trip-point is a maximum 3.5 V and the OVP trip-point is a minimum 5.9 V. This provides some headroom for the USB 2.0 specified minimum 4.4 V (Low-power) or 4.75 V (Full-power) and 5.25 V maximum; or the USB 3.0 specified minimum 4.45 V and 5.25 V maximum.

#### 9.2.1.2.2 Discharged Battery

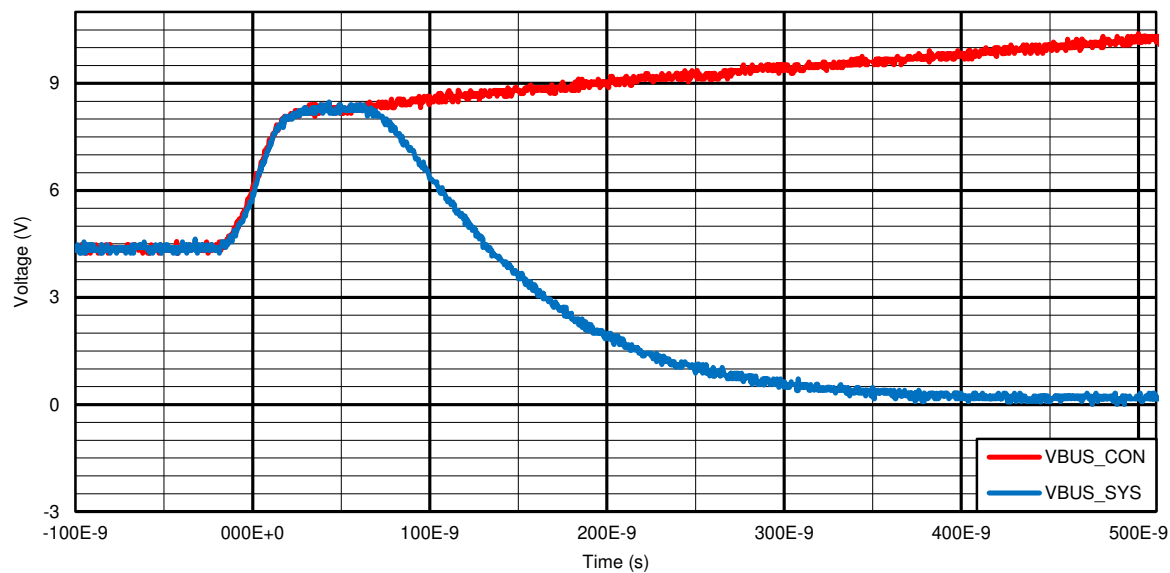
Connecting  $\overline{EN}$  to ground sets the part active at all times. OVP and UVLO are always active, even when the system battery is fully discharged. In the case of a discharged system battery,  $V_{BUS\_SYS}$  can be used to power the system when a source with voltage between  $V_{UVLO}$  and  $V_{OVP}$  is attached to  $V_{BUS\_CON}$ .

### 9.2.1.3 Application Curves



**Figure 11.  $V_{BUS\_SYS}$  Recovery Time From Over Voltage on  $V_{BUS\_CON}$**

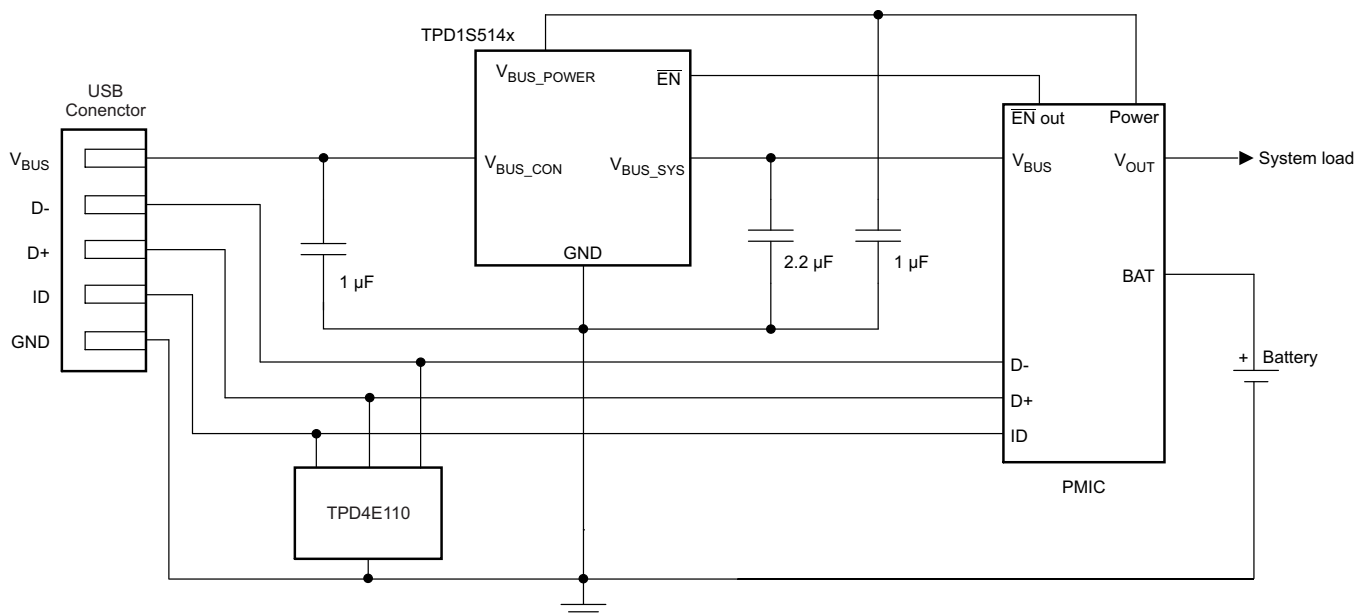




**Figure 12. OVP Response**

## 9.2.2 TPD1S514-1 USB 2.0/3.0 Case 2: PMIC Controlled $\overline{\text{EN}}$

The TPD1S514 Family offers more flexibility to system designers to power up the system during a dead battery condition. Refer to [Figure 13](#), the  $V_{\text{BUS\_POWER}}$  pin supplies 4.95 V and 3 mA to power the PMIC in a dead battery condition. Regardless of  $\overline{\text{EN}}$  state,  $V_{\text{BUS\_POWER}}$  is available to the PMIC. Utilizing this power, the PMIC can enable the TPD1S514 Family of devices when a valid  $V_{\text{BUS\_CON}}$  voltage is present.



**Figure 13. PMIC Controlled  $\overline{\text{EN}}$ , TPD1S514-1**

### 9.2.2.1 Design Requirements

For this example, use the following table as input parameters:

**Table 3. Design Parameters**

| DESIGN PARAMETERS                            | EXAMPLE VALUE |
|----------------------------------------------|---------------|
| Signal range on $V_{\text{BUS\_CON}}$        | 3.5 V – 5.9 V |
| Signal range on $V_{\text{BUS\_SYS}}$        | 3.9 V – 5.9 V |
| Drive $\overline{\text{EN}}$ low (enabled)   | 0 V – 0.8 V   |
| Drive $\overline{\text{EN}}$ high (disabled) | 1.2 V – 6.0 V |

### 9.2.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon. The designer needs to know the following:

- $V_{\text{BUS}}$  voltage range
- PMIC power requirement

#### 9.2.2.2.1 $V_{\text{BUS}}$ Voltage Range

The UVLO trip-point is a maximum 3.5 V and the OVP trip-point is a minimum 5.9 V. This provides some headroom for the USB 2.0 specified minimum 4.4 V (Low-power) or 4.75 V (Full-power) and 5.25 V maximum; or the USB 3.0 specified minimum 4.45 V and 5.25 V maximum.

#### 9.2.2.2.2 PMIC Power Requirement

The  $V_{\text{BUS\_POWER}}$  pin can source up to 3 mA of current and maintain a minimum 4.8 V, 4.95 V typical. TPD1S514-1 design provides an LDO regulator supplied voltage source which can be used to provide power to a PMIC when its internal battery supplied power is unavailable. When selecting a matching PMIC, ensure its power requirement can be met by the  $V_{\text{BUS\_POWER}}$  pin if designing for this scenario.

### 9.2.2.2.3 Discharged Battery

Powering the PMIC from  $V_{BUS\_POWER}$  allows logic control of the  $\overline{EN}$  pin to set TPD1S514-1 active and begin charging the battery and powering up the rest of the system.

### 9.2.2.3 Application Curve

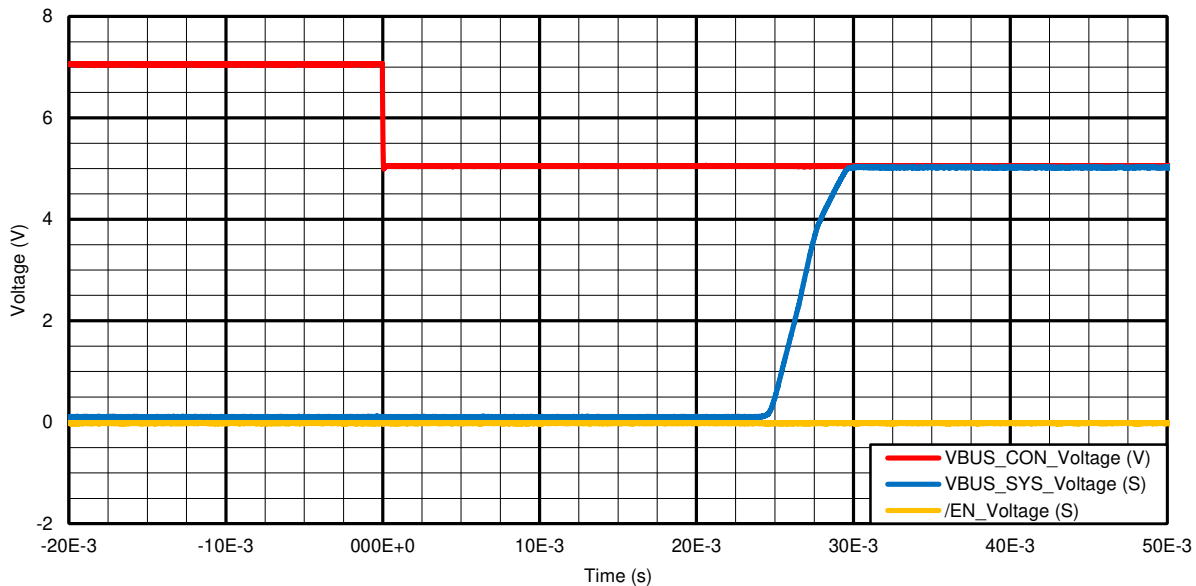


Figure 14.  $V_{BUS\_SYS}$  Recovery Time From Over Voltage on  $V_{BUS\_CON}$

## 10 Power Supply Recommendations

The TPD1S514 Family is designed to receive power from a USB 3.0 (or lower)  $V_{BUS}$  source. It can operate normally (nFET ON) between a minimum 3.5 V and a maximum  $V_{OVP\_MIN}$  V. Thus, the power supply (with a ripple of  $V_{RIPPLE}$ ) requirement for the TPD1S514 Family of devices to be able to switch the nFET ON is between  $3.5\text{ V} + V_{RIPPLE}$  and  $V_{OVP\_MIN} - V_{RIPPLE}$ , where  $V_{OVP\_MIN}$  is:

Table 4.  $V_{OP\_MIN}$  Values

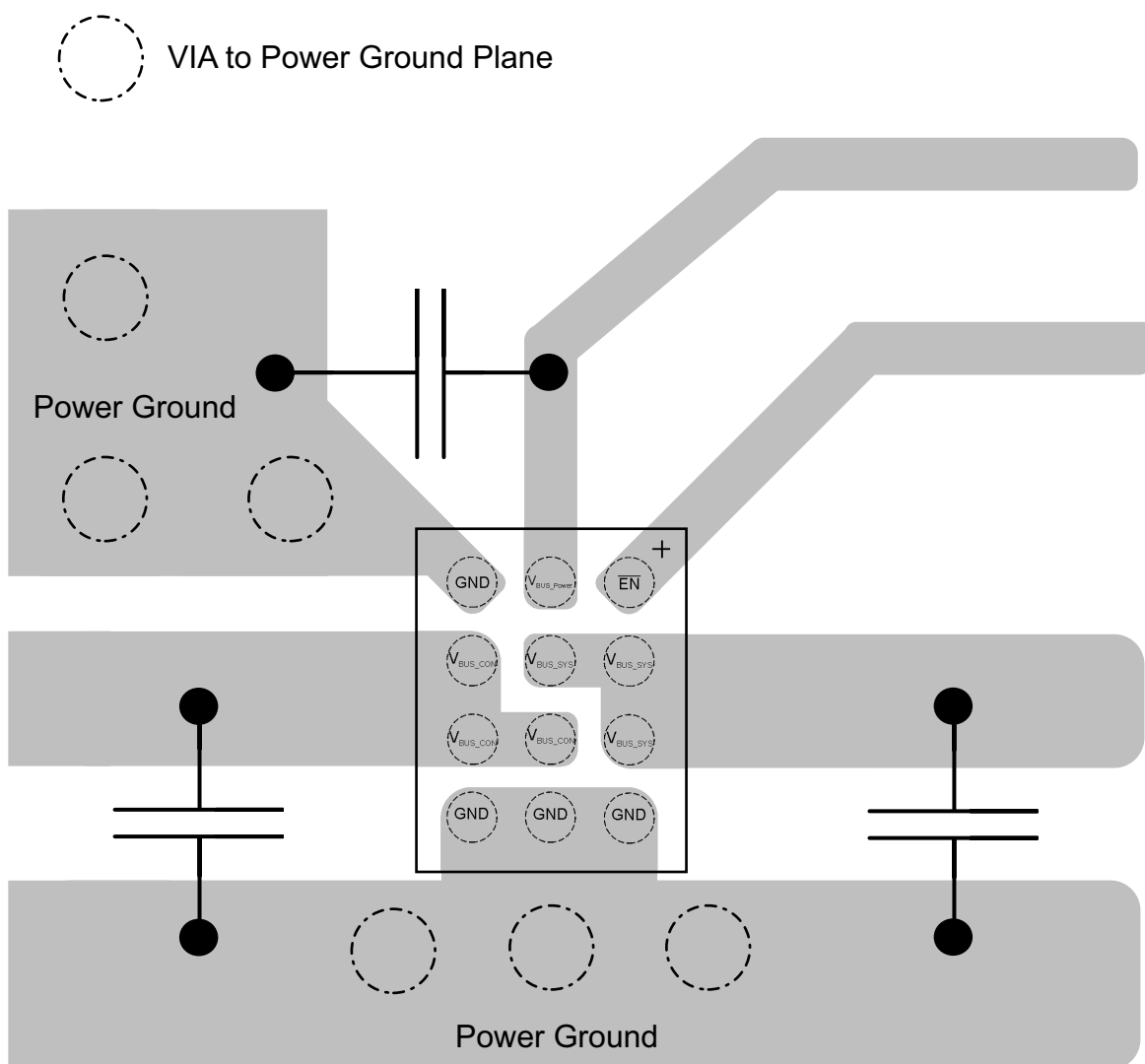
| DEVICE NAME | $V_{OVP\_MIN}$ |
|-------------|----------------|
| TPD1S514-1  | 5.90 V         |
| TPD1S514-2  | 9.9 V          |
| TPD1S514-3  | 13.5 V         |
| TPD1S514    | 5.90 V         |

## 11 Layout

### 11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

### 11.2 Layout Example



When designing layout for the TPD1S514 Family, note that  $V_{BUS\_CON}$  and  $V_{BUS\_SYS}$  pins allow extra wide traces for good power delivery. In the example shown, these pins are routed with 50 mil (1.27 mm) wide traces. Place the  $V_{BUS\_CON}$ ,  $V_{BUS\_SYS}$ , and  $V_{BUS\_POWER}$  capacitors as close to the pins as possible. Use external and internal ground planes and stitch them together with VIAs as close to the GND pins of TPD1S514 as possible. This allows for a low impedance path to ground so that the device can properly dissipate any surge or ESD events.

**Figure 15. Layout Recommendation**

## 12 Device and Documentation Support

### 12.1 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 13.1 Package Option Addendum

### 13.1.1 Packaging Information

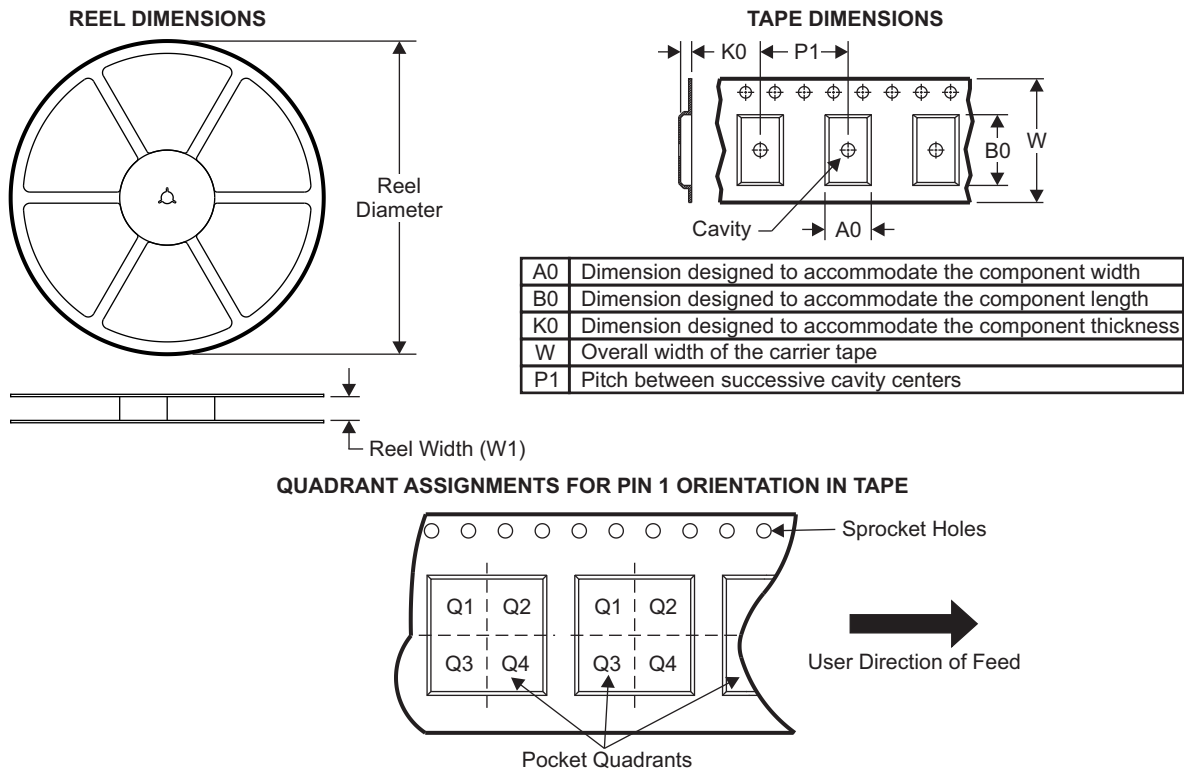
| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish <sup>(3)</sup> | MSL Peak Temp <sup>(4)</sup> | Op Temp (°C) | Device Marking <sup>(5)(6)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|---------------------------------|------------------------------|--------------|----------------------------------|
| TPD1S514-1YZR    | Active                | DSBGA        | YZ              | 12   | 3000        | Green (RoHS & no Sb/Br) | SNAGCU                          | Level-1-260C-UNLIM           | –40 to 85    | RH5141                           |
| TPD1S514-2YZR    | Active                | DSBGA        | YZ              | 12   | 3000        | Green (RoHS & no Sb/Br) | SNAGCU                          | Level-1-260C-UNLIM           | –40 to 85    | RH5142                           |
| TPD1S514-3YZR    | Active                | DSBGA        | YZ              | 12   | 3000        | Green (RoHS & no Sb/Br) | SNAGCU                          | Level-1-260C-UNLIM           | –40 to 85    | RH5143                           |

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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### 13.1.2 Tape and Reel Information



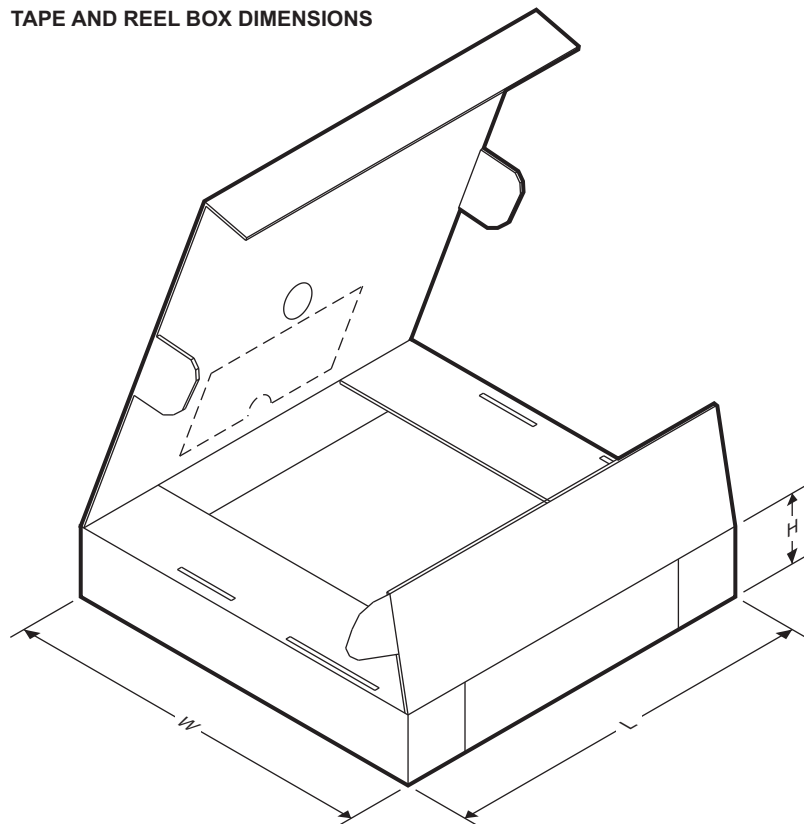
| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPD1S514-1YZR | DSBGA        | YZ              | 12   | 3000 | 180.0              | 8.4                | 1.39    | 2.09    | 0.75    | 4.0     | 8.0    | Q2            |
| TPD1S514-2YZR | DSBGA        | YZ              | 12   | 3000 | 180.0              | 8.4                | 1.39    | 2.09    | 0.75    | 4.0     | 8.0    | Q2            |
| TPD1S514-3YZR | DSBGA        | YZ              | 12   | 3000 | 180.0              | 8.4                | 1.39    | 2.09    | 0.75    | 4.0     | 8.0    | Q2            |

## TPD1S514x

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[www.ti.com](http://www.ti.com)

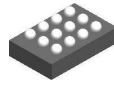
### TAPE AND REEL BOX DIMENSIONS



| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPD1S514-1YZR | DSBGA        | YZ              | 12   | 3000 | 182.0       | 182.0      | 20.0        |
| TPD1S514-2YZR | DSBGA        | YZ              | 12   | 3000 | 182.0       | 182.0      | 20.0        |
| TPD1S514-3YZR | DSBGA        | YZ              | 12   | 3000 | 182.0       | 182.0      | 20.0        |



TPD1S514-xYZ

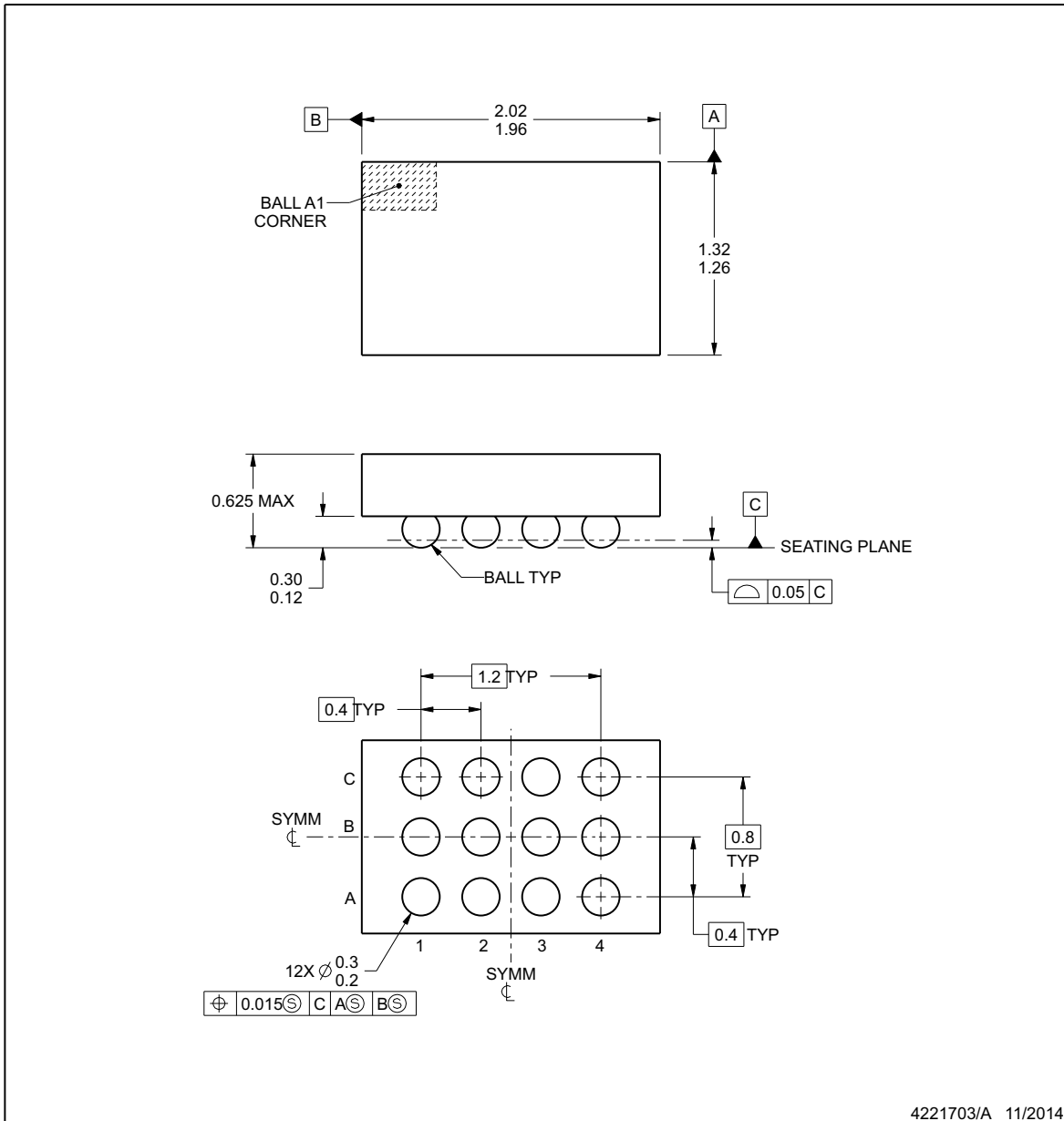


# PACKAGE OUTLINE

**YZ0012-C01**

**DSBGA - 0.625 mm max height**

DIE SIZE BALL GRID ARRAY



## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

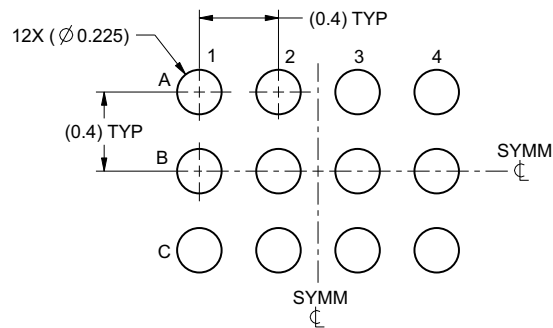
TPD1S514-xYZ

EXAMPLE BOARD LAYOUT

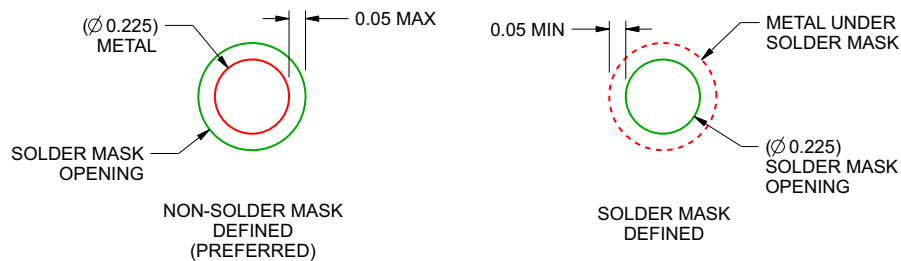
YZ0012-C01

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

4221703/A 11/2014

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 ([www.ti.com/lit/sbva017](http://www.ti.com/lit/sbva017)).

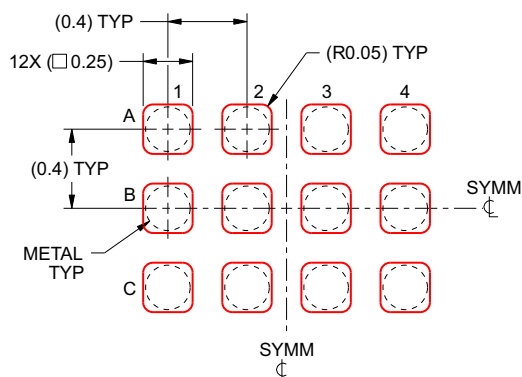
TPD1S514-xYZ

## EXAMPLE STENCIL DESIGN

**YZ0012-C01**

**DSBGA - 0.625 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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