TMUXHS4512 1.8V 6-Channel 20Gbps Differential 2:1 Mux / 1:2 Demux

1 Features

- Supports USB4 up to 20Gbps, DisplayPort 1.4/2.1 up to UHBR20
- Data rate support up to 20Gbps
- High-speed path supports common-mode voltage range of 0V to 1.0V
- Low R_{ON} of 8.8Ω typical for high-speed data pins
- –3dB differential BW of 13.0GHz for high-speed data pins
- Excellent dynamic characteristics at 10GHz:
  - Insertion loss: –2.5dB
  - Return loss: –13dB
  - Cross talk: –30dB
- All sideband signals can pass-through up to 1.8V levels and are 5.5V tolerant
- Support 1.2V, 1.8V and 3.3V control logic
- Single supply voltage of 1.8V
- Low active (500μA) and standby power (2μA)
- I_{OFF} protection that prevents current leakage when supply rail collapsed (V_{CC} = 0V)
- Temperature range: –40°C to 125°C
- Package: 40-pin, 3mm × 6mm, 0.4mm pitch WQFN

2 Applications

- PC and notebooks
- Gaming, Home theater & entertainment and TV
- Data center and enterprise computing
- Medical applications
- Test and measurements
- Factory automation and control
- Aerospace and defense
- Electronic point of sale (EPOS)
- Wireless infrastructure

3 Description

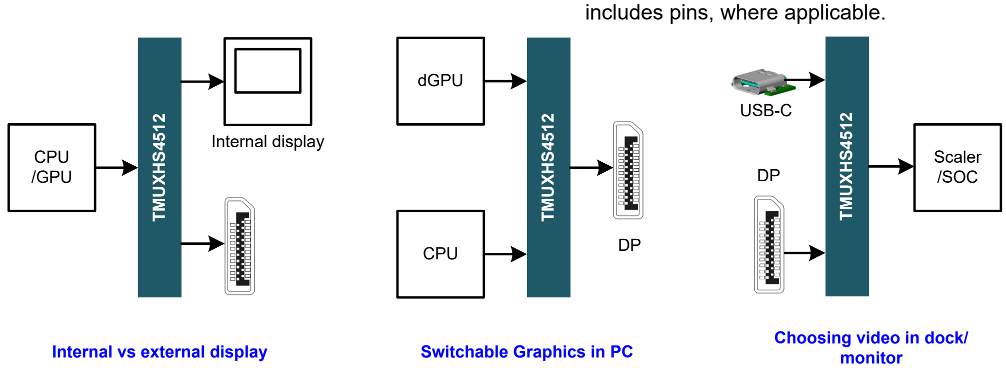
The TMUXHS4512 is a high-speed bidirectional passive switch in mux or demux configurations. The device is protocol agnostic supporting many applications including USB4, Thunderbolt3/4, and DisplayPort 1.4 / 2.1. The TMUXHS4512 is a generic analog differential passive mux or demux that works for many high-speed differential interfaces with data rates up to 20Gbps. The TMUXHS4512 high-speed channels support differential signaling and single-ended signaling as long as the single-ended signals do not violate $V_{P\text{-}N\_ABSMAX}$ parameter. The sideband channels are 5V tolerant and support single-ended and differential signaling such as I^2C, UART, DisplayPort AUX, and USB2, just to name few. The dynamic characteristics of the high-speed channel allows high-speed switching with minimal attenuation to the signal eye diagram and with very little added jitter. The silicon design of the device is optimized for excellent frequency response at higher frequency spectrum of the signals. The device supports differential signaling with common-mode voltage range (CMV) of 0V to 1.0V in the Dxx datapaths.

The TMUXHS4512 consumes very low active power of 500μA. The device also offers a power-down mode in which all channels become Hi-Z and the device operates with minimal power of just 2μA.

Package Information

PART NUMBER	TEMPERATURE	PACKAGE(1)	PACKAGE SIZE(2)
TMUXHS4512	T_A = 0°C to 105°C	RET (WQFN, 40)	6mm × 3mm
TMUXHS4512I	T_A = –40°C to 125°C		

(1) For all available packages, see Section 11.
(2) The package size (length x width) is a nominal value and includes pins, where applicable.



Simplified Use Cases

Table of Contents

4 Pin Configuration and Functions

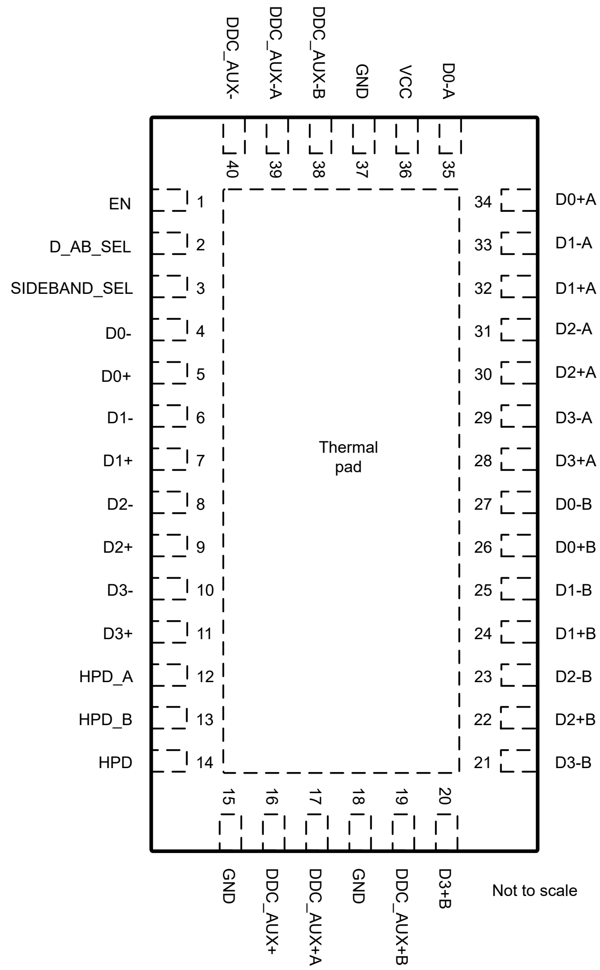


Figure 4-1. RET Package 40-Pin WQFN With Exposed Thermal Pad (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	1	I	Device Enable L: Device Disabled. All data and sideband signals in Hi-Z. H: Device Enabled. All data and sideband signals selected by D_AB_SEL and SIDEBAND_SEL are enabled.
D_AB_SEL	2	I	Selects between high-speed datapath A and B. L: High-speed datapath A H: High-speed datapath B
SIDEBAND_SEL	3	I	Selects between sideband path A and B L: Sideband path A H: Sideband path B
D0–	4	I/O	Common Port, Channel 0, –ve signal
D0+	5	I/O	Common Port, Channel 0, +ve signal
D1–	6	I/O	Common Port, Channel 1, –ve signal
D1+	7	I/O	Common Port, Channel 1, +ve signal
D2–	8	I/O	Common Port, Channel 2, –ve signal

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
D2+	9	I/O	Common Port, Channel 2, +ve signal
D3–	10	I/O	Common Port, Channel 3,–ve signal
D3+	11	I/O	Common Port, Channel 3, +ve signal
HPD_A	12	I/O	Port A, Hot Plug Detect sideband signal
HPD_B	13	I/O	Port B, Hot Plug Detect sideband signal
HPD	14	I/O	Common Port, Hot Plug Detect sideband signal
GND	15	GND	Ground
DDC_AUX+	16	I/O	Common Port, DDC or AUX sideband signal
DDC_AUX+A	17	I/O	Port A, DDC or AUX sideband signal
GND	18	GND	Ground
DDC_AUX+B	19	I/O	Port B, DDC or AUX sideband signal
D3+B	20	I/O	Port B, Channel 3, +ve signal
D3–B	21	I/O	Port B, Channel 3, –ve signal
D2+B	22	I/O	Port B, Channel 2, +ve signal
D2–B	23	I/O	Port B, Channel 2,–ve signal
D1+B	24	I/O	Port B, Channel 1, +ve signal
D1–B	25	I/O	Port B, Channel 1, –ve signal
D0+B	26	I/O	Port B, Channel 0, +ve signal
D0–B	27	I/O	Port B, Channel 0, –ve signal
D3+A	28	I/O	Port A, Channel 3, +ve signal
D3–A	29	I/O	Port A, Channel 3, –ve signal
D2+A	30	I/O	Port A, Channel 2, +ve signal
D2–A	31	I/O	Port A, Channel 2,–ve signal
D1+A	32	I/O	Port A, Channel 1, +ve signal
D1-A	33	I/O	Port A, Channel 1, –ve signal
D0+A	34	I/O	Port A, Channel 0, +ve signal
D0–A	35	I/O	Port A, Channel 0, –ve signal
VCC	36	Power	Supply Voltage
GND	37	GND	Ground
DDC_AUX-B	38	I/O	Port B, DDC or AUX sideband signal
DDC_AUX-A	39	I/O	Port A, DDC or AUX sideband signal
DDC_AUX-	40	I/O	Common Port, DDC or AUX sideband signal
GND	PowerPad	GND	Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
VCC_{ABSMAX}	Supply voltage range		–0.5	2.5	V
$V_{I/O-ABSMAX}$	Analog voltage range[2] [3] [4]	All high-speed data I/O pins	–0.5	4.0	V
$V_{I/O-ABSMAX}$	Analog voltage range[2] [3] [4]	All sideband[5] pins	–0.5	6.0	V
$V_{IN-ABSMAX}$	Digital input voltage range[2] [3]	All control pins[6]	–0.5	5.0	V
V_{P-N_ABSMAX}	Absolute value of positive pin minus negative pin	All high-speed data I/O pins		0.8	V
T_{jmax}	Maximum junction temperature TMUXHS4512		0	105	°C
T_{jmax}	Maximum junction temperature TMUXHS4512I		–40	125	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) Sideband pins: DDC_AUX+A, DDC_AUX-A, HPD_A, DDC_AUX+B, DDC_AUX-B, HPD_B, DDC_AUX+, DDC_AUX-, HPD
(6) Control pins: D_AB_SEL, SIDEBAND_SEL, EN

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, [1]	±1500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, [2]	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	1.62	1.8	1.98	V
$V_{I/O,CM}$	Input/Output common mode voltage (data pins)	0		1	V
$V_{I/O}$	Input/Output voltage data pins	0		1.4	V
$V_{I/O}$	Input/Output voltage sideband[2] pins	0		1.8	V
V_{IN}	Digital input voltage (control[3] pins)	0		VCC	V
DR	Data rate for differential signals			20	Gbps
T_A	Operating ambient temperature TMUXHS4512	0		105	°C
T_A	Operating ambient temperature TMUXHS4512I	–40		125	°C
T_J	Operating junction temperature TMUXHS4512	0		110	°C
T_J	Operating junction temperature TMUXHS4512I	–40		125	°C

(1) All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. For more information, see Implications of Slow or Floating CMOS Inputs application note.
(2) Sideband pins: DDC_AUX+A, DDC_AUX-A, HPD_A, DDC_AUX+B, DDC_AUX-B, HPD_B, DDC_AUX+, DDC_AUX-, HPD
(3) Control pins: D_AB_SEL, SIDEBAND_SEL, EN

5.4 Thermal Information

THERMAL METRIC[1]		TMUXHS4512 RET 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER [3] [4]			TEST CONDITIONS[1]	MIN	TYP[2]	MAX	UNIT
DC Characteristics (data and sideband)							
R_{ON-D}	ON-state resistance	All data pins;	V_{CM} = 0V to 1V; $I_{I/O}$ = –10mA; VCC = 1.8V ±10%; 0 to 85℃;		8.8	11	Ω
			V_{CM} = 0V to 1V; $I_{I/O}$ = –10mA; VCC = 1.8V ±10%; –40 to 125℃;		8.8	12	Ω
R_{ON-SB}	ON-state resistance	All sideband pins;	$V_{I/O}$ = 0V to VCC; $I_{I/O}$ = –10mA; VCC = 1.8V ±10%; 0 to 85℃;		8.5	12.5	Ω
			$V_{I/O}$ = 0V to VCC; $I_{I/O}$ = –10mA; VCC = 1.8V ±10%; –40 to 125℃;		8.5	13	Ω
$R_{ON-SB-3P6V}$	ON-state resistance	All sideband pins;	$V_{I/O}$ = 3.6V; $I_{I/O}$ = –10mA; VCC = 1.8V ±10%; –40 to 125℃;		120	160	Ω
$C_{ON-SB-1M}$	Sideband ON capacitance to GND		f = 1MHz;			7	pF
$C_{OFF-SB-1M}$	Sideband Off capacitance to GND		f = 1MHz;			4.5	pF
I_{IH-D}	Input current for high-speed data pair	All selected data pins. Leakage for each high-speed pair.	EN = H; $V_{I/O}$ = 1.4V; VCC = 1.8V ±10%;			1.5	µA
		All non-selected data pins. Leakage for each high-speed pair.	EN = H; $V_{I/O}$ = 1.4V; VCC = 1.8V ±10%;			35	µA
I_{IH-SB}	Input current for sideband	All selected sideband pins.	EN = H; $V_{I/O}$ = 1.8V; VCC = 1.8V ±10%;			2.5	µA
		All non-selected sideband pins.	EN = H; $V_{I/O}$ = 1.8V; VCC = 1.8V ±10%;			1	µA
$I_{OFF-DAB}$	Leakage under power off (failsafe current)	All data pins	VCC = 0V; $V_{I/O}$ = 0V to 1.4V;	–8		15	µA
I_{OFF-SB}	Leakage under power off (failsafe current)	All sideband pins	VCC = 0V; $V_{I/O}$ = 0V to 5.5V;	–1		5	µA
Control Inputs (SIDEBAND_SEL, D_AB_SEL, EN)							
$V_{IH-CTRL}$	High-level input voltage for control pins	Per pin for all control pins.	VCC = 1.8V ±10%;	1.0			V
$V_{IL-CTRL}$	Low-level input voltage for control pins	Per pin for all control pins.	VCC = 1.8V ±10%;			0.3	V
$I_{IH-CTRL}$	Input high leakage current for control pins	Per pin for all control pins.	VCC = 1.98V; V_{IN} = 1.98V;	–0.1		0.1	µA
$I_{IL-CTRL}$	Input low leakage current for control pins	Per pin for all control pins.	VCC = 1.98V; V_{IN} = 0V;	–0.1		0.1	µA
$I_{OFF-CTRL}$	Leakage under power off (failsafe current)	Per pin for all control pins.	VCC = 0V; VIN = 0V or 1.98V;	–0.1		0.1	µA
$C_{IN-CTRL}$	Input capacitance	Per pin for all control pins.	f = 1MHz;			5	pF
Power Supply							

over operating free-air temperature range (unless otherwise noted)

PARAMETER [3] [4]			TEST CONDITIONS[1]	MIN	TYP[2]	MAX	UNIT
I_{CC}	VCC supply current in active mode	VCC supply current in active mode	EN = H; V_{CM} = 1V			500	µA
I_{CC-PD}	VCC supply current in power-down mode	VCC supply current in power-down mode	EN = L; V_{CM} = 1V		0.07	2	µA

(1) V_I, V_O, I_I, and I_O refer to data and sideband I/O pins.V_{IN} refers to the control inputs.
(2) All typical values are at V_{CC} = 1.8V (unless otherwise noted), T_A = 25°C.
(3) Sideband pins: DDC_AUX+A, DDC_AUX-A, HPD_A, DDC_AUX+B, DDC_AUX-B, HPD_B, DDC_AUX+, DDC_AUX-, HPD
(4) Control pins: D_AB_SEL, SIDEBAND_SEL, EN

5.6 High-Speed Performance Parameters

over recommended operation free-air temperature range, (unless otherwise noted). For all data pins. R_L = 50Ω where applicable.

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
BW_{SB}	Sideband pins differential bandwidth (–3dB from DC)			2.0		GHz
BW_{HS}	High-speed pins differential bandwidth (–3dB from DC)			13		GHz
IL_{DAB}	Differential insertion loss	At 100MHz; VCM = 0V;		–0.7		dB
		At 1.7GHz; VCM = 0V;		–1.0		dB
		At 2.7GHz; VCM = 0V;		–1.1		dB
		At 4.0GHz; VCM = 0V;		–1.2		dB
		At 6.0GHz; VCM = 0V;		–1.6		dB
		At 10.0GHz; VCM = 0V;		–2.5		dB
RL_{DAB}	Differential return loss	At 100MHz; VCM = 0V;		–23		dB
		At 1.7GHz; VCM = 0V;		–22		dB
		At 2.7GHz; VCM = 0V;		–20		dB
		At 4.0GHz; VCM = 0V;		–19		dB
		At 6.0GHz; VCM = 0V;		–18		dB
		At 10.0GHz; VCM = 0V;		–13		dB
Xtalk	Differential crosstalk	At 100MHz; VCM = 0V;		–66		dB
		At 1.7GHz; VCM = 0V;		–40		dB
		At 2.7GHz; VCM = 0V;		–37		dB
		At 4.0GHz; VCM = 0V;		–44		dB
		At 6.0GHz; VCM = 0V;		–45		dB
		At 10.0GHz; VCM = 0V;		–30		dB
OISO	Differential off isolation	At 100MHz; VCM = 0V;		–65		dB
		At 1.7GHz; VCM = 0V;		–37		dB
		At 2.7GHz; VCM = 0V;		–33		dB
		At 4.0GHz; VCM = 0V;		–30		dB
		At 6.0GHz; VCM = 0V;		–27		dB
		At 10.0GHz; VCM = 0V;		–23		dB

(1) All Typical Values are at V_{CC} = 1.8V (unless otherwise noted), T_A = 25°C.

5.7 Switching Characteristics

PARAMETER			MIN	TYP	MAX	UNIT
Device Switching Time						
$t_{SW\_POWER\_ON}$	Device power ON time	EN pin from L to H;			200	µs
$t_{SW\_POWER\_OFF}$	Device power OFF time	EN pin from H to L;			550	ns
High Speed Pins						
t_{PD}	Switch differential propagation delay	f = 1GHz		60		ps

PARAMETER			MIN	TYP	MAX	UNIT
t_{SW_AB}	Switching time from A to B	Measured from 50% of select to 50% of VOH/VOL			60	µs
t_{SW_BA}	Switching time from B to A	Measured from 50% of select to 50% of VOH/VOL			60	µs
t_{SK_INTRA}	Intra-pair output skew between + and - pins for same channel	f = 1GHz		1.8	6	ps
t_{SK_INTER}	Inter-pair output skew between channels	f = 1GHz			9	ps
Sideband Pins						
$t_{PD\text{-}SB}$	Switch single-ended propagation delay	f = 1MHz			250	ps
$t_{SW\text{-}SB\_AB}$	Switching time from A to B	Measured from 50% of select to 50% of VOH/VOL			20	µs
$t_{SW\text{-}SB\_BA}$	Switching time from B to A	Measured from 50% of select to 50% of VOH/VOL			20	µs
$t_{SK\text{-}SB}$	Output skew between DDC_AUX+ and DDC_AUX- pins	f = 1MHz			8	ps

5.8 Typical Characteristics

Data taken from a single unit under nominal power supply and temperature conditions with $V_{I/O,CM}$ at 0V.

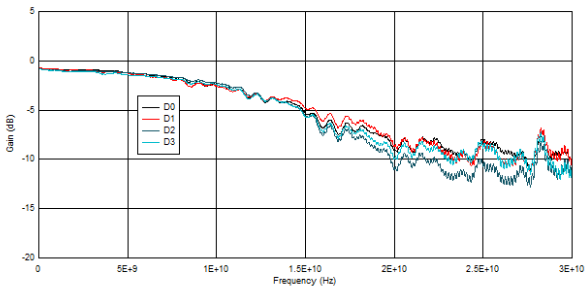


Figure 5-1. Differential Insertion Loss for port A

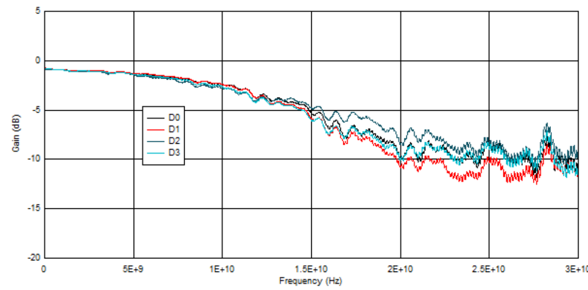


Figure 5-2. Differential Insertion Loss for port B

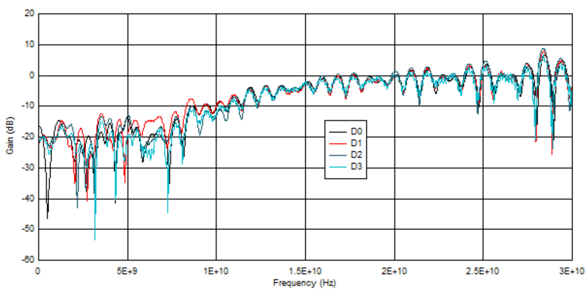


Figure 5-3. Input Differential Return Loss when port A is selected

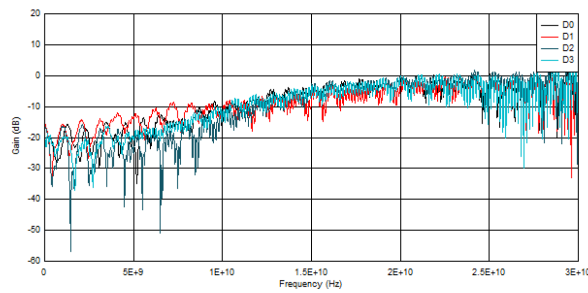


Figure 5-4. Output Differential Return Loss when port A is selected

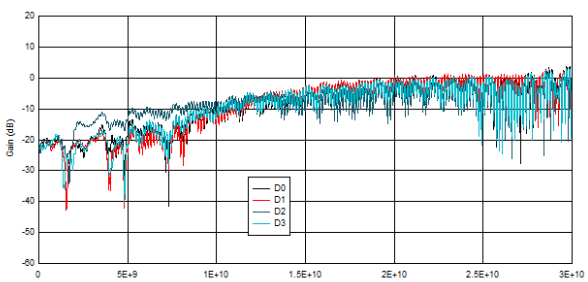


Figure 5-5. Output Differential Return Loss when port B is selected

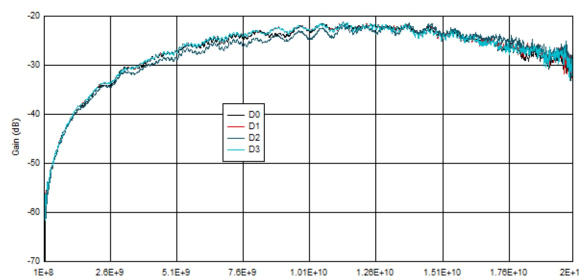


Figure 5-6. Off-State Isolation (OISO) for port A

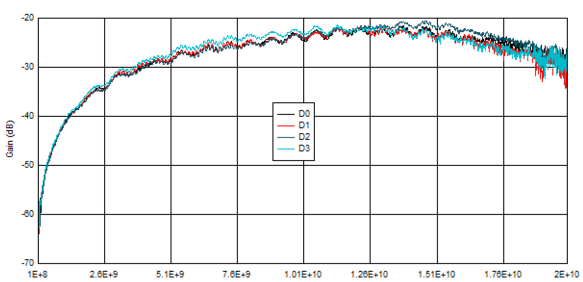


Figure 5-7. Off-State Isolation (OISO) for port B

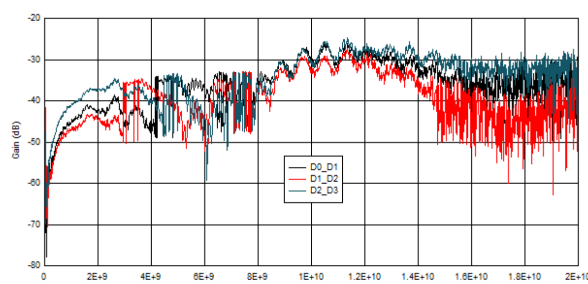
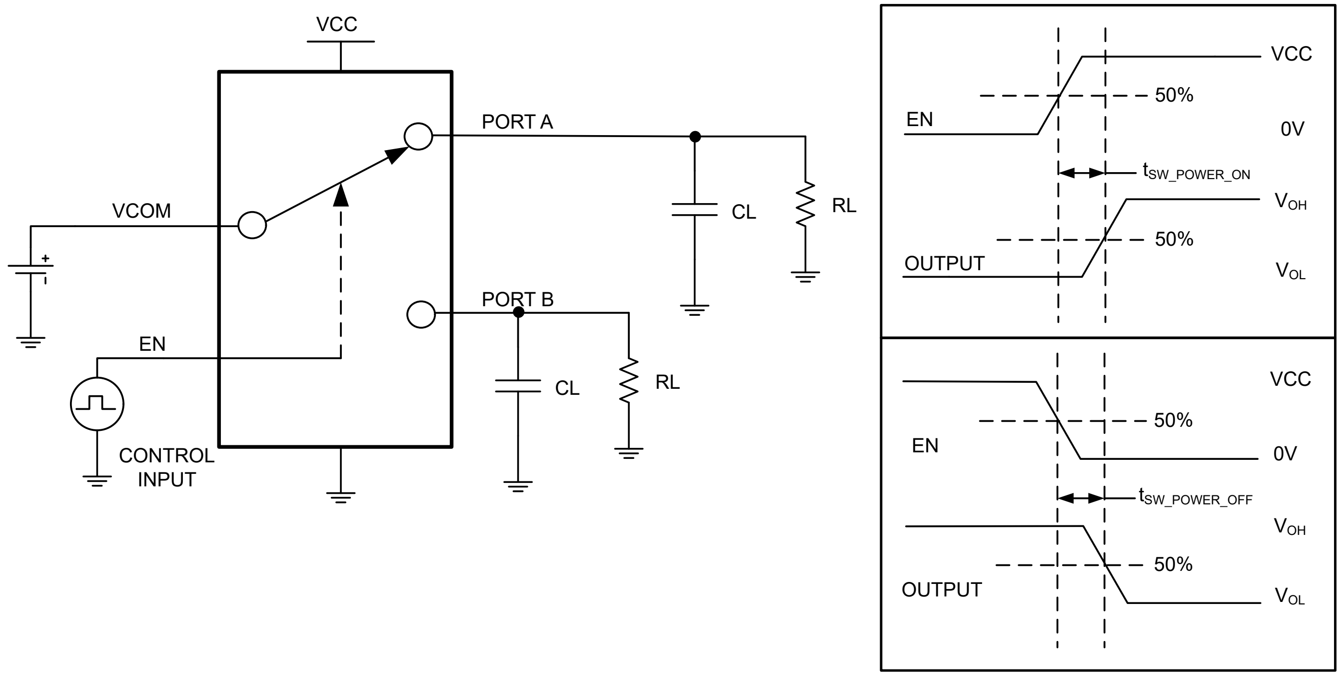


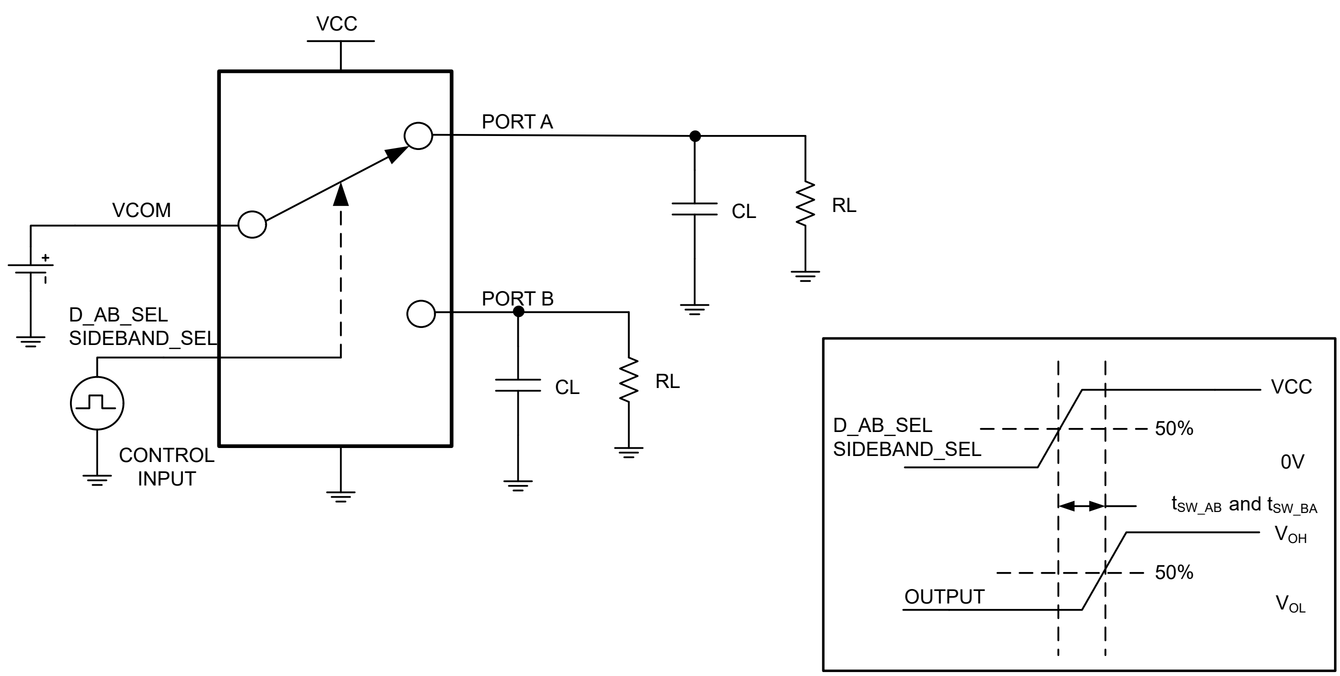
Figure 5-8. Crosstalk (Xtalk) between channels on common port side

6 Parameter Measurement Information



NOTE: RL = 10kΩ; VCOM = VCC; CL = 1pF

Figure 6-1. Switch Turn-On Time ($t_{SW\_POWER\_ON}$ and $t_{SW\_POWER\_OFF}$)



RL = 10kΩ; VCOM = VCC; CL = 1pF

Figure 6-2. Switching Time Between Channels (t_{SW_AB} and t_{SW_BA})

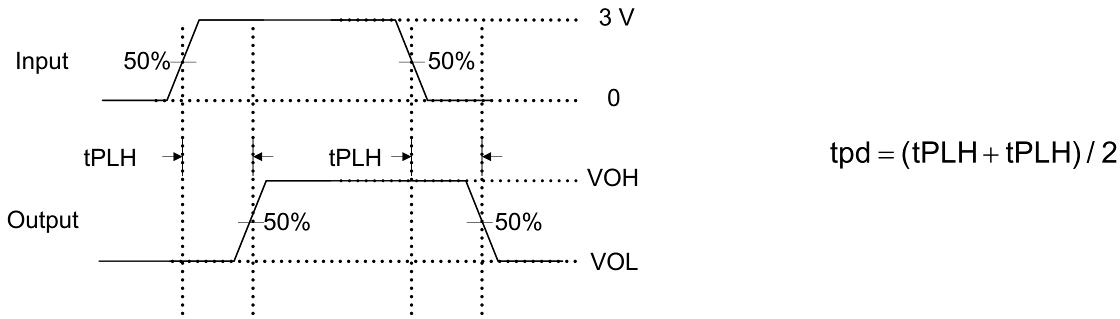


Figure 6-3. Propagation Delay (t_{pd})

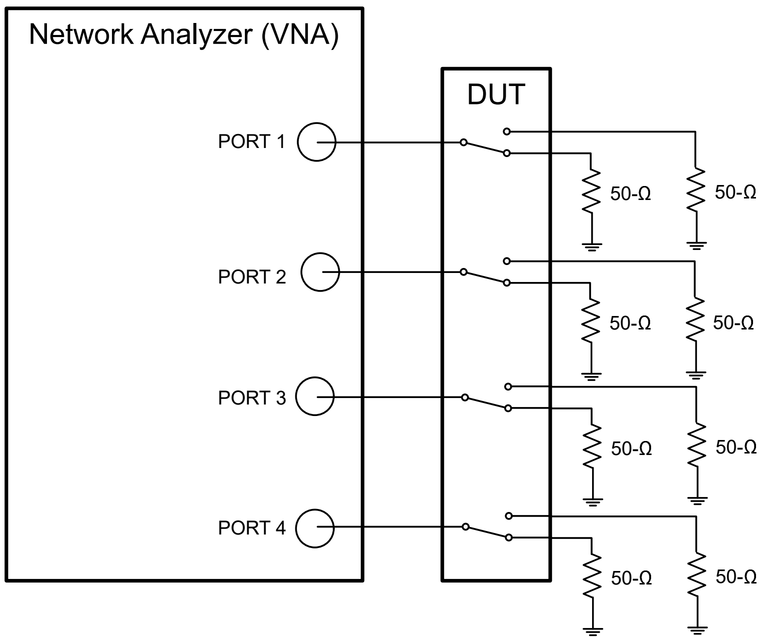


Figure 6-4. Crosstalk (Xtalk)

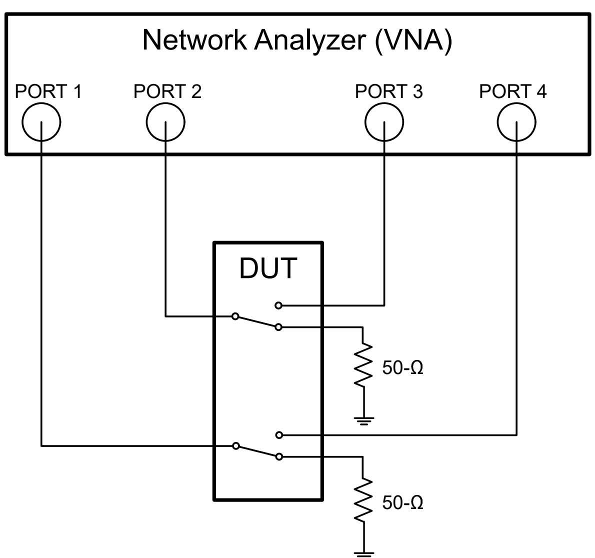


Figure 6-5. Differential Off-Isolation (OISO)

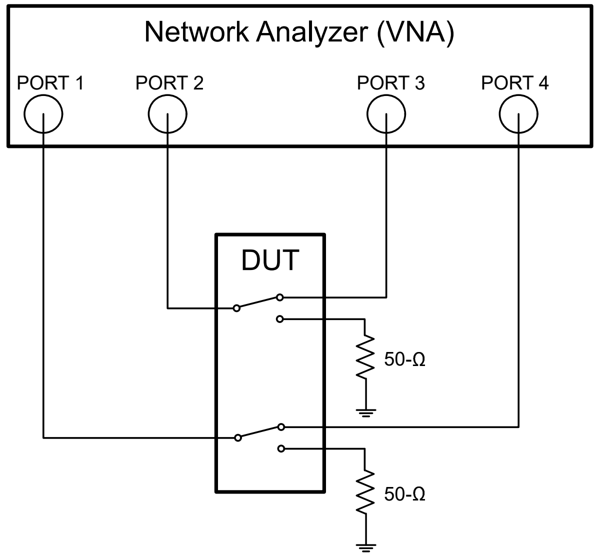


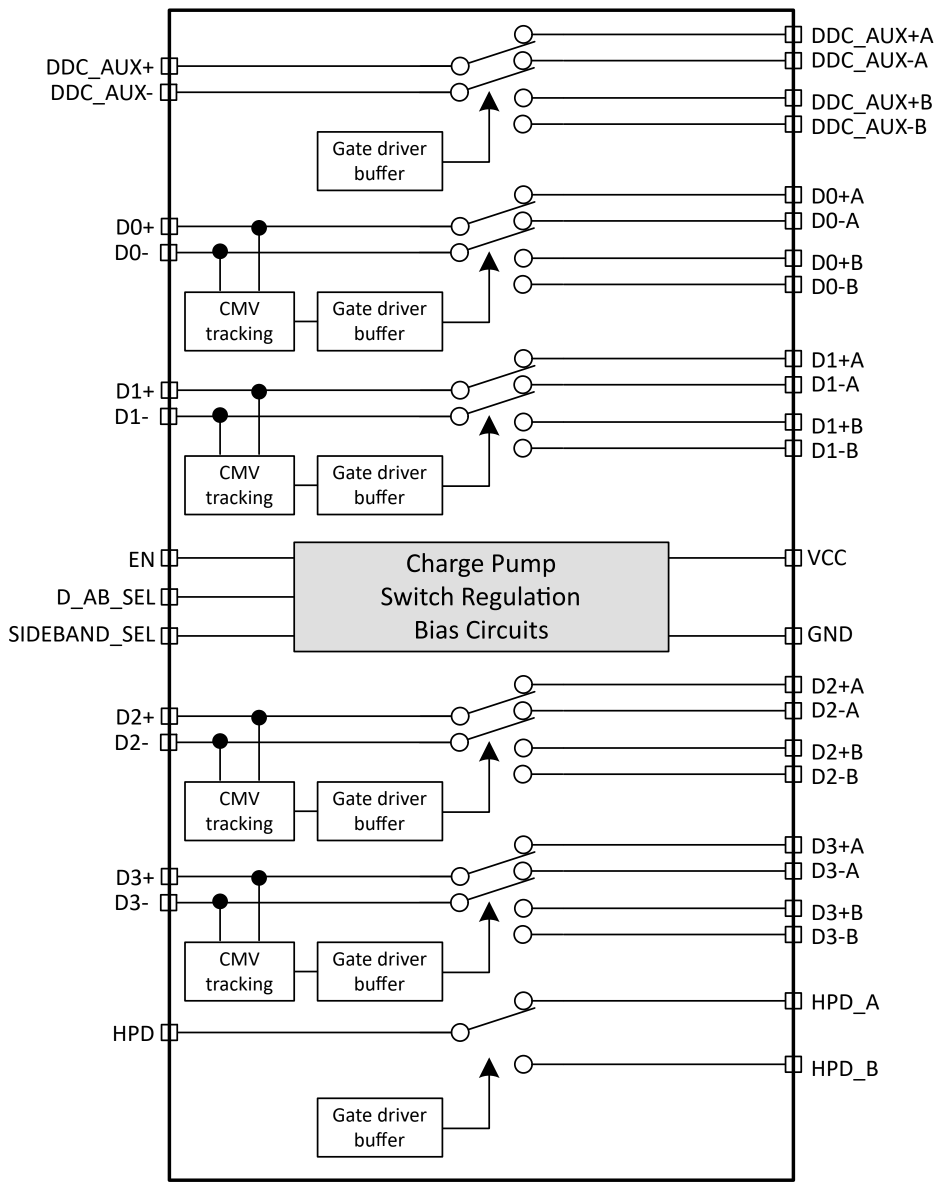
Figure 6-6. Differential Bandwidth (BW), Insertion Loss, and Return Loss

7 Detailed Description

7.1 Overview

The TMUXHS4512 is a protocol agnostic bidirectional multiplexer/demultiplexer that offers low on-state resistance as well as low I/O capacitance, which allows the device to achieve a high bandwidth of 13.0GHz typical for differential channels. The TMUXHS4512 is a passive mux that is recommended for data rates up to 20Gbps. However, the device can be used for interfaces with higher data rates if overall electrical link loss permits. The high-speed data channels of the device provide the high bandwidth necessary for many interfaces to handle differential as well as single-ended signals as long as the single-ended signals do not violate $V_{P\text{-}N\_ABSMAX}$. The high-speed channels of the device support differential signaling with common-mode voltage range (CMV) of 0V to 1.0V. The sideband channels are 5V tolerant. The sideband channels support 0V to 1.8V CMOS signals with a typical R_{ON} of 8.5Ω.

7.2 Functional Block Diagram



7.3 Feature Description

The TMUXHS4512 is based on proprietary TI technology which uses FET switches driven by a high-voltage generated from an integrated charge-pump to achieve a low on-state resistance. The TMUXHS4512's low power technology uses only 500µA in active and just 2µA in powerdown (EN = L) mode. The device has integrated ESD that can support up to 1.5kV Human-Body Model (HBM) and 750V Charge Device Model (CDM). The TMUXHS4512 also has a special feature that prevents the device from back-powering when the V_{CC} supply is not available and an analog signal is applied on the I/O pin. In this situation this special feature prevents leakage current in the device. The TMUXHS4512 is not designed for passing signals with negative swings.

7.4 Device Functional Modes

Table 7-1 lists the device functions for the TMUXHS4512 device.

Table 7-1. Functional Table

EN	D_AB_SEL	SIDEBAND_SEL	FUNCTION
L	X	X	Switch disabled. All channels are Hi-Z.
H	L	L	All A channels are enabled. All B channels are Hi-Z.
H	L	H	All A data high-speed channels are enabled and B sideband channels are enabled. All other channels are Hi-Z.
H	H	L	All B data high-speed channels are enabled and A sideband channels are enabled. All other channels are Hi-Z.
H	H	H	All B channels are enabled. All A channels are Hi-Z.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUXHS4512 is a generic analog differential passive mux or demux that works for many high-speed differential interfaces with data rates up to 20Gbps. The TMUXHS4512 supports differential signaling with common-mode voltage range (CMV) of 0V to 1.0V and with differential amplitude up to 1600mVpp in Dxx channels. The device can be also used for single-ended CMOS signals with swing limited to 0V to 1.8V in sideband channels. The TMUXHS4512 can be used as mux or demux switch for:

- DisplayPort (DP) for up to UHBR20 for data rates up to 20Gbps
- USB4 and Thunderbolt (TBT) 3 or 4 for data rates up to 20Gbps

8.2 Typical Application - DisplayPort

The TMUXHS4512 can be used to switch DisplayPort signals in both source and sink applications. In source applications DisplayPort port from a graphics processor can be demultiplexed into one of the two connectors or DisplayPort sinks. In a PC the TMUXHS4512 can be used to switch integrated graphics versus discrete graphics to a connector or sink. In a sink application the device also can be used to select between two connectors or DisplayPort sources to provide DisplayPort signals into a scaler (SOC) in sink application. This section provides detailed design implementation for a sink application where TMUXHS4512 provides 2:1 demultiplexing function.

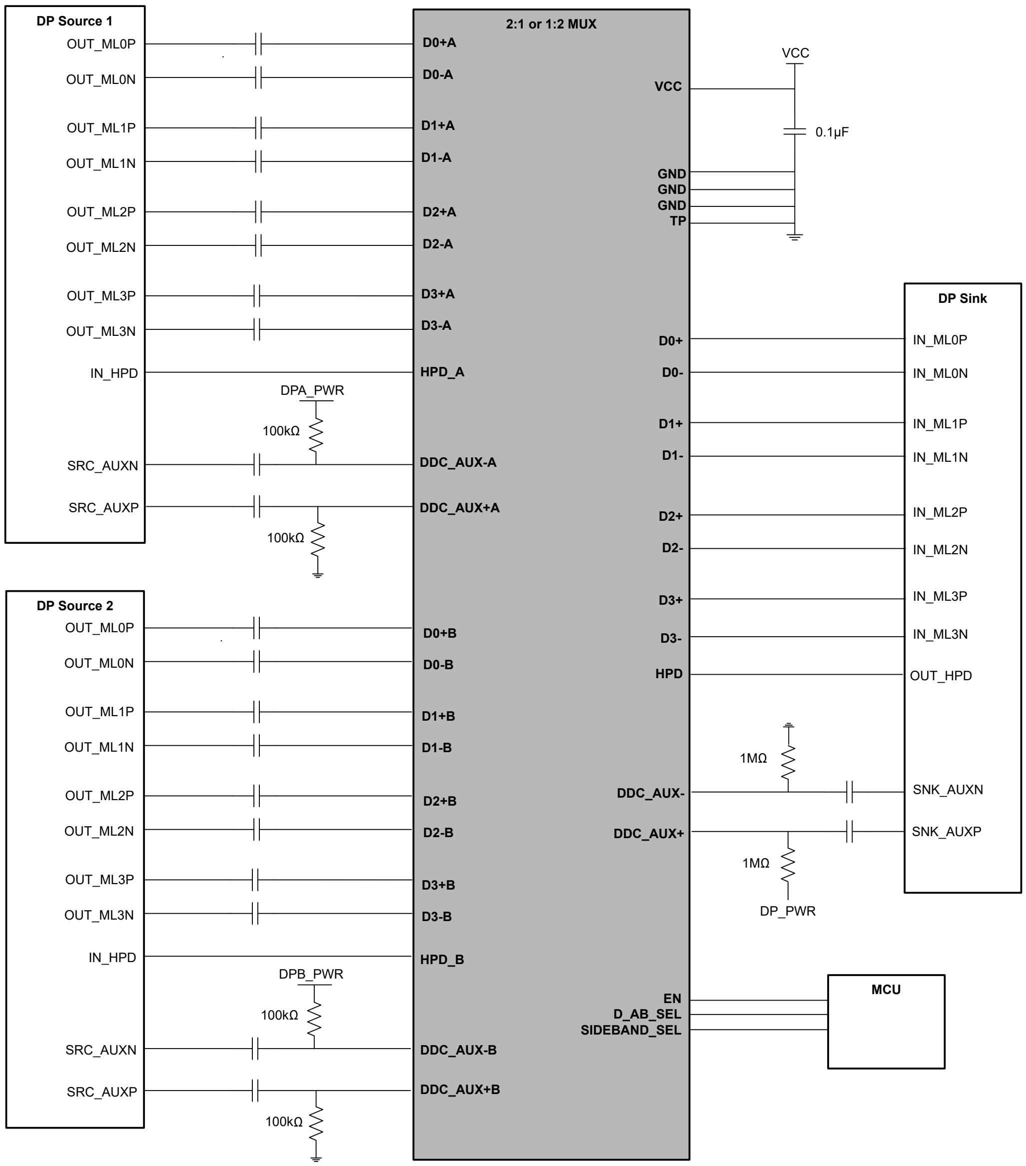


Figure 8-1. Choosing One of Two DisplayPorts - Application Schematic

8.2.1 Design Requirements

Table 8-1 lists the design parameters for this DisplayPort example.

Table 8-1. Design Parameters for DisplayPort Application

Design parameter	Example value
V_{CC}	1.62V to 1.98V
VCC decoupling capacitor	0.1µF
AUXp resistors	Sink Side: 1MΩ to 3.3V Source Side: 100kΩ to GND
AUXn resistors	Sink Side: 1MΩ to GND Source Side: 100kΩ to 3.3V

8.2.2 Detailed Design Procedure

The TMUXHS4512 is designed to operate with 1.62V to 1.98V power supply. Decoupling capacitors can be used to reduce noise and improve power supply integrity. AUX pullup resistors to 3.3V and pull-down resistors to GND must be placed on the source and sink according to DisplayPort standard.

8.2.3 Application Curves

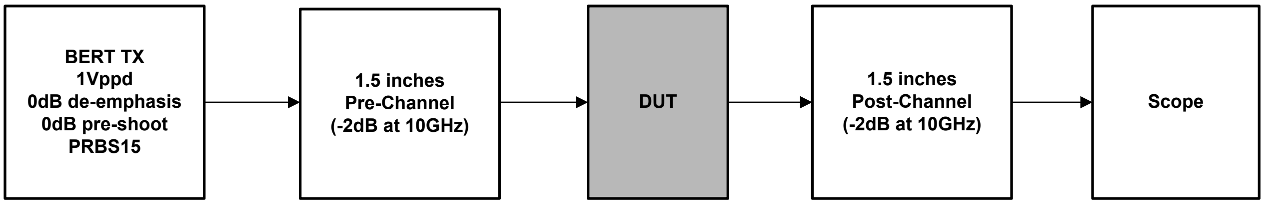


Figure 8-2. Test Setup

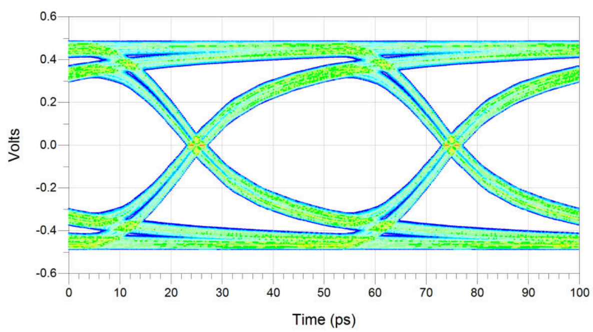


Figure 8-3. Eye Pattern: 20Gbps, No Device Through Path (Only One Channel Measured at a Time)

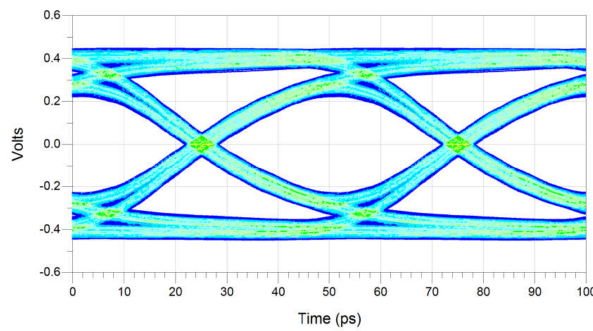


Figure 8-4. Eye Pattern: 20Gbps Port B, D0+ to D0+B, D0- to D0-B (Only One Channel Measured at a Time)

8.3 Power Supply Recommendations

Keep the V_{CC} in the range of 1.62V to 1.98V. Do not use voltage levels above those listed in the *Absolute Maximum Ratings* table. Use decoupling capacitors to reduce noise and improve power supply integrity. There are no power sequence requirements for the TMUXHS4512.

8.4 Layout

8.4.1 Layout Guidelines

To ensure reliability of the device, the following commonly used printed circuit board layout guidelines are recommended:

- Use decoupling capacitors between power supply pin and ground pin to ensure low impedance to reduce noise. To achieve a low impedance over a wide frequency range use capacitors with a high self-resonance frequency.
- Place ESD and EMI protection devices (if used) as close as possible to the connector.
- Use short trace lengths to avoid excessive loading.
- Keep traces at least two times the trace width apart to minimize the effects of crosstalk on adjacent traces.
- Separate high-speed signals from low-speed signals and digital from analog signals
- Avoid right-angle bends in a trace and try to route them at least with two 45° corners.
- Route the high-speed differential signal traces parallel to each other as much as possible. The traces are recommended to be symmetrical.
- Place a solid ground plane next to the high-speed signal layer. This also provides an excellent low-inductance path for the return current flow.

8.4.2 Layout Example

The TMUXHS4512 application with a single controller interfacing between a common port and two separate ports.

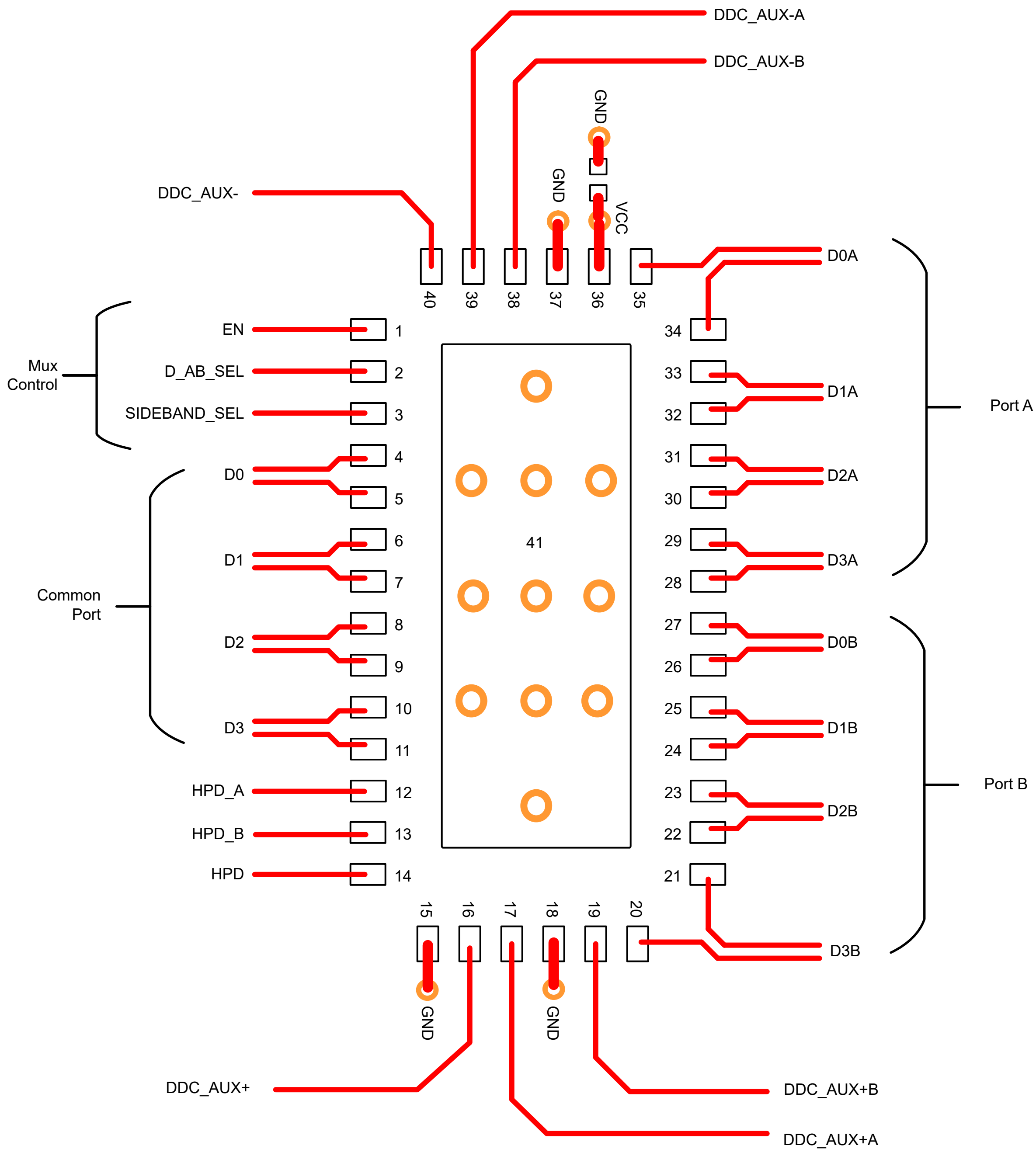


Figure 8-5. Layout Example

8.5 Systems Examples

8.5.1 DisplayPort 1:2 Mulitplexing

The TMUXHS4512 supports AC-coupled interfaces such as DisplayPort. External AC-coupling capacitors must be used on either the common side or the non-common side of the device. In this particular example, the external AC-coupling capacitors are placed on the common side. The non-common side is DC-coupled to the DP sinks. The choice of DC-coupling the non-common side or the common side is based on which DP source or DP sink meets the $V_{IO,CM}$ requirements of the device. If the DP source does not comply to the $V_{IO,CM}$ requirement, then place the AC-coupling capacitors between the DP source and TMUXHS4512. If the DP sink does not comply to the $V_{IO,CM}$ requirement, then place the AC-coupling capacitors between the DP sink and TMUXHS4512.

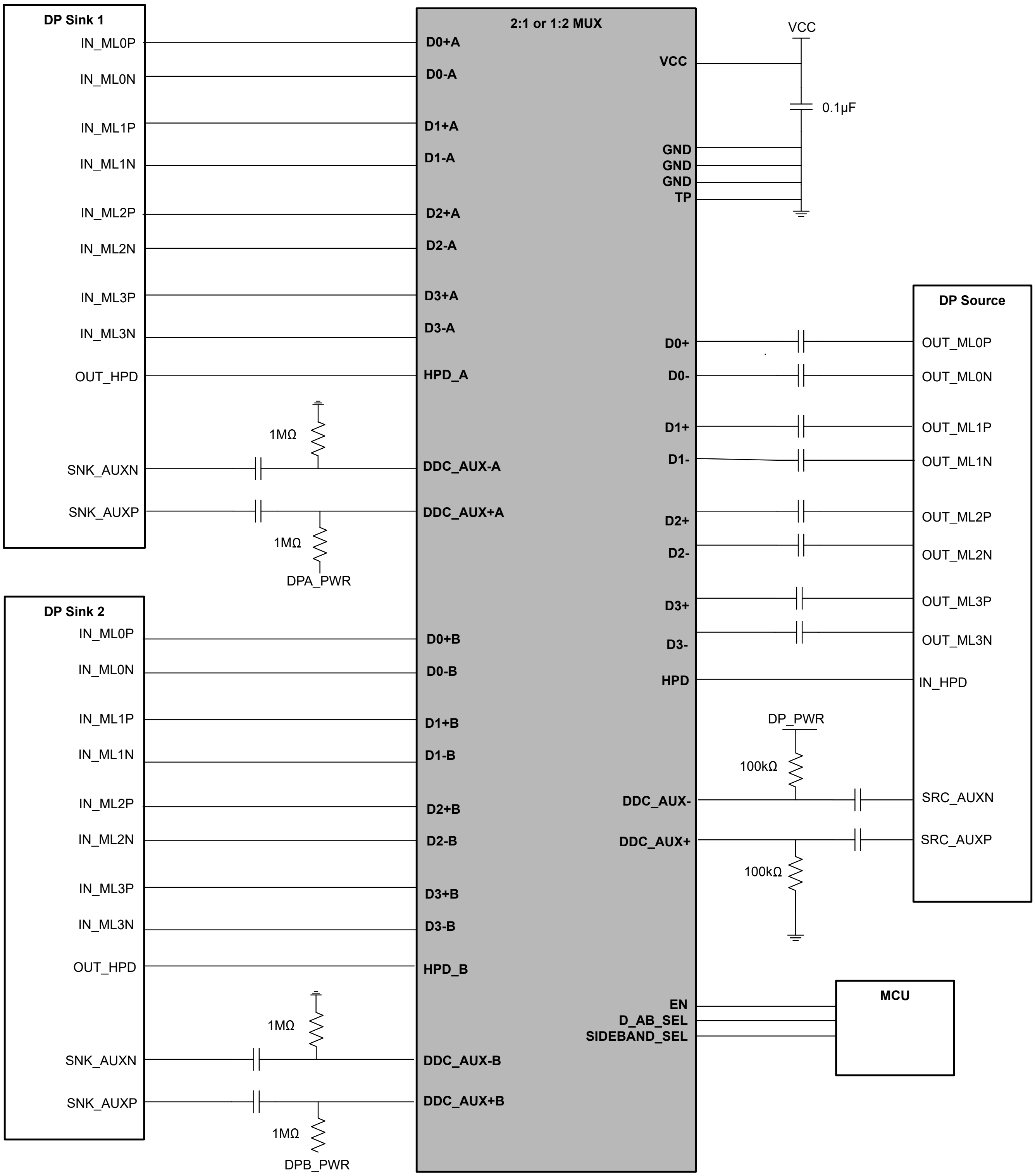


Figure 8-6. DisplayPort 1:2 Switching

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUXHS4512IRETR	Active	Production	WQFN (RET) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMX412
TMUXHS4512IRETR.A	Active	Production	WQFN (RET) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TMUXHS4512IRETR	TMX412
TMUXHS4512IRETT	Active	Production	WQFN (RET) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMX412
TMUXHS4512IRETT.A	Active	Production	WQFN (RET) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TMUXHS4512IRETT	TMX412
TMUXHS4512RETR	Active	Production	WQFN (RET) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 105	TMX412
TMUXHS4512RETR.A	Active	Production	WQFN (RET) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TMUXHS4512RETR	TMX412
TMUXHS4512RETT	Active	Production	WQFN (RET) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 105	TMX412
TMUXHS4512RETT.A	Active	Production	WQFN (RET) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TMUXHS4512RETT	TMX412

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

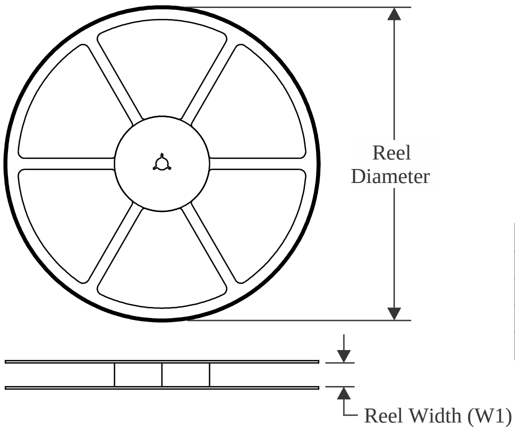
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

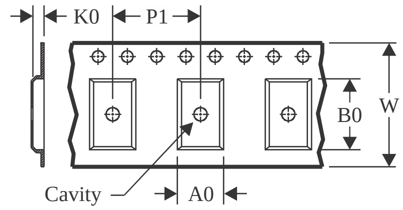
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

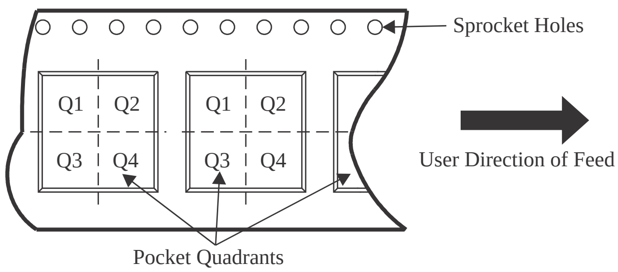


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

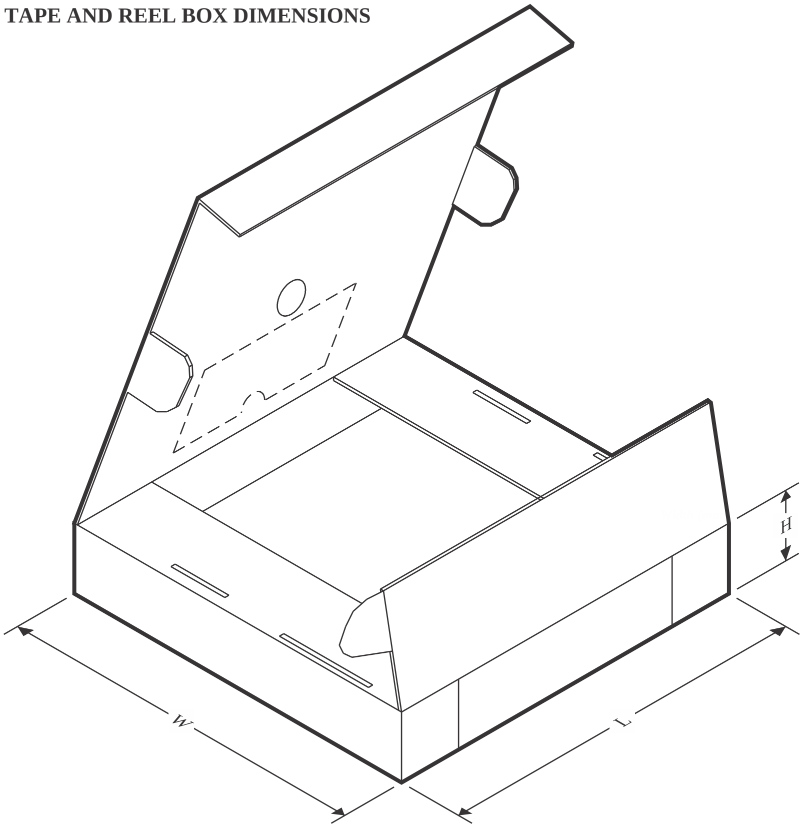
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

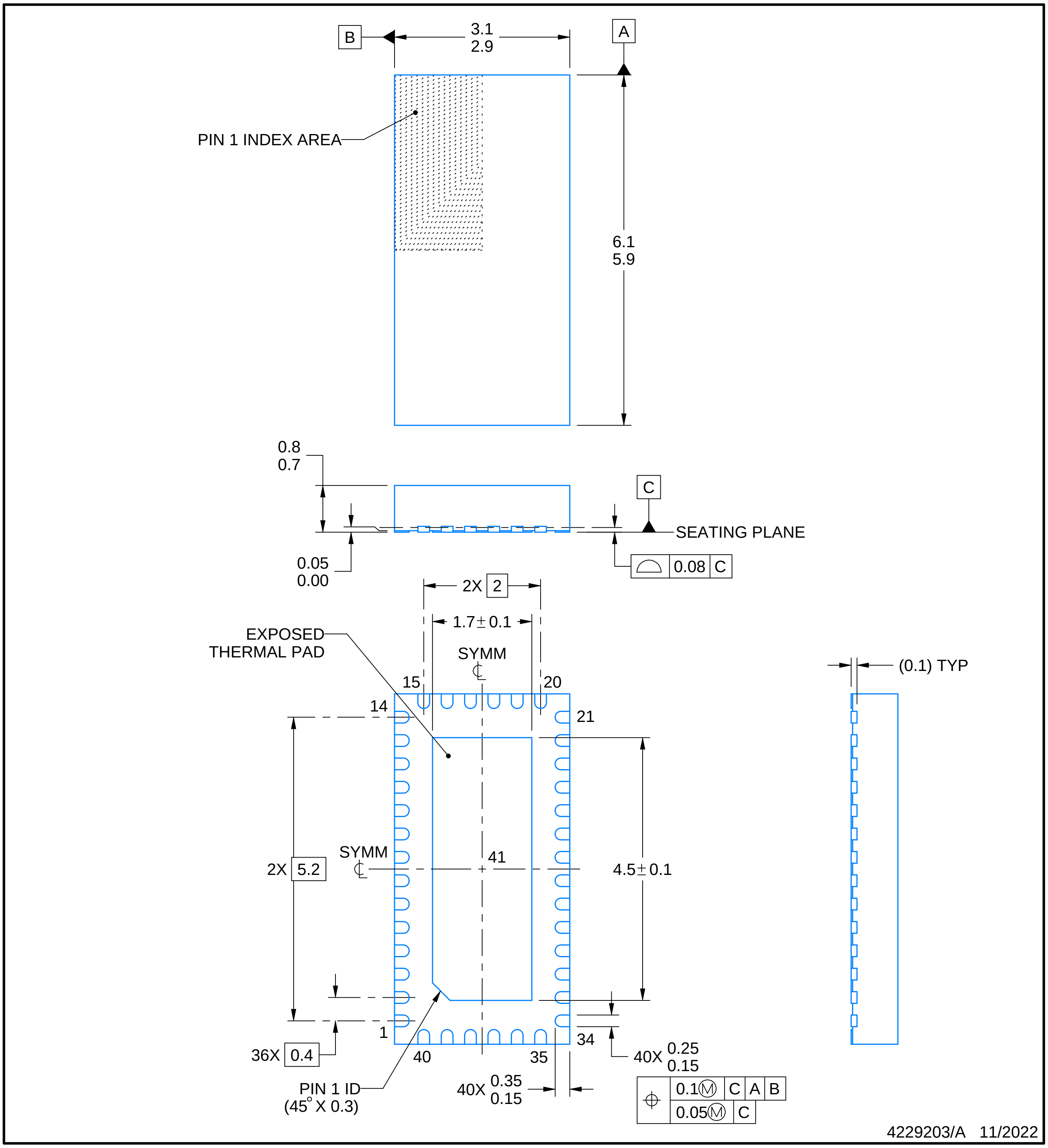
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUXHS4512IRETR	WQFN	RET	40	3000	330.0	16.4	3.3	6.3	1.0	8.0	16.0	Q1
TMUXHS4512IRETT	WQFN	RET	40	250	180.0	16.4	3.3	6.3	1.0	8.0	16.0	Q1
TMUXHS4512RETR	WQFN	RET	40	3000	330.0	16.4	3.3	6.3	1.0	8.0	16.0	Q1
TMUXHS4512RETT	WQFN	RET	40	250	180.0	16.4	3.3	6.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



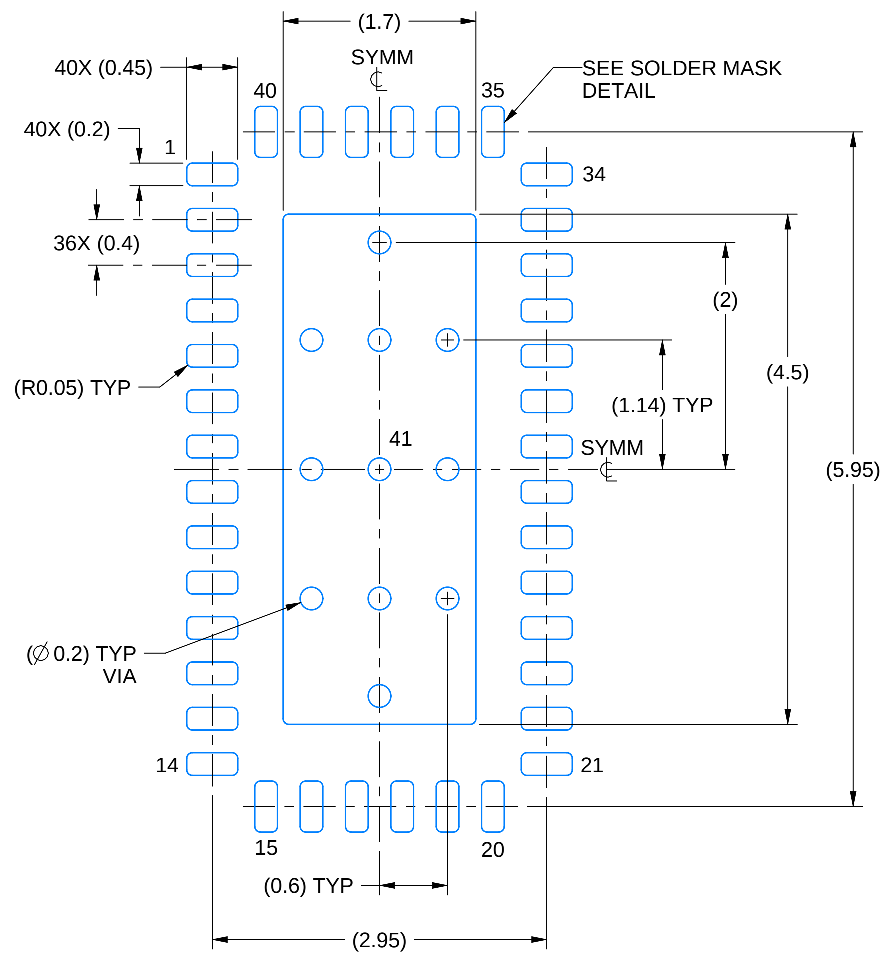
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUXHS4512IRETR	WQFN	RET	40	3000	367.0	367.0	38.0
TMUXHS4512IRETT	WQFN	RET	40	250	213.0	191.0	35.0
TMUXHS4512RETR	WQFN	RET	40	3000	367.0	367.0	38.0
TMUXHS4512RETT	WQFN	RET	40	250	213.0	191.0	35.0

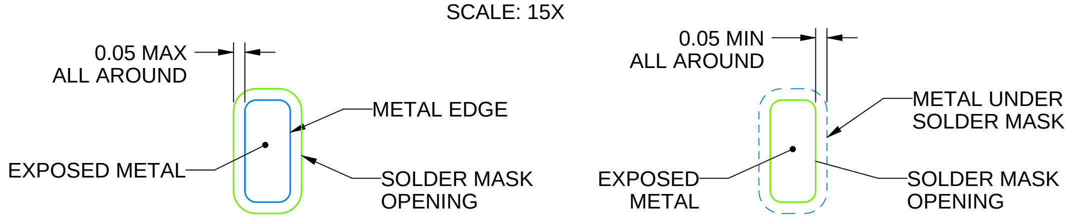


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

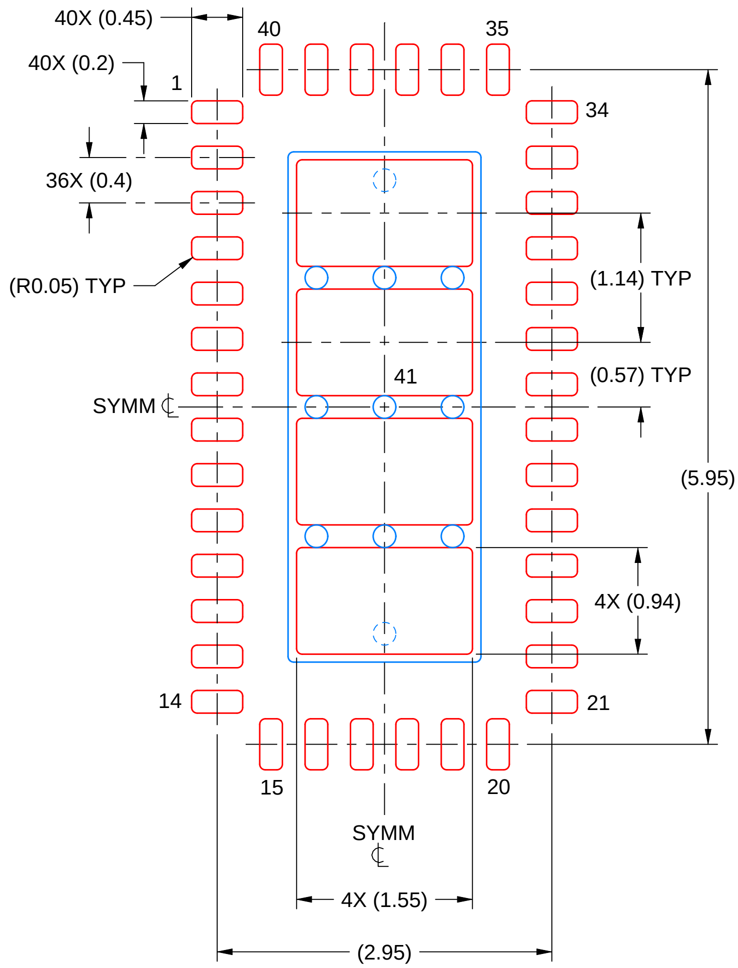
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4229203/A 11/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4229203/A 11/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.