







TMUX6221, TMUX6222

SCDS452B - MARCH 2023 - REVISED MAY 2024

TMUX622x 36 V, Low-RON, 1:1 (SPST), 2-Channel Switches with 1.8-V Logic

1 Features

Dual supply range: ±4.5 V to ±18 V

Single supply range: 4.5 V to 36 V

Low on-resistance: 2.1 Ω

-40°C to +125°C operating temperature

1.8 V logic compatible

Integrated pull-down resistor on logic pins

Fail-safe logic

Rail-to-rail operation

Bidirectional operation

2 Applications

Wired networking

Remote radio units

Patient monitoring and diagnostics

Ultrasound scanners

Optical test equipment

Optical networking

Factory automation and industrial controls

Programmable logic controllers (PLC)

Analog input modules

AC charging (pile) station

Semiconductor test

Data acquisition systems

Gas meters

Flow transmitters

3 Description

The TMUX622x are complementary metal-oxide semiconductor (CMOS) switch in a dual channel, 1:1 (SPST) configuration. The device works with a single supply (4.5 V to 36 V), dual supplies (±4.5 V to ±18 V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = -5 V). The TMUX622x supports bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from V_{SS} to V_{DD}.

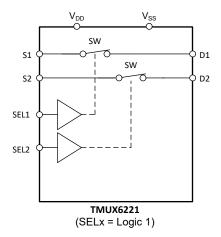
The TMUX622x can be enabled or disabled by controlling the SEL pins, turning on signal path 1 (S1 to D1) or signal path 2 (S2 to D2). All logic control inputs support logic levels from 1.8 V to V_{DD}, allowing for both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

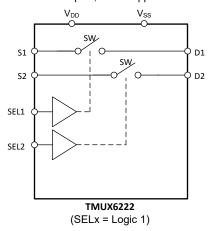
The TMUX622x is part of the precision switches and multiplexers family of devices. These devices have very low on and off leakage currents, 50 pA, allowing them to be used in high precision measurement applications.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾		
TMUX6221 TMUX6222	DGS (VSSOP, 10)	3 mm × 4.9 mm		

- For more information, see Section 11 (1)
- The package size (length × width) is a nominal value and includes pins, where applicable.





Block Diagram



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4 Pin Configuration and Functions

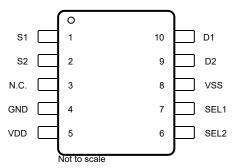


Figure 4-1. DGS Package, 10-Pin VSSOP (Top View)

Table 4-1. Pin Functions

F	PIN TYPE ⁽¹⁾ DESCRIPTION ⁽²⁾		DESCRIPTION(2)
NAME	NO.	ITPE(")	DESCRIPTION [/]
S1	1	I/O	Source pin 1. Can be an input or output.
S2	2	I/O	Source pin 2. Can be an input or output.
N.C.	3	_	No internal connection. Can be shorted to GND or left floating.
GND	4	Р	Ground (0 V) reference
V _{DD}	5	Р	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V _{DD} and GND.
SEL2	6	I	Logic control input, has internal pull-down resistor. Controls the switch connection. For more information, see Section 7.5.
SEL1	7	I	Logic control input, has internal pull-down resistor. Controls the switch connection. For more information, see Section 7.5.
V _{SS}	8	Р	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{SS} and GND.
D2	9	I/O	Drain pin 2. Can be an input or output.
D1	10	I/O	Drain pin 1. Can be an input or output.

- (1) I = input, O = output, I/O = input and output, P = power.
- (2) For what to do with unused pins, refer to Section 7.4.



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

	38	V
-0.5	38	V
-38	0.5	V
-0.5	38	V
-30	30	mA
V _{SS} -0.5	V _{DD} +0.5	V
-30	30	mA
	I _{DC} + 10 % ⁽⁴⁾	mA
-55	150	°C
-65	150	°C
	150	°C
	450	mW
	-38 -0.5 -30 V _{SS} -0.5 -30	-0.5 38 -38 0.5 -0.5 38 -30 30 V _{SS} -0.5 V _{DD} +0.5 -30 30 I _{DC} + 10 % ⁽⁴⁾ -55 150 -65 150

⁽¹⁾ Operation outside the Absolute Maximum Rating may cause permanent device damage. Absolute Maximum Rating do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Condition. If used outside the Recommended Operating Condition but within the Absolute Maximum Rating, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (4) Refer to Source or Drain Continuous Current table for I_{DC} specifications.
- (5) For VSSOP package: P_{tot} derates linearly above $T_A = 70^{\circ}\text{C}$ by 6.7mW/°C.

5.2 ESD Ratings

			VALUE	UNIT
TMUX622x				
V		Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	W
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins ⁽²⁾	±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Thermal Information

		TMUX622x	
	THERMAL METRIC(1)	DGS (VSSOP)	UNIT
		10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	154.3	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	52.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	73.9	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
$V_{DD} - V_{SS}$ (1)	Power supply voltage differential	4.5	36	V
V_{DD}	Positive power supply voltage	4.5	36	V
V _S or V _D	Signal path input/output voltage (source or drain pin) (Sx, D)	V _{SS}	V_{DD}	V
V _{SEL} or V _{EN}	Address or enable pin voltage	0	36	V
I _S or I _{D (CONT)}	Source or drain continuous current (Sx, D)		I _{DC} ⁽²⁾	mA
T _A	Ambient temperature	-40	125	°C

⁽¹⁾ V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} − V_{SS}) ≤ 36 V, and the minimum V_{DD} is met.

5.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINU	CONTINUOUS CURRENT PER CHANNEL (IDC) (2)		T _Δ = 85°C	T _Δ = 125°C	UNIT
PACKAGE	TEST CONDITIONS	T _A = 25°C	1A - 65 C	1A - 125 C	UNIT
DGS (VSSOP)	+36 V Single Supply ⁽¹⁾	360	250	130	mA
	±15 V Dual Supply	380	260	130	mA
	+12 V Single Supply	280	190	100	mA
	±5 V Dual Supply	240	160	90	mA

⁽¹⁾ Specified for nominal supply voltage only.

⁽²⁾ Refer to Source or Drain Continuous Current table for I_{DC} specifications.

⁽²⁾ Refer to Total power dissipation (P_{tot}) limits in *Absolute Maximum Ratings* table that must be followed with max continuous current specification.



5.6 ±15 V Dual Supply: Electrical Characteristics

 V_{DD} = +15 V ± 10%, V_{SS} = -15 V ±10%, GND = 0 V (unless otherwise noted) Typical at V_{DD} = +15 V, V_{SS} = -15 V, T_A = 25°C (unless otherwise noted)

Typical at	PARAMETER	TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
ANALOG	SWITCH						
			25°C		2.1	2.9	Ω
R _{ON}	On-resistance	$V_S = -10 \text{ V to } +10 \text{ V}$ $I_D = -10 \text{ mA}$	–40°C to +85°C			3.8	Ω
			-40°C to +125°C			4.5	Ω
			25°C		0.05	0.25	Ω
ΔR_{ON}	On-resistance mismatch between channels	$V_S = -10 \text{ V to } +10 \text{ V}$ $I_D = -10 \text{ mA}$	-40°C to +85°C			0.3	Ω
			-40°C to +125°C			0.35	Ω
			25°C		0.5	0.6	Ω
R _{ON FLAT}	On-resistance flatness	$V_S = -10 \text{ V to } +10 \text{ V}$ $I_S = -10 \text{ mA}$	-40°C to +85°C			0.7	Ω
		15 10 11 11	-40°C to +125°C			0.85	Ω
R _{ON DRIFT}	On-resistance drift	V _S = 0 V, I _S = -10 mA	-40°C to +125°C		0.01		Ω/°C
		V _{DD} = 16.5 V, V _{SS} = -16.5 V	25°C	-0.15	0.05	0.15	nA
I _{S(OFF)}	Source off leakage current ⁽¹⁾	Switch state is off V _S = +10 V / –10 V	-40°C to +85°C	-1.6		1.6	nA
, ,		$V_{\rm D} = -10 \text{ V} / + 10 \text{ V}$	-40°C to +125°C	-15		15	nA
		V_{DD} = 16.5 V, V_{SS} = -16.5 V Switch state is off V_{S} = +10 V / -10 V V_{D} = -10 V / + 10 V	25°C	-0.15	0.05	0.15	nA
I _{D(OFF)}	Drain off leakage current ⁽¹⁾		-40°C to +85°C	-1.6		1.6	nA
			-40°C to +125°C	-15		15	nA
		V _{DD} = 16.5 V, V _{SS} = –16.5 V	25°C	-0.15	0.05	0.15	nA
I _{S(ON)}	Channel on leakage current ⁽²⁾	Switch state is on	-40°C to +85°C	-1.6		1.6	nA
I _{D(ON)}		$V_S = V_D = \pm 10 \text{ V}$	-40°C to +125°C	-15		15	nA
LOGIC IN	PUTS (SEL / EN pins)						
V _{IH}	Logic voltage high		-40°C to +125°C	1.3		36	V
V _{IL}	Logic voltage low		-40°C to +125°C	0		0.8	V
I _{IH}	Input leakage current		-40°C to +125°C		1.5	2.5	μA
I _{IL}	Input leakage current		-40°C to +125°C	-0.1	-0.005		μA
C _{IN}	Logic input capacitance		-40°C to +125°C		3.5		pF
POWER S	SUPPLY						
			25°C		30	47	μA
I _{DD}	V _{DD} supply current	$V_{DD} = 16.5 \text{ V}, V_{SS} = -16.5 \text{ V}$ Logic inputs = 0 V, 5 V, or V_{DD}	-40°C to +85°C			55	μA
		20g.5 11 pate 0 v, 0 v, 01 v DD	-40°C to +125°C			72	μA
			25°C		7	15	μA
I _{SS}	V _{SS} supply current	$V_{DD} = 16.5 \text{ V}, V_{SS} = -16.5 \text{ V}$ Logic inputs = 0 V, 5 V, or V_{DD}	-40°C to +85°C			20	μA
		Logic inputs – 0 v, 5 v, or v _{DD}	-40°C to +125°C			30	μA

When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.

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When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.



5.7 ±15 V Dual Supply: Switching Characteristics

 V_{DD} = +15 V ± 10%, V_{SS} = -15 V ± 10%, GND = 0 V (unless otherwise noted) Typical at V_{DD} = +15 V, V_{SS} = -15 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T _A	MIN T	YP MAX	UNIT
			25°C		145 180	ns
t _{ON}	Turn-on time from control input	$V_S = 10 \text{ V}$ $R_I = 300 \Omega, C_I = 35 \text{ pF}$	–40°C to +85°C		190	ns
		11t_ 000 12, 0t_ 00 pi	-40°C to +125°C		145 180	ns
			25°C		100 180	ns
t _{OFF}	Turn-off time from control input	$V_S = 10 \text{ V}$ $R_1 = 300 \Omega, C_1 = 35 \text{ pF}$	-40°C to +85°C		195	ns
		11(000 11, OL 00 PI	-40°C to +125°C		210	ns
			25°C	0	.19	ms
t _{ON (VDD)}	Device turn on time (V _{DD} to output)	V_{DD} rise time = 1 μs R_L = 300 Ω, C_L = 35 pF	–40°C to +85°C		0.2	ms
	(VDD to suspat)	11(000 11, OL 00 PI	-40°C to +125°C		0.2	ms
t _{PD}	Propagation delay	$R_L = 50 \Omega$, $C_L = 5 pF$	25°C	;	500	ps
Q _{INJ}	Charge injection	V _S = 0 V, C _L = 100 pF	25°C		-15	pC
O _{ISO}	Off-isolation	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 0 V$, $f = 100 kHz$	25°C	-	-70	dB
O _{ISO}	Off-isolation	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 0 V$, $f = 1 MHz$	25°C	-	-50	dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 0 V$, $f = 100 kHz$	25°C	_	114	dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 0 V$, $f = 1MHz$	25°C	-	-93	dB
BW	–3dB Bandwidth	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 0 V$	25°C		45	MHz
IL	Insertion loss	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 0 V$, $f = 1 MHz$	25°C	-0	.18	dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C	-	-71	dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 15 \text{ V}, V_{BIAS} = 0 \text{ V}$ $R_L = 10 \text{ k}\Omega, C_L = 5 \text{ pF},$ $f = 20 \text{ Hz to } 20 \text{ kHz}$	25°C	0.00	005	%
C _{S(OFF)}	Source off capacitance	V _S = 0 V, f = 1 MHz	25°C		25	pF
C _{D(OFF)}	Drain off capacitance	V _S = 0 V, f = 1 MHz	25°C		33	pF
C _{S(ON),} C _{D(ON)}	On capacitance	V _S = 0 V, f = 1 MHz	25°C		120	pF



5.8 36 V Single Supply: Electrical Characteristics

 $V_{DD} = +36 \text{ V} \pm 10\%, V_{SS} = 0 \text{ V}, \text{GND} = 0 \text{ V} \text{ (unless otherwise noted)}$ $\text{Typical at V}_{DD} = +36 \text{ V}, V_{SS} = 0 \text{ V}, T_{A} = 25^{\circ}\text{C} \text{ (unless otherwise noted)}$

• •	PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG	SWITCH						
			25°C		2.5	3.2	Ω
R _{ON}	On-resistance	$V_S = 0 \text{ V to } 30 \text{ V}$ $I_D = -10 \text{ mA}$	–40°C to +85°C			4.2	Ω
			–40°C to +125°C			4.9	Ω
			25°C		0.1	0.22	Ω
ΔR_{ON}	On-resistance mismatch between channels	$V_S = 0 \text{ V to } 30 \text{ V}$ $I_D = -10 \text{ mA}$	–40°C to +85°C			0.25	Ω
	onamicis .		–40°C to +125°C			0.31	Ω
			25°C		0.3	1	Ω
R _{ON FLAT}	On-resistance flatness	$V_S = 0 \text{ V to } 30 \text{ V}$ $I_S = -10 \text{ mA}$	–40°C to +85°C			1.5	Ω
		IS TO TITA	–40°C to +125°C			2	Ω
R _{ON DRIFT}	On-resistance drift	V _S = 18 V, I _S = -10 mA	-40°C to +125°C		0.009		Ω/°C
		$V_{DD} = 39.6 \text{ V}, V_{SS} = 0 \text{ V}$	25°C	-0.25	0.05	0.25	nA
I _{S(OFF)}	Source off leakage current ⁽¹⁾	Switch state is off V _S = 30 V / 1 V	–40°C to +85°C	-3.5		3.5	nA
		$V_D = 1 \text{ V} / 30 \text{ V}$	–40°C to +125°C	-26		26	nA
	Drain off leakage current ⁽¹⁾	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V	25°C	-0.25	0.05	0.25	nA
I _{D(OFF)}			–40°C to +85°C	-3.5		3.5	nA
			-40°C to +125°C	-26		26	nA
		V _{DD} = 39.6 V, V _{SS} = 0 V	25°C	-0.25	0.05	0.25	nA
I _{S(ON)}	Channel on leakage current ⁽²⁾	Switch state is on	–40°C to +85°C	-3.5		3.5	nA
I _{D(ON)}		$V_S = V_D = 30 \text{ V or } 1 \text{ V}$	–40°C to +125°C	-26		4.2 4.9 0.22 0.25 0.31 1 1.5 2 0.25 3.5 26 0.25 3.5 26 0.25	nA
LOGIC IN	IPUTS (SEL / EN pins)						
V _{IH}	Logic voltage high		-40°C to +125°C	1.3		36	V
V _{IL}	Logic voltage low		-40°C to +125°C	0		0.8	V
I _{IH}	Input leakage current		–40°C to +125°C		0.5	2.75	μΑ
I _{IL}	Input leakage current		-40°C to +125°C	-0.1	-0.005		μΑ
C _{IN}	Logic input capacitance		-40°C to +125°C		3.5		pF
POWER S	SUPPLY		•				
		.,	25°C		50	60	μΑ
I_{DD}	V _{DD} supply current	$V_{DD} = 39.6 \text{ V}, V_{SS} = 0 \text{ V}$ Logic inputs = 0 V, 5 V, or V_{DD}	–40°C to +85°C			70	μΑ
		20gio inputo 0 v, 0 v, 0i v DD	–40°C to +125°C			3.2 4.2 4.9 0.22 0.25 0.31 1 1.5 2 0.25 3.5 26 0.25 3.5 26 0.25 3.5 26 0.25 3.5	μA

Product Folder Links: TMUX6221 TMUX6222

When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive. When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.



5.9 36 V Single Supply: Switching Characteristics

 $\begin{aligned} &V_{DD} = +36 \text{ V} \pm 10\%, \text{ V}_{SS} = 0 \text{ V}, \text{ GND} = 0 \text{ V} \text{ (unless otherwise noted)} \\ &\text{Typical at V}_{DD} = +36 \text{ V}, \text{ V}_{SS} = 0 \text{ V}, \text{ T}_{A} = 25^{\circ}\text{C} \text{ (unless otherwise noted)} \end{aligned}$

PARAMETER		TEST CONDITIONS	T _A	MIN TY	P MAX	UNIT
			25°C	11	0 180	ns
t _{ON}	Turn-on time from control input	$V_S = 18 \text{ V}$ $R_L = 300 \Omega, C_L = 35 \text{ pF}$	–40°C to +85°C		190	ns
		11t_ 000 12, 0t_ 00 pi	–40°C to +125°C		200	ns
			25°C	9	0 180	ns
t _{OFF}	Turn-off time from control input	$V_S = 18 \text{ V}$ $R_1 = 300 \Omega, C_1 = 35 \text{ pF}$	–40°C to +85°C		195	ns
		1.1 000 11, 0[00 p.	-40°C to +125°C		200	ns
			25°C	0.1	7	ms
t _{ON (VDD)}	Device turn on time (V _{DD} to output)	V_{DD} rise time = 1 μs R_1 = 300 Ω, C_1 = 35 pF	–40°C to +85°C	0.1	9	ms
	(VDD to output)	11, 000 12, 01 00 pi	–40°C to +125°C	0.1	9	ms
t _{PD}	Propagation delay	$R_L = 50 \Omega$, $C_L = 5 pF$	25°C	50	0	ps
Q _{INJ}	Charge injection	V _S = 18 V, C _L = 100 pF	25°C	-1	3	рC
O _{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C	-7	-70	
O _{ISO}	Off-isolation	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 6 V$, $f = 1 MHz$	25°C	-50		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 6 V$, $f = 100 kHz$	25°C	-11	2	dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 6 V$, $f = 1 MHz$	25°C	-9	3	dB
BW	–3dB Bandwidth	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 6 V$	25°C	4	5	MHz
IL	Insertion loss	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 6 V$, $f = 1 MHz$	25°C	-0.1	9	dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	V _{DD} and V _{SS} 5 pF, 25°C		1	dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 18 V, V_{BIAS} = 18 V R_{L} = 10 k Ω , C_{L} = 5 pF, f = 20 Hz to 20 kHz	25°C	0.000	4	%
C _{S(OFF)}	Source off capacitance	V _S = 18 V, f = 1 MHz	25°C	2	6	pF
C _{D(OFF)}	Drain off capacitance	V _S = 18 V, f = 1 MHz	25°C	3	5	pF
C _{S(ON)} , C _{D(ON)}	On capacitance	V _S = 18 V, f = 1 MHz	25°C	12	0	pF



5.10 12 V Single Supply: Electrical Characteristics

 V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted) Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

TEST CONDITIONS MIN UNIT **PARAMETER TYP** MAX T_A **ANALOG SWITCH** 25°C 4.6 6 Ω $V_{S} = 0 \ V \text{ to } 10 \ V$ -40°C to +85°C 7.5 Ω R_{ON} On-resistance $I_{D} = -10 \text{ mA}$ -40°C to +125°C 8.4 Ω 25°C 0.08 0.2 Ω $V_S = 0 V \text{ to } 10 V$ On-resistance mismatch between ΔR_{ON} -40°C to +85°C 0.32 Ω channels $I_D = -10 \text{ mA}$ -40°C to +125°C Ω 0.35 25°C 1.2 2 0 $V_{S} = 0 \ V \text{ to } 10 \ V$ $R_{\text{ON FLAT}}$ On-resistance flatness -40°C to +85°C 2.2 Ω $I_{S} = -10 \text{ mA}$ -40°C to +125°C 2.4 Ω -40°C to +125°C Ω/°C $V_S = 6 \text{ V}, I_S = -10 \text{ mA}$ 0.017 R_{ON DRIFT} On-resistance drift $V_{DD} = 13.2 \text{ V}, V_{SS} = 0 \text{ V}$ 25°C -0.50.05 0.5 nΑ Switch state is off Source off leakage current(1) -40°C to +85°C -2 2 nΑ I_{S(OFF)} $V_S = 10 V / 1 V$ -40°C to +125°C -12 $V_D = 1 V / 10 V$ 12 nΑ $V_{DD} = 13.2 \text{ V}, V_{SS} = 0 \text{ V}$ 25°C 0.5 -0.50.05 nΑ Switch state is off -40°C to +85°C -2 2 Drain off leakage current(1) nΑ I_{D(OFF)} $V_S = 10 V / 1 V$ $V_D = 1 V / 10 V$ -40°C to +125°C -1212 nΑ 25°C -0.50.05 0.5 nΑ $V_{DD} = 13.2 \text{ V}, V_{SS} = 0 \text{ V}$ I_{S(ON)} -40°C to +85°C -2 2 Channel on leakage current⁽²⁾ Switch state is on nΑ $I_{D(ON)}$ $V_S = V_D = 10 \text{ V or } 1 \text{ V}$ -40°C to +125°C 12 -12nΑ LOGIC INPUTS (SEL / EN pins) -40°C to +125°C ٧ V_{IH} Logic voltage high 1.3 36 -40°C to +125°C 0 0.8 V_{IL} Logic voltage low V Input leakage current -40°C to +125°C 0.5 2.5 μΑ

-40°C to +125°C

-40°C to +125°C

-40°C to +85°C

-40°C to +125°C

25°C

-0.1

-0.005

3.5

30

μΑ

pF

μΑ

μΑ

μΑ

40

50

62

 $V_{DD} = 13.2 \text{ V}, V_{SS} = 0 \text{ V}$

Logic inputs = 0 V, 5 V, or V_{DD}

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Input leakage current

V_{DD} supply current

Logic input capacitance

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I_{IН} I_{IL}

 I_{DD}

POWER SUPPLY

⁽¹⁾ When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.

⁽²⁾ When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.



5.11 12 V Single Supply: Switching Characteristics

 V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted) Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN TYP	MAX	UNIT
			25°C	120	180	ns
t _{ON}	Turn-on time from control input	$V_S = 8 V$ $R_L = 300 \Omega, C_L = 35 pF$	–40°C to +85°C		210	ns
		11t_ 000 12, 0t_ 00 pi	–40°C to +125°C		230	ns
			25°C	130	210	ns
t _{OFF}	Turn-off time from control input	$V_S = 8 V$ $R_1 = 300 \Omega, C_1 = 35 pF$	-40°C to +85°C		235	ns
			-40°C to +125°C		250	ns
	D : ("		25°C	0.19		ms
t _{ON (VDD)}	Device turn on time (V _{DD} to output)	V_{DD} rise time = 1 μs R_L = 300 Ω, C_L = 35 pF	-40°C to +85°C	0.2		ms
	(188 11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		–40°C to +125°C	0.2		ms
t_{PD}	Propagation delay	$R_L = 50 \Omega$, $C_L = 5 pF$	25°C	500		ps
Q_{INJ}	Charge injection	V _S = 6 V, C _L = 100 pF	25°C	-6		рC
O _{ISO}	Off-isolation	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 6 V$, $f = 100 kHz$	25°C	-70		dB
O _{ISO}	Off-isolation	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 6 V$, $f = 1 MHz$ $25^{\circ}C$ -50			dB	
X _{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C	-112		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 6 V$, $f = 1 MHz$	25°C	-93		dB
BW	–3dB Bandwidth	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 6 V$	25°C	60		MHz
IL	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C	-0.3		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C	-76		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 6 \text{ V}, V_{BIAS} = 6 \text{ V}$ $R_{L} = 10 \text{ k}\Omega$, $C_{L} = 5 \text{ pF}$, f = 20 Hz to 20 kHz	25°C	0.0009		%
C _{S(OFF)}	Source off capacitance	V _S = 6 V, f = 1 MHz	25°C	30		pF
C _{D(OFF)}	Drain off capacitance	V _S = 6 V, f = 1 MHz	25°C	38		pF
C _{S(ON)} , C _{D(ON)}	On capacitance	V _S = 6 V, f = 1 MHz	25°C	110		pF



5.12 ±5 V Dual Supply: Electrical Characteristics

 V_{DD} = +5 V ± 10%, V_{SS} = -5 V ±10%, GND = 0 V (unless otherwise noted) Typical at V_{DD} = +5 V, V_{SS} = -5 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
ANALOG	SWITCH						
		V _{DD} = +4.5 V, V _{SS} = -4.5 V	25°C		4	7.2	Ω
R _{ON}	On-resistance	$V_S = -4.5 \text{ V to } +4.5 \text{ V}$	-40°C to +85°C			8.6	Ω
		$I_D = -10 \text{ mA}$	-40°C to +125°C			10	Ω
			25°C		0.1	0.3	Ω
ΔR_{ON}	On-resistance mismatch between channels	$V_S = -4.5 \text{ V to } +4.5 \text{ V}$ $I_D = -10 \text{ mA}$	-40°C to +85°C			0.35	Ω
			-40°C to +125°C			0.4	Ω
			25°C		1.3	2.2	Ω
R _{ON FLAT}	On-resistance flatness	$V_S = -4.5 \text{ V to } +4.5 \text{ V}$ $I_D = -10 \text{ mA}$	-40°C to +85°C			2.5	Ω
			-40°C to +125°C			2.8	Ω
R _{ON DRIFT}	On-resistance drift	V _S = 0 V, I _S = -10 mA	-40°C to +125°C		0.019		Ω/°C
		V _{DD} = +5.5 V, V _{SS} = -5.5 V	25°C	-0.25	0.05	0.25	nA
I _{S(OFF)}	Source off leakage current ⁽¹⁾	Switch state is off $V_S = +4.5 \text{ V} / -4.5 \text{ V}$	-40°C to +85°C	-1		1	nA
, ,		$V_D = -4.5 \text{ V} / + 4.5 \text{ V}$	-40°C to +125°C	-12		12	nA
	Drain off leakage current ⁽¹⁾	V_{DD} = +5.5 V, V_{SS} = -5.5 V Switch state is off V_{S} = +4.5 V / -4.5 V	25°C	-0.25	0.05	0.25	nA
I _{D(OFF)}			-40°C to +85°C	-1		1	nA
, ,		$V_{D} = -4.5 \text{ V} / + 4.5 \text{ V}$	-40°C to +125°C	-12		12	nA
		V _{DD} = +5.5 V, V _{SS} = -5.5 V	25°C	-0.25	0.05	0.25	nA
I _{S(ON)}	Channel on leakage current ⁽²⁾	Switch state is on	-40°C to +85°C	-1		1	nA
I _{D(ON)}		$V_S = V_D = \pm 4.5 \text{ V}$	-40°C to +125°C	-12		12	nA
LOGIC IN	PUTS (SEL / EN pins)						
V _{IH}	Logic voltage high		-40°C to +125°C	1.3		36	V
V _{IL}	Logic voltage low		-40°C to +125°C	0		0.8	V
I _{IH}	Input leakage current		-40°C to +125°C		0.5	2	μA
I _{IL}	Input leakage current		-40°C to +125°C	-0.1	-0.005		μA
C _{IN}	Logic input capacitance		-40°C to +125°C		3.5		pF
POWER S	SUPPLY						
			25°C		28	40	μA
I _{DD}	V _{DD} supply current	V_{DD} = +5.5 V, V_{SS} = -5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	-40°C to +85°C			50	μA
		Logic inputs – 0 v, 5 v, or vDD	-40°C to +125°C			60	μA
			25°C		5	10	μA
I _{SS}	V _{SS} supply current	V_{DD} = +5.5 V, V_{SS} = -5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	-40°C to +85°C			12	μA
		Logic inputs – 0 v, 5 v, or v _{DD}	-40°C to +125°C			21	μA

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When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive. When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.



5.13 ±5 V Dual Supply: Switching Characteristics

 V_{DD} = +5 V ± 10%, V_{SS} = -5 V ±10%, GND = 0 V (unless otherwise noted) Typical at V_{DD} = +5 V, V_{SS} = -5 V, T_A = 25°C (unless otherwise noted)

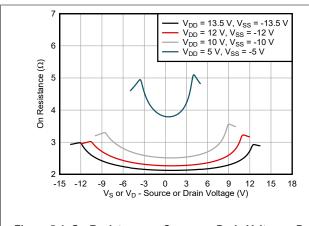
PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
			25°C		220	300	ns
t _{ON}	Turn-on time from control input	$V_S = 3 V$ $R_1 = 300 \Omega, C_1 = 35 pF$	–40°C to +85°C			350	ns
		11, 000 12, 01 00 pi	–40°C to +125°C			380	ns
			25°C		210	280	ns
t _{OFF}	Turn-off time from control input	$V_S = 3 V$ $R_1 = 300 \Omega, C_1 = 35 pF$	–40°C to +85°C			330	ns
		1.1 000 11, 0[00 p.	–40°C to +125°C			350	ns
			25°C		0.19		ms
t _{ON (VDD)}	Device turn on time (V _{DD} to output)	V_{DD} rise time = 1 μs R_1 = 300 Ω , C_1 = 35 pF	–40°C to +85°C		0.19		ms
	(VDD to suspat)	11, 000 12, 01 00 pi	–40°C to +125°C		0.19		ms
t _{PD}	Propagation delay	$R_L = 50 \Omega$, $C_L = 5 pF$	25°C		500		ps
Q _{INJ}	Charge injection	V _S = 0 V, C _L = 100 pF	25°C		– 5		рС
O _{ISO}	Off-isolation	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 0 V$, $f = 100 kHz$	25°C		-70		dB
O _{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		-50		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 0 V$, $f = 100 kHz$	25°C		–117		dB
X _{TALK}	Crosstalk	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 0 V$, $f = 1 MHz$	25°C		-94		dB
BW	–3dB Bandwidth	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 0 V$	25°C		67		MHz
IL	Insertion loss	$R_L = 50 \Omega$, $C_L = 5 pF$ $V_S = 0 V$, $f = 1 MHz$	25°C	-	-0.35		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C	-76			dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 5 \text{ V}, V_{BIAS} = 0 \text{ V}$ $R_L = 10 \text{ k}\Omega$, $C_L = 5 \text{ pF}$, f = 20 Hz to 20 kHz	25°C	C	0.001		%
C _{S(OFF)}	Source off capacitance	V _S = 0 V, f = 1 MHz	25°C		30		pF
C _{D(OFF)}	Drain off capacitance	V _S = 0 V, f = 1 MHz	25°C		40		pF
C _{S(ON),} C _{D(ON)}	On capacitance	V _S = 0 V, f = 1 MHz	25°C		120		pF



V_{DD} = 18 V, V_{SS} = -18 V V_{DD} = 15 V, V_{SS} = -15 V

5.14 Typical Characteristics

at $T_A = 25$ °C

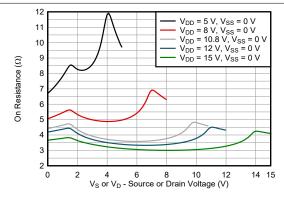


C) 3.5 20 1.5 -18 -14 -10 -6 -2 2 6 10 14 18 V_S or V_D - Source or Drain Voltage (V)

4.5

Figure 5-1. On-Resistance vs Source or Drain Voltage – Dual Supply

Figure 5-2. On-Resistance vs Source or Drain Voltage – Dual Supply



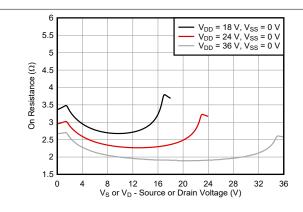
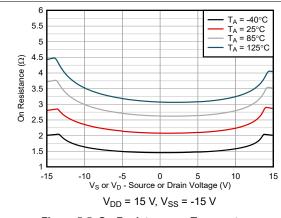


Figure 5-3. On-Resistance vs Source or Drain Voltage – Single Supply





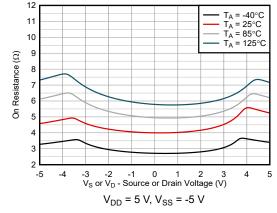
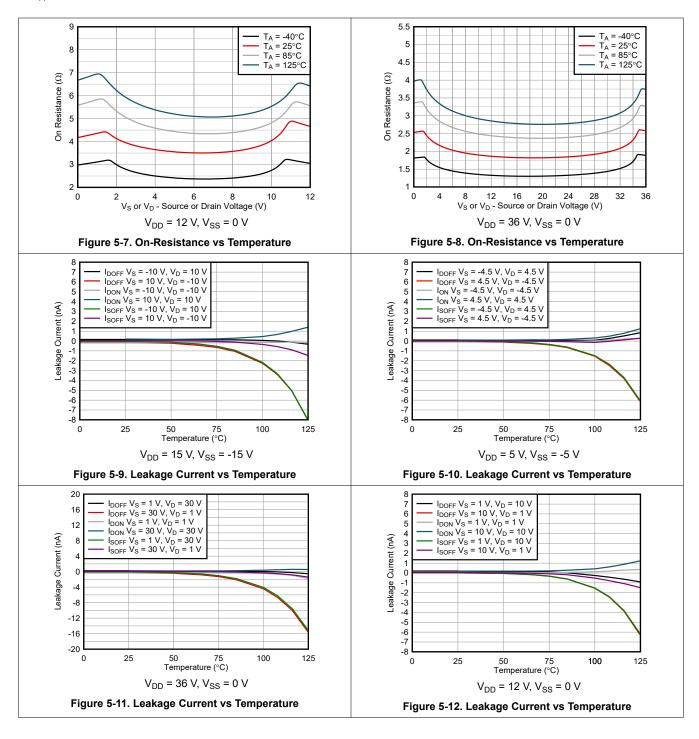


Figure 5-5. On-Resistance vs Temperature Figure 5-6. On-Resistance vs Temperature

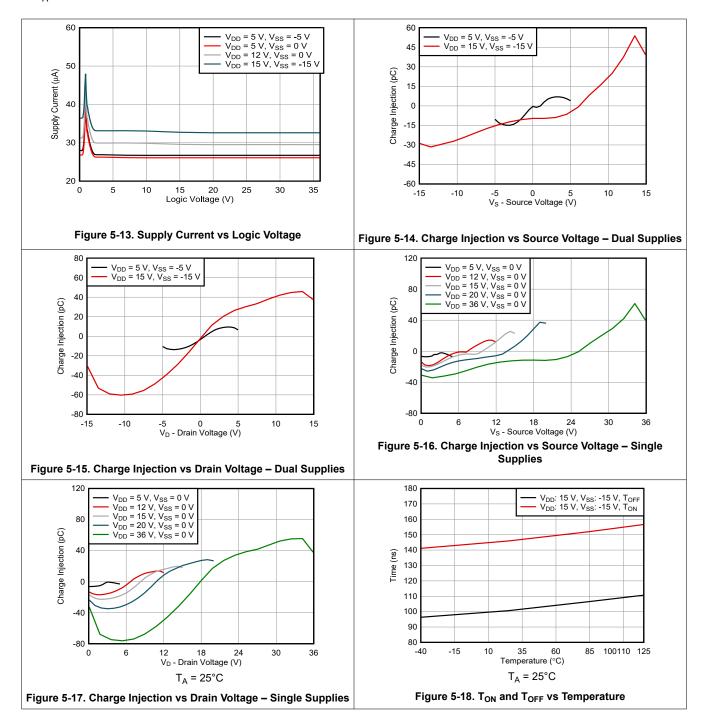


at $T_A = 25$ °C



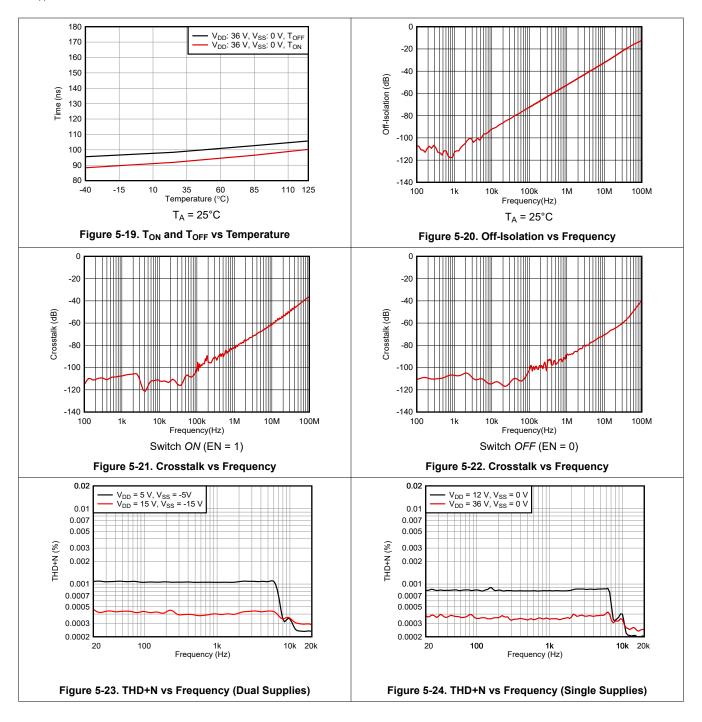


at $T_A = 25$ °C



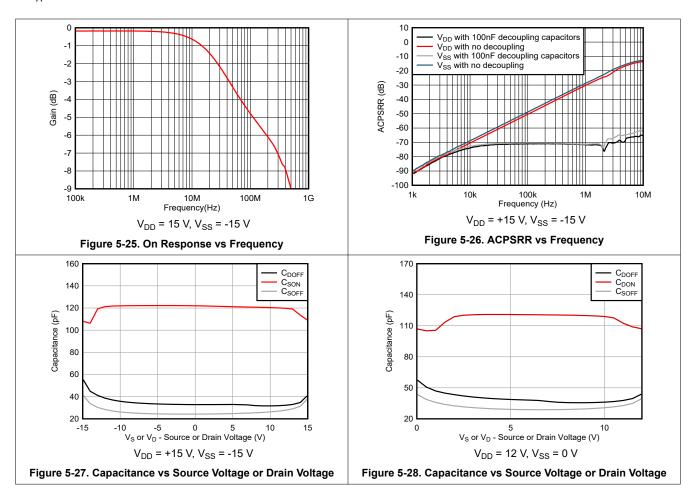


at $T_A = 25$ °C





at T_A = 25°C





6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 6-1 shows the measurement setup used to measure R_{ON} . Voltage (V) and current (I_{SD}) are measured using the following setup, where R_{ON} is computed as $R_{ON} = V / I_{SD}$.

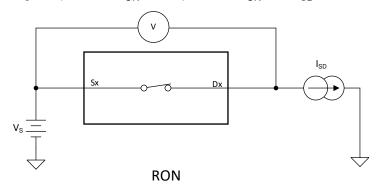


Figure 6-1. On-Resistance

6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

- 1. Source off-leakage current.
- 2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 6-2 shows the setup used to measure both off-leakage currents.

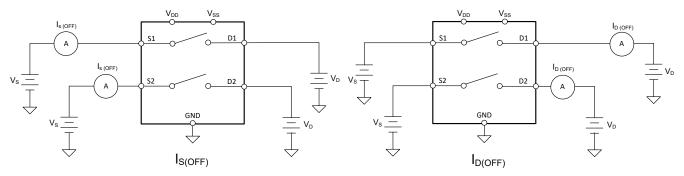


Figure 6-2. Off-Leakage Measurement Setup



6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

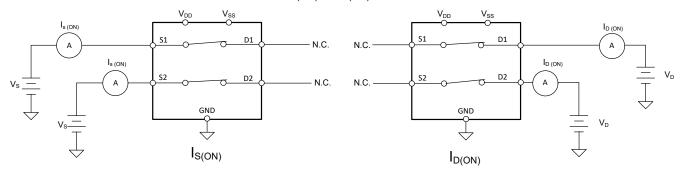


Figure 6-3. On-Leakage Measurement Setup

6.4 t_{ON(EN)} and t_{OFF(EN)}

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(FN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure turn-off time, denoted by the symbol t_{OFF(EN)}.

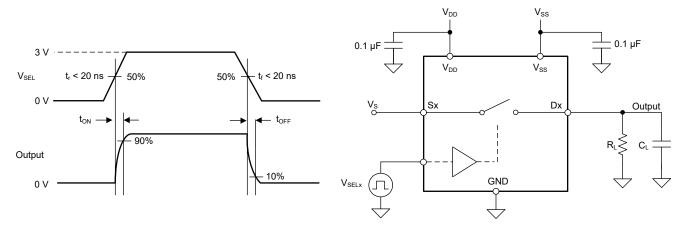


Figure 6-4. Turn-On and Turn-Off Time Measurement Setup

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6.5 t_{ON (VDD)} Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 6-5 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

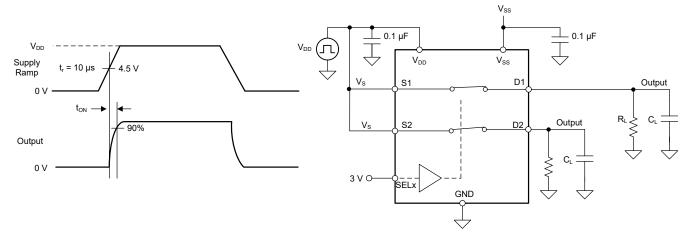


Figure 6-5. t_{ON (VDD)} Time Measurement Setup

6.6 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-6 and Equation 1 shows the setup used to measure propagation delay, denoted by the symbol t_{PD} .

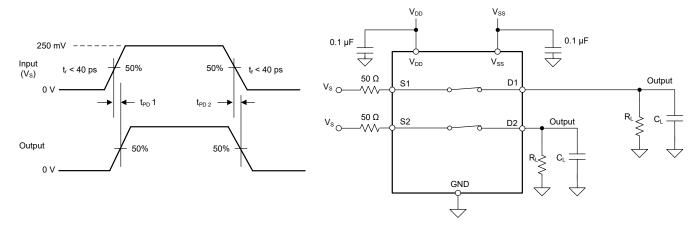


Figure 6-6. Propagation Delay Measurement Setup

$$t_{Prop\ Delay} = max\left(t_{PD}\ 1,\ t_{PD}\ 2\right) \tag{1}$$

6.7 Charge Injection

The TMUX622x has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 6-7 shows the setup used to measure charge injection from source (Sx) to drain (D).

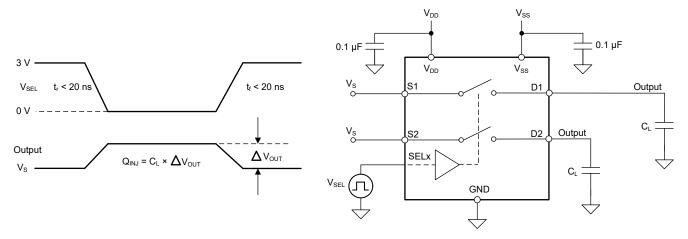


Figure 6-7. Charge-Injection Measurement Setup

6.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0 , for the measurement is 50 Ω . Figure 6-8 and Equation 2 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

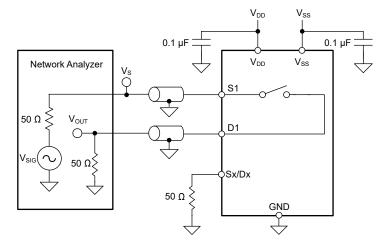


Figure 6-8. Off Isolation Measurement Setup

$$Off \ Isolation = 20 \times LOG \ \frac{V_{OUT}}{V_S}$$
 (2)

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6.9 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 6-9 shows the setup used to measure, and Equation 3 shows the equation used to calculate crosstalk.

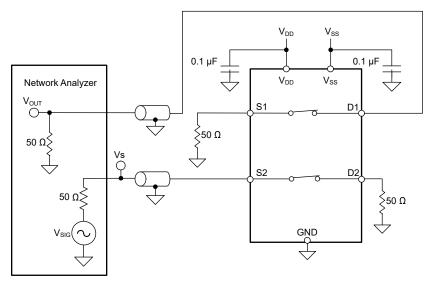


Figure 6-9. Crosstalk Measurement Setup

$$Crosstalk = 20 \times LOG \frac{V_{OUT}}{V_S}$$
 (3)

6.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0 , for the measurement is 50 Ω . Figure 6-10 and Equation 4 shows the setup used to measure bandwidth.

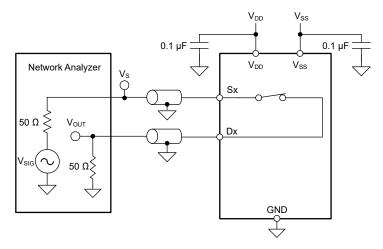


Figure 6-10. Bandwidth Measurement Setup

$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$
 (4)

6.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

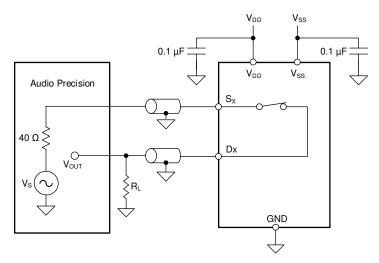


Figure 6-11. THD + N Measurement Setup

6.12 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100 mV_{PP} . The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.

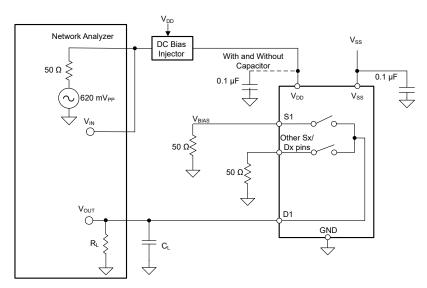


Figure 6-12. AC PSRR Measurement Setup

$$PSRR = 20 \times Log \frac{V_{OUT}}{V_{IN}} \tag{5}$$

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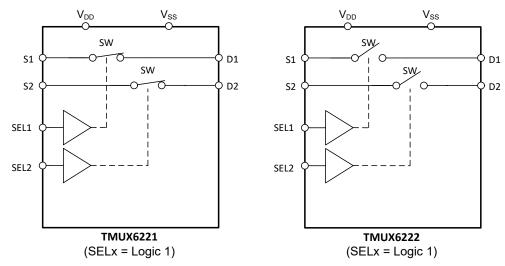
7 Detailed Description

7.1 Overview

The TMUX622x is a 1:1, 2-channel switch. Each input is turned on or turned off based on the state of the select line and enable pin.

7.2 Functional Block Diagram

The following figure shows the functional block diagram of the TMUX622x.



7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX622x conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX622x ranges from V_{SS} to V_{DD} .

7.3.3 1.8 V Logic Compatible Inputs

The TMUX622x has 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the device to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to Simplifying Design with 1.8 V logic Muxes and Switches.

7.3.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX622x have internal weak pull-down resistors to GND so that the logic pins are not left floating. The value of this pull-down resistor is approximately 4 M Ω , but is clamped to about 1 μ A at higher voltages. This feature integrates up to four external components and reduces system size and cost.

7.3.5 Fail-Safe Logic

The TMUX622x supports Fail-Safe Logic on the control input pins (EN and SEL) allowing for operation up to 36 V above ground, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pins of the TMUX622x to be ramped to +36 V while V_{DD} and V_{SS} = 0 V. The logic control inputs are protected against positive faults of up to +36 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

7.3.6 Latch-Up Immune

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX622x family of devices are constructed on silicon-on-insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX622x family of switches and multiplexers to be used in harsh environments.

7.3.7 Ultra-Low Charge Injection

The TMUX622x has a transmission gate topology, as shown in Figure 7-1. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

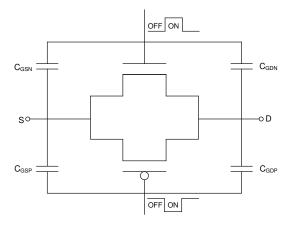


Figure 7-1. Transmission Gate Topology

The TMUX622x contains specialized architecture to reduce charge injection on the Drain (Dx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the Source (Sx). Doing this will push excess charge from the switch transition into the compensation capacitor on the Source (Sx) instead of the Drain (Dx). As a general rule, Cp should be 20x larger than the equivalent load capacitance on the Drain (Dx). Figure 7-2 shows charge injection variation with different compensation capacitors on the Source side. This plot was captured on the TMUX6219 as part of the TMUX62xx family with a 100 pF load capacitance.

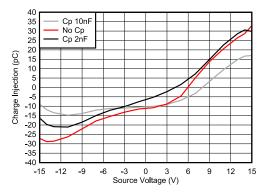


Figure 7-2. Charge Injection Compensation

Product Folder Links: TMUX6221 TMUX6222



7.4 Device Functional Modes

The TMUX622x devices have two independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins can be as high as 36 V.

The TMUX622x devices can be operated without any external components except for the supply decoupling capacitors. The SEL pins has internal pull-down resistor of 4 M Ω . If unused, tie the SEL pins to GND so that the device does not consume additional current. For more information, see *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (S1, S2, D1, or D2) should be connected to GND.

7.5 Truth Tables

Table 7-1 provides the truth tables for the TMUX622x.

Table 7-1. TMUX6221 Truth Table

SEL x	CHANNEL x
0	Channel x OFF
1	Channel x ON

Table 7-2. TMUX6222 Truth Table

SEL x	CHANNEL x
0	Channel x ON
1	Channel x OFF

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

TMUX622x is part of the precision switches and multiplexers family of devices. TMUX622x offers low RON, low on and off leakage currents and ultra-low charge injection performance. These properties make TMUX622x ideal for implementing high precision industrial systems requiring selection of one of two inputs or outputs.

8.2 Typical Applications

8.2.1 Switched Gain Amplifier - Discrete PGA

Switches and multiplexers are commonly used in the feedback path of the amplifier circuits to provide configurable gain control. By using various resistor values on each switch path, the TMUX622x allows the system to have multiple gain settings. An external resistor causes the amplifier to not operate in an open loop configuration and gives up to 4 gain settings. The leakage current, on-resistance, and charge injection performance of the TMUX622x are key specifications to evaluate when selecting a device for gain control.

Figure 8-1 shows the TMUX622x configured to select the gain of an op-amp, creating a discrete PGA.

For more information on how to use TI's analog switches in Discrete Programmable Gain Amplifier (PGA) such as the impact of On-Capacitance, see *Choosing the Right Multiplexer for a Discrete Programmable Gain Amplifier (PGA)*

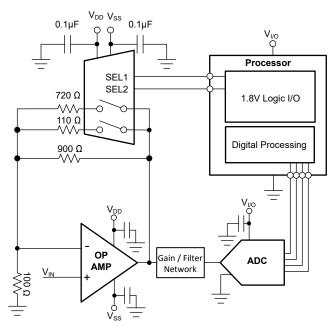


Figure 8-1. Gain Switching

Product Folder Links: TMUX6221 TMUX6222



8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETERS	VALUES		
Supply (V _{DD})	15 V		
Supply (V _{SS})	-15 V		
Input or output signal range	-15 V to 15 V (Rail-to-Rail)		
Control logic thresholds	1.8 V compatible		

8.2.1.2 Detailed Design Procedure

The TMUX622x device can operate without any external components except for the supply decoupling capacitors. All inputs signals passing through the switch must fall within the recommend operating conditions of the TMUX622x including signal range and continuous current. For this design example, with a supply of +15 V and -15 V, the signals can range from +15 V to -15 V when the device is powered.

The application shown in *Switching Gain Settings* demonstrates how to use the TMUX622x to control the feedback gain of a precision op-amp. This feedback design can very sensitive to induced voltage and current offsets. The TMUX622x has a typical on-leakage current of 100 pA which would lead to an accuracy well within 1% of a full scale 1 µA signal, thus minimizing errors from current offsets. The low on-resistance of the TMUX622x leads to a low error in the feedback resistance and resulting gain. This additionally minimizes any voltage offsets.

Table 8-2. Programmable Gain and Error

SEL1	SEL2	Gain	Gain Error
0	0	10x	0%
1	0	5x	0.13%
0	1	2x	0.16%

8.2.1.3 Application Curves

The TMUX622x is capable of switching signals with minimal distortion because of the ultra-low leakage currents and excellent on-resistance flatness. Figure 8-2 shows how the on-resistance for the TMUX622x varies with different supply voltages.

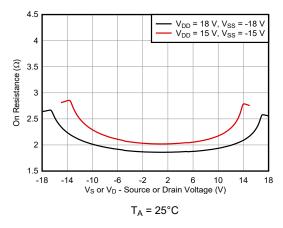


Figure 8-2. On-Resistance vs Source or Drain Voltage



8.3 Power Supply Recommendations

The TMUX622x operates across a wide supply range of ±4.5 V to ±18 V (4.5 V to 36 V in single-supply mode). The device also performs well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = -5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

8.4 Layout

8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

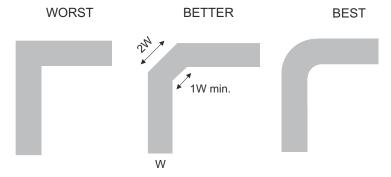


Figure 8-3. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD/VSS and GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

Product Folder Links: TMUX6221 TMUX6222



8.4.2 Layout Example

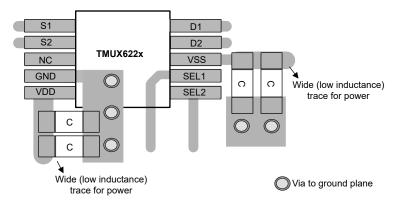


Figure 8-4. TMUX622x Layout Example



9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, Improve Stability Issues with Low CON Multiplexers.
- Texas Instruments, Improving Signal Measurement Accuracy in Automated Test Equipment.
- Texas Instruments, Multiplexers and Signal Switches Glossary.
- Texas Instruments, QFN/SON PCB Attachment.
- Texas Instruments, Quad Flat pack No-Lead Logic Packages.
- Texas Instruments, Simplifying Design with 1.8 V logic Muxes and Switches.
- Texas Instruments, System-Level Protection for High-Voltage Analog Multiplexers.
- Texas Instruments, True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2023) to Revision B (May 2024)

Page

Updated the Pin Configuration section to accurately reflect the correct pin number for SEL1 and SEL2........3

Changes from Revision * (March 2023) to Revision A (September 2023)

Page

Product Folder Links: TMUX6221 TMUX6222



11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
TMUX6221DGSR	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TM221
TMUX6221DGSR.B	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TM221
TMUX6222DGSR	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TM222
TMUX6222DGSR.B	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TM222

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX6221DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMUX6222DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX6221DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TMUX6222DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

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