

# TMUX1119 5-V, Low-Leakage-Current, 2:1 Precision Switch

## 1 Features

- Wide supply range: 1.08V to 5.5V
- Low leakage current: 3pA
- Low on-resistance: 1.8Ω
- Low charge injection: –6pC
- –40°C to +125°C operating temperature
- [1.8V logic compatible](#)
- [Fail-safe logic](#)
- [Rail to rail operation](#)
- [Bidirectional signal path](#)
- Break-before-make switching
- ESD protection HBM: 2000V

## 2 Applications

- [Ultrasound scanners](#)
- [Patient monitoring and diagnostics](#)
- [Blood glucose monitors](#)
- [Optical module](#)
- [Optical transport](#)
- [Remote radio units](#)
- [Data acquisition systems](#)
- [Semiconductor test equipment](#)
- [Factory automation and industrial controls](#)
- [Flow transmitters](#)
- [Programmable logic controllers \(PLC\)](#)
- [Analog input modules](#)
- [Battery test](#)

## 3 Description

The TMUX1119 is a complementary metal-oxide semiconductor (CMOS) single-pole double-throw (2:1) switch. Wide operating supply of 1.08V to 5.5V allows for use in a broad array of applications from medical equipment to industrial systems. The device supports bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from GND to  $V_{DD}$ . All logic inputs have [1.8V logic compatible](#) thresholds, allowing for both TTL and CMOS logic compatibility when operating in the valid supply voltage range. [Fail-Safe Logic](#) circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

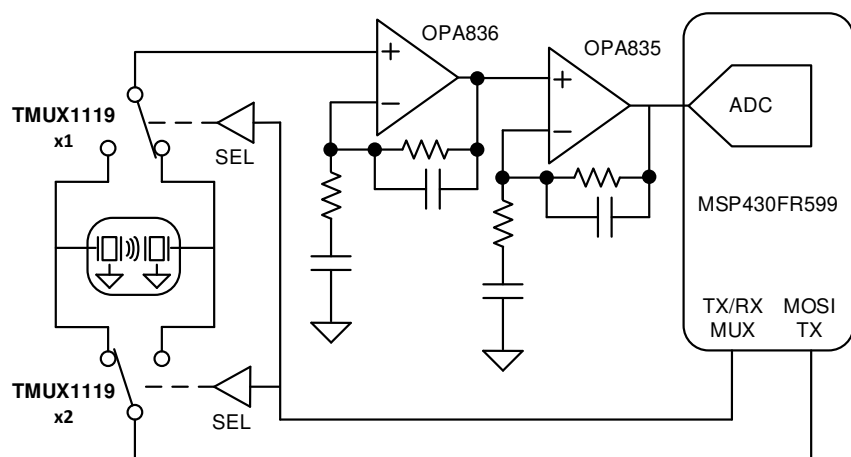
The TMUX1119 is part of the precision switches and multiplexers family of devices. These devices have very low on and off leakage currents and low charge injection, allowing them to be used in high precision measurement applications. A low supply current of 3nA and small package options enable use in portable applications.

### Package Information

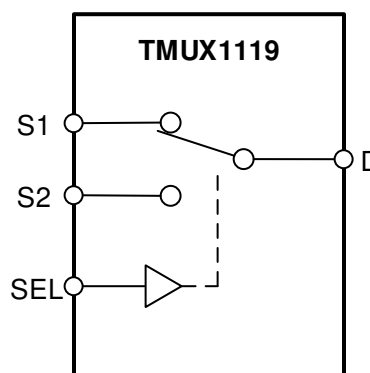
PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TMUX1119	DCK (SC70, 6)	2mm × 2.1mm
	DBV (SOT-23, 6)	2.9mm × 2.8mm

(1) For more information, see [Section 11](#)

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Example



Block Diagram



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## 4 Pin Configuration and Functions

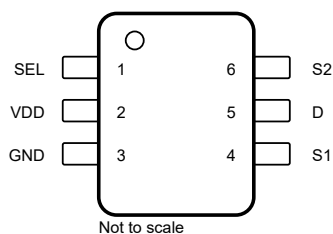


Figure 4-1. DCK Package, 6-Pin SC70 (Top View)

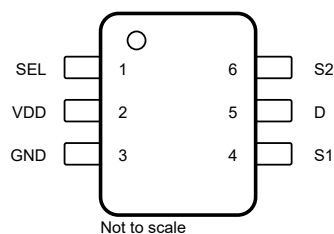


Figure 4-2. DBV Package, 6-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
SEL	1	I	Select pin: controls state of the switch according to Table 7-1. (Logic Low = S1 to D, Logic High = S2 to D)
VDD	2	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between $V_{DD}$ and GND.
GND	3	P	Ground (0V) reference
S1	4	I/O	Source pin 1. Can be an input or output.
D	5	I/O	Drain pin. Can be an input or output.
S2	6	I/O	Source pin 2. Can be an input or output.

(1) I = input, O = output, I/O = input and output, P = power

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage	−0.5	6	V
V <sub>SEL</sub> or V <sub>EN</sub>	Logic control input pin voltage (SEL)	−0.5	6	V
I <sub>SEL</sub> or I <sub>EN</sub>	Logic control input pin current (SEL)	−30	30	mA
V <sub>S</sub> or V <sub>D</sub>	Source or drain voltage (Sx, D)	−0.5	V <sub>DD</sub> +0.5	V
I <sub>S</sub> or I <sub>D</sub> (CONT)	Source or drain continuous current (Sx, D)	I <sub>DC</sub> ± 10 % <sup>(3)</sup>	I <sub>DC</sub> ± 10 % <sup>(3)</sup>	mA
I <sub>S</sub> or I <sub>D</sub> (PEAK)	Source and drain peak current: (1 ms period maximum, 10% duty cycle maximum) (Sx, D)	I <sub>peak</sub> ± 10 % <sup>(3)</sup>	I <sub>peak</sub> ± 10 % <sup>(3)</sup>	mA
T <sub>stg</sub>	Storage temperature	−65	150	°C
P <sub>tot</sub>	Total power dissipation <sup>(4) (5)</sup>		300	mW
T <sub>J</sub>	Junction temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) Refer to Recommended Operating Conditions for I<sub>DC</sub> and I<sub>peak</sub> ratings
- (4) For DCK(SC70) package: P<sub>tot</sub> derates linearly above TA=77°C by 4.11mW/°C
- (5) For DGS(SOT-23) package: P<sub>tot</sub> derates linearly above TA=86°C by 4.71mW/°C

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±750

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage	1.08		5.5	V
V <sub>S</sub> or V <sub>D</sub>	Signal path input/output voltage (source or drain pin) (Sx, D)	0		V <sub>DD</sub>	V
V <sub>SEL</sub>	Logic control input pin voltage (SEL)	0		5.5	V
T <sub>A</sub>	Ambient temperature	−40		125	°C
I <sub>DC</sub>	Continuous current through switch	T <sub>J</sub> = 25°C	150		
		T <sub>J</sub> = 85°C	120		mA
		T <sub>J</sub> = 125°C	60		mA
		T <sub>J</sub> = 130°C	50		mA
I <sub>peak</sub>	Peak current through switch(1 ms period maximum, 10% duty cycle maximum)	T <sub>J</sub> = 25°C	300		mA
		T <sub>J</sub> = 85°C	300		mA
		T <sub>J</sub> = 125°C	180		mA
		T <sub>J</sub> = 130°C	160		mA

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TMUX1119		UNIT
		DCK (SC70)	DBV (SOT-23)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	243.1	212.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	206.0	156.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	128.3	96.5	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	107.8	80.7	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	128.0	96.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics ( $V_{DD} = 5V \pm 10\%$ )

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5V$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R <sub>ON</sub>	On-resistance	V <sub>S</sub> = 0V to V <sub>DD</sub> I <sub>SD</sub> = 10mA Refer to <a href="#">Section 6.1</a>	25°C		1.8	4	Ω
			–40°C to +85°C			4.5	Ω
			–40°C to +125°C			4.9	Ω
ΔR <sub>ON</sub>	On-resistance matching between channels	V <sub>S</sub> = 0V to V <sub>DD</sub> I <sub>SD</sub> = 10mA Refer to <a href="#">Section 6.1</a>	25°C		0.13		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
R <sub>ON</sub> FLAT	On-resistance flatness	V <sub>S</sub> = 0V to V <sub>DD</sub> I <sub>SD</sub> = 10mA Refer to <a href="#">Section 6.1</a>	25°C		0.85		Ω
			–40°C to +85°C			1.4	Ω
			–40°C to +125°C			1.6	Ω
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 5V Switch Off V <sub>D</sub> = 4.5V / 1.5V V <sub>S</sub> = 1.5V / 4.5V Refer to <a href="#">Section 6.2</a>	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA
I <sub>D(ON)</sub> I <sub>S(ON)</sub>	Channel on leakage current	V <sub>DD</sub> = 5V Switch On V <sub>D</sub> = V <sub>S</sub> = 2.5V Refer to <a href="#">Section 6.3</a>	25°C	–0.025	±0.003	0.025	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.95		0.95	nA
I <sub>D(ON)</sub> I <sub>S(ON)</sub>	Channel on leakage current	V <sub>DD</sub> = 5V Switch On V <sub>D</sub> = V <sub>S</sub> = 4.5V / 1.5V Refer to <a href="#">Section 6.3</a>	25°C	–0.1	±0.01	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SEL)							
V <sub>IH</sub>	Input logic high		–40°C to +125°C	1.49		5.5	V
V <sub>IL</sub>	Input logic low		–40°C to +125°C	0		0.87	V
I <sub>IH</sub> I <sub>IL</sub>	Input leakage current		25°C		±0.005		μA
I <sub>IH</sub> I <sub>IL</sub>	Input leakage current		–40°C to +125°C			±0.05	μA
C <sub>IN</sub>	Logic input capacitance		25°C		1		pF
C <sub>IN</sub>	Logic input capacitance		–40°C to +125°C			2	pF

## 5.5 Electrical Characteristics ( $V_{DD} = 5V \pm 10\%$ ) (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5V$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
POWER SUPPLY							
I <sub>DD</sub>	V <sub>DD</sub> supply current	Logic inputs = 0V or 5.5V	25°C	0.003			μA
			−40°C to +125°C	1		μA	
DYNAMIC CHARACTERISTICS							
t <sub>TRAN</sub>	Switching time between channels	V <sub>S</sub> = 3V R <sub>L</sub> = 200Ω, C <sub>L</sub> = 15pF Refer to <a href="#">Section 6.4</a>	25°C	12			ns
			−40°C to +85°C	18		ns	
			−40°C to +125°C	19		ns	
t <sub>OPEN</sub> (BBM)	Break before make time	V <sub>S</sub> = 3V R <sub>L</sub> = 200Ω, C <sub>L</sub> = 15pF Refer to <a href="#">Section 6.5</a>	25°C	8			ns
			−40°C to +85°C	1		ns	
			−40°C to +125°C	1		ns	
Q <sub>C</sub>	Charge Injection	V <sub>D</sub> = 1V R <sub>S</sub> = 0Ω, C <sub>L</sub> = 1 nF Refer to <a href="#">Section 6.6</a>	25°C	−6			pC
O <sub>ISO</sub>	Off Isolation	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF f = 1MHz Refer to <a href="#">Section 6.7</a>	25°C	−65			dB
		R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF f = 10MHz Refer to <a href="#">Section 6.7</a>	25°C	−45			dB
X <sub>TALK</sub>	Crosstalk	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF f = 1MHz Refer to <a href="#">Section 6.8</a>	25°C	−65			dB
		R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF f = 10MHz Refer to <a href="#">Section 6.8</a>	25°C	−45			dB
BW	Bandwidth	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF Refer to <a href="#">Section 6.9</a>	25°C	250			MHz
C <sub>SOFF</sub>	Source off capacitance	f = 1MHz	25°C	6			pF
C <sub>SON</sub> C <sub>DON</sub>	On capacitance	f = 1MHz	25°C	20			pF

(1) When  $V_S$  is 4.5V,  $V_D$  is 1.5V, and vice versa.

## 5.6 Electrical Characteristics ( $V_{DD} = 3.3V \pm 10\%$ )

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3V$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = 0V$ to $V_{DD}$ $I_{SD} = 10\text{mA}$ Refer to <a href="#">Section 6.1</a>	25°C		3.7	8.8	Ω
			–40°C to +85°C			9.5	Ω
			–40°C to +125°C			9.8	Ω
$\Delta R_{ON}$	On-resistance matching between channels	$V_S = 0V$ to $V_{DD}$ $I_{SD} = 10\text{mA}$ Refer to <a href="#">Section 6.1</a>	25°C		0.13		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
$R_{ON}$ FLAT	On-resistance flatness	$V_S = 0V$ to $V_{DD}$ $I_{SD} = 10\text{mA}$ Refer to <a href="#">Section 6.1</a>	25°C		1.9		Ω
			–40°C to +85°C		2		Ω
			–40°C to +125°C		2.2		Ω

## 5.6 Electrical Characteristics ( $V_{DD} = 3.3V \pm 10\%$ ) (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3V$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 3.3V Switch Off V <sub>D</sub> = 3V / 1V V <sub>S</sub> = 1V / 3V Refer to <a href="#">Section 6.2</a>	25°C	−0.05	±0.001	0.05	nA
			−40°C to +85°C	−0.1		0.1	nA
			−40°C to +125°C	−0.5		0.5	nA
I <sub>D(ON)</sub> I <sub>S(ON)</sub>	Channel on leakage current	V <sub>DD</sub> = 3.3V Switch On V <sub>D</sub> = V <sub>S</sub> = 3V / 1V Refer to <a href="#">Section 6.3</a>	25°C	−0.1	±0.005	0.1	nA
			−40°C to +85°C	−0.35		0.35	nA
			−40°C to +125°C	−2		2	nA
LOGIC INPUTS (SEL)							
V <sub>IH</sub>	Input logic high		−40°C to +125°C	1.35		5.5	V
V <sub>IL</sub>	Input logic low		−40°C to +125°C	0		0.8	V
I <sub>IH</sub> I <sub>IL</sub>	Input leakage current		25°C		±0.005		μA
I <sub>IH</sub> I <sub>IL</sub>	Input leakage current		−40°C to 125°C			±0.05	μA
C <sub>IN</sub>	Logic input capacitance		25°C		1		pF
C <sub>IN</sub>	Logic input capacitance		−40°C to +125°C			2	pF
POWER SUPPLY							
I <sub>DD</sub>	V <sub>DD</sub> supply current	Logic inputs = 0V or 5.5V	25°C		0.003		μA
			−40°C to +125°C			0.8	μA
DYNAMIC CHARACTERISTICS							
t <sub>TRAN</sub>	Switching time between channels	V <sub>S</sub> = 2V R <sub>L</sub> = 200Ω, C <sub>L</sub> = 15pF Refer to <a href="#">Section 6.4</a>	25°C		14		ns
			−40°C to +85°C			20	ns
			−40°C to +125°C			21	ns
t <sub>OPEN</sub> (BBM)	Break before make time	V <sub>S</sub> = 2V R <sub>L</sub> = 200Ω, C <sub>L</sub> = 15pF Refer to <a href="#">Section 6.5</a>	25°C		9		ns
			−40°C to +85°C	1			ns
			−40°C to +125°C	1			ns
Q <sub>C</sub>	Charge Injection	V <sub>D</sub> = 1V R <sub>S</sub> = 0Ω, C <sub>L</sub> = 1 nF Refer to <a href="#">Section 6.6</a>	25°C		−6		pC
O <sub>ISO</sub>	Off Isolation	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF f = 1MHz Refer to <a href="#">Section 6.7</a>	25°C		−65		dB
		R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF f = 10MHz Refer to <a href="#">Section 6.7</a>	25°C		−45		dB
X <sub>TALK</sub>	Crosstalk	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF f = 1MHz Refer to <a href="#">Section 6.8</a>	25°C		−65		dB
		R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF f = 10MHz Refer to <a href="#">Section 6.8</a>	25°C		−45		dB
BW	Bandwidth	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF Refer to <a href="#">Section 6.9</a>	25°C		250		MHz
C <sub>SOFF</sub>	Source off capacitance	f = 1MHz	25°C		6		pF
C <sub>SON</sub> C <sub>DON</sub>	On capacitance	f = 1MHz	25°C		20		pF

(1) When  $V_S$  is 3V,  $V_D$  is 1V, and vice versa.

## 5.7 Electrical Characteristics ( $V_{DD} = 1.8V \pm 10\%$ )

At  $T_A = 25^\circ C$ ,  $V_{DD} = 1.8V$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT	
ANALOG SWITCH								
R <sub>ON</sub>	On-resistance	V <sub>S</sub> = 0V to V <sub>DD</sub> I <sub>SD</sub> = 10mA Refer to <a href="#">Section 6.1</a>	25°C	40			Ω	
			-40°C to +85°C			80	Ω	
			-40°C to +125°C			80	Ω	
ΔR <sub>ON</sub>	On-resistance matching between channels	V <sub>S</sub> = 0V to V <sub>DD</sub> I <sub>SD</sub> = 10mA Refer to <a href="#">Section 6.1</a>	25°C	0.4			Ω	
			-40°C to +85°C			1.5	Ω	
			-40°C to +125°C			1.5	Ω	
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 1.98V Switch Off V <sub>D</sub> = 1.62V / 1V V <sub>S</sub> = 1V / 1.62V Refer to <a href="#">Section 6.2</a>	25°C	-0.05	±0.003	0.05	nA	
			-40°C to +85°C			-0.1	0.1	nA
			-40°C to +125°C			-0.5	0.5	nA
I <sub>D(ON)</sub> I <sub>S(ON)</sub>	Channel on leakage current	V <sub>DD</sub> = 1.98V Switch On V <sub>D</sub> = V <sub>S</sub> = 1.62V / 1V Refer to <a href="#">Section 6.3</a>	25°C	-0.1	±0.005	0.1	nA	
			-40°C to +85°C			-0.5	0.5	nA
			-40°C to +125°C			-2	2	nA
LOGIC INPUTS (SEL)								
V <sub>IH</sub>	Input logic high		-40°C to +125°C	1.07			5.5	V
V <sub>IL</sub>	Input logic low		-40°C to +125°C	0			0.68	V
I <sub>IH</sub> I <sub>IL</sub>	Input leakage current		25°C	±0.005				μA
I <sub>IH</sub> I <sub>IL</sub>	Input leakage current		-40°C to +125°C				±0.05	μA
C <sub>IN</sub>	Logic input capacitance		25°C	1				pF
C <sub>IN</sub>	Logic input capacitance		-40°C to +125°C				2	pF
POWER SUPPLY								
I <sub>DD</sub>	V <sub>DD</sub> supply current	Logic inputs = 0V or 5.5V	25°C	0.001				μA
			-40°C to +125°C			0.85		μA
DYNAMIC CHARACTERISTICS								
t <sub>TRAN</sub>	Transition time between channels	V <sub>S</sub> = 1V R <sub>L</sub> = 200Ω, C <sub>L</sub> = 15pF Refer to <a href="#">Section 6.4</a>	25°C	28				ns
			-40°C to +85°C			44		ns
			-40°C to +125°C			44		ns
t <sub>OPEN</sub> (BBM)	Break before make time	V <sub>S</sub> = 1V R <sub>L</sub> = 200Ω, C <sub>L</sub> = 15pF Refer to <a href="#">Section 6.5</a>	25°C	16				ns
			-40°C to +85°C			1		ns
			-40°C to +125°C			1		ns
Q <sub>C</sub>	Charge Injection	V <sub>D</sub> = 1V R <sub>S</sub> = 0Ω, C <sub>L</sub> = 1 nF Refer to <a href="#">Section 6.6</a>	25°C	-3				pC
O <sub>ISO</sub>	Off Isolation	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF f = 1MHz Refer to <a href="#">Section 6.7</a>	25°C	-65				dB
		R <sub>L</sub> = 50Ω, C <sub>L</sub> = 5pF f = 10MHz Refer to <a href="#">Section 6.7</a>	25°C	-45				dB

## 5.7 Electrical Characteristics ( $V_{DD} = 1.8V \pm 10\%$ ) (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.8V$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
X <sub>TALK</sub>	Crosstalk	$R_L = 50\Omega$ , $C_L = 5\text{pF}$ $f = 1\text{MHz}$ Refer to <a href="#">Section 6.8</a>	25°C		–65		dB
		$R_L = 50\Omega$ , $C_L = 5\text{pF}$ $f = 10\text{MHz}$ Refer to <a href="#">Section 6.8</a>	25°C		–45		dB
BW	Bandwidth	$R_L = 50\Omega$ , $C_L = 5\text{pF}$	25°C		250		MHz
C <sub>SOFF</sub>	Source off capacitance	$f = 1\text{MHz}$	25°C		6		pF
C <sub>SON</sub> C <sub>DON</sub>	On capacitance	$f = 1\text{MHz}$	25°C		20		pF

(1) When  $V_S$  is 1.62V,  $V_D$  is 1V, and vice versa.

## 5.8 Electrical Characteristics ( $V_{DD} = 1.2V \pm 10\%$ )

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.2V$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R <sub>ON</sub>	On-resistance	V <sub>S</sub> = 0V to V <sub>DD</sub> I <sub>SD</sub> = 10mA Refer to <a href="#">Section 6.1</a>	25°C		70		Ω
			–40°C to +85°C			105	Ω
			–40°C to +125°C			105	Ω
ΔR <sub>ON</sub>	On-resistance matching between channels	V <sub>S</sub> = 0V to V <sub>DD</sub> I <sub>SD</sub> = 10mA Refer to <a href="#">Section 6.1</a>	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 1.32V Switch Off V <sub>D</sub> = 1V / 0.8V V <sub>S</sub> = 0.8V / 1V Refer to <a href="#">Section 6.2</a>	25°C	–0.05	±0.003	0.05	nA
			–40°C to +85°C	–0.1		0.1	nA
			–40°C to +125°C	–0.5		0.5	nA
I <sub>D(ON)</sub> I <sub>S(ON)</sub>	Channel on leakage current	V <sub>DD</sub> = 1.32V Switch On V <sub>D</sub> = V <sub>S</sub> = 1V / 0.8V Refer to <a href="#">Section 6.3</a>	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SEL)							
V <sub>IH</sub>	Input logic high		–40°C to +125°C	0.96		5.5	V
V <sub>IL</sub>	Input logic low		–40°C to +125°C	0		0.36	V
I <sub>IH</sub> I <sub>IL</sub>	Input leakage current		25°C		±0.005		μA
I <sub>IH</sub> I <sub>IL</sub>	Input leakage current		–40°C to +125°C			±0.05	μA
C <sub>IN</sub>	Logic input capacitance		25°C		1		pF
C <sub>IN</sub>	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I <sub>DD</sub>	V <sub>DD</sub> supply current	Logic inputs = 0V or 5.5V	25°C		0.003		μA
			–40°C to +125°C			0.7	μA
DYNAMIC CHARACTERISTICS							
t <sub>TRAN</sub>	Transition time between channels	V <sub>S</sub> = 1V R <sub>L</sub> = 200Ω, C <sub>L</sub> = 15pF Refer to <a href="#">Section 6.4</a>	25°C		55		ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			190	ns



## 5.8 Electrical Characteristics ( $V_{DD} = 1.2V \pm 10\%$ ) (continued)

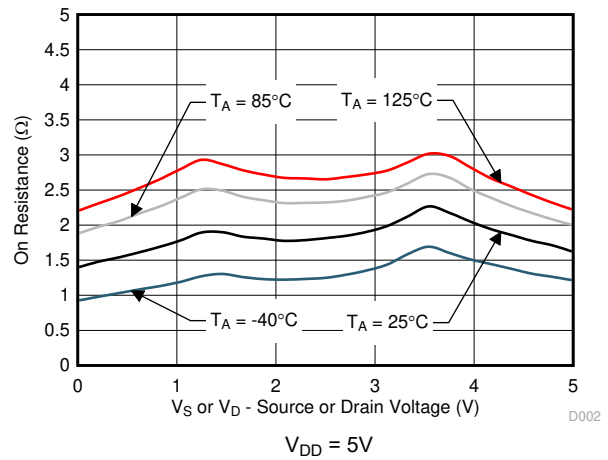
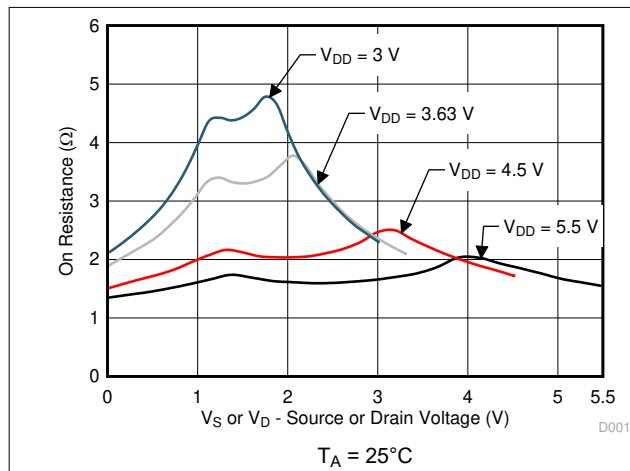
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.2V$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
$t_{\text{OPEN}}$ (BBM)	Break before make time	$V_S = 1V$ $R_L = 200\Omega$ , $C_L = 15\text{pF}$ Refer to <a href="#">Section 6.5</a>	$25^\circ\text{C}$		28		ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$	1			ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$	1			ns
$Q_C$	Charge Injection	$V_D = 1V$ $R_S = 0\Omega$ , $C_L = 1\text{nF}$ Refer to <a href="#">Section 6.6</a>	$25^\circ\text{C}$		-2		pC
$O_{\text{ISO}}$	Off Isolation	$R_L = 50\Omega$ , $C_L = 5\text{pF}$ $f = 1\text{MHz}$ Refer to <a href="#">Section 6.7</a>	$25^\circ\text{C}$		-65		dB
		$R_L = 50\Omega$ , $C_L = 5\text{pF}$ $f = 10\text{MHz}$ Refer to <a href="#">Section 6.7</a>	$25^\circ\text{C}$		-45		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\Omega$ , $C_L = 5\text{pF}$ $f = 1\text{MHz}$ Refer to <a href="#">Section 6.8</a>	$25^\circ\text{C}$		-65		dB
		$R_L = 50\Omega$ , $C_L = 5\text{pF}$ $f = 10\text{MHz}$ Refer to <a href="#">Section 6.8</a>	$25^\circ\text{C}$		-45		dB
BW	Bandwidth	$R_L = 50\Omega$ , $C_L = 5\text{pF}$	$25^\circ\text{C}$		250		MHz
$C_{\text{SOFF}}$	Source off capacitance	$f = 1\text{MHz}$	$25^\circ\text{C}$		6		pF
$C_{\text{SON}}$ $C_{\text{DON}}$	On capacitance	$f = 1\text{MHz}$	$25^\circ\text{C}$		20		pF

(1) When  $V_S$  is 1V,  $V_D$  is 0.8V, and vice versa.

### Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5V$  (unless otherwise noted)



## Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$  (unless otherwise noted)

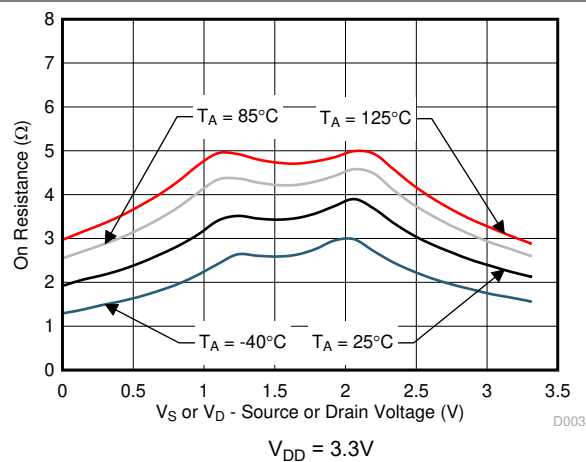


Figure 5-3. On-Resistance vs Temperature

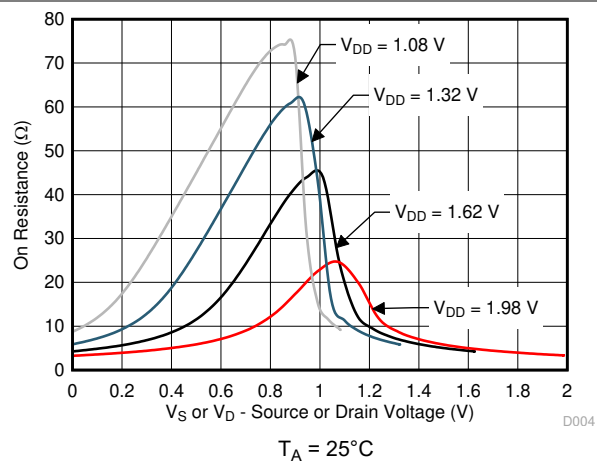


Figure 5-4. On-Resistance vs Source or Drain Voltage

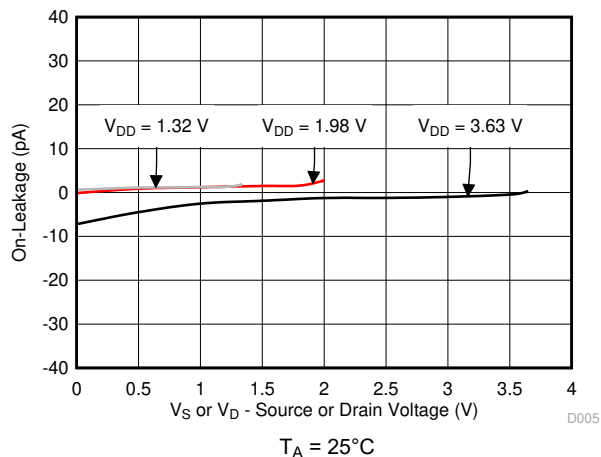


Figure 5-5. On-Leakage vs Source or Drain Voltage

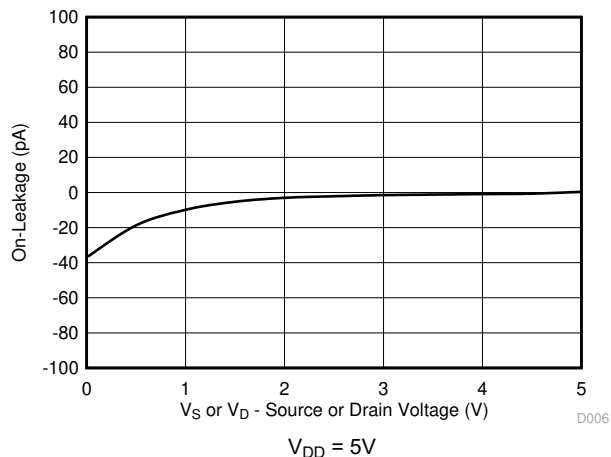


Figure 5-6. On-Leakage vs Source or Drain Voltage

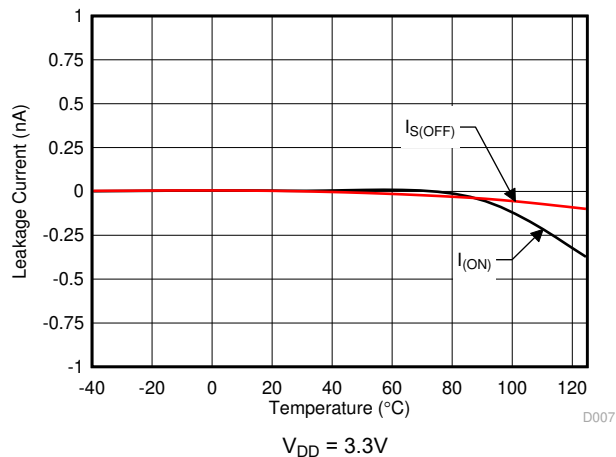


Figure 5-7. Leakage Current vs Temperature

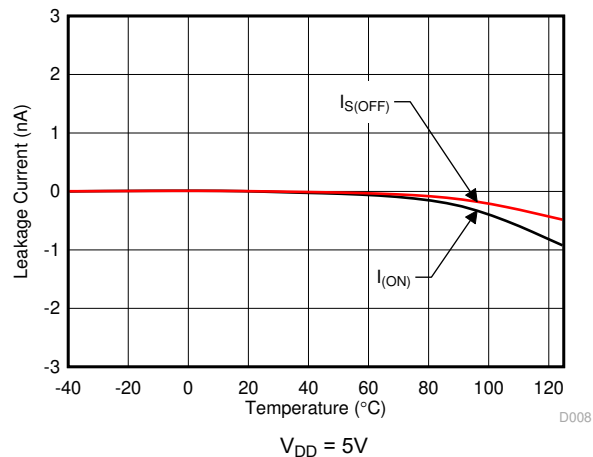


Figure 5-8. Leakage Current vs Temperature

## Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$  (unless otherwise noted)

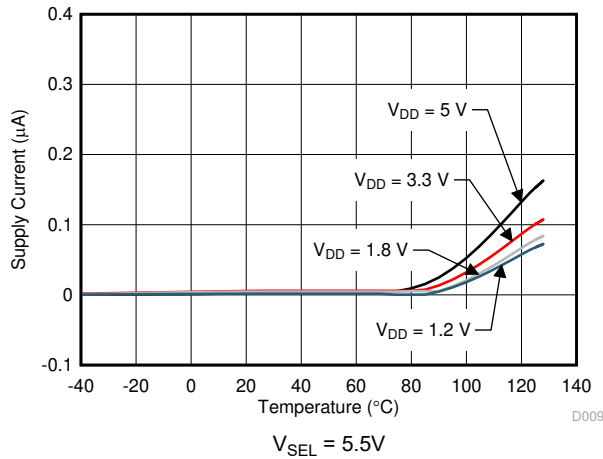


Figure 5-9. Supply Current vs Temperature

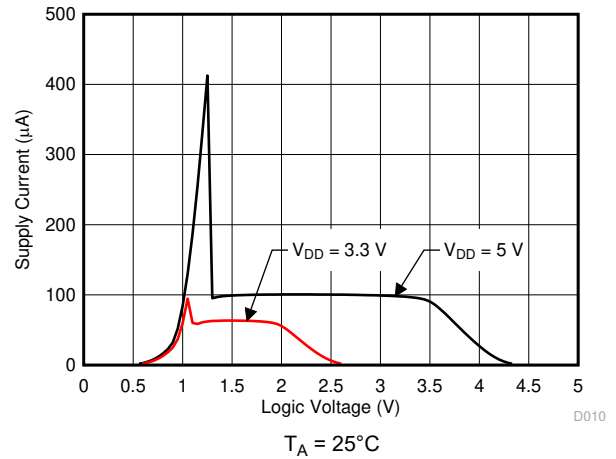


Figure 5-10. Supply Current vs Logic Voltage

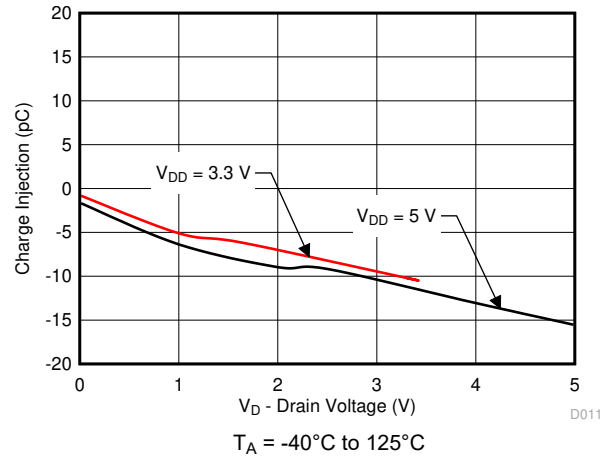


Figure 5-11. Charge Injection vs Drain Voltage

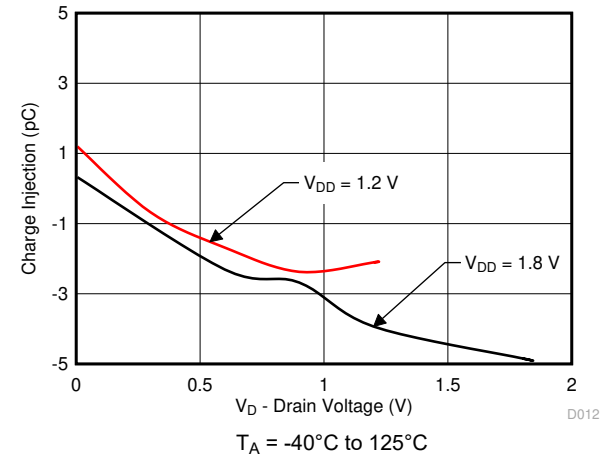


Figure 5-12. Charge Injection vs Drain Voltage

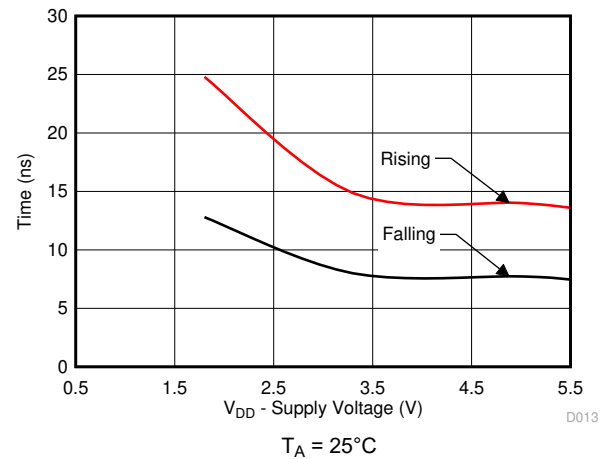


Figure 5-13. Output  $T_{\text{TRANSITION}}$  vs Supply Voltage

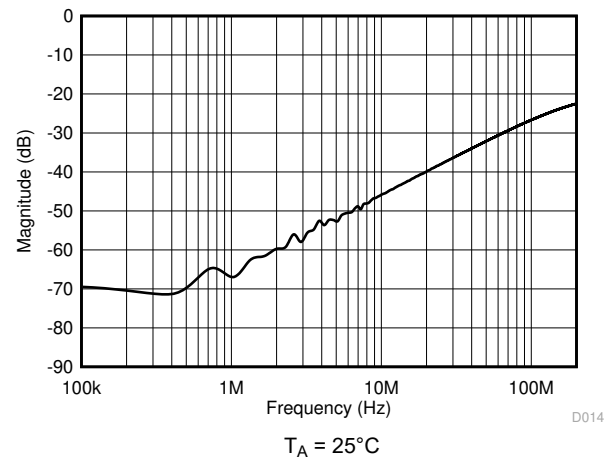


Figure 5-14. Xtalk and Off-Isolation vs Frequency

## Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$  (unless otherwise noted)

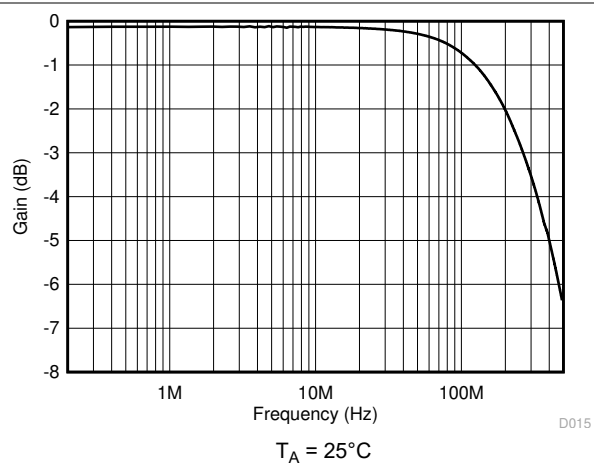


Figure 5-15. On Response vs Frequency

## 6 Parameter Measurement Information

### 6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol  $R_{ON}$  is used to denote on-resistance. The measurement setup used to measure  $R_{ON}$  is shown in Figure 6-1. Voltage (V) and current ( $I_{SD}$ ) are measured using this setup, and  $R_{ON}$  is computed with  $R_{ON} = V / I_{SD}$ :

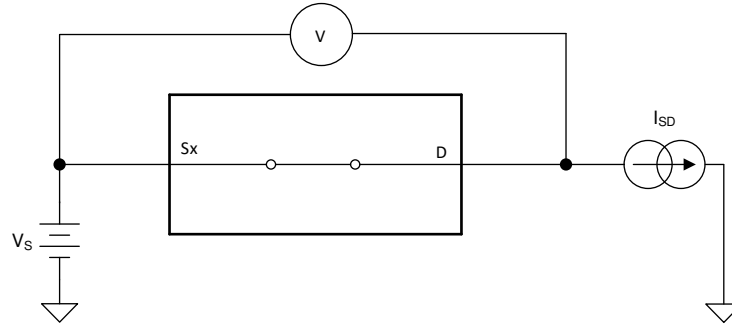


Figure 6-1. On-Resistance Measurement Setup

### 6.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol  $I_{S(OFF)}$ .

The setup used to measure off-leakage current is shown in Figure 6-2.

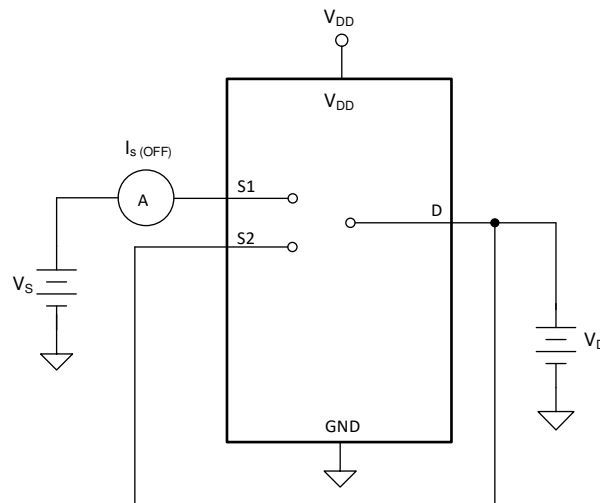


Figure 6-2. Off-Leakage Measurement Setup

### 6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol  $I_{S(ON)}$ .

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol  $I_{D(ON)}$ .

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by  $I_{S(ON)}$  or  $I_{D(ON)}$ .

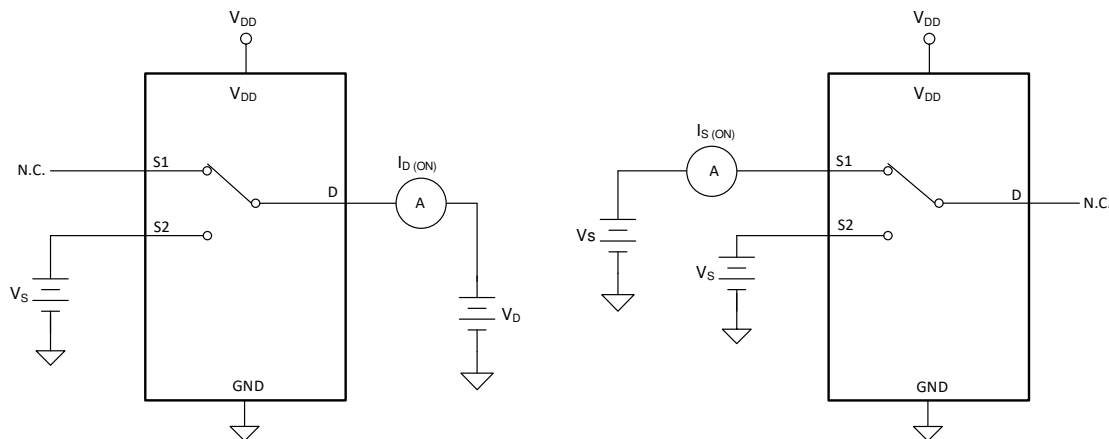


Figure 6-3. On-Leakage Measurement Setup

### 6.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure transition time, denoted by the symbol  $t_{\text{TRANSITION}}$ .

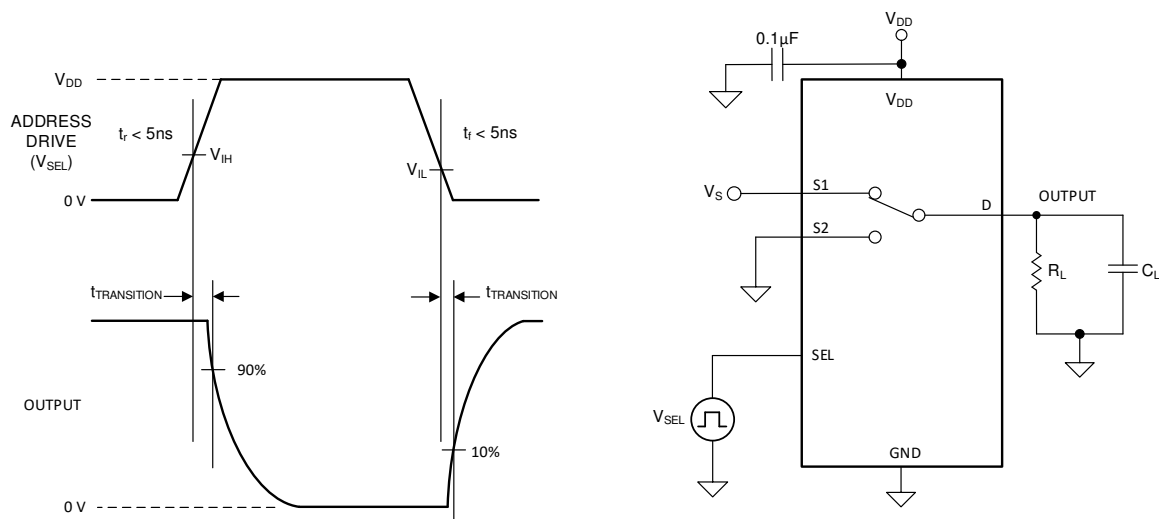


Figure 6-4. Transition-Time Measurement Setup

## 6.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 6-5 shows the setup used to measure break-before-make delay, denoted by the symbol  $t_{\text{OPEN(BBM)}}$ .

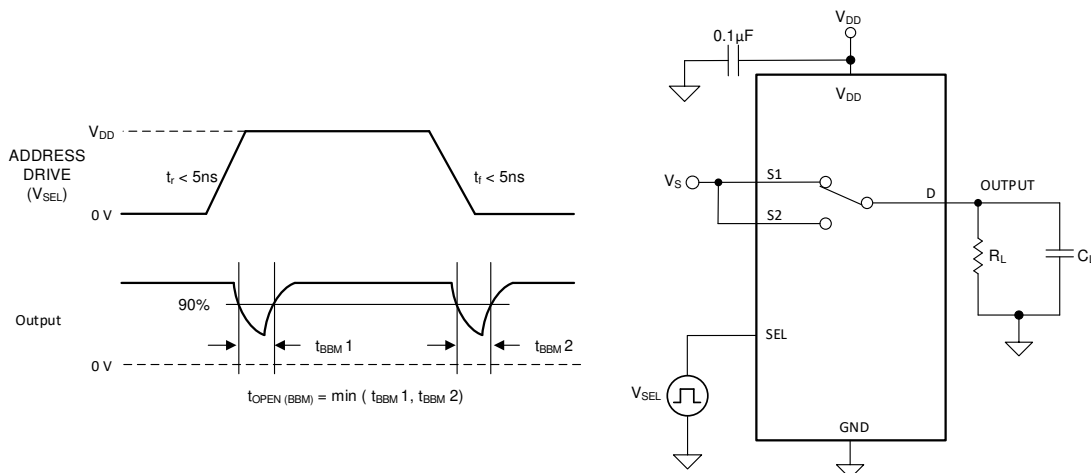


Figure 6-5. Break-Before-Make Delay Measurement Setup

## 6.6 Charge Injection

The TMUX1119 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol  $Q_C$ . Figure 6-6 shows the setup used to measure charge injection from Drain (D) to Source ( $S_x$ ).

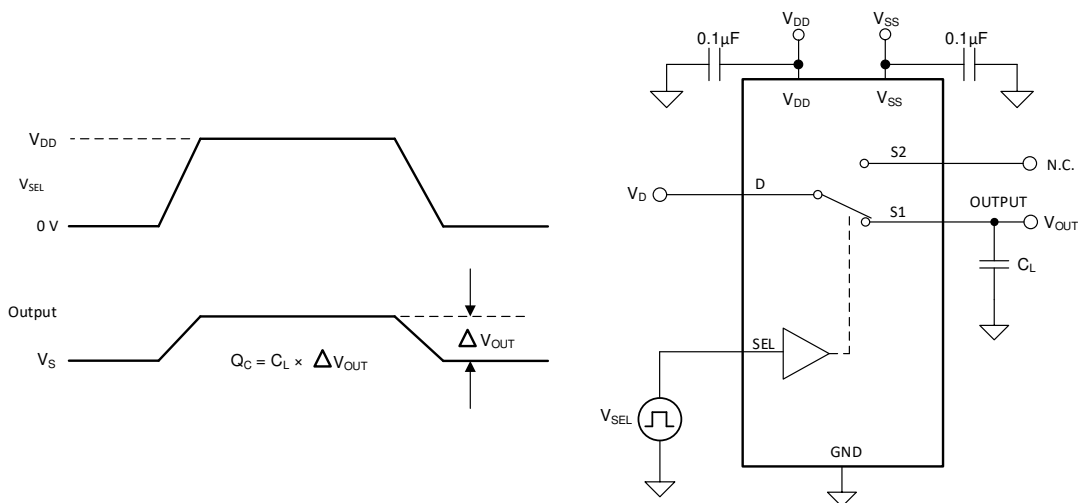
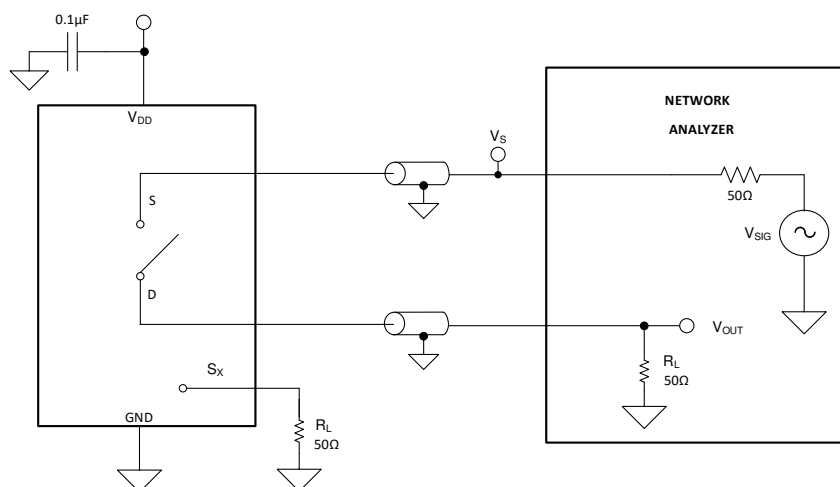


Figure 6-6. Charge-Injection Measurement Setup

## 6.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 6-7 shows the setup used to measure, and the equation used to calculate off isolation.

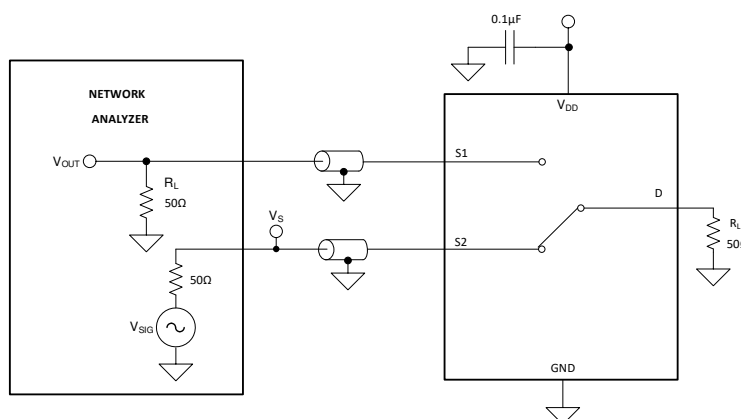


**Figure 6-7. Off Isolation Measurement Setup**

$$\text{Off Isolation} = 20 \cdot \log \left( \frac{V_{\text{OUT}}}{V_S} \right) \quad (1)$$

## 6.8 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 6-8 shows the setup used to measure, and the equation used to calculate crosstalk.



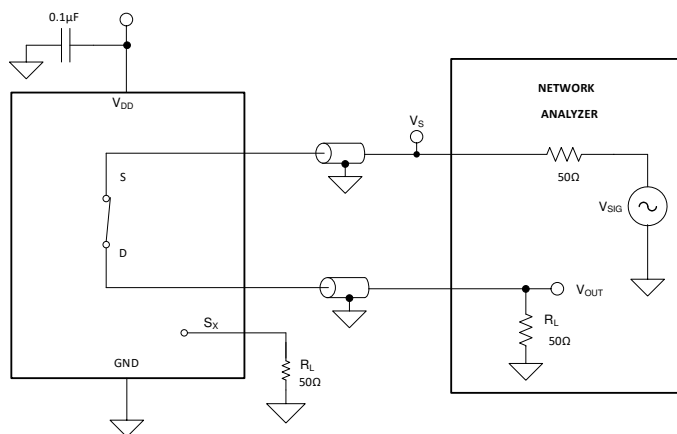
**Figure 6-8. Crosstalk Measurement Setup**

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \log \left( \frac{V_{\text{OUT}}}{V_S} \right) \quad (2)$$



## 6.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 6-9 shows the setup used to measure bandwidth.



**Figure 6-9. Bandwidth Measurement Setup**

## 7 Detailed Description

### 7.1 Overview

The TMUX1119 is an 2:1, 1-ch. (SPDT), analog switch where the input is controlled with a single select (SEL) control pin.

### 7.2 Functional Block Diagram

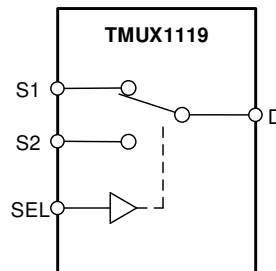


Figure 7-1. TMUX1119 Functional Block Diagram

### 7.3 Feature Description

#### 7.3.1 Bidirectional Operation

The TMUX1119 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). The device has very similar characteristics in both directions and supports both analog and digital signals.

#### 7.3.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX1119 ranges from GND to  $V_{DD}$ .

#### 7.3.3 1.8V Logic Compatible Inputs

The TMUX1119 has 1.8V logic compatible control for the logic control input (SEL). The logic input threshold scales with supply but still provide 1.8V logic control when operating at 5.5V supply voltage. 1.8V logic level inputs allow the TMUX1119 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8V logic implementations refer to [Simplifying Design with 1.8V logic Muxes and Switches](#)

#### 7.3.4 Fail-Safe Logic

The TMUX1119 supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pin of the TMUX1119 to be ramped to 5.5V while  $V_{DD} = 0V$ . Additionally, the feature enables operation of the TMUX1119 with  $V_{DD} = 1.2V$  while allowing the select pin to interface with a logic level of another device up to 5.5V.

### 7.3.5 Ultra-Low Leakage Current

The TMUX1119 provides extremely low on-leakage and off-leakage currents. The TMUX1119 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. Figure 7-2 shows typical leakage currents of the TMUX1119 versus temperature.

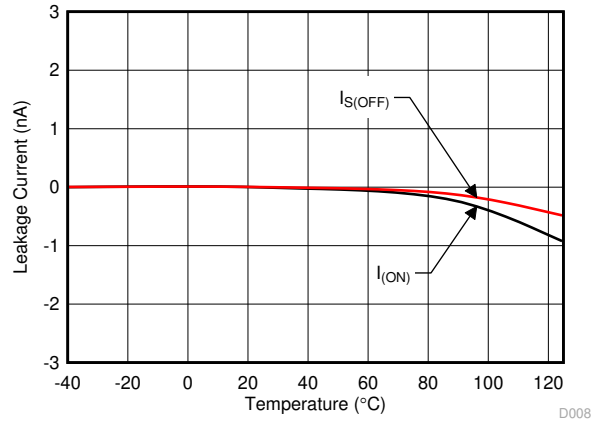


Figure 7-2. Leakage Current vs Temperature

### 7.3.6 Ultra-Low Charge Injection

The TMUX1119 has a transmission gate topology, as shown in Figure 7-3. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

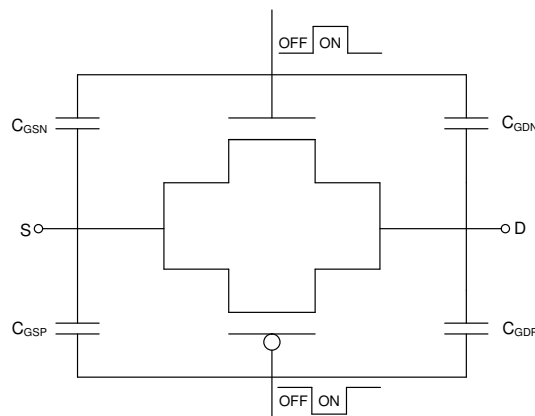
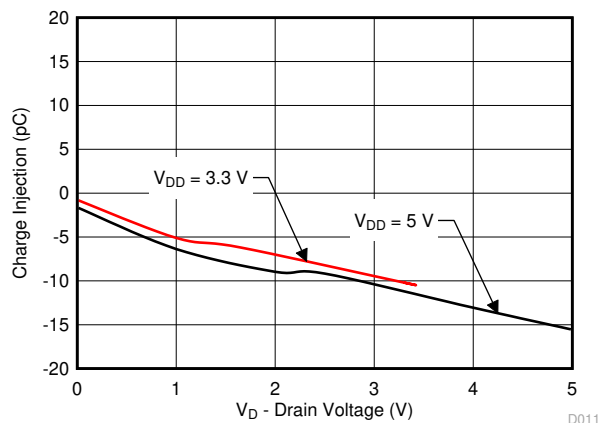


Figure 7-3. Transmission Gate Topology

The TMUX1119 has special charge-injection cancellation circuitry that reduces the drain-to-source charge injection to -6pC at  $V_D = 1V$  as shown in Figure 7-4.



**Figure 7-4. Charge Injection vs Drain Voltage**

## 7.4 Device Functional Modes

The select (SEL) pin of the TMUX1119 controls which switch is connected to the drain of the device. When a given input is not selected, that source pin is in high impedance mode (HI-Z). The control pins can be as high as 5.5V.

## 7.5 Truth Tables

**Table 7-1. TMUX1119 Truth Table**

CONTROL LOGIC (SEL)	Selected Source (Sx) Connected To Drain (D) Pin
0	S1
1	S2

## 8 Application and Implementation

### Note

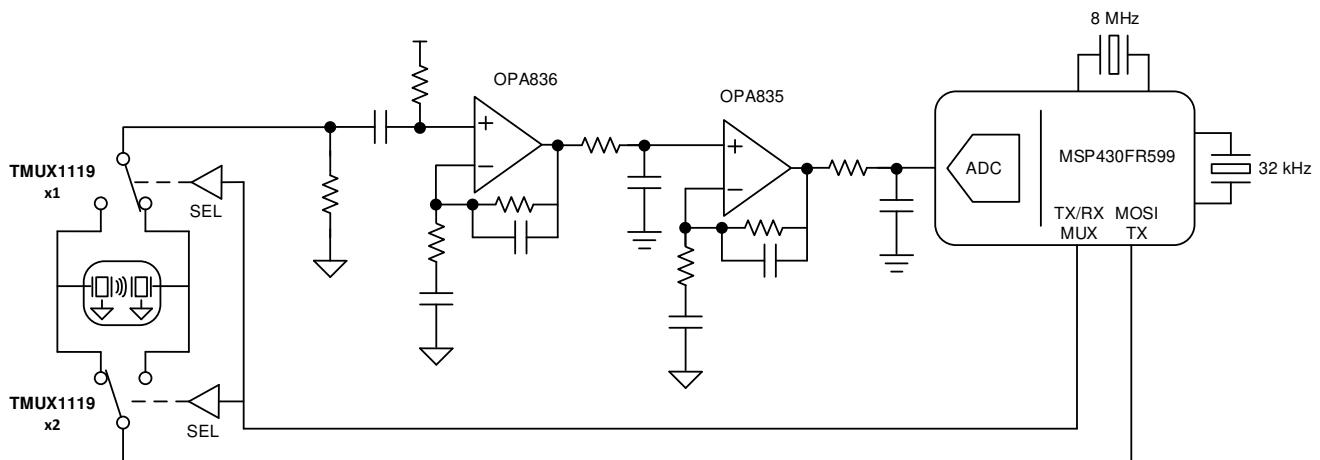
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The TMUX11xx family offers ultra-low input and output leakage currents and low charge injection. These devices operate up to 5.5V, and offer true rail-to-rail input and output of both analog and digital signals. The TMUX1119 has a low on-capacitance which allows faster settling time when multiplexing inputs in the time domain. These features make the TMUX11xx devices a family of precision, high-performance switches and multiplexers for low-voltage applications.

### 8.2 Typical Application

Figure 8-1 shows an ultrasonic gas meter front end. The ultrasonic front end design utilizes time of flight (TOF) measurement to determine the amount of gas flowing in a pipe. The circuit utilizes the MSP430FR5994, two ultra low power operational amplifiers, OPA835 and OPA836, along with two TMUX1119, 2:1 precision switches.



**Figure 8-1. Ultrasonic Gas Meter System**

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

**Table 8-1. Design Parameters**

PARAMETERS	VALUES
Supply ( $V_{DD}$ )	5V
I/O signal range	0V to $V_{DD}$ (Rail to Rail)
Control logic thresholds	1.8V compatible
Single-shot standard deviation (STD)	<2ns
Zero-flow drift (ZFD)	<1ns

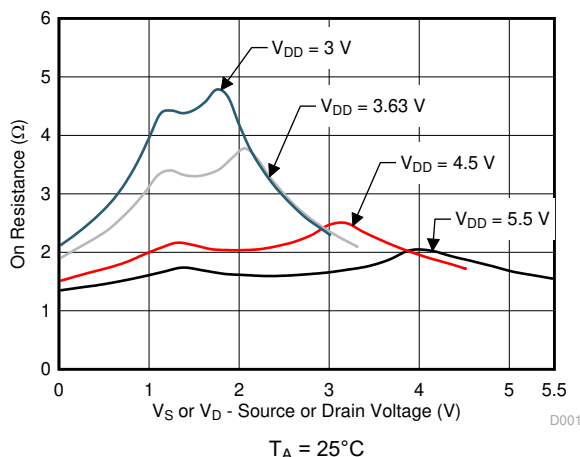
## 8.2.2 Detailed Design Procedure

The TMUX1119 can be operated without any external components except for the supply decoupling capacitors. All inputs passing through the switch must fall within the recommended operating conditions of the TMUX1119, including signal range and continuous current. For this design with a supply of 5V the signal range can be 0V to 5V, and the maximum continuous current can be 30mA.

The TMUX1119 device is a bidirectional, single-pole double-throw (SPDT) switch that offers low on-resistance, low leakage, and low power. These features make this device suitable for portable and power sensitive applications such as ultrasonic gas metering systems. The two TMUX1119 devices are used to switch the transmission and reception signals from the MCU to the two transceivers in an efficient manner without distortion. Exceptional on-resistance flatness, leakage performance, and charge injection allows the TMUX1119 to be utilized in place of the TS5A9411 in [Ultrasonic Gas Meter Front-End With MSP430™ Reference Design](#). For a more detailed analysis of the entire system refer to the [reference design](#).

## 8.2.3 Application Curve

The TMUX1119 is capable of switching signals with minimal distortion because of the ultra-low leakage currents and excellent On-resistance flatness. [Figure 8-2](#) shows how the on-resistance of the TMUX1119 varies with different supply voltages.



**Figure 8-2. On-Leakage vs Source or Drain Voltage**

## 8.3 Power Supply Recommendations

The TMUX1119 operates across a wide supply range of 1.08V to 5.5V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

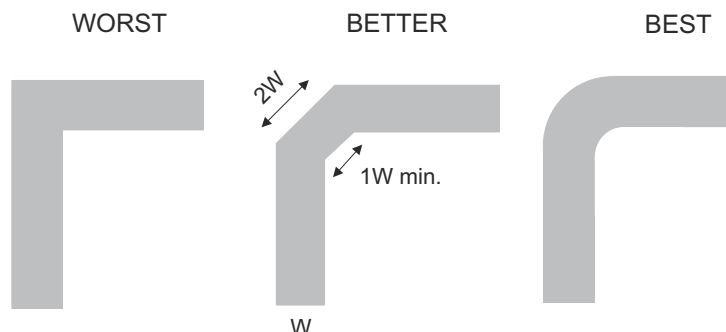
Power-supply bypassing improves noise margin and prevents switching noise propagation from the  $V_{DD}$  supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 $\mu\text{F}$  to 10 $\mu\text{F}$  from  $V_{DD}$  to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This

increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 8-3](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.



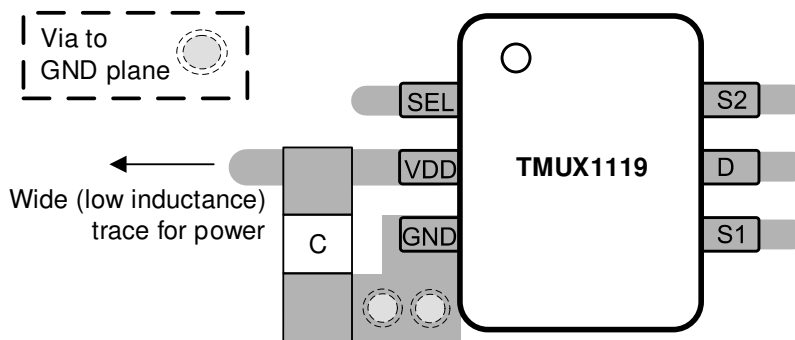
**Figure 8-3. Trace Example**

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

[Figure 8-4](#) shows an example of a PCB layout with the TMUX1119. Some key considerations are as follows:

- Decouple the  $V_{DD}$  pin with a 0.1 $\mu$ F capacitor, placed as close to the pin as possible. Ensure that the capacitor voltage rating is sufficient for the  $V_{DD}$  supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

#### 8.4.2 Layout Example



**Figure 8-4. TMUX1119 Layout Example**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Ultrasonic Gas Meter Front-End With MSP430™ Reference Design](#).
- Texas Instruments, [True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit](#).
- Texas Instruments, [Improve Stability Issues with Low CON Multiplexers](#).
- Texas Instruments, [Simplifying Design with 1.8V logic Muxes and Switches](#).
- Texas Instruments, [Eliminate Power Sequencing with Powered-off Protection Signal Switches](#).
- Texas Instruments, [System-Level Protection for High-Voltage Analog Multiplexers](#).
- Texas Instruments, [QFN/SON PCB Attachment](#).
- Texas Instruments, [Quad Flatpack No-Lead Logic Packages](#).

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.4 Trademarks

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (May 2020) to Revision C (February 2024)</b>	<b>Page</b>
• Updated Is or Id (Continuous Current) values.....	<a href="#">3</a>
• Added Ipeak values to <i>Recommended Operating Conditions</i> table.....	<a href="#">3</a>
<hr/>	
<b>Changes from Revision A (November 2019) to Revision B (May 2020)</b>	<b>Page</b>
• Changed status of DBV package From: <i>Product Preview</i> To: <i>Production Data</i> .....	<a href="#">1</a>
• Added Thermal information for DBV package.....	<a href="#">4</a>



<b>Changes from Revision * (December 2018) to Revision A (November 2019)</b>	<b>Page</b>
• Changed the data sheet title From: <i>Precision Analog Multiplexer</i> To: <i>Precision Switch</i> .....	<a href="#">1</a>
• Changed the <i>Applications</i> list.....	<a href="#">1</a>
• Changed Thermal Information for DCK package.....	<a href="#">4</a>

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TMUX1119DBVR</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26HT
TMUX1119DBVR.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26HT
<a href="#">TMUX1119DCKR</a>	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU   SN   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1DF
TMUX1119DCKR.A	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1DF
TMUX1119DCKRG4	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1DF
TMUX1119DCKRG4.A	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1DF

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1119DBVR	SOT-23	DBV	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMUX1119DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMUX1119DCKR	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TMUX1119DCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1119DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TMUX1119DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TMUX1119DCKR	SC70	DCK	6	3000	183.0	183.0	20.0
TMUX1119DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0



### SOT - 1.1 max height

Technical drawing of a connector housing, showing three views: front, side, and cross-section.

**Front View:**

- Overall width: 2.4
- Pin pitch: 1.8
- Pin diameter: 0.65
- Pin 1 INDEX AREA
- Pin 1 location: 1.4
- Pin 2 location: 1.1
- Pin 3 location: 1.3
- Pin 4 location: 2.15
- Pin 5 location: 1.85
- Pin 6 location: 0.30
- Pin 7 location: 0.15
- Pin 8 location: 0.30
- Pin 9 location: 0.15
- Pin 10 location: 0.30
- Pin 11 location: 0.15
- Pin 12 location: 0.30
- Pin 13 location: 0.15
- Pin 14 location: 0.30
- Pin 15 location: 0.15
- Pin 16 location: 0.30
- Pin 17 location: 0.15
- Pin 18 location: 0.30
- Pin 19 location: 0.15
- Pin 20 location: 0.30
- Pin 21 location: 0.15
- Pin 22 location: 0.30
- Pin 23 location: 0.15
- Pin 24 location: 0.30
- Pin 25 location: 0.15
- Pin 26 location: 0.30
- Pin 27 location: 0.15
- Pin 28 location: 0.30
- Pin 29 location: 0.15
- Pin 30 location: 0.30
- Pin 31 location: 0.15
- Pin 32 location: 0.30
- Pin 33 location: 0.15
- Pin 34 location: 0.30
- Pin 35 location: 0.15
- Pin 36 location: 0.30
- Pin 37 location: 0.15
- Pin 38 location: 0.30
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- Pin 92 location: 0.30
- Pin 93 location: 0.15
- Pin 94 location: 0.30
- Pin 95 location: 0.15
- Pin 96 location: 0.30
- Pin 97 location: 0.15
- Pin 98 location: 0.30
- Pin 99 location: 0.15
- Pin 100 location: 0.30

**Side View:**

- Overall height: 2.15
- Pin diameter: 0.1
- Pin pitch: 0.8
- Pin 1 location: 1.1
- Pin 2 location: 0.8
- Pin 3 location: 0.8
- Pin 4 location: 0.8
- Pin 5 location: 0.8
- Pin 6 location: 0.8
- Pin 7 location: 0.8
- Pin 8 location: 0.8
- Pin 9 location: 0.8
- Pin 10 location: 0.8
- Pin 11 location: 0.8
- Pin 12 location: 0.8
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- Pin 89 location: 0.8
- Pin 90 location: 0.8
- Pin 91 location: 0.8
- Pin 92 location: 0.8
- Pin 93 location: 0.8
- Pin 94 location: 0.8
- Pin 95 location: 0.8
- Pin 96 location: 0.8
- Pin 97 location: 0.8
- Pin 98 location: 0.8
- Pin 99 location: 0.8
- Pin 100 location: 0.8

**Cross-section View:**

- Top width: 0.46 TYP
- Bottom width: 0.26 TYP
- Height: 0.15
- Seating Plane
- Gage Plane
- 4X 4° -15°
- 0.22 TYP
- 0.08 TYP
- 8° TYP
- 0° TYP

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 THICK STENCIL  
 SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



**DBV0006A****PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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