TLV906xS-Q1 Automotive 10-MHz, RRIO, CMOS Operational Amplifiers

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD classification level 3A
  - Device CDM ESD classification level C6
- Rail-to-rail input and output
- Low input offset voltage: ±0.3 mV
- Unity-gain bandwidth: 10 MHz
- Low broadband noise: 10 nV/$\sqrt{Hz}$
- Low input bias current: 0.5 pA
- Low quiescent current: 538 µA
- Unity-gain stable
- Internal RFI and EMI filter
- Wide supply range: 1.8 V to 5.5 V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Shutdown version: TLV906xS
- Functional Safety-Capable
  - Documentation available to aid functional safety system design

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- Infotainment and cluster
- Passive safety
- Body electronics and lighting
- HEV/EV inverter and motor control
- On-board (OBC) and wireless charger
- Powertrain current sensor
- Advanced driver assistance systems (ADAS)
- Single-supply, low-side, unidirectional current-sensing circuit

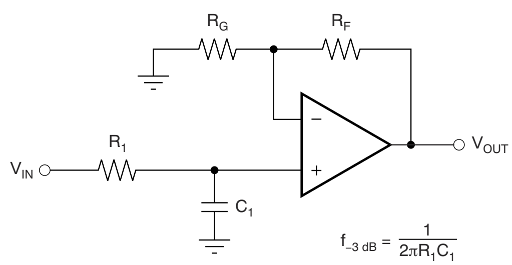
3 Description

The TLV9061-Q1 (single), TLV9062-Q1 (dual) and TLV9064-Q1 (quad) are single-, dual- and quad-low-voltage (1.8 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail input- and output-swing capabilities. These devices are cost-effective methods for automotive applications where low-voltage operation, a small footprint, and high capacitive load drive are required. Although the capacitive load drive of the TLV906x-Q1 is 100 pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler. These op amps are designed specifically for low-voltage operation (1.8 V to 5.5 V) with performance specifications similar to the OPAx316 and TLVx316 devices, and identical to their non-automotive qualified TLV906x counterparts.

Device Information

PART NUMBER(2)	CHANNEL COUNT	PACKAGE(1)	PACKAGE SIZE(3)
TLV9061-Q1	Single	DBV (SOT-23, 5)	2.90 mm × 2.80 mm
		DCK (SC70, 5)	2.00 mm × 2.2 mm
TLV9061S-Q1	Single with shutdown	DBV (SOT-23, 6)	2.90 mm × 2.80 mm
TLV9062-Q1	Dual	D (SOIC, 8)	4.90 mm × 6.00 mm
		PW (TSSOP, 8)	3.00 mm × 6.40 mm
		DGK (VSSOP, 8)	3.00 mm × 4.90 mm
TLV9064-Q1	Quad	D (SOIC, 14)	8.65 mm × 6.00 mm
		PW (TSSOP, 14)	5.00 mm × 6.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) See *Device Comparison Table*.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



$$f_{-3\,dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Single-Pole, Low-Pass Filter

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2023) to Revision H (June 2023) — **Page**

- Changed the status of the 8-PIN TSSOP (PW) packages from: *preview* to: *active* 1
- Updated the format of the *Device Information* table 1

Changes from Revision F (January 2023) to Revision G (April 2023) — **Page**

- Changed the status of the 5-PIN SC70 (DCK) packages from: *preview* to: *active* 1

Changes from Revision E (February 2021) to Revision F (January 2023) — **Page**

- Added 5-pin SOT-23 (DBV) and 5-PIN SC70 (DCK) packages to *Device Information* section 1
- Changed the *Description (continued)* section to include TLV9061-Q1 4
- Changed the *Device Comparison Table* to include 5-pin DBV and DCK 4
- Added 5-pin SOT-23 and SC70 to *Pin Configuration and Functions* section 5
- Added 5-pin DBV (SOT-23) and DCK (SC70) to the *Thermal Information: TLV9061-Q1* table 9

Changes from Revision D (October 2020) to Revision E (February 2021) — **Page**

- Deleted preview note from SOT-23 (6) package from *Device Information* section 1
- Added separate ESD rating for TLV9061S-Q1 in *ESD Ratings* table 8
- Updated DBV (SOT-23) thermal information in *Thermal Information: TLV9061S-Q1* table 9

Changes from Revision C (September 2020) to Revision D (October 2020) — **Page**

- Added TLV9061-Q1 GPN throughout the data sheet 1

Changes from Revision B (September 2020) to Revision C (September 2020) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Functional Safety-Capable document link added in the *Features* section 1
- Added note 5 to differential input voltage in *Absolute Maximum Ratings* table 8

Changes from Revision A (March 2020) to Revision B (September 2020) — **Page**

- Deleted preview note from VSSOP (8) and TSSOP (14) package from *Device Information* section 1
- Added thermal information for VSSOP (8) package in *Thermal Information* section 9

- Added thermal information for TSSOP (14) package in *Thermal Information* section....................................... 9

Changes from Revision * (April 2019) to Revision A (March 2020)	Page

- First public release of data sheet 1

5 Description (continued)

The TLV906x-Q1 family of devices serve as general-purpose automotive amplifiers for use in low-voltage systems requiring low noise and wide bandwidth or both.

The TLV906x-Q1 family helps simplify system design, because the family is unity-gain stable, integrates the RFI and EMI rejection filter, and provides no phase reversal in overdrive condition.

These devices are available in single-channel (TLV9061-Q1), dual-channel (TLV9062-Q1), and quad-channel (TLV9064-Q1) versions. The single-channel is available in industry standard 5-pin SOT-23, 5-pin SC70 and 6-pin SOT-23 packaging. The 6-pin SOT-23 package features an additional pin for shutdown functionality. Both the dual-channel and quad-channel versions are available in industry standard SOIC and TSSOP packages, with the dual channel also available as a VSSOP.

6 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS				
		DBV	DCK	D	DGK	PW
TLV9061-Q1	1	5	5	—	—	—
TLV9061S-Q1	1	6	—	—	—	—
TLV9062-Q1	2	—	—	8	8	8
TLV9064-Q1	4	—	—	14	—	14

7 Pin Configuration and Functions

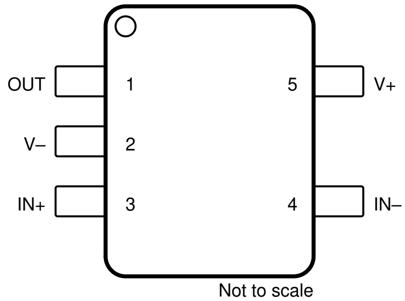


Figure 7-1. TLV9061-Q1 DBV Package, 5-Pin SOT-23 (Top View)

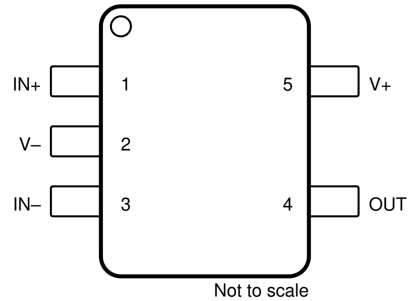


Figure 7-2. TLV9061-Q1 DCK Package, 5-Pin SC70 (Top View)

Table 7-1. Pin Functions: TLV9061-Q1

PIN			TYPE[(1)]	DESCRIPTION
NAME	DBV	DCK		
+IN	3	1	I	Noninverting input
–IN	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V–	2	2	—	Negative (lowest) power supply

(1) I = input, O = output

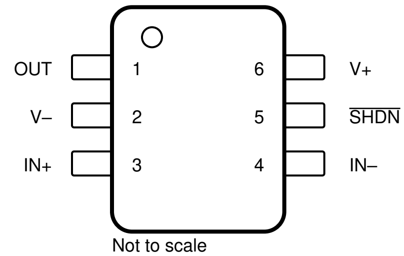


Figure 7-3. TLV9061S-Q1 DBV Package, 6-Pin SOT-23 (Top View)

Table 7-2. Pin Functions: TLV9061S-Q1

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IN–	4	I	Inverting input
IN+	3	I	Noninverting input
OUT	1	O	Output
SHDN	5	I	Shutdown: low = amp disabled, high = amp enabled. See *Shutdown Function* section for more information.
V–	2	I or —	Negative (lowest) supply or ground (for single-supply operation)
V+	6	I	Positive (highest) supply

(1) I = input, O = output

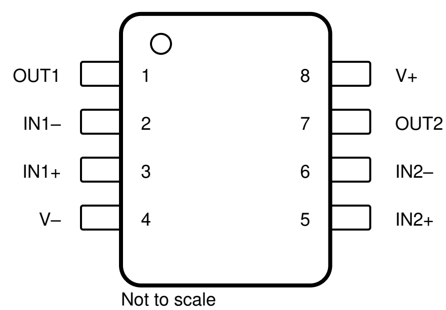


Figure 7-4. TLV9062-Q1 D, DGK, and PW Package, 8-Pin SOIC, VSSOP, and TSSOP (Top View)

Table 7-3. Pin Functions: TLV9062-Q1

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

(1) I = input, O = output

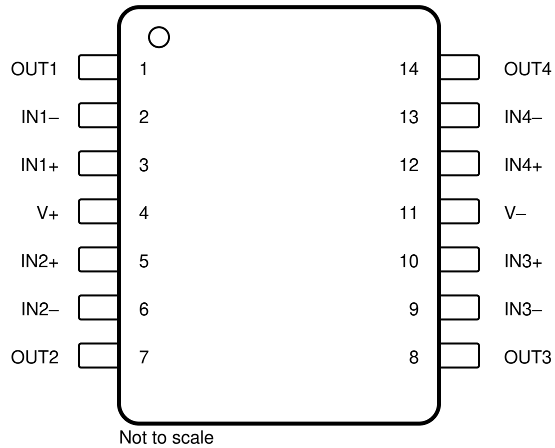


Figure 7-5. TLV9064-Q1 D and PW Package, 14-Pin SOIC and TSSOP (Top View)

Table 7-4. Pin Functions: TLV9064-Q1

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
NC	—	—	No internal connection
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	I or —	Negative (lowest) supply or ground (for single-supply operation)
V+	4	I	Positive (highest) supply

(1) I = input, O = output

8 Specifications

8.1 Absolute Maximum Ratings

over operating ambient temperature (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
Supply voltage [(V+) – (V–)]			0	6	V
Signal input pins	Voltage[(2)]	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential[(5)]		(V+) – (V–) + 0.2	V
	Current[(2)]		–10	10	mA
Output short-circuit[(3) (4)]			Continuous		mA
Temperature	Specified, T_A		–40	125	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.
(4) Long term continuous current limit is determined by electromigration limits.
(5) Differential input voltages greater than 0.5 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.

8.2 ESD Ratings

			VALUE	UNIT
TLV9061S-Q1 PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	
ALL OTHER PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JEDEC JS-001 Specification.

8.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage (V_S = [V+] – [V–])	1.8	5.5	V
V_I	Input voltage	(V–) – 0.1	(V+) + 0.1	V
V_O	Output voltage	V–	V+	V
V_{SHDN_IH}	High level input voltage at shutdown pin (amplifier enabled)	1.1	V+	V
V_{SHDN_IL}	Low level input voltage at shutdown pin (amplifier disabled)	V–	0.2	V
T_A	Specified temperature	–40	125	°C

8.4 Thermal Information: TLV9061-Q1

THERMAL METRIC[(1)]		TLV9061S-Q1	TLV9061-Q1		UNIT
		DBV (SOT-23)	DBV (SOT-23)	DCK (SC70)	
		6 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.9	232.5	246.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	130.5	131.0	157.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.7	99.6	95.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	70.1	66.5	68.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	91.5	99.1	95.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Thermal Information: TLV9062-Q1

THERMAL METRIC[(1)]		TLV9062-Q1			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	152.0	198.5	205.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.1	87.2	93.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	95.6	120.3	135.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	40.1	23.8	25.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.8	118.7	134.0	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

8.6 Thermal Information: TLV9064-Q1

THERMAL METRIC[(1)]		TLV9064-Q1		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.8	111.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.1	67.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.9	67	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.2	27.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	76.3	66.6	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

8.7 Electrical Characteristics

For V_S (total supply voltage) = (V+) – (V–) = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.3	±1.85	mV
		V_S = 5 V, T_A = –40°C to 125°C			±2	
dV_{OS}/dT	Drift	V_S = 5 V, T_A = –40°C to 125°C		±0.53		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V – 5.5 V, V_{CM} = (V–)		±7	±80	µV/V
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 1.8 V to 5.5 V	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C	80	103		dB
		V_S = 5.5 V, V_{CM} = –0.1 V to 5.6 V T_A = –40°C to 125°C	57	75		
		V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to 125°C		88		
		V_S = 1.8 V, V_{CM} = –0.1 V to 1.9 V T_A = –40°C to 125°C		70		
INPUT BIAS CURRENT						
I_B	Input bias current			±5		pA
I_{OS}	Input offset current			±5		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		4.77		μV_{PP}
e_n	Input voltage noise density	V_S = 5 V, f = 10 kHz		10		$nV/\sqrt{Hz}$
		V_S = 5 V, f = 1 kHz		16		
i_n	Input current noise density	f = 1 kHz		23		$fA/\sqrt{Hz}$
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ		100		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	104	130		
		V_S = 1.8 V, (V–) + 0.06 V < V_O < (V+) – 0.06 V, R_L = 2 kΩ		100		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5 V, G = +1		10		MHz
φ_m	Phase margin	V_S = 5 V, G = +1		55		°
SR	Slew rate	V_S = 5 V, G = +1		6.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF		0.5		µs
		To 0.01%, V_S = 5 V, 2-V step, G = +1, C_L = 100 pF		1		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.2		µs
THD + N	Total harmonic distortion + noise(1)	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz		0.0008%		
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ			20	mV
		V_S = 5.5 V, R_L = 2 kΩ			60	
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA

8.7 Electrical Characteristics (continued)

For V_S (total supply voltage) = (V+) – (V–) = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz		100		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 mA		538	750	µA
		V_S = 5.5 V, I_O = 0 mA T_A = –40°C to 125°C			800	
SHUTDOWN [2]						
I_{QSD}	Quiescent current per amplifier	V_S = 1.8 V to 5.5 V, all amplifiers disabled, $\overline{SHDN}$ = Low		0.5	1.5	µA
Z_{SHDN}	Output impedance during shutdown	V_S = 1.8 V to 5.5 V, amplifier disabled		10 || 8		GΩ || pF
$V_{SHDN\_THR\_HI}$	High level voltage shutdown threshold (amplifier enabled)	V_S = 1.8 V to 5.5 V		(V–) + 0.9	(V–) + 1.1	V
$V_{SDHN\_THR\_LO}$	Low level voltage shutdown threshold (amplifier disabled)	V_S = 1.8 V to 5.5 V	(V–) + 0.2	(V–) + 0.7		V
t_{ON}	Amplifier enable time (shutdown)[3]	V_S = 1.8 V to 5.5 V, full shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2, R_L connected to V–		10		µs
t_{OFF}	Amplifier disable time[3]	V_S = 1.8 V to 5.5 V, G = 1, V_{OUT} = 0.1 × V_S / 2, R_L connected to V–		0.6		µs
	$\overline{SHDN}$ pin input bias current (per pin)	V_S = 1.8 V to 5.5 V, V+ ≥ $\overline{SHDN}$ ≥ (V+) – 0.8 V		130		pA
		V_S = 1.8 V to 5.5 V, V– ≤ $\overline{SHDN}$ ≤ V– + 0.8 V		40		

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.
(2) Ensured by design and characterization; not production tested.
(3) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

8.8 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

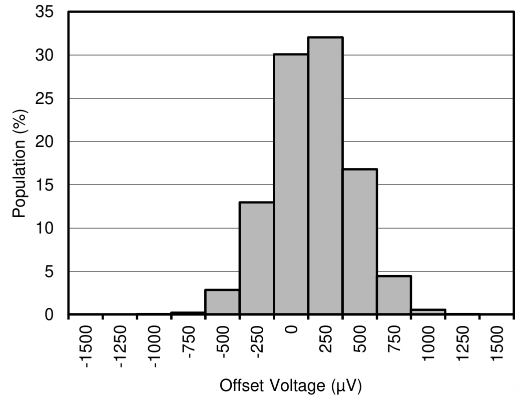
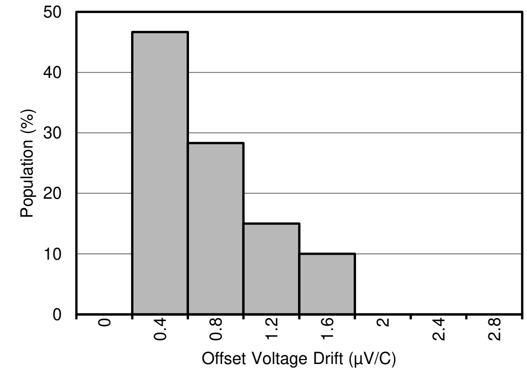


Figure 8-1. Offset Voltage Production Distribution



T_A = –40°C to 125°C

Figure 8-2. Offset Voltage Drift Distribution

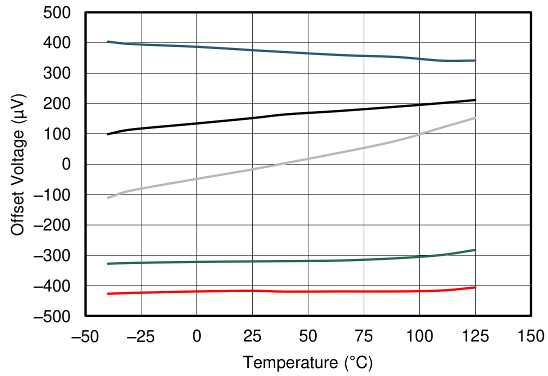
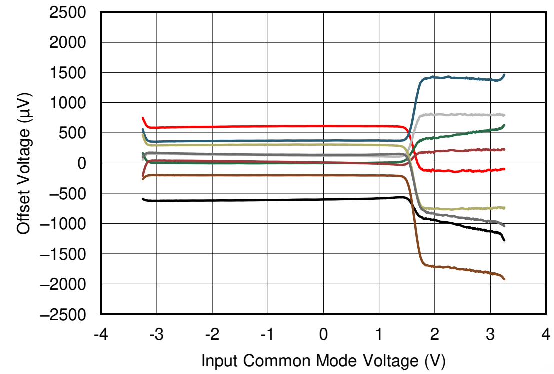
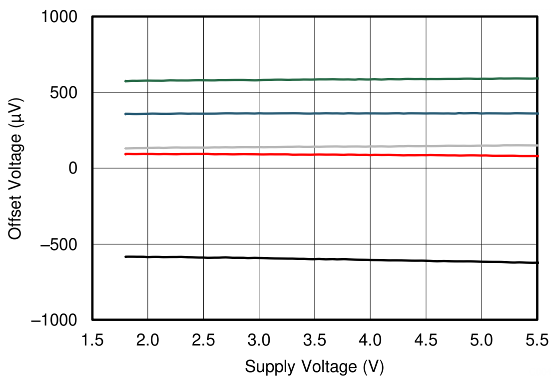


Figure 8-3. Offset Voltage vs Temperature



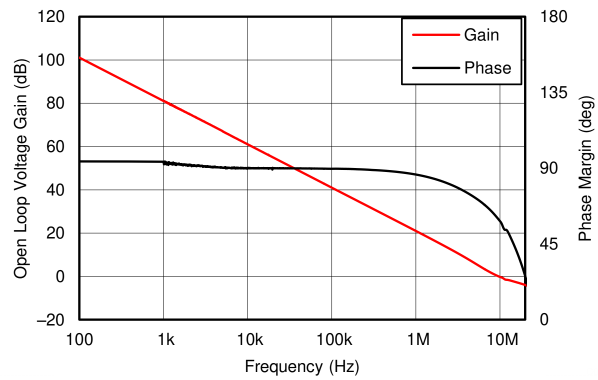
V+ = 2.75 V V– = –2.75 V

Figure 8-4. Offset Voltage vs Common-Mode Voltage



V_S = 1.8 V to 5.5 V

Figure 8-5. Offset Voltage vs Power Supply

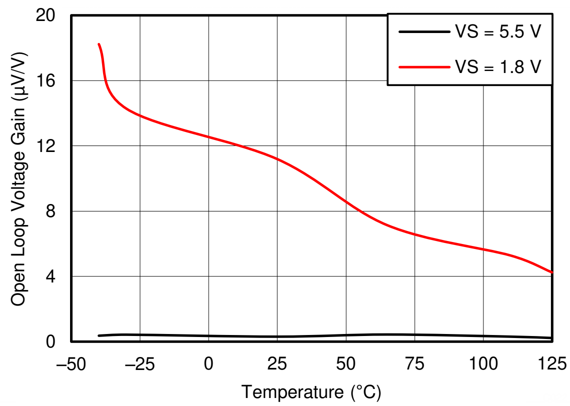


C_L = 10 pF

Figure 8-6. Open-Loop Gain and Phase vs Frequency

8.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



R_L = 2 kΩ

Figure 8-7. Open-Loop Gain vs Temperature

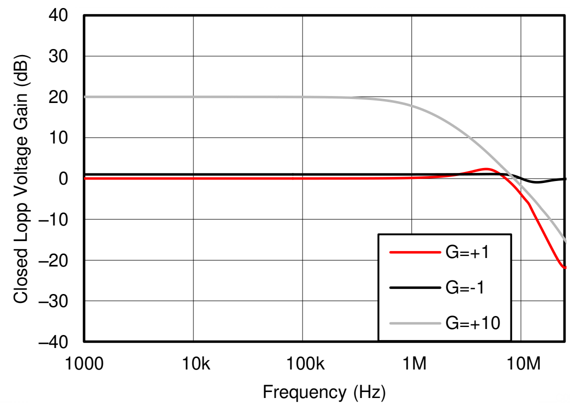


Figure 8-8. Closed-Loop Gain vs Frequency

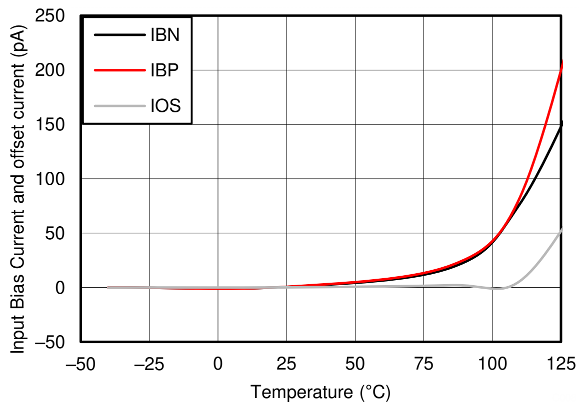
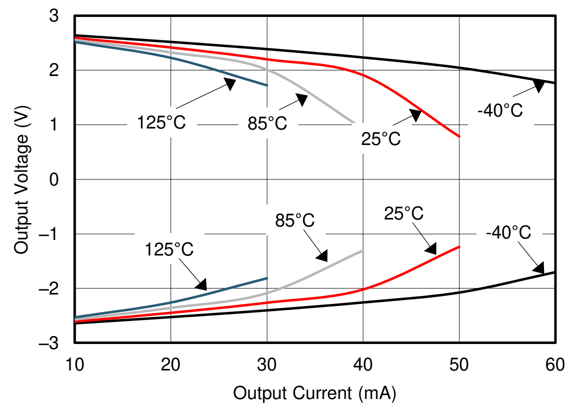


Figure 8-9. Input Bias Current vs Temperature



V+ = 2.75 V V– = –2.75 V

Figure 8-10. Output Voltage Swing vs Output Current

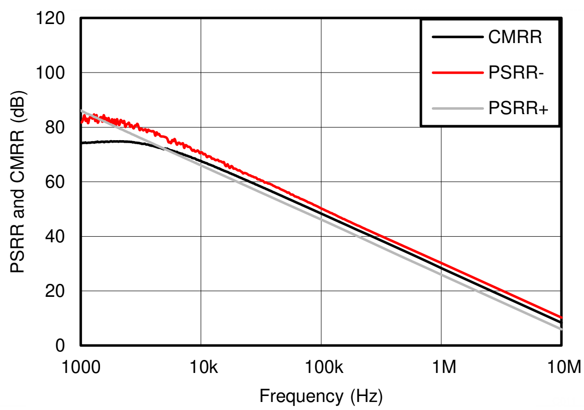
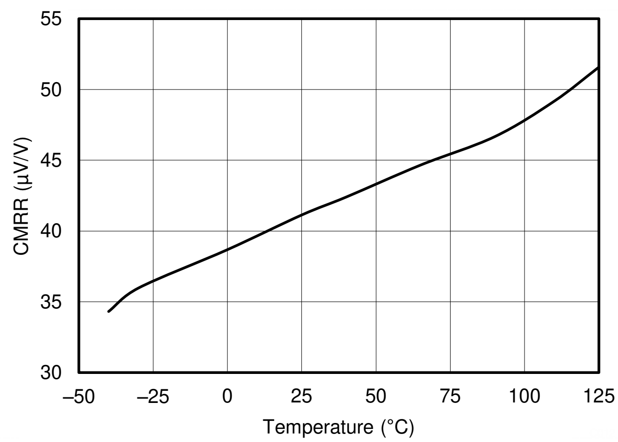


Figure 8-11. CMRR and PSRR vs Frequency (Referred to Input)

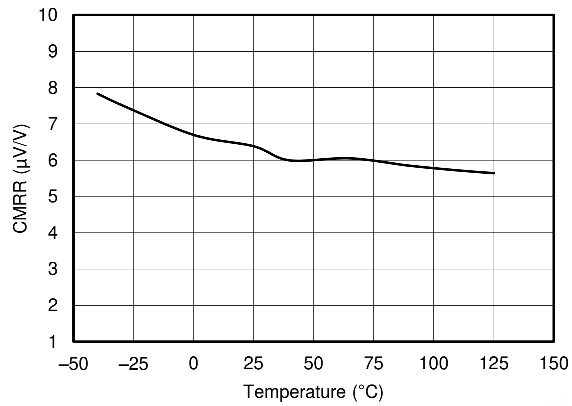


V_S = 5.5 V V_{CM} = –0.1 V to 5.6 V T_A= –40°C to 125°C
R_L= 10 kΩ

Figure 8-12. CMRR vs Temperature

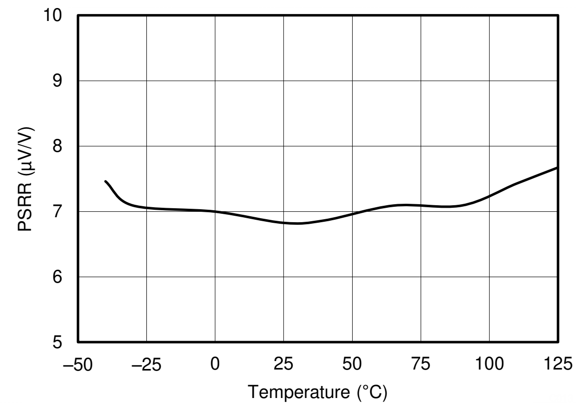
8.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



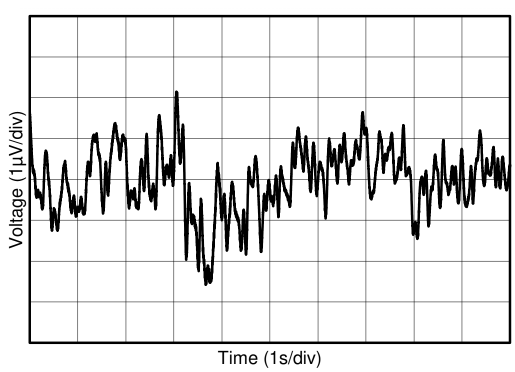
V_{CM} = (V–) – 0.1 V to (V+) – 1.4 V
T_A= –40°C to 125°C R_L= 10 kΩ V_S = 5.5 V

Figure 8-13. CMRR vs Temperature



V_S = 1.8 V to 5.5 V

Figure 8-14. PSRR vs Temperature



V_S = 1.8 V to 5.5 V

Figure 8-15. 0.1-Hz to 10-Hz Input Voltage Noise

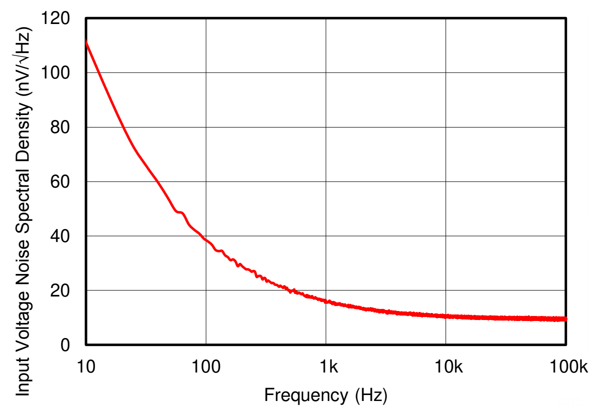
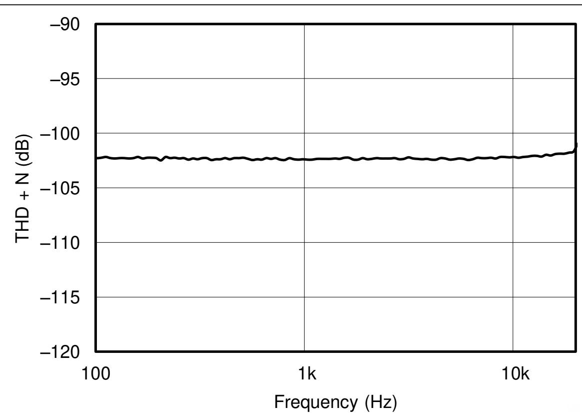
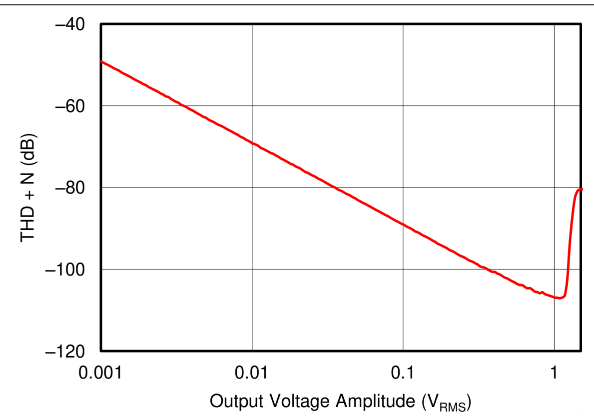


Figure 8-16. Input Voltage Noise Spectral Density vs Frequency



V_S = 5.5 V V_{CM} = 2.5 V R_L = 2 kΩ
V_{OUT} = 0.5 V_{RMS} BW = 80 kHz G = +1

Figure 8-17. THD + N vs Frequency

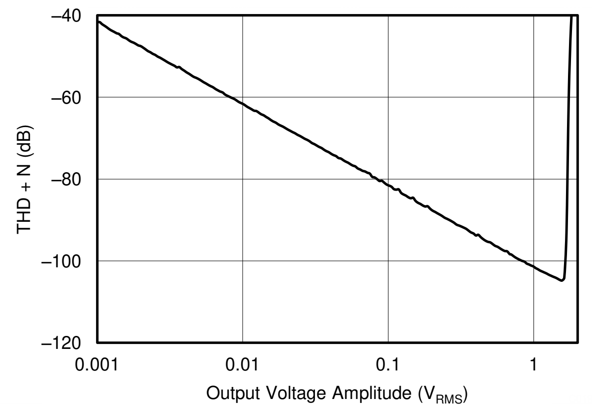


V_S = 5.5 V R_L = 2 kΩ G = +1
V_{CM} = 2.5 V BW = 80 kHz f = 1 kHz

Figure 8-18. THD + N vs Amplitude

8.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5 V V_{CM} = 2.5 V R_L = 2 kΩ
G = –1 BW = 80 kHz f = 1 kHz

Figure 8-19. THD + N vs Amplitude

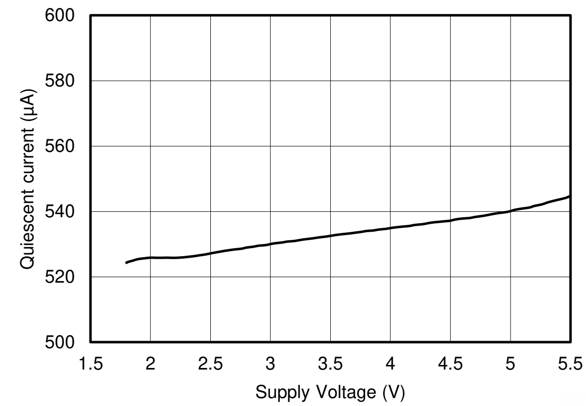


Figure 8-20. Quiescent Current vs Supply Voltage

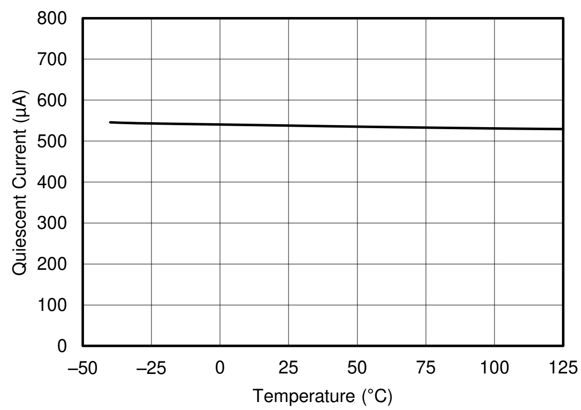


Figure 8-21. Quiescent Current vs Temperature

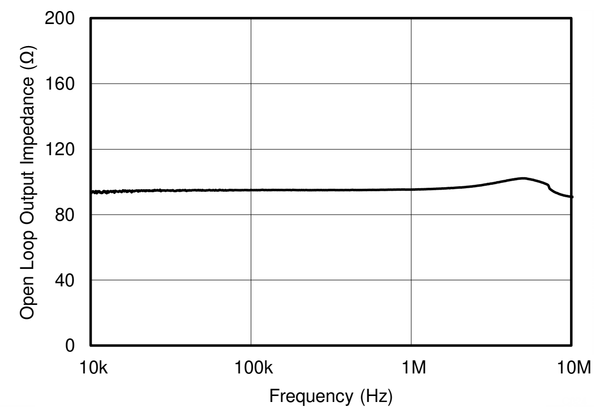
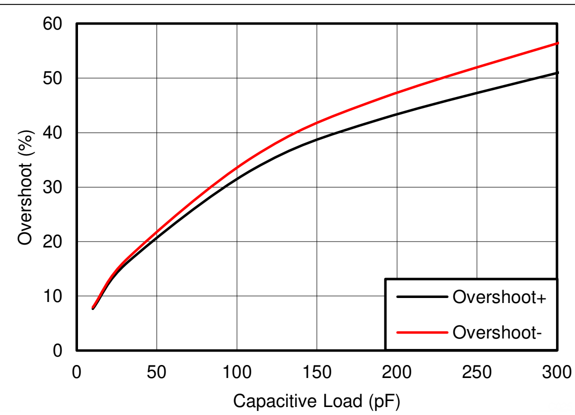
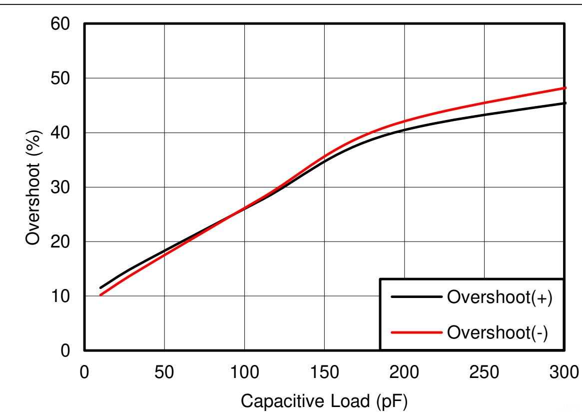


Figure 8-22. Open-Loop Output Impedance vs Frequency



V+ = 2.75 V V– = –2.75 V G = +1 V/V
V_{OUT} step = 100 mV_{p-p} R_L = 10 kΩ

Figure 8-23. Small-Signal Overshoot vs Load Capacitance

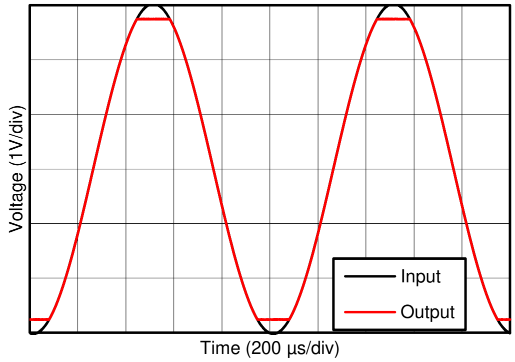


V+ = 2.75 V V– = –2.75 V G = –1 V/V
V_{OUT} step = 100 mV_{p-p} R_L = 10 kΩ

Figure 8-24. Small-Signal Overshoot vs Load Capacitance

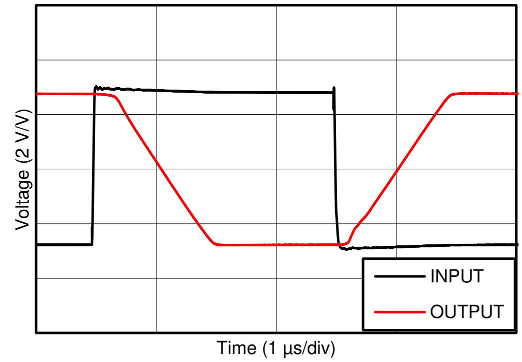
8.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



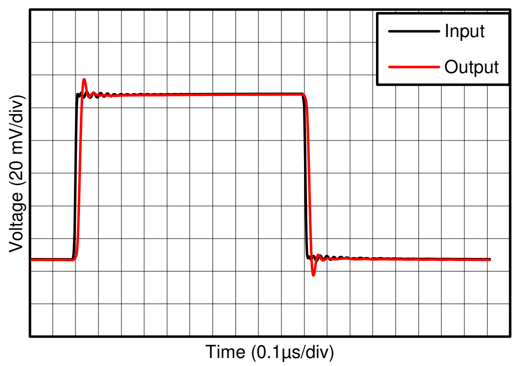
V+ = 2.75 V   V– = –2.75 V

Figure 8-25. No Phase Reversal



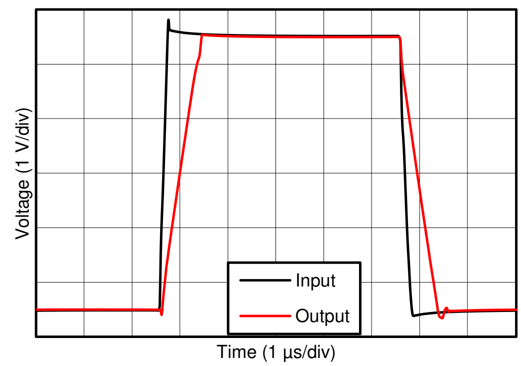
V+ = 2.75 V   V– = –2.75 V   G = –10 V/V

Figure 8-26. Overload Recovery



V+ = 2.75 V   V– = –2.75 V   G = 1 V/V

Figure 8-27. Small-Signal Step Response



V+ = 2.75 V   V– = –2.75 V C_L = 100 pF
G = 1 V/V

Figure 8-28. Large-Signal Step Response

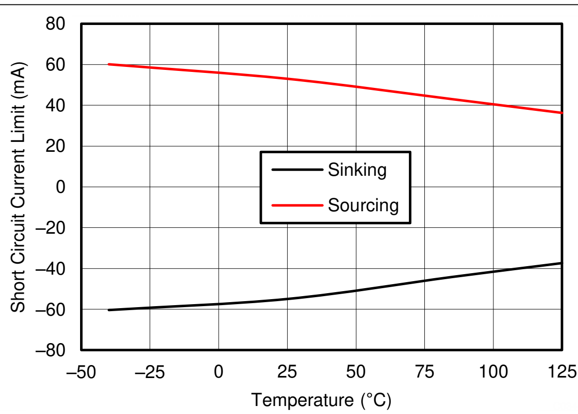
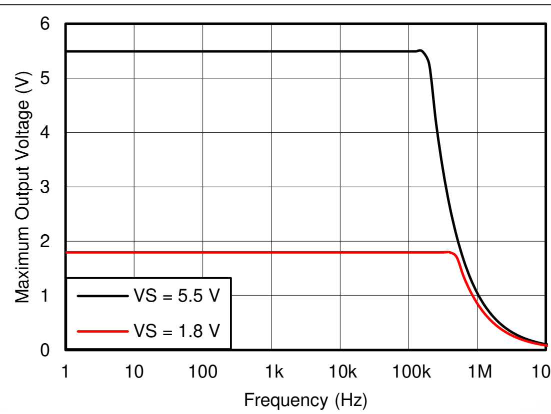


Figure 8-29. Short-Circuit Current vs Temperature

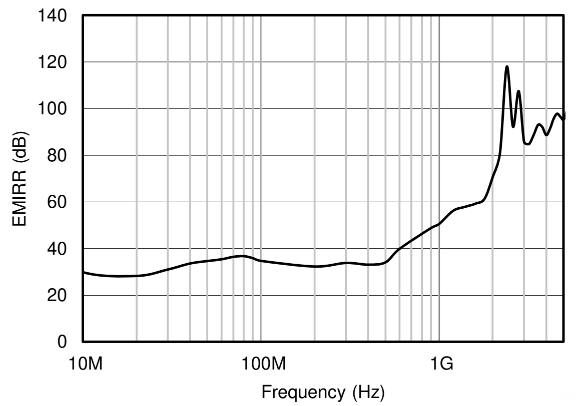


R_L = 10 kΩ C_L = 10 pF

Figure 8-30. Maximum Output Voltage vs Frequency and Supply Voltage

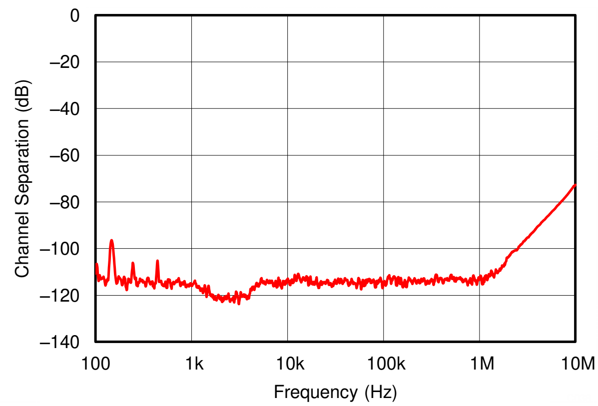
8.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



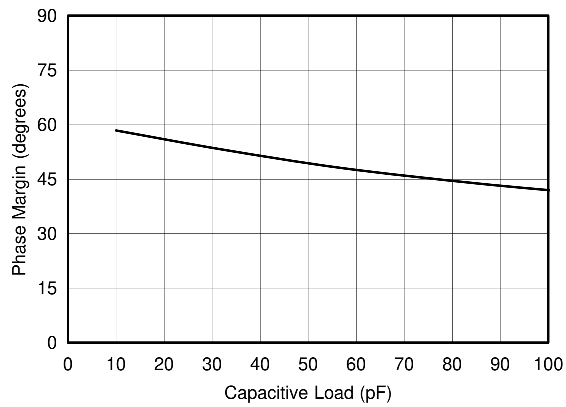
P_{RF} = –10 dBm

Figure 8-31. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



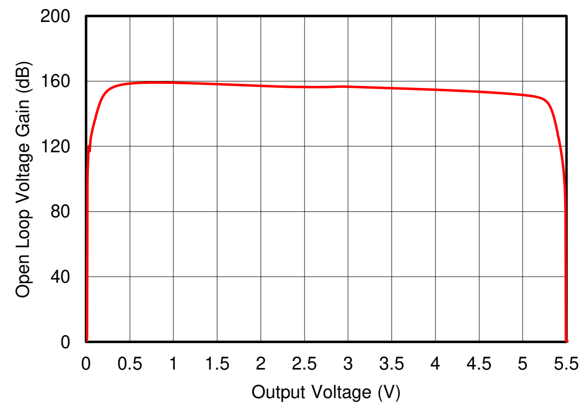
V+ = 2.75 V V– = –2.75 V

Figure 8-32. Channel Separation vs Frequency



V_S = 5.5 V

Figure 8-33. Phase Margin vs Capacitive Load



V_S = 5.5 V

Figure 8-34. Open Loop Voltage Gain vs Output Voltage

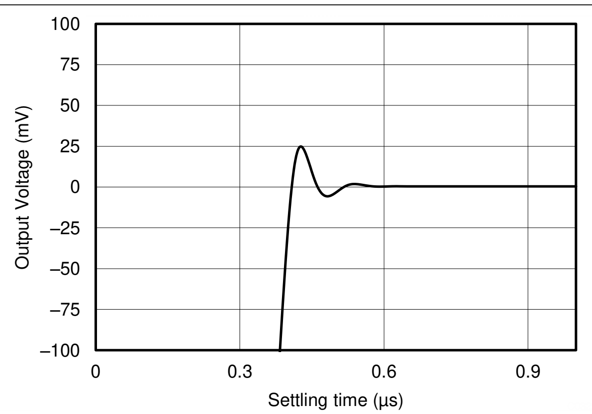


Figure 8-35. Large Signal Settling Time (Positive)

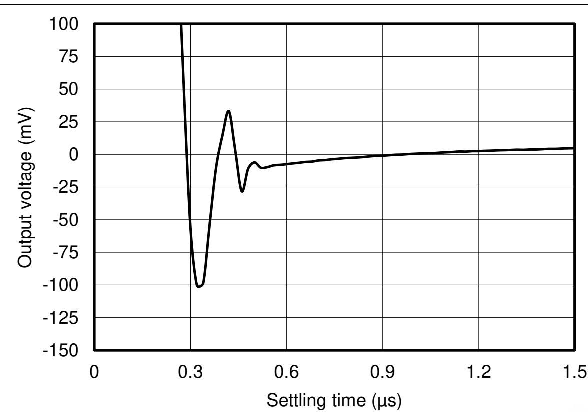


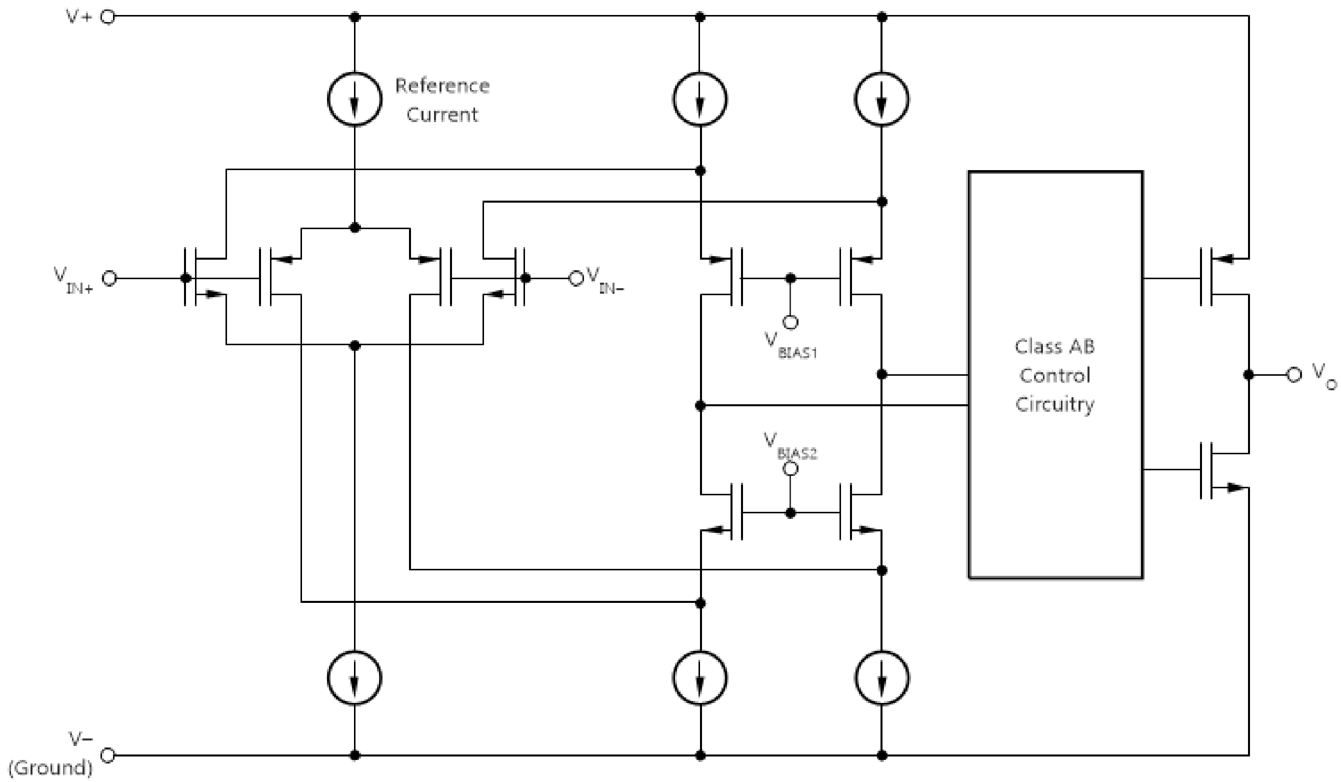
Figure 8-36. Large Signal Settling Time (Negative)

9 Detailed Description

9.1 Overview

The TLV906x-Q1 devices are a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV906x-Q1 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. The high bandwidth enables this family to drive the sample-hold circuitry of analog-to-digital converters (ADCs).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TLV906x-Q1 family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram* section. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

9.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV906x-Q1 series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10-kΩ, the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

9.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV906x-Q1 family is approximately 200 ns.

9.3.4 Shutdown Function

The TLV906xS-Q1 devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing the op amp into a low-power standby mode. In this mode, the op amp typically consumes less than 1 µA. The $\overline{\text{SHDN}}$ pins are active-low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to maintain smooth switching characteristics. To make sure of excellent shutdown behavior, the $\overline{\text{SHDN}}$ pins must be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.2 V and V+. The shutdown pin must either be connected to a valid high or a low voltage or driven, and not left as an open circuit.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled, and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life. The enable time is 10 µs for full shutdown of all channels; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the TLV906xS-Q1 to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To make sure of shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required. If using the TLV906xS-Q1 without a load, then the resulting turnoff time is significantly increased.

9.4 Device Functional Modes

Devices in the TLV906x-Q1 family are operational when the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V). The TLV906xS devices feature a shutdown mode and are shut down when a valid logic low is applied to the shutdown pin.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TLV906x-Q1 family features 10-MHz bandwidth and 6.5-V/µs slew rate with only 538 µA of supply current per channel, providing good AC performance at very low power consumption. DC applications are well served with a very low input noise voltage of 10 nV/√ Hz at 10 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

10.2 Typical Applications

10.2.1 Typical Low-Side Current Sense Application

Figure 10-1 shows the TLV906x-Q1 configured in a low-side current-sensing application.

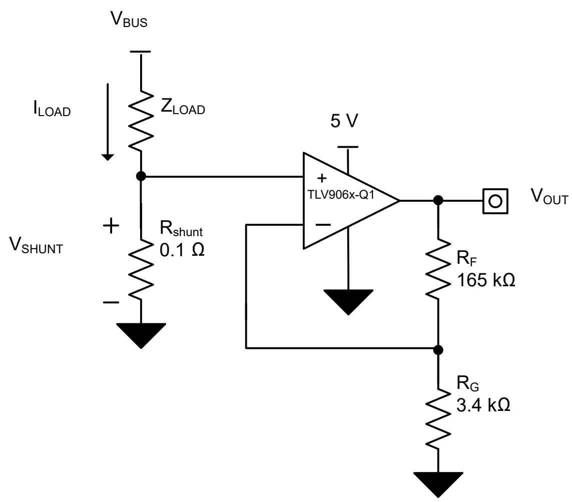


Figure 10-1. TLV906x-Q1 in a Low-Side, Current-Sensing Application

10.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

10.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 10-1 is given in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times GAIN \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \tag{2}$$

Using Equation 2, R_{SHUNT} equals 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV906x-Q1 to produce an output voltage of approximately 0 V to 4.95 V. Equation 3 calculates the gain required for the TLV906x-Q1 to produce the required output voltage.

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \tag{3}$$

Using Equation 3, the required gain equals 49.5 V/V, which is set with the R_F and R_G resistors. Equation 4 sizes the R_F and R_G, resistors to set the gain of the TLV906x-Q1 to 49.5 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \tag{4}$$

Selecting R_F to equal 165 kΩ and R_G to equal 3.4 kΩ provides a combination that equals approximately 49.5 V/V. Figure 10-2 shows the measured transfer function of the circuit shown in Figure 10-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistor values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no best impedance selection that works for every system; designers must choose an impedance that is best for the system parameters.

10.2.1.3 Application Curve

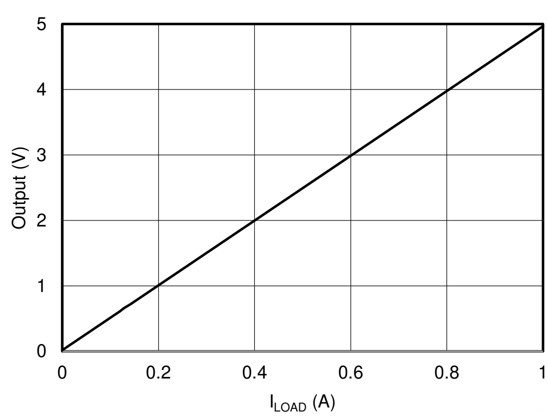


Figure 10-2. Low-Side, Current-Sense, Transfer Function

10.2.2 Typical Comparator Application

Comparators are used to differentiate between two different signal levels. For example, a comparator can be used to differentiate between an overvoltage situation and normal operation. The TLV9062-Q1 can be used as a comparator by applying the two voltages being compared to each input without any feedback from output to inverting input.

The TLV9062-Q1 features a rail-to-rail input and output stage with an input common-mode range that exceeds the supply rails by 100 mV. The TLV9062-Q1 is designed to prevent phase reversal over the entire input common-mode range. The propagation delay for the TLV9062-Q1 used as a comparator is equal to the overload recovery time plus the slew rate. Overdrive voltages less than 100 mV result in longer propagation delays because the overload recovery time increases and the slew rate decreases.

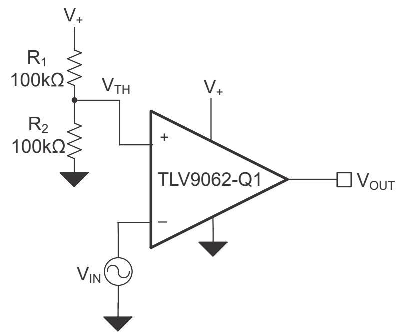


Figure 10-3. Typical Comparator Application

10.2.2.1 Design Requirements

The design requirements for this design are:

- Supply voltage (V_+): 5 V
- Input (V_{IN}): 0 V to 5 V
- Threshold voltage (V_{TH}): 2.5 V

10.2.2.2 Detailed Design Procedure

The inverting comparator circuit applies the input voltage (V_{IN}) to the inverting terminal of the op amp. Two resistors (R1 and R2) divide the supply voltage (V_{CC}) to create a midsupply threshold voltage (V_{TH}) as calculated in Equation 5. The circuit is shown in Figure 10-3. When V_{IN} is less then V_{TH}, the output voltage transitions to the positive supply and equals the high-level output voltage. When V_{IN} is greater than V_{TH}, the output voltage transitions to the negative supply and equals the low-level output voltage, V_{TH}.

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_+ = 2.5\,V \tag{5}$$

10.2.2.3 Application Curves

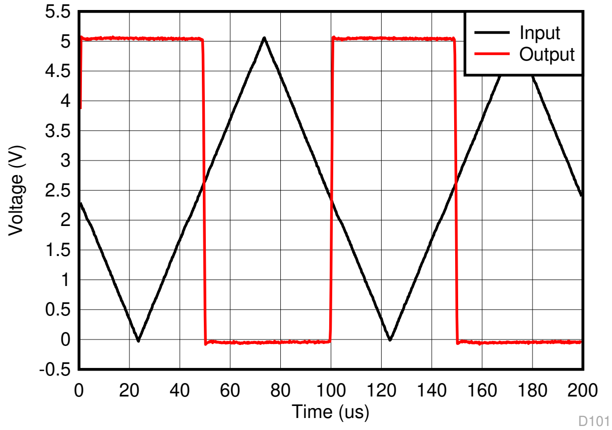


Figure 10-4. Comparator Response to Input Voltage (Propagation Delay Included)

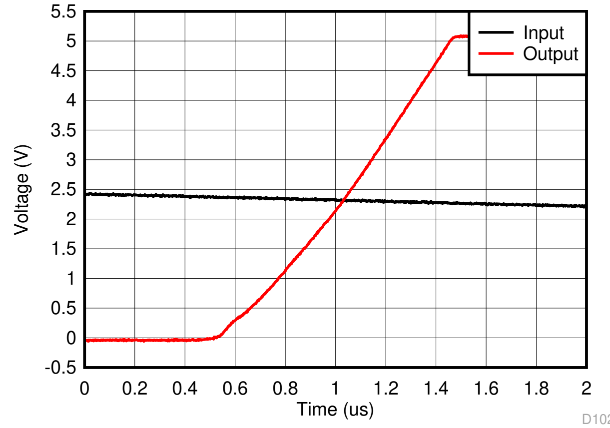


Figure 10-5. Rising Edge

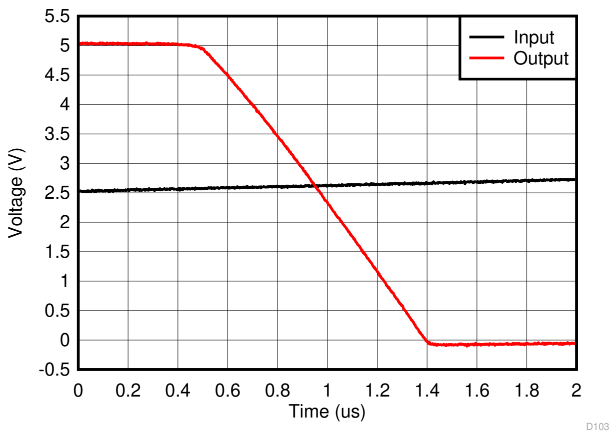


Figure 10-6. Falling Edge

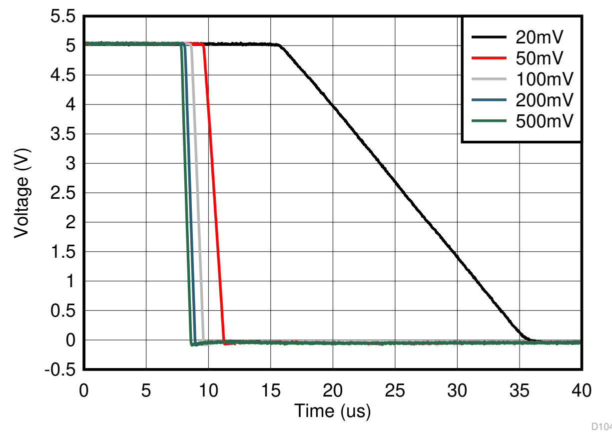


Figure 10-7. Falling Edge Propagation Delay vs Input Overdrive Voltage

10.3 Power Supply Recommendations

The TLV906x-Q1 series is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

> **CAUTION**
>
> Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

10.3.1 Input and ESD Protection

The TLV906x-Q1 series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as shown in the *Absolute Maximum Ratings* table. Figure 10-8 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

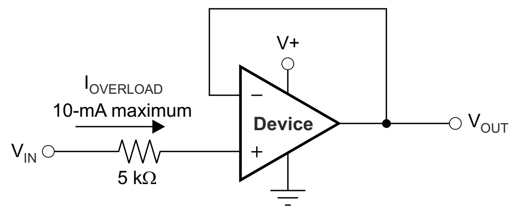


Figure 10-8. Input Current Protection

10.4 Layout

10.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 10-10, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.4.2 Layout Example

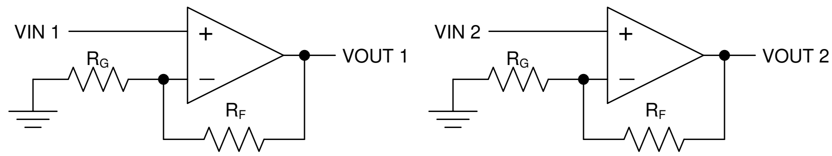


Figure 10-9. Schematic Representation

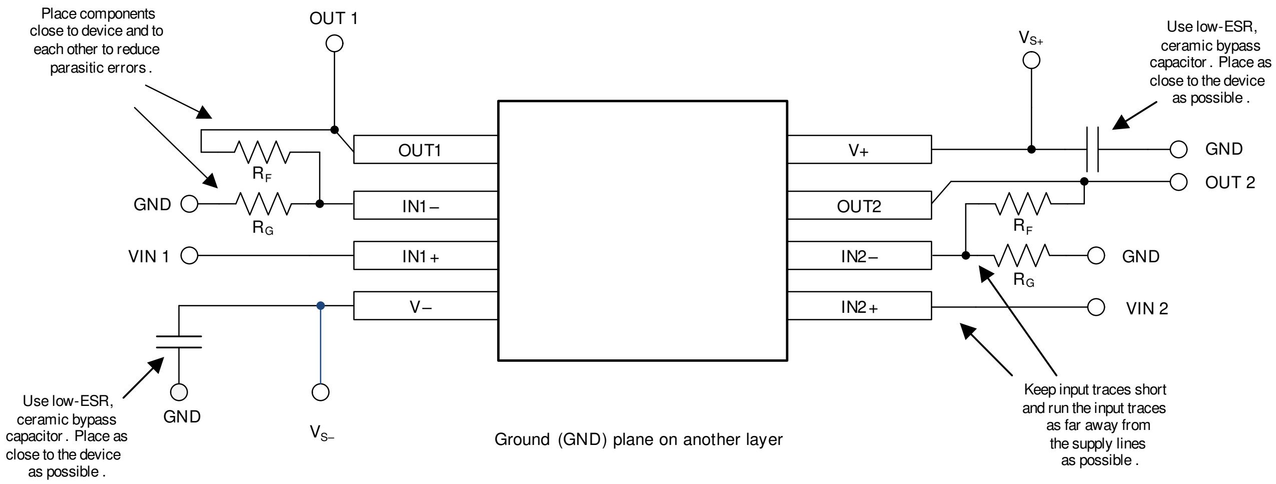


Figure 10-10. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TLVx313-Q1 Low-Power, Rail-to-Rail In/Out, 500-μV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet.
- Texas Instruments, *TLVx314-Q1 3-MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier* data sheet.
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report.
- Texas Instruments, *QFN/SON PCB Attachment* application report.
- Texas Instruments, *Single-Ended Input to Differential Output Conversion Circuit Reference Design*.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9061QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1N2
TLV9061QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1N2
TLV9061QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1N5
TLV9061QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1N5
TLV9061SQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2CTF
TLV9061SQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2CTF
TLV9062QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27CT
TLV9062QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27CT
TLV9062QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9062Q
TLV9062QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9062Q
TLV9062QPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QTL906
TLV9062QPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QTL906
TLV9064QDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9064QD
TLV9064QDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9064QD
TLV9064QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9064Q
TLV9064QPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9064Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

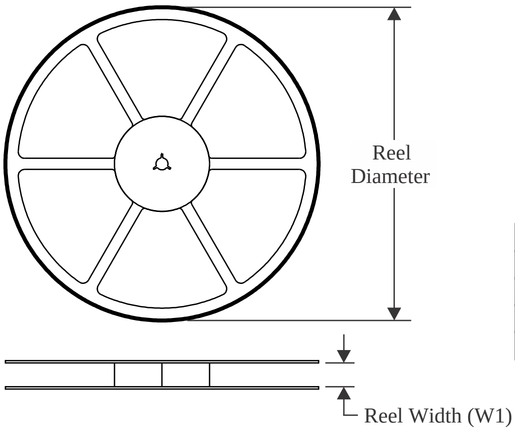
OTHER QUALIFIED VERSIONS OF TLV9061-Q1, TLV9062-Q1, TLV9064-Q1 :

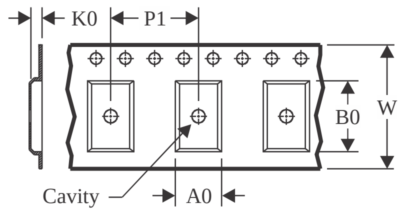
- Catalog : TLV9061, TLV9062, TLV9064

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

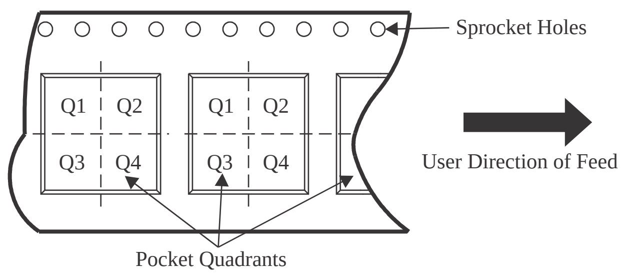
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

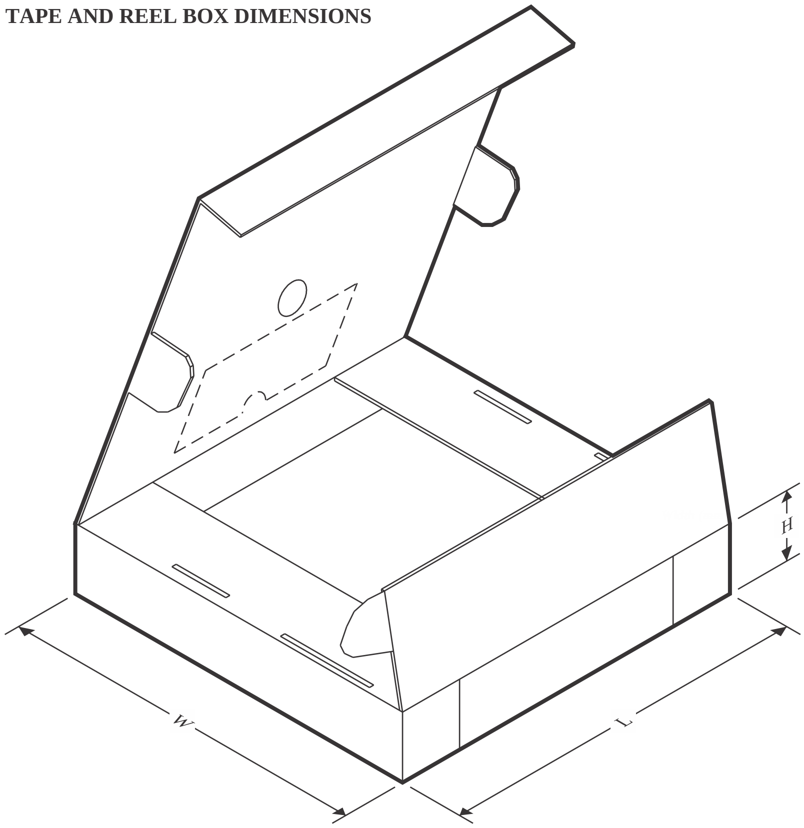
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

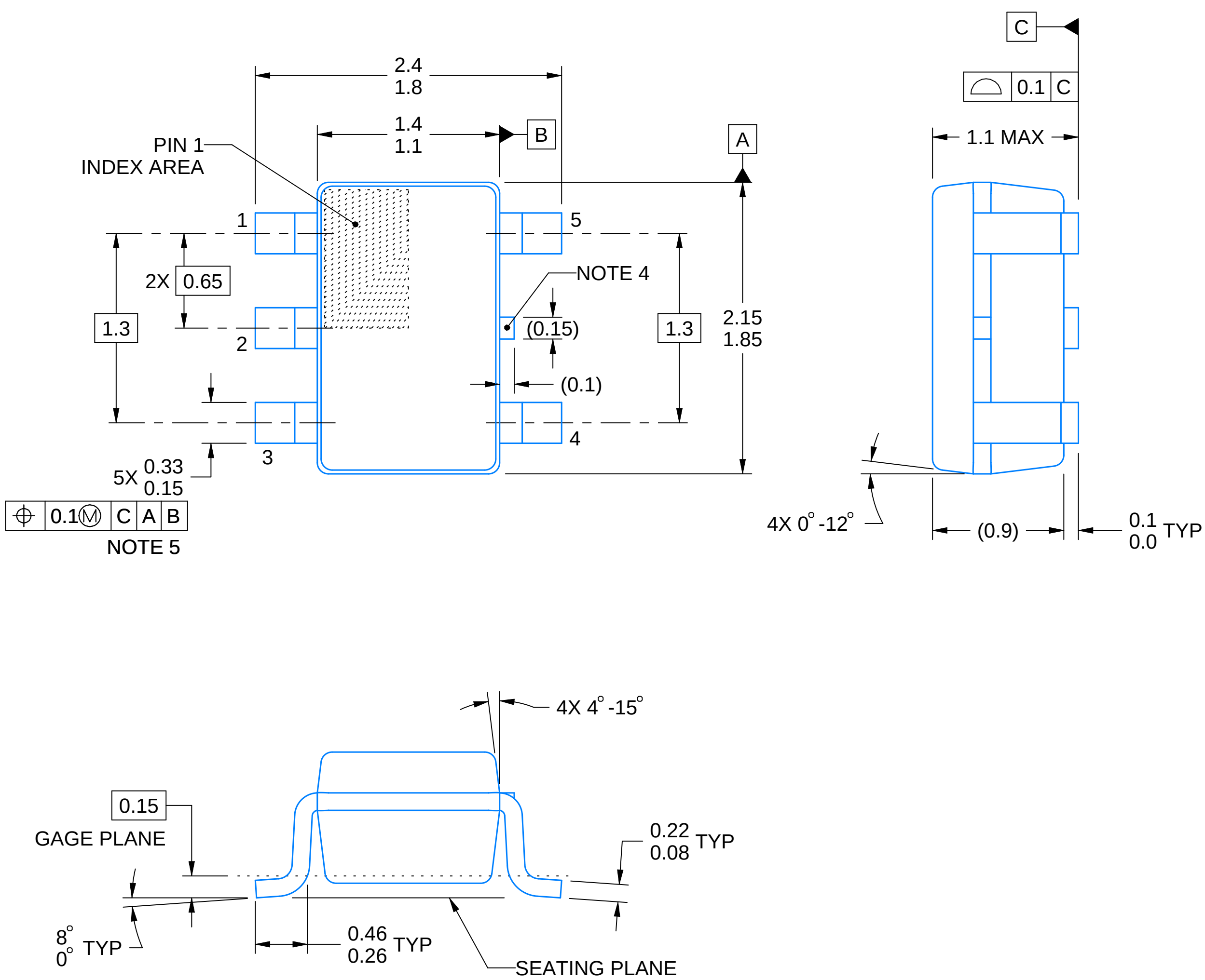
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9061QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9061SQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9062QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV9062QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062QPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9064QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9064QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

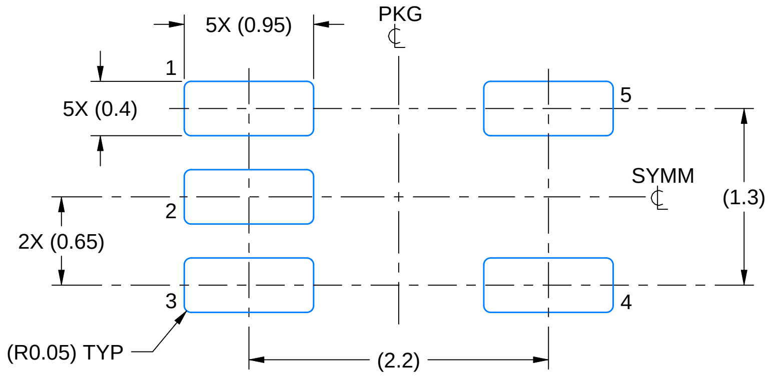
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9061QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9061QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
TLV9061SQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9062QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9062QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TLV9062QPWRQ1	TSSOP	PW	8	3000	353.0	353.0	32.0
TLV9064QDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
TLV9064QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0



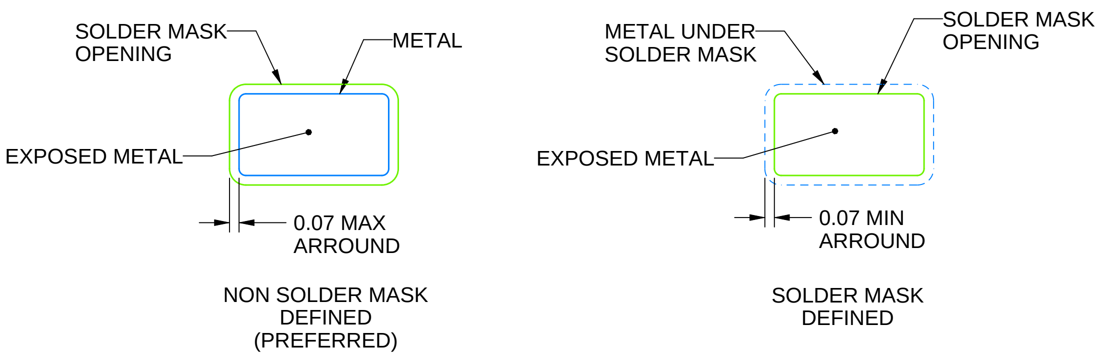
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

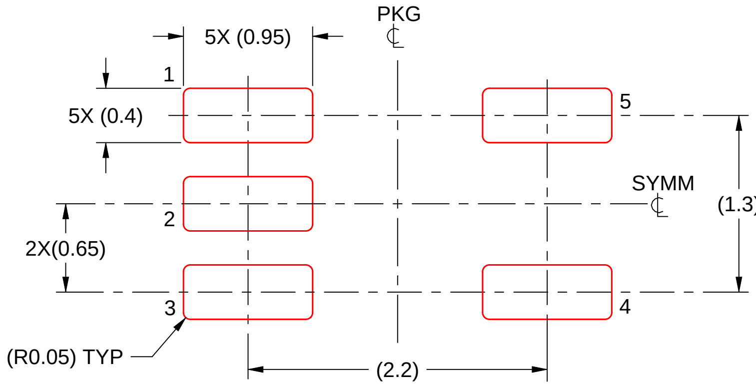


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

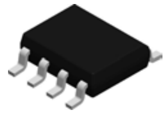


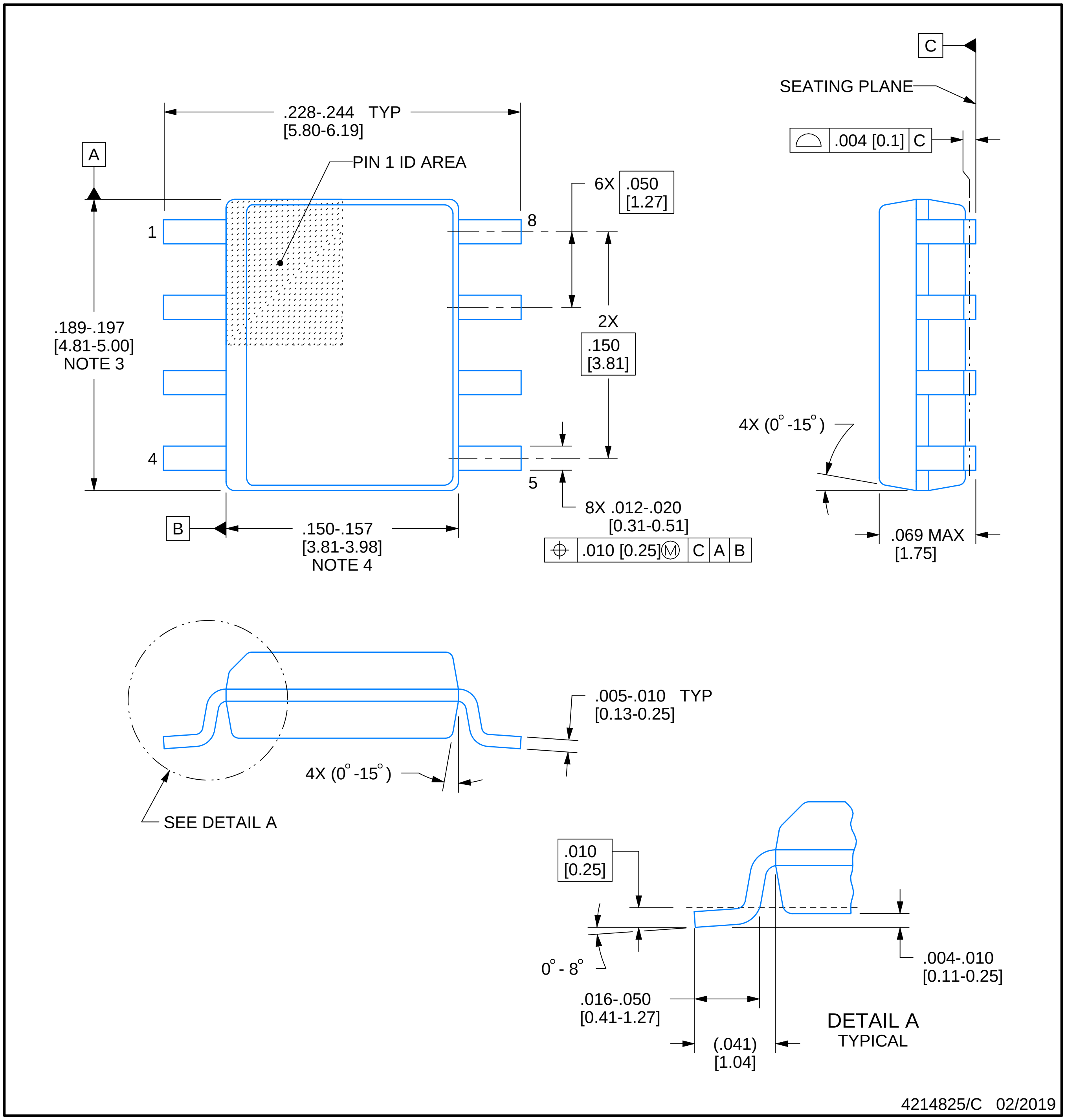
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

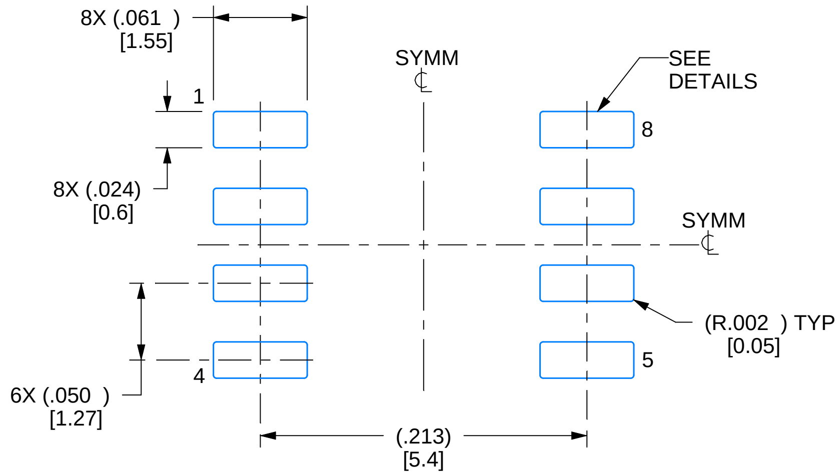
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



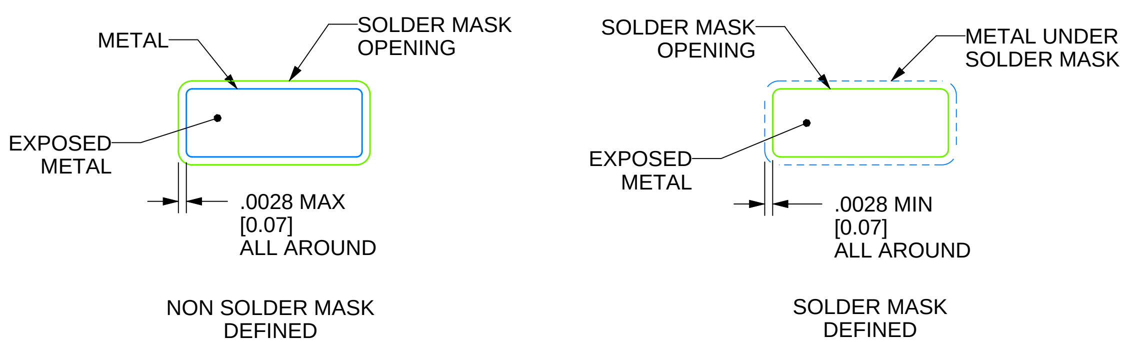


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

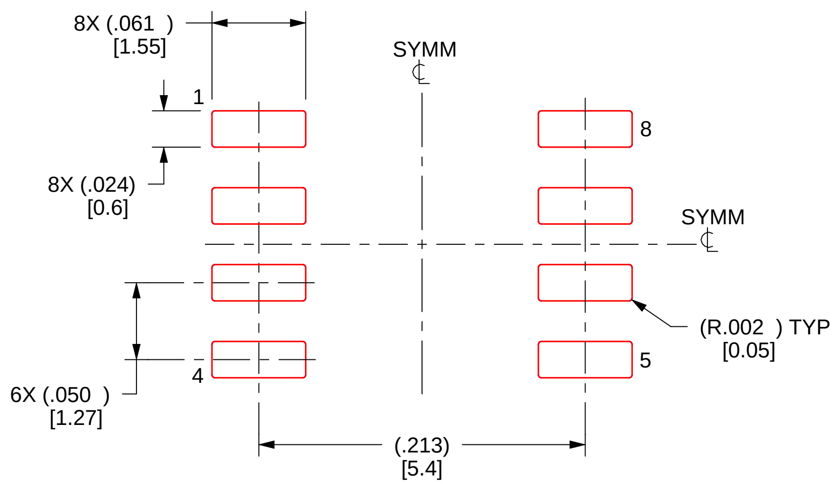


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

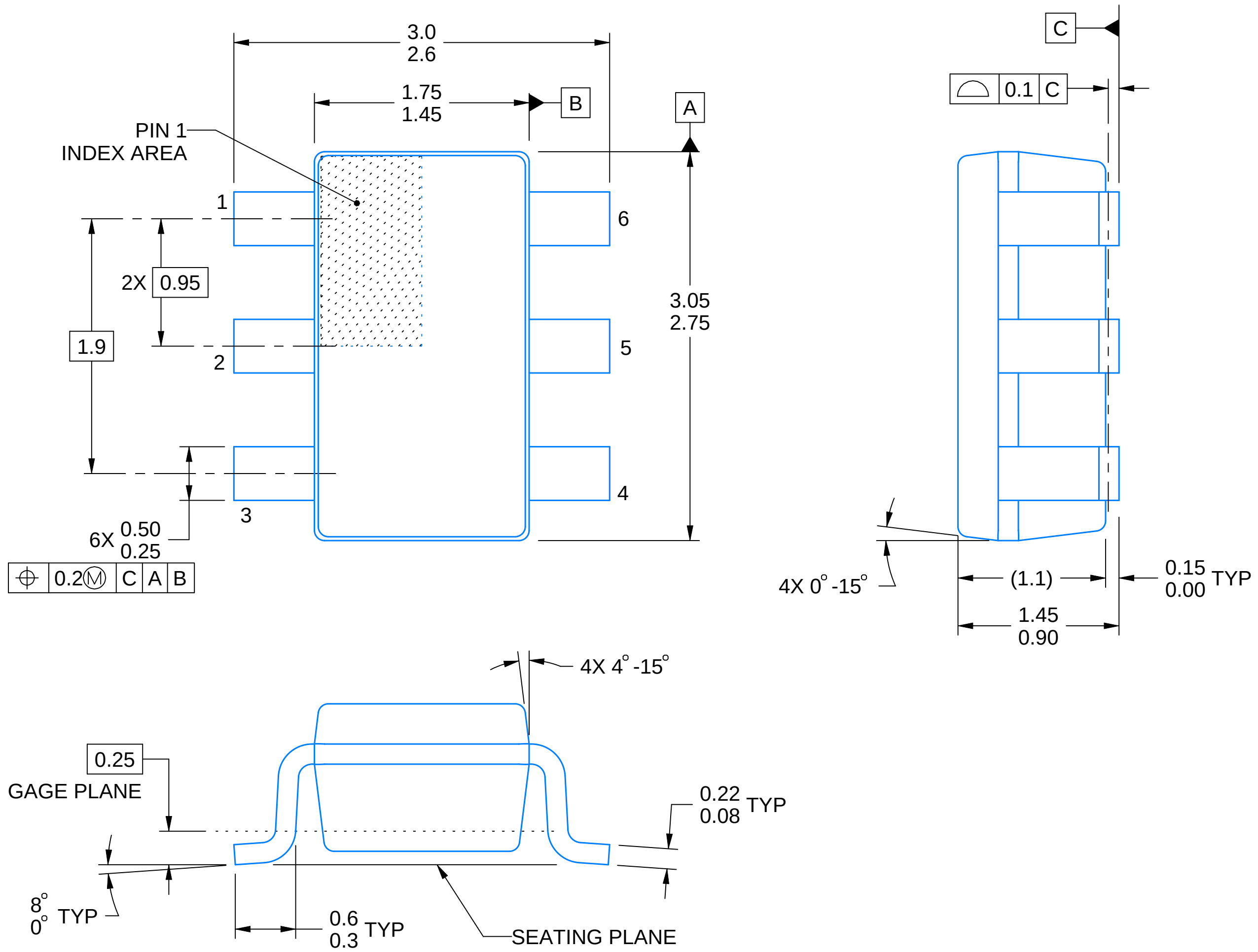


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

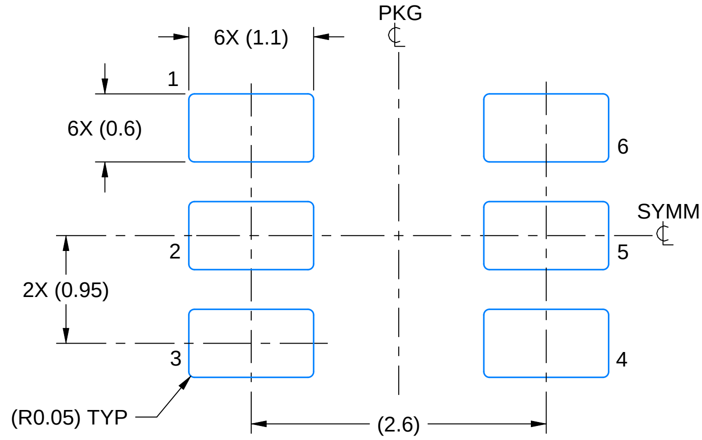
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



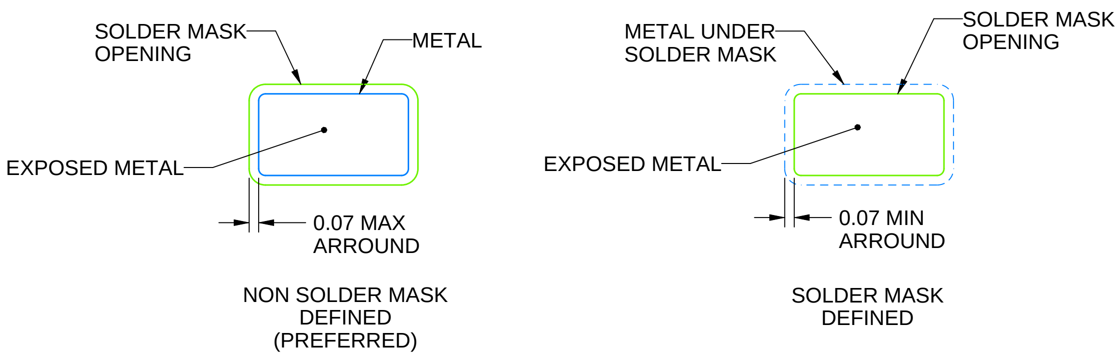
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

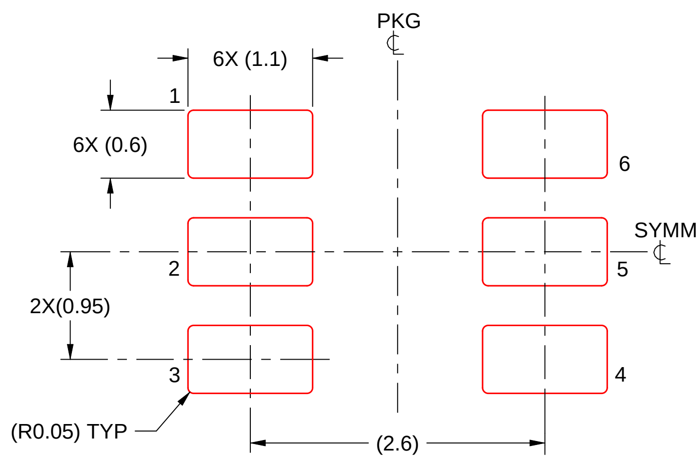


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

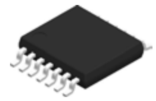


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

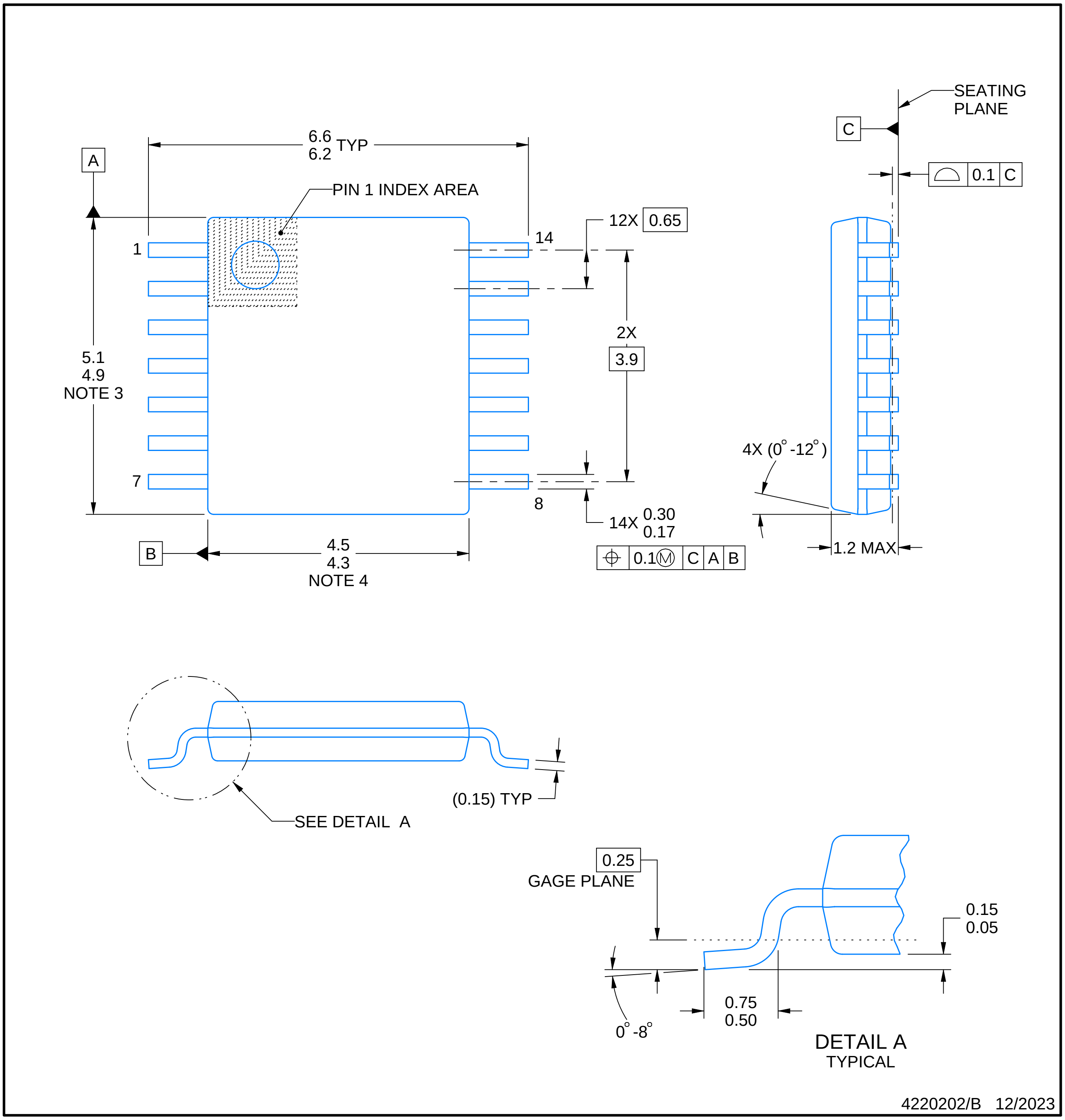


PACKAGE OUTLINE

PW0014A

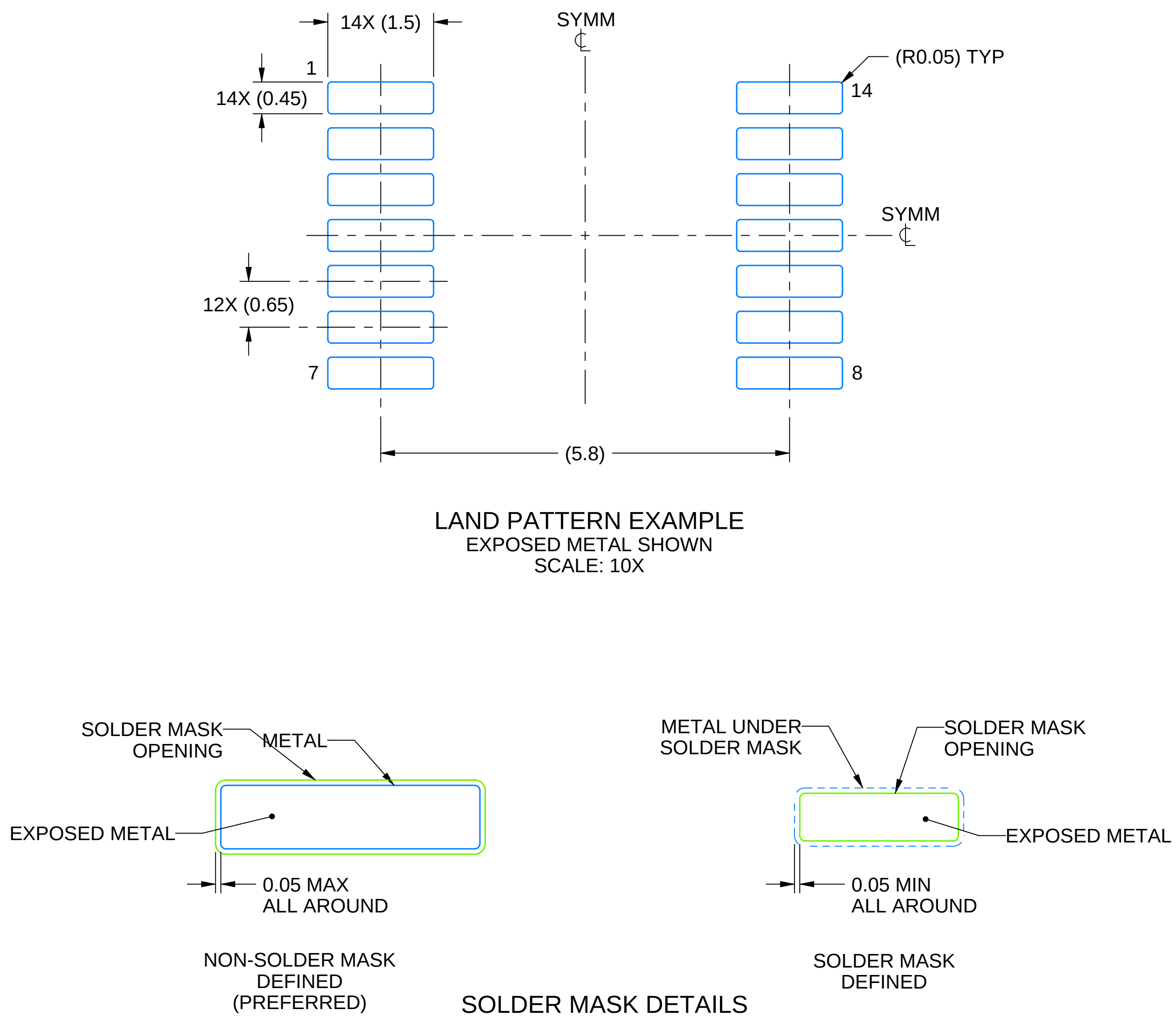
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

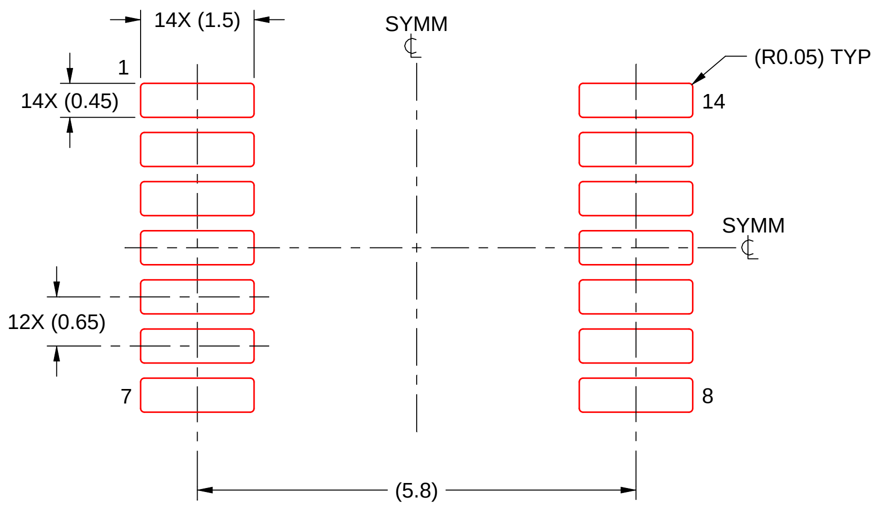
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

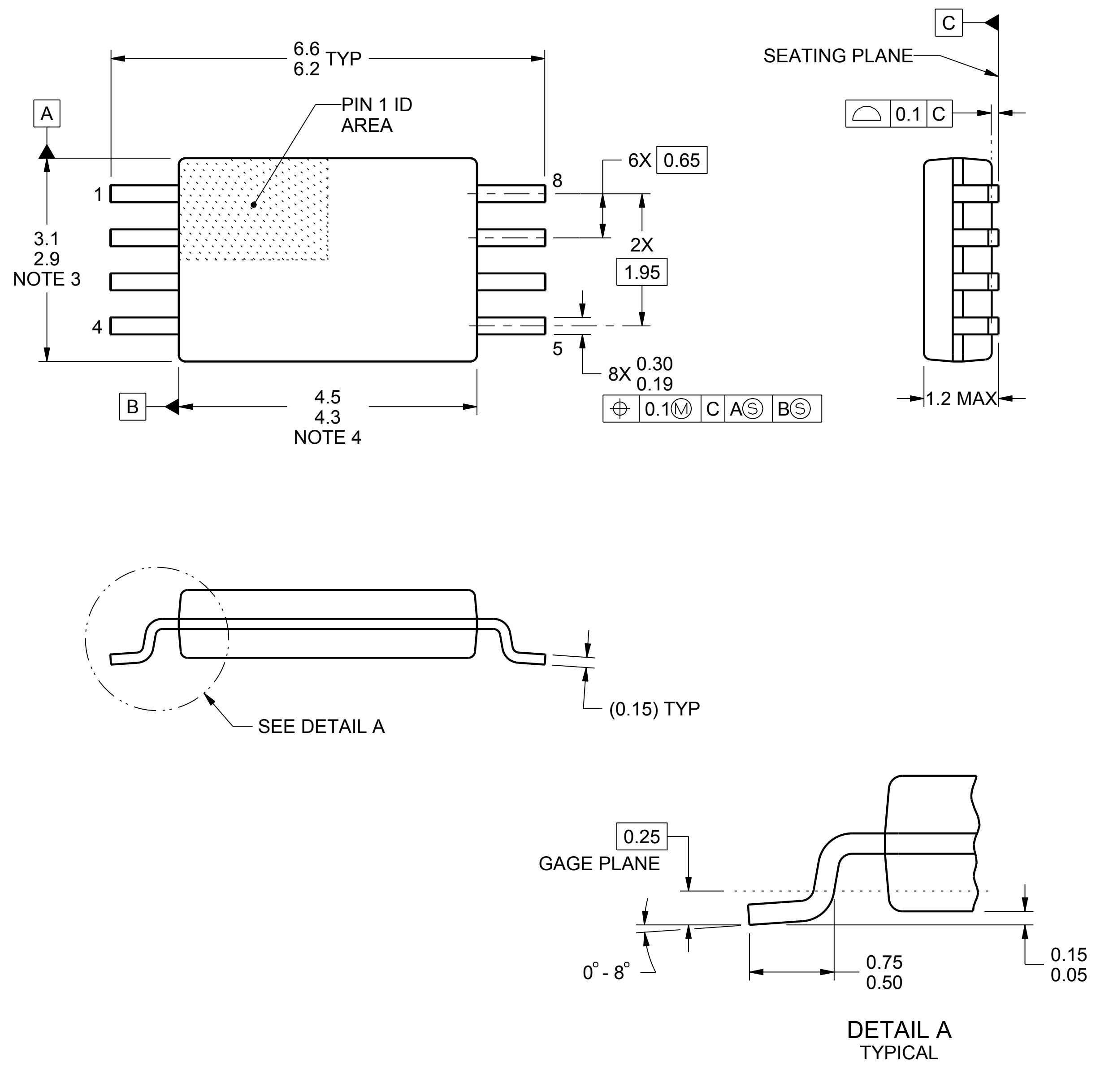


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

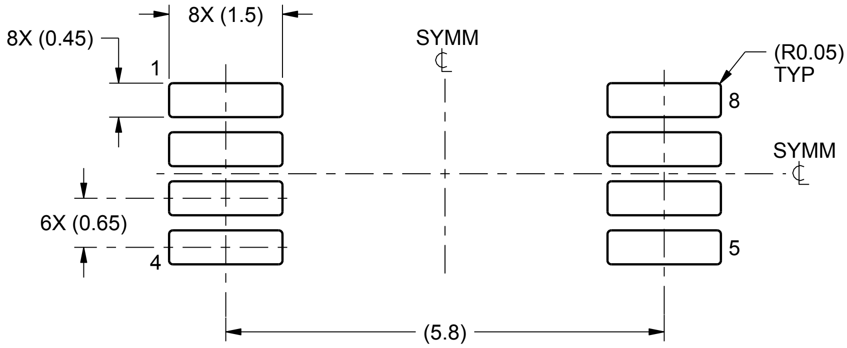
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



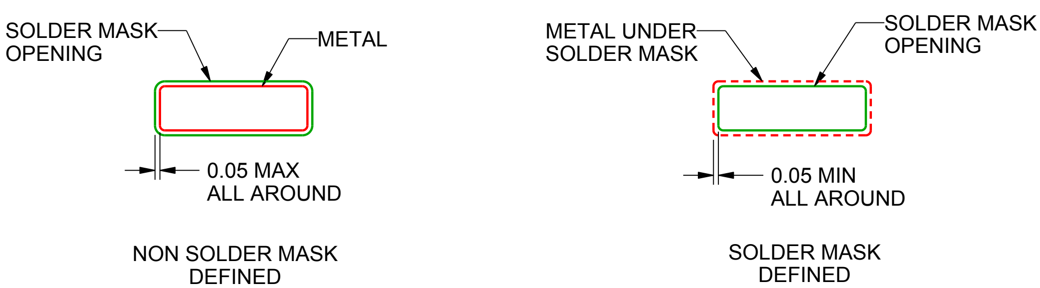
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

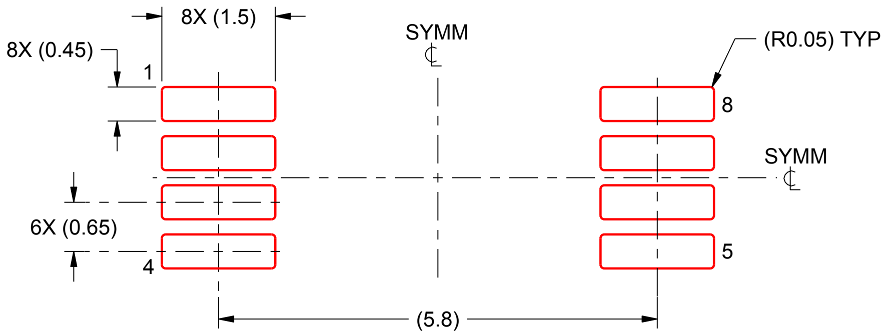


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

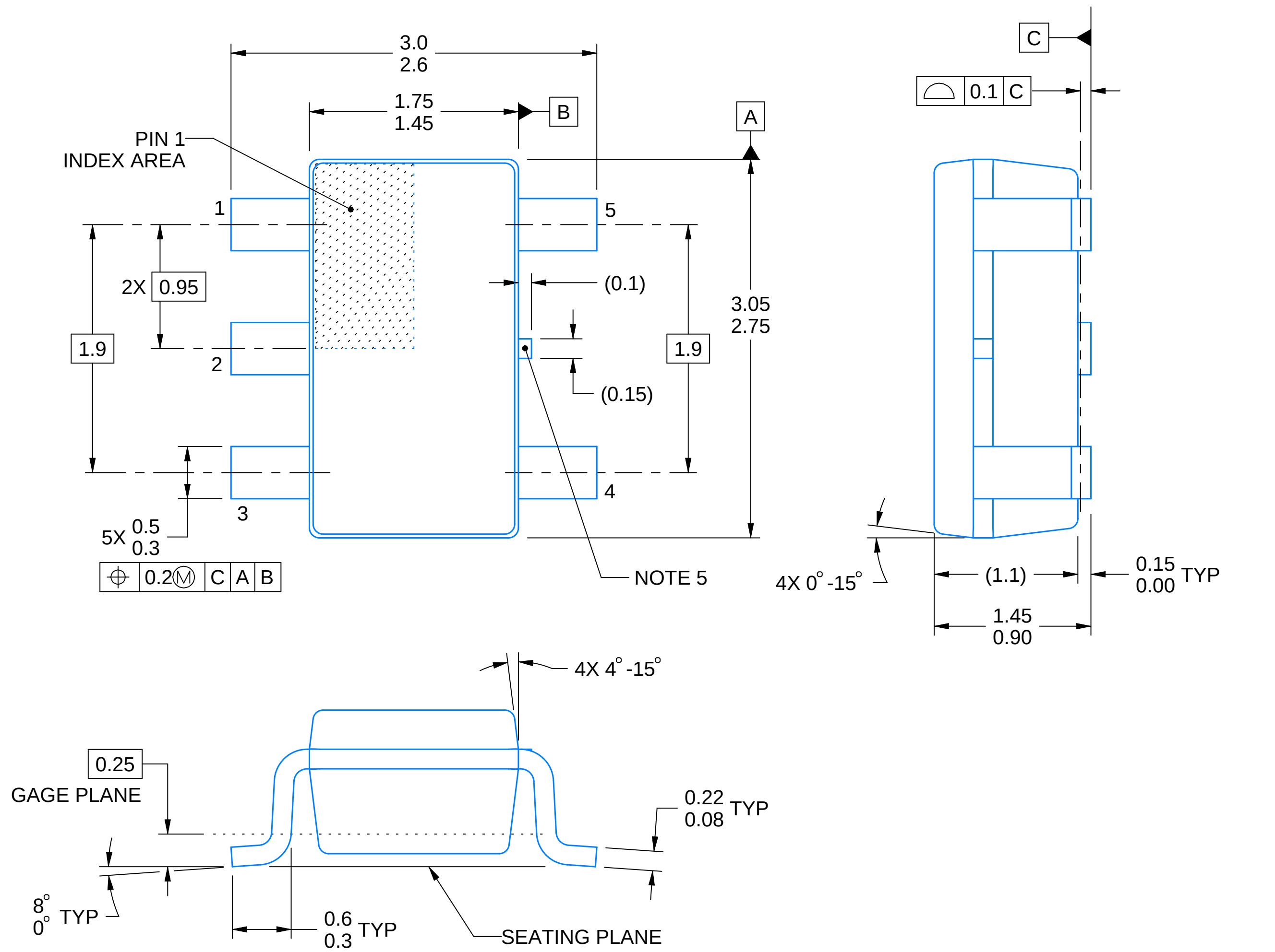


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

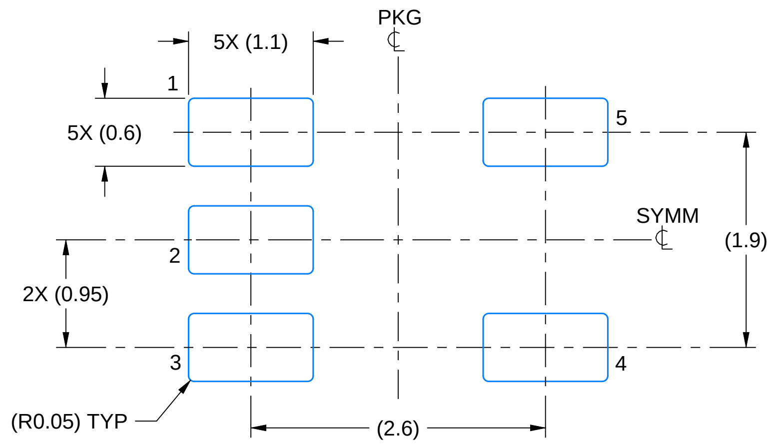
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



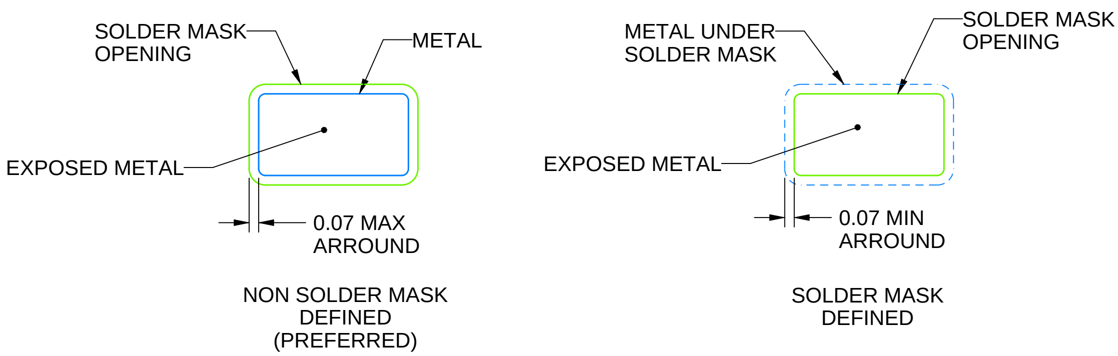
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

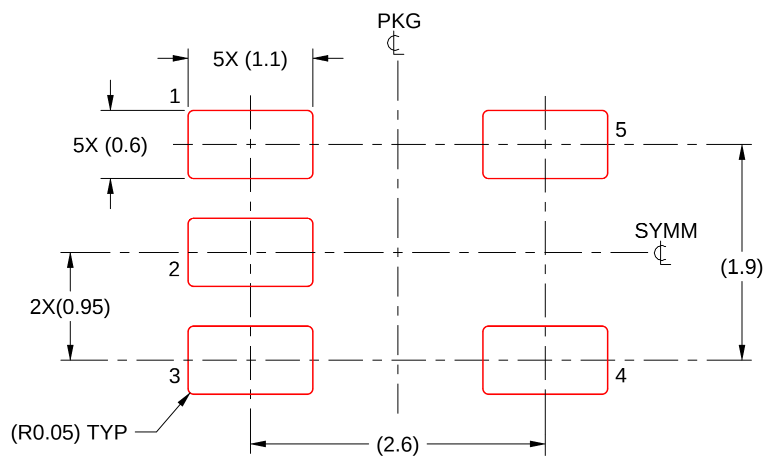


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

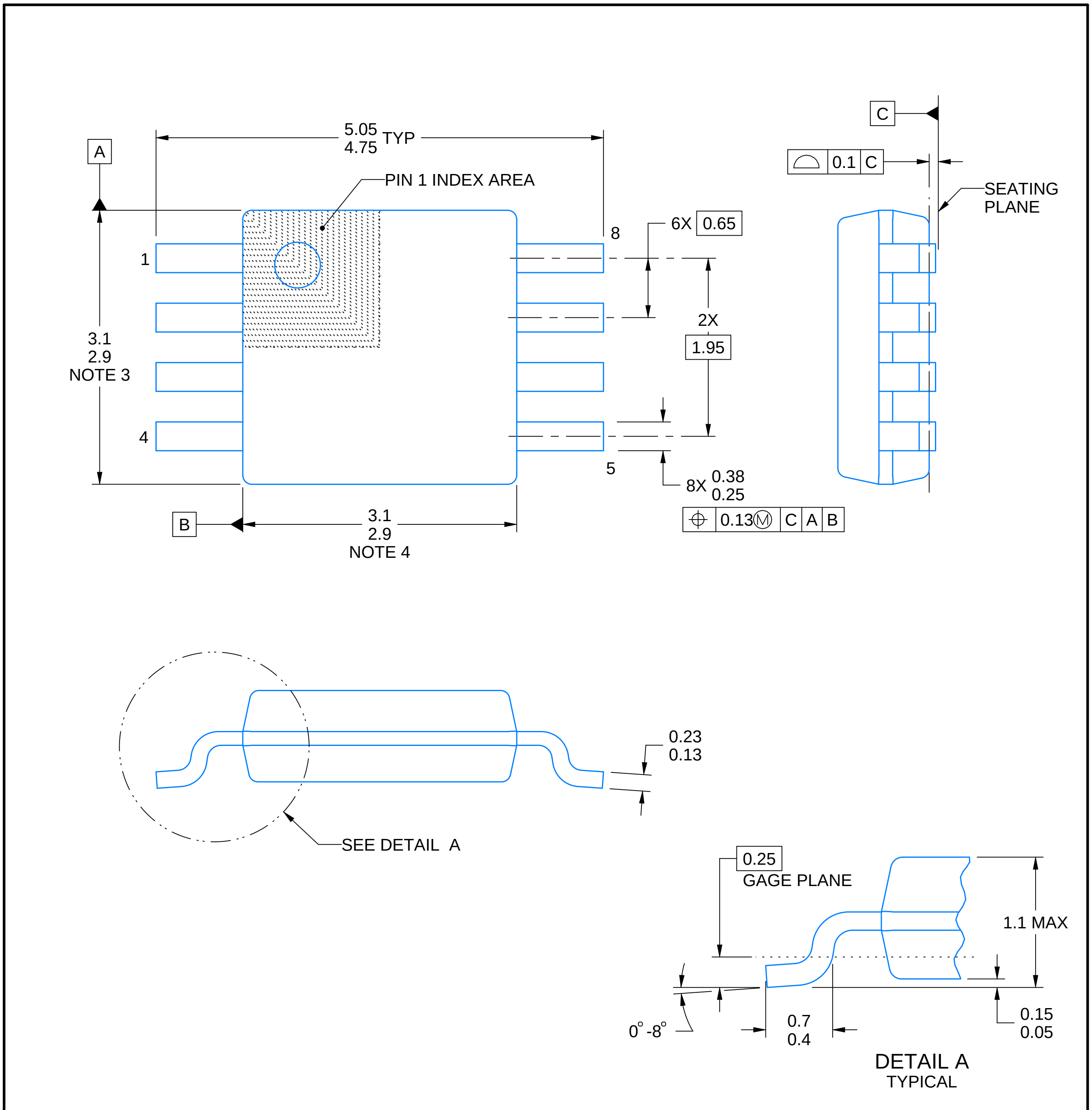


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

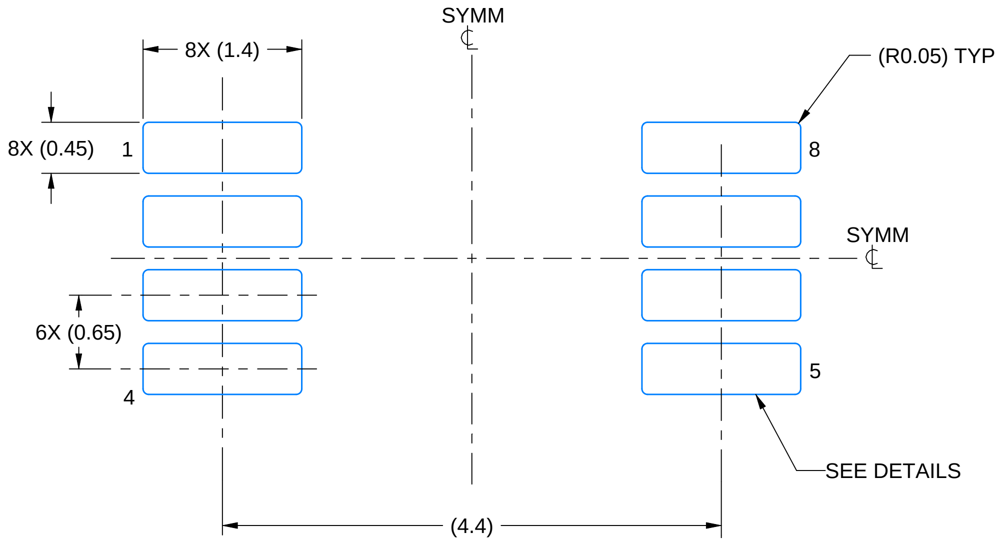


4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK DEFINED (PREFERRED)

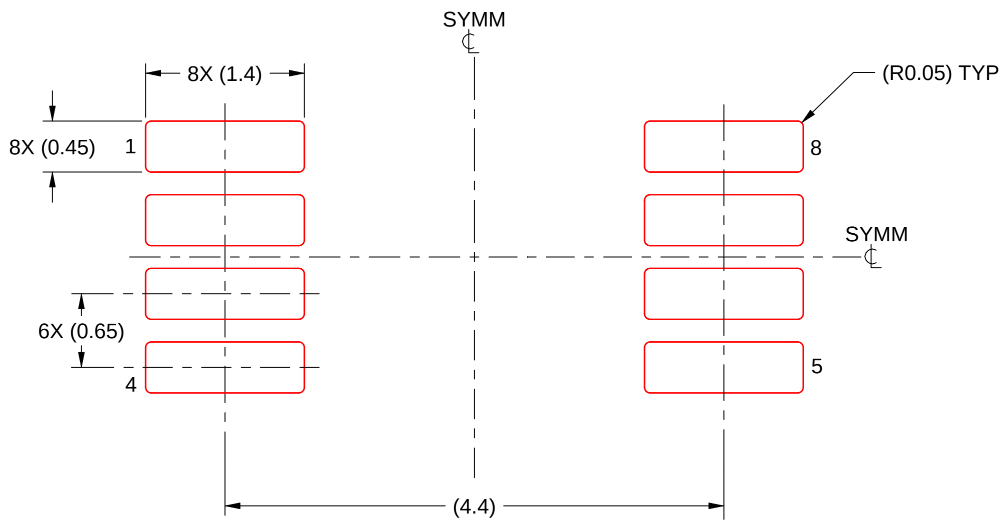
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

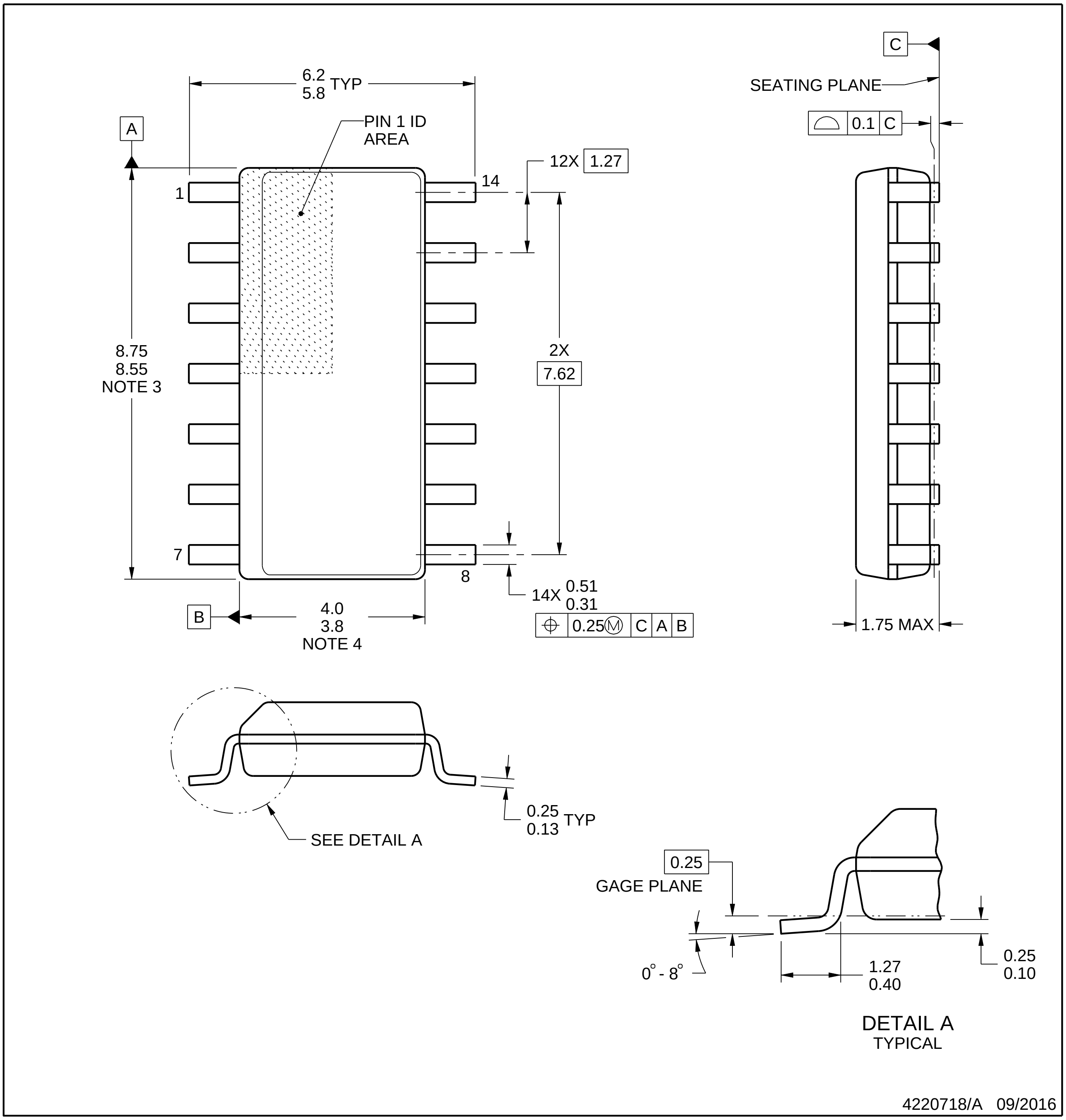


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

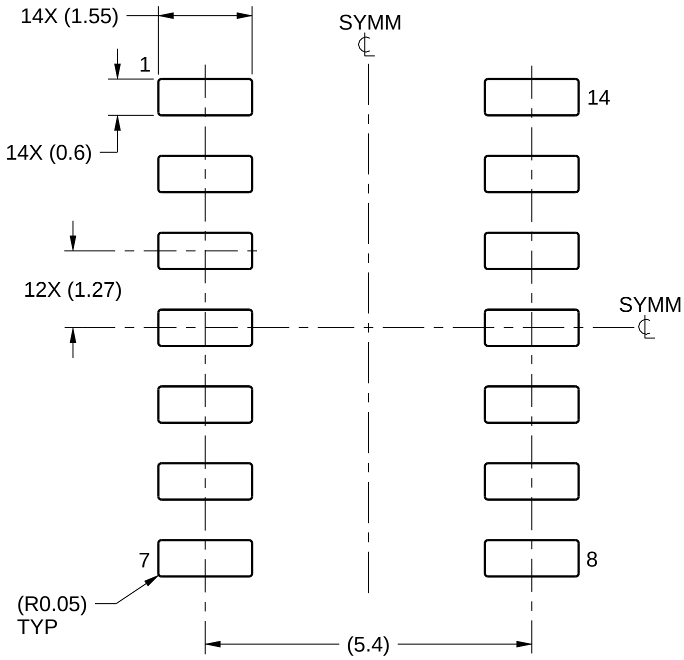
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

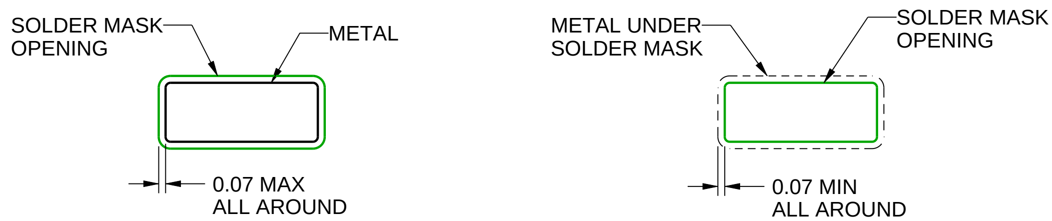


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK DEFINED

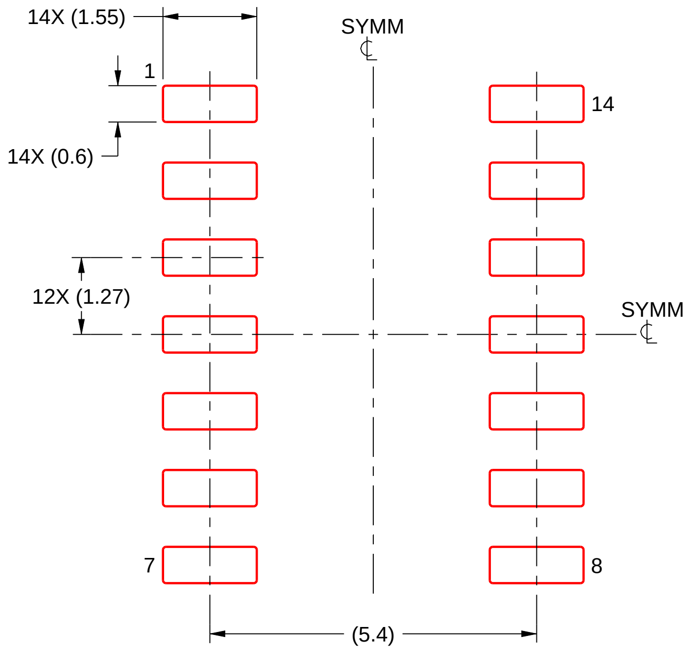
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.