





TLV840-Q1 SNVSBY3A - NOVEMBER 2020 - REVISED APRIL 2021

TLV840-Q1 Nano-Power Voltage Supervisor with Adjustable Reset Time Delay

1 Features

Qualified for automotive applications:

- AEC-Q100 qualified with the following results:
 - Device temperature grade 1: –40°C to +125°C ambient operating temperature
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C7B

Designed for high performance:

- Nano supply current: 120 nA (Typ)
- High accuracy: ±0.5% (Typ)
- Built-in hysteresis (V_{HYS}): 5% (Typ)
- Fixed threshold voltage (V_{IT-}): 0.8 V to 5.4 V

Designed for a wide range of applications:

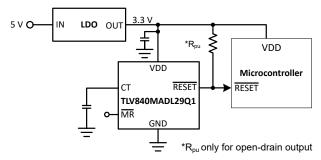
- Operating voltage range: 0.7 V to 6 V
- Fixed (V_{IT-}) voltage: 0.8 V to 5.4 V in 0.1 V steps
- Programmable reset time delay (t_D)
 - Min time delay: 40 µs (typ) without capacitor
- Active-low manual reset (MR)

Multiple output topologies / Package type:

- Four output topologies (RESET / RESET):
 - TLV840MADL-Q1: open-drain, active-low
 - TLV840MAPL-Q1: push-pull, active-low
 - TLV840MADH-Q1: open-drain, active-high
 - TLV840MAPH-Q1: push-pull, active-high
- Package: SOT23-5 (DBV)

2 Applications

- Surround view system, front camera
- Automotive gateway
- Radar ECU
- Automotive head unit
- ADAS controller
- **Emergency call**
- Telematics control unit



Typical Application Circuit

3 Description

The TLV840-Q1 device is a voltage supervisor or reset IC that can operate at wide input voltage levels from 0.7 V to 6 V while maintaining very low quiescent current across the whole VDD and temperature range. TLV840-Q1 offers the best combination of low power consumption, high accuracy and low propagation delay (t_p HI = 30 μ s typical).

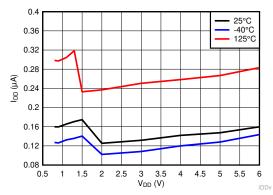
Reset output signal is asserted when the voltage at VDD drops below the negative voltage threshold (V_{IT-}). Reset signal is cleared when VDD rise above V_{IT}- plus hysteresis (V_{HYS}) and the reset time delay (t_D) expires. Reset time delay can be programmed by connecting a capacitor between the CT pin and ground. For a minimum reset delay time the CT pin can be left floating. The TLV840-Q1, with its manual reset pin (MR), offers program flexibility by forcing the system into a hard reset when the pin is asserted.

Additional features: Low power-on reset voltage (V_{POR}), built-in glitch immunity protection for VDD, built-in hysteresis, low open-drain output leakage current (I_{lkg(OD)}). TLV840-Q1 is a perfect voltage monitoring solution for automotive applications and battery-powered / low-power applications.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TLV840-Q1	SOT-23 (5) (DBV)	2.90 mm × 1.60 mm

For package details, see the mechanical drawing addendum at the end of the data sheet.



Typical Supply Current



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4 Revision History

Cł	hanges from Revision * (November 2020) to Revision A (April 2021)	Page
•	RTM release.	

5 Device Comparison

Figure 5-1 shows the device naming nomenclature to compare the different device variants. See Section 12.1 for a more detailed explanation.

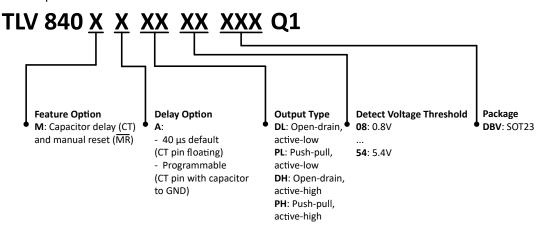


Figure 5-1. Device Naming Nomenclature



6 Pin Configuration and Functions

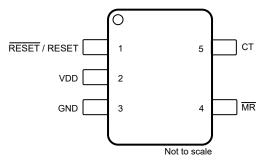


Figure 6-1. Pin Configuration TLV840M-Q1 DBV Package 5-Pin SOT-23 TLV840M-Q1 Top View

Table 6-1. Pin Functions

	Table 0-1.1 III I difficults						
	PIN		1/0	DESCRIPTION			
PIN NO.	TLV840MAxL-Q1	TLV840MAxH-Q1	1/0	DESCRIPTION			
1	RESET	N/A	0	Active-Low Output Reset Signal: This pin is driven logic low when VDD voltage falls below the negative voltage threshold (V_{IT}). RESET remains low (asserted) for the delay time period (t_D) after VDD voltage rises above $V_{IT+} = V_{IT-} + V_{HYS}$.			
1	N/A	RESET	0	Active-High Output Reset Signal: This pin is driven logic high when VDD voltage falls below the negative voltage threshold (V_{IT}). RESET remains high (asserted) for the delay time period (t_D) after VDD voltage rises above V_{IT} + V_{IT} + V_{HYS} .			
2	VDD	VDD	I	Input Supply Voltage: TLV840-Q1 monitors VDD voltage			
3	GND	GND	_	Ground			
4	MR	MR	I	Manual Reset : Pull this pin to a logic low to assert a reset signal in the \overline{RESET} output pin. After \overline{MR} pin is left floating or pulls to logic high, the \overline{RESET} output deasserts to the nominal state after the reset delay time (t _D) expires.			
5	СТ	СТ	-	Capacitor Time Delay Pin: The CT pin offers a user- programmable delay time. Connect an external capacitor on this pin to adjust time delay. When not in use leave pin floating for the smallest fixed time delay.			

Product Folder Links: TLV840-Q1



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD	-0.3	6.5	V
Voltage	CT, MR ⁽²⁾ , RESET (TLV840MAPL), RESET (TLV840MAPH)	-0.3	V _{DD} +0.3 ⁽³⁾	V
	RESET (TLV840MADL)	-0.3	6.5	
Current	RESET, RESET pin	-20	20	mA
Temperature (4)	Operating ambient temperature, T _A	-40	125	°C
Temperature (4)	Storage, T _{stg}	-65	150	C

- (1) Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If the logic signal driving $\overline{\text{MR}}$ is less than VDD, then I_{DD} current increases based on voltage differential.
- (3) The absolute maximum rating is (VDD + 0.3) V or 6.5 V, whichever is smaller
- (4) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

			VALUE	UNIT
V		Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
V(ESD)	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	±750	, '

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
	VDD (TLV840MAxL)	0.7	6	
Voltage	CT, $\overline{\text{RESET}}$ (TLV840MAxL), RESET (TLV840MAPH) , MR	0	6	V
Current	RESET and RESET pin current	-5	5	mA
T _A	Operating ambient temperature	-40	125	°C

7.4 Thermal Information

		TLV840-Q1	
	THERMAL METRIC ⁽¹⁾	DBV (SOT23-5)	UNIT
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.5	°C/W
R ₀ JC(top)	Junction-to-case (top) thermal resistance	117.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.5	°C/W
ΨЈТ	Junction-to-top characterization parameter	43.4	°C/W
ΨЈВ	Junction-to-board characterization parameter	97.8	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



7.5 Electrical Characteristics

At 0.7 V \leq V_{DD} \leq 6 V, CT = \overline{MR} = Open, \overline{RESET} pull-up resistor (R_{pull-up}) = 100 k Ω to VDD, output reset load (C_{LOAD}) = 10 pF and over operating free-air temperature range -40° C to 125°C, unless otherwise noted. VDD ramp rate \leq 100 mV/ μ s. Typical values are at T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
соммо	ON PARAMETERS					
V_{DD}	Input supply voltage	TLV840MAxL	0.7		6	V
\/	Negative-going input threshold accuracy	V _{IT-} = 0.8 V to 1.7 V	-2.5	±0.5	2.5	
V_{IT-}	(1)	V _{IT-} = 1.8 V to 5.4 V	-2	±0.5	2	%
V _{HYS}	Hysteresis on V _{IT} pin		2.5	5	7	%
	County compatints VDD min (2)	V _{DD} = 2 V; V _{IT} = 0.8 V to 1.8 V		0.12	1.0	
I _{DD}	Supply current into VDD pin (2)	V _{DD} = 6 V; V _{IT} = 0.8 V to 5.4 V		0.15	1.2	μA
$V_{\overline{MR}_L}$	Manual reset logic low input (2)				0.3V _{DD}	V
V _{MR_H}	Manual reset logic high input (2)		0.7V _{DD}			V
R _{MR}	Manual reset internal pull-up resistance			100		kΩ
R _{CT}	CT pin internal resistance			500		kΩ
TLV840	MADL (Open-drain active-low)		'		'	
V _{POR}	Power on Reset Voltage (3)	$V_{OL(max)} = 300 \text{ mV}$ $I_{OUT(Sink)} = 15 \mu\text{A}$			700	mV
		$V_{DD} = 0.7 \text{ V}, 0.8 \text{ V} \le V_{IT-} \le 1.5 \text{ V}$ $I_{OUT(Sink)} = 15 \mu\text{A}$			300	
V_{OL}	Low level output voltage	V_{DD} =1.5 V, 1.6 V \leq V _{IT} \leq 3.3 V $I_{OUT(Sink)}$ = 500 μ A			300	mV
		V_{DD} = 3.3 V, 3.4 V \leq V _{IT} \leq 5.5 V $I_{OUT(Sink)}$ = 2 mA			300	
I _{lkg(OD)}	Open-Drain output leakage current	$V_{DD} = V_{PULLUP} = 6V$ $T_A = -40^{\circ}C$ to 85°C		10	100	nA
3(-)		V _{DD} = V _{PULLUP} = 6V		10	350	nA
TLV840	MAPL (Push-pull active-low)					
V _{POR}	Power on Reset Voltage (3)	$V_{OL(max)} = 300 \text{ mV}$ $I_{OUT(Sink)} = 15 \mu\text{A}$			700	mV
		$V_{DD} = 0.7 \text{ V}, 0.8 \text{ V} \le V_{IT-} \le 1.5 \text{ V}$ $I_{OUT(Sink)} = 15 \mu\text{A}$			300	
V_{OL}	Low level output voltage	V_{DD} = 1.5 V, 1.6 V \leq V _{IT} \leq 3.3 V $I_{OUT(Sink)}$ = 500 μ A			300	mV
		V_{DD} = 3.3 V, 3.4 V \leq V _{IT} \leq 5.5 V $I_{OUT(Sink)}$ = 2 mA			300	
		V_{DD} = 1.8 V, 0.8 V \leq V _{IT} \leq 1.4 V $I_{OUT(Source)}$ = 500 μ A	0.8V _{DD}			
V_{OH}	High level output voltage	V_{DD} = 3.3 V, 1.5 V ≤ V_{IT-} ≤ 3.0 V $I_{OUT(Source)}$ = 500 μA	0.8V _{DD}			٧
		$V_{DD} = 6 \text{ V}, 3.1 \text{ V} \le V_{IT-} \le 5.5 \text{ V}$ $I_{OUT(Source)} = 2 \text{ mA}$	0.8V _{DD}			

Product Folder Links: TLV840-Q1

7.5 Electrical Characteristics (continued)

At 0.7 V \leq V_{DD} \leq 6 V, CT = $\overline{\text{MR}}$ = Open, $\overline{\text{RESET}}$ pull-up resistor (R_{pull-up}) = 100 k Ω to VDD, output reset load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40°C to 125°C, unless otherwise noted. VDD ramp rate \leq 100 mV/ μ s. Typical values are at T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TLV840	MAPH (Push-pull active-high)	'	<u> </u>			
V _{POR}	Power on Reset Voltage (3)	$V_{OH(min)} = 0.8V_{DD} V$ $I_{OUT (Source)} = 15 \text{ uA}$			900	mV
V _{OL}	Low level output voltage	$VDD=3.3 V$ 0.8 V ≤ V _{IT-} ≤ 3.0 V $I_{OUT(Sink)} = 500 \mu A$			300	mV
		VDD=6 V 3.1 V \leq V _{IT-} \leq 5.5 V I _{OUT(Sink)} = 2 mA			300	mV
		$VDD = 0.9 V$ 1 V ≤ V _{IT-} ≤ 1.5 V $I_{OUT(Sink)} = 15 μA$	0.8V _{DD}			V
V_{OH}	High level output voltage	VDD=1.5 V 1.6 V \leq V _{IT-} \leq 3.3 V I _{OUT(Sink)} = 500 μA	0.8V _{DD}			V
		VDD=3.3 V 3.4 V \leq V _{IT-} \leq 5.5 V I _{OUT(Sink)} = 2 mA	0.8V _{DD}			V

- (1) V_{IT-} threshold voltage range from 0.8 V to 5.4 V (for DL, PL versions) in 100 mV steps
- (2) If the logic signal driving MR is less than VDD, then IDD current increases based on voltage differential
- (3) V_{POR} is the minimum V_{DD} voltage level for a controlled output state

7.6 Timing Requirements

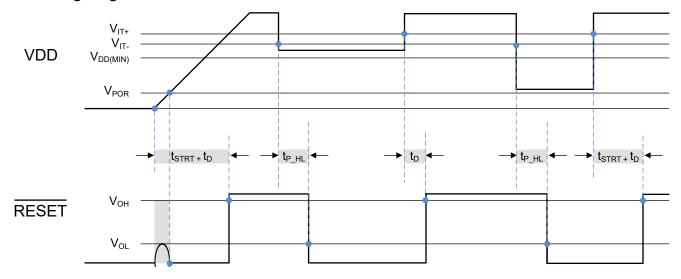
At $0.7~V \le V_{DD} \le 6~V$, $CT = \overline{MR} = Open$, \overline{RESET} pull-up resistor ($R_{pull-up}$) = 100 k Ω to VDD, output reset load (C_{LOAD}) = 10 pF and over operating free-air temperature range $-40^{\circ}C$ to 125 $^{\circ}C$, unless otherwise noted. VDD ramp rate $\le 100~mV/\mu s$. Typical values are at $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{P_HL}	Propagation detect delay for VDD falling below V _{IT} _	V _{DD} : (V _{IT+} + 10%) to (V _{IT-} – 10%)		30	50	μs
		CT pin = Open or NC (V _{IT-} - 10%) to (V _{IT+} + 10%)		40	80	μs
t _D	Reset time delay	CT pin = 10 nF	-	6.2		ms
		CT pin = 1 µF		619		ms
t _{GI_VIT}	Glitch immunity V _{IT} _	5% V _{IT} overdrive ⁽²⁾		10		μs
t _{STRT}	Startup Delay (3)	CT pin = Open or NC			300	μs
t _{MR_PW}	MR pin pulse duration to assert reset (4)			500		ns
t _{MR_RES}	Propagation delay from MR low to reset assertion	$V_{DD} = 3.3 \text{ V},$ $\overline{MR} = V_{\overline{MR}_{-H}} \text{ to } V_{\overline{MR}_{-L}}$		1		μs
t _{MR_tD}	Delay from MR release to reset deassert	$V_{DD} = 3.3 \text{ V},$ $\overline{MR} = V_{\overline{MR}_L} \text{ to } V_{\overline{MR}_H}$		t _D		ms

- (1) $t_{P HL}$ measured from threshold trip point (V_{IT-}) to RESET assert. $V_{IT+} = V_{IT-} + V_{HYS}$
- (2) Overdrive % = $[(V_{DD}/V_{IT-}) 1] \times 100\%$
- (3) When VDD starts from less than the specified minimum V_{DD} and then exceeds V_{IT-}, reset is release after the startup delay (t_{STRT}), a capacitor at CT pin will add t_D delay to t_{STRT} time
- (4) Refer section on Manual Reset Input for min pulse width needed on MR pin

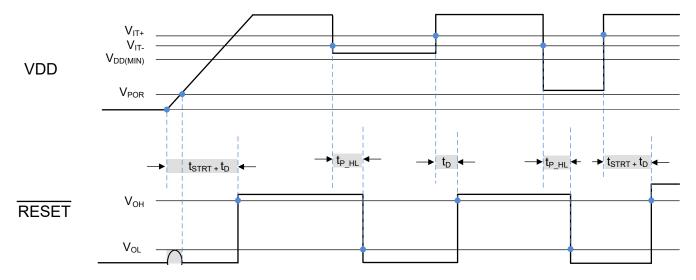


7.7 Timing Diagrams



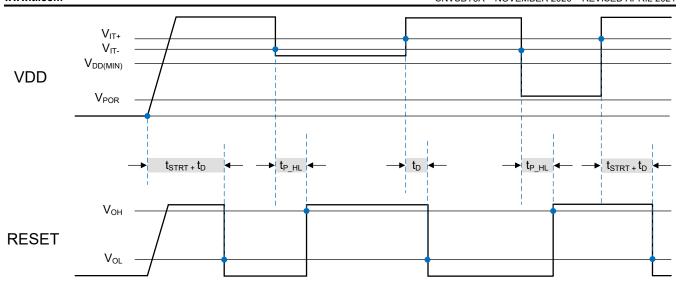
- (1) $t_{D \text{ (no cap)}}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time will be added to the startup time, VDD slew rate = 100 mV / μ s.
- (2) Open-Drain timing diagram where RESET is pulled up to VDD via an external pull-up resistor
- (3) $\overline{\text{RESET}}$ output is undefined when V_{DD} is $< V_{POR}$

Figure 7-1. Timing Diagram TLV840MADL-Q1 (Open-Drain Active-Low)



- (4) $t_{D \text{ (no cap)}}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time will be added to the startup time, VDD slew rate = 100 mV / μ s.
- (5) \overline{RESET} output is undefined when V_{DD} is < V_{POR} and limited to V_{OL} for V_{DD} slew rate = 100 mV / μS

Figure 7-2. Timing Diagram TLV840MAPL-Q1 (Push-Pull Active-Low)



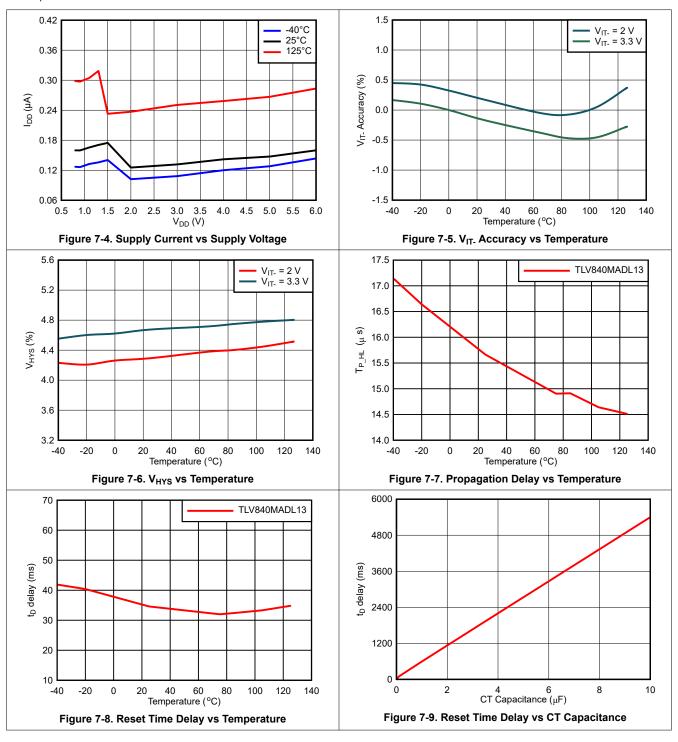
(6) $t_{D \text{ (no cap)}}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time will be added to the startup time, VDD slew rate = 100 mV / μ s.

Figure 7-3. Timing Diagram TLV840MAPH-Q1 (Push-Pull Active-High)



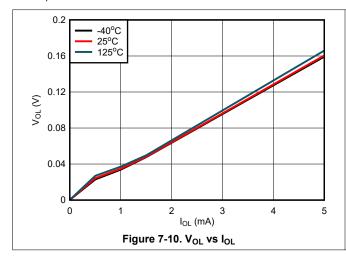
7.8 Typical Characteristics

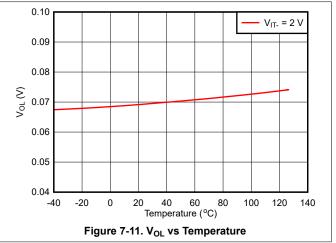
Typical characteristics show the typical performance of the TLV840-Q1 device. Test conditions are T_A = 25°C, VDD = 3.3 V, $R_{Pull-Up}$ = 100 k Ω , C_{LOAD} = 50 pF, unless otherwise noted.



7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TLV840-Q1 device. Test conditions are T_A = 25°C, VDD = 3.3 V, $R_{Pull-Up}$ = 100 k Ω , C_{LOAD} = 50 pF, unless otherwise noted.







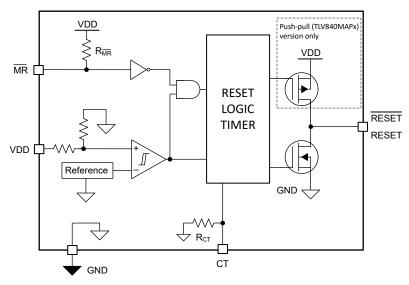
8 Detailed Description

8.1 Overview

The TLV840-Q1 is a family of nano-quiescent current voltage detectors with fixed threshold voltage. TLV840-Q1 features include programable reset time delay using external capacitor, active-low manual reset, 0.5% typical monitor threshold accuracy with hysteresis and glitch immunity.

Fixed negative threshold voltages ($V_{\text{IT-}}$) can be factory set from 0.8 V to 5.4 V. TLV840-Q1 is available in SOT-23 5-pin industry standard package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage (VDD)

VDD pin is monitored by the internal comparator to indicate when VDD falls below the fixed threshold voltage. VDD also functions as the supply for the internal bandgap, internal regulator, state machine, buffers and other control logic blocks. Good design practice involve placing a 0.1 µF to 1 µF bypass capacitor at VDD input for noisy applications to ensure enough charge is available for the device to power up correctly.

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8.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below V_{IT} the output reset is asserted. When the voltage at the VDD pin goes above V_{IT} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

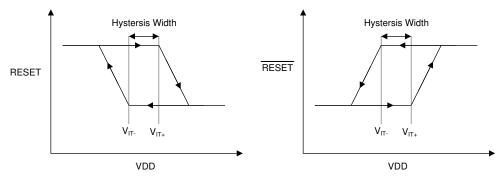


Figure 8-1. Hysteresis Diagram

8.3.1.2 VDD Transient Immunity

The TLV840-Q1 is immune to quick voltage transients or excursion on VDD. Sensitivity to transients depends on both pulse duration (t_{Gl_VIT-}) found in Section 7.6 and overdrive. Overdrive is defined by how much VDD deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 1.

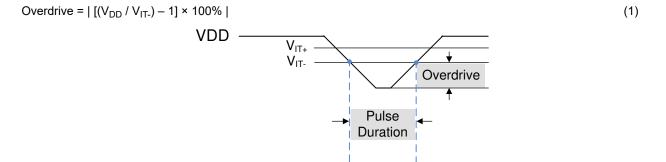


Figure 8-2. Overdrive vs Pulse Duration

8.3.2 User-Programmable Reset Time Delay

The reset time delay can be set to a minimum value of 80 μ s by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 μ F delay capacitor. The reset time delay (t_D) can be programmed by connecting a capacitor no larger than 10 μ F between CT pin and GND.

The relationship between external capacitor (C_{CT}) in μF at CT pin and the time delay (t_D) in seconds is given by Equation 2.

$$t_{D (typ)} = -ln (0.29) \times R_{CT} \times C_{CT} + t_{D (no cap)}$$
 (2)

Equation 3 solves for external capacitor (μF) by plugging R_{CT} and t_D (CT pin = Open) given in Section 7.5 section:

$$C_{CT} = (t_D - 80 \ \mu s) \div 618937$$
 (3)

The reset delay varies according to three variables: the external capacitor (C_{CT}), CT pin internal resistance (R_{CT}) provided in Section 7.5, and a constant. The minimum and maximum variance due to the constant is show in Equation 4 and Equation 5:

$$t_{D \text{ (min)}} = -\ln (0.37) \times R_{CT \text{ (min)}} \times C_{CT \text{ EXT (min)}} + t_{D \text{ (no cap)}}$$
 (4)

$$t_{D (max)} = -ln (0.25) x R_{CT (max)} x C_{CT EXT (max)} + t_{D (no cap)}$$
 (5)

The recommended maximum delay capacitor for the TLV840-Q1 is limited to 10 μ F as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the reset delay will be shorter than expected because the delay capacitor will begin charging from a voltage above zero. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault. The amount of time required to discharge the delay capacitor relative to the reset delay increases as VDD overdrive increases as shown in Figure 8-3. From the graph below, to ensure the CT capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

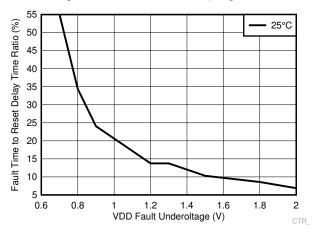


Figure 8-3. C_{CT} Discharge Time During Fault Condition (V_{IT} = 2 V, C_{CT} = 1 μF)

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8.3.3 Manual Reset (MR) Input

The manual reset (\overline{MR}) input allows a processor GPIO or other logic circuits to initiate a reset. A logic low on \overline{MR} with pulse duration longer than $t_{\overline{MR}_PW}$ will cause the reset output to assert. After \overline{MR} returns to a logic high ($V_{\overline{MR}_H}$) and VDD is above $V_{\overline{IT}+}$, reset is deasserted after the user programmed reset time delay (t_D) expires.

The minimum duration for which \overline{MR} is held under $V_{\overline{MR}_L}$ must be at least 1% of $t_{\overline{MR}_tD}$. Otherwise, the effective reset delay will be shorter roughly by the difference between 1% of $t_{\overline{MR}_tD}$ and the actual \overline{MR} pulse width. For large capacitor based delays this difference could be noticeable unless care is taken to lengthen the \overline{MR} pulse width.

 \overline{MR} is internally connected to VDD through a pull-up resistor $R_{\overline{MR}}$ shown in Section 8.2. If the logic signal controlling \overline{MR} is less than VDD, then additional current flows from VDD into \overline{MR} internally. For minimum current consumption, drive \overline{MR} to either VDD or GND. $V_{\overline{MR}}$ should not be higher than VDD voltage.

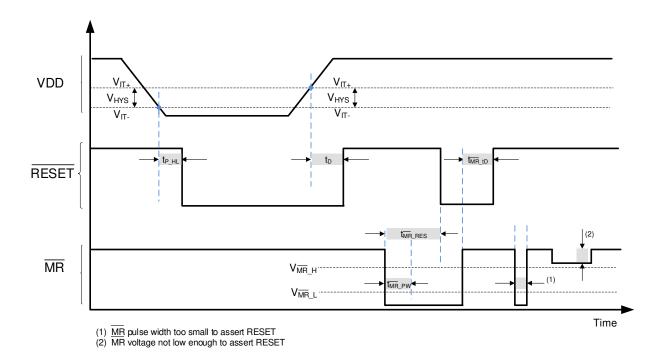


Figure 8-4. Timing Diagram MR and RESET



8.3.4 Output Logic

8.3.4.1 RESET Output, Active-Low

RESET (Active-Low) applies to TLV840DL-Q1 (Open-Drain) and TLV840PL-Q1 (Push-Pull) hence the "L" in the device name. \overline{RESET} remains high (deasserted) as long as VDD is above the negative threshold (V_{IT-}) and the \overline{MR} pin is floating or above V_{MR_H}. If VDD falls below the negative threshold (V_{IT-}) or if \overline{MR} is driven low, then \overline{RESET} is asserted.

When \overline{MR} is again logic high or floating and VDD rise above V_{IT+} , the delay circuit will hold \overline{RESET} low for the specified reset time delay (t_D). When the reset time delay has elapsed, the \overline{RESET} pin goes back to logic high voltage (V_{OH}).

The TLV840**D**L-Q1 (Open-Drain) version, denoted with "**D**" in the device name, requires an external pull-up resistor to hold \overline{RESET} pin high. Connect the external pull-up resistor to the desired pull-up voltage source and \overline{RESET} can be pulled up to any voltage up to 6.5 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The external pull-up resistor value determines the actual V_{OL} , the output capacitive loading, and the output leakage current ($I_{lkq(OD)}$).

The Push-Pull variants (TLV840PL-Q1 and TLV840PH-Q1), denoted with "P" in the device name, does not require an external pull-up resistor.

8.3.4.2 RESET Output, Active-High

RESET (Active-High), denoted with no bar above the pin label, applies to TLV840D**H**-Q1 (Open-Drain) and TLV840P**H**-Q1 push-pull active-high version, hence the "**H**" in the device name. RESET remains low (deasserted) as long as VDD is above the negative threshold (V_{IT}) and the \overline{MR} pin is floating or above $V_{\overline{MR}_H}$. If VDD falls below the negative threshold (V_{IT}) or if \overline{MR} is driven low, then RESET is asserted driving the RESET pin to high voltage (V_{OH}).

When \overline{MR} is again logic high or floating and VDD rise above V_{IT+} the delay circuit will hold RESET high for the specified reset time delay (t_D). When the reset time delay has elapsed, the RESET pin goes back to logic low voltage (V_{OL}).

The TLV840**D**H-Q1 (Open-Drain) version, denoted with "**D**" in the device name, requires an external pull-up resistor to hold RESET pin high. Connect the external pull-up resistor to the desired pull-up voltage source and RESET can be pulled up to any voltage up to 6.5 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The external pull-up resistor value determines the actual V_{OL} , the output capacitive loading, and the output leakage current ($I_{lkq(OD)}$).

The Push-Pull variants (TLV840PL-Q1 and TLV840PH-Q1), denoted with "P" in the device name, does not require an external pull-up resistor.

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8.4 Device Functional Modes

Table 8-1 summarizes the various functional modes of the device. Logic high is represented by "H" and logic low is represented by "L".

Table 8-1. Truth Table

VDD	MR	RESET	RESET
VDD < V _{POR}	Ignored	Undefined	Undefined
V _{POR} < V _{DD} < V _{IT} -	Ignored	Н	L
VDD ≥ V _{IT-}	L	Н	L
VDD ≥ V _{IT-}	Н	L	Н
VDD ≥ V _{IT-}	Floating	L	Н

8.4.1 Normal Operation ($V_{DD} > V_{POR}$)

When VDD is greater than V_{POR} , the reset signal is determined by the voltage on the VDD pin with respect to the trip point (V_{IT-})

- MR high: the reset signal corresponds to VDD with respect to the threshold voltage.
- MR low: in this mode, the reset is asserted regardless of the threshold voltage.

8.4.2 Below Power-On-Reset (V_{DD} < V_{POR})

When the voltage on VDD is lower than V_{POR} , the device does not have enough bias voltage to internally pull the asserted output low or high and reset voltage level is undefined.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

9.2.1 Design 1: Dual Rail Monitoring with Power-up Sequencing

A typical application for the TLV840-Q1 is voltage rail monitoring and power-up sequencing as shown in Figure 9-1. The TLV840-Q1 can be used to monitor any rail above 0.9 V. In this design application, two TLV840-Q1 devices monitor two separate voltage rails and sequences the rails upon power-up. The TLV840MAPL29-Q1 is used to monitor the 3.3-V main power rail and the TLV840MADL10-Q1 is used to monitor the 1.2-V rail provided by the LDO for other system peripherals. The RESET output of the TLV840MAPL29-Q1 is connected to the enable (EN) input of the LDO. A reset event is initiated on either voltage supervisor when the VDD voltage is less than $V_{\text{IT-}}$. For a system-wide reset event, both $\overline{\text{MR}}$ pins are tied to the $\overline{\text{SYS}_{\text{RST}}}$. For the purpose of this application, the design detail on $\overline{\text{MR}}$ are not covered. For more information on the function of $\overline{\text{MR}}$, please see Section 8.3.3

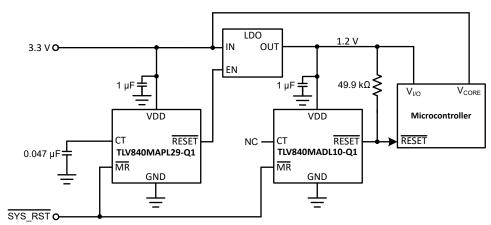


Figure 9-1. TLV840-Q1 Voltage Rail Monitor and Power-Up Sequencer Design Block Diagram

9.2.1.1 Design Requirements

This design requires voltage supervision on two separate rails: 3.3-V and 1.2-V rails. The voltage rail needs to sequence upon power up with the 3.3-V rail coming up first followed by the 1.2-V rail at least 25 ms after.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Two Rail Voltage Supervision	Monitor 3.3-V and 1.2-V rails	Two TLV840-Q1 devices provide voltage monitoring with 1% accuracy with device options available in 0.1 V variations
Voltage Rail Sequencing	Power up the 3.3-V rail first followed by 1.2-V rail 25 ms after	The CT capacitor on TLV840MAPL29-Q1 is set to 0.047 µF for a reset time delay of 29 ms typical
Maximum device current consumption	1 μΑ	Each TLV840-Q1 requires 120 nA typical

9.2.1.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TLV840-Q1 can monitor any voltage between 0.8 V and 5.4 V. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to choose. In this example, the first TLV840-Q1 triggers when the 3.3-V rail falls to 2.9 V. The second TLV840-Q1 triggers a reset when the 1.2-V rail falls to 0.9 V. The secondary constraint for this application is the reset time delay that must be at least 25 ms to allow the microprocessor, and all other devices using the 3.3-V rail, enough time to startup correctly before the 1.2-V rail is enabled via the LDO. Because a minimum time is required, the user must account for capacitor tolerance. For applications with ambient temperatures ranging from -40° C to $+125^{\circ}$ C, C_{CT} can be calculated using R_{CT} and solving for C_{CT} in Equation 2. Solving Equation 2 for 25 ms gives a minimum capacitor value of 0.0403 μ F which is rounded up to a standard value 0.047 μ F to account for capacitor tolerance.

A 1 μF decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the Open-Drain device variants and is calculated to ensure that V_{OL} does not exceed max limit given the Isink possible at the expected supply voltage. In this design example nominal VDD is 1.2 V but dropping to 0.9 V. In Section 7.5, max V_{OL} provides 15 μA I sink for 0.7 V VDD, which is the closest voltage to this design example. Using 15 μA of Isink and 300 mV max V_{OL} , gives us 40 k Ω for the pull-up resistor. Any value higher than 40 k Ω would ensure that V_{OL} will not exceed 300 mV max specification.

9.2.1.3 Application Curves



Figure 9-2. Startup Sequence Highlighting the Delay Between 3.3 V and 1.2 V Rails



9.2.2 Application Curve: Adjusting Output Reset Delay on TLV840EVM

These application curves are taken with the TLV840EVM and they display a change in reset delay time with different capacitor values. The output reset delay time was designed with the ease of programability for the customer. Figure 9-3 displays an output reset delay time of 57.6 µs with no capacitor on the CT pin. Figure 9-4 and Figure 9-5 have output reset delay times of 5.42 ms and 56.8 ms, respectively. Both the output delay times and capacitors used resulted in an order of magnitude difference. Please see the *TLV840EVM User Guide* for more information.

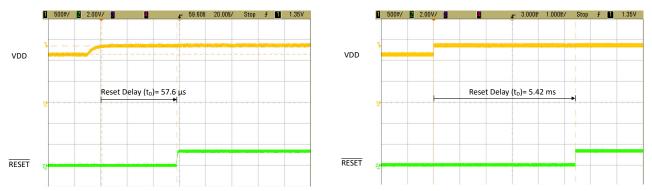


Figure 9-3. TLV840EVM RESET Time Delay (t_D) with Figure 9-4. TLV840EVM RESET Time Delay (t_D) with No Capacitor 0.01-µF Capacitor



Figure 9-5. TLV840EVM RESET Time Delay (t_D) with 0.1-µF Capacitor

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10 Power Supply Recommendations

The TLV840 is designed to operate from an input supply with a voltage range between 0.7 V and 6 V. TI recommends an input supply capacitor between the VDD pin and GND pin. This device has a 6.5 V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 6.5 V, additional precautions must be taken.



11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a minimum $0.1~\mu F$ ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the rest time delay is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a > 0.1 μF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CT} capacitor is used, place these components as close as possible to the CT pin. If the CT pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin to < 5 pF.
- Place the pull-up resistors on RESET pin as close to the pin as possible.

11.2 Layout Example

The layout example in shows how the TLV840DL-Q1 is laid out on a printed circuit board (PCB) with a user-defined delay.

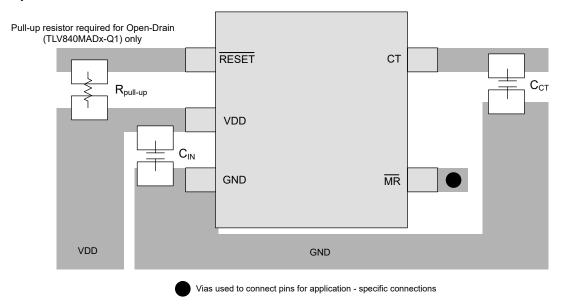


Figure 11-1. TLV840M-Q1 Recommended Layout

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12 Device and Documentation Support

12.1 Device Nomenclature

Table 12-1 shows how to decode the function of the device based on its part number

Table 12-1. Device Naming Convention

DESCRIPTION	NOMENCLATURE	VALUE				
Generic Part number	TLV840	TLV840				
Feature Option	M 1 Manual Reset option in addition to CT pin					
Delay Option	A 40 µs (Default internal reset time delay)					
Variant code (Output Topology)	DL	Open-Drain, Active-Low				
	PL	Push-Pull, Active-Low				
	DH	Open-Drain, Active-High				
	PH	Push-Pull, Active-High				
Detect Voltage Option	## (two characters)	Example: 12 stands for 1.2 V threshold				
Package	DBV	SOT23-5				
Reel	R	Large Reel				
Automotive Version	Q1	AEC-Q100				

1. Orderable part numbers with TLV840M-Q1 are only available with the delay option A. However, longer delays can be achieved through an external capacitor on the CT pin. Leaving the CT pin floating will result in typical 40 µs delay feature option.



12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

12.4 Trademarks

All trademarks are the property of their respective owners.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: TLV840-Q1

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TLV840MADL12DBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2HNF
TLV840MADL12DBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HNF
TLV840MADL12DBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HNF
TLV840MADL22DBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2HOF
TLV840MADL22DBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HOF
TLV840MADL22DBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HOF
TLV840MADL29DBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	3OZF
TLV840MADL29DBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3OZF
TLV840MADL30DBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2HPF
TLV840MADL30DBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2HPF
TLV840MADL30DBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2HPF
TLV840MADL31DBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HMF
TLV840MADL31DBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HMF
TLV840MADL32DBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2HQF
TLV840MADL32DBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HQF
TLV840MADL32DBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HQF
TLV840MADL40DBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2HDF
TLV840MADL40DBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HDF
TLV840MADL40DBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HDF
TLV840MAPH29DBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2INF
TLV840MAPH29DBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2INF
TLV840MAPH29DBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2INF
TLV840MAPL36DBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2HVF
TLV840MAPL36DBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HVF
TLV840MAPL36DBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HVF

⁽¹⁾ Status: For more details on status, see our product life cycle.

PACKAGE OPTION ADDENDUM

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(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLV840-Q1:

Catalog: TLV840

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV840MADL12DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MADL22DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MADL29DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MADL30DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MADL31DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MADL32DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MADL40DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MAPH29DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MAPL36DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MAPL36DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3



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*All dimensions are nominal

7 til dilliciololio ale nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV840MADL12DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MADL22DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MADL29DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MADL30DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MADL31DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MADL32DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MADL40DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MAPH29DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MAPL36DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MAPL36DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0



SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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