TLV7A03 Nanopower, 250nA I_Q, 200mA I_{OUT}, Low-Dropout Regulator With Fast Transient Response

1 Features

- Ultra-low I_Q: 250nA (typ), 400nA (max)
- Shutdown I_Q: 3nA (typ)
- Excellent transient response (1mA to 50mA)
  - < 10µs settling time
  - 80mV undershoot
- Packages:
  - 1.0mm × 1.0mm X2SON
  - SOT23-5
- Input voltage range: 1.5V to 6.0V
- Output voltage range: 0.8V to 5.0V (fixed)
- Output accuracy: 1.5% over temperature
- Smart enable pulldown
- Very low dropout:
  - 270mV (max) at 200mA (V_{OUT} = 3.3V)
- Stable with a 1µF or larger capacitor

2 Applications

- Wearables electronics
- Thermostats, smoke and heat detectors
- Gas, heat, and water meters
- Blood glucose monitors and pulse oximeters
- Residential circuit breakers and fault indicators
- Building security and video surveillance devices
- EPOS card readers

3 Description

The TLV7A03 is an ultra-small, ultra-low quiescent current low-dropout linear regulator (LDO) that sources 200mA with excellent transient performance.

The TLV7A03, with an ultra-low I_Q of 250nA, is designed specifically for applications where very low quiescent current is a critical parameter. This device maintains low I_Q consumption even in dropout mode to further increase battery life. When in shutdown or disabled mode, the device consumes only 3nA I_Q, which helps increase battery shelf life. The TLV7A03 has an output range of 0.8V to 5.0V, available in 50mV steps, to support the lower core voltages of modern microcontrollers (MCUs).

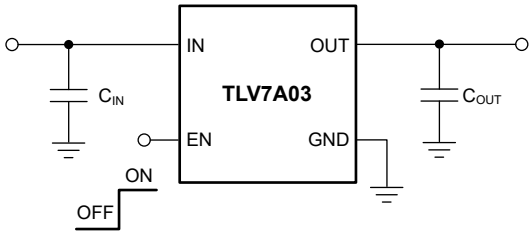
The TLV7A03 features a smart enable circuit with an internally controlled pulldown resistor that keeps the LDO disabled even when the EN pin is floating. This circuit also helps minimize the external components used to pulldown the EN pin. This circuit also helps minimize the current drawn through the external pulldown circuit when the device is enabled.

The TLV7A03 is fully specified for T_J = –40°C to +125°C operation.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLV7A03	DQN (X2SON, 4)	1mm × 1mm
	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

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4 Pin Configuration and Functions

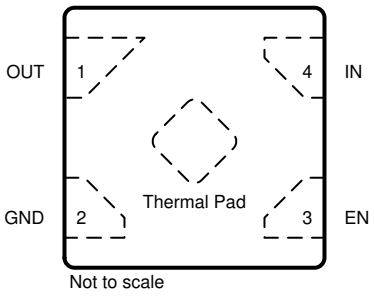


Figure 4-1. DQN Package, 1mm × 1mm, 4-Pin X2SON (Top View)

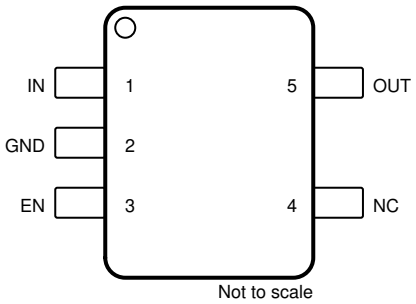


Figure 4-2. DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions: DQN, DBV

PIN			TYPE	DESCRIPTION
NAME[1]	DQN	DBV		
EN	3	3	Input	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low or floating this pin disables the device. This pin features an internal pulldown resistor, which is disconnected when EN is driven high externally and the device has started up.
GND	2	2	—	Ground pin. Connect this pin to ground on the board.
IN	4	1	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground. See the *Recommended Operating Conditions* table. Place the input capacitor as close to the input of the device as possible.
NC	—	4	—	No connect pin. This pin is not internally connected. Connect to ground or leave floating.
OUT	1	5	Output	Regulated output pin. A 0.5µF or greater effective capacitance is required from OUT to ground for stability. For best transient response, use a 1µF or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible; see the *Recommended Operating Conditions* table.
Thermal pad		—	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to ground.

(1) NC = No internal connection.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6.5	V
	V_{EN}	–0.3	6.5	
	V_{OUT}	–0.3	V_{IN} + 0.3 or 5.5(2)	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum is V_{IN} + 0.3 V or 5.5 V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.5		6.0	V
V_{EN}	Enable voltage	0		6.0	V
V_{OUT}	Output voltage	0.8		5.0	V
I_{OUT}	Output current	0		200	mA
C_{IN}	Input capacitor		1		µF
C_{OUT}	Output capacitor(1) (2)	1	1	22	µF
F_{EN}	EN toggle frequency			10	kHz
T_J	Operating junction temperature	–40		125	°C

(1) Effective output capacitance of 0.5 µF minimum required for stability.
(2) 22 µF is the maximum derated capacitance that can be used for stability.

5.4 Thermal Information

THERMAL METRIC(1)		TLV7A03		UNIT
		DQN (X2SON)	DBV (SOT-23-5)	
		4 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	179.1	181.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	137.6	53.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	116.3	88.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	27.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	116.3	52.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	112.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

Specified at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Nominal accuracy	T_J = 25°C, V_{OUT} ≥ 1.5V, 1µA[3] ≤ I_{OUT} ≤ 1mA		–1		1	%
		T_J = 25°C; V_{OUT} < 1.5V		–15		15	mV
	Accuracy over temperature	V_{OUT} ≥ 1.5V	T_J = –40°C to +125°C	–1.5		1.5	%
		V_{OUT} < 1.5V		–20		20	mV
$\Delta V_{OUT}(\Delta V_{IN})$	Line regulation	$V_{OUT(nom)}$ + 0.5V ≤ V_{IN} ≤ 6.0V[1]	T_J = –40°C to +125°C			5	mV
$\Delta V_{OUT}(\Delta I_{OUT})$	Load regulation[2]	1mA ≤ I_{OUT} ≤ 200mA, V_{IN} = $V_{OUT(nom)}$ + 0.5V[1]	T_J = –40°C to +85°C		20	38	mV
			T_J = –40°C to +125°C			50	
I_{GND}	Ground current	I_{OUT} = 0mA	T_J = 25°C		250	300	nA
			T_J = –40°C to +85°C			400	
I_{GND}/I_{OUT}	Ground current vs load current	20µA ≤ I_{OUT} < 1mA	T_J = 25°C		1		%
		1mA ≤ I_{OUT} ≤ 100mA			0.25		
		I_{OUT} ≥ 100mA			0.15		
$I_{GND(DO)}$	Ground current in dropout[3]	I_{OUT} = 0mA, V_{IN} = 95% x $V_{OUT\ (NOM)}$	T_J = 25°C		270		nA
I_{SHDN}	Shutdown current	V_{EN} = 0V, 1.5V ≤ V_{IN} ≤ 5.0V, T_J = 25°C			3	10	nA
I_{CL}	Output current limit	V_{OUT} = 90% × $V_{OUT(nom)}$	V_{OUT} < 2.5V, V_{IN} = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 1.0 V	240	450	750	mA
			V_{OUT} ≥ 2.5V, V_{IN} = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 0.5 V	240	450	750	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0V			65		mA
V_{DO}	Dropout voltage[4]	T_J = –40°C to +85°C	0.8V ≤ V_{OUT} < 1.0V			1050	mV
			1.0V ≤ V_{OUT} < 1.2V			790	
			1.2V ≤ V_{OUT} < 1.5V			650	
			1.5V ≤ V_{OUT} < 1.8V			490	
			1.8V ≤ V_{OUT} < 2.5V			400	
			2.5V ≤ V_{OUT} < 3.3V			310	
			3.3V ≤ V_{OUT} ≤ 5.0V			270	
		T_J = –40°C to +125°C	0.8V ≤ V_{OUT} < 1.0V			1100	
			1.0V ≤ V_{OUT} < 1.2V			850	
			1.2V ≤ V_{OUT} < 1.5V			700	
			1.5V ≤ V_{OUT} < 1.8V			560	
			1.8V ≤ V_{OUT} < 2.5V			450	
			2.5V ≤ V_{OUT} < 3.3V			360	
			3.3V ≤ V_{OUT} ≤ 5.0V			310	
PSRR	Power-supply rejection ratio	f = 1kHz, I_{OUT} = 30mA			55		dB
V_N	Output voltage noise	BW = 10Hz to 100kHz, V_{OUT} = 0.8V, I_{OUT} = 30mA			130		μV_{RMS}
V_{UVLO}	UVLO threshold	V_{IN} rising		1.23	1.3	1.47	V
		V_{IN} falling		1.0	1.12	1.41	
$V_{UVLO(HYST)}$	UVLO hysteresis	V_{IN} hysteresis			180		mV

5.5 Electrical Characteristics (continued)

Specified at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{EN(HI)}$	EN pin logic high voltage		1.1			V
$V_{EN(LOW)}$	EN pin logic low voltage				0.3	V
I_{EN}	EN pin leakage current	V_{EN} = V_{IN} = 6.0V		10		nA
$R_{EN(PULLDOWN)}$	Smart enable pulldown resistor	V_{EN} = 0.3V		500		KΩ
$R_{PULLDOWN}$	Pulldown resistor	V_{IN} = 3.3V, device disabled		60		Ω
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing		145		

(1) V_{IN} = 2.0V for V_{OUT} ≤ 1.5V.
(2) Load Regulation is normalized to the output voltage at I_{OUT} = 1mA.
(3) Specified by design
(4) Dropout is measured by ramping V_{IN} down until V_{OUT} = $V_{OUT\ (nom)}$ x 95%, with I_{OUT} = 200mA.

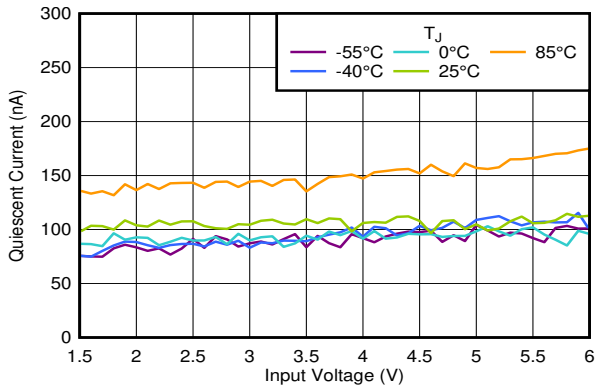
5.6 Switching Characteristics

Specified at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{STR}	Start-up time	From EN assertion to V_{OUT} = 90% × $V_{OUT(nom)}$	0.8V ≤ V_{OUT} ≤ 1.5V		500	800	µs
			1.5V < V_{OUT} ≤ 3.0V		750	1200	
			3.0V < V_{OUT} ≤ 5.0V		1200	1600	

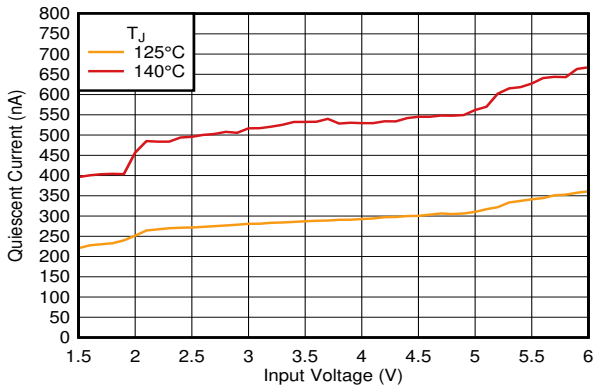
5.7 Typical Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



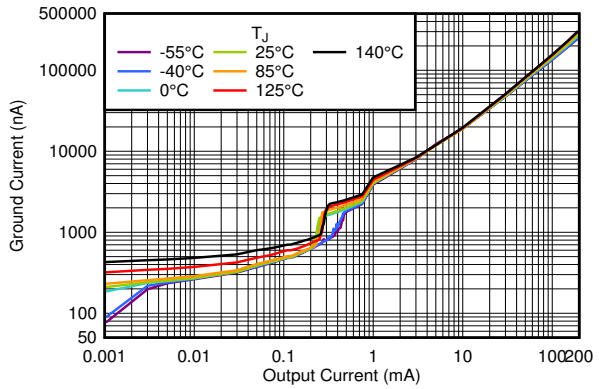
V_{OUT} = 1.8V, V_{IN} = V_{EN} = 2.3V

Figure 5-1. I_Q vs V_{IN} and Temperature



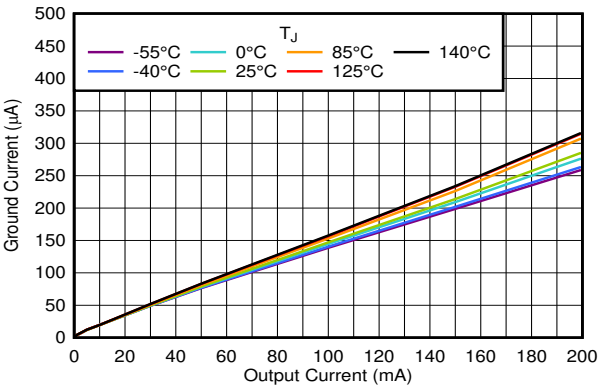
I_{OUT} = 0mA, V_{EN} = V_{IN}

Figure 5-2. I_Q vs V_{IN} and Temperature



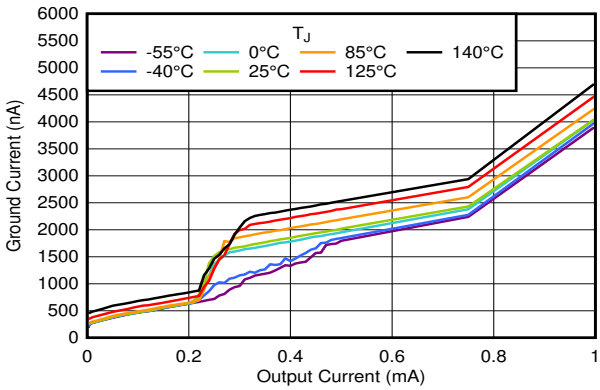
V_{OUT} = 1.8V, V_{IN} = V_{EN} = 2.3V

Figure 5-3. I_Q vs I_{OUT} and Temperature Up to 200mA



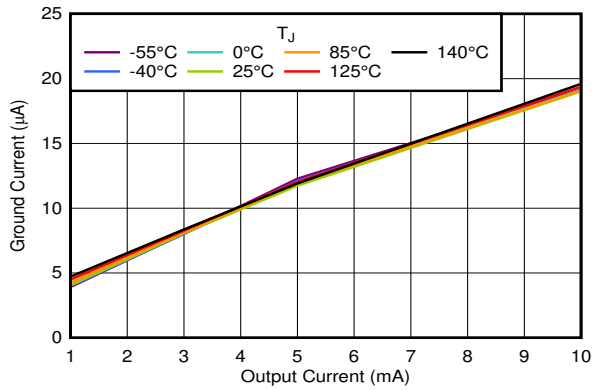
V_{OUT} = 1.8V, V_{IN} = V_{EN} = 2.3V

Figure 5-4. I_Q vs I_{OUT} and Temperature Up to 200mA



V_{OUT} = 1.8V, V_{IN} = V_{EN} = 2.3V

Figure 5-5. I_Q vs I_{OUT} and Temperature Up to 1mA

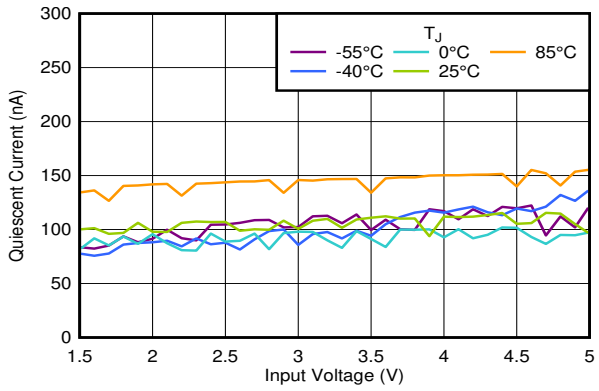


V_{OUT} = 1.8V, V_{IN} = V_{EN} = 2.3V

Figure 5-6. I_Q vs I_{OUT} and Temperature for 1mA to 10mA

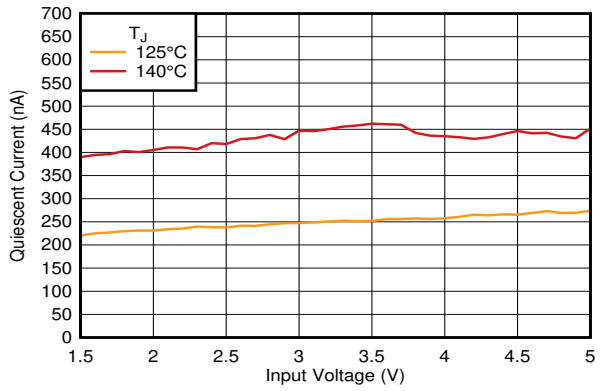
5.7 Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



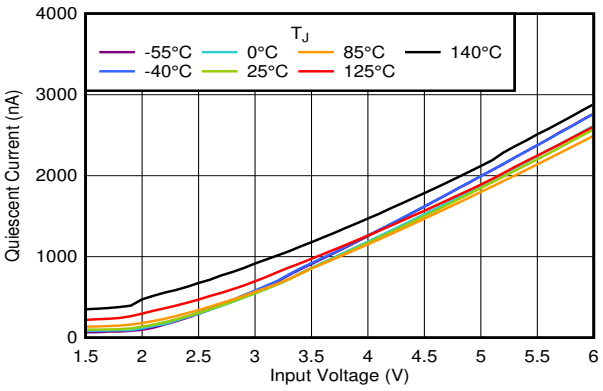
V_{OUT} = 5.0V, V_{IN} = V_{EN}

Figure 5-7. I_Q in Dropout vs V_{IN} and Temperature



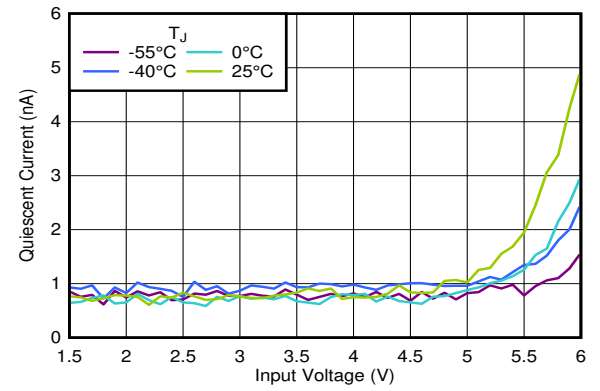
V_{OUT} = 5.0V, V_{IN} = V_{EN}

Figure 5-8. I_Q in Dropout vs V_{IN} and Temperature



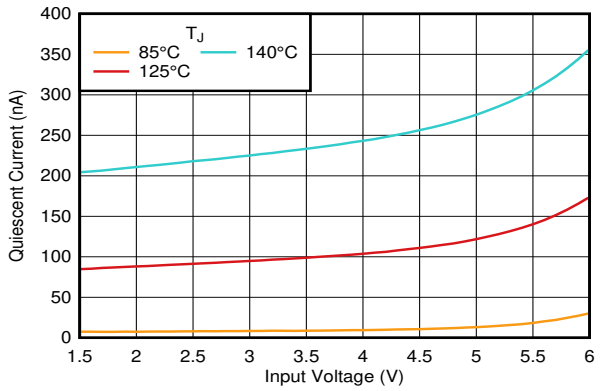
I_{OUT} = 0mA, V_{EN} = 1.1V

Figure 5-9. I_Q vs V_{IN} and Temperature



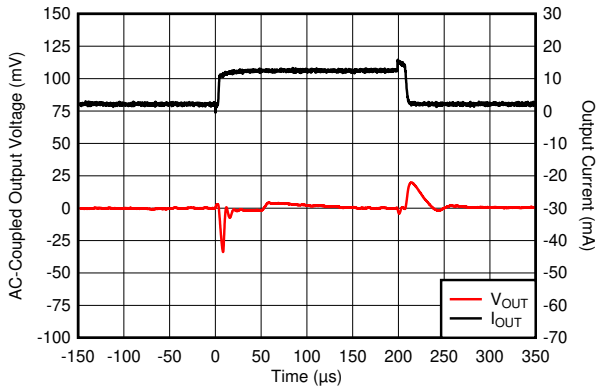
V_{EN} = 0V

Figure 5-10. I_{SHDN} vs V_{IN} and Temperature



V_{EN} = 0V

Figure 5-11. I_{SHDN} vs V_{IN} and Temperature

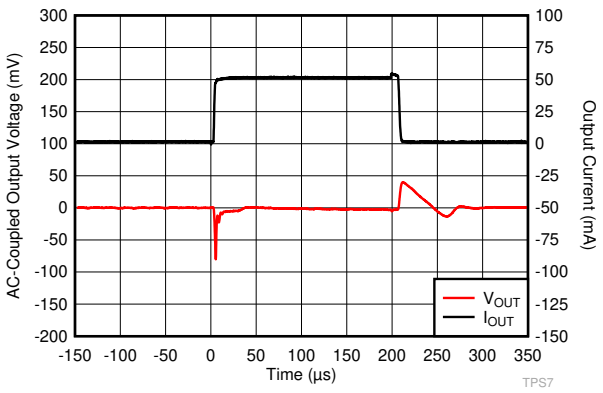


V_{OUT} = 1.8V, V_{IN} = 2.8V, C_{OUT} = 1µF, t_r = t_f = 1µs

Figure 5-12. I_{OUT} Transient From 1mA to 10mA

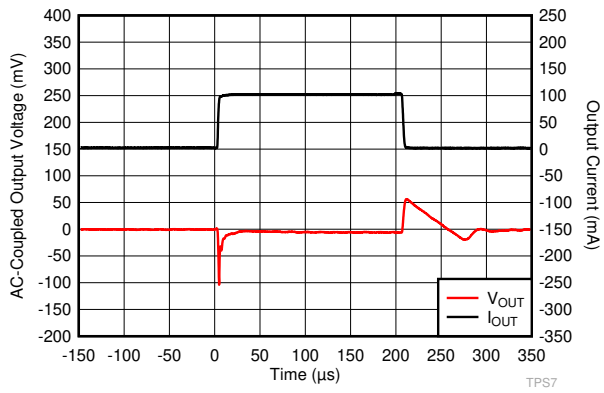
5.7 Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



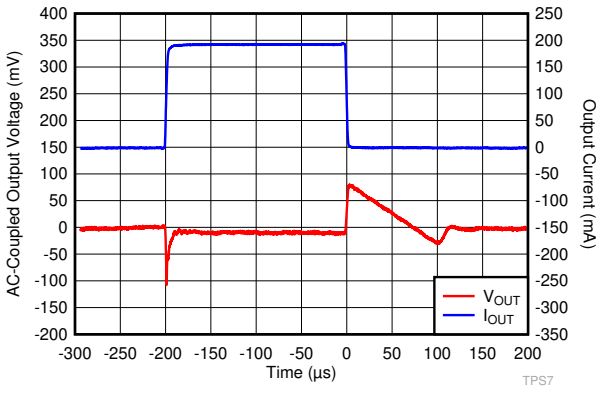
V_{OUT} = 1.8V, V_{IN} = 2.8V, C_{OUT} = 1µF, t_r = t_f = 1µs

Figure 5-13. I_{OUT} Transient From 1mA to 50mA



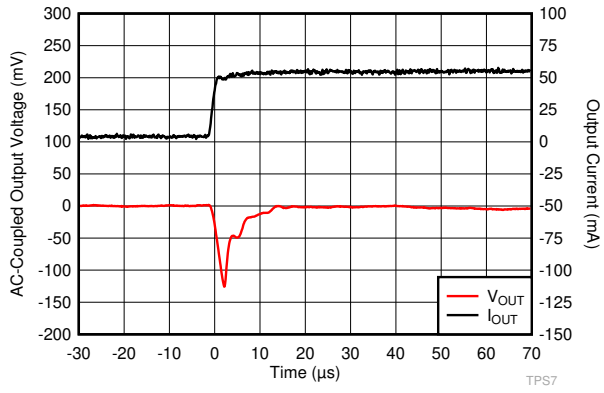
V_{OUT} = 1.8V, V_{IN} = 2.8V, C_{OUT} = 1µF, t_r = t_f = 1µs

Figure 5-14. I_{OUT} Transient From 1mA to 100mA



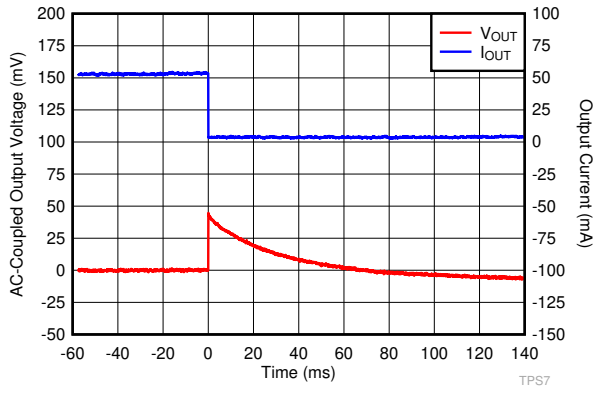
V_{OUT} = 1.8V, V_{IN} = 2.8V, C_{OUT} = 1µF, t_r = t_f = 1µs

Figure 5-15. I_{OUT} Transient From 1mA to 200mA



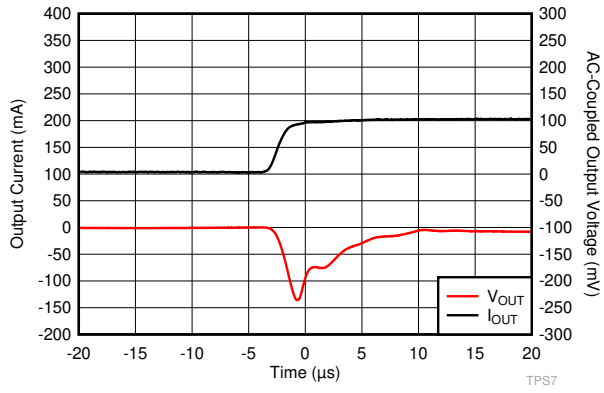
V_{OUT} = 1.8V, V_{IN} = 2.8V, C_{OUT} = 1µF, t_r = t_f = 1µs

Figure 5-16. I_{OUT} Transient From 0mA to 50mA



V_{OUT} = 1.8V, V_{IN} = 2.8V, C_{OUT} = 1µF, t_r = t_f = 1µs

Figure 5-17. I_{OUT} Transient From 50mA to 0mA

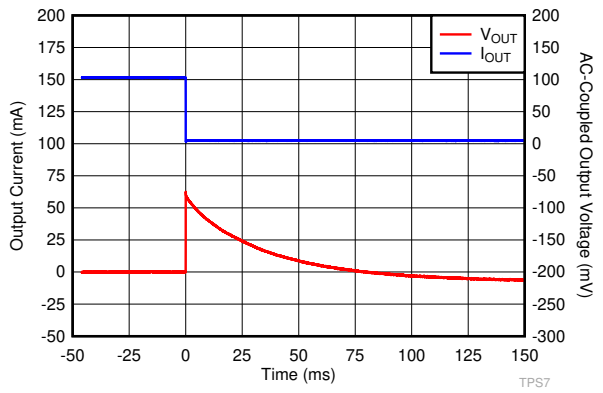


V_{OUT} = 1.8V, V_{IN} = 2.8V, C_{OUT} = 1µF, t_r = t_f = 1µs

Figure 5-18. I_{OUT} Transient From 0mA to 100mA

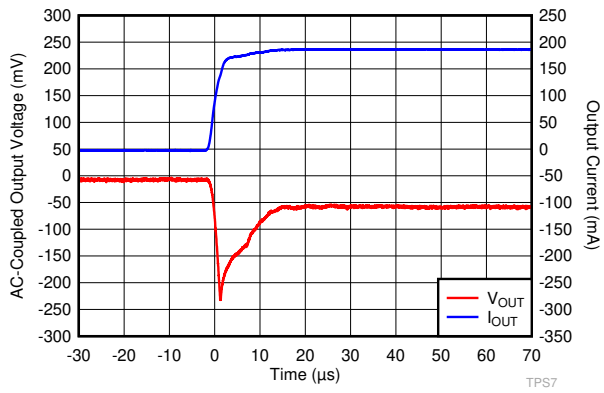
5.7 Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



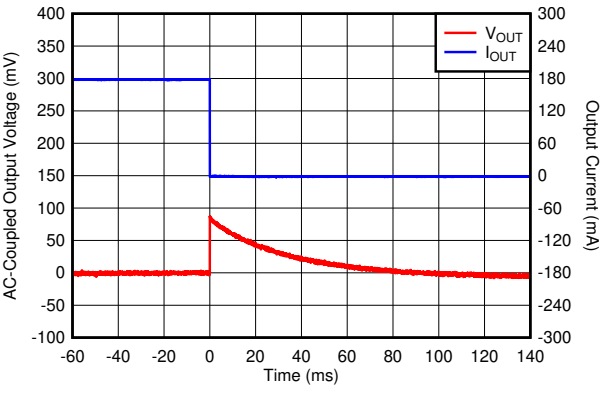
V_{OUT} = 1.8V, V_{IN} = 2.8V, C_{OUT} = 1µF, t_r = t_f = 1µs

Figure 5-19. I_{OUT} Transient From 100mA to 0mA



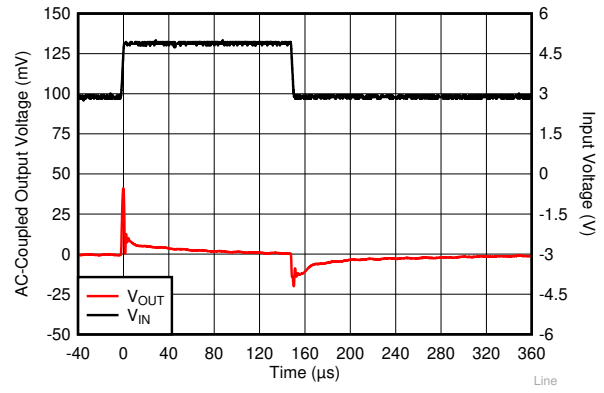
V_{OUT} = 1.8V, V_{IN} = 2.8V, C_{OUT} = 1µF, t_r = t_f = 1µs

Figure 5-20. I_{OUT} Transient From 0mA to 200mA



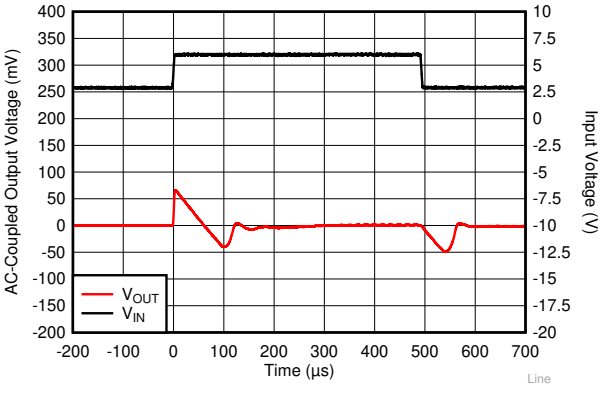
V_{OUT} = 1.8V, V_{IN} = 2.8V, C_{OUT} = 1µF, t_r = t_f = 1µs

Figure 5-21. I_{OUT} Transient From 200mA to 0mA



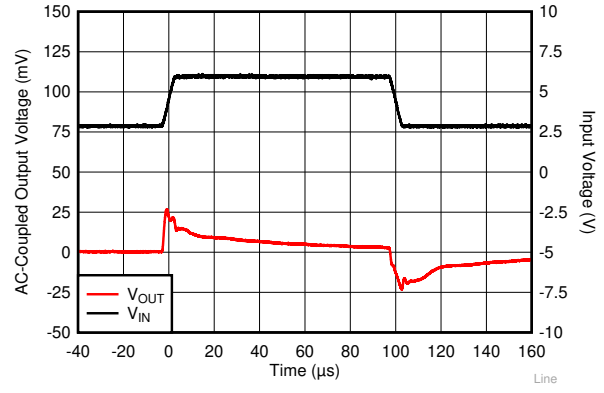
V_{OUT} = 1.8V, I_{OUT} = 200mA, C_{OUT} = 1µF, slew rate = 1V/µs

Figure 5-22. V_{IN} Transient From 2.8V to 4.8V



V_{OUT} = 1.8V, I_{OUT} = 1mA, C_{OUT} = 1µF, slew rate = 1V/µs

Figure 5-23. V_{IN} Transient From 2.8V to 6.0V

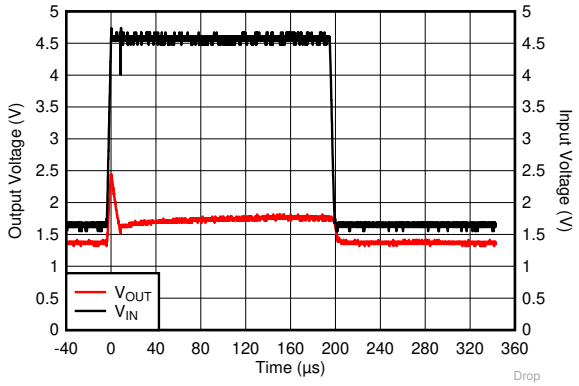


V_{OUT} = 1.8V, I_{OUT} = 200mA, C_{OUT} = 1µF, slew rate = 1V/µs

Figure 5-24. V_{IN} Transient From 2.8V to 6.0V

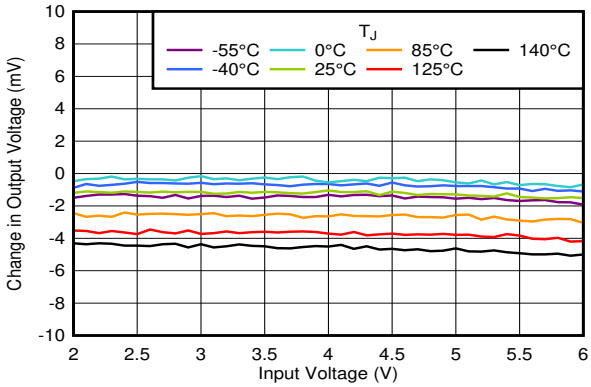
5.7 Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



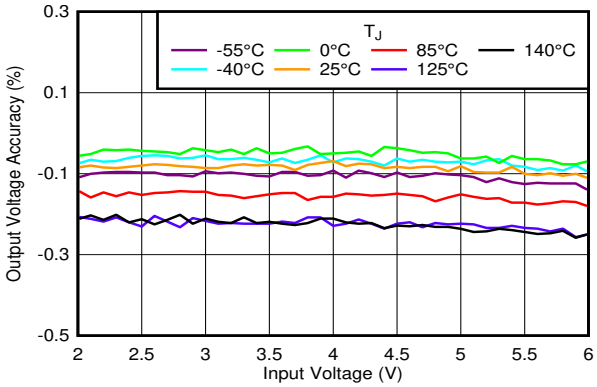
V_{OUT} = 1.8V, I_{OUT} = 100mA, C_{OUT} = 1µF, slew rate = 1V/µs

Figure 5-25. V_{IN} Transient From 1.5V to 4.5V



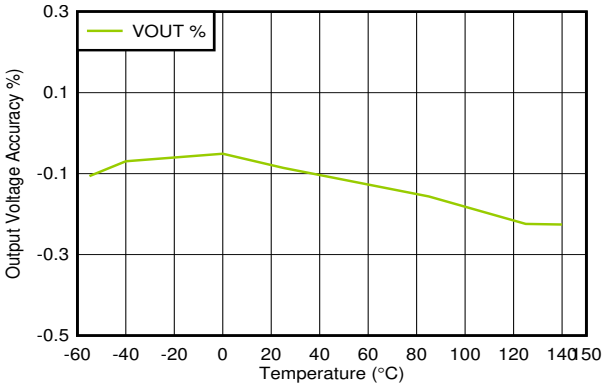
V_{OUT} = 1.8V, I_{OUT} = 1mA

Figure 5-26. Line Regulation vs V_{IN} and Temperature



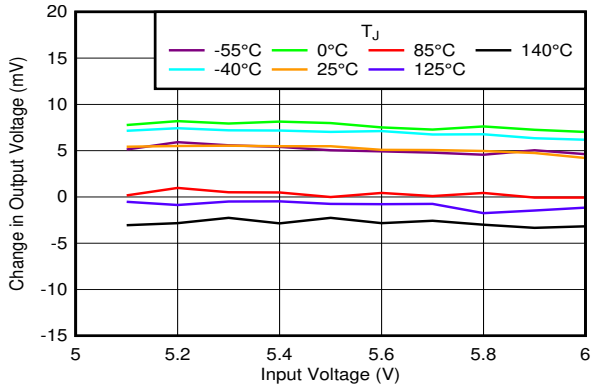
V_{OUT} = 1.8V, I_{OUT} = 1mA

Figure 5-27. Output Accuracy vs V_{IN} and Temperature



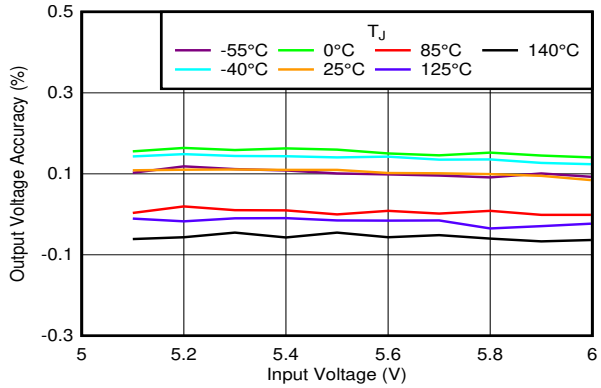
V_{OUT} = 1.8V, I_{OUT} = 1mA

Figure 5-28. Output Accuracy vs Temperature



V_{OUT} = 5.0V, I_{OUT} = 1mA

Figure 5-29. Line Regulation vs V_{IN} and Temperature

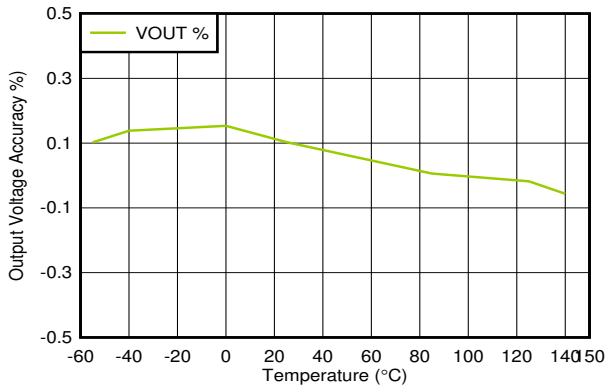


V_{OUT} = 5.0V, I_{OUT} = 1mA

Figure 5-30. Output Accuracy vs V_{IN} and Temperature

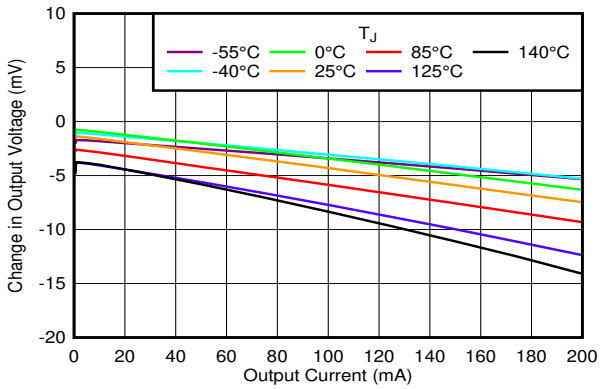
5.7 Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



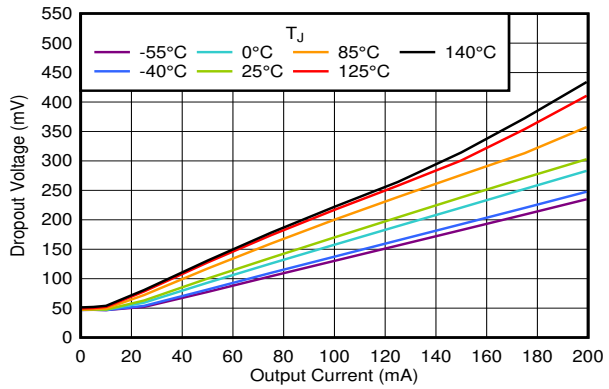
V_{OUT} = 5.0V, I_{OUT} = 1mA

Figure 5-31. Output Accuracy vs Temperature



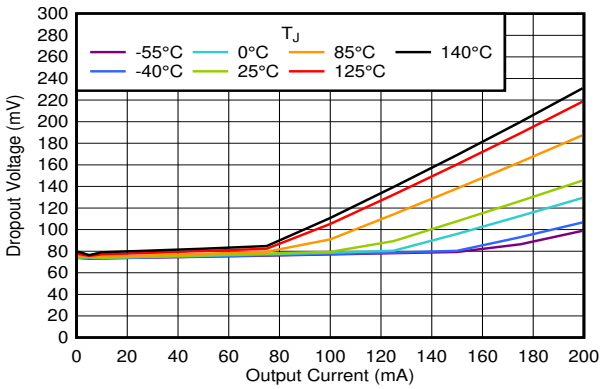
V_{OUT} = 1.8V

Figure 5-32. Load Regulation vs V_{IN} and Temperature



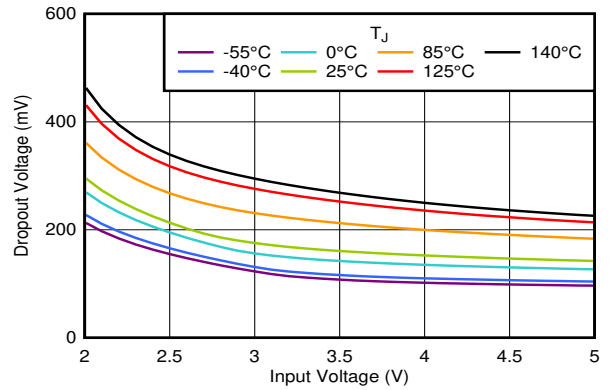
V_{OUT} = 1.8V

Figure 5-33. Dropout vs I_{OUT} and Temperature



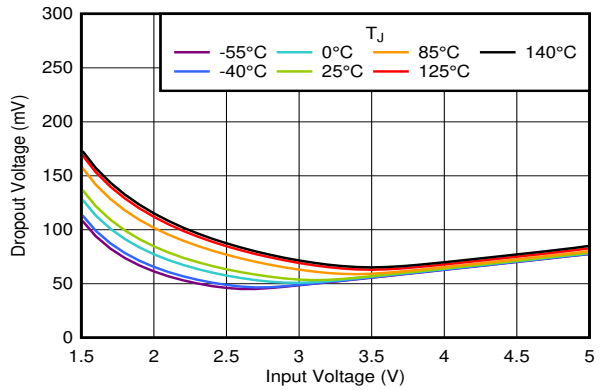
V_{OUT} = 5.0V

Figure 5-34. Dropout vs I_{OUT} and Temperature



I_{OUT} = 200mA

Figure 5-35. Dropout vs V_{IN} and Temperature

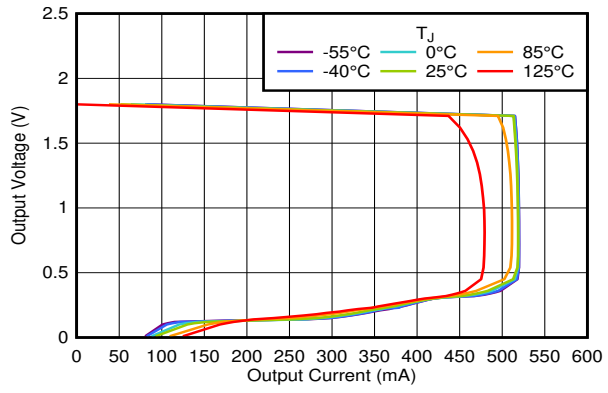


I_{OUT} = 50mA

Figure 5-36. Dropout vs V_{IN} and Temperature

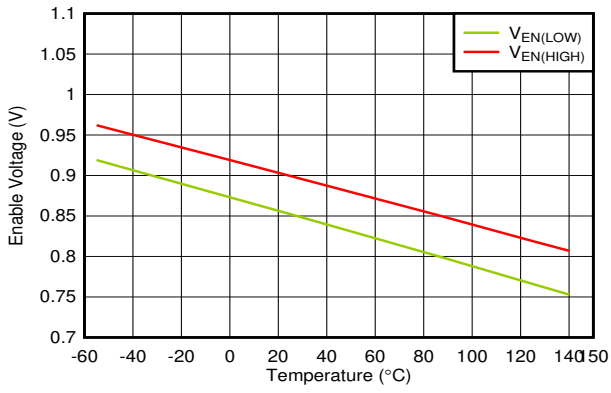
5.7 Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



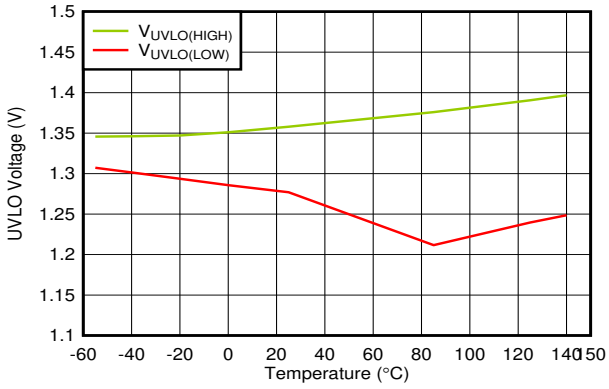
V_{OUT} = 1.8V

Figure 5-37. Foldback Current Limit vs I_{OUT} and Temperature



V_{OUT} = 5.0V

Figure 5-38. EN High and Low Threshold vs Temperature



V_{OUT} = 5.0V, I_{OUT} = 1mA

Figure 5-39. UVLO Rising and Falling Threshold vs Temperature

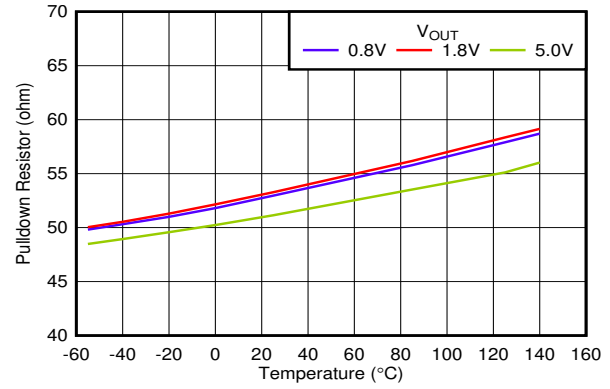


Figure 5-40. Pulldown Resistor vs Temperature and V_{OUT}

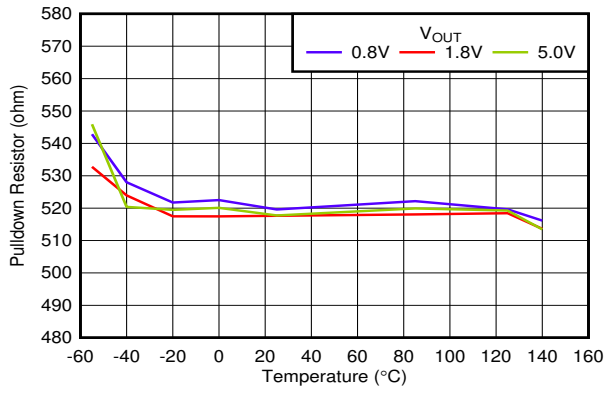
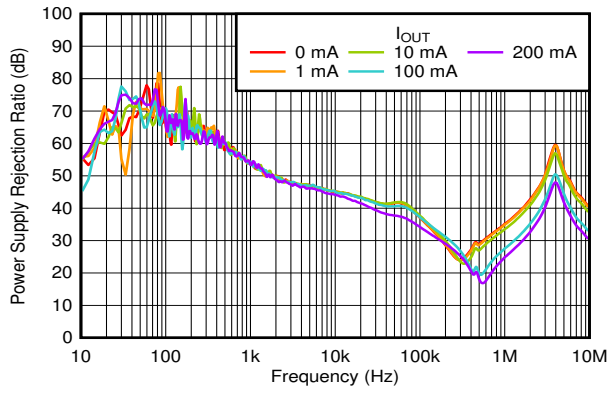


Figure 5-41. Smart Enable Pulldown Resistor vs Temperature and V_{OUT}

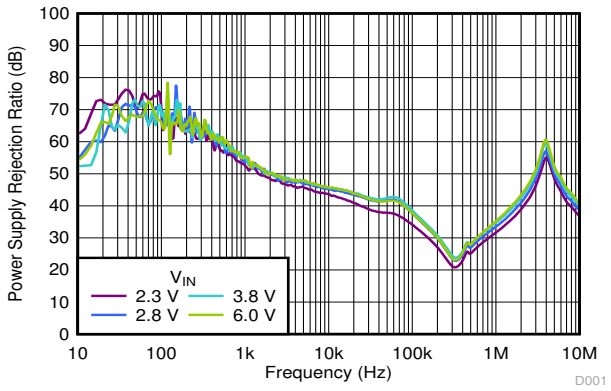


V_{IN} = 2.8V, V_{OUT} = 1.8V, C_{OUT} = 1µF

Figure 5-42. PSRR vs Frequency and I_{OUT}

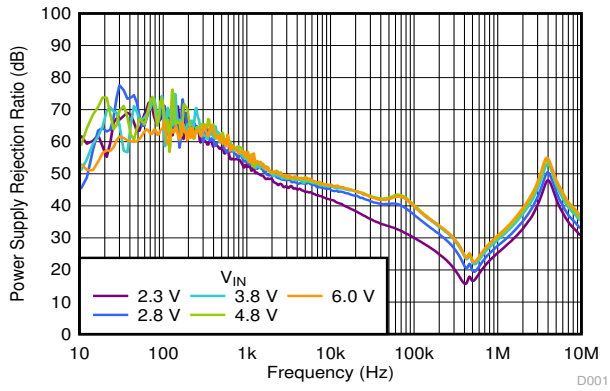
5.7 Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



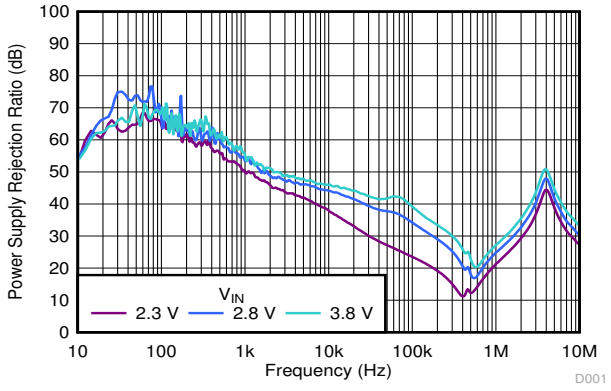
V_{OUT} = 1.8V, I_{OUT} = 10mA, C_{OUT} = 1µF

Figure 5-43. PSRR vs Frequency and V_{IN}



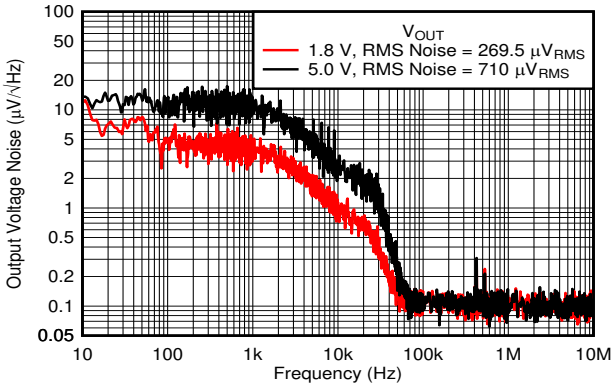
V_{OUT} = 1.8V, I_{OUT} = 100mA, C_{OUT} = 1µF

Figure 5-44. PSRR vs Frequency and V_{IN}



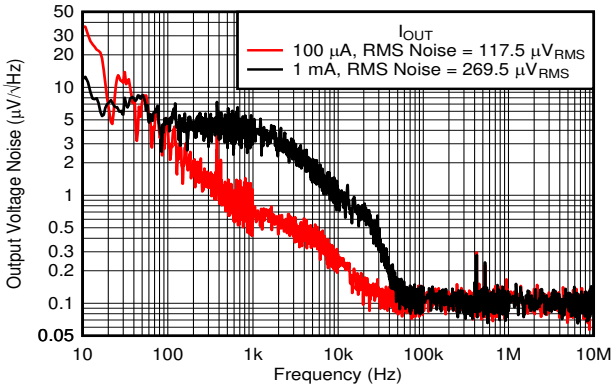
V_{OUT} = 1.8V, I_{OUT} = 200mA, C_{OUT} = 1µF

Figure 5-45. PSRR vs Frequency and V_{IN}



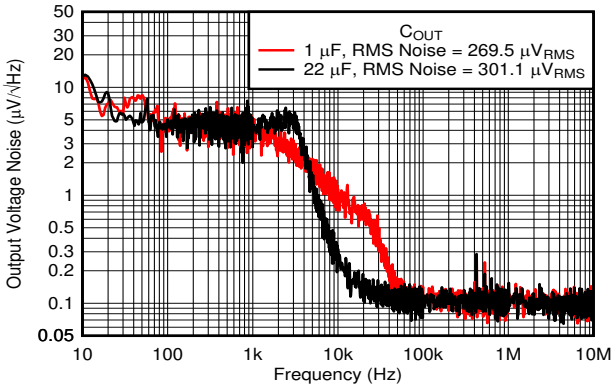
V_{IN} = V_{OUT} + 1.0V, I_{OUT} = 1mA, C_{OUT} = 1µF

Figure 5-46. Output Noise vs Frequency and V_{OUT}



V_{OUT} = 1.8V, V_{IN} = 2.8V, C_{OUT} = 1µF

Figure 5-47. Output Noise vs Frequency and I_{OUT}

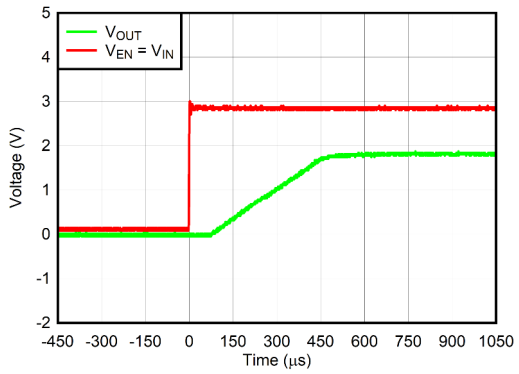


V_{OUT} = 1.8V, V_{IN} = 2.8V, I_{OUT} = 1mA

Figure 5-48. Output Noise vs Frequency and C_{OUT}

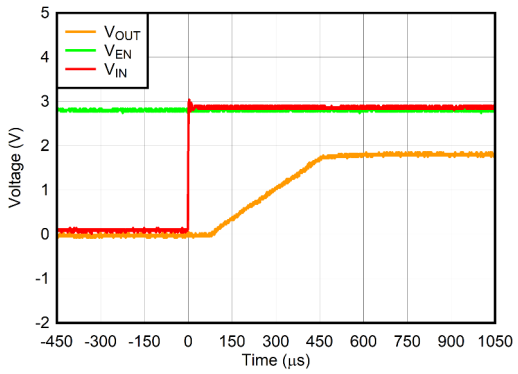
5.7 Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



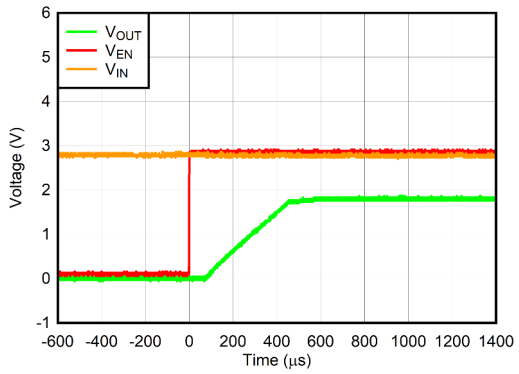
V_{OUT} = 1.8V, I_{OUT} = 200mA, C_{OUT} = 1µF

Figure 5-49. Start-Up With V_{EN} = V_{IN}



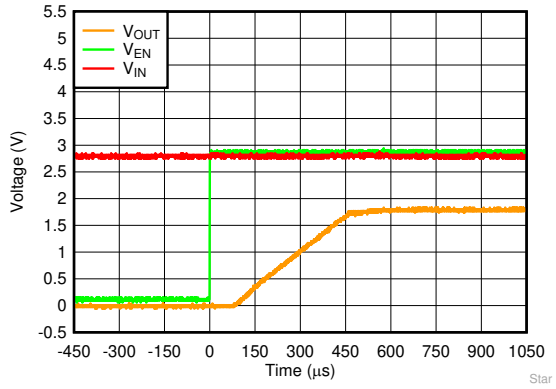
V_{OUT} = 1.8V, I_{OUT} = 200mA, C_{OUT} = 1µF

Figure 5-50. Start-Up With V_{EN} Before V_{IN}



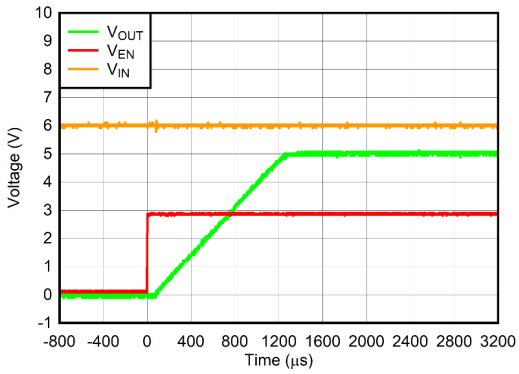
V_{OUT} = 1.8V, I_{OUT} = 200mA, C_{OUT} = 1µF

Figure 5-51. Start-Up With V_{EN} After V_{IN}



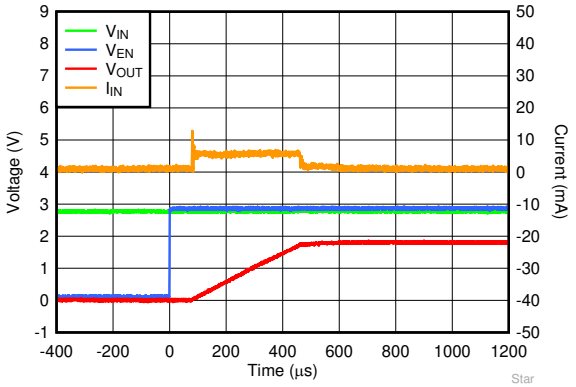
V_{OUT} = 1.8V, I_{OUT} = 0mA, C_{OUT} = 1µF

Figure 5-52. Start-Up With V_{EN} After V_{IN}



V_{OUT} = 5.0V, I_{OUT} = 200mA, C_{OUT} = 1µF

Figure 5-53. Start-Up With V_{EN} After V_{IN}

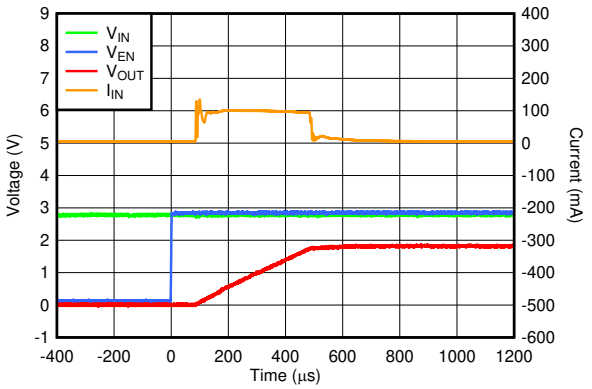


V_{OUT} = 1.8V, I_{OUT} = 0mA

Figure 5-54. Start-Up Inrush Current With C_{OUT} = 1µF

5.7 Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 1mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1µF (unless otherwise noted)



V_{OUT} = 1.8V, I_{OUT} = 0mA

Figure 5-55. Start-Up Inrush Current With C_{OUT}= 22µF

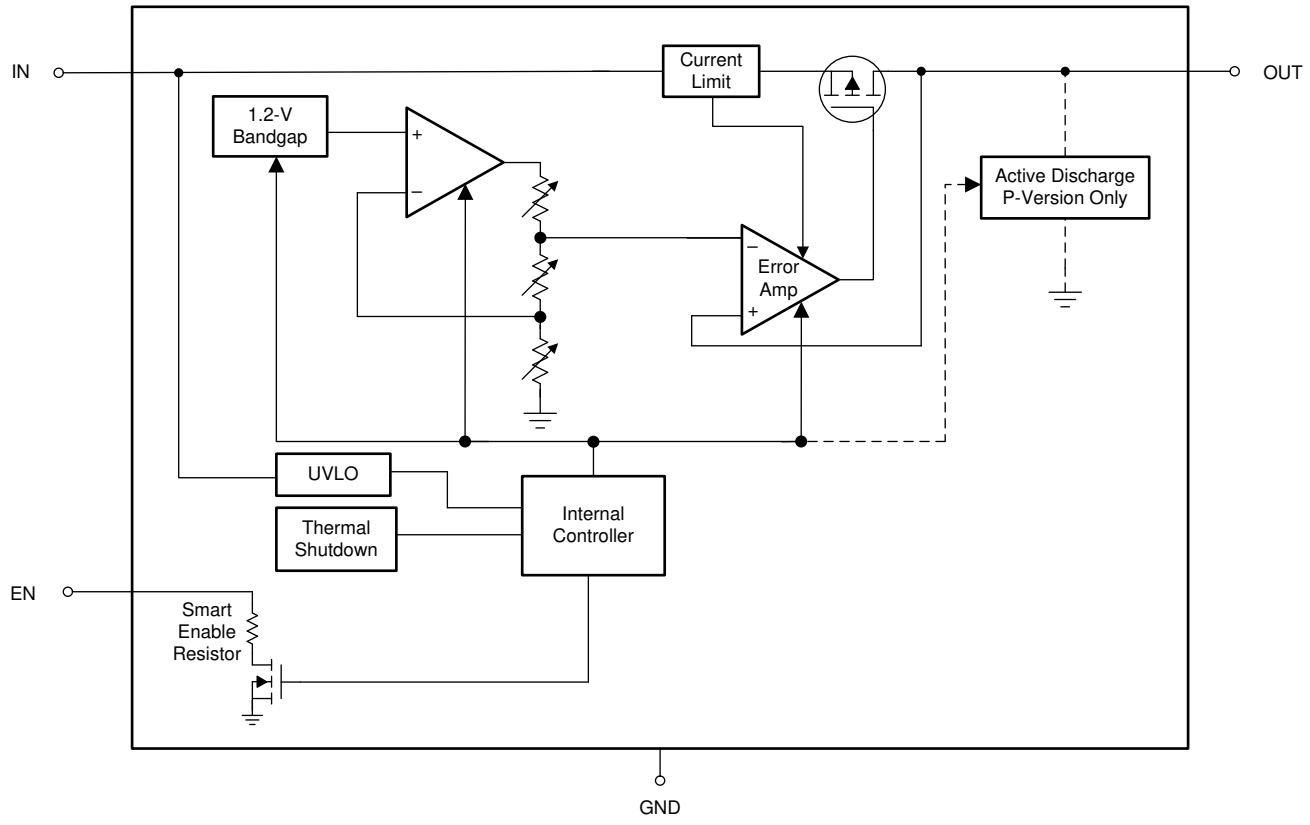
6 Detailed Description

6.1 Overview

The TLV7A03 is a ultra-low I_Q linear voltage regulator optimized for excellent transient performance. These characteristics make the device designed for most battery-powered applications.

This low-dropout linear regulator (LDO) offers active discharge, foldback current limit, shutdown, and thermal protection capability.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Excellent Transient Response

The TLV7A03 includes several innovative circuits to provide excellent transient response. Dynamic biasing increases the I_Q for a short duration during transients to extend the closed-loop bandwidth and improve the output response time to transients.

Adaptive biasing increases the I_Q as the DC load current increases, extending the bandwidth of the loop. The response time across the output voltage range is constant because a buffered reference topology is used, which keeps the control loop in unity gain at any output voltage.

These features give the device a wide loop bandwidth during transients that provides excellent transient response while maintaining low I_Q in steady-state conditions.

6.3.2 Active Discharge (P-Version Only)

The device has an internal pulldown MOSFET that connects a $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin or by the undervoltage lockout (UVLO).

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed. Reverse current potentially flows from the output to the input. This reverse current flow potentially causes damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

6.3.3 Low I_Q in Dropout

In most LDOs the I_Q significantly increases when the device is placed into dropout, which is especially true for low I_Q LDOs. The TLV7A03 helps to reduce the battery discharge by detecting when the device is operating in dropout conditions and maintaining a low I_Q.

6.3.4 Smart Enable

The enable (EN) input polarity is active high. The output voltage is enabled when the voltage of the enable input is greater than $V_{EN(HI)}$ and disabled when the enable input voltage is less than $V_{EN(LOW)}$. If independent control of the output voltage is not needed, connect EN to IN.

This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above $V_{EN(HI)}$, as listed in the *Electrical Characteristics* table, the device is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the device. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

This device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

6.3.5 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.6 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 0.5V.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-1 shows a diagram of the foldback current limit.

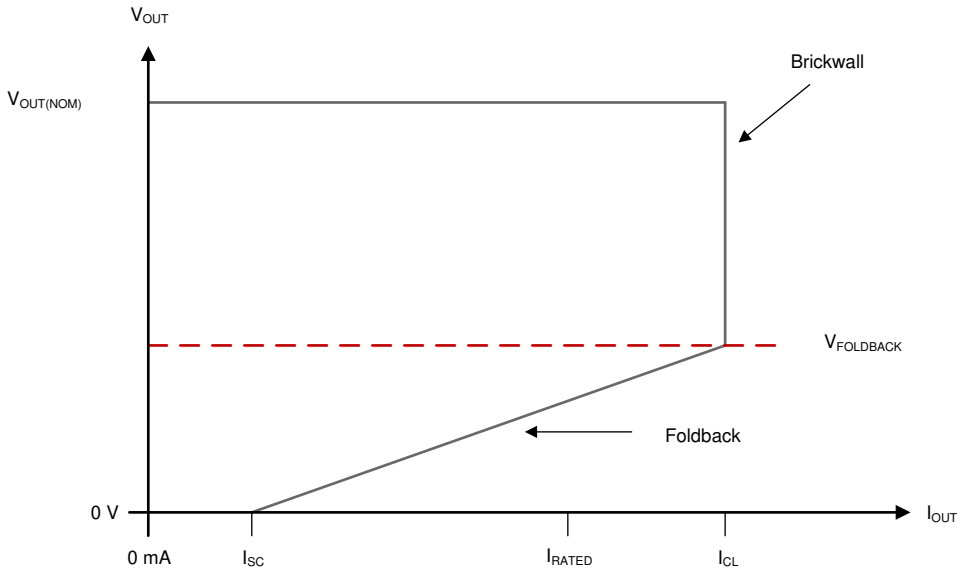


Figure 6-1. Foldback Current Limit

6.3.7 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

6.3.8 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus, the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up is high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.3 Dropout Operation

The device operates in dropout mode when the input voltage is lower than the nominal output voltage plus the specified dropout voltage. However, make sure all other conditions are met for normal operation. In this mode, the output voltage tracks the input voltage. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. Because of this operation, the transient performance of the device becomes significantly degraded. Line or load transients in dropout results in large output-voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven into the ohmic or triode region. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start-up. During dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the input voltage returns to a value ≥ $V_{OUT(NOM)} + V_{DO}$, the output voltage overshoots for a short period of time. During this time, the device pulls the pass transistor back into the linear region. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage.

6.4.4 Disabled

The device output is shutdown by forcing the enable pin voltage to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, and internal circuits are shutdown. The output voltage is also actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. Use a higher value capacitor if large, fast rise-time load or line transients are anticipated. Additionally, use this capacitor if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response. These transitions are from a light to a heavy load and from a heavy to a light load. The regions shown in Figure 7-1 are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

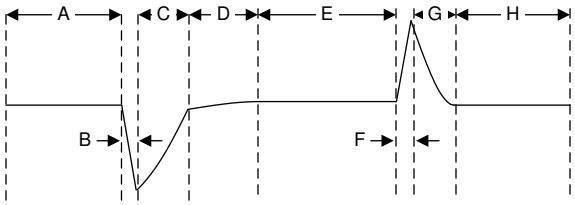


Figure 7-1. Load Transient Waveform

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. Larger DC loads reduce the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

7.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit makes sure the device stays disabled before the input supply reaches the minimum operational voltage range. This circuit also makes sure the device shuts down when the input supply collapses. Figure 7-2 shows the UVLO circuit response to various input voltage events. The diagram is separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output potentially falls out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0V. The output falls because of the load and active discharge circuit.

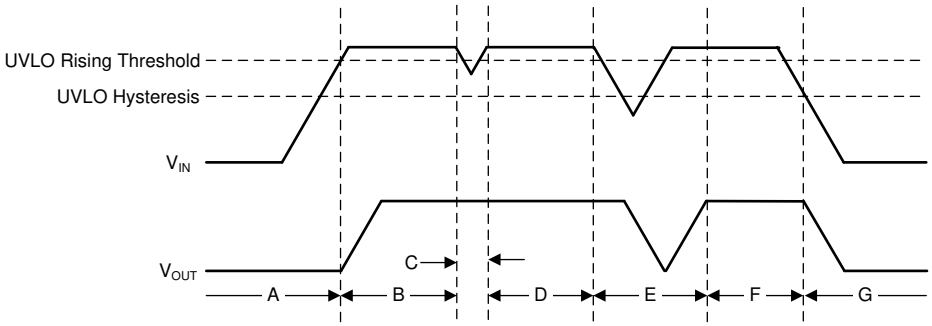


Figure 7-2. Typical UVLO Operation

7.1.5 Power Dissipation (P_D)

Circuit reliability demands proper consideration be given to device power dissipation and location of the circuit on the printed circuit board (PCB). Verify correct sizing of the thermal plane. Make sure the PCB area around the regulator is as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use Equation 2 to approximate P_D:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation is minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TLV7A03 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to Equation 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$). The $R_{\theta JA}$ component is the combined PCB and device package and the temperature of the ambient air (T_A). Equation 4 rearranges Equation 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (4)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. Therefore, $R_{\theta JA}$ varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area. This value is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package $R_{\theta JC(bot)}$ plus the thermal resistance contribution by the PCB copper. $R_{\theta JC(bot)}$ is the junction-to-case (bottom) thermal resistance.

7.1.5.1 Estimating Junction Temperature

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \quad (5)$$

where:

- P_D is the power dissipated as explained in Equation 2
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

7.1.5.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in Figure 7-3 and is separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by Equation 4. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO. Thus when $V_{IN} - V_{OUT}$ increases, the output current decreases.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

Figure 7-3 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Thermal Information* table.

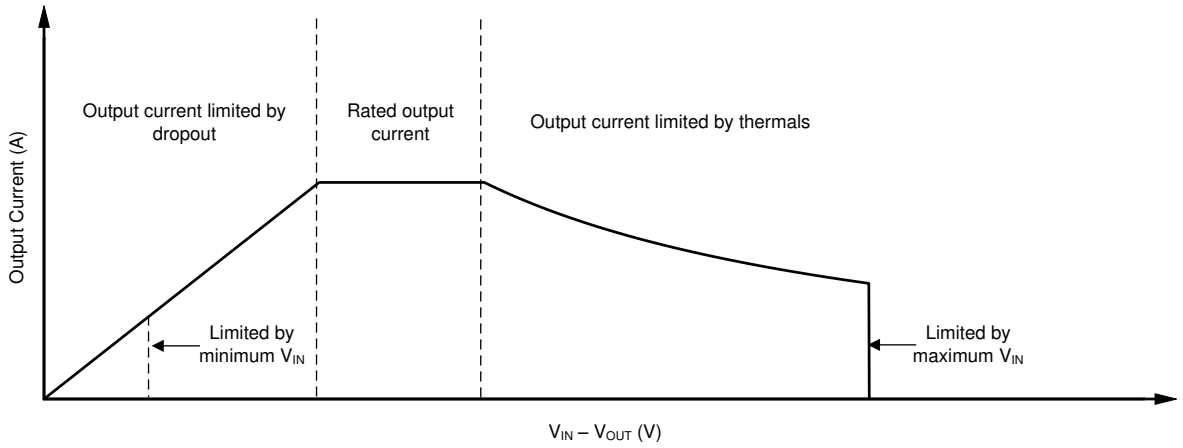


Figure 7-3. Region Description of Continuous Operation Regime

7.2 Typical Application

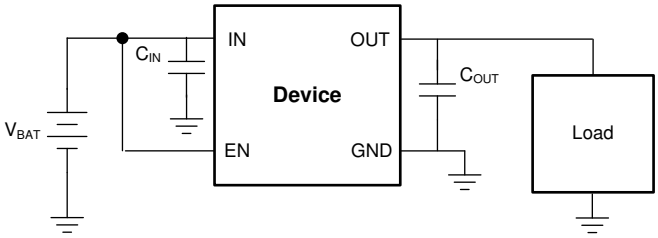


Figure 7-4. Operation From a Battery Input Supply

7.2.1 Design Requirements

Table 7-1 lists the design parameters for Figure 7-4.

Table 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	2.0V to 3.2V (Li/MnO_2 coin cell)
Output voltage	1.2V, ±20mV
Input current	200mA, maximum
Output load	10mA DC
Maximum ambient temperature	70°C

7.2.2 Detailed Design Procedure

For this design example, the 1.2V TLV7A03 is selected. A Li/MnO_2 coin cell is used, thus a 1.0µF input capacitor is recommended to minimize transient currents drawn from the battery. Use a 1.0µF output capacitor for excellent load transient response. Keep the dropout voltage (V_{DO}) within the TLV7A03 dropout voltage specification for the 1.2V output voltage option. This voltage level keeps the device in regulation under all load and temperature conditions for this design. Use the recommend 1µF input and output capacitor. Coin cells typically have output resistance values equal to several 10s of ohms, depending on capacity, temperature, and state of charge. The very small ground current consumed by the regulator maintains a high current efficiency as compared to the load current consumed by the system. This efficiency is depicted in Figure 7-5, which allows for long battery life. Equation 6 calculates the current efficiency (I_η) of this system.

$$I_{\eta}(\%) = I_{OUT} / (I_{OUT} + I_{Q}) \times 100 \quad (6)$$

7.2.3 Application Curve

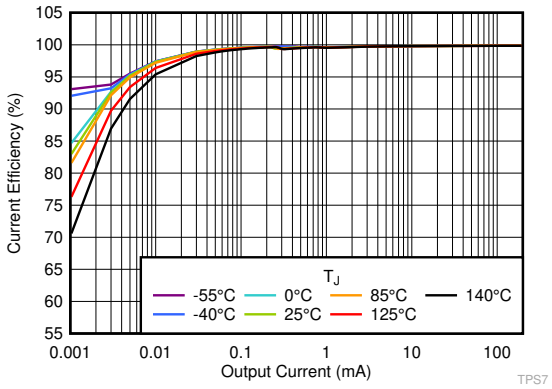


Figure 7-5. Current Efficiency vs I_{OUT} and Temperature

7.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.5V to 6.0V. Make sure the input supply is well regulated and free of spurious noise. To verify that the output voltage is well regulated and dynamic performance is optimum, make sure the input supply is at least $V_{OUT(nom)}$ + 0.5V. Use a 1µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

7.4 Layout

7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via potentially wicks solder or solder paste away from the thermal pad joint during the soldering process. Therefore, leading to a compromised solder joint on the thermal pad.

7.4.2 Layout Examples

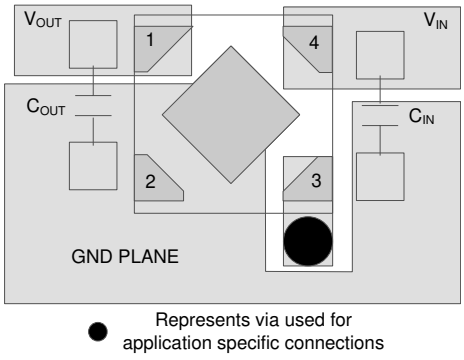


Figure 7-6. Layout Example for DQN Package

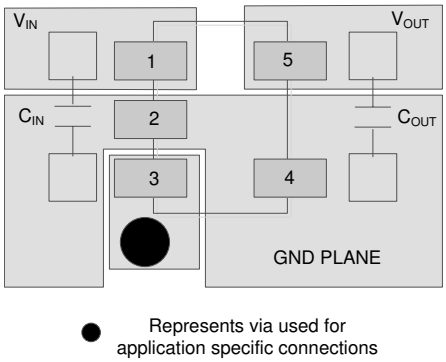


Figure 7-7. Layout Example for DBV Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1) (2)	DESCRIPTON
TLV7A03 **xx(x)Pyyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100mV, two digits are used in the ordering number. Otherwise, three digits are used (for example, 28 = 2.8V; 125 = 1.25V). **P** indicates an active output discharge feature. **yyy** is the package designator. **z** is the package quantity. R indicates reel (3000 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.8V to 5.0V in 50mV increments are available. Contact the factory for details and availability.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7A0312PDQNR1	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RK
TLV7A0315PDQNR1	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RL
TLV7A0318PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3RSH
TLV7A0318PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RM
TLV7A0325PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3RTH
TLV7A0325PDQNR3	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RN
TLV7A0328PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RO
TLV7A0330PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3RVH
TLV7A0330PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RP
TLV7A0331PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RU
TLV7A0333PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3RUH
TLV7A0333PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

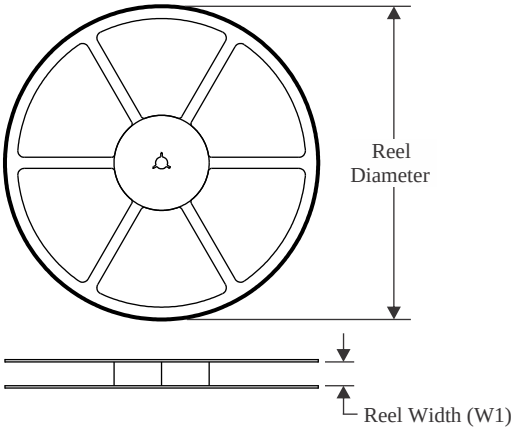
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

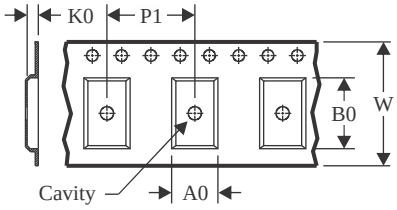
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

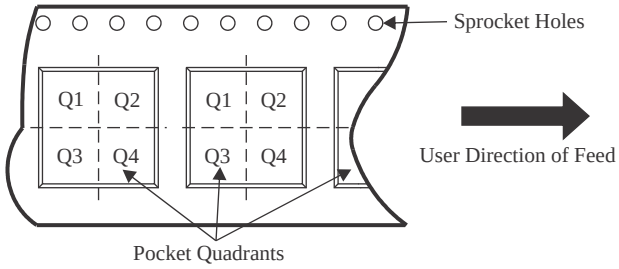


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

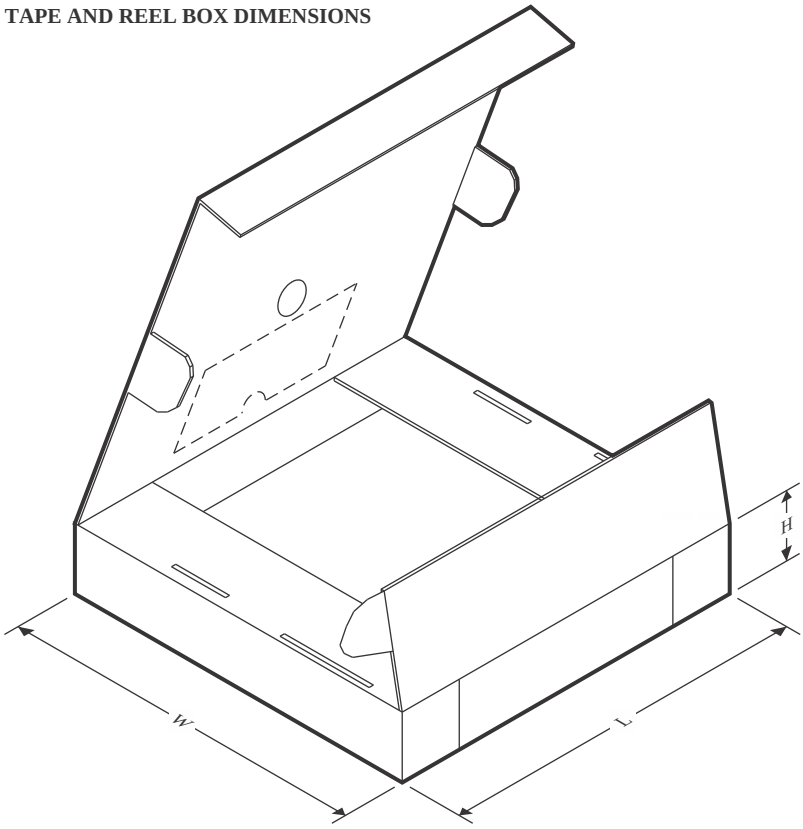
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7A0312PDQNR1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q1
TLV7A0315PDQNR1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q1
TLV7A0318PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7A0318PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV7A0325PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7A0325PDQNR3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q3
TLV7A0328PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV7A0330PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7A0330PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV7A0331PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV7A0333PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7A0333PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7A0312PDQNR1	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV7A0315PDQNR1	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV7A0318PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7A0318PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV7A0325PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7A0325PDQNR3	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV7A0328PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV7A0330PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7A0330PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV7A0331PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV7A0333PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7A0333PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

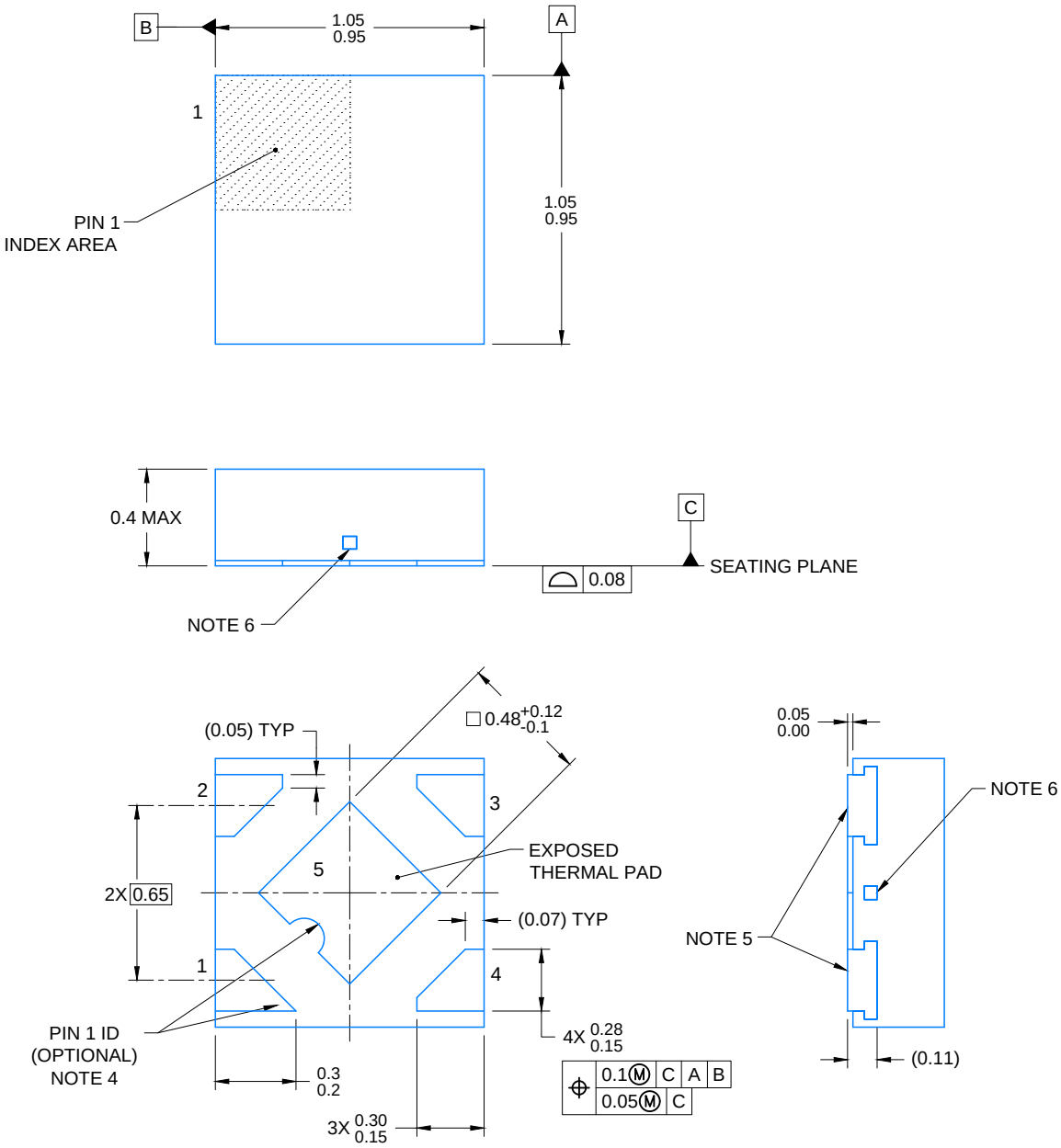
4210367/F

PACKAGE OUTLINE

DQN0004A

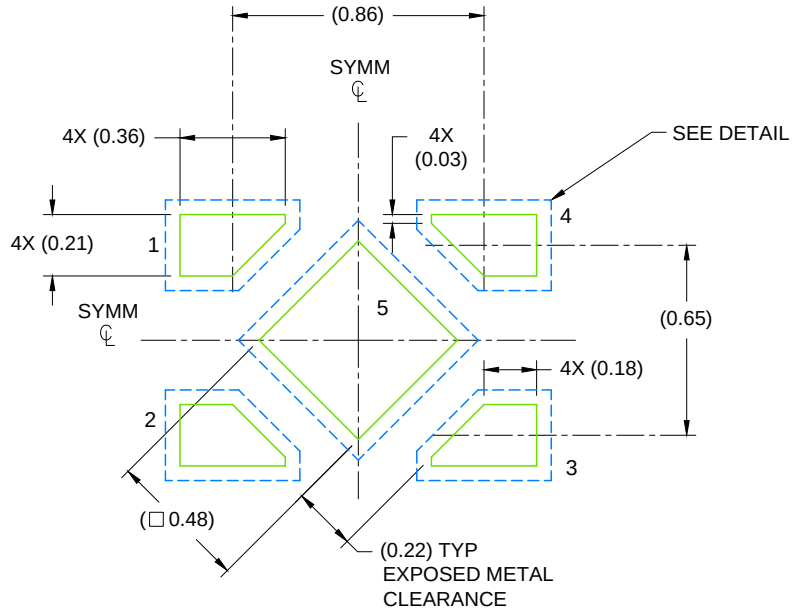
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



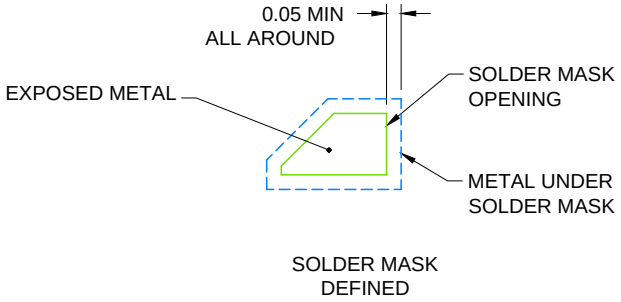
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X

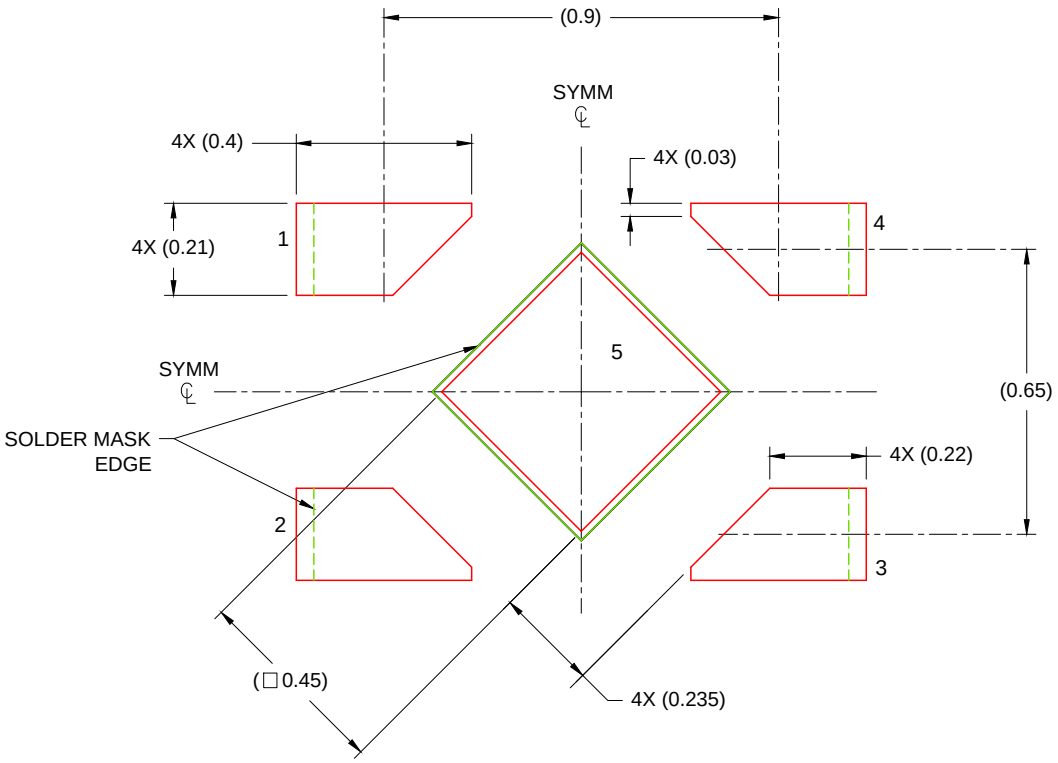


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

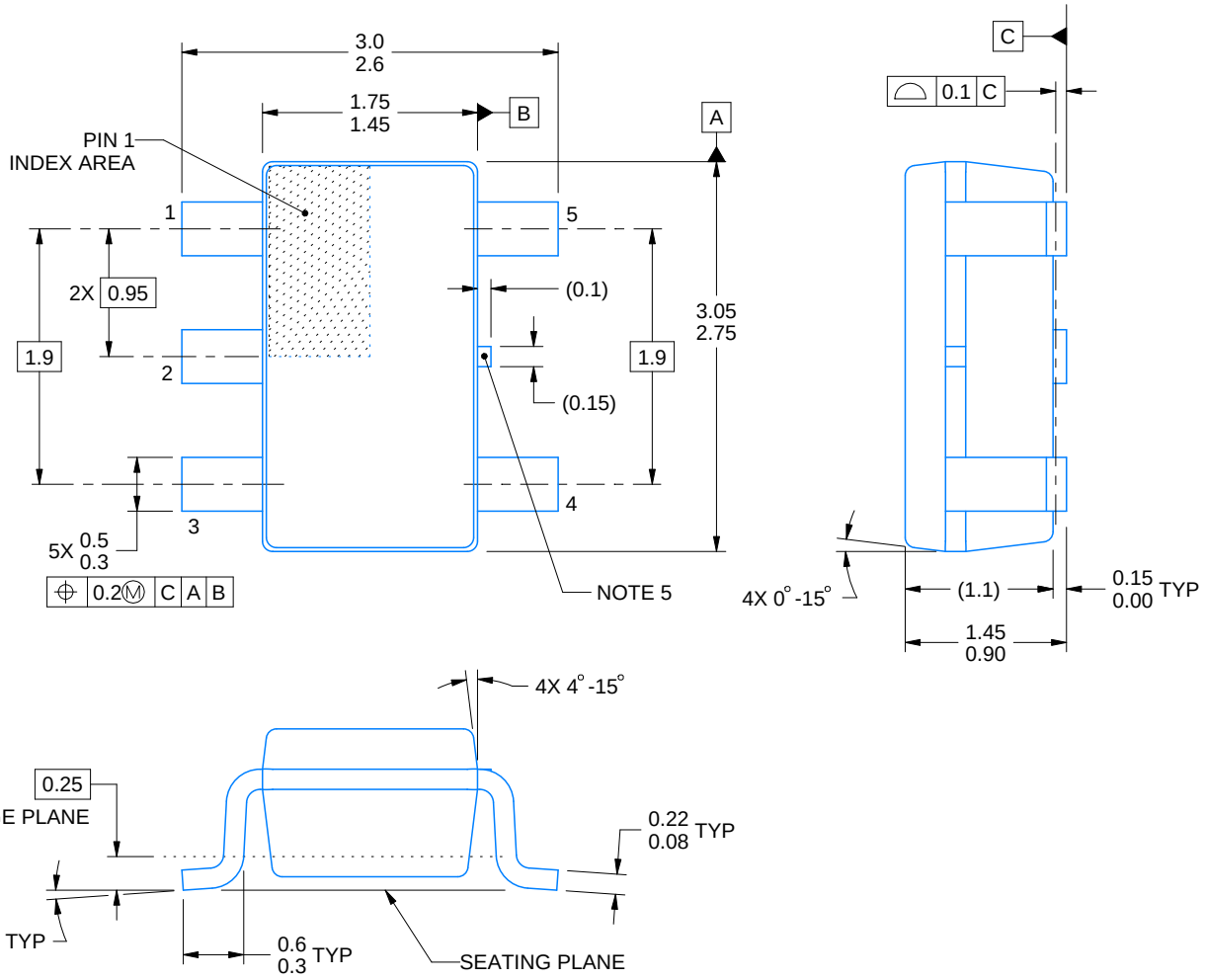
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

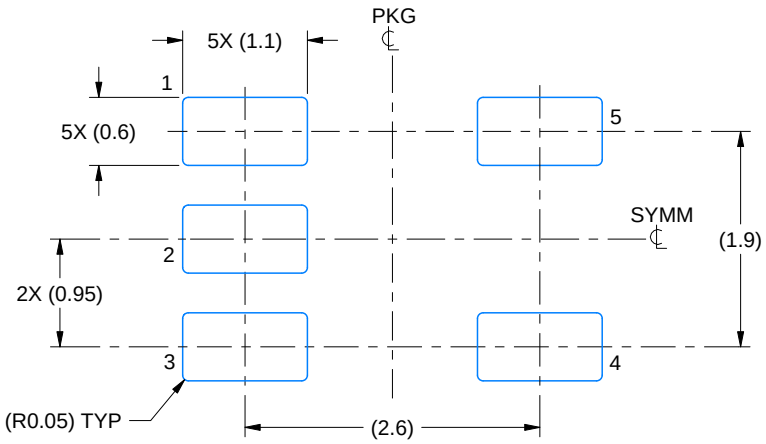
SMALL OUTLINE TRANSISTOR



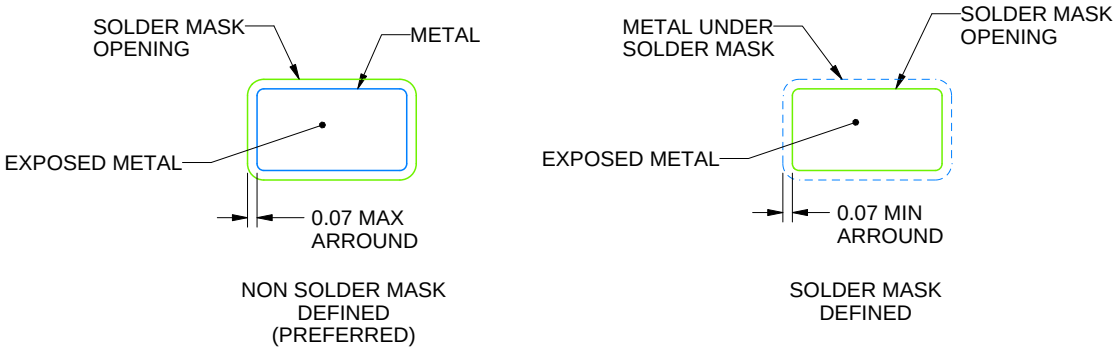
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

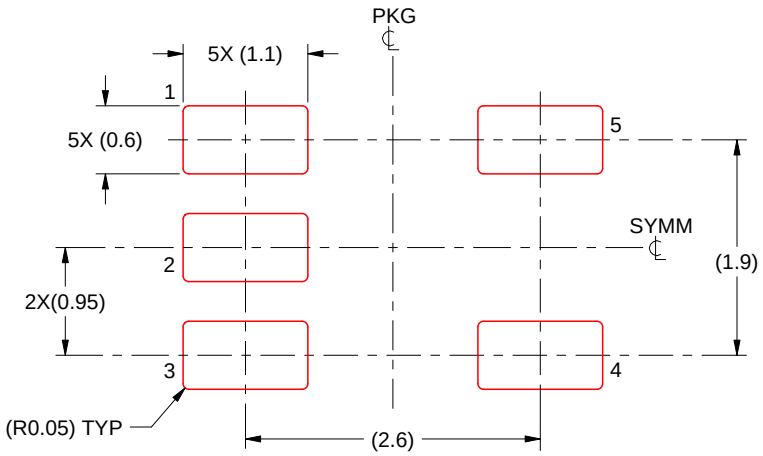


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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