features

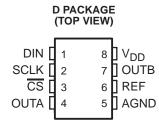
- Dual 8-Bit Voltage Output DAC
- Programmable Internal Reference
- Programmable Settling Time
 - 3 μs in Fast Mode
 - 10 µs in Slow Mode
- Compatible With TMS320 and SPI[™] Serial Ports
- Differential Nonlinearity <0.2 LSB Max
- Monotonic Over Temperature

description

The TLV5625 is a dual 8-bit voltage output DAC with a flexible 3-wire serial interface. The serial interface is compatible with TMS320, SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 4 control and 8 data bits.

applications

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices



The resistor string output voltage is buffered by an x2 gain rail-to-rail output buffer. The buffer features a Class-AB output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed versus power dissipation.

Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in an 8-pin SOIC package in standard commercial and industrial temperature ranges.

AVAILABLE OPTIONS

	PACKAGE
TA	SOIC
	(D)
0°C to 70°C	TLV5625CD
-40°C to 85°C	TLV5625ID



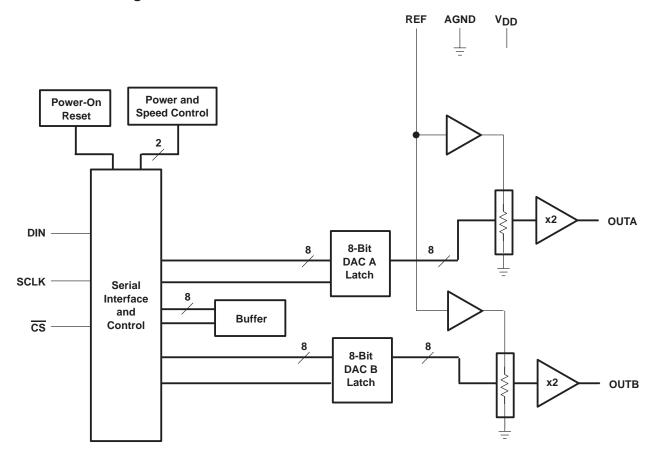
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Microwire is a trademark of National Semiconductor Corporation.



functional block diagram



Terminal Functions

TERM	TERMINAL		PERCEINTION							
NAME	NO.	I/O/P	DESCRIPTION							
AGND	5	Р	Ground							
CS	3	I	Chip select. Digital input active low, used to enable/disable inputs.							
DIN	1	I	Digital serial data input							
OUTA	4	0	DAC A analog voltage output							
OUTB	7	0	DAC B analog voltage output							
REF	6	I	Analog reference voltage input							
SCLK	2	I	Digital serial clock input							
V_{DD}	8	Р	Positive power supply							

2.7-V TO 5.5-V LOW-POWER DUAL 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V _{DD} to AGND)	
Reference input voltage range	$\dots - 0.3 \text{ V to V}_{DD} + 0.3 \text{ V}$
Digital input voltage range	\dots – 0.3 V to V _{DD} + 0.3 V
Operating free-air temperature range, T _A : TLV5625C	0°C to 70°C
TLV5625I	–40°C to 85°C
Storage temperature range, T _{stq}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT	
Complements of No.	$V_{DD} = 5 V$		4.5	5	5.5	V	
Supply voltage, V _{DD}	$V_{DD} = 3 V$		2.7	3	3.3	V	
Power on reset, POR			0.55		2	V	
Likeb Level Belletter of cellene M	V _{DD} = 2.7 V		2				
High-level digital input voltage, V _{IH}	V _{DD} = 5.5 V		2.4			V	
	V _{DD} = 2.7 V				0.6	.,	
Low-level digital input voltage, V _{IL}	V _{DD} = 5.5 V				1	V	
Defended by the DEF terminal	V _{DD} = 5 V (see Note 1)	AC	SND	2.048	V _{DD} -1.5	V	
Reference voltage, V _{ref} to REF terminal	V _{DD} = 3 V (see Note 1)	AC	SND	1.024	V _{DD} -1.5	V	
Load resistance, R _L			2			kΩ	
Load capacitance, CL					100	pF	
Clock frequency, f _{CLK}					20	MHz	
On arcting free air temperature T	TLV5625C		0		70	°C	
Operating free-air temperature, T _A	TLV5625I		-40		85	, J	

NOTE 1: Due to the x2 output buffer, a reference input voltage ≥ (V_{DD}−0.4 V)/2 causes clipping of the transfer function.



TLV5625

2.7-V TO 5.5-V LOW-POWER DUAL 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN

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electrical characteristics over recommended operating conditions (unless otherwise noted)

power supply

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I _{DD}	Dougs oursely oursest	No load, All inputs = AGND or	Fast		1.8	2.3	A
	Power supply current	V _{DD} , DAC latch = 0x800	Slow		0.8	1	mA
	Power-down supply current				1	3	μΑ
2000		Zero scale, See Note 2			-65		
PSRR	Power supply rejection ratio	Full scale, See Note 3			-65		dB

NOTES: 2. Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:

 $PSRR = 20 \log [(E_{ZS}(V_{DD}max) - E_{ZS}(V_{DD}min)/V_{DD}max]]$

3. Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by: PSRR = 20 log [(E_G(V_{DD}max) – E_G(V_{DD}min)/V_{DD}max]

static DAC specifications

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		8			bits
INL	Integral nonlinearity	See Note 4		±0.3	±0.5	LSB
DNL	Differential nonlinearity	See Note 5		±0.07	±0.2	LSB
EZS	Zero-scale error (offset error at zero scale)	See Note 6			±12	mV
E _{ZS} TC	Zero-scale-error temperature coefficient	See Note 7		10		ppm/°C
EG	Gain error	See Note 8			±0.5	% full scale V
E _G T _C	Gain-error temperature coefficient	See Note 9		10		ppm/°C

- NOTES: 4. The relative accuracy of integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale, excluding the effects of zero-code and full-scale errors.
 - 5. The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1-LSB amplitude change of any two adjacent codes.
 - 6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
 - 7. Zero-scale error temperature coefficient is given by: E_{ZS} TC = $[E_{ZS}$ (T_{max}) E_{ZS} (T_{min})]/2 V_{ref} × 10⁶/(T_{max} T_{min}).
 - 8. Gain error is the deviation from the ideal output (2 V_{ref} 1 LSB) with an output load of 10 k Ω .
 - 9. Gain temperature coefficient is given by: $E_G T_C = [E_G (T_{max}) E_g (T_{min})]/2V_{ref} \times 10^6/(T_{max} T_{min})$.

output specifications

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VO	Output voltage range	$R_L = 10 \text{ k}\Omega$	0		V _{DD} -0.4	V
	Output load regulation accuracy	$V_{O} = 4.096 \text{ V}, 2.048 \text{ V R}_{L} = 2 \text{ k}\Omega$			±0.29	% FS

reference input

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
٧ı	Input voltage range			0		V _{DD-1.5}	V
R _I	Input resistance				10		ΜΩ
Cl	Input capacitance				5		pF
	Deference input handwidth	DEE 0.27 + 4.0247/do	Fast		1.3		MHz
	Reference input bandwidth	REF = 0.2 V _{pp} + 1.024 V dc	Slow		525		kHz
	Reference feedthrough	REF = 1 V _{pp} at 1 kHz + 1.024 V dc (see Note 10)	·		-80		dB

NOTE 10: Reference feedthrough is measured at the DAC output with an input code = 0x000.



2.7-V TO 5.5-V LOW-POWER DUAL 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN

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electrical characteristics over recommended operating conditions (unless otherwise noted) (Continued)

digital inputs

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
lіН	High-level digital input current	$V_I = V_{DD}$			1	μΑ
IIL	Low-level digital input current	V _I = 0 V	-1			μΑ
Ci	Input capacitance			8		pF

analog output dynamic performance

	PARAMETER	TEST	CONDITIONS		MIN	TYP	MAX	UNIT
	Output anti-on time full and	$R_L = 10 \text{ k}\Omega$,	C _L = 100 pF,	Fast		1	3	
ts(FS)	Output settling time, full scale	See Note 11		Slow		3	10	μs
4	Output cottling time and to and	$R_L = 10 \text{ k}\Omega$,	C _L = 100 pF,	Fast	1			_
ts(CC)	Output settling time, code to code	See Note 12		Slow		2		μs
O.D.	Olemente	$R_L = 10 \text{ k}\Omega$, C		Fast		3		\// -
SR	Slew rate	See Note 13		Slow		0.5		V/μs
	Glitch energy	$\frac{DIN}{CS} = 0 \text{ to } 1,$ $\overline{CS} = V_{DD}$	FCLK = 100 kH		5		nV-s	
SNR	Signal-to-noise ratio				52	54		
SINAD	Signal-to-noise + distortion	f _S = 102 kSPS,	$f_{\text{out}} = 1 \text{ kHz},$ $C_{\text{L}} = 100 \text{ pF}$		48	49		dB
THD	Total harmonic distortion	$R_L = 10 \text{ k}\Omega$,				-50	-48	
SFDR	Spurious free dynamic range			48	50			

NOTES: 11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0xFDF and 0xFDF to 0x020 respectively. Not tested, assured by design.



^{12.} Settling time is the time for the output signal to remain within \pm 0.5 LSB of the final measured value for a digital input code change of one count. Not tested, assured by design.

^{13.} Slew rate determines the time it takes for a change of the DAC output from 10% to 90% of full-scale voltage.

digital input timing requirements

		MIN	NOM	MAX	UNIT
t _{su(CS-CK)}	Setup time, CS low before first negative SCLK edge	10			ns
t _{su(C16-CS)}	Setup time, 16 th negative SCLK edge before CS rising edge	10			ns
t _{wH}	SCLK pulse width high	25			ns
t _{wL}	SCLK pulse width low	25			ns
t _{su(D)}	Setup time, data ready before SCLK falling edge	10			ns
t _{h(D)}	Hold time, data held valid after SCLK falling edge	10			ns

timing requirements

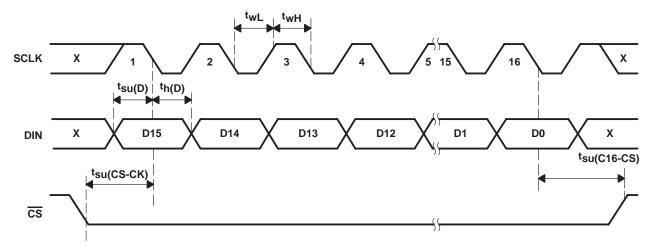


Figure 1. Timing Diagram



TYPICAL CHARACTERISTICS

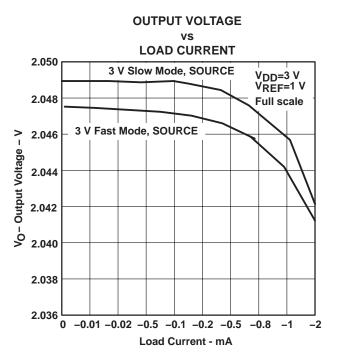


Figure 2

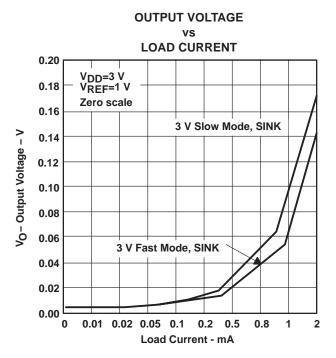


Figure 4

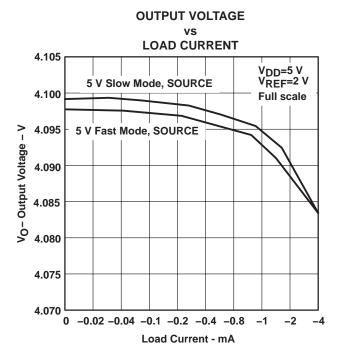


Figure 3

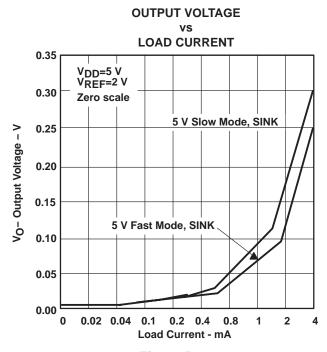
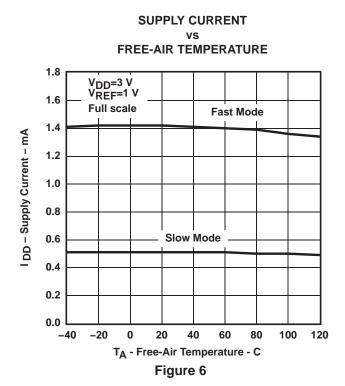
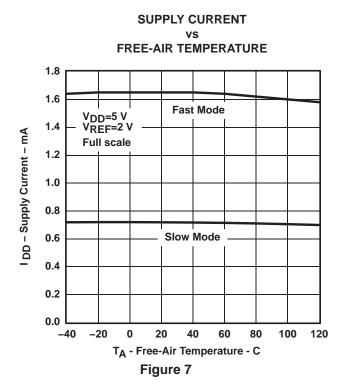
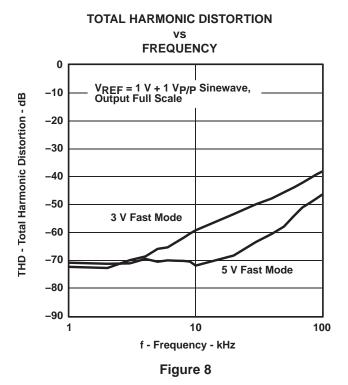


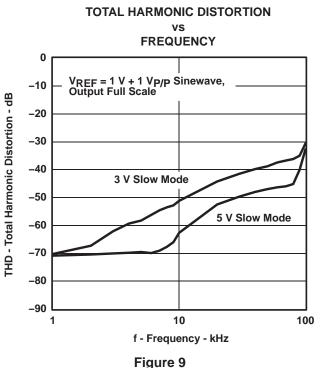
Figure 5

TYPICAL CHARACTERISTICS









TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY vs DIGITAL OUTPUT CODE

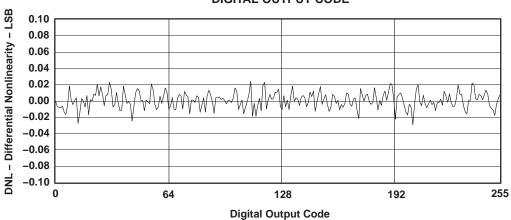


Figure 10

INTEGRAL NONLINEARITY vs DIGITAL OUTPUT CODE

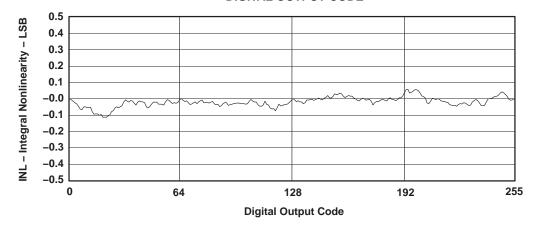


Figure 11

2.7-V TO 5.5-V LOW-POWER DUAL 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN

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APPLICATION INFORMATION

general function

The TLV5625 is a dual 8-bit, single-supply DAC, based on a resistor-string architecture. It consists of a serial interface, a speed and power-down control logic, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by the reference) is given by:

$$2 REF \frac{CODE}{2^n} [V]$$

Where REF is the reference voltage and CODE is the digital input value within the range of 0₁₀ to 2ⁿ–1, where n=8 (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the *data format* section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

serial interface

A falling edge of \overline{CS} starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or \overline{CS} rises, the content of the shift register is moved to the target latches (DAC A, DAC B, BUFFER, CONTROL), depending on the control bits within the data word.

Figure 2 shows examples of how to connect the TLV5625 to TMS320, SPI™, and Microwire™.

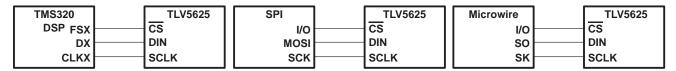


Figure 12. Three-Wire Interface

Notes on SPI[™] and Microwire[™]: Before the controller starts the data transfer, the software has to generate a falling edge on the pin connected to \overline{CS} . If the word width is 8 bits (SPI[™] and Microwire[™]) two write operations must be performed to program the TLV5625. After the write operation(s), the holding registers or the control register are updated automatically on the 16th positive clock edge.

serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$\rm f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 20 \; MHz$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16 \left(t_{whmin} + t_{wlmin} \right)} = 1.25 \text{ MHz}$$

Note that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5625 should also be considered.



APPLICATION INFORMATION

data format

The 16-bit data word for the TLV5625 consists of two parts:

• Program bits (D15..D12)

New data (D11..D4)

١	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
١	R1	SPD	PWR	R0	MSB			8 Dat	a bits			LSB	0	0	0	0

SPD: Speed control bit $1 \rightarrow$ fast mode $0 \rightarrow$ slow mode PWR: Power control bit $1 \rightarrow$ power down $0 \rightarrow$ normal operation On power up, SPD and PWD are reset to 0 (slow mode and normal operation)

The following table lists all possible combination of register-select bits:

register-select bits

R1	R0	REGISTER
0	0	Write data to DAC B and BUFFER
0	1	Write data to BUFFER
1	0	Write data to DAC A and update DAC B with BUFFER content
1	1	Reserved

The meaning of the 12 data bits depends on the register. If one of the DAC registers or the BUFFER is selected, then the 12 data bits determine the new DAC value:

examples of operation

Set DAC A output, select fast mode:

Write new DAC A value and update DAC A output:

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ſ	1	1	0	0			Nev	v DAC A	output va	alue			0	0	0	0

The DAC A output is updated on the rising clock edge after D0 is sampled.

Set DAC B output, select fast mode:

Write new DAC B value to BUFFER and update DAC B output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0		New E	BUFFER	content a	and DAC	B output	value		0	0	0	0

The DAC A output is updated on the rising clock edge after D0 is sampled.

- Set DAC A value, set DAC B value, update both simultaneously, select slow mode:
 - 1. Write data for DAC B to BUFFER:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1				New DAC	CB value				0	0	0	0

2. Write new DAC A value and update DAC A and B simultaneously:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0		New DAC A value								0	0	0



2.7-V TO 5.5-V LOW-POWER DUAL 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN

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APPLICATION INFORMATION

examples of operation (continued)

Both outputs are updated on the rising clock edge after D0 from the DAC A data word is sampled.

Set power-down mode:

ĺ	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ſ	Х	Х	1	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х

X = Don't care

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 13.

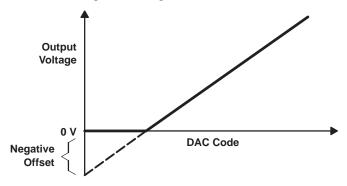


Figure 13. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

power-supply bypassing and ground management

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane, making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1- μF ceramic-capacitor bypass should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 14 shows the ground plane layout and bypassing technique.



APPLICATION INFORMATION

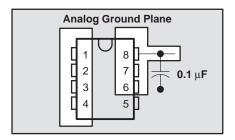


Figure 14. Power-Supply Bypassing

definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

zero-scale error (E_{7S})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (E_G)

Gain error is the error in slope of the DAC transfer function.

signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

SFDR is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental signal and is expressed in decibels.

2.7-V TO 5.5-V LOW-POWER DUAL 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN

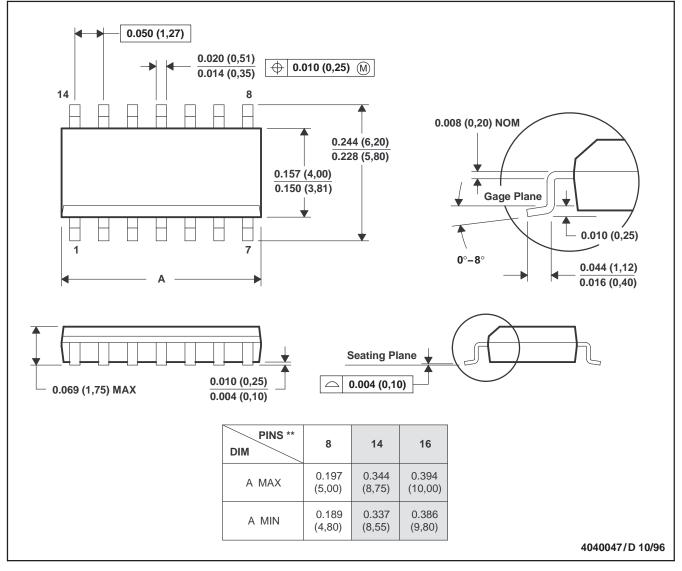
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MECHANICAL DATA

D (R-PDSO-G**)

14 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
TLV5625CD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5625
TLV5625CD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5625
TLV5625CDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5625
TLV5625CDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5625
TLV5625ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5625
TLV5625ID.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5625
TLV5625IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5625
TLV5625IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5625

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5625CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV5625IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5625CDR	SOIC	D	8	2500	350.0	350.0	43.0
TLV5625IDR	SOIC	D	8	2500	350.0	350.0	43.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV5625CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV5625CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLV5625ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV5625ID.A	D	SOIC	8	75	505.46	6.76	3810	4

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