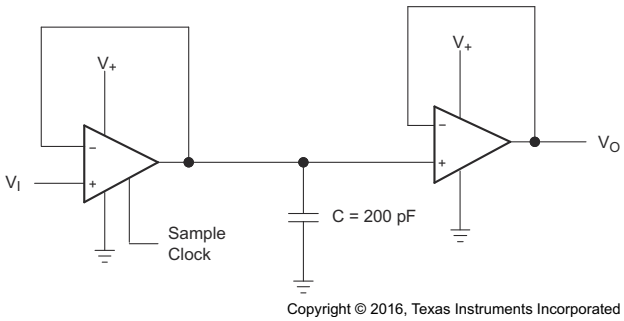
TLV34xx Low-Voltage Rail-to-Rail Output CMOS Operational Amplifiers With Shutdown

1 Features

- 1.8V and 5V performance
- Low offset (A grade)
  - 1.25mV maximum (25°C)
  - 1.7mV maximum (–40°C to 125°C)
- Rail-to-rail output swing
- Wide common-mode input voltage range: –0.2V to (V_+ – 0.5V)
- Input bias current: 1pA (typical)
- Input offset voltage: 0.3mV (typical)
- Low supply current: 70µA/channel
- Low shutdown current: 10pA (typical) per channel
- Gain bandwidth: 2.3MHz (typical)
- Slew rate: 0.9V/µs (typical)
- Turnon time from shutdown: 5µs (typical)
- Input referred voltage noise (at 10kHz): 20nV/$\sqrt{\text{Hz}}$
- ESD protection exceeds JESD 22:
  - 2000V Human-Body Model (HBM)
  - 750V Charged-device model (CDM)

2 Applications

- Cellular phones
- Consumer electronics (laptops)
- Audio preamplifier for voice
- Portable and battery-powered electronic equipment
- Supply current monitoring
- Battery monitoring
- Buffers
- Filters



Sample and Hold Circuit Using Two TLV341

3 Description

The TLV34xx devices are single and dual CMOS operational amplifiers, respectively, with low-voltage, low-power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultra-low input bias current of 1pA (typical) and an offset voltage of 0.3mV (typical). For applications requiring excellent dc precision, the A grade (TLV34xA) has a low offset voltage of 1.25mV (maximum) at 25°C.

These single-supply amplifiers are designed specifically for ultra-low-voltage (1.5V to 5V) operation, with a common-mode input voltage range that typically extends from –0.2V to 0.5V from the positive supply rail.

The TLV341 (single) and TLV342 (dual) in the RUG package also offer a shutdown (SHDN) pin that can be used to disable the device. In shutdown mode, the supply current is reduced to 45pA (typical). Offered in both the SOT-23 and smaller SC70 packages, the TLV341 is an excellent choice for the most space-constrained applications. The dual TLV342 is offered in the standard SOIC, VSSOP, and X2QFN packages.

An extended industrial temperature range from –40°C to 125°C makes the TLV34xx flexible for use in a wide variety of commercial and industrial applications.

Package Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
TLV341	(SOT-23, 6)	2.90mm × 1.60mm
	(SC70, 6)	2.00mm × 1.25mm
	(SOT, 6)	1.60mm × 1.20mm
TLV342	(SOIC, 8)	4.90mm × 3.91mm
	(VSSOP, 8)	3.00mm × 3.00mm
	(X2QFN, 10)	1.50mm × 2.00mm
TLV342S	(X2QFN, 10)	1.50mm × 2.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Pin Configuration and Functions

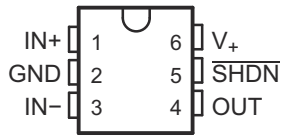


Figure 4-1. TLV341 DBV or DCK Package, 6-Pin SOT-23 or SC70 (Top View)

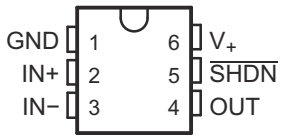


Figure 4-2. TLV341 DRL Package, 6-Pin SOT (Top View)

Table 4-1. Pin Functions: TLV341

PIN			I/O	DESCRIPTION
NAME	SOT-23, SC70	SOT		
1IN+	1	2	I	Noninverting input on channel 1
1IN–	3	3	I	Inverting input on channel 1
1OUT	4	4	O	Output on channel 1
GND	2	1	—	Ground
$\overline{SHDN}$	5	5	I	Shutdown active low
V_+	6	6	—	Positive power supply

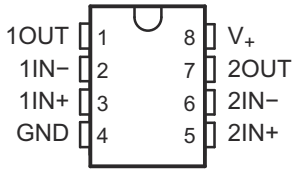


Figure 4-3. TLV342 D or DGK Package, 10-Pin SOIC or VSSOP (Top View)

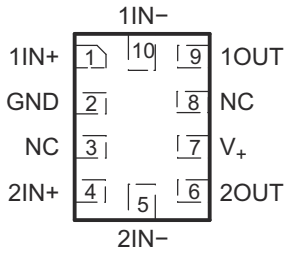


Figure 4-4. TLV342 RUG Package, 10-Pin X2QFN (Top View)

Table 4-2. Pin Functions: TLV342

PIN			I/O	DESCRIPTION
NAME	SOIC, VSSOP	X2QFN		
1IN+	3	1	I	Noninverting input on channel 1
1IN–	2	10	I	Inverting input on channel 1
1OUT	1	9	O	Output on channel 1
2IN+	5	4	I	Noninverting input on channel 2
2IN–	6	5	I	Inverting input on channel 2
2OUT	7	6	O	Output on channel 2
GND	4	2	—	Ground
NC(1)	—	3, 8	—	Not connected
V_+	8	7	—	Positive power supply

(1) NC – No internal connection

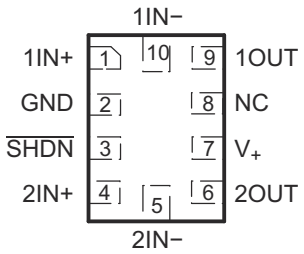


Figure 4-5. TLV342S RUG Package, 10-Pin X2QFN (Top View)

Table 4-3. Pin Functions: TLV342S

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN+	1	I	Noninverting input on channel 1
1IN–	10	I	Inverting input on channel 1
1OUT	9	O	Output on channel 1
2IN+	4	I	Noninverting input on channel 2
2IN–	5	I	Inverting input on channel 2
2OUT	6	O	Output on channel 2
GND	2	—	Ground
NC(1)	8	—	Not connected
$\overline{SHDN}$	3	I	Shutdown active low
V_+	7	—	Positive power supply

(1) NC – No internal connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_+	Supply voltage(2)	–0.3	5.5	V
V_{ID}	Differential input voltage(3)		±5.5	V
V_I	Input voltage (either input or $\overline{\text{shutdown}}$)	–0.3	5.5	V
V_O	Output voltage	–0.3	V_{CC} + 0.3	V
T_J	Operating virtual-junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values (except differential voltages) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN−.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_+	Supply voltage (single-supply operation)	1.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

5.4 Thermal Information: TLV341

THERMAL METRIC(1)		TLV341			UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	
		6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.4	196.8	221.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	145.6	82.4	109.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.1	95.2	111.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	34.1	1.8	6.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.4	93.2	109.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Thermal Information: TLV342

THERMAL METRIC[1]		TLV342			UNIT
		D (SOIC)	DGK (MSOP)	RUG (X2QFN)	
		8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123.6	192.3	167	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.8	78.2	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.9	112.6	94.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.4	15.2	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.4	111.2	94	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.6 Thermal Information: TLV342S

THERMAL METRIC[1]		TLV342S	UNIT
		RUG (X2QFN)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	87	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.7 Electrical Characteristics: V_+ = 1.8V

V_+ = 1.8V, GND = 0V, V_{IC} = V_O = V_+/2, R_L > 1MΩ (unless otherwise noted). See *Section 5.9*.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP[1]	MAX	UNIT
V_{IO}	Input offset voltage	Standard grade		25°C		0.3	4	mV
				Full range			4.5	
		A grade		25°C		0.3	1.25	
				0°C to 125°C		0.3	1.5	
				–40°C to 125°C		0.3	1.7	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		1.9		µV/°C
I_{IB}	Input bias current			25°C		1	100	pA
				–40°C to 85°C			375	
				–40°C to 125°C			3000	
I_{IO}	Input offset current			25°C		6.6		fA
CMRR	Common-mode rejection ratio	0 ≤ V_{ICR} ≤ 1.2V		25°C	60	85		dB
				Full range	50			
k_{SVR}	Supply-voltage rejection ratio	1.8V ≤ V_+ ≤ 5V		25°C	75	95		dB
				Full range	65			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 60dB		25°C	0		1.2	V
A_V	Large-signal voltage gain[2]	R_L = 10kΩ to 1.35V		25°C	70	110		dB
				Full range	60			
		R_L = 2kΩ to 1.35V		25°C	65	100		
				Full range	55			
V_O	Output swing (delta from supply rails)	R_L = 2kΩ to 1.35V	Low level	25°C		22	50	mV
				Full range			75	
			High level	25°C		25	50	
				Full range			75	
		R_L = 10kΩ to 1.35V	Low level	25°C		14	20	
				Full range			25	
			High level	25°C		7	20	
				Full range			25	
I_{CC}	Supply current (per channel)			25°C		150	200	µA
				Full range			210	
I_{OS}	Output short-circuit current	Sourcing		25°C	6	12		mA
		Sinking			10	20		
SR	Slew rate	R_L = 10kΩ[3]		25°C		0.9		V/µs
GBW	Unity-gain bandwidth	R_L = 10kΩ, C_L = 200pF		25°C		2.2		MHz
φ_m	Phase margin	R_L = 100kΩ, C_L = 200pF		25°C		55		°
G_m	Gain margin	R_L = 100kΩ, C_L = 200pF		25°C		15		dB
V_n	Equivalent input noise voltage	f = 1kHz		25°C		33		nV/√Hz
I_n	Equivalent input noise current	f = 1kHz		25°C		0.001		pA/√Hz
THD	Total harmonic distortion	f = 1kHz, A_V = 1, R_L = 600Ω, V_I = 1 V_{PP}		25°C		0.015%		

(1) Typical values represent the most likely parametric norm.
(2) GND + 0.2V ≤ V_O ≤ V_+ – 0.2V
(3) Connected as voltage follower with 2V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

5.8 Electrical Characteristics: V_+ = 5V

V_+ = 5V, GND = 0V, V_{IC} = V_O = V_+/2, R_L > 1MΩ (unless otherwise noted). See *Section 5.10*.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP[1]	MAX	UNIT
V_{IO}	Input offset voltage	Standard grade		25°C		0.3	4	mV
				Full range			4.5	
		A grade		25°C		0.3	1.25	
				0°C to 125°C		0.3	1.5	
				–40°C to 125°C		0.3	1.7	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		1.9		µV/°C
I_{IB}	Input bias current			25°C		1	200	pA
				–40°C to 85°C			375	
				–40°C to 125°C			3000	
I_{IO}	Input offset current			25°C		6.6		fA
CMRR	Common-mode rejection ratio	0 ≤ V_{ICR} ≤ 4.4V		25°C	75	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio	1.8V ≤ V_+ ≤ 5V		25°C	75	95		dB
				Full range	65			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 70dB		25°C	0		4.4	V
A_V	Large-signal voltage gain[2]	R_L = 10kΩ to 2.5V		25°C	80	110		dB
				Full range	70			
		R_L = 2kΩ to 2.5V		25°C	75	105		
				Full range	60			
V_O	Output swing (delta from supply rails)	R_L = 2kΩ to 2.5V	Low level	25°C		40	60	mV
				Full range			85	
			High level	25°C		25	60	
				Full range			85	
		R_L = 10kΩ to 2.5V	Low level	25°C		18	30	
				Full range			40	
			High level	25°C		7	15	
				Full range			20	
I_{CC}	Supply current (per channel)			25°C		150	200	µA
				Full range			215	
I_{OS}	Output short-circuit current	Sourcing		25°C	60	113		mA
		Sinking			80	115		
SR	Slew rate	R_L = 10kΩ[3]		25°C		1		V/µs
GBW	Unity-gain bandwidth	R_L = 10kΩ, C_L = 200pF		25°C		2.3		MHz
φ_m	Phase margin	R_L = 100kΩ, C_L = 200pF		25°C		55		°
G_m	Gain margin	R_L = 100kΩ, C_L = 200pF		25°C		15		dB
V_n	Equivalent input noise voltage	f = 1kHz		25°C		33		nV/√Hz
I_n	Equivalent input noise current	f = 1kHz		25°C		0.001		pA/√Hz
THD	Total harmonic distortion	f = 1kHz, A_V = 1, R_L = 600Ω, V_I = 1V_{PP}		25°C		0.012%		

5.9 Shutdown Characteristics: V_+ = 1.8V

V_+ = 1.8V, GND = 0V, V_{IC} = V_O = V_+/2, R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode	V_{SD} = 0V	25°C		0.01	1	µA
			Full range			1.5	
$t_{(on)}$	Amplifier turnon time		25°C		5		µs
V_{SD}	Recommended shutdown pin voltage range	On mode	25°C	1.5		1.8	V
		Shutdown mode		0		0.2	

5.10 Shutdown Characteristics: V_+ = 5V

V_+ = 5V, GND = 0V, V_{IC} = V_O = V_+/2, R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode	V_{SD} = 0V	25°C		0.01	1	µA
			Full range			1.5	
$t_{(on)}$	Amplifier turnon time		25°C		5		µs
V_{SD}	Recommended shutdown pin voltage range	On mode	25°C	4.5		5	V
		Shutdown mode		0		0.2	

5.11 Typical Characteristics

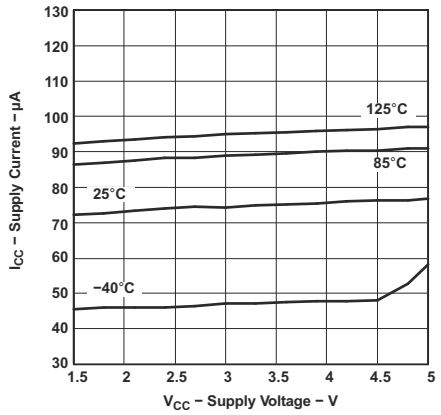


Figure 5-1. Supply Current vs Supply Voltage

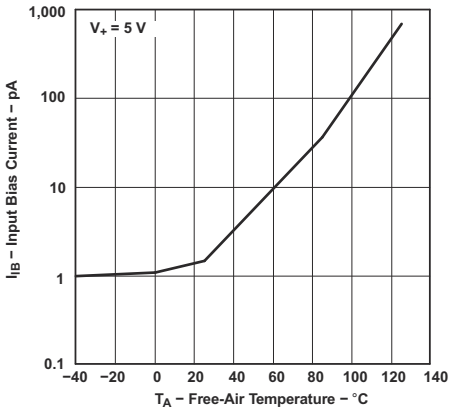


Figure 5-2. Input Bias Current vs Temperature

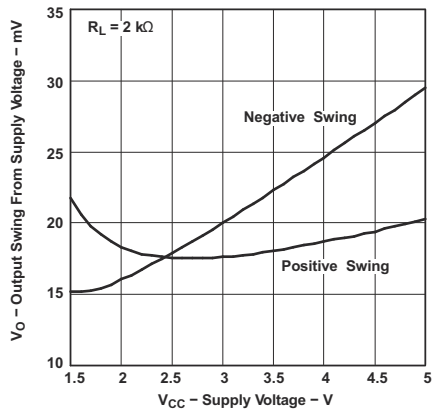


Figure 5-3. Output Voltage Swing vs Supply Voltage

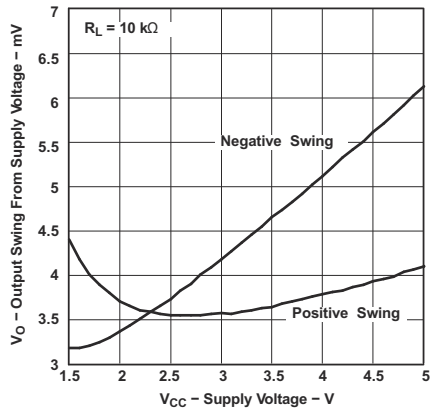


Figure 5-4. Output Voltage Swing vs Supply Voltage

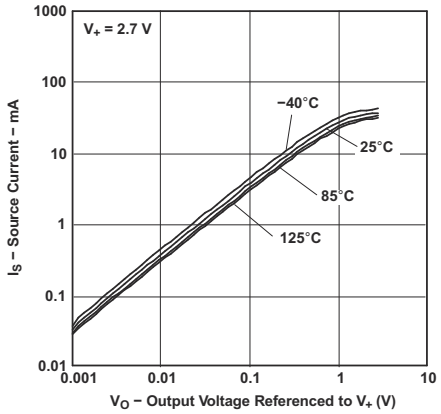


Figure 5-5. Source Current vs Output Voltage

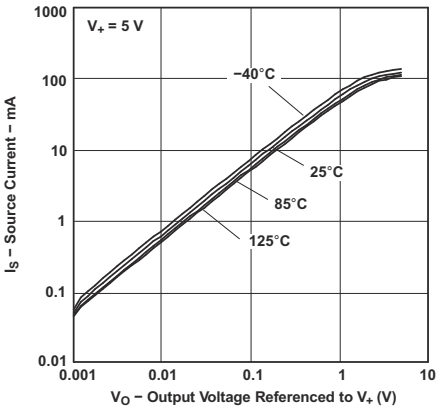


Figure 5-6. Source Current vs Output Voltage

5.11 Typical Characteristics (continued)

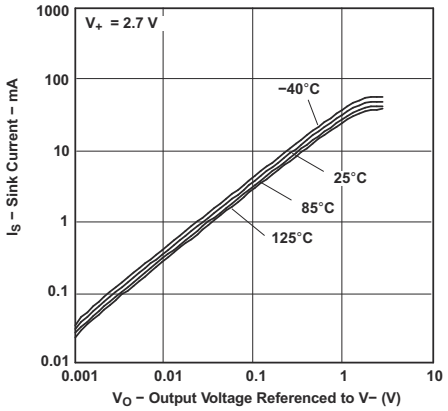


Figure 5-7. Sink Current vs Output Voltage

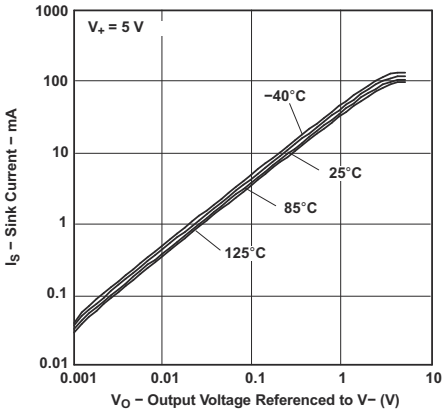


Figure 5-8. Sink Current vs Output Voltage

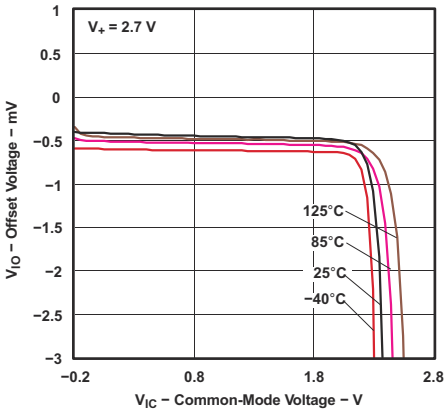


Figure 5-9. Offset Voltage vs Common-Mode Voltage

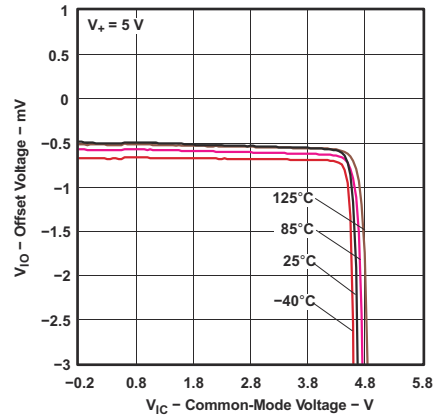


Figure 5-10. Offset Voltage vs Common-Mode Voltage

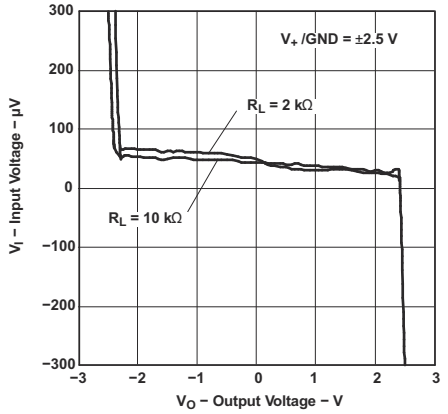


Figure 5-11. Input Voltage vs Output Voltage

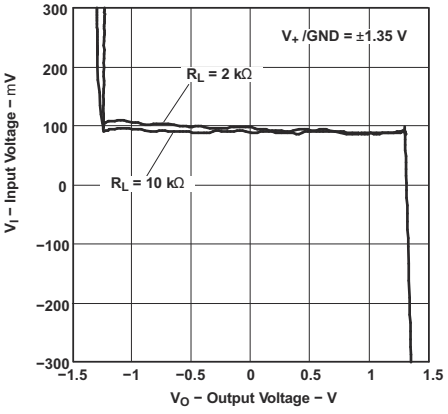


Figure 5-12. Input Voltage vs Output Voltage

5.11 Typical Characteristics (continued)

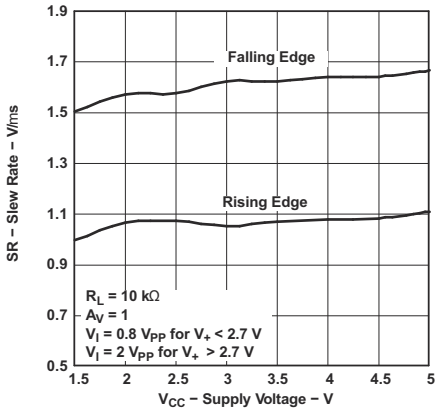


Figure 5-13. Slew Rate vs Supply Voltage

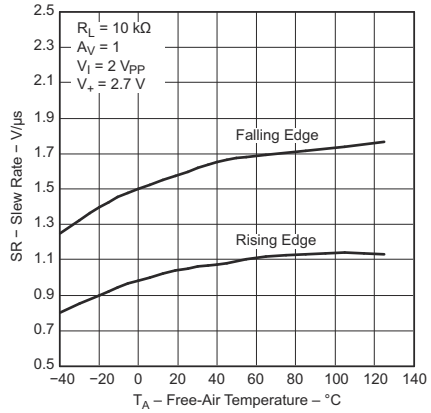


Figure 5-14. Slew Rate vs Temperature

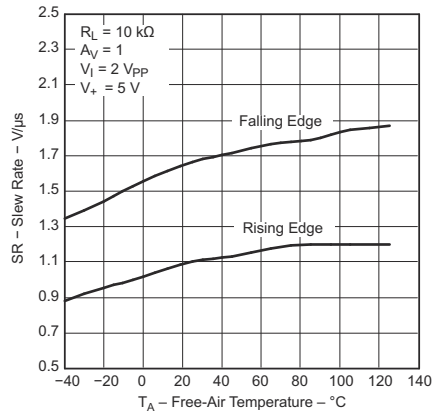


Figure 5-15. Slew Rate vs Temperature

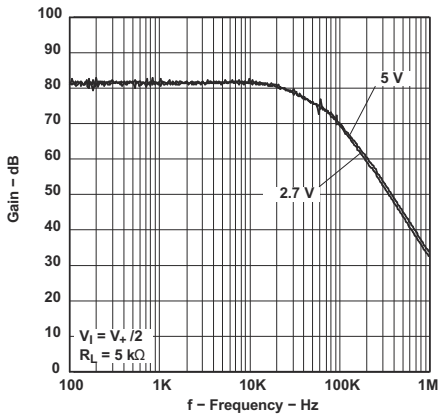


Figure 5-16. CMRR vs Frequency

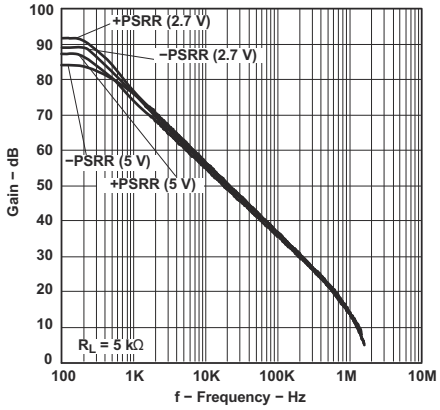


Figure 5-17. PSRR vs Frequency

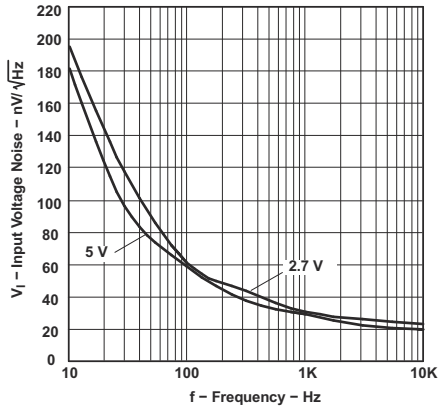


Figure 5-18. Input Voltage Noise vs Frequency

5.11 Typical Characteristics (continued)

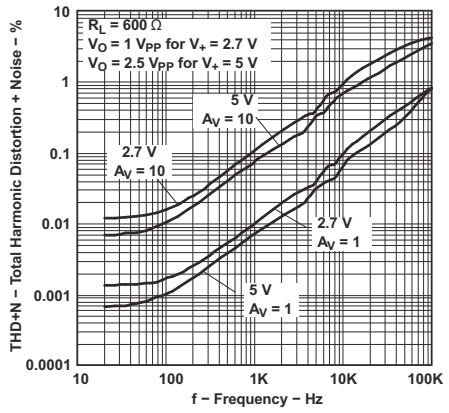


Figure 5-19. Total Harmonic Distortion +Noise vs Frequency

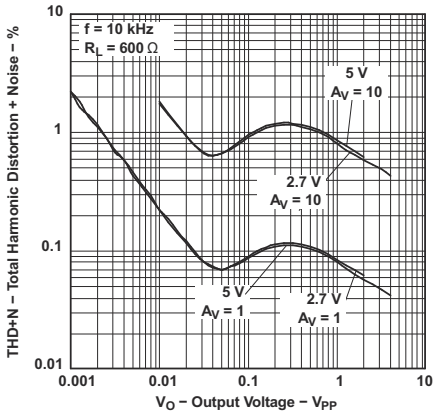


Figure 5-20. Total Harmonic Distortion +Noise vs Output Voltage

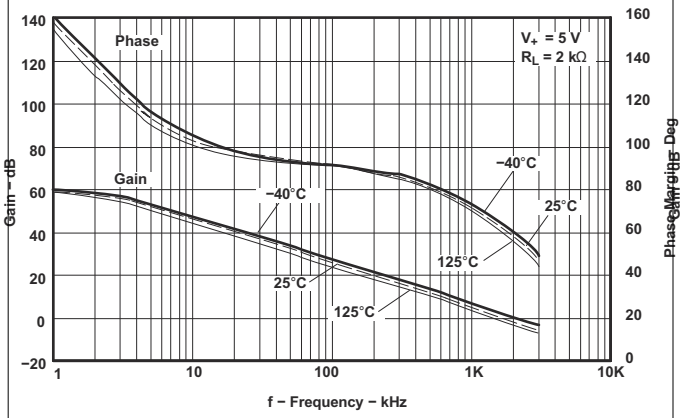


Figure 5-21. Frequency Response vs Temperature

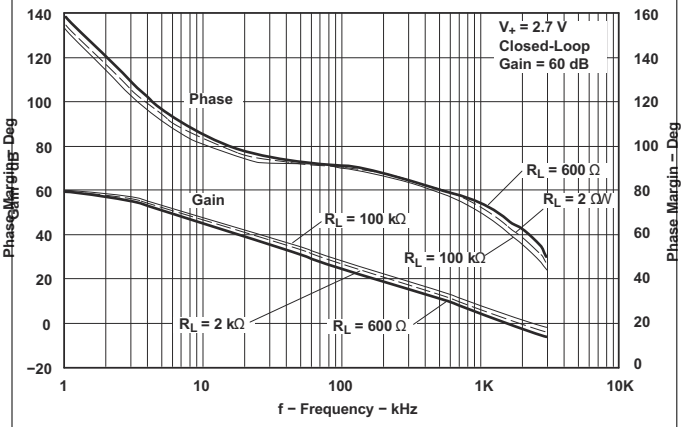


Figure 5-22. Frequency Response vs R_L

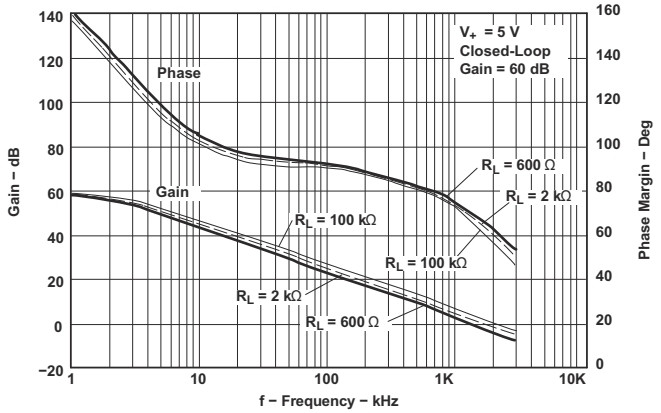


Figure 5-23. Frequency Response vs R_L

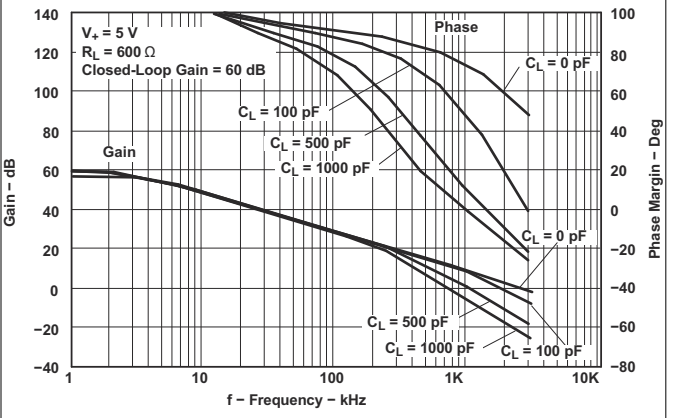


Figure 5-24. Frequency Response vs C_L

5.11 Typical Characteristics (continued)

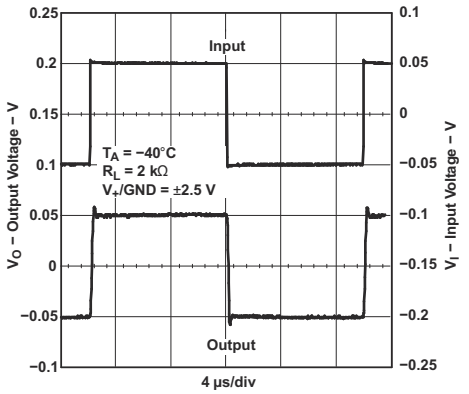


Figure 5-25. Small-Signal Noninverting Response

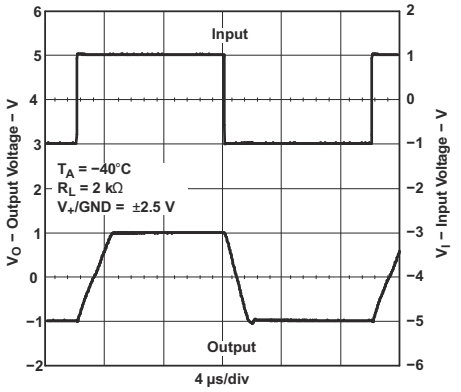


Figure 5-26. Large-Signal Noninverting Response

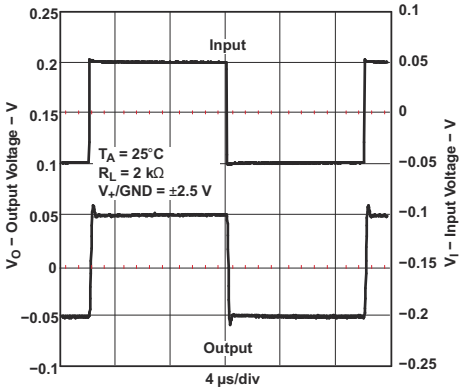


Figure 5-27. Small-Signal Noninverting Response

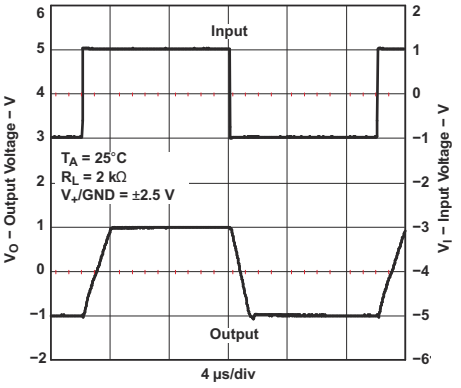


Figure 5-28. Large-Signal Noninverting Response

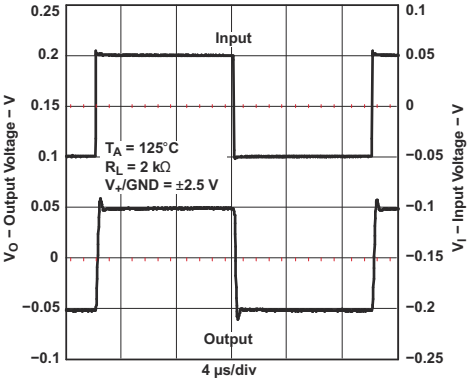


Figure 5-29. Small-Signal Noninverting Response

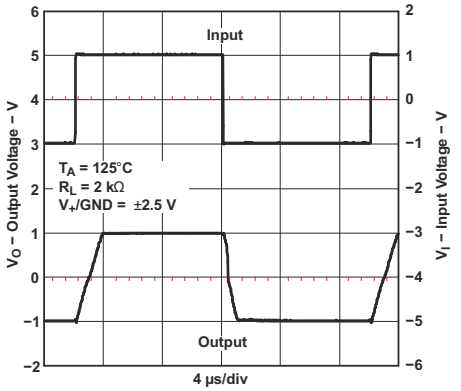


Figure 5-30. Large-Signal Noninverting Response

5.11 Typical Characteristics (continued)

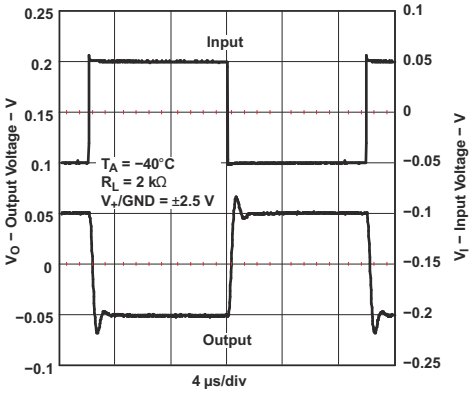


Figure 5-31. Small-Signal Noninverting Response

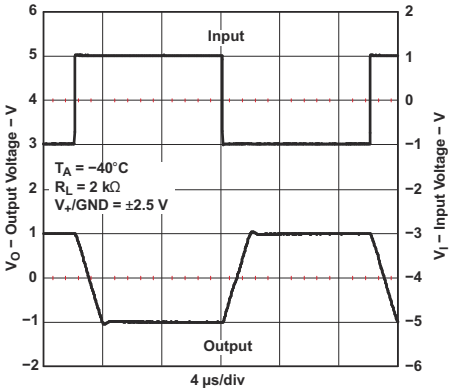


Figure 5-32. Large-Signal Inverting Response

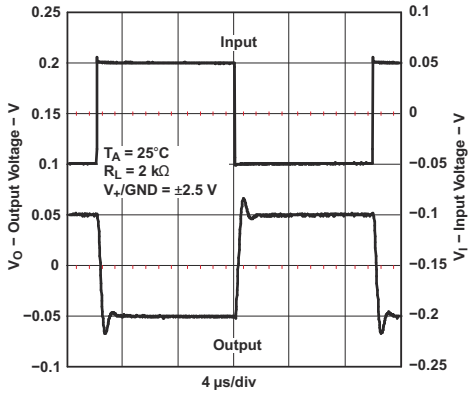


Figure 5-33. Small-Signal Inverting Response

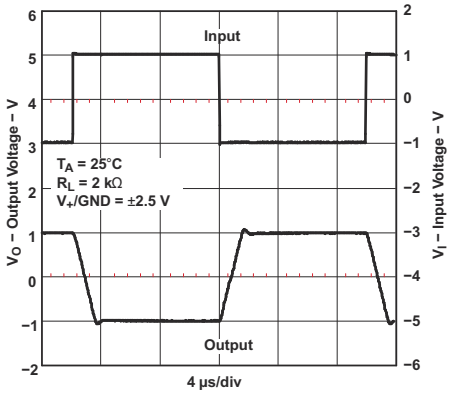


Figure 5-34. Large-Signal Inverting Response

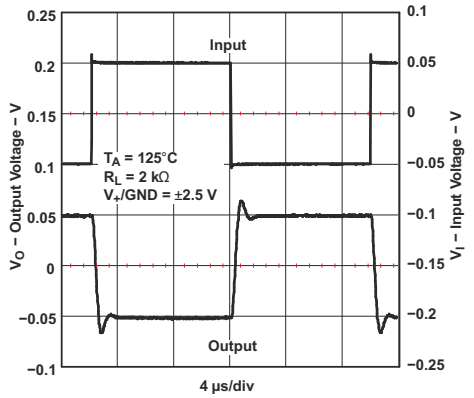


Figure 5-35. Small-Signal Inverting Response

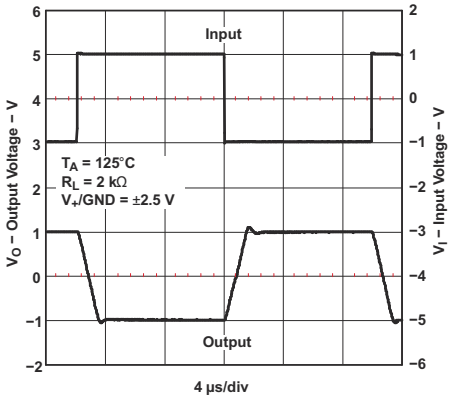


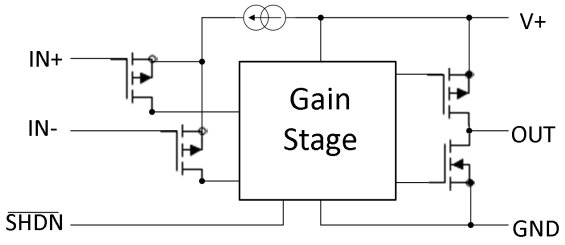
Figure 5-36. Large-Signal Inverting Response

6 Detailed Description

6.1 Overview

The TLV34xx devices are precision operational amplifiers with CMOS inputs for very low input bias current. Grade A devices offer lower V_{IO} for high accuracy in direct-coupled applications. Output is rail to rail and input common mode includes ground. TLV341 and TLV342S have shutdown mode for very low supply current.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 PMOS Input Stage

PMOS Input Stage supports a lower input range that includes ground. Upper range limit is VCC – 0.6V.

6.3.2 CMOS Output Stage

The CMOS drain output topology allows rail-to-rail output swing.

6.3.3 Shutdown

TLV341 and TLV342S include a shutdown pin. During shutdown, I_{CC} is nearly zero and the output becomes high impedance. The typical turnon time coming out of shutdown is 5µs.

6.4 Device Functional Modes

The TLV34xx devices have two operation modes:

- Normal operation when $\overline{SHDN}$ pin is at V_+ level or the $\overline{SHDN}$ pin is not present
- Shutdown mode when $\overline{SHDN}$ is at GND level; I_{CC} is very low and output is high impedance.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV34xx devices have rail-to-rail output and input range from ground to VCC – 0.6V. CMOS inputs provide very low input current. Shutdown capability is an option in dual amplifier version. Operation from 1.5V to 5.5V is possible.

7.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes outputs a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative voltages positive.

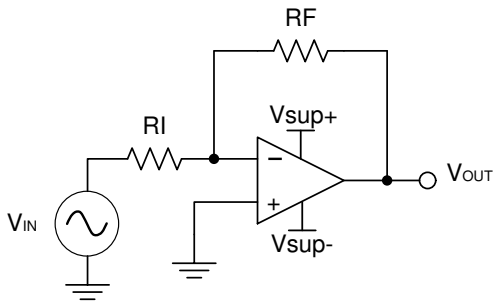


Figure 7-1. Application Schematic

7.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and output voltage range. For instance, this application scales a signal of ±0.5V to ±1.8V. Setting the supply at ± 2V is sufficient to accommodate this application. The supplies can power up in any order; however, neither supply can be of opposite polarity relative to ground at any time; otherwise, a large current can flow though the input ESD diodes. TI highly recommends adding a series resistor to the grounded input to limit current in such an occurrence. Vsup+ must be more positive than Vsup– at all times; otherwise, a large reverse supply current can flow.

7.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_V = \frac{VOUT}{VIN} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit uses currents in the mA range. This maintains that the part does not draw too much current. For this example, choose 10kΩ for RI, which means 36kΩ is used for RF. This is determined by Equation 3.

$$A_V = -\frac{RF}{RI} \tag{3}$$

7.2.3 Application Curve

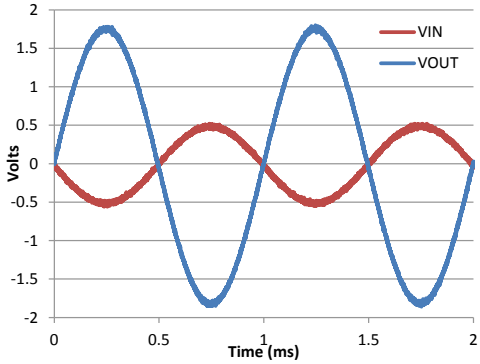


Figure 7-2. Input and Output Voltages of the Inverting Amplifier

7.3 Power Supply Recommendations

CAUTION

Supply voltages larger than 5.5V for a single supply can permanently damage the device (see the *Section 5.1*).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V_+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds while paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If not possible to keep them separate, cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Section 7.4.1* .
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

7.4.2 Layout Example

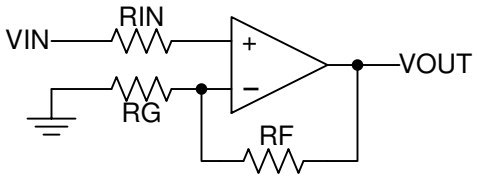


Figure 7-3. Layout Schematic

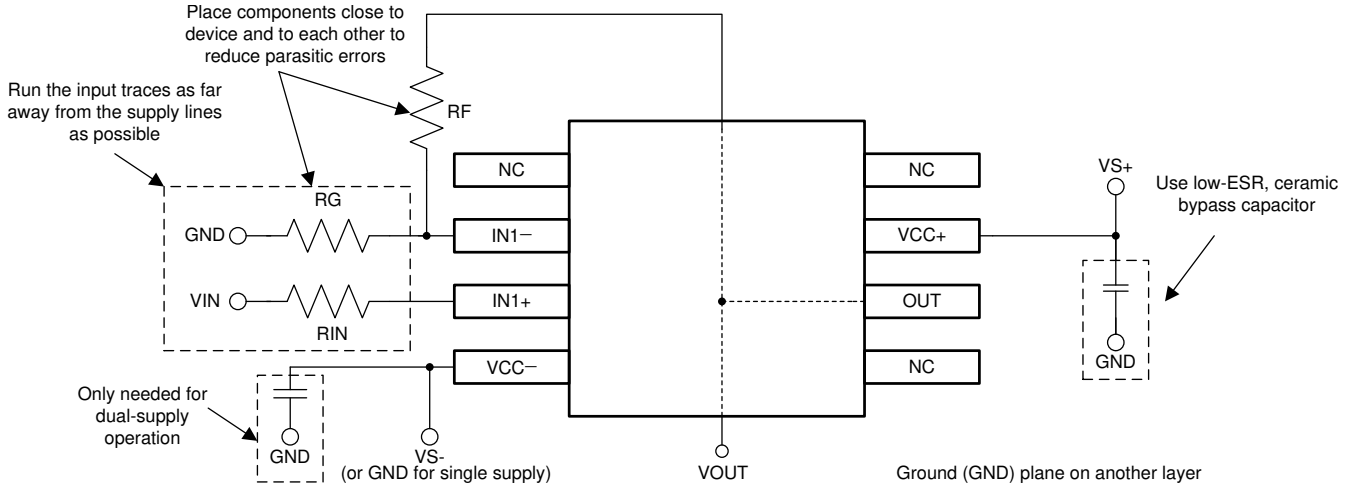


Figure 7-4. Operational Amplifier Schematic for Noninverting Configuration

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (February 2016) to Revision E (June 2025) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Changed typical supply current (per channel) at 25°C from 70µA to 150µA for both V_+ = 1.8V and V_+ = 5V supply voltages 7
- Changed maximum supply current (per channel) at 25°C from 150µA to 200µA for both V_+ = 1.8V and V_+ = 5V supply voltages 7
- Changed maximum supply current (per channel) at full temperature range and V_+ = 1.8V from 200µA to 210µA 7
- Changed maximum supply current (per channel) at full temperature range and V_+ = 5V from 200µA to 215µA. 8
- Changed maximum recommended shutdown pin voltage from 0.5V to 0.2V for both V_+ = 1.8V and V_+ = 5V supply voltages 9

Changes from Revision C (November 2007) to Revision D (February 2016) — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Removed DPK Package, and TLV344 part from the *Pin Configuration and Functions* table 3

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV341AIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YCGE
TLV341AIDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YCGE
TLV341AIDBVT	Obsolete	Production	SOT-23 (DBV) | 6	-	-	Call TI	Call TI	-40 to 125	YCGE
TLV341AIDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Y5E
TLV341AIDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Y5E
TLV341AIDCKT	Obsolete	Production	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 125	Y5E
TLV341IDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YC9E
TLV341IDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YC9E
TLV341IDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Y4E
TLV341IDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	Y4E
TLV341IDCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y4E
TLV341IDCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y4E
TLV341IDCKT	Obsolete	Production	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 125	Y4E
TLV341IDRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(Y4A, Y4W)
TLV341IDRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(Y4A, Y4W)
TLV342AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	TY342A
TLV342AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY342A
TLV342AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY342A
TLV342ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	TY342
TLV342IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	Y6A
TLV342IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	Y6A
TLV342IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY342
TLV342IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY342
TLV342IRUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(1S8, Y6E)
TLV342IRUGR.A	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(1S8, Y6E)
TLV342IRUGRG4	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1S8
TLV342IRUGRG4.A	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1S8
TLV342SIRUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(1OA, 2YE)
TLV342SIRUGR.A	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(1OA, 2YE)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV342SIRUGRG4	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OA
TLV342SIRUGRG4.A	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

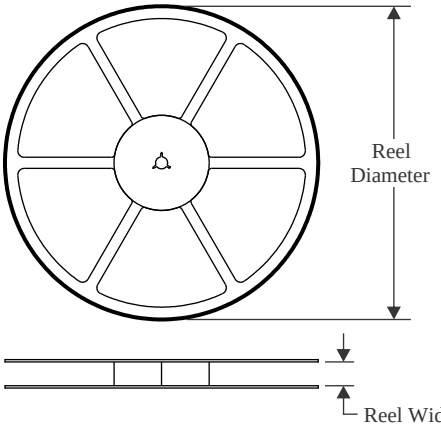
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

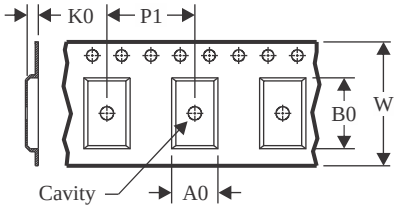
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

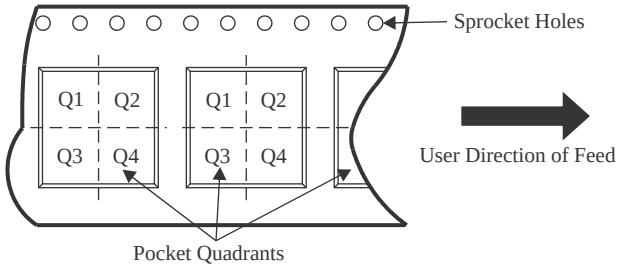


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

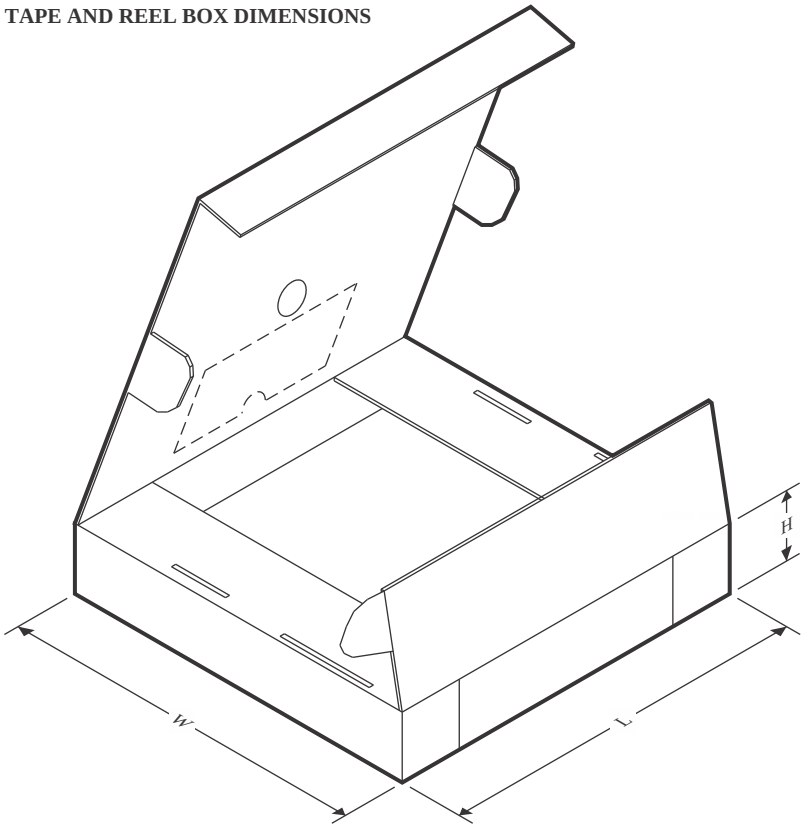
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV341AIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV341AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV341IDBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV341IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV341IDCKRG4	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV341IDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TLV342AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV342IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV342IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV342IRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
TLV342IRUGRG4	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
TLV342SIRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
TLV342SIRUGRG4	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

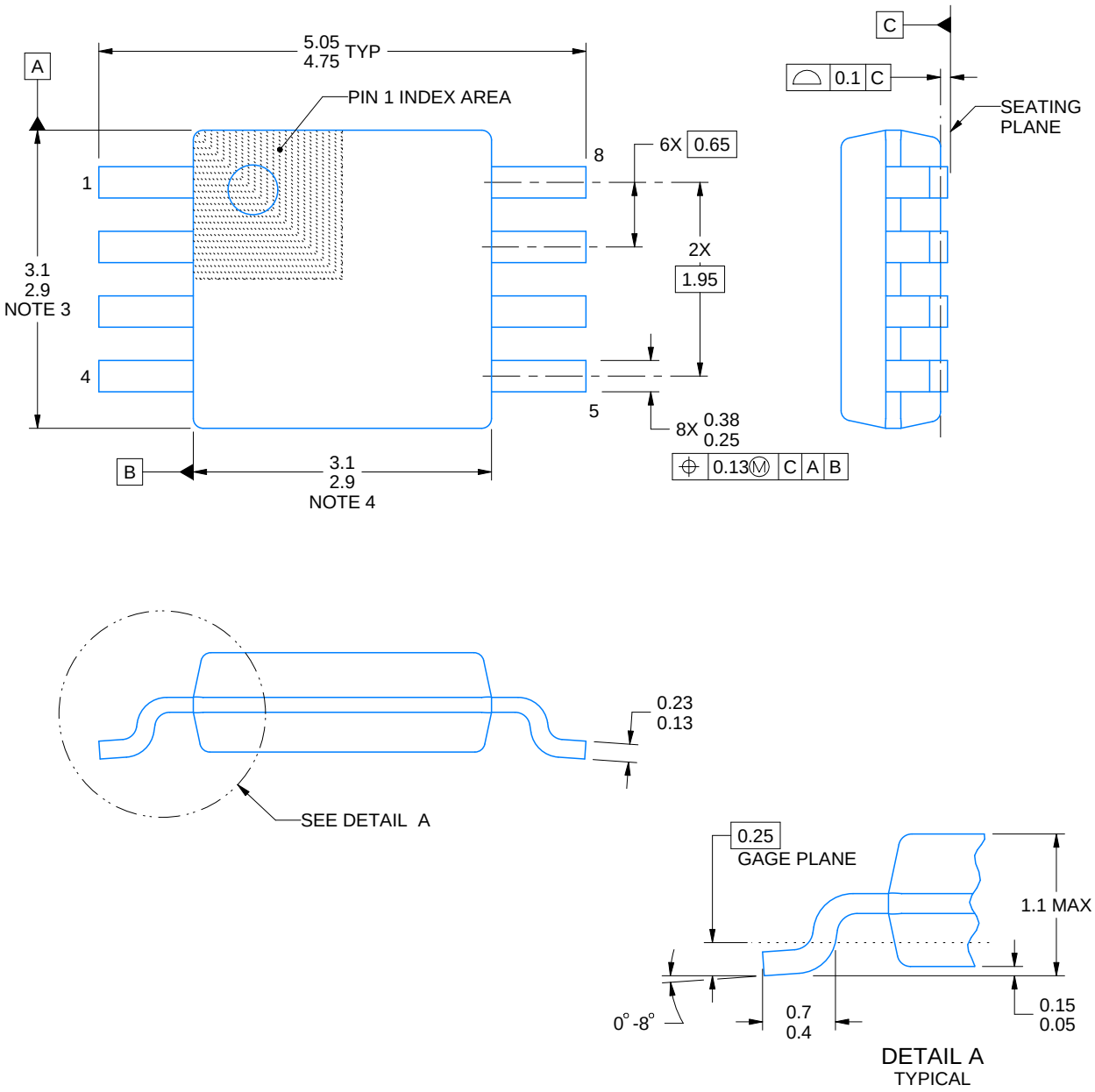
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV341AIDBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TLV341AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV341IDBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TLV341IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV341IDCKRG4	SC70	DCK	6	3000	200.0	183.0	25.0
TLV341IDRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
TLV342AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV342IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV342IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV342IRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
TLV342IRUGRG4	X2QFN	RUG	10	3000	210.0	185.0	35.0
TLV342SIRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
TLV342SIRUGRG4	X2QFN	RUG	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

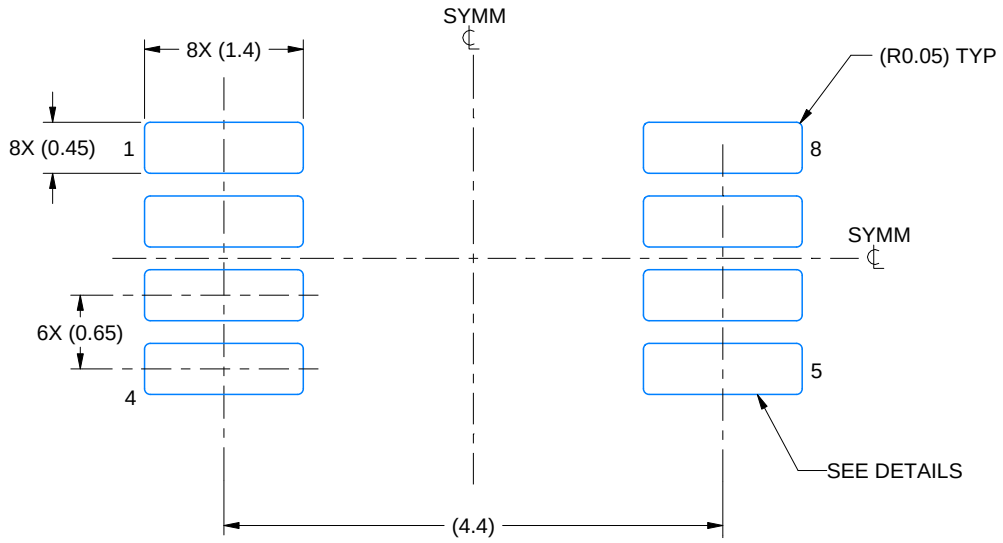
SMALL OUTLINE PACKAGE



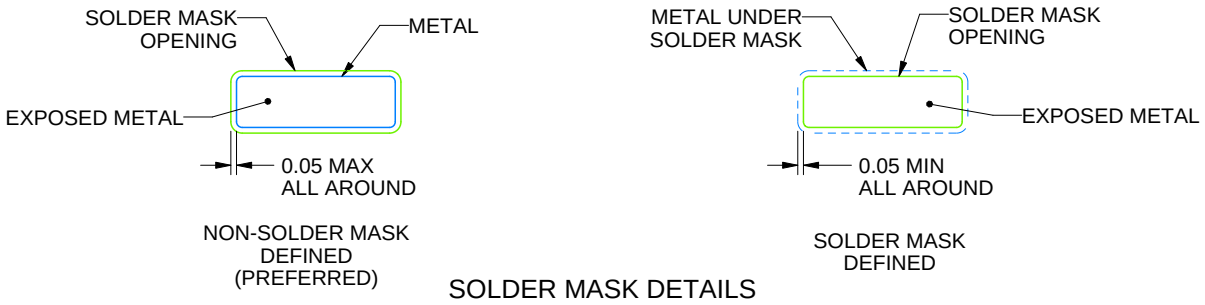
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

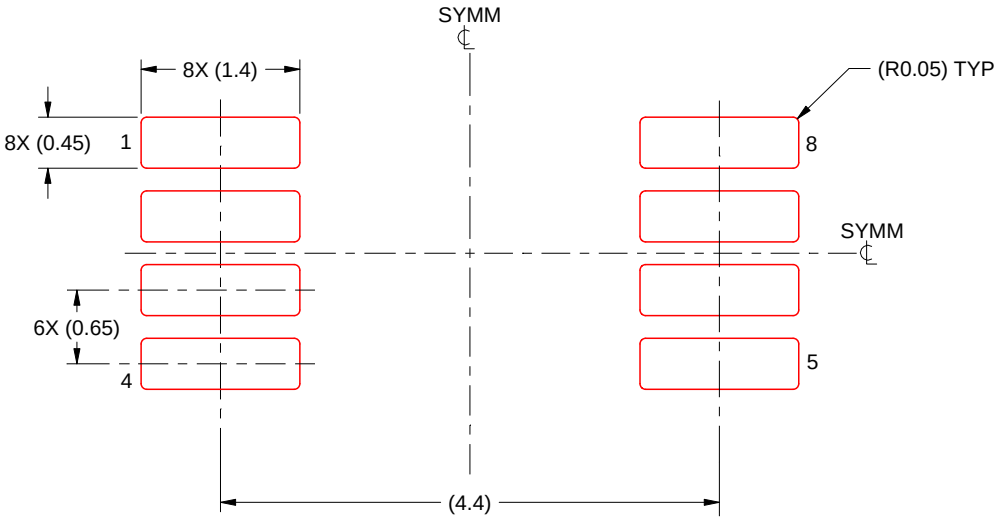


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

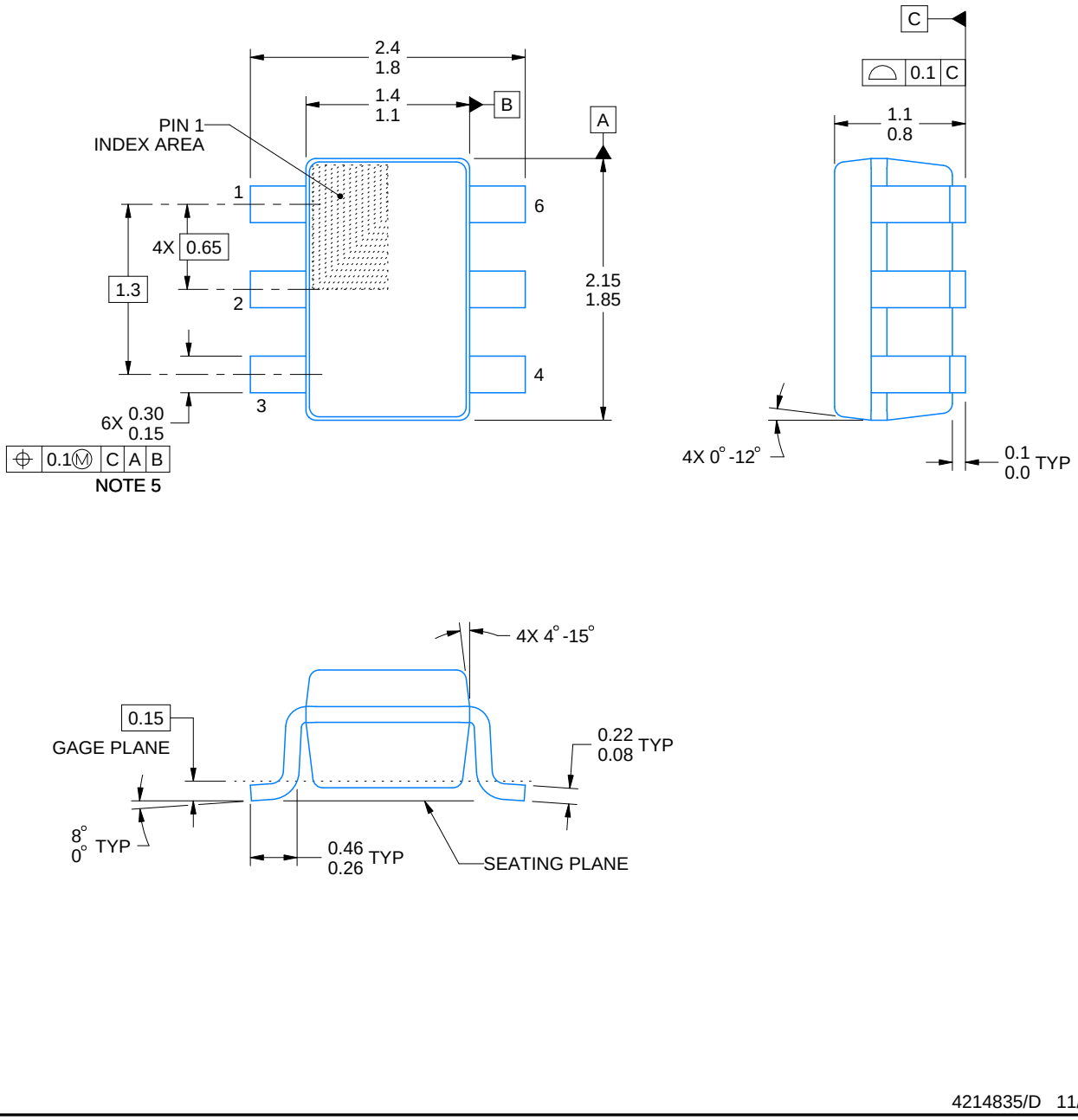
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

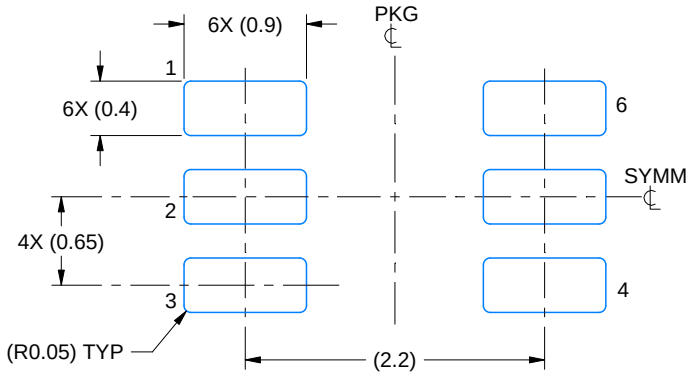
SMALL OUTLINE TRANSISTOR



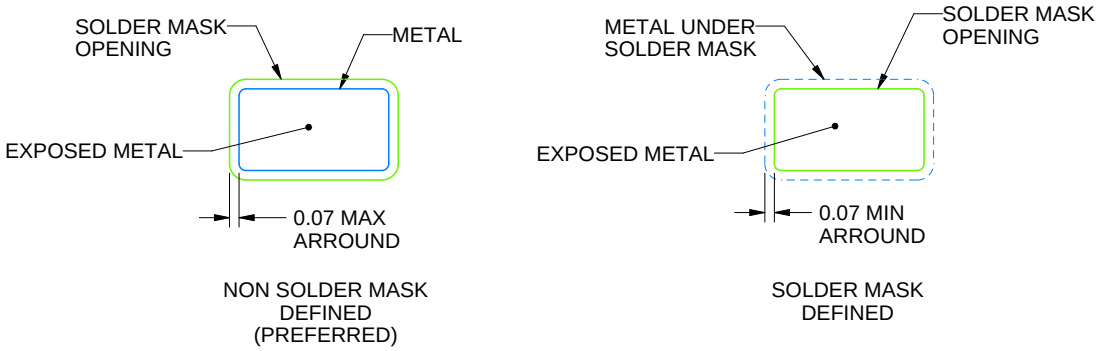
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

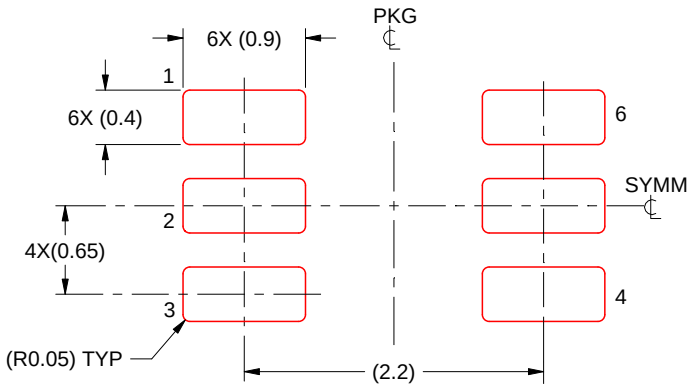


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

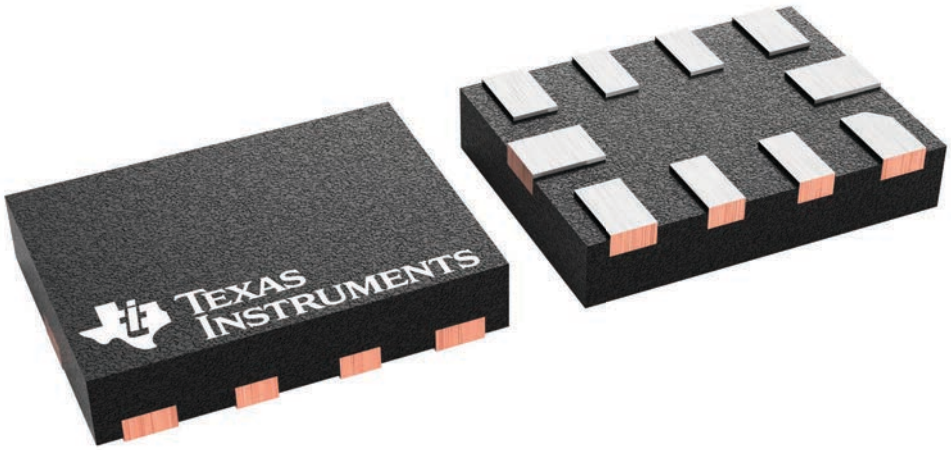
RUG 10

X2QFN - 0.4 mm max height

1.5 x 2, 0.5 mm pitch

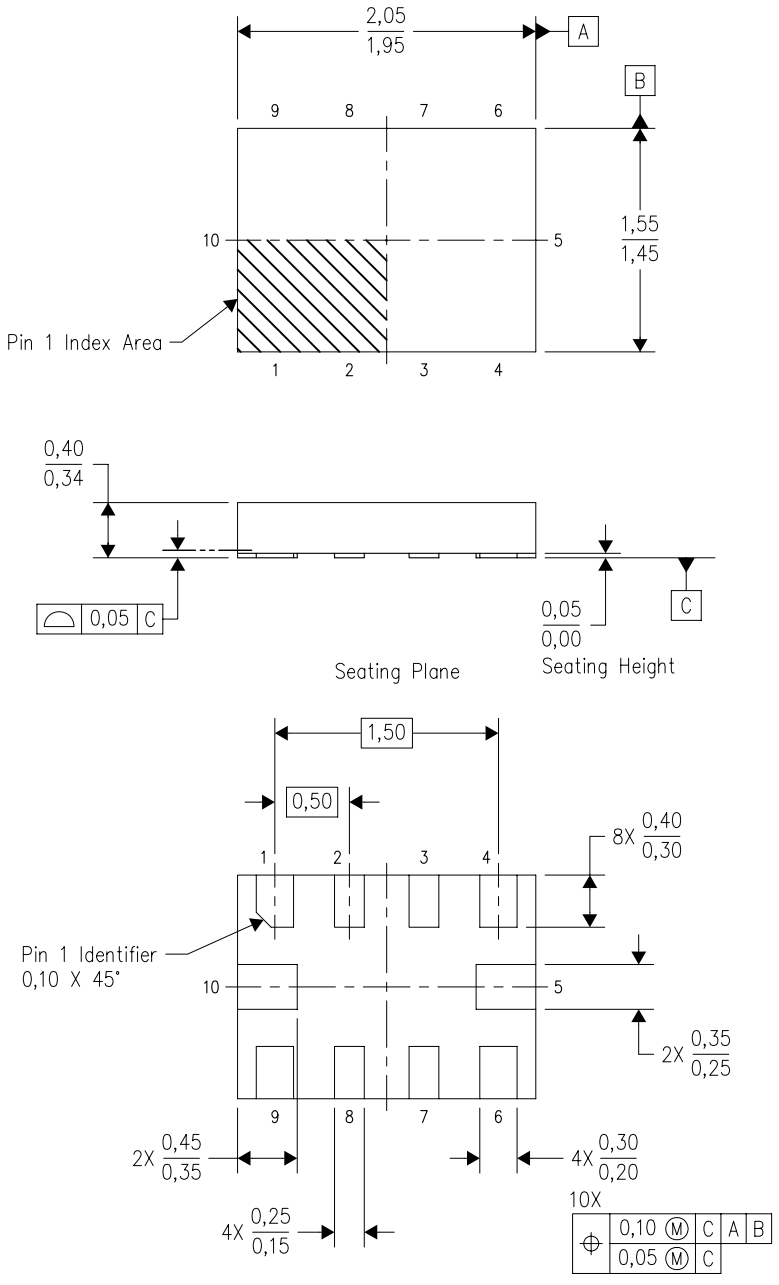
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231768/A

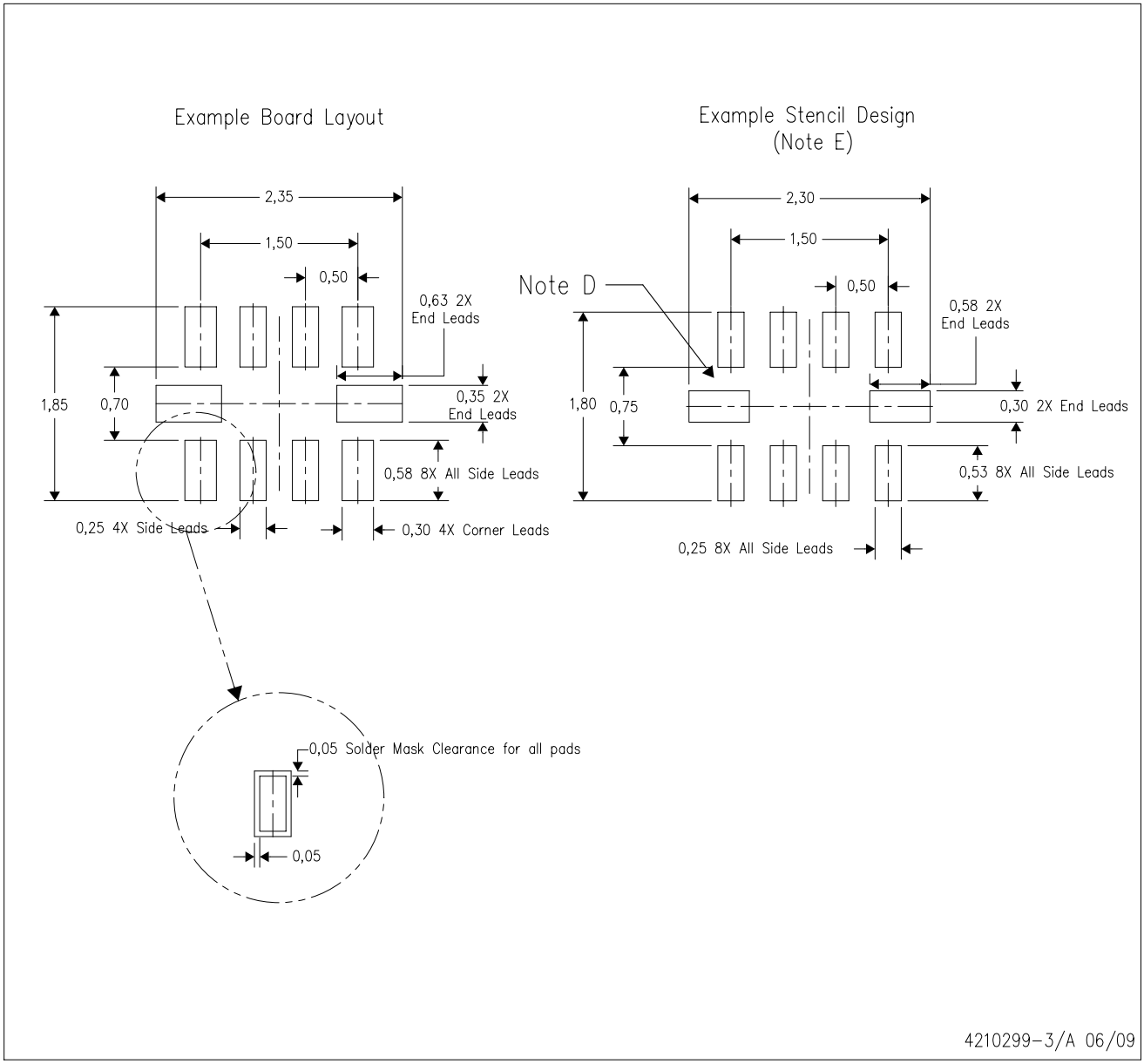
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)



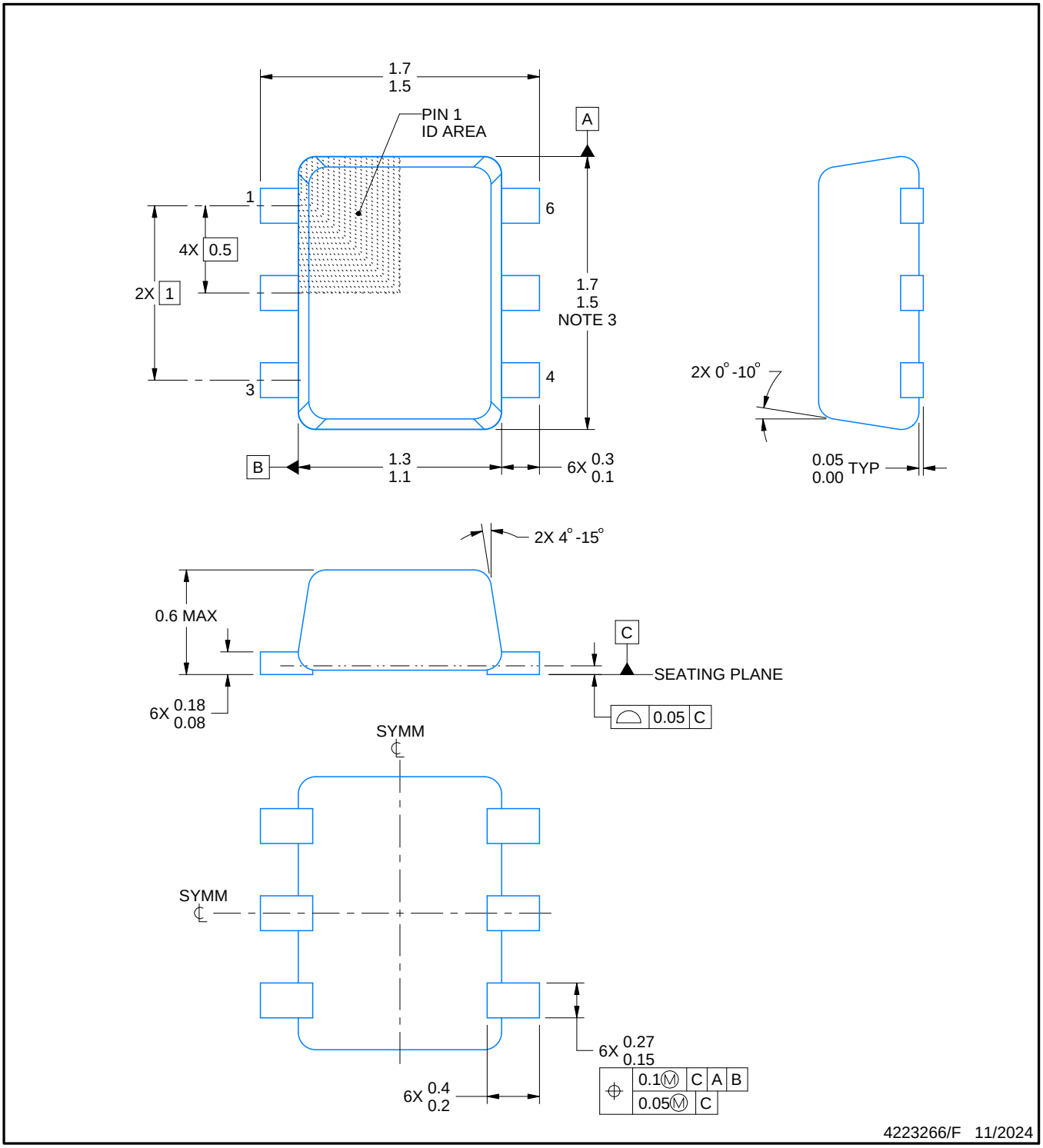
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

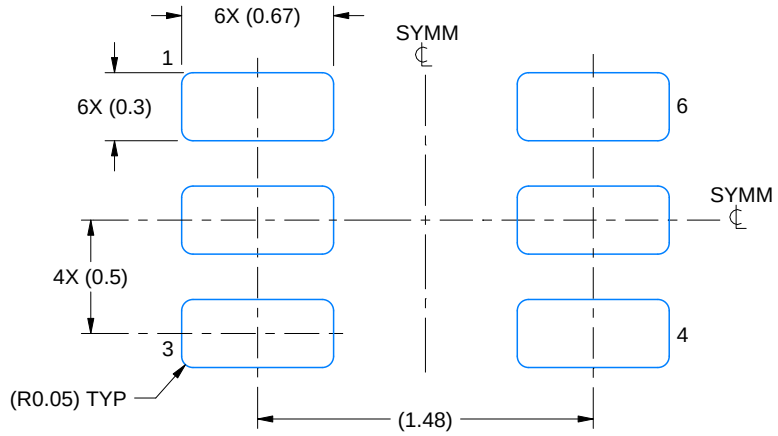
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

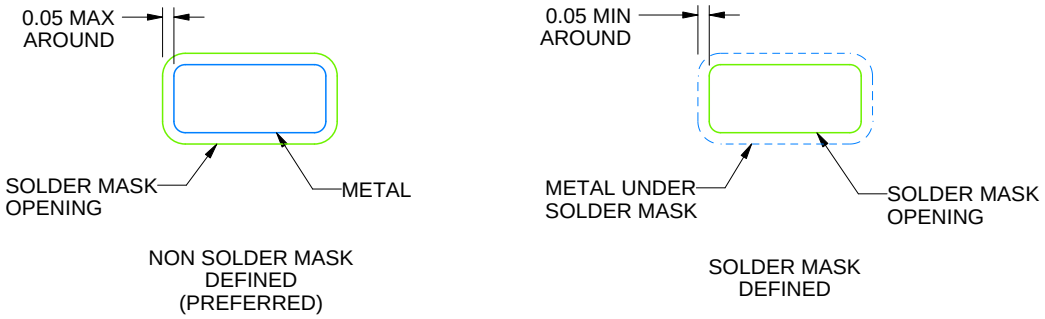
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

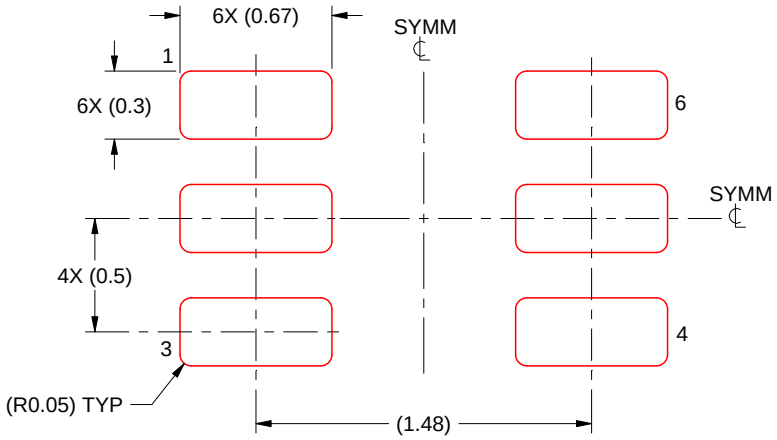
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

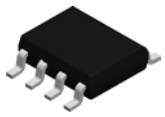


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

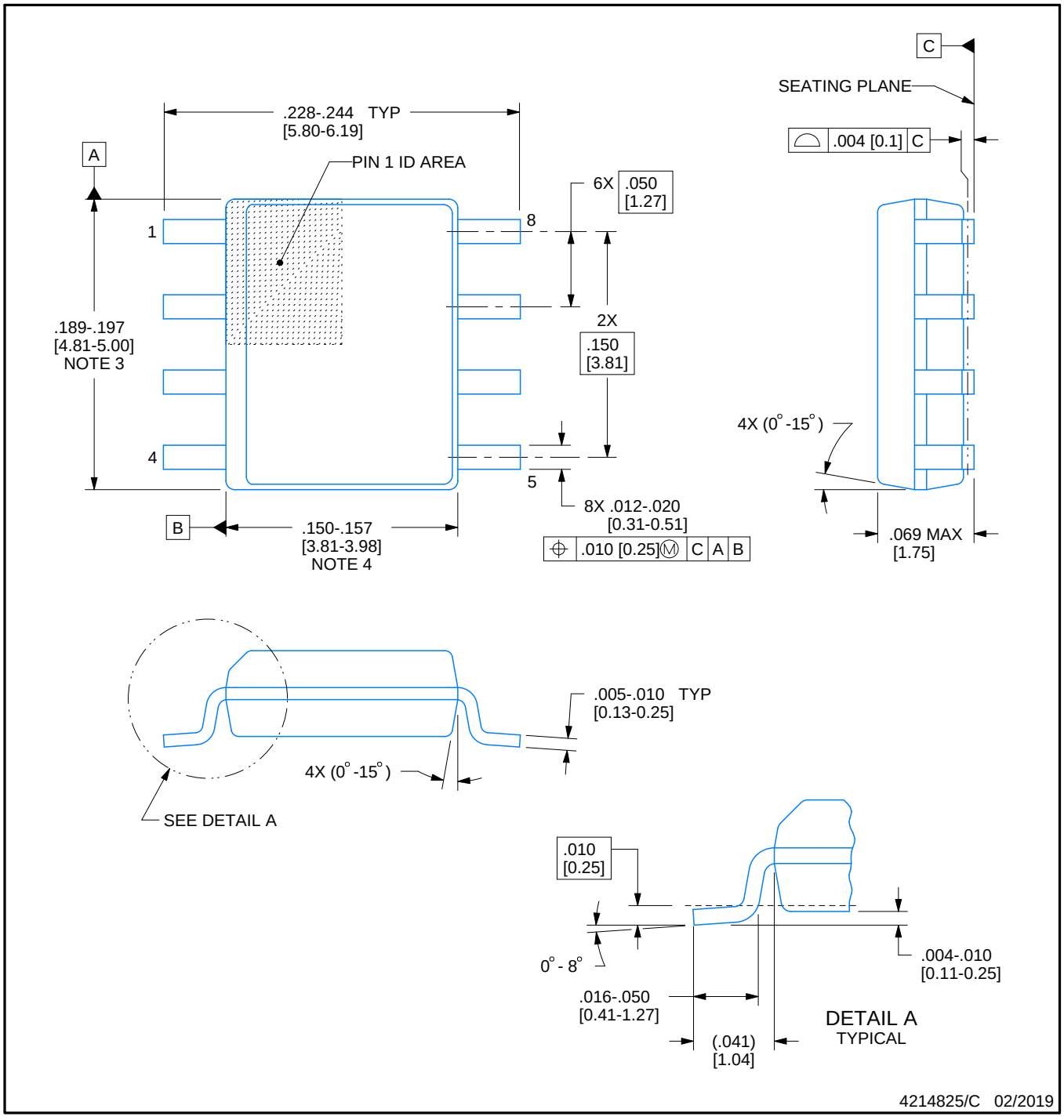


PACKAGE OUTLINE

D0008A

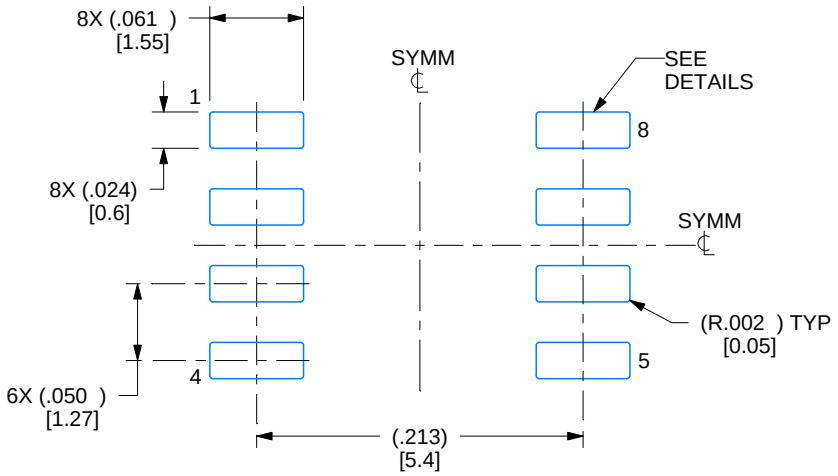
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

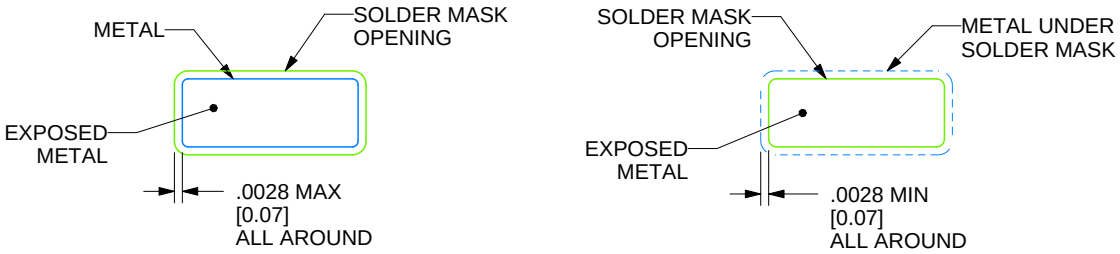


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

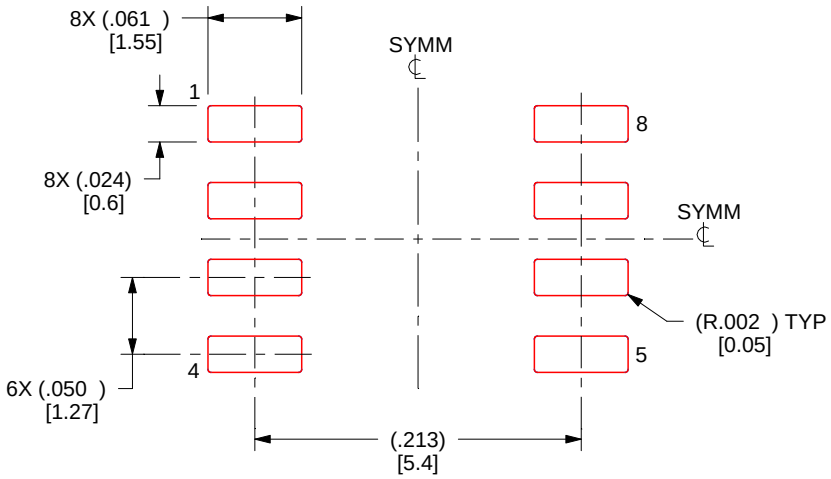
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

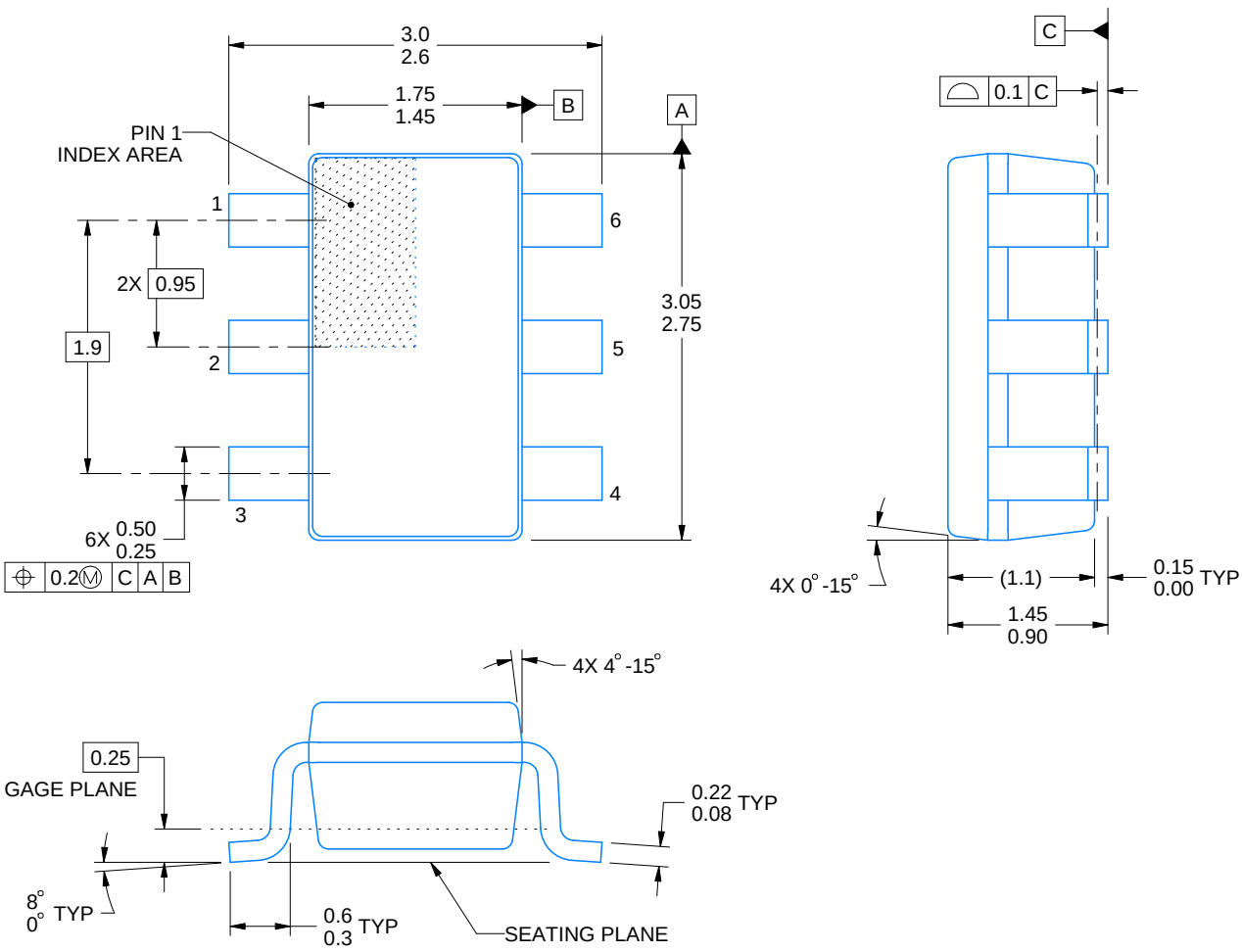
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

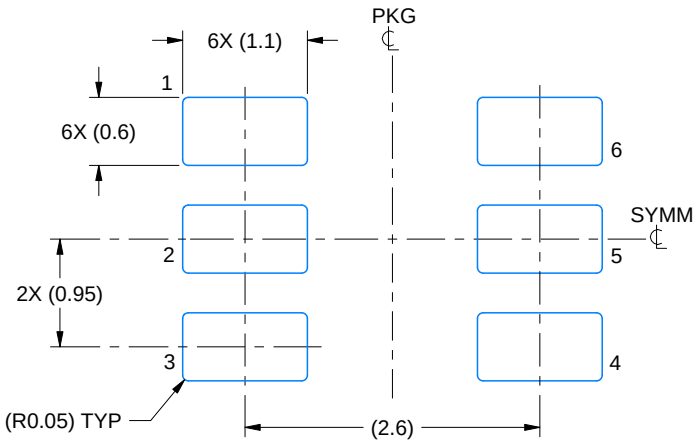
SMALL OUTLINE TRANSISTOR



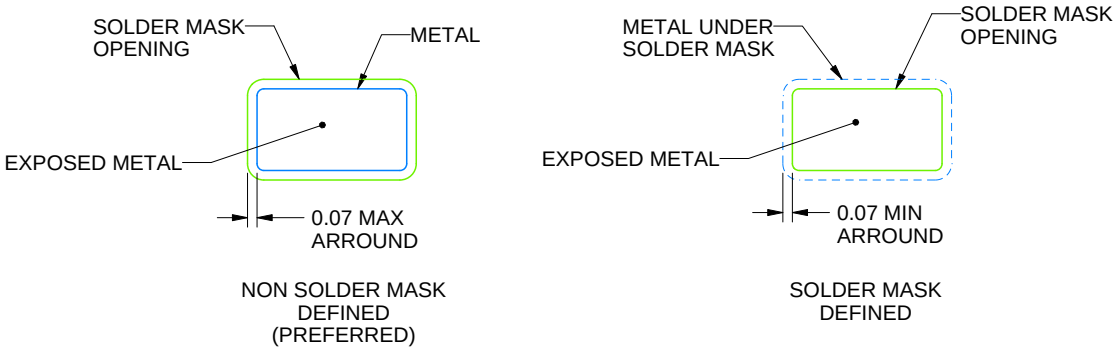
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

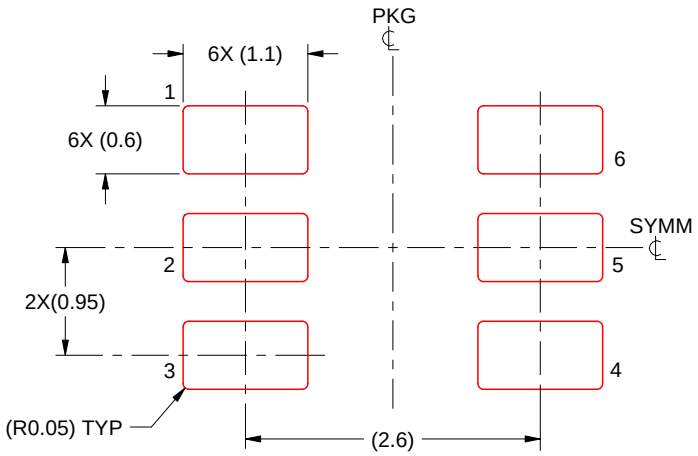


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025