

FAMILY OF MICROPOWER RAIL-TO-RAIL INPUT AND OUTPUT OPERATIONAL AMPLIFIERS

FEATURES

- **BiMOS Rail-to-Rail Input/Output**
- **Input Bias Current . . . 1 pA**
- **High Wide Bandwidth . . . 160 kHz**
- **High Slew Rate . . . 0.1 V/ μ s**
- **Supply Current . . . 7 μ A (per channel)**
- **Input Noise Voltage . . . 90 nV/ $\sqrt{\text{Hz}}$**
- **Supply Voltage Range . . . 2.7 V to 16 V**
- **Specified Temperature Range**
 - **–40°C to 125°C . . . Industrial Grade**
- **Ultra-Small Packaging**
 - **5 Pin SOT-23 (TLV2381)**

APPLICATIONS

- **Portable Medical**
- **Power Monitoring**
- **Low Power Security Detection Systems**
- **Smoke Detectors**

DESCRIPTION

The TLV238x single supply operational amplifiers provide rail-to-rail input and output capability. The TLV238x takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range, while adding the rail-to-rail output swing feature. The TLV238x also provides 160-kHz bandwidth from only 7 μ A. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from (± 8 V supplies down to ± 1.35 V) two rechargeable cells.

The combination of rail-to-rail inputs and outputs make them good upgrades for the TLC27Lx family—offering more bandwidth at a lower quiescent current. The offset voltage is lower than the TLC27LxA variant.

To maintain cost effectiveness the TLV2381/2 are only available in the extended industrial temperature range. This means that one device can be used in a wide range of applications that include PDAs as well as automotive sensor interface.

All members are available in SOIC, with the singles in the small SOT-23 package, duals in the MSOP.

SELECTION GUIDE

DEVICE	V _S [V]	I _Q /ch [μ A]	V _{ICR} [V]	V _{IO} [mV]	I _{IB} [pA]	GBW [MHz]	SLEW RATE [V/ μ s]	V _n , 1 kHz [nV/ $\sqrt{\text{Hz}}$]
TLV238x	2.7 to 16	10	–0.2 to V _S + 0.2	4.5	60	0.16	0.06	100
TLV27Lx	2.7 to 16	11	–0.2 to V _S – 1.2	5	60	0.16	0.06	100
TLC27Lx	4 to 16	17	–0.2 to V _S – 1.5	10/5/2	60	0.085	0.03	68
OPAx349	1.8 to 5.5	2	–0.2 to V _S + 0.2	10	10	0.070	0.02	300
OPAx347	2.3 to 5.5	34	–0.2 to V _S + 0.2	6	10	0.35	0.01	60
TLC225x	2.7 to 16	62.5	0 to V _S – 1.5	1.5/0.85	60	0.200	0.02	19

NOTE: All dc specs are maximums while ac specs are typicals.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	SYMBOL	SPECIFIED TEMPERATURE RANGE	ORDER NUMBER	TRANSPORT MEDIA
TLV2381ID	SOIC-8	D	2381I	–40°C to 125°C	TLV2381ID	Tube
					TLV2381IDR	Tape and Reel
TLV2381IDBV	SOT-23	DBV	VBKI		TLV2381IDBVR	Tape and Reel
					TLV2381IDBVT	
TLV2382ID	SOIC-8	D	2382I		TLV2382ID	Tube
					TLV2382IDR	Tape and Reel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_S	16.5 V
Input voltage, V_I (see Notes 1 and 2)	$V_S + 0.2$ V
Output current, I_O	100 mA
Differential input voltage, V_{ID}	V_S
Continuous total power dissipation	See Dissipation Rating Table
Maximum junction temperature, T_J	150°C
Operating free-air temperature range, T_A : I suffix	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Relative to GND pin.
2. Maximum is 16.5 V or $V_S + 0.2$ V whichever is the lesser value.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW	370 mW
DBV (5)	55	324.1	385 mW	201 mW
DBV (6)	55	294.3	425 mW	221 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, (V_S)	Dual supply	± 1.35	± 8	V
	Single supply	2.7	16	
Input common-mode voltage range		-0.2	$V_S + 0.2$	V
Operating free air temperature, T_A	I-suffix	-40	125	°C

electrical characteristics at recommended operating conditions, $V_S = 2.7$ V, 5 V, and 15 V (unless otherwise noted)

dc performance

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	V _{IC} = V _S /2, R _L = 100 kΩ V _O = V _S /2 R _S = 50 Ω		25°C		0.5	4.5	mV
				Full range			6.5	
α _{VIO}	Offset voltage drift			25°C		1.1		μV/°C
CMRR	Common-mode rejection ratio	V _{IC} = 0 V to V _S , R _S = 50 Ω	V _S = 2.7 V	25°C	54	69		dB
				Full range	53			
				25°C	71	86		
				Full range	70			
		V _{IC} = 0 V to V _S , R _S = 50 Ω	V _S = 5 V	25°C	58	74		dB
				Full range	57			
				25°C	72	88		
				Full range	70			
		V _{IC} = 0 V to V _S , R _S = 50 Ω	V _S = 15 V	25°C	65	80		dB
				Full range	64			
				25°C	72	90		
				Full range	70			
A _{VD}	Large-signal differential voltage amplification	V _{O(PP)} =V _S /2, R _L = 100 kΩ	V _S = 2.7 V	25°C	80	100		dB
				Full range	77			
			V _S = 5 V	25°C	80	100		
				Full range	77			
			V _S = 15 V	25°C	77	83		
				Full range	74			

† Full range is -40°C to 125°C.

input characteristics

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
I _{IO}	Input offset current	V _{IC} = V _S /2, R _L = 100 kΩ , V _O = V _S /2, R _S = 50 Ω	≤25°C		1	60	pA
			≤70°C			100	
			≤125°C			1000	
I _{IB}	Input bias current		≤25°C		1	60	pA
			≤70°C			200	
			≤125°C			1000	
r _{i(d)}	Differential input resistance		25°C		1000		GΩ
C _{IC}	Common-mode input capacitance	f = 1 kHz	25°C		8		pF

electrical characteristics at recommended operating conditions, $V_S = 2.7\text{ V}$, 5 V , and 15 V (unless otherwise noted) (continued)

power supply

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
I_{DD} Supply current (per channel)	$V_O = V_S/2$	25°C		7	10	μA
		Full range			15	
PSRR Power supply rejection ratio ($\Delta V_S/\Delta V_{IO}$)	$V_S = 2.7\text{ V}$ to 16 V , $V_{IC} = V_S/2\text{ V}$ No load,	25°C	74	82		dB
		Full range	70			

† Full range is -40°C to 125°C for I suffix.

output characteristics

PARAMETER	TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
V_O Output voltage swing from rail	$V_{IC} = V_S/2$, $I_O = 100\text{ }\mu\text{A}$	$V_S = 2.7\text{ V}$	25°C	200	160		mV
			Full range	220			
		$V_S = 5\text{ V}$	25°C	120	85		
			Full range	200			
		$V_S = 15\text{ V}$	25°C	120	50		
			Full range	150			
	$V_{IC} = V_S/2$, $I_O = 500\text{ }\mu\text{A}$	$V_S = 5\text{ V}$	25°C	800	420		mV
			Full range	900			
		$V_S = 15\text{ V}$	25°C	400	200		
			Full range	500			
I_O Output current	$V_O = 0.5\text{ V}$ from rail	$V_S = 2.7\text{ V}$	25°C		400		μA

† Full range is -40°C to 125°C for I suffix.

dynamic performance

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
GBP Gain bandwidth product	$R_L = 100\text{ k}\Omega$, $C_L = 10\text{ pF}$, $f = 1\text{ kHz}$	25°C		160		kHz
SR Slew rate at unity gain	$V_{O(pp)} = 2\text{ V}$, $R_L = 100\text{ k}\Omega$, $C_L = 10\text{ pF}$	25°C		0.06		$\text{V}/\mu\text{s}$
		-40°C		0.05		
		125°C		0.08		
ϕ_M Phase margin	$R_L = 100\text{ k}\Omega$, $C_L = 50\text{ pF}$	25°C		62		$^\circ$
Gain margin		25°C		6.7		dB
t_s Settling time (0.1%)	$V_{(STEP)pp} = 1\text{ V}$, $A_V = -1$, $C_L = 10\text{ pF}$, $R_L = 100\text{ k}\Omega$	25°C		31		μs
				61		

noise/distortion performance

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$	25°C		90		$\text{nV}/\sqrt{\text{Hz}}$

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V _{IO}	Input offset voltage	vs Common-mode input voltage	1, 2, 3
I _B /I _O	Input bias and offset current	vs Free-air temperature	4
V _{OH}	High-level output voltage	vs High-level output current	5, 7, 9
V _{OL}	Low-level output voltage	vs Low-level output current	6, 8, 10
I _Q	Quiescent current	vs Supply voltage	11
		vs Free-air temperature	12
Supply voltage and supply current ramp up			13
A _{VD}	Differential voltage gain and phase shift	vs Frequency	14
GBP	Gain-bandwidth product	vs Free-air temperature	15
ϕ _m	Phase margin	vs Load capacitance	16
CMRR	Common-mode rejection ratio	vs Frequency	17
PSRR	Power supply rejection ratio	vs Frequency	18
Input referred noise voltage		vs Frequency	19
SR	Slew rate	vs Free-air temperature	20
V _{O(PP)}	Peak-to-peak output voltage	vs Frequency	21
Inverting small-signal response			22
Inverting large-signal response			23
Crosstalk		vs Frequency	24

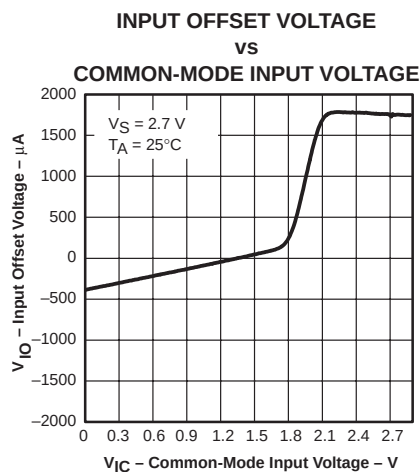


Figure 1

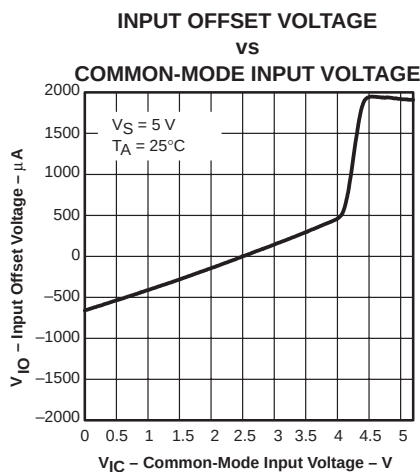


Figure 2

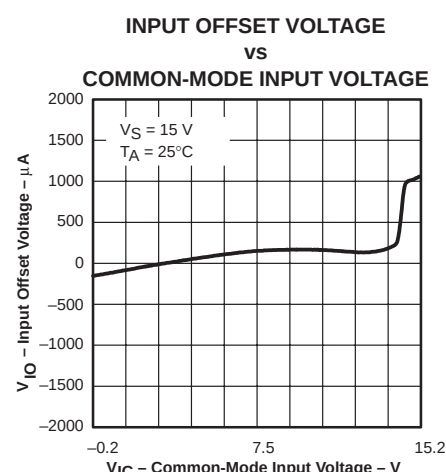


Figure 3

TYPICAL CHARACTERISTICS

INPUT BIAS AND INPUT
OFFSET CURRENT
VS
FREE-AIR TEMPERATURE

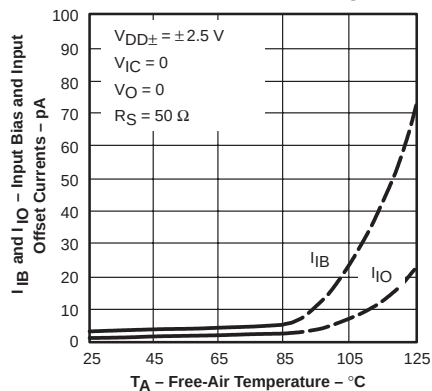


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT

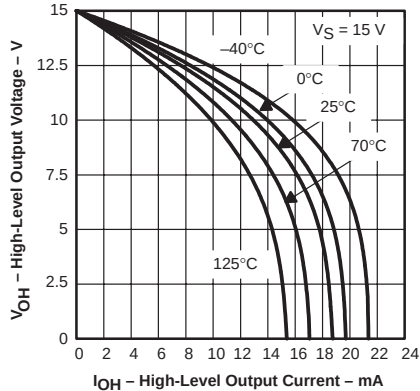


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT

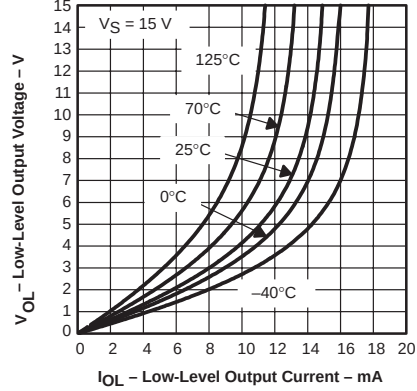


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT

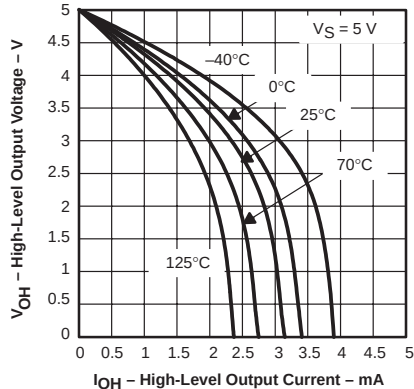


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT

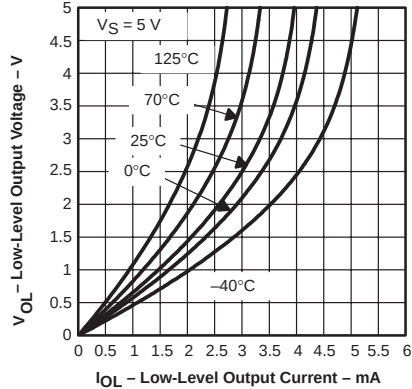


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT

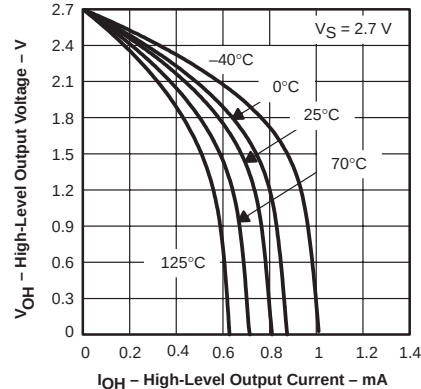


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT

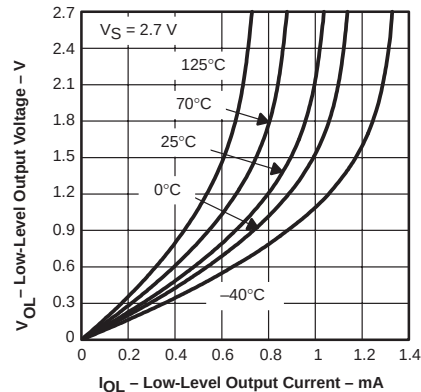


Figure 10

QUIESCENT CURRENT
VS
SUPPLY VOLTAGE

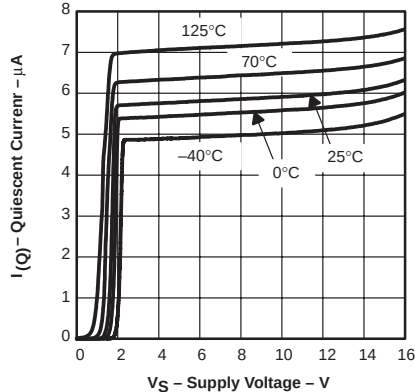


Figure 11

QUIESCENT CURRENT
VS
FREE-AIR TEMPERATURE

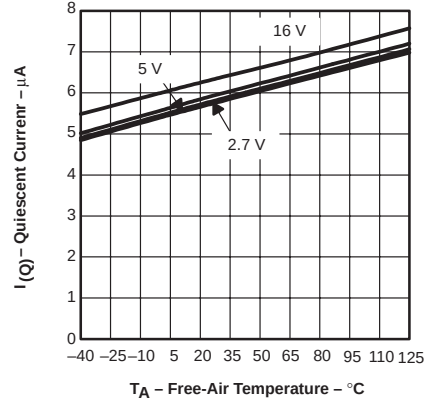


Figure 12

TYPICAL CHARACTERISTICS

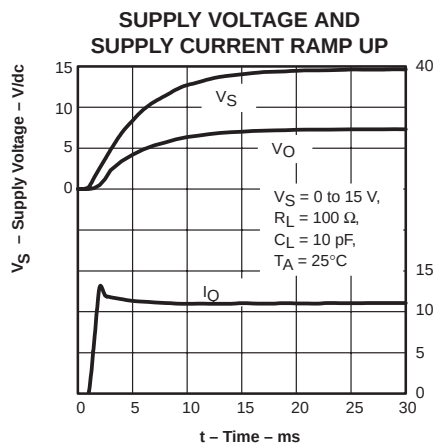


Figure 13

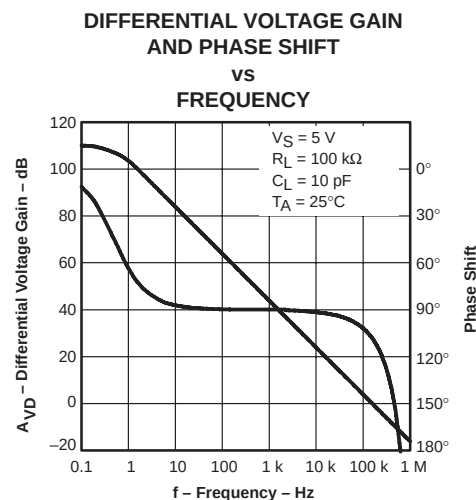


Figure 14

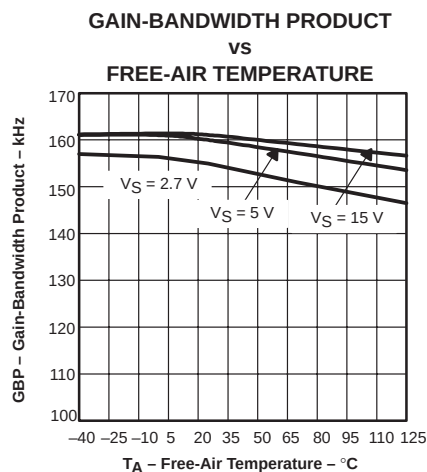


Figure 15

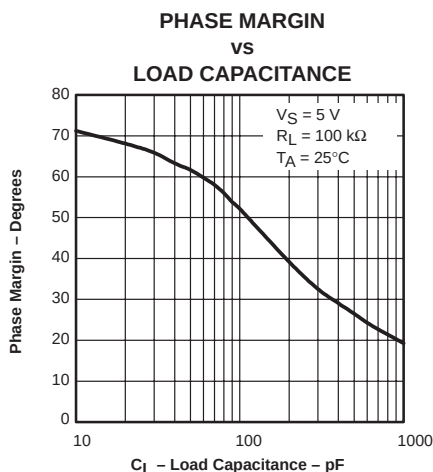


Figure 16

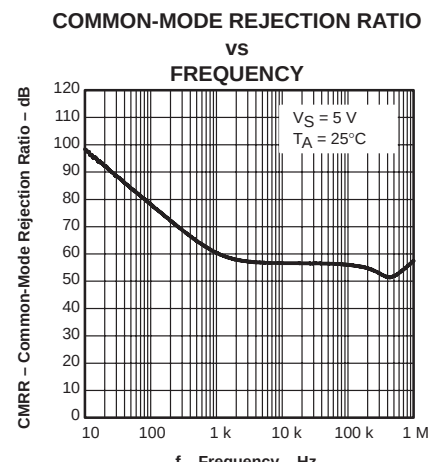


Figure 17

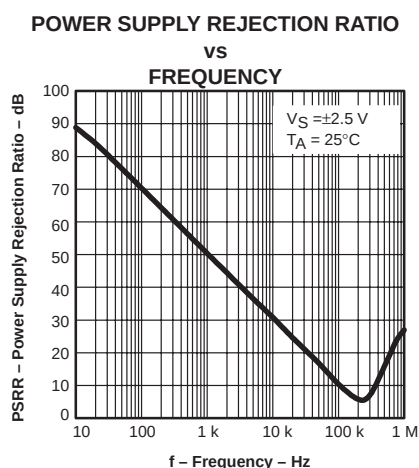


Figure 18

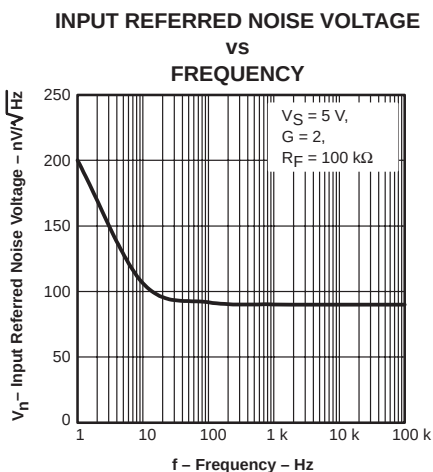


Figure 19

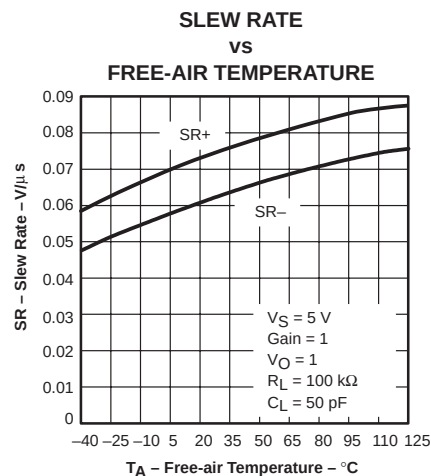
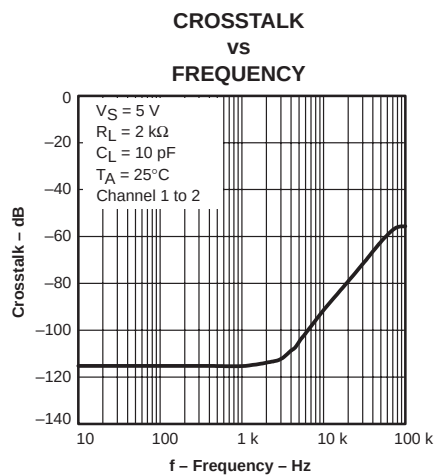
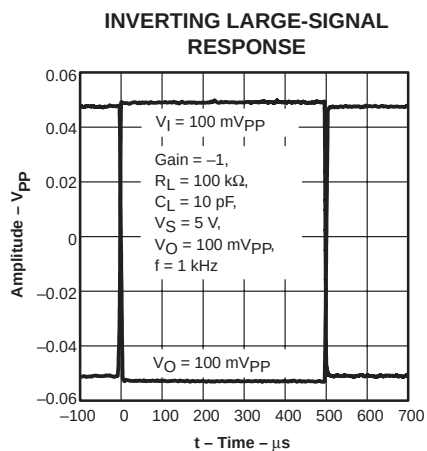
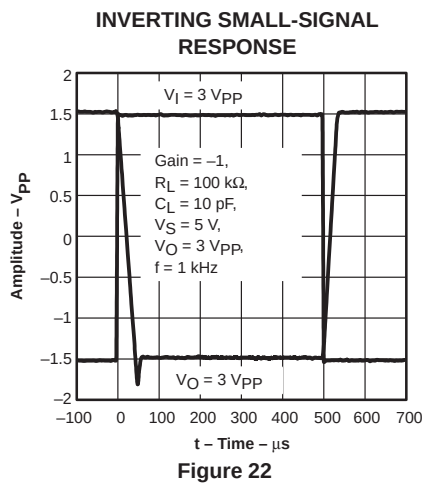
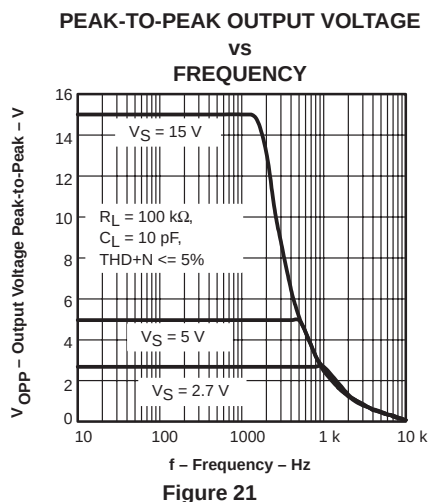


Figure 20

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION

offset voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

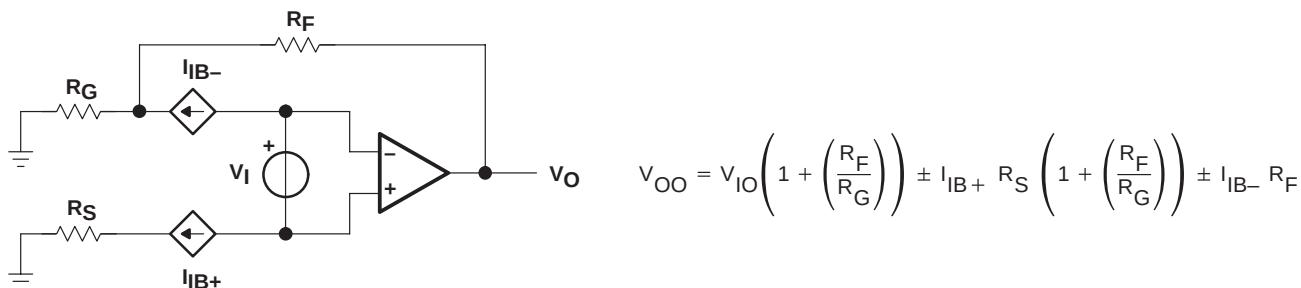


Figure 25. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 26).

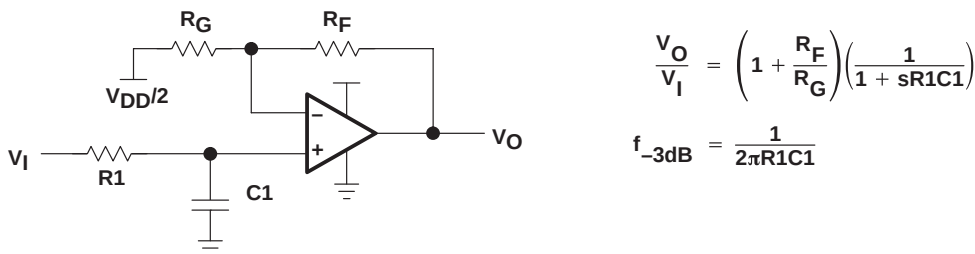


Figure 26. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

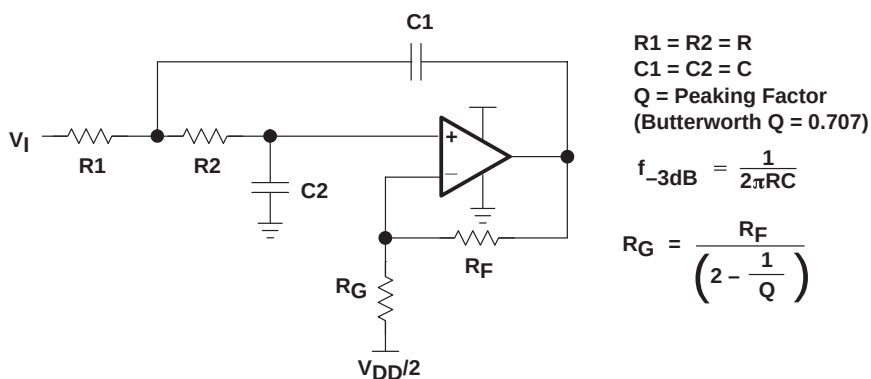


Figure 27. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV238x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- **Ground planes**—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- **Proper power supply decoupling**—Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- **Sockets**—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- **Short trace runs/compact part placements**—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- **Surface-mount passive components**—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

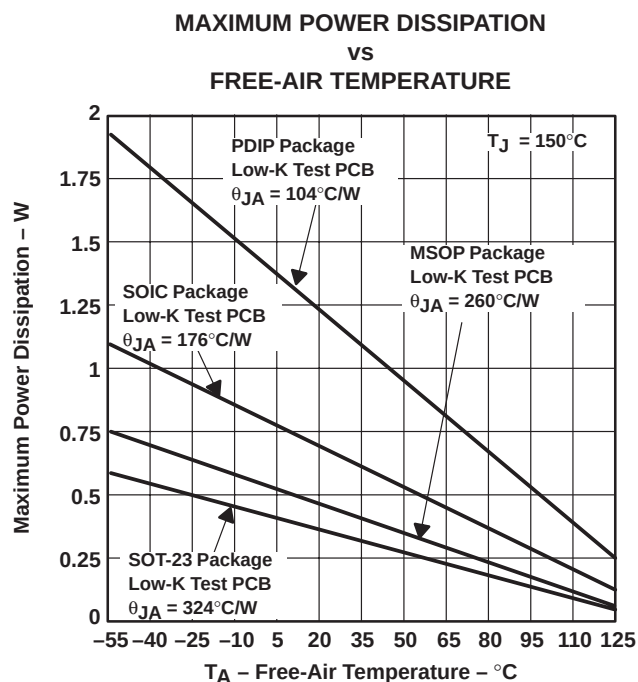
general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 28 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

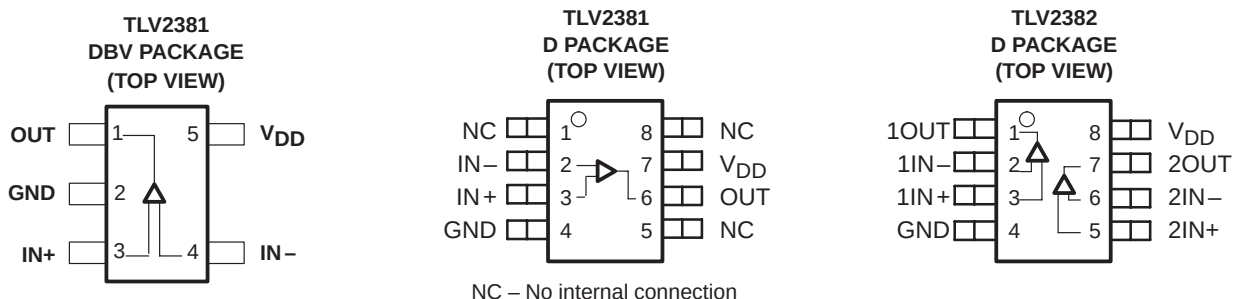
Where:

- P_D = Maximum power dissipation of TLV238x IC (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
 - θ_{JC} = Thermal coefficient from junction to case
 - θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 28. Maximum Power Dissipation vs Free-Air Temperature



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2381ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2381I
TLV2381ID.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2381I
TLV2381IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VBKI
TLV2381IDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VBKI
TLV2381IDBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VBKI
TLV2381IDBVT.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	VBKI
TLV2381IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2381I
TLV2381IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2381I
TLV2382ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2382I
TLV2382ID.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2382I
TLV2382IDG4	Active	Production	SOIC (D) 8	75 TUBE	-	Call TI	Call TI	-40 to 125	
TLV2382IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2382I
TLV2382IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2382I
TLV2382IDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2382I
TLV2382IDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2382I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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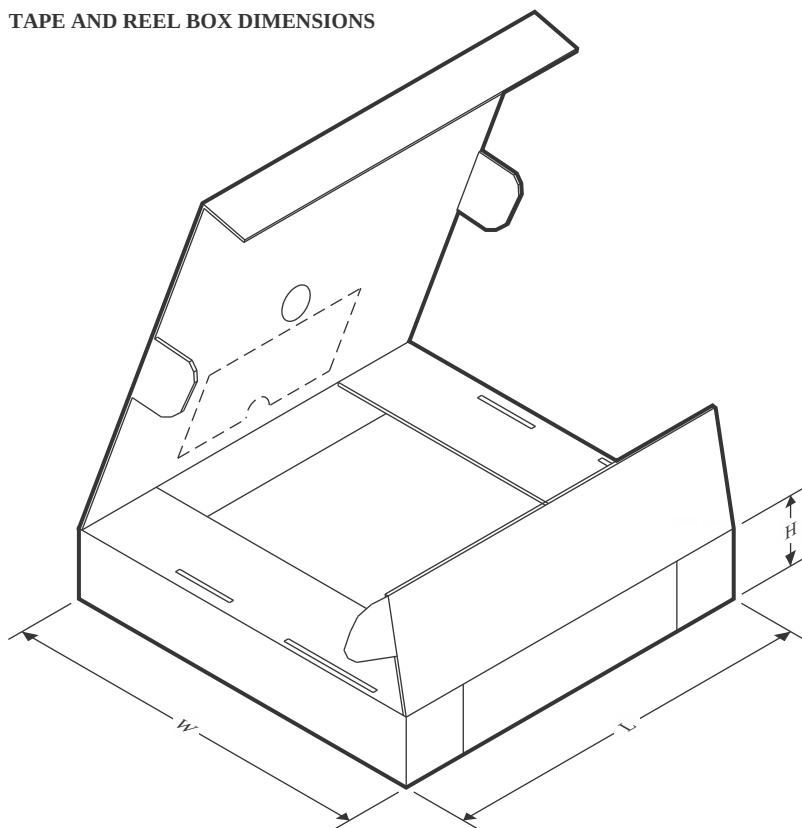
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2381IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2381IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2381IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2382IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2382IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2381IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV2381IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV2381IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2382IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2382IDRG4	SOIC	D	8	2500	353.0	353.0	32.0

TUBE

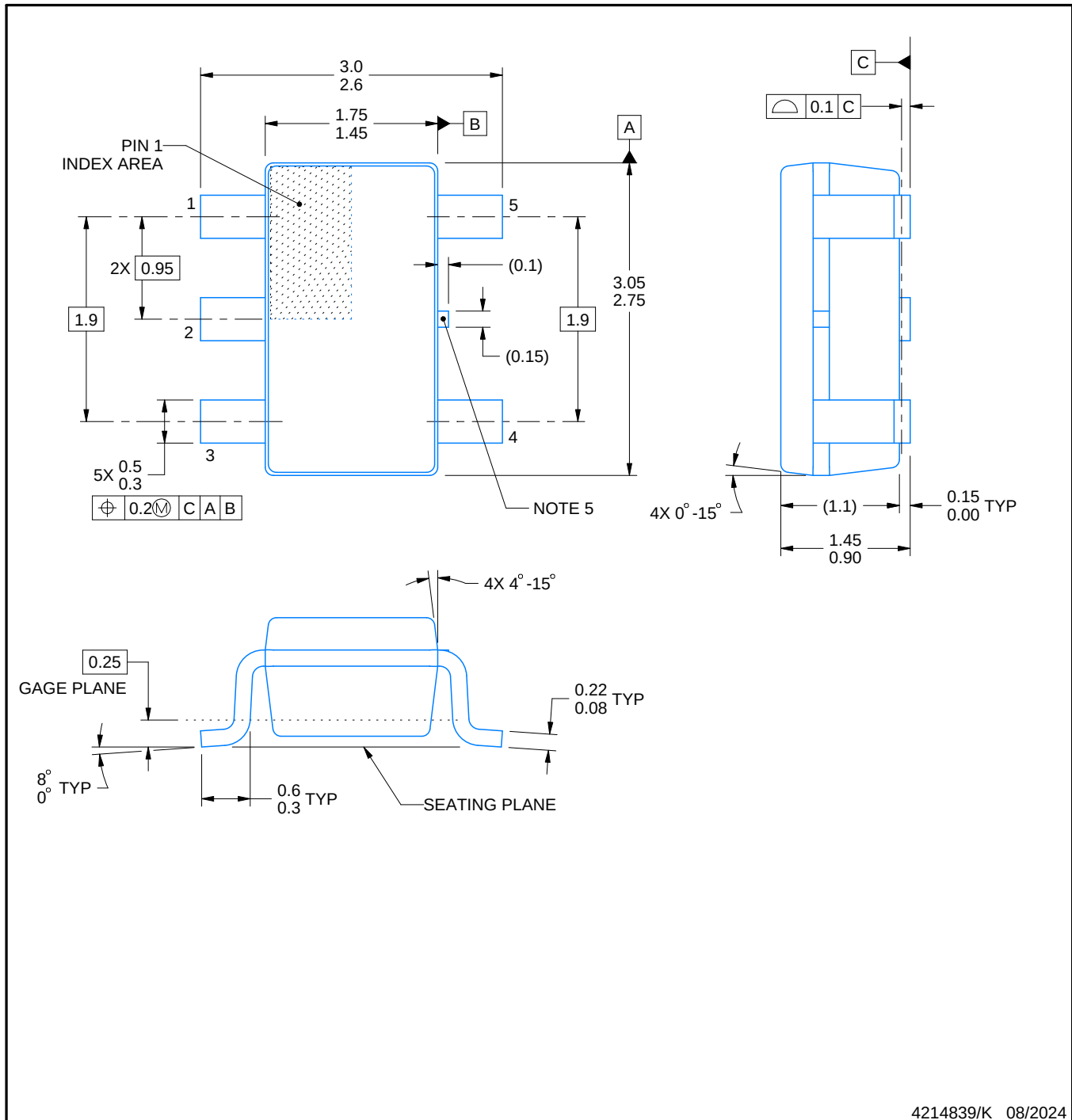


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV2381ID	D	SOIC	8	75	507	8	3940	4.32
TLV2381ID.A	D	SOIC	8	75	507	8	3940	4.32
TLV2382ID	D	SOIC	8	75	507	8	3940	4.32
TLV2382ID.A	D	SOIC	8	75	507	8	3940	4.32

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR

**NOTES:**

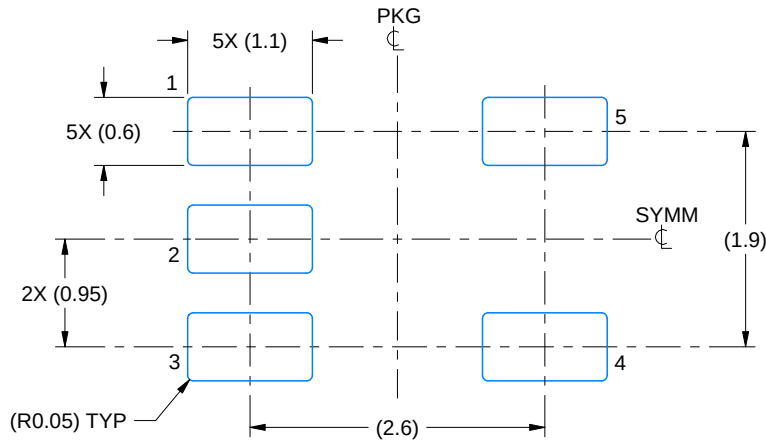
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

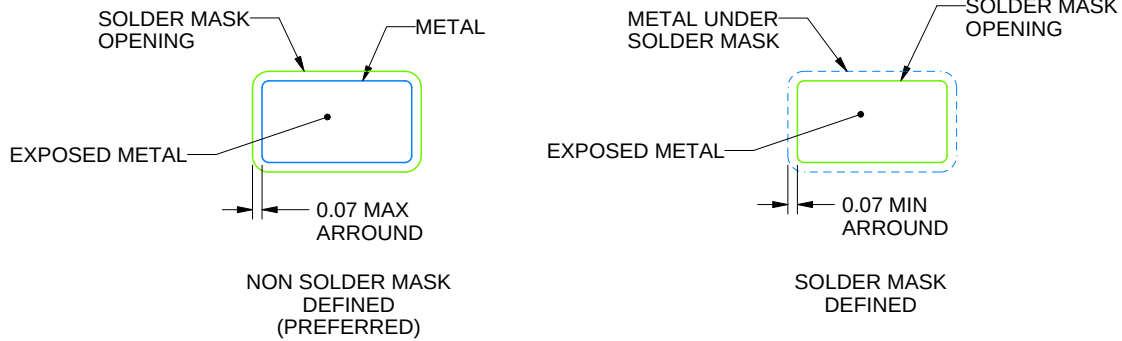
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

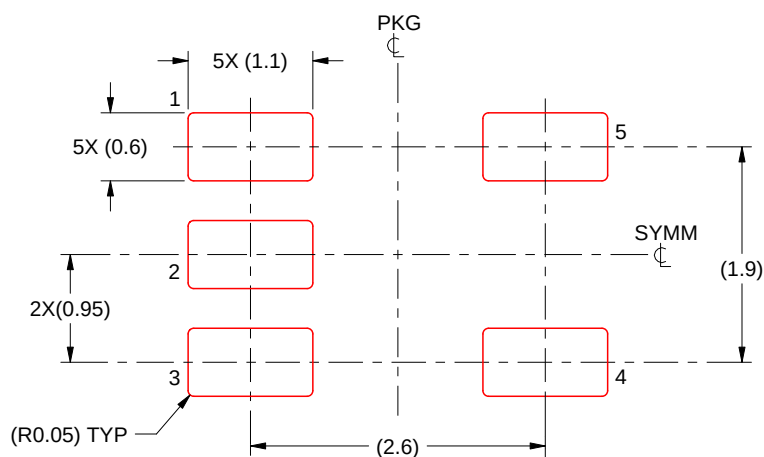
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

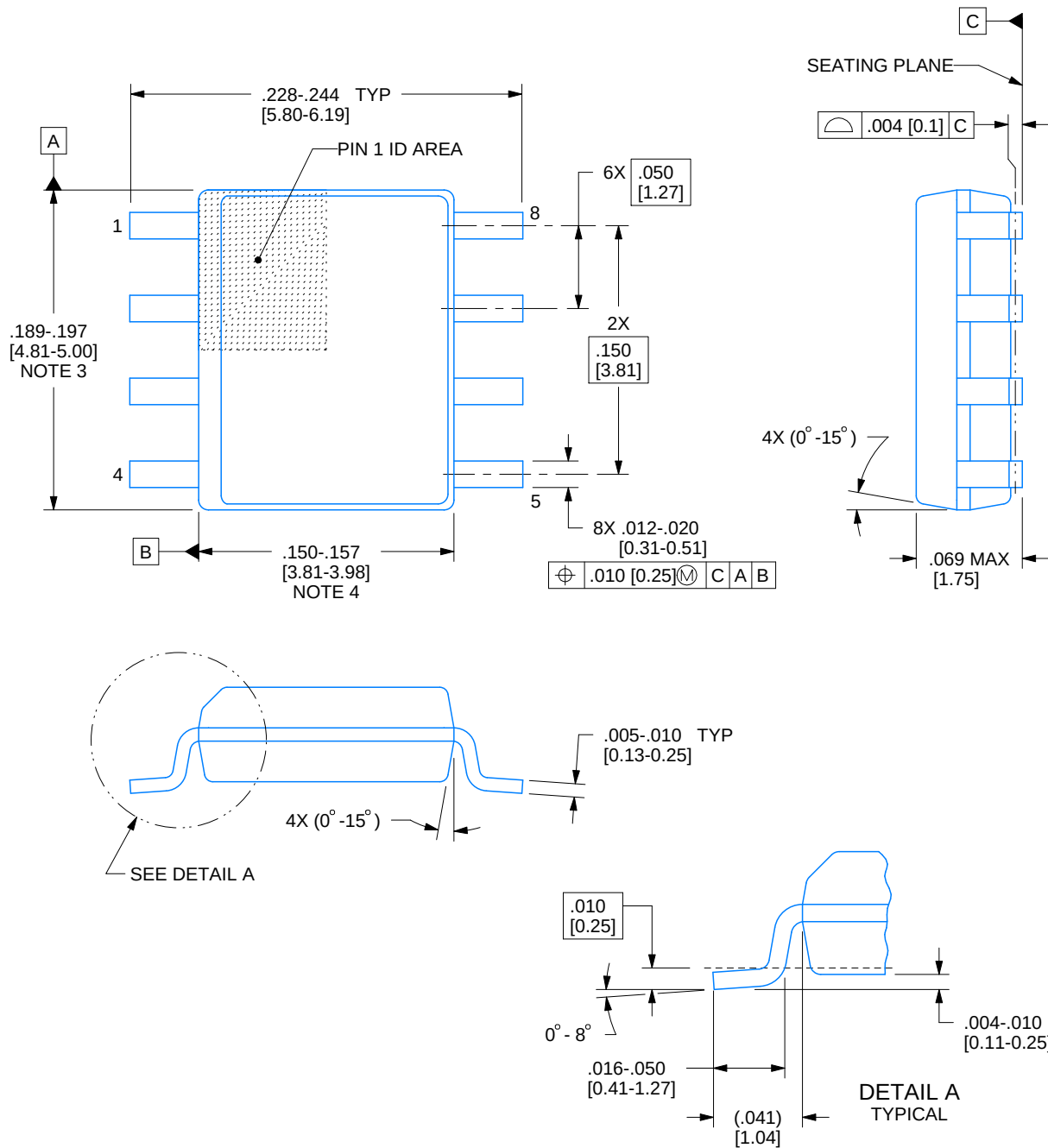
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

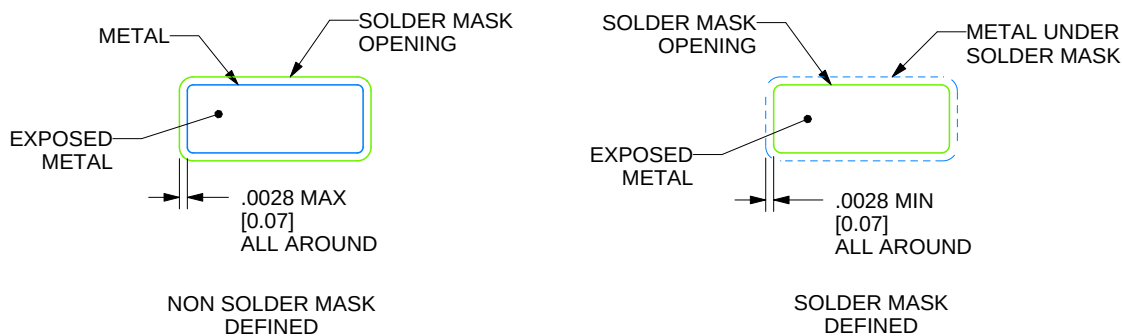
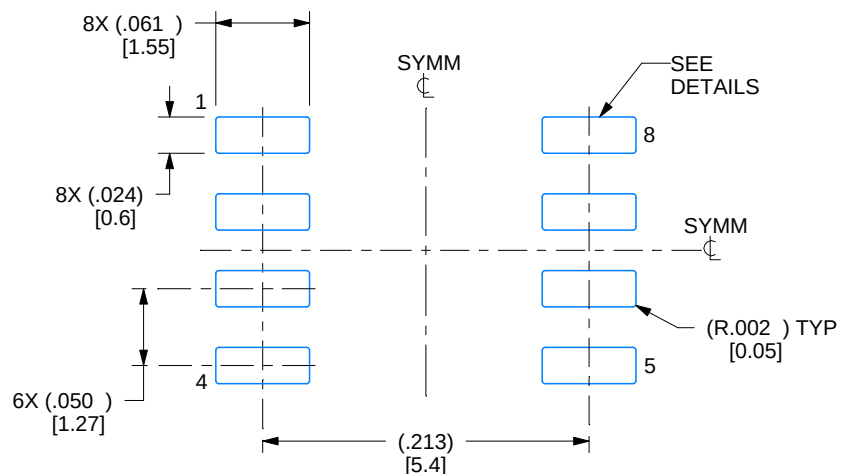
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

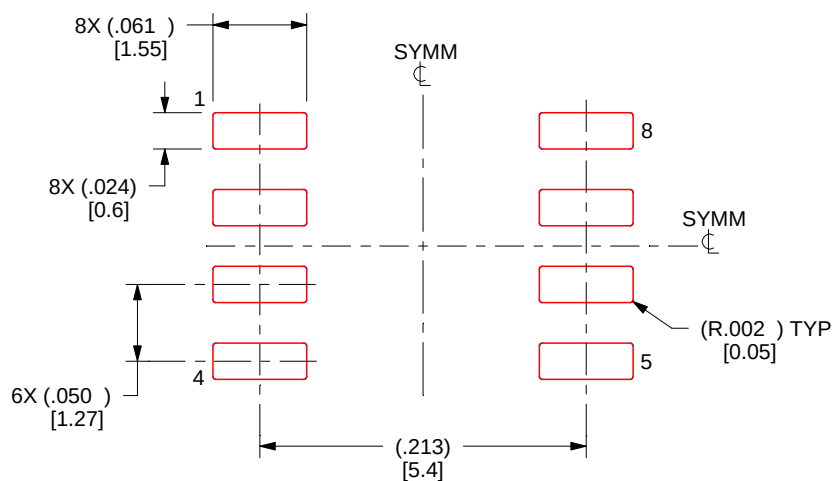
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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