TLV232x Low-Voltage, Low-Power Operational Amplifiers

1 Features

- Wide range of supply voltages over specified temperature range:
  - T_A = –40°C to +85°C, V_{DD} = 2.7V to 8V
- Fully characterized at 3V and 5V
- Single-supply operation
- Common-mode input voltage range extends to less than the negative rail and up to V_{DD} –1V at T_A = 25°C
- Output voltage range includes negative rail
- High input impedance: $10^{12}\Omega$ typical
- ESD-protection circuitry
- Designed-in latch-up immunity

2 Applications

- Smoke and heat detector
- Field transmitter and sensor
  - Flow transmitter
  - Pressure transmitter
  - Temperature transmitter
  - Level transmitter
- Motion detector

3 Description

The TLV2322 and TLV2324 (TLV232x) operational amplifiers are in a family of devices that have been specifically designed for use in low-voltage, single-supply applications. This amplifier is especially useful for ultra-low-power systems that require devices to consume the absolute minimum of supply currents. Each amplifier is fully functional down to a minimum supply voltage of 2.7V, and is fully characterized, tested, and specified at both 3V and 5V power supplies. The common-mode input voltage range includes the negative rail and extends to within 1V of the positive rail.

These amplifiers are specifically targeted for use in very low-power, portable, battery-driven applications with the maximum supply current per operational amplifier specified at only 27µA over the full temperature range of –40°C to +85°C.

Low-voltage and low-power operation is possible by using the Texas Instruments silicon-gate LinCMOS™ technology. The LinCMOS technology process also features extremely high input impedance and ultra-low bias currents making these amplifiers an excellent choice for interfacing to high-impedance sources such as sensor circuits or filter applications.

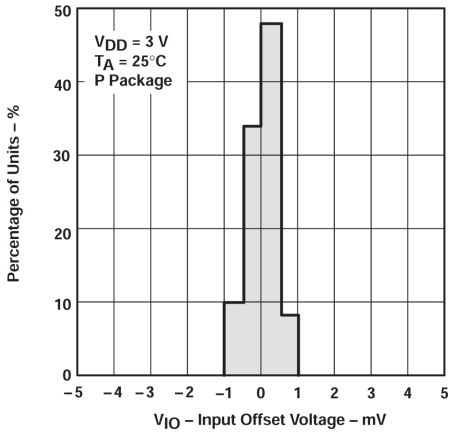
To facilitate the design of small portable equipment, the TLV232x is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard, surface-mount package. The maximum height of only 1.1mm makes this device particularly attractive when space is critical.

The device inputs and outputs are designed to withstand –100mA currents without sustaining latch-up. The TLV232x incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000V as tested under MIL-STD 883C, Method 3015.2. However, exercise care in handling these devices because exposure to ESD potentially results in the degradation of device parametric performance.

Device Information

PART NUMBER	V_{IOMAX} AT 25°C	PACKAGE(1)
TLV2322	9mV	D (SOIC, 8)
		P (PDIP, 8)
		PW (TSSOP, 8)
TLV2324	10mV	D (SOIC, 14)
		N (PDIP, 14)
		PW (TSSOP, 14)

(1) For all available packages, see Section 10.



Sample Distribution of Input Offset Voltage (TLV2322)

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4 Pin Configuration and Functions

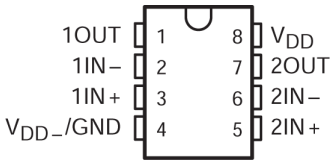


Figure 4-1. TLV2322 D Package, 8-Pin SOIC and P Package, 8-Pin PDIP (Top View)

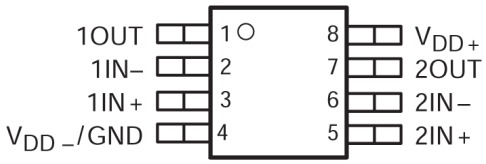


Figure 4-2. TLV2322 PW Package, 8-Pin TSSOP (Top View)

Table 4-1. Pin Functions: TLC2322

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	3	Input	Noninverting input, channel 1
1IN–	2	Input	Inverting input, channel 1
2IN+	5	Input	Noninverting input, channel 2
2IN–	6	Input	Inverting input, channel 2
OUT1	1	Output	Output, channel 1
OUT2	7	Output	Output, channel 2
V_{DD+}	8	—	Positive (highest) power supply
$V_{DD–}$ / GND	4	—	Ground or negative (lowest) power supply

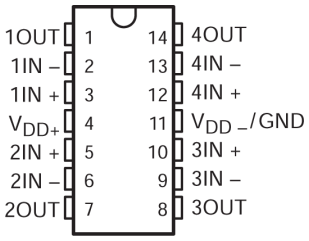


Figure 4-3. TLV2324 D Package, 14-Pin SOIC, or N Package, 14-Pin PDIP (Top View)

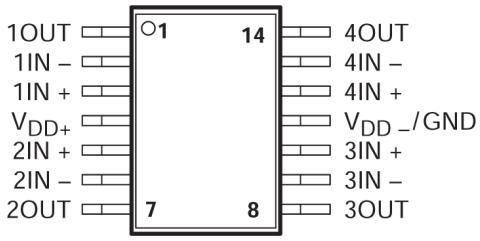


Figure 4-4. TLV2324 PW Package, 14-Pin TSSOP (Top View)

Table 4-2. Pin Functions: TLC2324

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	3	Input	Noninverting input, channel 1
1IN–	2	Input	Inverting input, channel 1
2IN+	5	Input	Noninverting input, channel 2
2IN–	6	Input	Inverting input, channel 2
3IN+	10	Input	Noninverting input, channel 3
3IN–	9	Input	Inverting input, channel 3
4IN+	12	Input	Noninverting input, channel 4
4IN–	13	Input	Inverting input, channel 4
OUT1	1	Output	Output, channel 1
OUT2	7	Output	Output, channel 2
OUT3	8	Output	Output, channel 3
OUT4	14	Output	Output, channel 4
V_{DD+}	4	—	Positive (highest) power supply
$V_{DD–}$ / GND	11	—	Ground or negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} (2)	Supply voltage		8	V
V_{ID} (3)	Differential input voltage		V_{DD}±	V
V_I (any input)	Input voltage	–0.3	V_{DD}	V
I_I	Input current		±5	mA
I_O	Output current		±30	mA
	Duration of short-circuit current at (or less than) T_A = 25°C(4)	Unlimited		
	Continuous total dissipation	See *Dissipation Ratings*		
T_A	Operating free-air temperature	–40	85	°C
T_{stg}	Storage temperature	–65	150	°C
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at the noninverting input with respect to the inverting input.
(4) The output is able to be shorted to either supply. Limit temperature, supply voltages, or both to not exceed the maximum dissipation ratings (see Section 7.1.6).

5.2 Dissipation Ratings

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR, T_A > 25°C	T_A = 85°C POWER RATING
D (SOIC, 8)	725mW	5.8mW/°C	377mW
D (SOIC, 14)	950mW	7.6mW/°C	494mW
N (PDIP, 14)	1575mW	12.6mW/°C	819mW
P (PDIP, 8)	1000mW	8.0mW/°C	520mW
PW (TSSOP, 8)	525mW	4.2mW/°C	273mW
PW (TSSOP, 14)	700mW	5.6mW/°C	364mW

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Supply voltage		2.7	8	V
V_{IC}	Common-mode input voltage	V_{DD} = 3V	–0.2	1.8	V
		V_{DD} = 5V	–0.2	3.8	
T_A	Operating free-air temperature		–40	85	°C

5.4 Electrical Characteristics, TLV2322

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TLV2322						UNIT
				V_{DD} = 3V			V_{DD} = 5V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1V, V_{IC} = 1V, R_S = 50Ω, R_L = 1MΩ	25°C		1.1	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		µV/°C
I_{IO}	Input offset current (2) (3)	V_O = 1V, V_{IC} = 1V	25°C		0.5			0.5		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (2) (3)	V_O = 1V, V_{IC} = 1V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (4)		25°C	−0.2 to 2	−0.2 to 2.3		−0.2 to 4	−0.2 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1V, V_{ID} = 100mV, I_{OH} = −1mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1V, V_{ID} = 100mV, I_{OH} = −1mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1V, R_L = 1MΩ (5)	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1V, R_S = 50Ω V_{IC} = V_{ICR}min	25°C	61	83		65	88		dB
			Full range	59			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1V, V_O = 1V, R_S = 50Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1V, V_{IC} = 1V, no load	25°C		13	34		20	34	µA
			Full range			54			54	

(1) Full range is –40°C to +85°C.
(2) The typical values of input bias current and input offset current less than 5pA are determined mathematically.
(3) Values specified by characterization.
(4) This range also applies to each input individually.
(5) At V_{DD} = 5V, $V_{O(PP)}$ = 0.25V to 2V; at V_{DD} = 3V, V_O = 0.5V to 1.5V.

5.5 Operating Characteristics TLV2322, V_{DD} = 3V

at specified free-air temperature, V_{DD} = 3V

PARAMETER		TEST CONDITIONS	T_A	TLV2322			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1V, $V_{I(PP)}$ = 1V, R_L = 1MΩ, C_L = 20pF,see Figure 6-1	25°C		0.02		V/µs
			85°C		0.02		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	25°C		2.5		kHz
			85°C		2		
B_1	Unity-gain bandwidth	V_I = 10mV, R_L = 1MΩ, C_L = 20pF, see Figure 6-3	25°C		27		kHz
			85°C		21		
ϕ_m	Phase margin	V_I = 10mV, f = B_1, R_L = 1MΩ, C_L = 20pF, see Figure 6-3	−40°C		39		°
			25°C		34		
			85°C		28		

5.6 Operating Characteristics, TLV2322, V_{DD} = 5V

at specified free-air temperature, V_{DD} = 5V

PARAMETER		TEST CONDITIONS		T_A	TLV2322			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1V, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	$V_{I(PP)}$ = 1V	25°C		0.03		V/µs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1MΩ, C_L = 20pF, see Figure 6-1		25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10mV, R_L = 1MΩ, C_L = 20pF, see Figure 6-3		25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10mV, f = B_1, R_L = 1MΩ, C_L = 20pF, see Figure 6-3		−40°C		38		°
				25°C		34		
				85°C		28		

5.7 Electrical Characteristics, TLV2324

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	TLV2324						UNIT
				V_{DD} = 3V			V_{DD} = 5V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1V, V_{IC} = 1V, R_S = 50Ω, R_L = 1MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		µV/°C
I_{IO}	Input offset current (2) (3)	V_O = 1V, V_{IC} = 1V	25°C		0.5			0.5		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (2) (3)	V_O = 1V, V_{IC} = 1V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range(4)		25°C	−0.2 to 2	−0.2 to 2.3		−0.2 to 4	−0.2 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1V, V_{ID} = 100mV, I_{OH} = −1mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1V, V_{ID} = −100mV, I_{OL} = 1mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1V, R_L = 1MΩ(5)	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1V, R_S = 50Ω, V_{IC} = V_{ICR}min	25°C	61	83		65	88		dB
			Full range	59			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_O = 1V, V_{IC} = 1V, R_S = 50Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1V, V_{IC} = 1V, no load	25°C		26	68		39	68	µA
			Full range			108			108	

(1) Full range is –40°C to 85°C.
(2) The typical values of input bias current and input offset current below 5pA are determined mathematically.
(3) Values specified by characterization.
(4) This range also applies to each input individually.
(5) At V_{DD} = 5V, VO(PP) = 0.25V to 2V; at V_{DD} = 3V, V_O = 0.5V to 1.5V.

5.8 Operating Characteristics, TLV2324, V_{DD} = 3V

at specified free-air temperature, V_{DD} = 3V

PARAMETER		TEST CONDITIONS	T_A	TLV2324			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1V, $V_{I(PP)}$ = 1V, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	25°C		0.02		V/µs
			85°C		0.02		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	25°C		2.5		kHz
			85°C		2		
B_1	Unity-gain bandwidth	V_I = 10mV, R_L = 1MΩ, C_L = 20pF, see Figure 6-3	25°C		27		kHz
			85°C		21		
ϕ_m	Phase margin	V_I = 10mV, f = B_1, R_L = 1MΩ, C_L = 20pF, see Figure 6-3	−40°C		39		°
			25°C		34		
			85°C		28		

5.9 Operating Characteristics, TLV2324, V_{DD} = 5V

at specified free-air temperature, V_{DD} = 5V

PARAMETER		TEST CONDITIONS		T_A	TLV2324			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1V, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	$V_{I(PP)}$= 1V	25°C		0.03		V/µs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2		25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1MΩ, C_L = 20pF, see Figure 6-1		25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10mV, R_L = 1MΩ, C_L = 20pF, see Figure 6-3		25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10mV, f = B_1, R_L = 1MΩ, C_L = 20pF, see Figure 6-3		−40°C		38		°
				25°C		34		
				85°C		28		

5.10 Typical Characteristics

Table 5-1. Table of Graphs

			FIGURE
V_{IO}	Input Offset Voltage	Distribution	1–4
α_{VIO}	Input Offset Voltage Temperature Coefficient	Distribution	5–8
I_{IB}	Input Bias Current	vs Free-Air Temperature	9
I_{IO}	Input Offset Current	vs Free-Air Temperature	9
V_{IC}	Common-Mode Input Voltage	vs Supply Voltage	10
V_{OH}	High-Level Output Voltage	vs High-Level Output Current	11
		vs Supply Voltage	12
		vs Free-Air Temperature	13
V_{OL}	Low-Level Output Voltage	vs Common-Mode Input Voltage	14
		vs Free-Air Temperature	15, 16
		vs Differential Input Voltage	17
		vs Low-Level Output Current	18
A_{VD}	Large-Signal Differential Voltage Amplification	vs Supply Voltage	19
		vs Free-Air Temperature	20
		vs Frequency	21, 22
I_{DD}	Supply Current	vs Supply Voltage	23
		vs Free-Air Temperature	24, 25
S_R	Slew Rate	vs Supply Voltage	26
		vs Free-Air Temperature	27
$V_{O(PP)}$	Maximum Peak-to-Peak Output Voltage	vs Frequency	28
B_1	Unity-Gain Bandwidth	vs Supply Voltage	29
		vs Free-Air Temperature	30
ϕ_m	Phase Margin	vs Supply Voltage	31
		vs Free-Air Temperature	32
		vs Load Capacitance	33
	Phase Shift	vs Frequency	21, 22
V_n	Equivalent Input Noise Voltage	vs Frequency	34

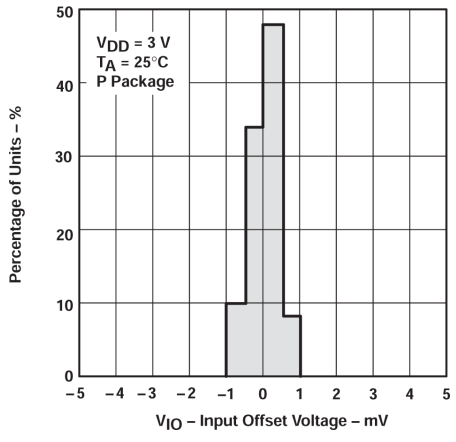


Figure 5-1. Distribution of TLV2322 Input Offset Voltage

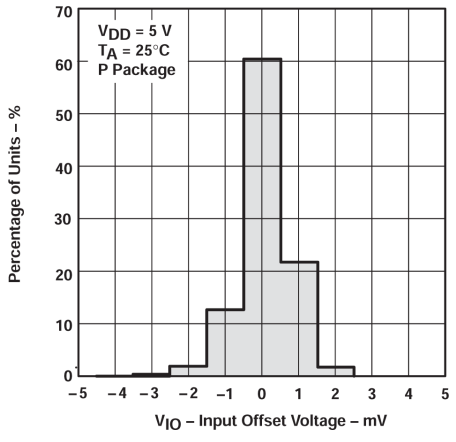


Figure 5-2. Distribution of TLV2322 Input Offset Voltage

5.10 Typical Characteristics (continued)

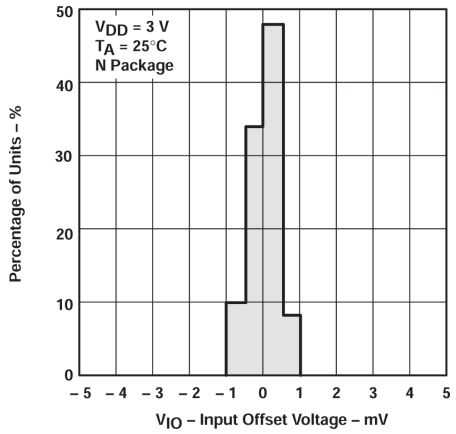


Figure 5-3. Distribution of TLV2324 Input Offset Voltage

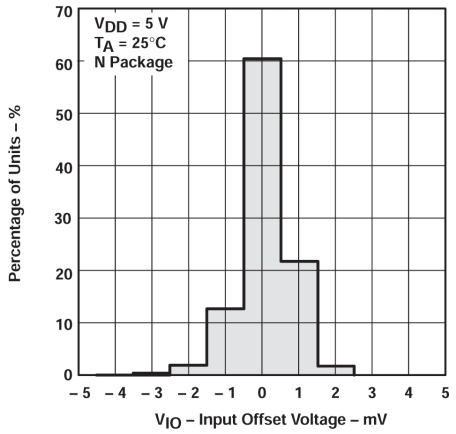


Figure 5-4. Distribution of TLV2324 Input Offset Voltage

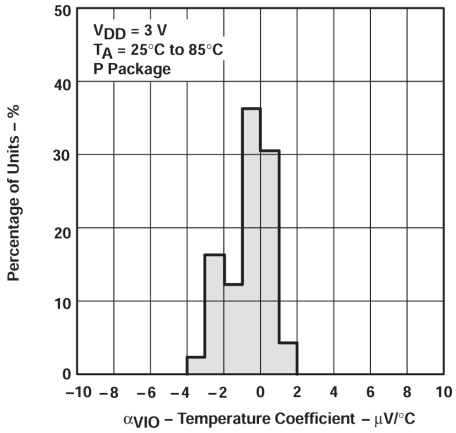


Figure 5-5. Distribution of TLV2322 Input Offset Voltage Temperature Coefficient

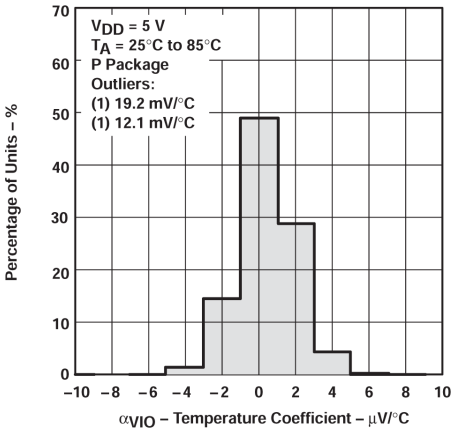


Figure 5-6. Distribution of TLV2322 Input Offset Voltage Temperature Coefficient

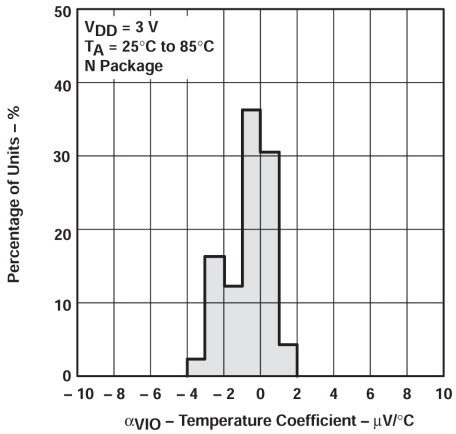


Figure 5-7. Distribution of TLV2324 Input Offset Voltage Temperature Coefficient

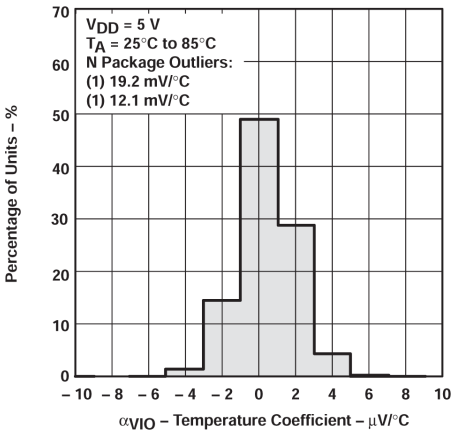
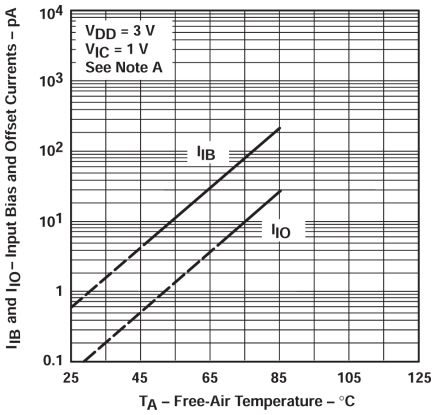


Figure 5-8. Distribution of TLV2324 Input Offset Voltage Temperature Coefficient

5.10 Typical Characteristics (continued)



Typical values of input bias current and input offset current less than 5pA determined mathematically

Figure 5-9. Input Bias Current and Input Offset Current vs Free-Air Temperature

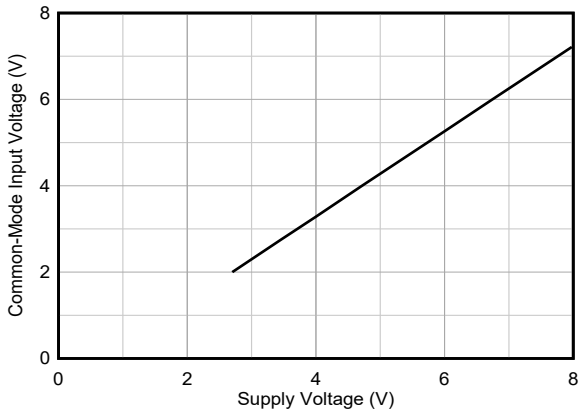


Figure 5-10. Common-Mode Input Voltage vs Supply Voltage

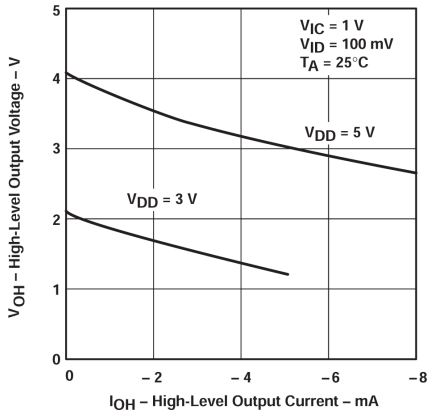
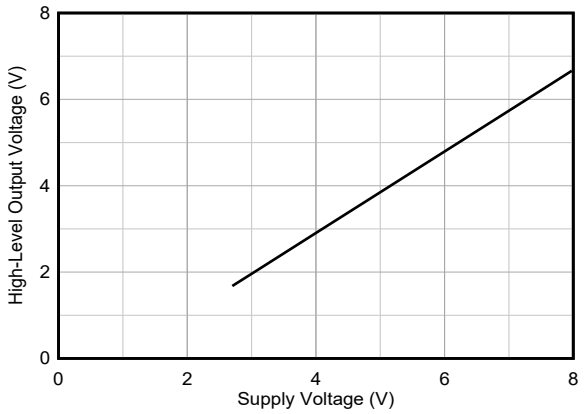


Figure 5-11. High-Level Output Voltage vs High-Level Output Current



V_{IC} = 1V, V_{ID} = 100mV, R_L = 1MΩ

Figure 5-12. High-Level Output Voltage vs Supply Voltage

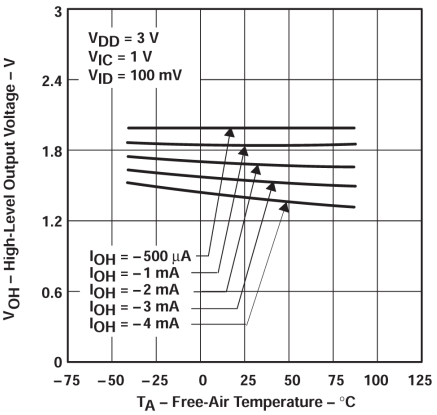


Figure 5-13. High-Level Output Voltage vs Free-Air Temperature

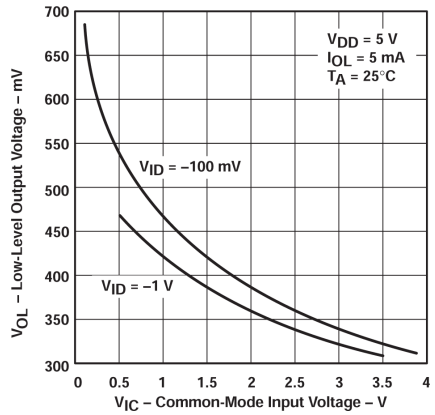


Figure 5-14. Low-Level Output Voltage vs Common-Mode Input Voltage

5.10 Typical Characteristics (continued)

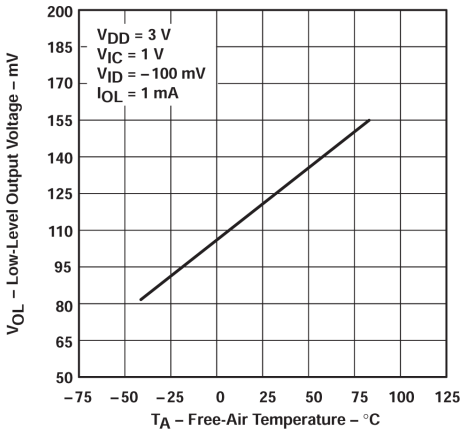


Figure 5-15. Low-Level Output Voltage vs Free-Air Temperature

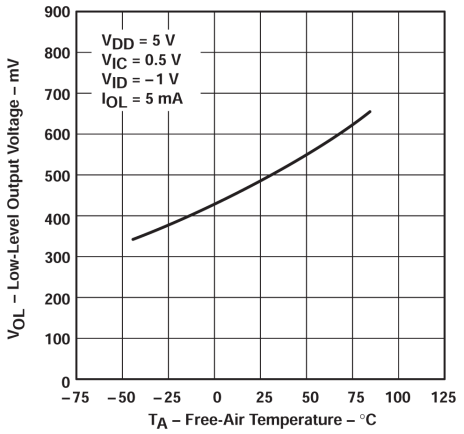


Figure 5-16. Low-Level Output Voltage vs Free-Air Temperature

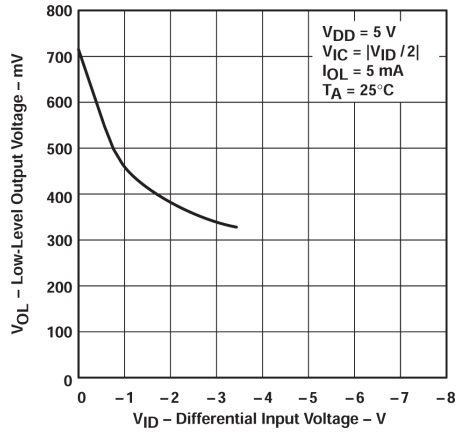


Figure 5-17. Low-Level Output Voltage vs Differential Input Voltage

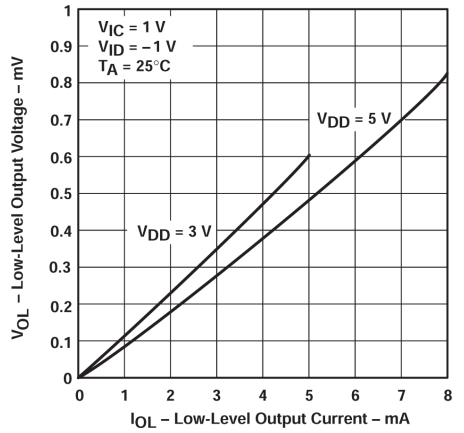


Figure 5-18. Low-Level Output Voltage vs Low-level Output Current

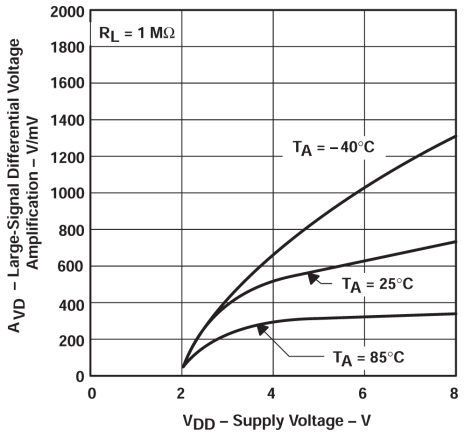


Figure 5-19. Large-Signal Differential Voltage Amplification vs Supply Voltage

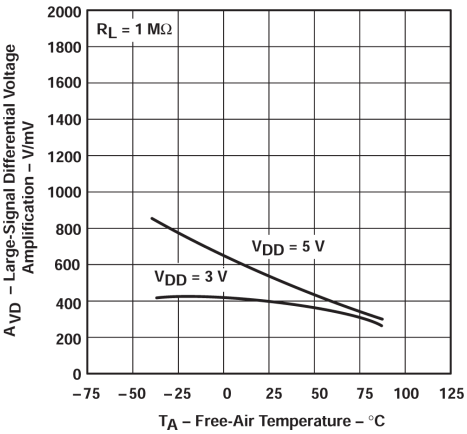


Figure 5-20. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

5.10 Typical Characteristics (continued)

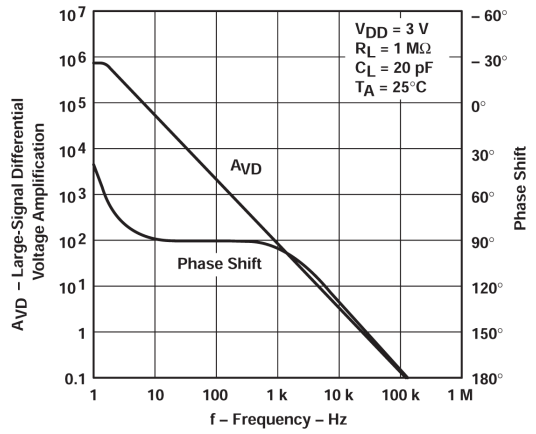


Figure 5-21. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

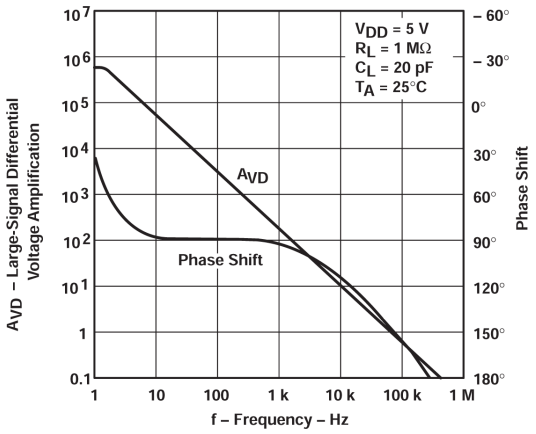
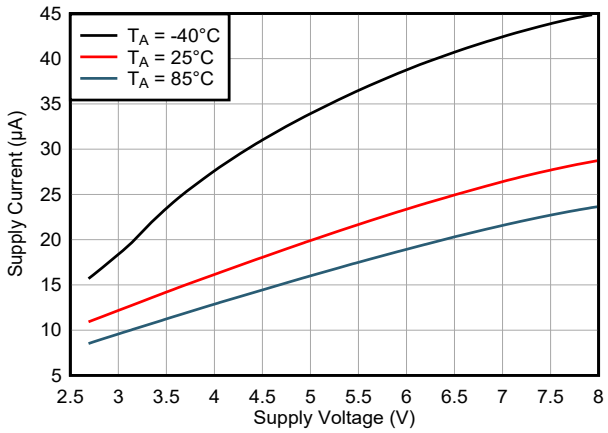


Figure 5-22. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency



$V_{IC} = V_O = 1V$, No Load

Figure 5-23. Supply Current vs Supply Voltage

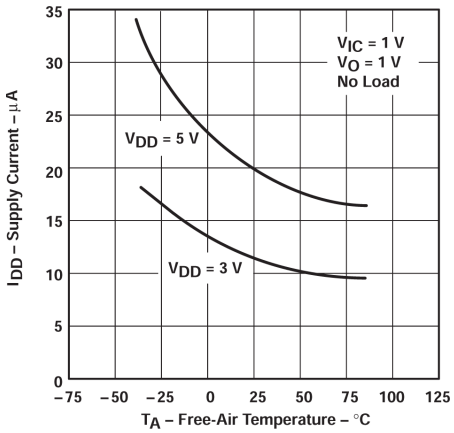


Figure 5-24. TLV2322 Supply Current vs Free-Air Temperature

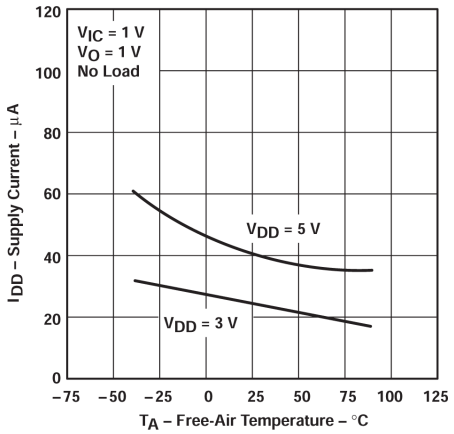
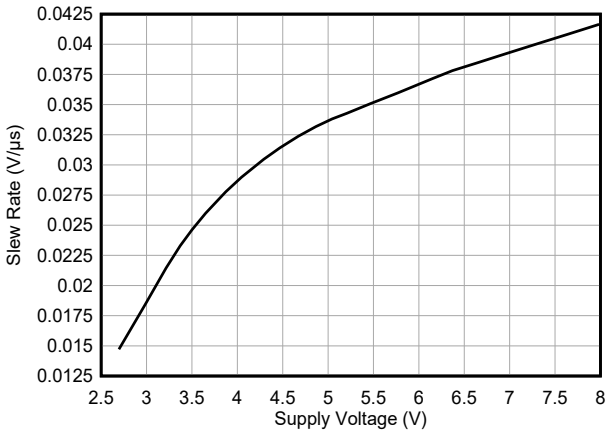


Figure 5-25. TLV2324 Supply Current vs Free-Air Temperature



$V_{IC} = V_{I(PP)} = 1V$, $A_V = 1$, $R_L = 1M\Omega$, $C_L = 20pF$

Figure 5-26. Slew Rate vs Supply Voltage

5.10 Typical Characteristics (continued)

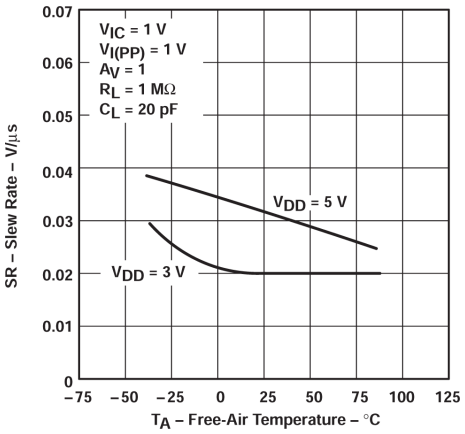


Figure 5-27. Slew Rate vs Free-Air Temperature

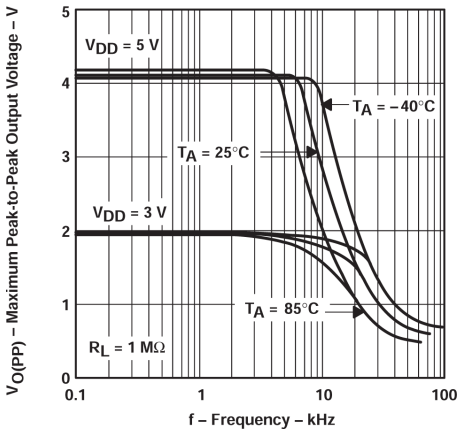


Figure 5-28. Maximum Peak-to-Peak Output Voltage vs Frequency

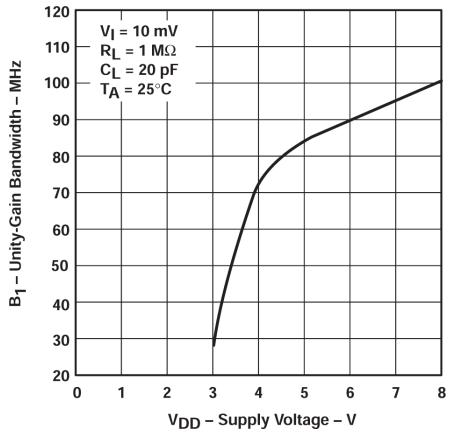


Figure 5-29. Unity-Gain Bandwidth vs Supply Voltage

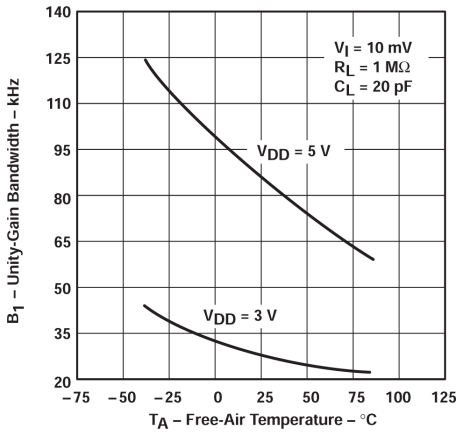
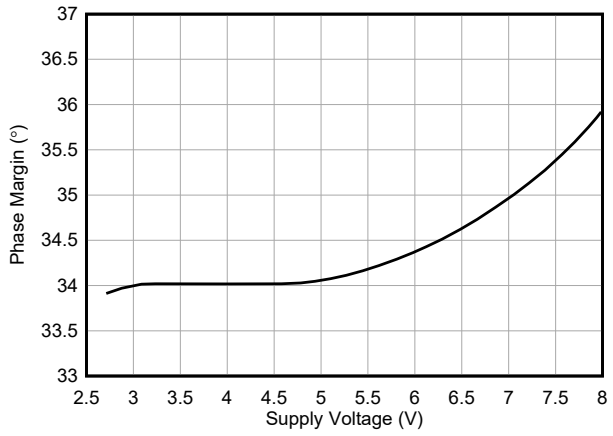


Figure 5-30. Unity-Gain Bandwidth vs Free-Air Temperature



V_I = 10mV, R_L = 1MΩ, C_L = 20pF

Figure 5-31. Phase Margin vs Supply Voltage

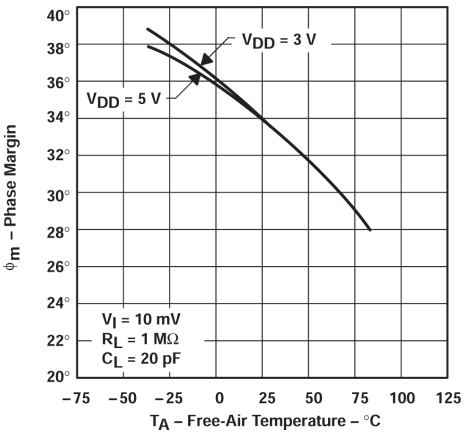


Figure 5-32. Phase Margin vs Free-Air Temperature

5.10 Typical Characteristics (continued)

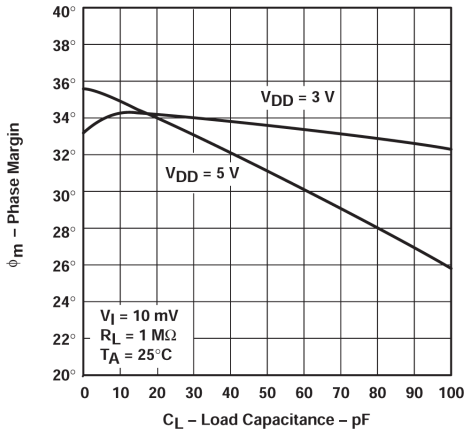


Figure 5-33. Phase Margin vs Load Capacitance

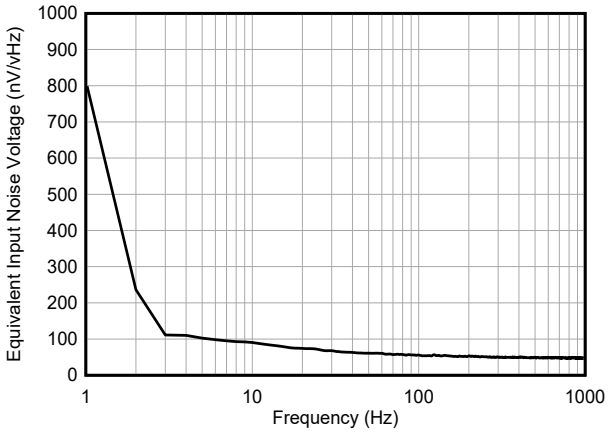


Figure 5-34. Equivalent Input Noise Voltage vs Frequency

6 Parameter Measurement Information

6.1 Single-Supply Versus Split-Supply Test Circuits

Because the TLV232x is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience because the input signal, in many cases, must be offset from ground. Avoid this inconvenience by testing the device with split supplies and the output load tied to the negative rail. The following figures show a comparison of single-supply versus split-supply test circuits. The use of either circuit gives the same result.

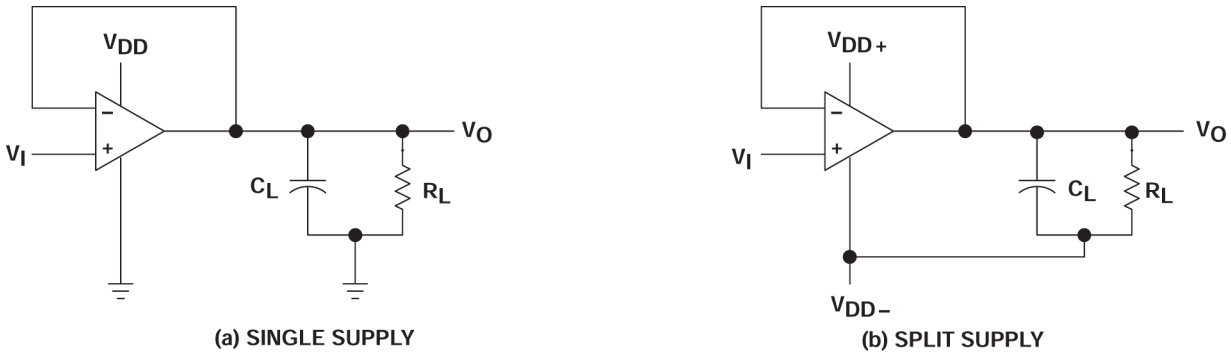


Figure 6-1. Unity-Gain Amplifier

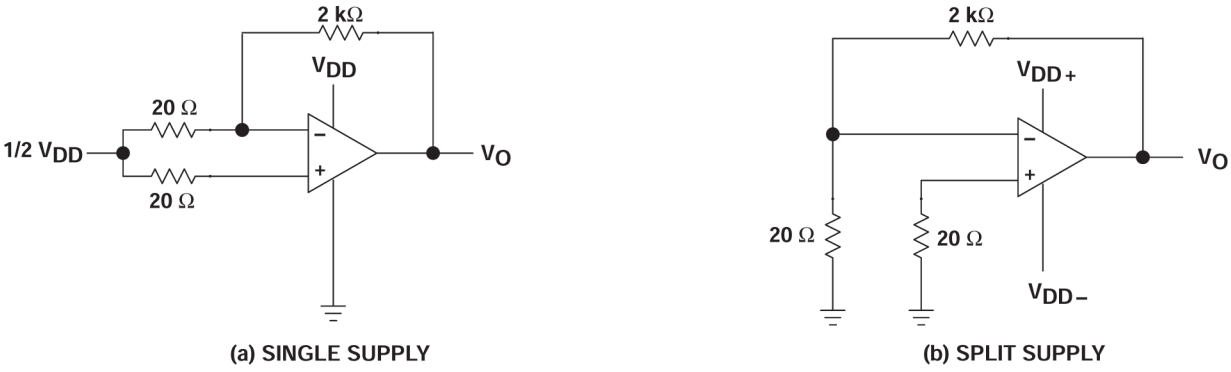


Figure 6-2. Noise-Test Circuits

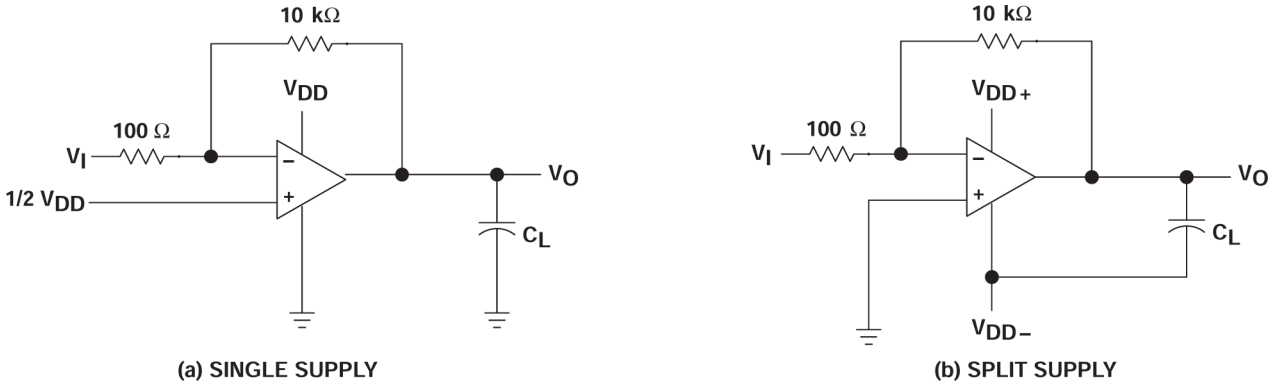


Figure 6-3. Gain-of-100 Inverting Amplifier

6.2 Input Bias Current

Because of the high input impedance of the TLV232x operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 6-4). Leakages that can otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

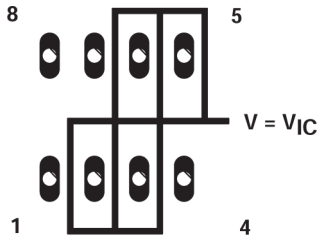


Figure 6-4. Isolation Metal Around Device Inputs (P Package)

6.3 Low-level Output Voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, observe these two conditions. If conditions other than these are to be used, see the *Typical Characteristics* in Section 5.10.

6.4 Input Offset Voltage Temperature Coefficient

Erroneous readings often result from attempts to measure the temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is less than freezing, moisture is able to collect on both the device and the test socket. This moisture results in leakage and contact resistance that potentially causes erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage because the moisture also covers the isolation metal, thereby rendering the techniques useless. Perform these measurements at temperatures greater than freezing to minimize error.

6.5 Full-Power Response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is typically measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal. When the output shows significant distortion, the input frequency is noted as the full-linear bandwidth. The full-peak response is defined as the maximum output frequency, without regard to distortion, at which the full peak-to-peak output swing is maintained. When the output frequency is greater than the full-peak response bandwidth, or maximum output-swing bandwidth, the full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet, and is measured using the circuit of Figure 6-1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 6-5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

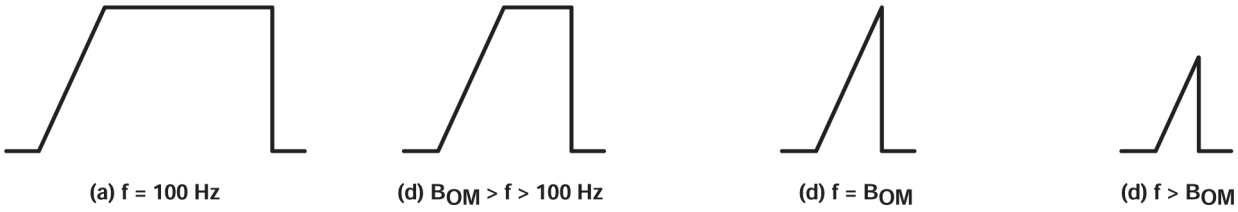


Figure 6-5. Full-Power-Response Output Signal

6.6 Test Time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than bipolar and BiFET devices. The problem becomes more pronounced with reduced supply levels and lower temperatures.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Single-Supply Operation

While the TLV232x performs well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This optimization includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2.7V, thus allowing operation with supply levels typically available for TTL and HCMOS.

Many single-supply applications require that a voltage is applied to one input to establish a reference level that is greater than ground. This virtual ground is generated using two large resistors and a buffer amplifier, such as OPA202.

The TLV232x works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, take the following recommended precautions:

- Power the linear devices from separate bypassed supply lines (see Figure 7-1); otherwise, the linear device supply rails potentially fluctuate as a result of voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling is probably necessary in high-frequency applications.

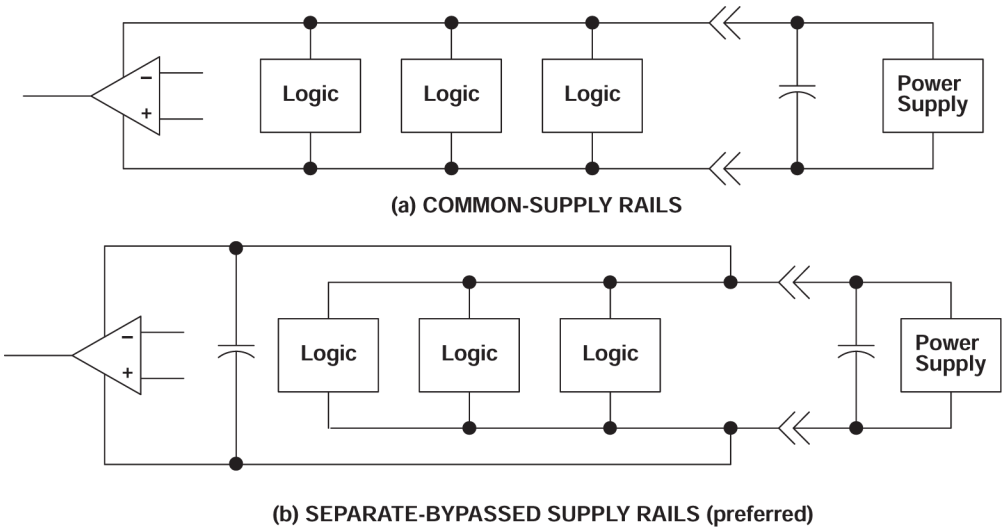


Figure 7-1. Common Versus Separate Supply Rails

7.1.2 Input Characteristics

The TLV232x is specified with a minimum and a maximum input voltage that if exceeded at either input, possibly causes the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1V at T_A = 25°C and at V_{DD} – 1.2V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the legacy TLV232x very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in

CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time is calculated to be typically 0.1µV/month, including the first month of operation.

Migration from the legacy 150mm LinCMOS process to a 300mm diameter wafer process has brought associated improvements to input offset voltage precision, slew rate, phase margin, output current drive capability, and high-level output voltage. However, this change does introduce a new crossover region, where shifts in input offset (typically 300µV–400µV) occur as the input common-mode voltage approaches the V_{DD} rail. Figure 7-2 and Figure 7-3 plot the mean and standard deviation of this characteristic at various temperatures for a 5V supply.

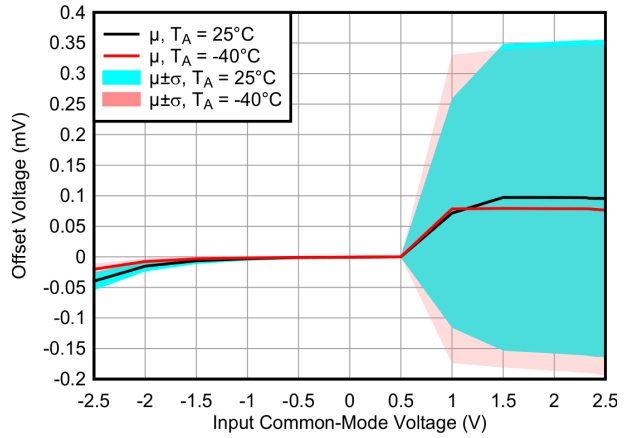


Figure 7-2. Offset Voltage vs Input Common-mode Voltage

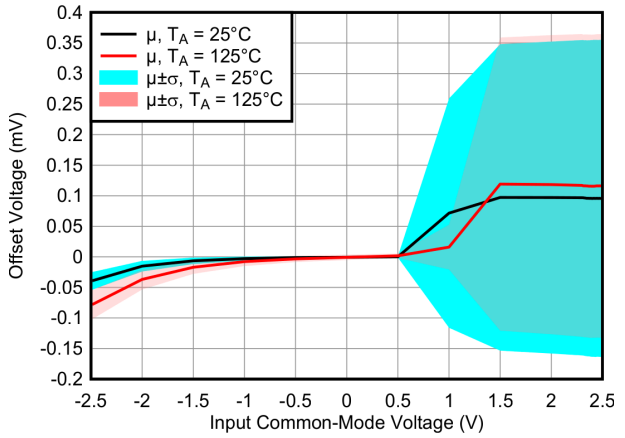


Figure 7-3. Offset Voltage vs Input Common-mode Voltage

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV232x is an excellent choice for low-level signal processing. However, leakage currents on printed-circuit boards and sockets sometimes easily exceed bias-current requirements and cause a degradation in device performance. As best practice, include guard rings around inputs (similar to those of Figure 6-4 in the *Parameter Measurement Information* section). Drive these guards from a low-impedance source at the same voltage level as the common-mode input (see Figure 7-4).

Tie the inputs of any unused amplifiers to ground to avoid possible oscillation.

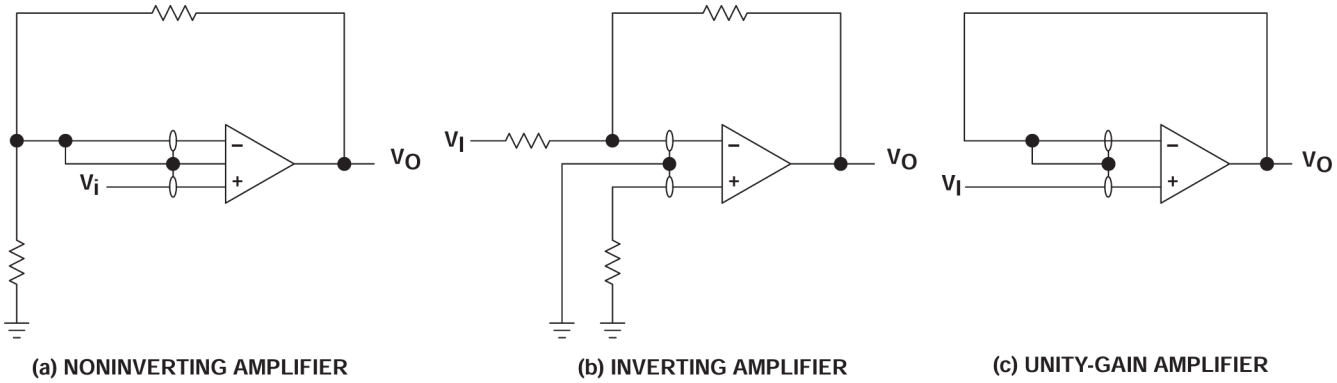


Figure 7-4. Guard-Ring Schemes

7.1.3 Noise Performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLV232x result in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50kΩ because bipolar devices exhibit greater noise currents.

7.1.4 Feedback

Operational amplifier circuits nearly always employ feedback, and because feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 7-5). The value of this capacitor is optimized empirically.

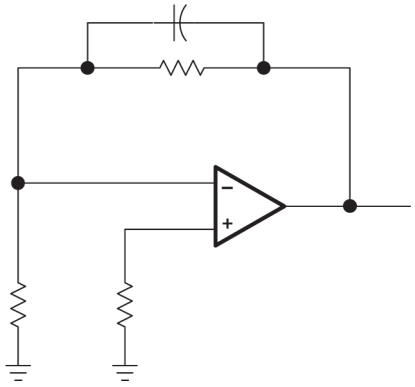


Figure 7-5. Compensation for Input Capacitance

7.1.5 Electrostatic-Discharge Protection

The TLV232x incorporates an internal electrostatic-discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000V as tested under MIL-PRF-38535, Method 3015.2. However, exercise care when handling these devices as exposure to ESD potentially results in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

7.1.6 Latch-Up

Because CMOS devices are susceptible to latch-up due to inherent parasitic thyristors, the TLV232x inputs and outputs are designed to withstand –100mA surge currents without sustaining latch-up. However, use best practices to reduce the chance of latch-up whenever possible. Do not forward bias internal-protection diodes. Do not exceed the supply voltage by more than 300mV for applied input and output voltages. Exercise care when using capacitive coupling on pulse generators. Shunt supply transients by using decoupling capacitors (0.1µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is typically between the positive supply rail and ground, and is triggered by surges on the supply lines, voltages on either the output or inputs that exceed the supply voltage, or both. After latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and typically results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

7.1.7 Output Characteristics

The output stage of the TLV232x is designed to sink and source relatively high amounts of current (see Section 5.10). If the output is subjected to a short-circuit condition, this high-current capability is able to cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV232x possess excellent high-level output voltage and current capability, methods are available to boost this capability, if needed. The simplest method uses a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 7-6). Using this circuit has two disadvantages. First, the NMOS pulldown transistor sinks a comparatively large amount of current. In this circuit, the pulldown transistor behaves like a linear resistor with an on-resistance between approximately 60Ω and 180Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to the pulldown transistor. Thus, the gain of the op amp is reduced at output voltage levels where the corresponding pullup transistor is not supplying the output current.

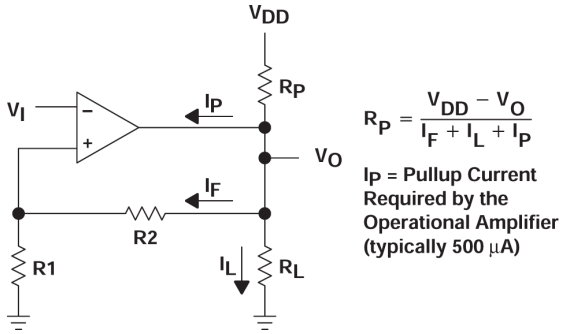


Figure 7-6. Resistive Pullup to Increase v_{OH}

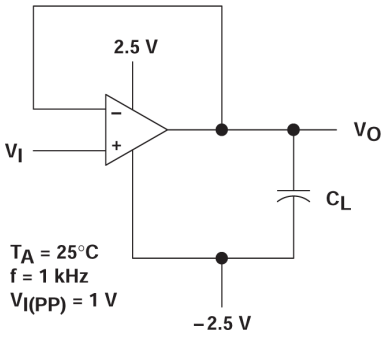
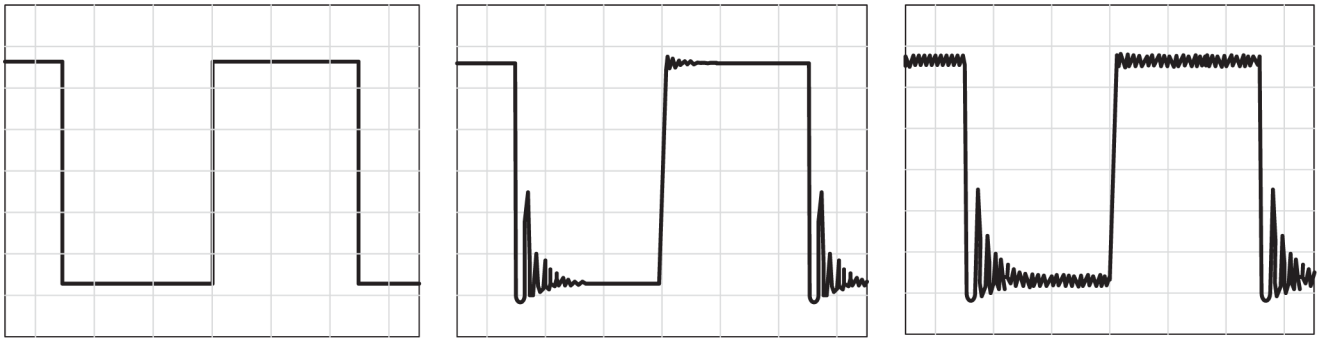


Figure 7-7. Test Circuit for Output Characteristics

All operating characteristics of the TLV232x are measured using a 20pF load. The device drives higher capacitive loads. However, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 7-7 and Figure 7-8). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.



(a) C_L = 20 pF, R_L = NO LOAD

(b) C_L = 260 pF, R_L = NO LOAD

(c) C_L = 310 pF, R_L = NO LOAD

Figure 7-8. Effect of Capacitive Loads

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

LinCMOS™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 1997) to Revision A (July 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *Applications*, *Pin Configuration and Functions*, *Application and Implementation*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Deleted obsolete TLE2322Y and TLE2324Y devices and associated content from data sheet	1
• Changed minimum supply voltage from 2V to 2.7V in *Features*, *Description*, *Recommended Operating Conditions*, *Electrical Characteristics*, *Typical Characteristics*, and *Single-Supply Operation*	1
• Deleted *Equivalent Schematic (Each Amplifier)* section	3
• Added *Pin Configuration and Functions* section with pin descriptions	3
• Added table note that input bias current and input offset current are specified by characterization	5
• Changed typical input offset current from 0.1pA to 0.5pA	5
• Changed minimum input common-mode voltage for T_A = 25°C from −0.3V to −0.2V	5
• Changed typical supply current for V_{DD} = 3V at T_A = 25°C from 12µA to 13µA	5
• Changed minimum CMRR for V_{DD} = 3V at T_A = 25°C from 65dB to 61dB	5
• Changed typical CMRR for V_{DD} = 3V at T_A = 25°C from 88dB to 83dB	5
• Changed minimum CMRR for V_{DD} = 3V across full temp range from 60dB to 59dB	5
• Changed typical CMRR for V_{DD} = 5V at T_A = 25°C from 94dB to 88dB	5
• Added table note that input bias current and input offset current are specified by characterization	7
• Changed typical input offset current from 0.1pA to 0.5pA	7
• Changed minimum input common-mode voltage for T_A = 25°C from −0.3V to −0.2V	7

- Changed typical supply current for V_{DD} = 3V at T_A = 25°C from 24µA to 26µA....7
- Changed minimum CMRR for V_{DD} = 3V at T_A = 25°C from 65dB to 61dB 7
- Changed typical CMRR for V_{DD} = 3V from 88dB to 83dB at T_A = 25°C....7
- Changed minimum CMRR for V_{DD} = 3V across full temp range from 60dB to 59dB....7
- Changed typical CMRR for V_{DD} = 5V at T_A = 25°C from 94dB to 88dB....7
- Updated Figures 5-10, 5-12, 5-23, 5-26, 5-31, and 5-34....9
- Updated description of full-linear and full-peak responses in *Full-Power Response* 18
- Deleted Figure 40 and updated virtual ground generation guidance in *Single-supply Operation* 19
- Added guidance concerning changes to input crossover region to *Input Characteristics* 19

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2322ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	2322I
TLV2322IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2322I
TLV2322IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2322I
TLV2322IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLV2322IP
TLV2322IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLV2322IP
TLV2322IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2322
TLV2322IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2322
TLV2324ID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	TLV2324I
TLV2324IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV2324I
TLV2324IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV2324I
TLV2324IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLV2324IN
TLV2324IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLV2324IN
TLV2324IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2324
TLV2324IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2324

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

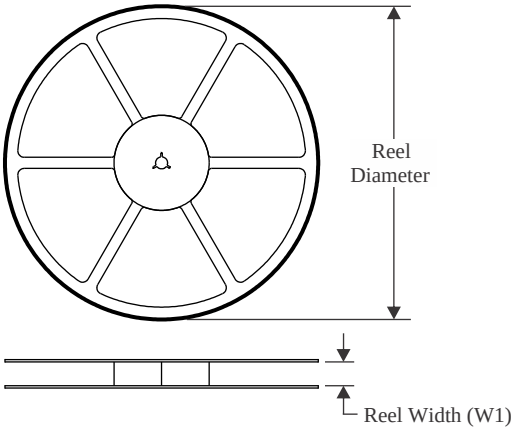
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

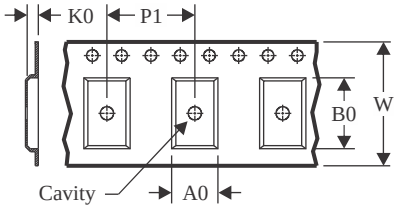
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

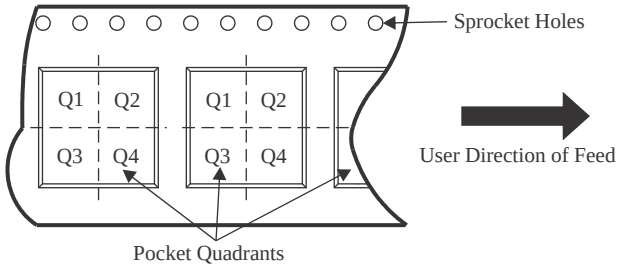


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

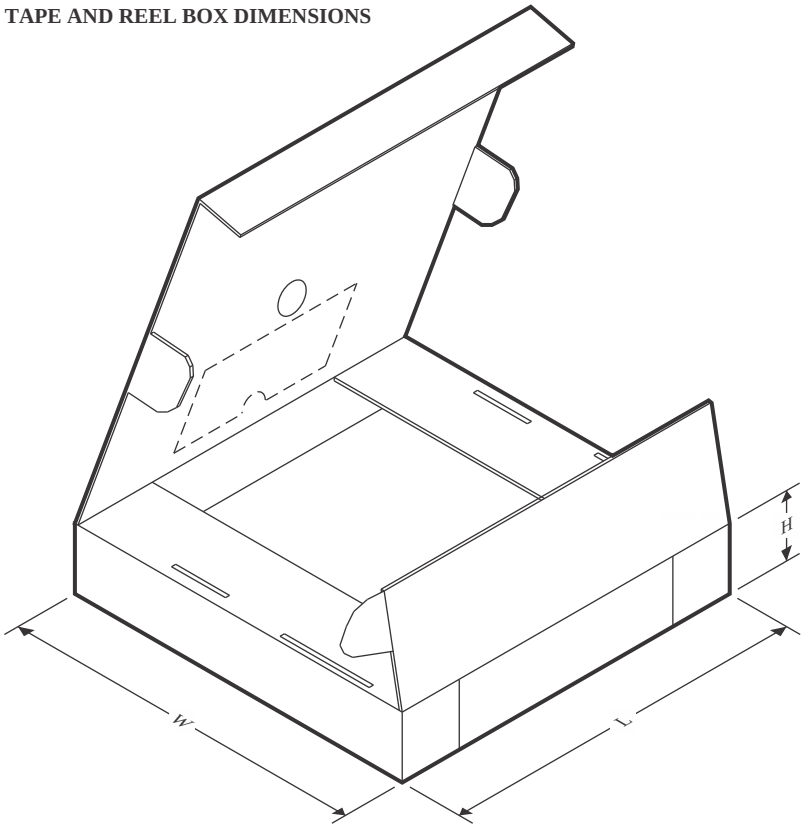
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2322IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2322IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2322IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2324IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2324IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

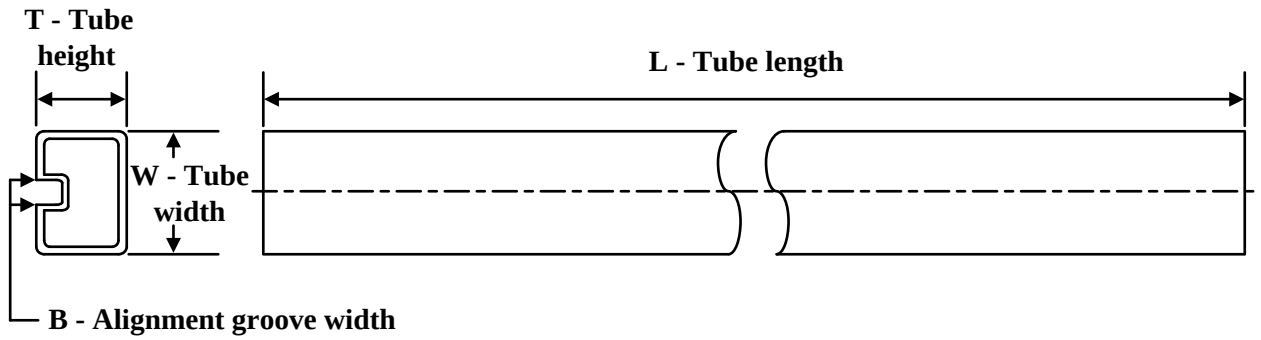
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

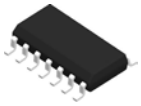
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2322IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2322IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2322IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLV2324IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2324IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV2322IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2322IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLV2324IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2324IN.A	N	PDIP	14	25	506	13.97	11230	4.32

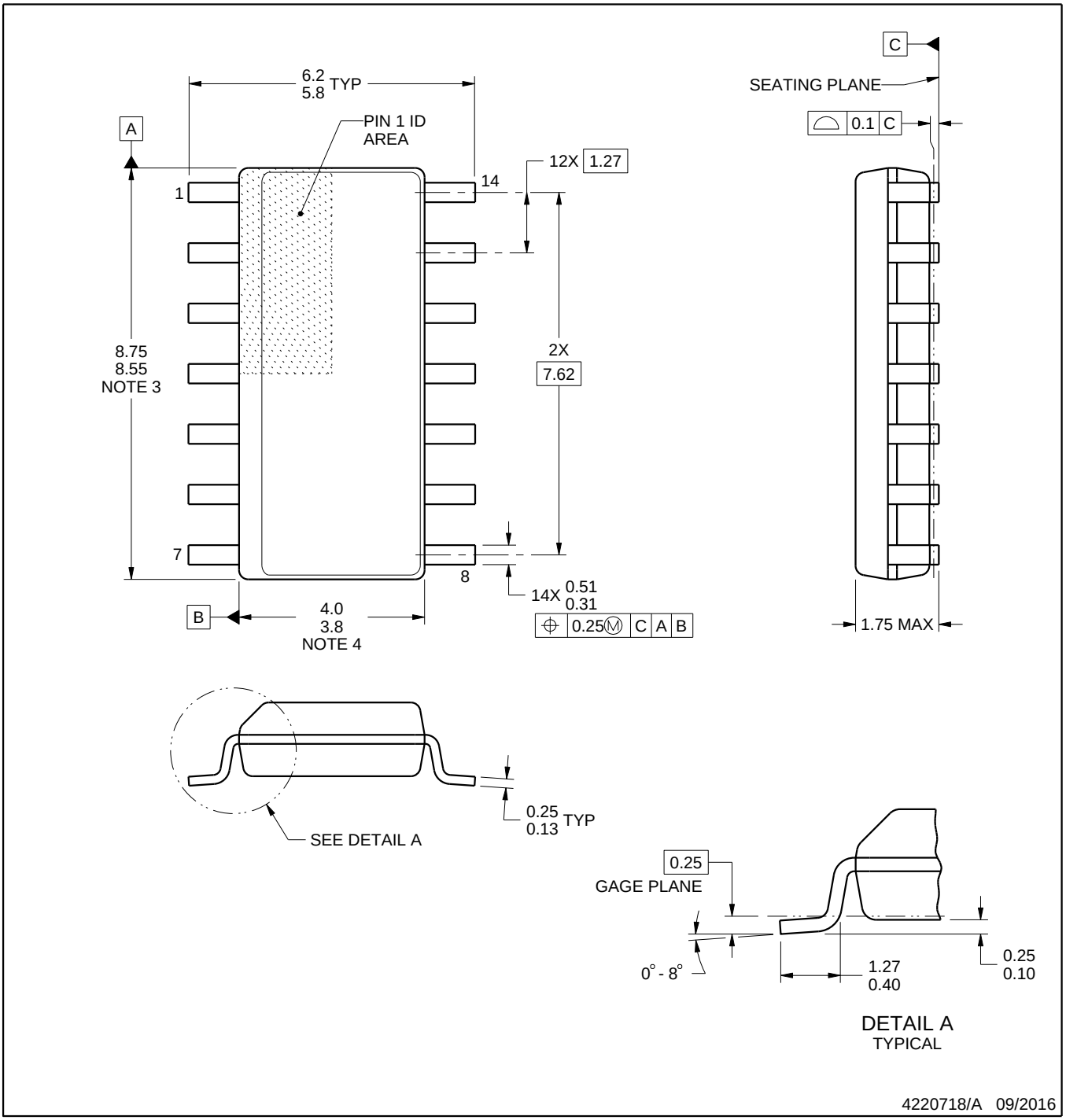


PACKAGE OUTLINE

D0014A

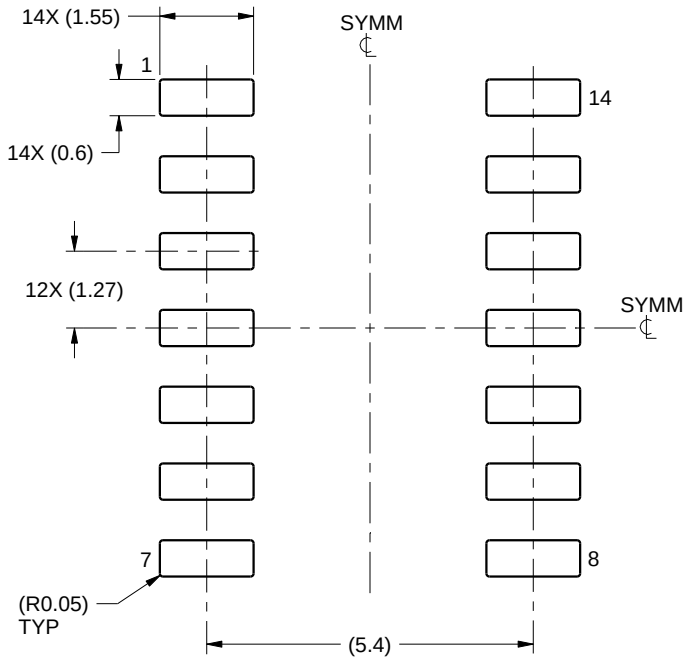
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

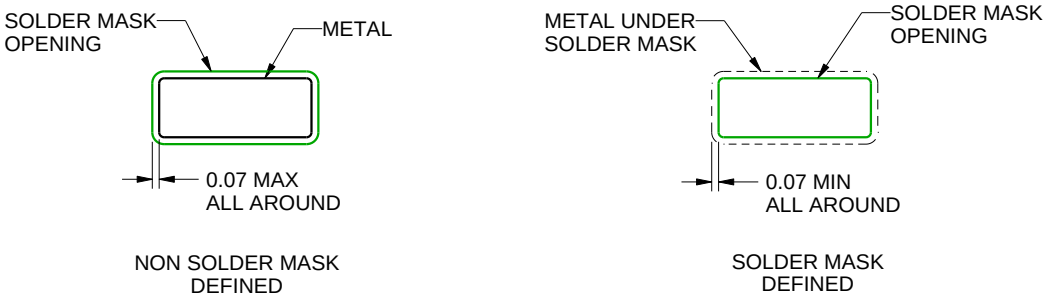


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

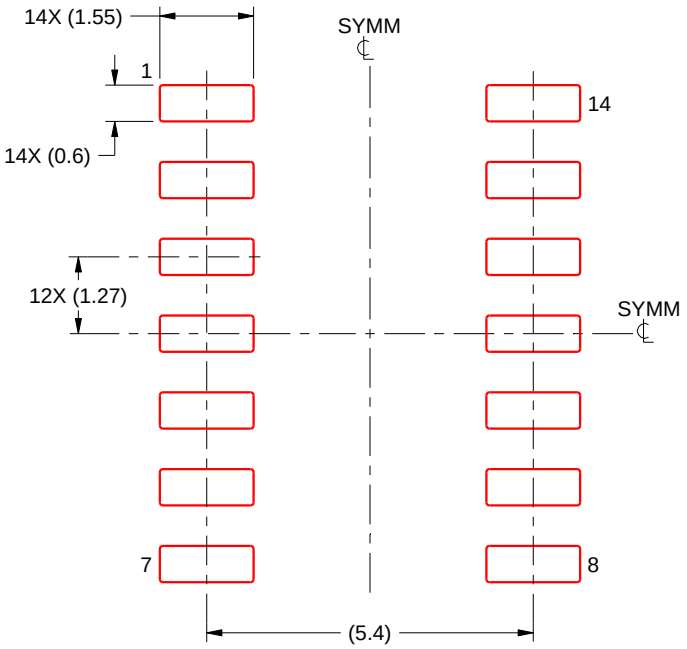
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

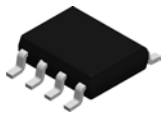


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

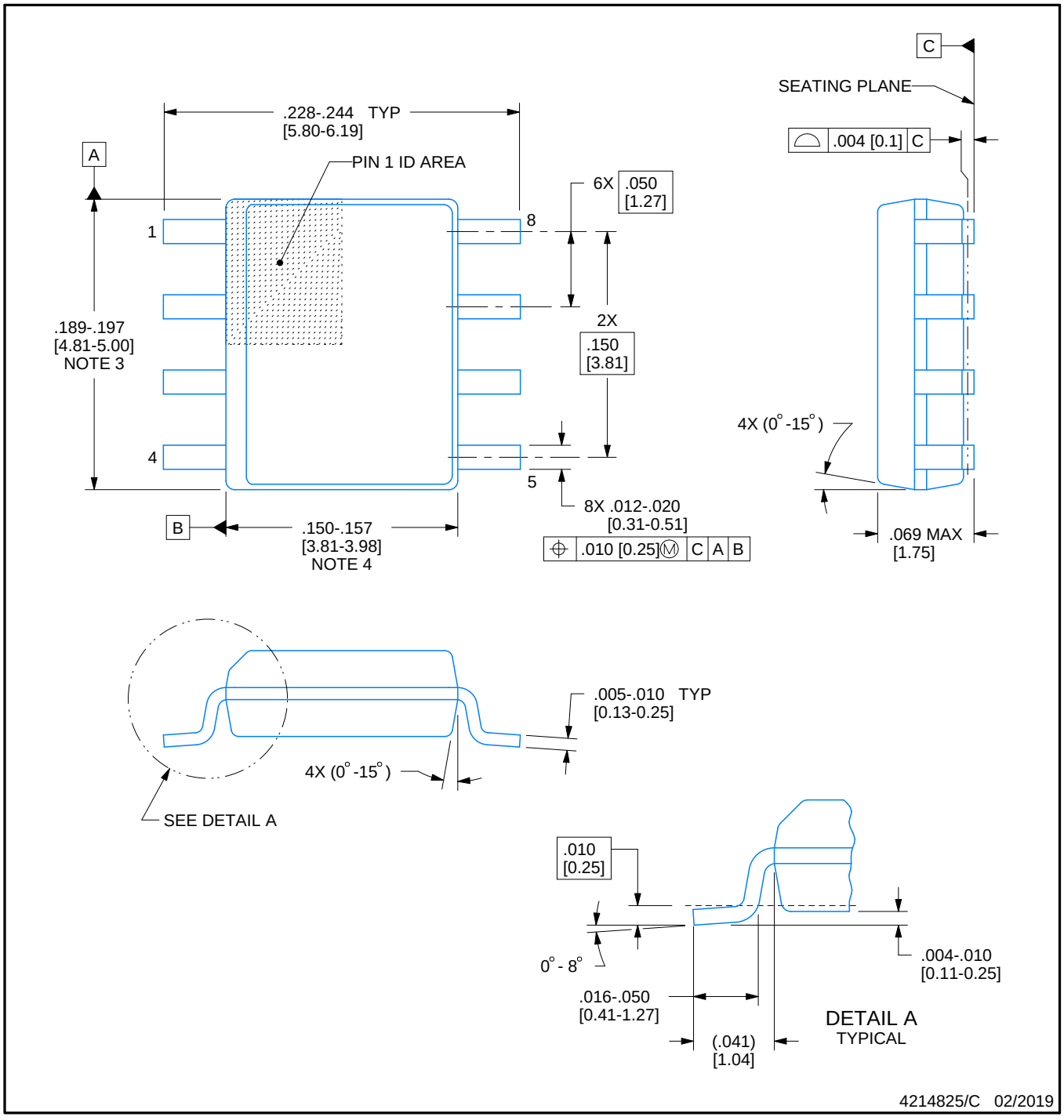


PACKAGE OUTLINE

D0008A

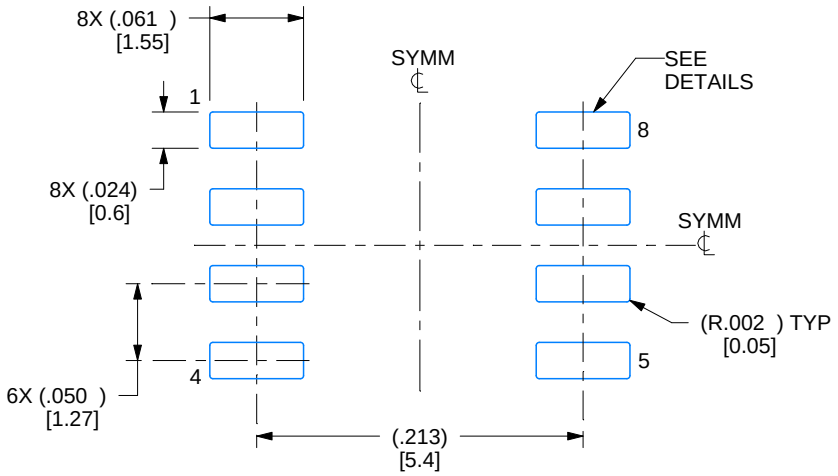
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

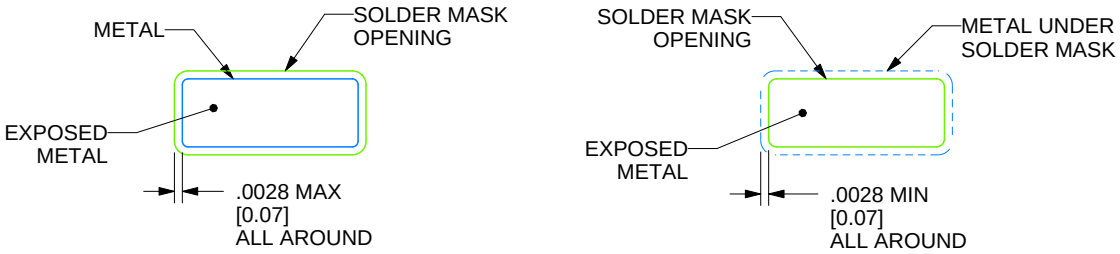


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

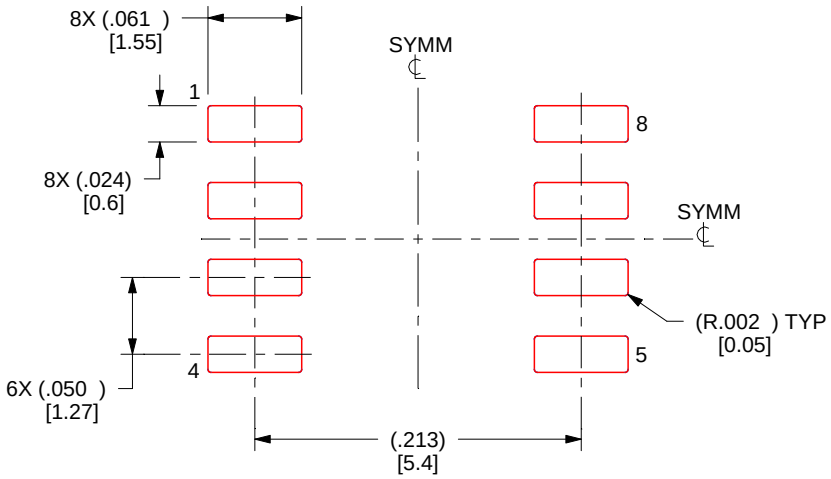
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



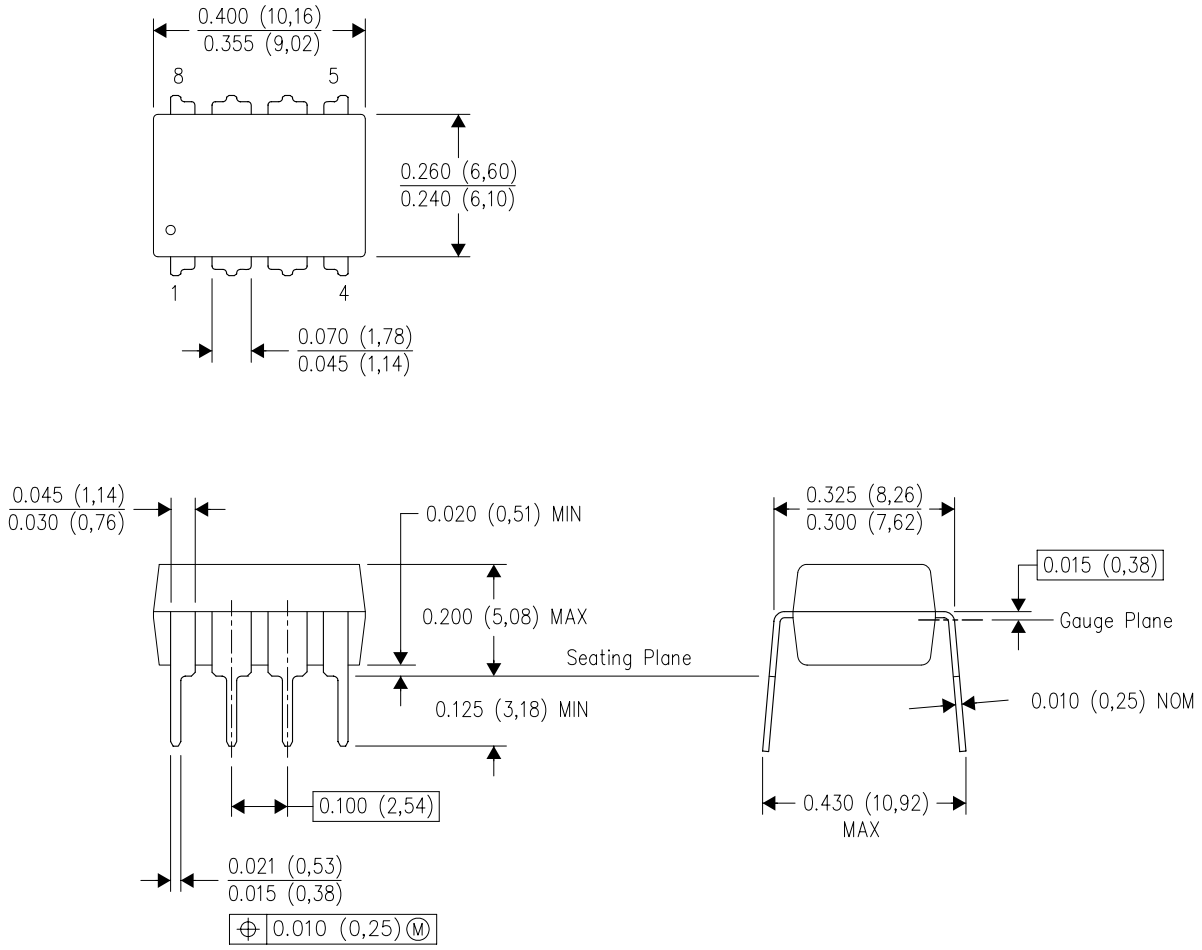
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

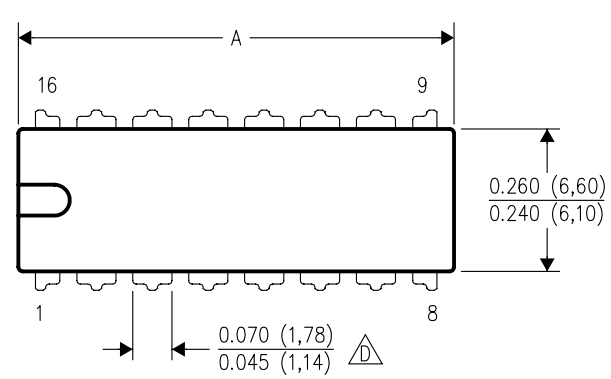


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

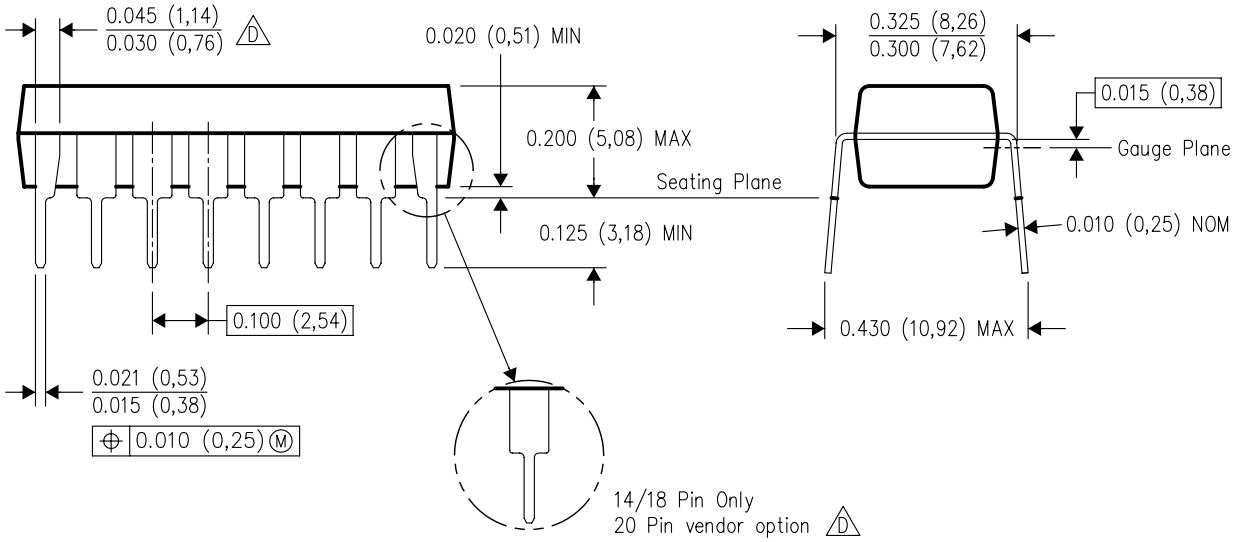
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

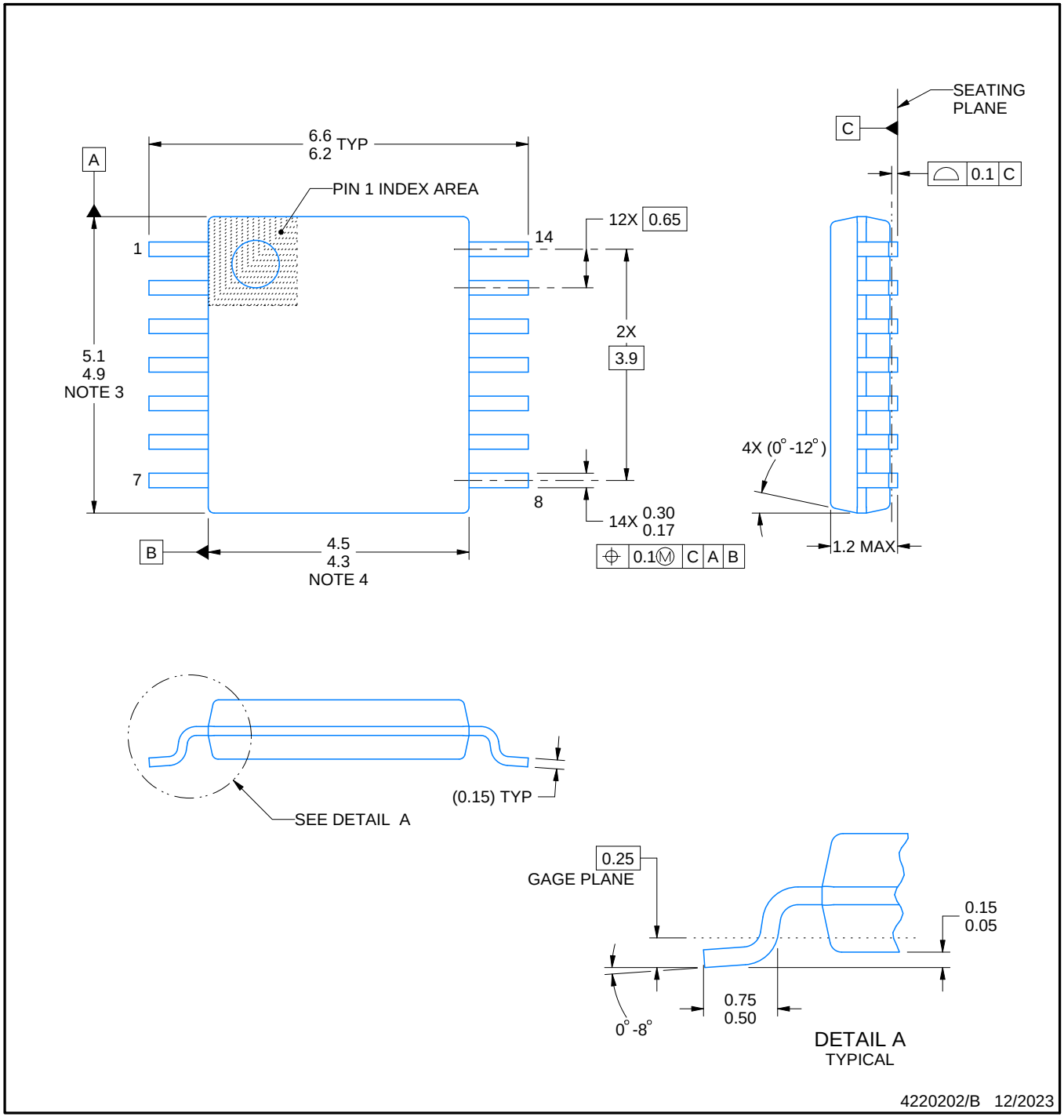
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

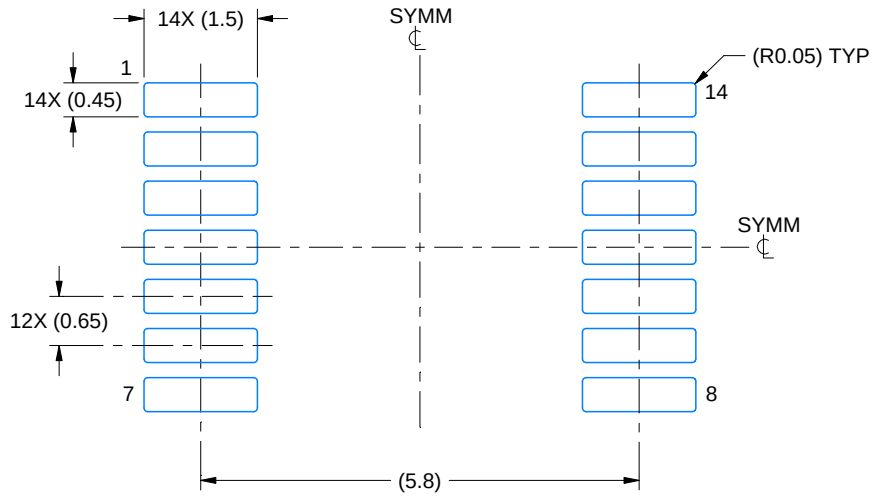
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

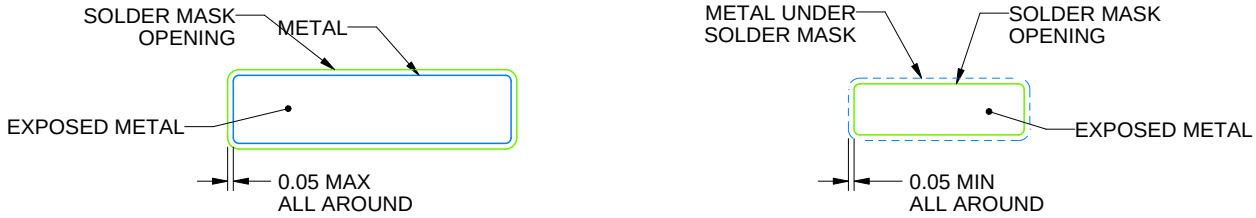


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

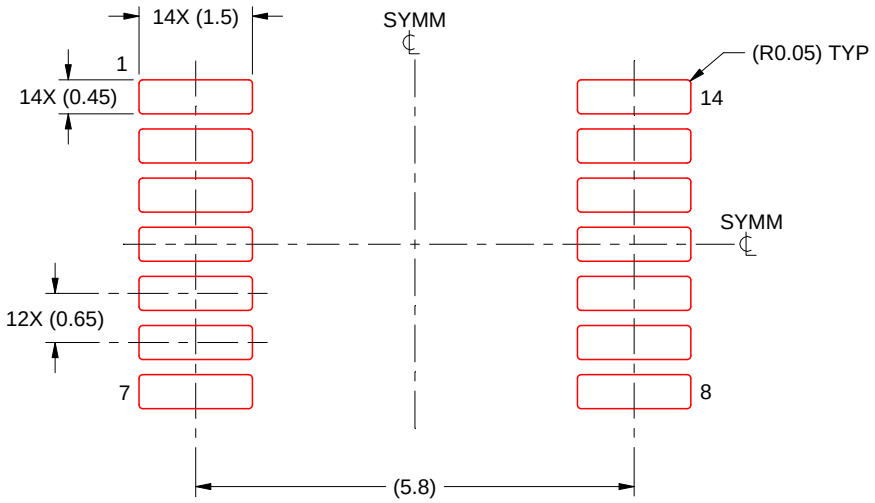


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

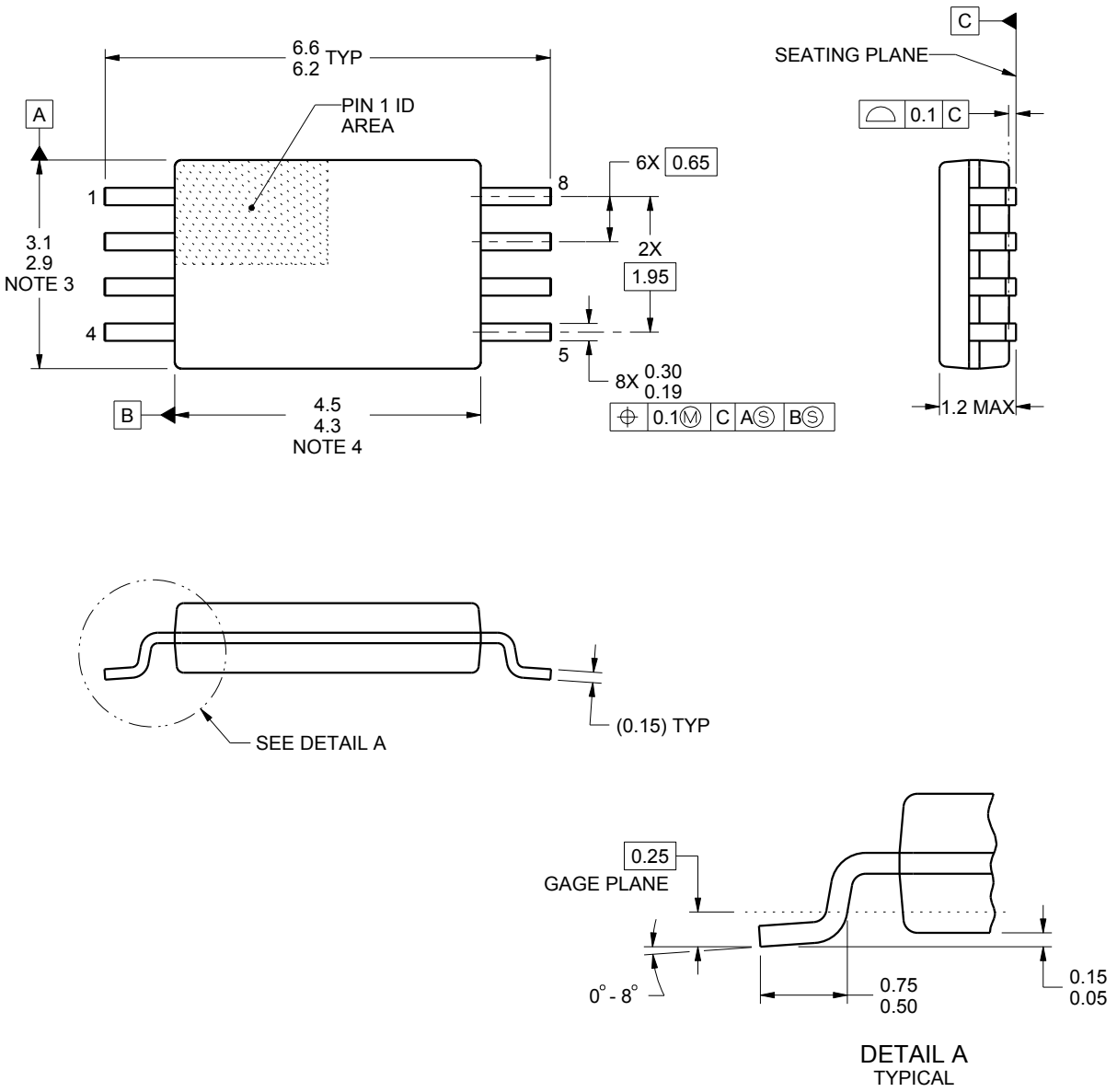
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

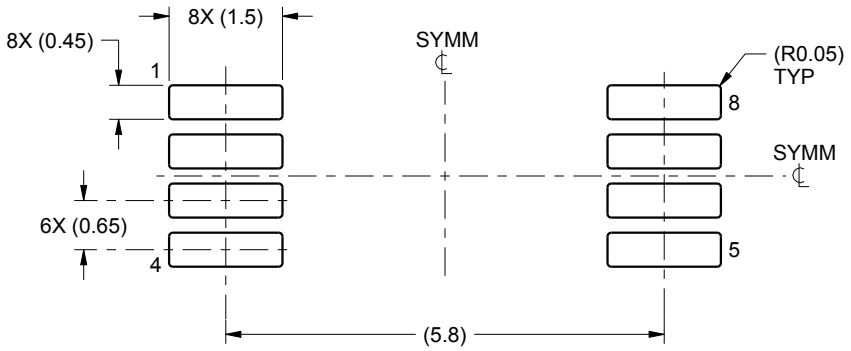
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

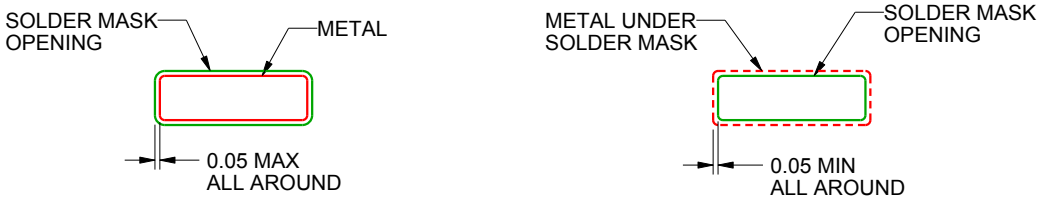


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

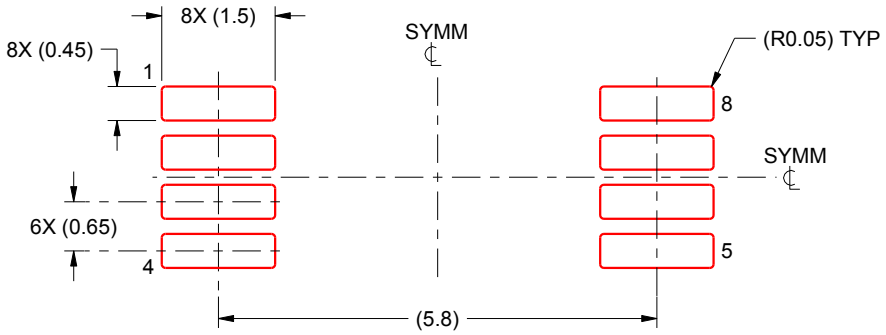


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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