TLV1704-SEP 2.2V to 24V, Radiation-Tolerant microPower Quad Comparator in Space Enhanced Plastic

1 Features

- VID V62/18613
- Radiation-Tolerant
  - Single Event Latch-up (SEL) immune to 43MeV-cm^2/mg at 125°C
  - ELDRS free to 30krad(Si)
  - Total Ionizing Dose (TID) rlat for every wafer lot up to 30krad(Si)
- Space enhanced plastic
  - Controlled baseline
  - Gold wire
  - NiPdAu lead finish
  - One assembly and test site
  - One fabrication site
  - Available in military (–55°C to 125°C) temperature range
  - Extended product life cycle
  - Extended product-change notification
  - Product traceability
  - Enhanced mold compound for low outgassing
- Supply range: 2.2V to 24V
- Low quiescent current: 55µA per comparator
- Input common-mode range includes both rails
- Low propagation delay: 560ns
- Low input offset voltage: 300µV
- Open collector outputs:
  - Up to 24V above negative supply regardless of supply voltage
- Small packages:
  - Quad: TSSOP-14

2 Applications

- Command & data handling (C&DH)
- Aircraft cockpit display
- Flight control unit
- Satellite electrical power system (EPS)

3 Description

The TLV1704-SEP (Quad) device offers a wide supply range, rail-to-rail inputs, low quiescent current, and low propagation delay. All these features come in an industry-standard, TSSOP-14 plastic package, making these devices appropriate for applications where size, weight, and design flexibility are important..

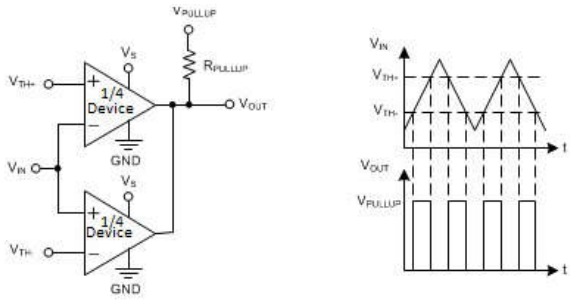
The open-collector output offers the advantage of allowing the output to be level shifted to any voltage rail up to 24V above the negative power supply, regardless of the TLV1704-SEP supply voltage. Likewise, the outputs can be wired together to form a single alert signal.

The device is a microPower comparator. Low input offset voltage, low input bias currents, low supply current, and open-collector configuration make the TLV1704-SEP device well-suited for system diagnostics such as voltage monitoring, current sensing, and zero-cross detection.

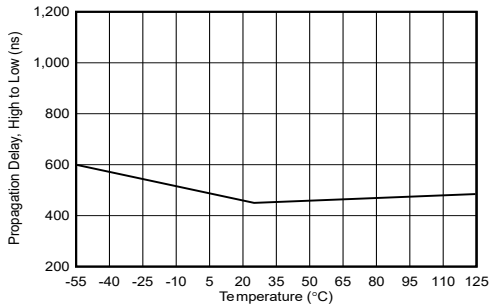
Device Information

PART NUMBER	GRADE (1)	PACKAGE (2)
TLV1704AMPWTPSEP	30krad(Si) RLAT	TSSOP (14)
TLV1704AMPWPSEP		

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TLV1704-SEP as a Window Comparator



Stable Propagation Delay vs Temperature

Table of Contents

4 Pin Configuration and Functions

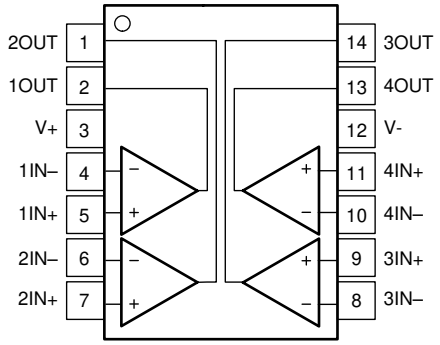


Figure 4-1. TLV1704-SEP PW Package
14-Pin TSSOP
Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	—	I	Noninverting input.
1IN+	5	I	Noninverting input, channel 1.
2IN+	7	I	Noninverting input, channel 2.
3IN+	9	I	Noninverting input, channel 3.
4IN+	11	I	Noninverting input, channel 4.
IN–	—	I	Inverting input.
1IN–	4	I	Inverting input, channel 1.
2IN–	6	I	Inverting input, channel 2.
3IN–	8	I	Inverting input, channel 3.
4IN–	10	I	Inverting input, channel 4.
OUT	—	O	Output.
1OUT	2	O	Output, channel 1.
2OUT	1	O	Output, channel 2.
3OUT	14	O	Output, channel 3.
4OUT	13	O	Output, channel 4.
V+	3	—	Positive (highest) power supply.
V–	12	—	Negative (lowest) power supply.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage			24	V
Signal input pins	Voltage(2)	(V_S–) – 0.5	(V_S+) + 0.5	V
	Current(2)		±10	mA
Output short-circuit(3)		Continuous		mA
Operating Junction temperature, T_J		–55	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(3) Short-circuit to ground; one comparator per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage V_S = (V_S+) – (V_S–)	2.2		24	V
Specified temperature	–55		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TLV1704-SEP PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_A = –55°C to 125°C, V_S = 2.2V to 24V, C_L = 15pF, R_{PULLUP} = 5.1kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C, V_S = 2.2V		±0.5	±3.5	mV
		T_A = 25°C, V_S = 24V		±0.3	±2.5	mV
		T_A = –55°C to 125°C			±5.5	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –55°C to 125°C		±4	±20	µV/°C
PSRR	Power-supply rejection ratio	T_A = 25°C		15	100	µV/V
		T_A = –55°C to 125°C		20		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –55°C to 125°C	(V–)		(V+)	V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		5	15	nA
		T_A = –55°C to 125°C			20	nA
I_{OS}	Input offset current	T_A = 25°C		0.5		nA
C_{LOAD}	Capacitive load drive		See *Section 5.7*			
OUTPUT						
V_O	Voltage output swing from rail	I_O ≤ 4mA, input overdrive = 100mV, V_S = 24V			1100	mV
		I_O = 0mA, input overdrive = 100mV, V_S = 24V			700	mV
I_{SC}	Short circuit sink current	T_A = 25°C		20		mA
	Output leakage current	V_{IN+} > $V_{IN–}$, T_J = 25°C		70		nA
POWER SUPPLY						
V_S	Specified voltage range		2.2		24	V
I_Q	Quiescent current (per channel)	I_O = 0A , T_A = 25°C		55	75	µA
		I_O = 0A, T_A = –55°C to 125°C			100	µA

5.6 Switching Characteristics

at T_A = –55°C to 125°C, V_S = 2.2V to 24V, C_L = 15pF, R_{PULLUP} = 5.1kΩ, V_{CM} = V_S / 2, and V_S = V_{PULLUP} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHL}	Propagation delay time, high-to-low	Input overdrive = 100mV, T_A = 25°C		460		ns
t_{pLH}	Propagation delay time, low-to-high	Input overdrive = 100mV, T_A = 25°C		560		ns
t_R	Rise time	Input overdrive = 100mV, T_A = 25°C		365		ns
t_F	Fall time	Input overdrive = 100mV, T_A = 25°C		240		ns

5.7 Typical Characteristics

at T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1kΩ, and input overdrive = 100mV (unless otherwise noted)

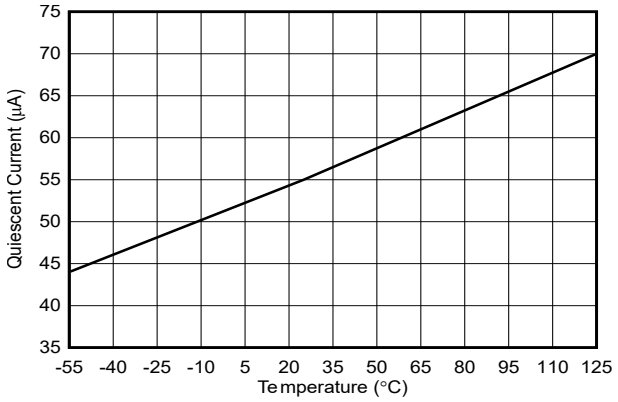


Figure 5-1. Quiescent Current vs Temperature

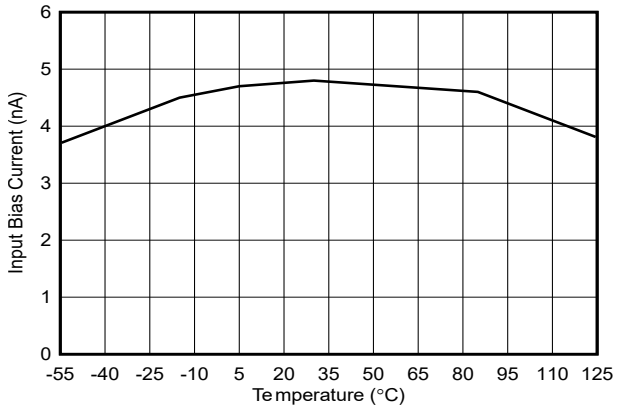


Figure 5-2. Input Bias Current vs Temperature

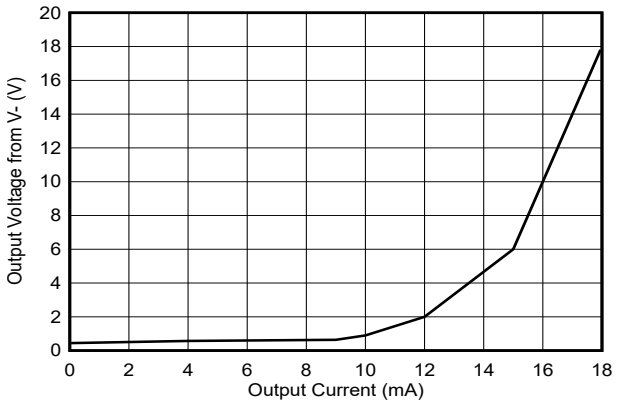
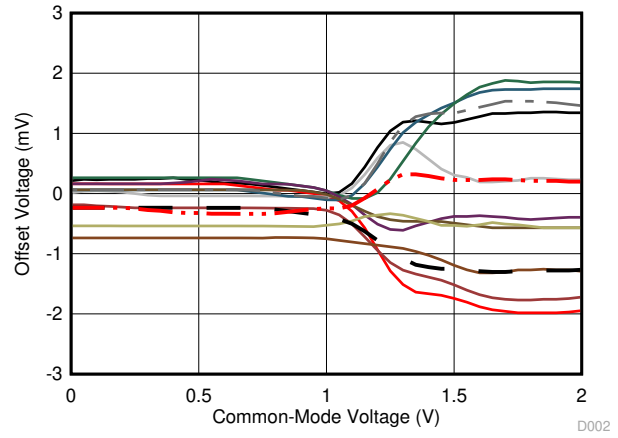


Figure 5-3. Output Voltage vs Output Current



V_S = 2.2V 13 typical units shown

Figure 5-4. Offset Voltage vs Common-Mode Voltage

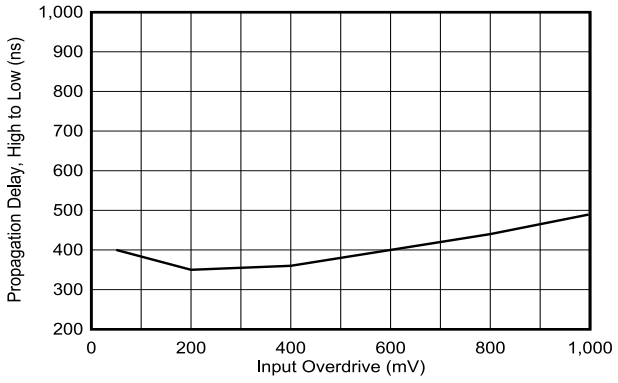
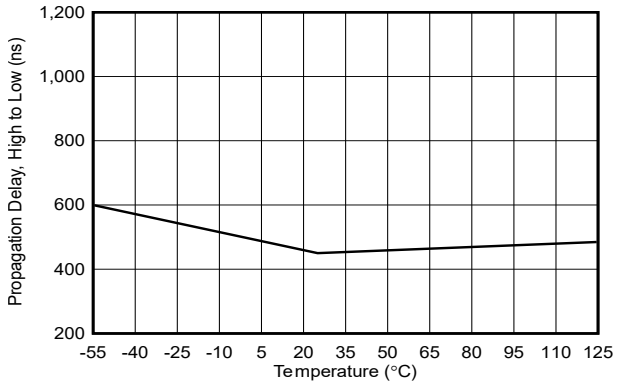


Figure 5-5. Propagation Delay vs Input Overdrive

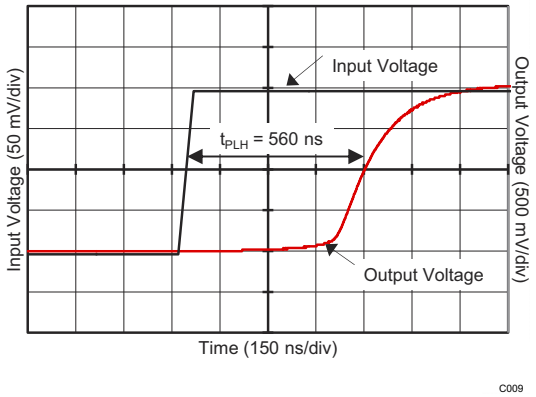


V_{OD} = 100mV

Figure 5-6. Propagation Delay vs Temperature

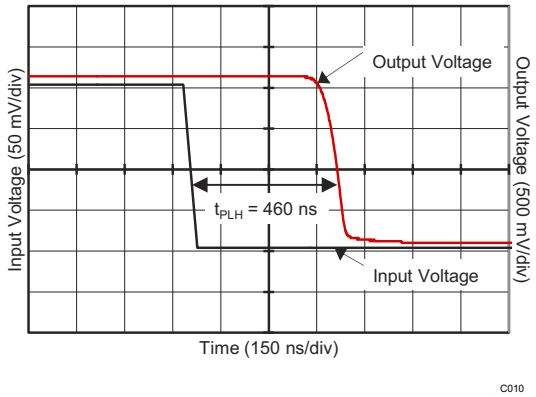
5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1kΩ, and input overdrive = 100mV (unless otherwise noted)



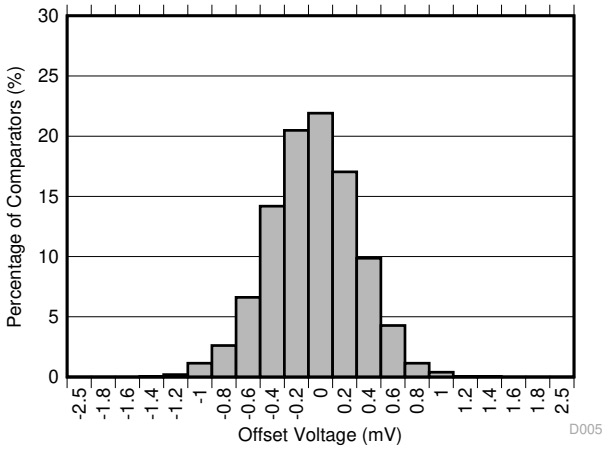
V_S = 2.2V Overdrive = 100mV

Figure 5-7. Propagation Delay (T_{pLH})



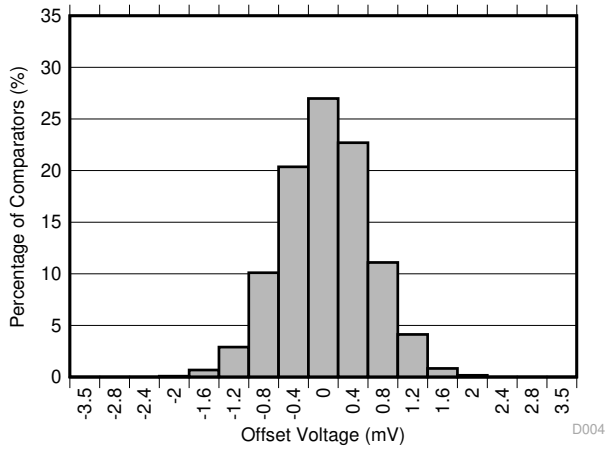
V_S = 2.2V Overdrive = 100mV

Figure 5-8. Propagation Delay (T_{pHL})



V_S = 24V Distribution taken from 2524 comparators

Figure 5-9. Offset Voltage Production Distribution



V_S = 2.2V Distribution taken from 2524 comparators

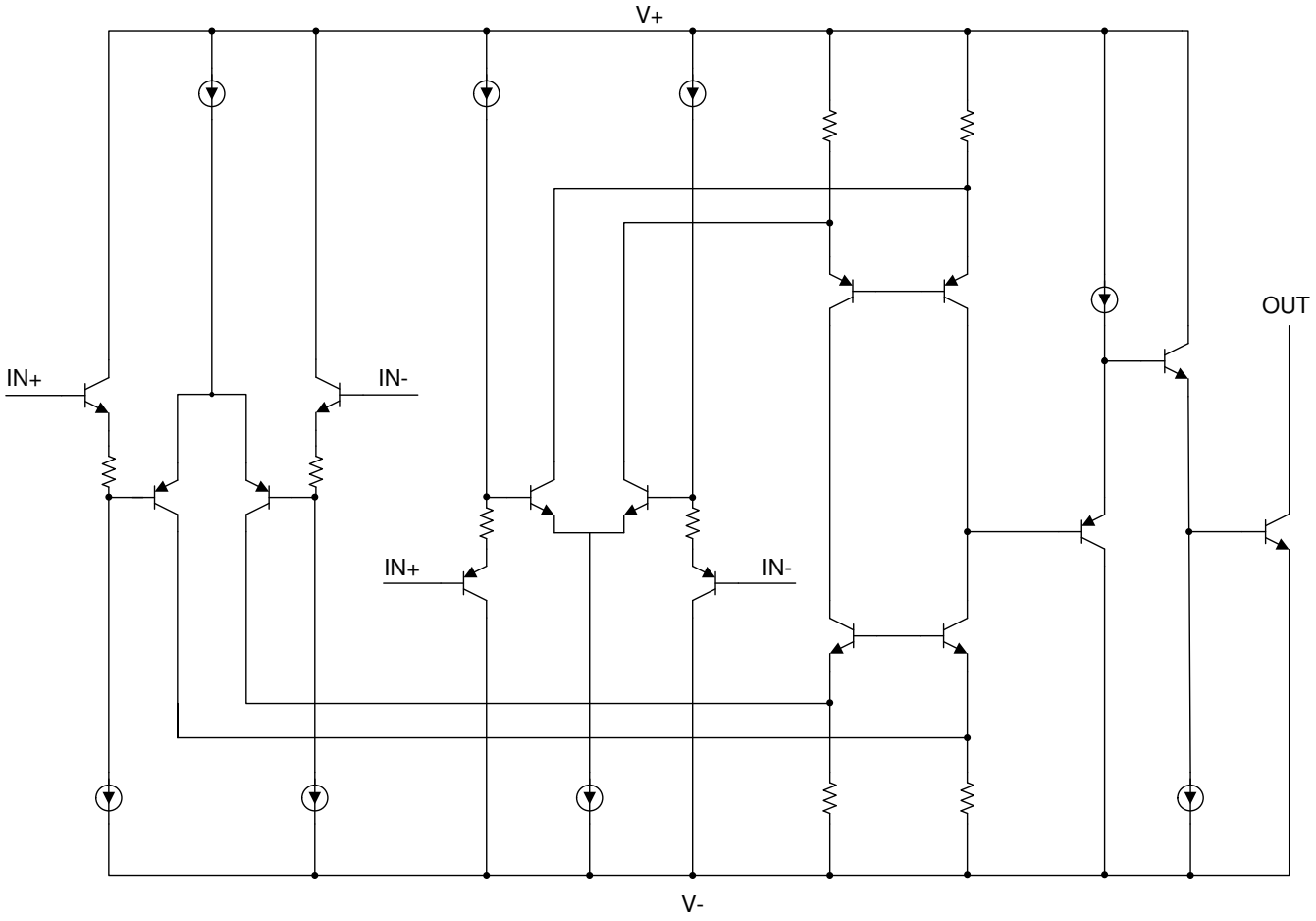
Figure 5-10. Offset Voltage Production Distribution

6 Detailed Description

6.1 Overview

The TLV1704-SEP comparator features rail-to-rail input and output on supply voltages as high as 24V. The rail-to-rail input stage enables detection of signals close to the supply and ground. The open-collector configuration allows the device to be used in wired-OR configurations, such as a window comparator. A low supply current of 55µA per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Comparator Inputs

The TLV1704-SEP device is a rail-to-rail input comparator, with an input common-mode range that includes the supply rails. The TLV1704-SEP device is designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 6-1 shows the TLV1704-SEP device response when input voltages exceed the supply, resulting in no phase inversion.

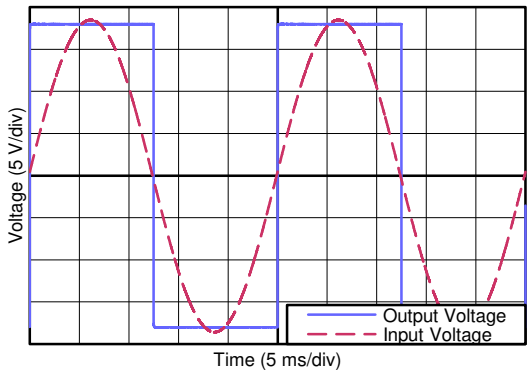


Figure 6-1. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

6.4 Device Functional Modes

6.4.1 Setting Reference Voltage

Using a stable reference is important when setting the transition point for the TLV1704-SEP device. The REF3333, as shown in Figure 6-2, provides a 3.3V reference voltage with low drift and only 3.9µA of quiescent current.

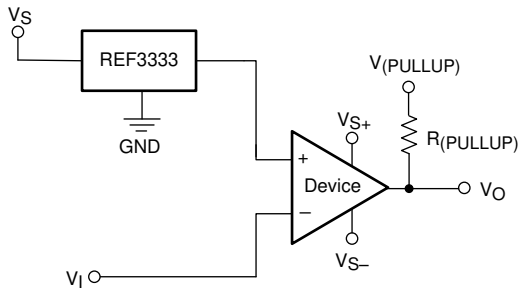


Figure 6-2. Reference Voltage for the TLV1704-SEP

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV1704-SEP device can be used in a wide variety of applications, such as zero crossing detectors, window comparators, over and undervoltage detectors, and high-side voltage sense circuits.

7.2 Typical Application

Comparators are used to differentiate between two different signal levels. For example, a comparator differentiates between an overtemperature and normal-temperature condition. However, noise or signal variation at the comparison threshold causes multiple transitions. This application example sets upper and lower hysteresis thresholds to eliminate the multiple transitions caused by noise.

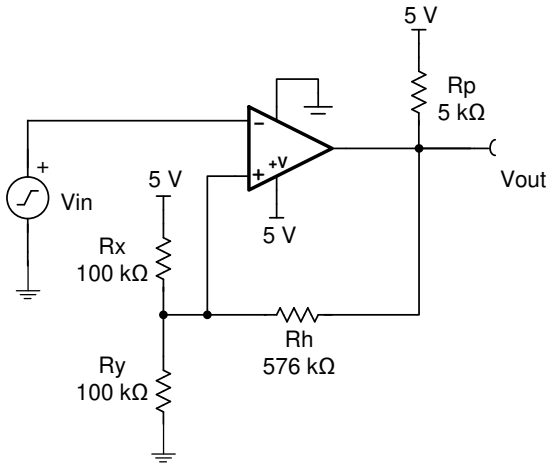


Figure 7-1. Comparator Schematic With Hysteresis

7.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5V
- Input: 0V to 5V
- Lower threshold (VL) = 2.3V ±0.1V
- Upper threshold (VH) = 2.7V ±0.1V
- VH – VL = 2.4V ±0.1V
- Low-power consumption

7.2.2 Detailed Design Procedure

Make a small change to the comparator circuit to add hysteresis. Hysteresis uses two different threshold voltages to avoid the multiple transitions introduced in the previous circuit. The input signal must exceed the upper threshold (VH) to transition low, or below the lower threshold (VL) to transition high.

Figure 7-1 illustrates hysteresis on a comparator. Resistor Rh sets the hysteresis level. An open-collector output stage requires a pullup resistor (Rp). The pullup resistor creates a voltage divider at the comparator output that introduces an error when the output is at logic high. This error can be minimized if Rh > 100 Rp.

When the output is at a logic high (5V), Rh is in parallel with Rx (ignoring Rp). This configuration drives more current into Ry, and raises the threshold voltage (VH) to 2.7V. The input signal must drive above VH = 2.7V to cause the output to transition to logic low (0V).

When the output is at logic low (0V), Rh is in parallel with Ry. This configuration reduces the current into Ry, and reduces the threshold voltage to 2.3V. The input signal must drive below VL = 2.3V to cause the output to transition to logic high (5V).

For more details on this design and other alternative devices that can be used in place of the TLV1702, refer to Precision Design TIPD144, *Comparator with Hysteresis Reference Design*.

7.2.3 Application Curve

Figure 7-2 shows the upper and lower thresholds for hysteresis. The upper threshold is 2.76V and the lower threshold is 2.34V, both of which are close to the design target.

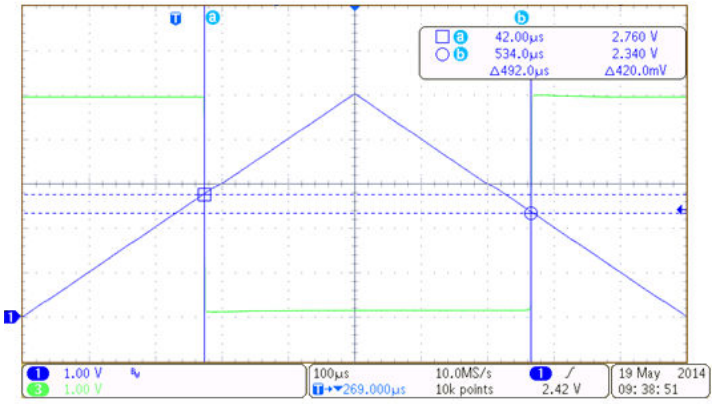


Figure 7-2. TLV1701 Upper and Lower Threshold With Hysteresis

7.3 Power Supply Recommendations

The TLV1704-SEP device is specified for operation from 2.2V to 24V; many specifications apply from –55°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Section 5.7* section.

CAUTION

Supply voltages larger than 40V can permanently damage the device; see the *Section 5.1* .

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the *Section 7.4.1* section.

7.4 Layout

7.4.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the TLV1704-SEP device.
- To minimize supply noise, place a decoupling capacitor (0.1µF ceramic, surface-mount capacitor) as close as possible to V_S as shown in Figure 7-3.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

7.4.2 Layout Example

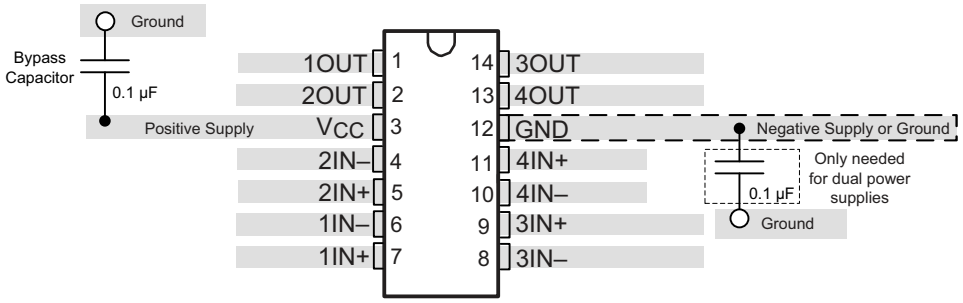


Figure 7-3. Comparator Board Layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- *Precision Design, Comparator with Hysteresis Reference Design* , TIDU020
- *REF33xx 3.9-µA, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/°C Drift Voltage Reference* , SBOS392

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2022) to Revision B (July 2024)	Page
• Changed maximum supply voltage from 36V to 24V	1
• Changed device grade in the *Device Information* table from 20krad(Si) RLAT to 30krad(Si) RLAT	1
• Updated formatting for measurements throughout the document	1
• Updated the *Typical Performance Characteristics* graphs	6

Changes from Revision * (November 2018) to Revision A (November 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the title from Radiation Hardened to Radiation-Tolerant	1
• Updated Applications with links	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1704AMPWPSEP	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP
TLV1704AMPWTPSEP	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP
V62/18613-01XE	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP
V62/18613-01XE-T	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV1704-SEP :

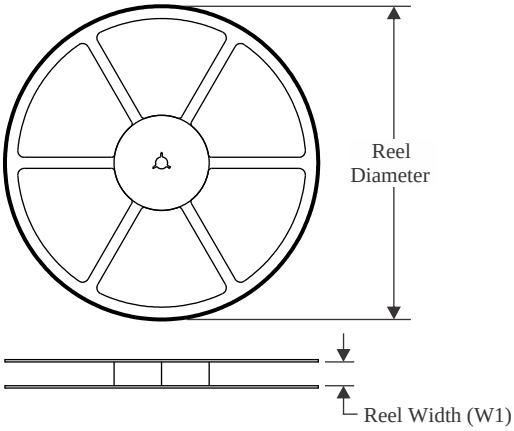
- Automotive : TLV1704-Q1

NOTE: Qualified Version Definitions:

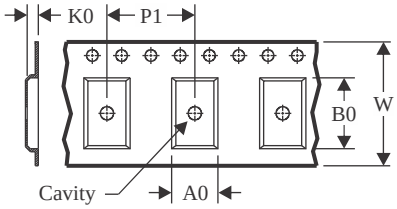
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

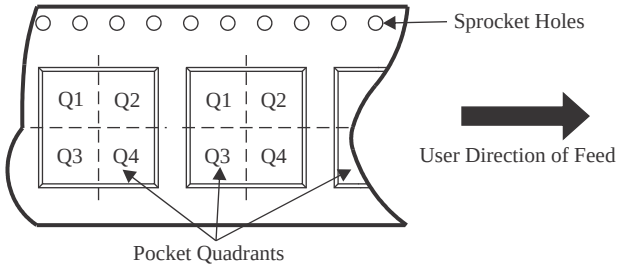


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

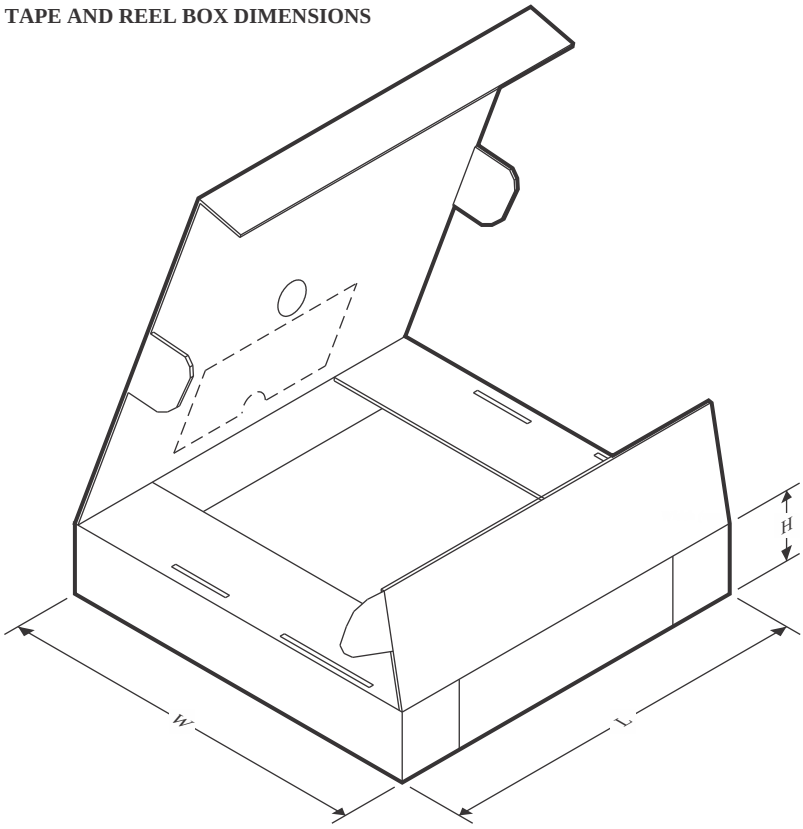
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1704AMPWTPSEP	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

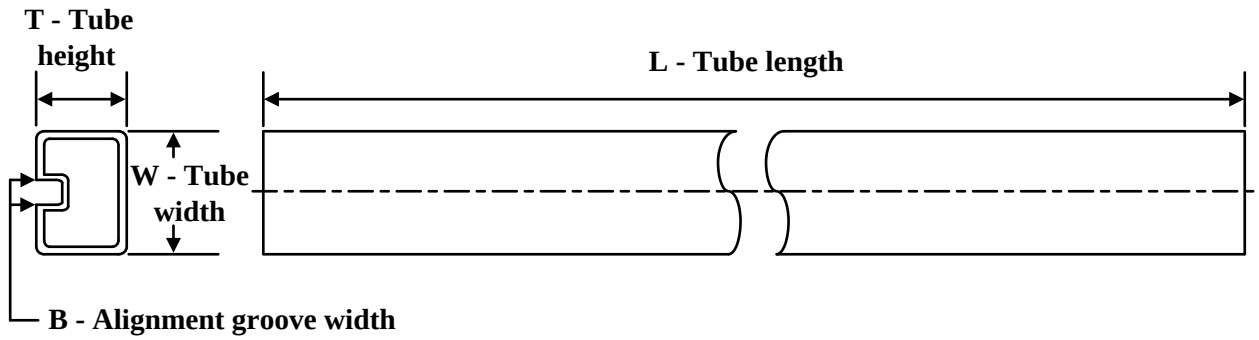
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1704AMPWTPSEP	TSSOP	PW	14	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

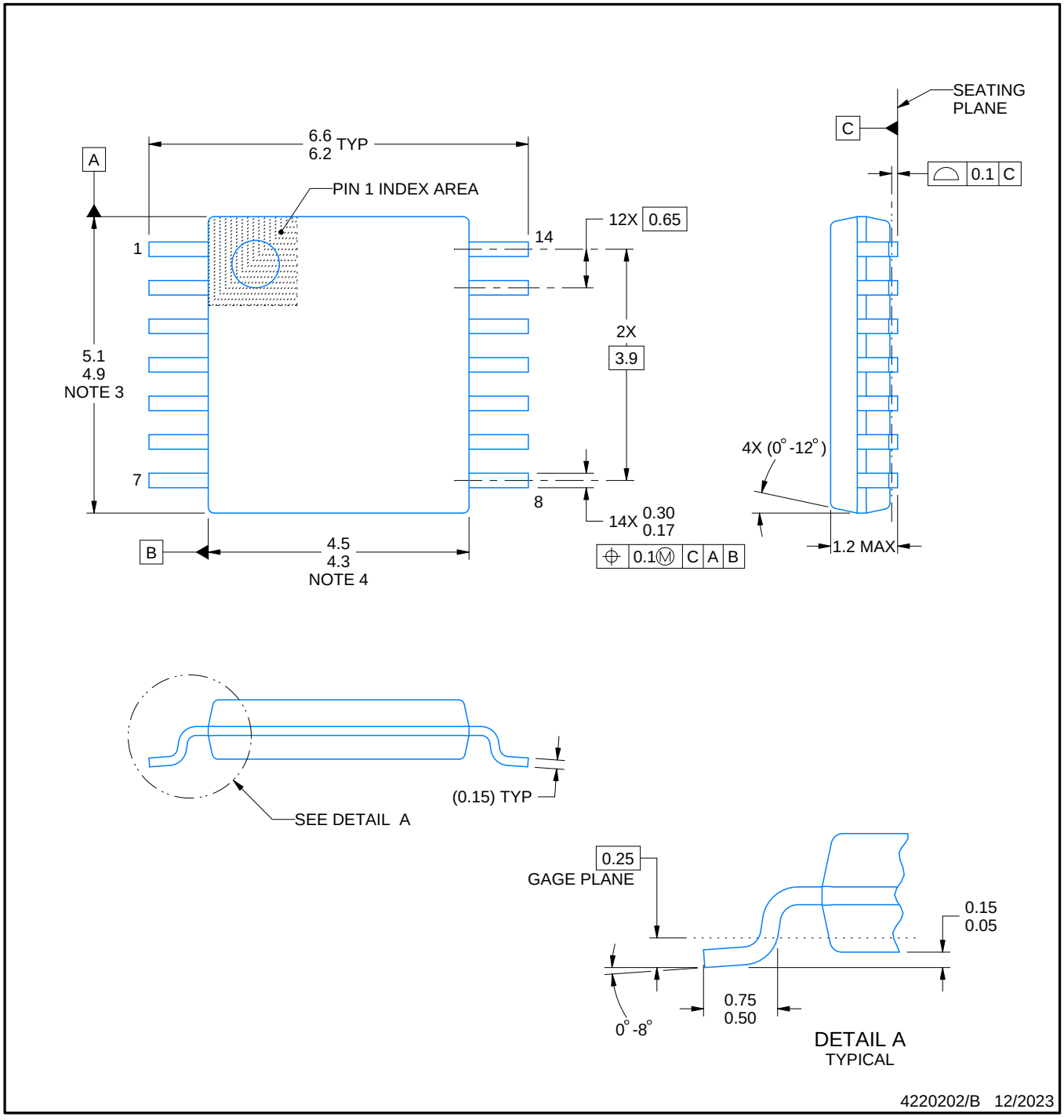
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV1704AMPWPSEP	PW	TSSOP	14	90	530	10.2	3600	3.5
V62/18613-01XE-T	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

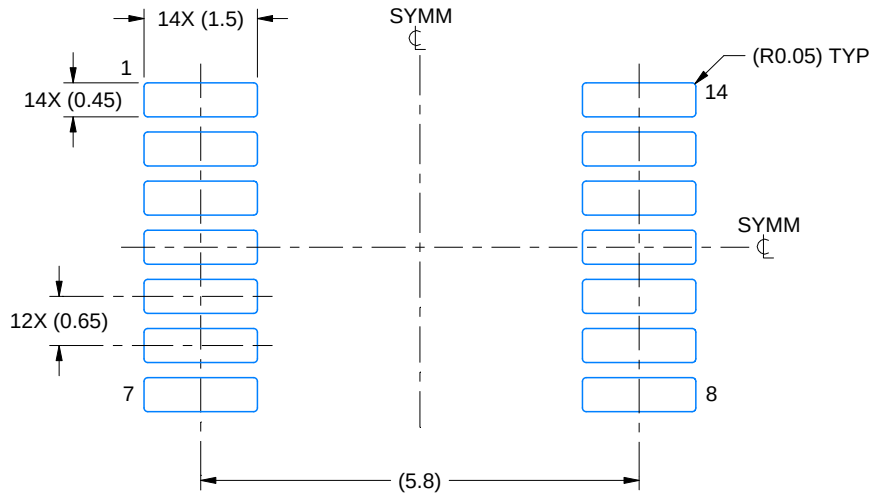
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

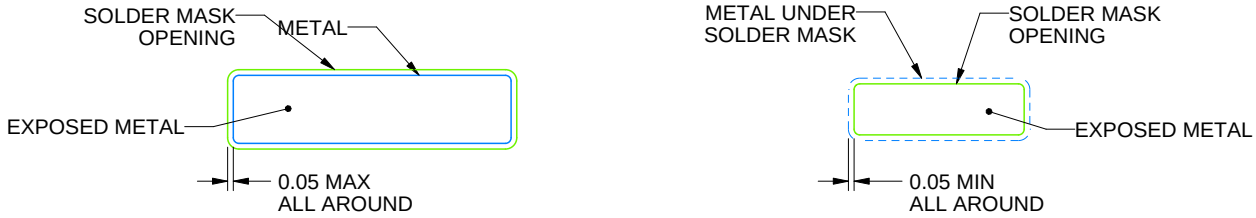


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

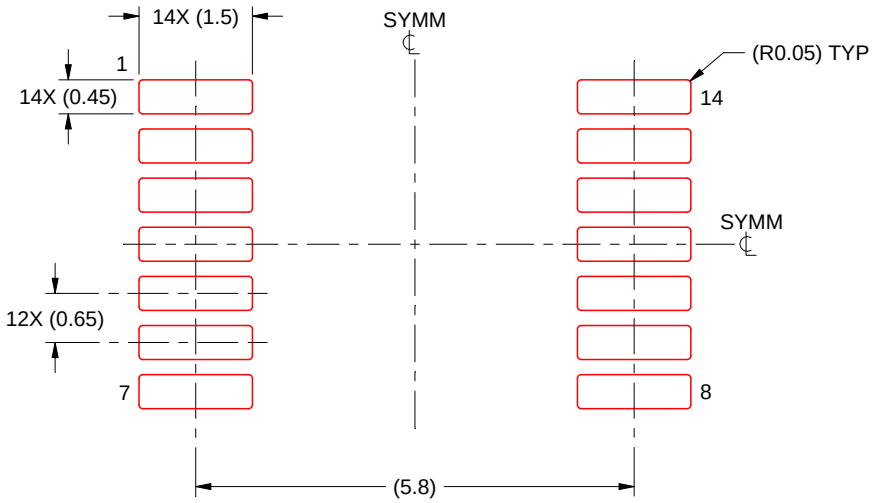


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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