SBVS152C - DECEMBER 2010 - REVISED OCTOBER 2011

16-Channel, Constant-Current LED Driver with 4-Channel Grouped Delay

Check for Samples: TLC59282

FEATURES

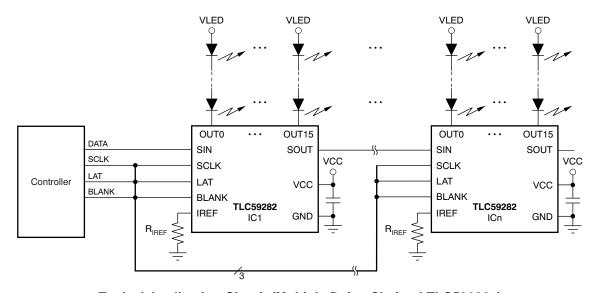
- 16 Channels, Constant-Current Sink Output with On/Off Control
- Capability (Constant-Current Sink): 35 mA (V_{CC} ≤ 3.6 V), 45 mA (V_{CC} > 3.6 V)
- LED Power-Supply Voltage up to 17 V
- V_{CC} = 3 V to 5.5 V
- Constant-Current Accuracy:
 - Channel-to-Channel = ±0.6% (typ),±2% (max)
 - Device-to-Device = $\pm 1\%$ (typ), $\pm 3\%$ (max)
- Low Saturation Voltage: 0.31 V at 20 mA (typ)
 - $T_A = +25$ °C, One Channel On
- · CMOS Logic Level I/O
- Data Transfer Rate: 35 MHz
- BLANK Pulse Width: 30 ns
- Four-Channel Grouped Delay for
 - Noise Reduction
- Operating Temperature: –40°C to +85°C

APPLICATIONS

- Video Displays
- Message Boards
- Illumination

DESCRIPTION

The TLC59282 is a 16-channel, constant-current sink driver. Each channel can be individually controlled via a simple serial communications protocol that is compatible with 3.3 V or 5 V CMOS logic levels, depending on the operating VCC. Once the serial data buffer is loaded, a rising edge on LATCH transfers the data to the LEDx outputs. The BLANK pin can be used to turn off all OUTn outputs during power-on and output data latching to prevent unwanted image displays during these times. The constant-current value of all 16 channels is set by a single external resistor. Multiple TLC59282s can be cascaded together to control additional LEDs from the same processor.



Typical Application Circuit (Multiple Daisy-Chained TLC59282s)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC59282	SSOP-24/QSOP-24	TLC59282DBQR	Tape and Reel, 2500
1LC59282	330P-24/Q30P-24	TLC59282DBQ	Tube, 50
TI 050202	OEN 24	TLC59282RGER	Tape and Reel, 3000
TLC59282	QFN-24	TLC59282RGE	Tape and Reel, 250

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

	PAR	AMETER	TLC59282	UNIT
V_{CC}	Supply voltage		-0.3 to +6	V
l _{OUT}	Output current (dc)	OUT0 to OUT15	50	mA
V_{IN}	Input voltage range	SIN, SCLK, LAT, BLANK, IREF	-0.3 to V _{CC} + 0.3	V
V	Output voltage renge	SOUT	-0.3 to V _{CC} + 0.3	V
V _{OUT}	Output voltage range	OUT0 to OUT15	-0.3 to +18	V
$T_{J(MAX)}$	Operating junction temperature	re	+150	°C
T _{STG}	Storage temperature range		–55 to +150	°C
	ECD roting	Human body model (HBM)	4000	V
	ESD rating	Charged device model (CDM)	1000	V

⁽¹⁾ Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

THERMAL INFORMATION

		TLC		
	THERMAL METRIC ⁽¹⁾	DBQ	RGE	UNITS
		24 PINS	24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	73.2	46.8	
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.6	48.6	
θ_{JB}	Junction-to-board thermal resistance	38.9	23.0	°C // //
ΨЈТ	Junction-to-top characterization parameter	12.3	1.2	°C/W
ΨЈВ	Junction-to-board characterization parameter	39.7	22.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	6.3	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

⁽²⁾ All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

At $T_A = -40$ °C to +85°C, unless otherwise noted.

			Т	LC59282		
	PARAMETER	TEST CONDITIONS	MIN	NOM	NOM MAX	
DC Characte	eristics: V _{CC} = 3 V to 5.5 V					
V _{CC}	Supply voltage		3		5.5	V
Vo	Voltage applied to output	OUT0 to OUT15			17	V
V _{IH}	High-level input voltage		0.7 × V _{CC}		V _{CC}	V
V _{IL}	Low-level input voltage		GND		0.3 × V _{CC}	V
ОН	High-level output current	SOUT			-1	mA
OL	Low-level output current	SOUT			1	mA
		OUT0 to OUT15, 3 V ≤ V _{CC} < 3.6 V	2		35	mA
I _{OLC}	Constant output sink current	OUT0 to OUT15, 3.6 V ≤ V _{CC} < 5.5 V	2		45	mA
ГА	Operating free-air temperature range		-40		+85	°C
ГЈ	Operating junction temperature range		-40		+125	°C
AC Charact	eristics: V _{CC} = 3 V to 5.5 V		·			
: CLK (SCLK)	Data shift clock frequency	SCLK			35	MHz
T _{WH0}		SCLK	10			ns
Γ _{WL0}		SCLK	10			ns
Γ _{WH1}	Pulse duration	LAT	20			ns
Γ _{WH2}		BLANK	60			ns
Γ _{WL2}		BLANK	30			ns
r _{suo}	Contract time of	SIN-SCLK↑	4			ns
Γ _{SU1}	Setup time	LAT↓-SCLK↑	10			ns
Γ _{H0}	Hald Care	SIN-SCLK↑	4			ns
T _{H1}	Hold time	LAT↓-SCLK↑	10			ns



ELECTRICAL CHARACTERISTICS

At $V_{CC} = 3$ V to 5.5 V and $T_A = -40$ °C to +85°C. Typical values at $V_{CC} = 3.3$ V and $T_A = +25$ °C, unless otherwise noted.

			1	LC59282		
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA at SOUT	V _{CC} - 0.4		V _{CC}	V
V _{OL}	Low-level output voltage	I _{OL} = 1 mA at SOUT			0.4	V
I _{IN}	Input current	V _{IN} = V _{CC} or GND at SIN and SCLK	-1		1	μΑ
I _{CC0}		SIN/SCLK/LAT = low, BLANK = high, $V_{OUTn} = 1 \text{ V}$, $R_{IREF} = \text{open}$		0.1	1	mA
I _{CC1}	County compact (A/)	SIN/SCLK/LAT = low, BLANK = high, $V_{OUTn} = 1 \text{ V}$, $R_{IREF} = 3 \text{ k}\Omega \text{ (}I_{OUT} = 16.8 \text{ mA target)}$		4.5	6	mA
I _{CC2}	Supply current (V _{CC})	All OUTn = ON, SIN/SCLK/LAT/BLANK = low, V_{OUTn} = 1 V, R_{IREF} = 3 k Ω		7	15	mA
ссз		All OUTn = ON, SIN/SCLK/LAT/BLANK = low, V_{OUTn} = 1 V, R_{IREF} = 1.5 k Ω (I_{OUT} = 33.6mA target)		16	34	mA
locc	Constant output current	All OUTn = ON, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 k Ω at OUT0 to OUT15 (see Figure 6), T_A = +25°C	32.1	33.7	35.3	mA
l _{oLKG}	Output leakage current	OUTn = OFF, $V_{OUTn} = V_{OUTfix} = 17 \text{ V}$, BLANK = high, $R_{IREF} = 1.5 \text{ k}\Omega$ at OUT0 to OUT15 (see Figure 6)			0.1	μA
ΔI _{OLC0}	Constant-current error (channel-to-channel) (1)	All OUTn = ON, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 $k\Omega$ at OUT0 to OUT15		±0.6	±2	%
∆I _{OLC1}	Constant-current error (device-to-device) ⁽²⁾	All OUTn = ON, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 k Ω at OUT0 to OUT15, T_A = +25°C		±1	±3	%
∆I _{OLC2}	Line regulation (3)	All OUTn = ON, V _{OUTn} = V _{OUTfix} = 1 V, R _{IREF} = 1.5 k Ω at OUT0 to OUT15, V _{CC} = 3 V to 5.5 V		±0.5	±1	%/V
∆I _{OLC3}	Load regulation ⁽⁴⁾	All OUTn = ON, V_{OUTn} = 1 V to 3V, V_{OUTfix} = 1 V, R_{IREF} = 1.5 k Ω		±1	±3	%/V
V _{IREF}	Reference voltage output	$R_{IREF} = 1.5 \text{ k}\Omega, T_A = +25^{\circ}\text{C}$	1.18	1.205	1.23	V
R _{PUP}	Pull-up resistor	BLANK	250	500	750	kΩ
R _{PDWN}	Pull-down resistor	LAT	250	500	750	kΩ

(1) The deviation of each output from the average of OUT0-OUT15 constant-current. Deviation is calculated by the formula:

$$\Delta \text{ (\%)} = \left[\frac{I_{\text{OUTn}}}{\frac{(I_{\text{OUT0}} + I_{\text{OUT1}} + \dots + I_{\text{OUT14}} + I_{\text{OUT15}})}{16}} - 1 \right] \times 100$$

The deviation of the OUT0-OUT15 constant-current average from the ideal constant-current value. Deviation is calculated by the following formula:

$$\Delta \text{ (\%) = } \left[\begin{array}{c} \frac{(I_{\text{OUT0}} + I_{\text{OUT1}} + \dots I_{\text{OUT15}})}{16} - \text{(Ideal Output Current)} \\ \hline & \text{Ideal Output Current} \end{array} \right] \times 100$$

Ideal current is calculated by the formula:
$$I_{OUT(IDEAL)} = 41.9 \times \left[\frac{1.205}{R_{IREF}} \right]$$

(3) Line regulation is calculated by this equation:
$$\Delta \ (\%/V) = \left\{ \frac{(I_{OUTn} \ at \ V_{CC} = 5.5 \ V) - (I_{OUTn} \ at \ V_{CC} = 3 \ V)}{(I_{OUTn} \ at \ V_{CC} = 3 \ V)} \right\} \times \frac{100}{5.5 \ V - 3 \ V}$$

(4) Load regulation is calculated by the equation:

$$\Delta \ (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3 \text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1 \text{ V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1 \text{ V})} \right) \times \frac{100}{3 \text{ V} - 1 \text{ V}}$$

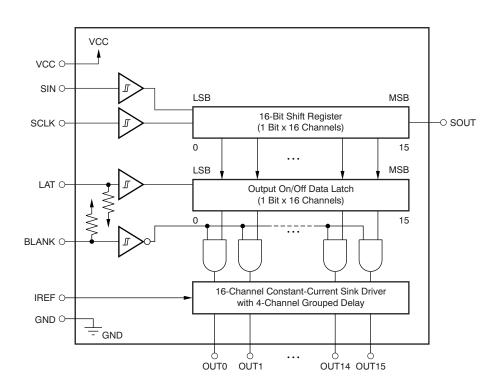
SWITCHING CHARACTERISTICS

At V_{CC} = 3 V to 5.5 V, T_A = -40°C to +85°C, C_L = 15 pF, R_L = 130 Ω , R_{IREF} = 1.5 k Ω , and V_{LED} = 5.5 V. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

			TL	C59282		
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{R0}	Dies time	SOUT (see Figure 5)		5	12	ns
t _{R1}	Rise time	OUTn (see Figure 4)		10	30	ns
t _{F0}	Fall times	SOUT (see Figure 5)		5	12	ns
t _{F1}	Fall time	OUTn (see Figure 4)		10	30	ns
t _{D0}		SCLK↑ to SOUT↑↓		8	20	ns
t _{D1}		LAT↑ or BLANK↑↓ to OUT0/OUT7/OUT8/OUT15 on/off		18	36	ns
t _{D2}		LAT↑ or BLANK↑↓ to OUT1/OUT6/OUT9/OUT14 on/off		38	69	ns
t _{D3}	Propagation delay time	LAT↑ or BLANK↑↓ to OUT2/OUT5/OUT10/OUT13 on/off		58	102	ns
t _{D4}		LAT↑ or BLANK↑↓ to OUT3/OUT4/OUT11/OUT12 on/off		78	135	ns
t _{ON_ERR}	Output on-time error ⁽¹⁾	On/off latch data = all '1', 30 ns BLANK low level one-shot pulse input	-15		15	ns

⁽¹⁾ Output on-time error (t_{ON_ERR}) is calculated by the formula: t_{ON_ERR} (ns) = t_{OUT_ON} – BLANK low level one-shot pulse width (T_{WL2}) . t_{OUT_ON} indicates the actual on-time of the constant-current output.

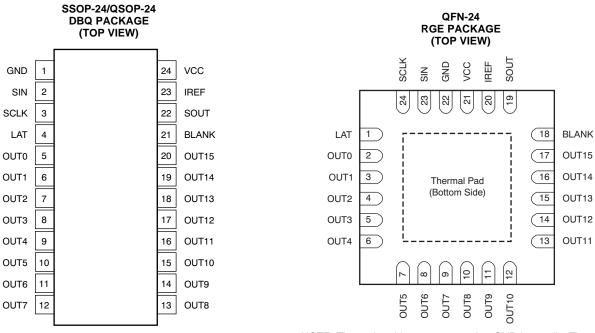
FUNCTIONAL BLOCK DIAGRAM



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DEVICE INFORMATION



NOTE: Thermal pad is not connected to GND internally. The thermal pad must be connected to GND via the PCB pattern.

TERMINAL FUNCTIONS

	TERMINAL	_		
NAME	DBQ	RGE	I/O	DESCRIPTION
SIN	2	23	ı	Serial data input for driver on/off control; Schmitt buffer input. When SIN is high, data '1' are written into the LSB of the 16-bit shift register at the SCLK rising edge.
SCLK	3	24	I	Serial data shift clock; Schmitt buffer input. All data in the 16-bit shift register are shifted toward the MSB by 1-bit synchronization of SCLK.
LAT	4	1	1	Level triggered latch; Schmitt buffer input. The data in the 16-bit shift register continue to transfer to the output on/off data latch while LAT is high. Therefore, if the data in the 16-bit shift register are changed when LAT is high, the data in the data latch are also changed. The data in the data latch are held when LAT is low. This pin is internally pulled down to GND with a 500 k Ω (typ) resistor.
BLANK	21	18	I	Blank, all outputs; Schmitt buffer input. When BLANK is high, all constant-current outputs (OUT0–OUT15) are forced off. When BLANK is low, all constant-current outputs are controlled by the data in the output on/off data latch. This pin is internally pulled up to V_{CC} with a 500 k Ω (typ) resistor.
IREF	23	20	I/O	Constant-current value setting, OUT0–OUT15 sink constant-current is set to desired value by connection to an external resistor between IREF and GND.
SOUT	22	19	0	Serial data output. This output is connected to the MSB of the 16-bit shift register. SOUT data changes at the rising edge of SCLK.
OUT0	5	2	0	Constant-current output. Each output can be tied together with others to increase the constant-current. Different voltages can be applied to each output.
OUT1	6	3	0	Constant-current output
OUT2	7	4	0	Constant-current output
OUT3	8	5	0	Constant-current output
OUT4	9	6	0	Constant-current output
OUT5	10	7	0	Constant-current output
OUT6	11	8	0	Constant-current output
OUT7	12	9	0	Constant-current output
OUT8	13	10	0	Constant-current output
OUT9	14	11	0	Constant-current output
OUT10	15	12	0	Constant-current output
OUT11	16	13	0	Constant-current output
OUT12	17	14	0	Constant-current output
OUT13	18	15	0	Constant-current output
OUT14	19	16	0	Constant-current output
OUT15	20	17	0	Constant-current output
VCC	24	21	_	Power-supply voltage
GND	1	22	_	Power ground



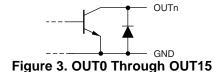
PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

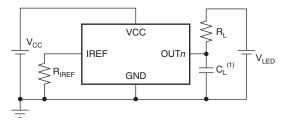


Figure 1. SIN, SCLK, LAT, BLANK

Figure 2. SOUT

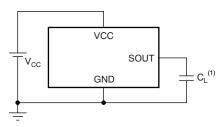


TEST CIRCUITS



(1) C₁ includes measurement probe and jig capacitance.

Figure 4. Rise Time and Fall Time Test Circuit for OUTn



(1) C_L includes measurement probe and jig capacitance.

Figure 5. Rise Time and Fall Time Test Circuit for SOUT

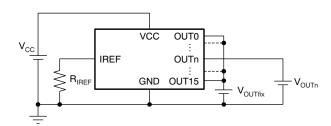
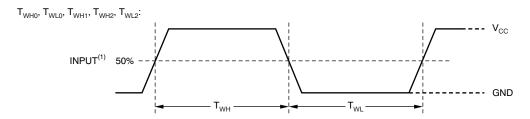
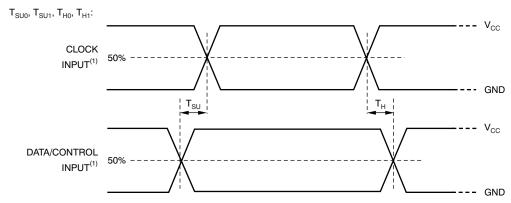


Figure 6. Constant-Current Test Circuit for OUTn



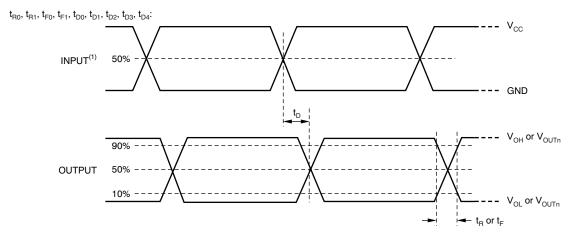
TIMING DIAGRAMS





(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 7. Input Timing

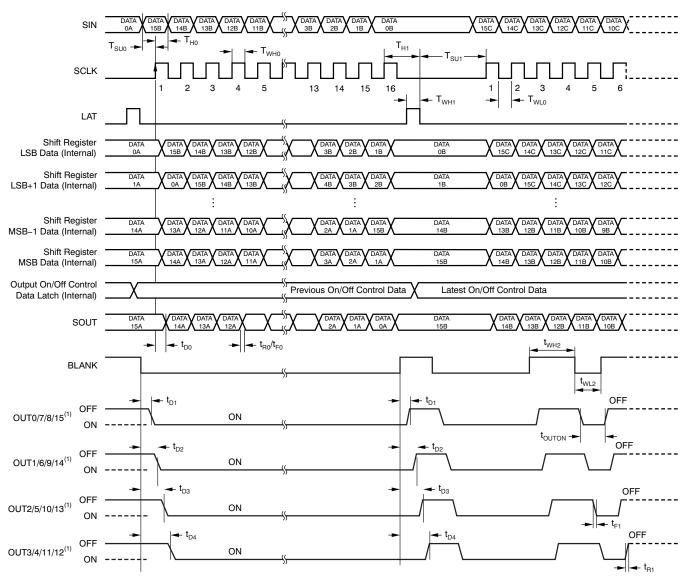


(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 8. Output Timing

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- (1) Output on/off data = FFFFh.
- (2) $t_{ON_ERR} = t_{OUTON} T_{WL2}$.

Figure 9. Timing Diagram



TYPICAL CHARACTERISTICS

At $V_{CC} = 3.3 \text{ V}$ and $T_A = +25^{\circ}\text{C}$, unless otherwise noted.

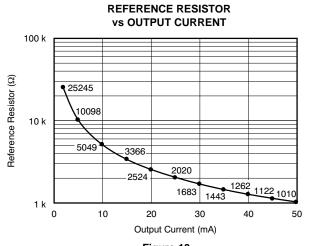


Figure 10.

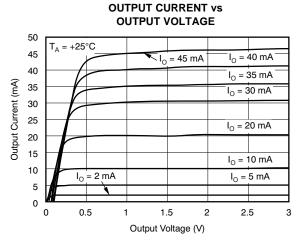


Figure 11.

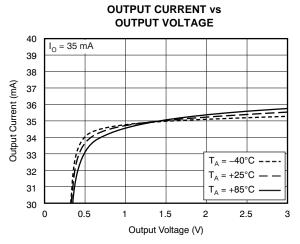


Figure 12.

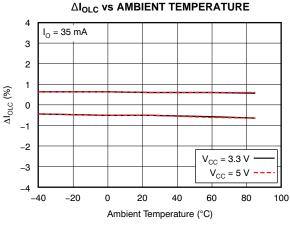


Figure 13.

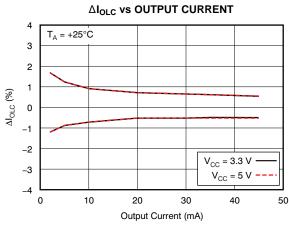


Figure 14.

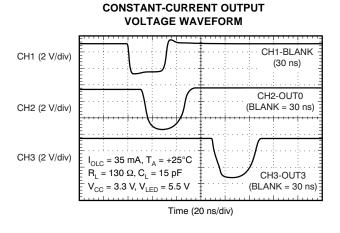


Figure 15.



DETAILED DESCRIPTION

SETTING FOR THE CONSTANT SINK CURRENT VALUE

The constant-current values are determined by an external resistor (R_{IREF}) placed between IREF and GND. The resistor (R_{IREF}) value is calculated by Equation 1.

$$R_{IREF} (k\Omega) = \frac{V_{IREF} (V)}{I_{OLC} (mA)} \times 41.9$$

Where:

$$V_{IREF}$$
 = the internal reference voltage on the IREF pin (typically 1.205 V) (1)

 I_{OLC} must be set in the range of 2 mA to 35 mA when V_{CC} is less than 3.6 V. Also, when V_{CC} is equal to 3.6 V or greater, I_{OLC} must be set in the range of 2 mA to 45 mA. The constant sink current characteristic for the external resistor value is shown in Figure 10. Table 1 describes the constant-current output versus external resistor value.

Table 1. Constant-Current Output versus External Resistor Value

I _{OLC} (mA, Typical)	R_{IREF} (k Ω)
45 (V _{CC} > 3.6 V only)	1.12
40 (V _{CC} > 3.6 V only)	1.26
35	1.44
30	1.68
25	2.02
20	2.52
15	3.37
10	5.05
5	10.1
2	25.2

CONSTANT-CURRENT DRIVER ON/OFF CONTROL

When BLANK is low, the corresponding output is turned on if the data in the on/off control data latch are '1' and remains off if the data are '0'. When BLANK is high, all outputs are forced off. This control is shown in Table 2.

Table 2. On/Off Control Data Truth Table

OUTPUT ON/OFF DATA	CONSTANT-CURRENT OUTPUT STATUS
0	Off
1	On

When the IC is initially powered on, the data in the 16-bit shift register and output on/off data latch are not set to the respective default value. Therefore, the output on/off data must be written to the data latch before turning the constant-current output on. BLANK should be at a high level when powered on because the constant-current may be turned on as a result of random data in the output on/off data latch.

The output on/off data corresponding to any unconnected OUTn outputs should be set to '0' before turning on the remaining outputs. Otherwise, the supply current (I_{CC}) increases while the LEDs are on.

REGISTER CONFIGURATION

The TLC59282 has a 16-bit shift register and an output on/off data latch. Both the shift register and data latch are 16 bits long and are used to turn the constant-current outputs on and off. Figure 16 shows the shift register and data latch configuration. The data at the SIN pin are shifted in to the LSB of the 16-bit shift register at the rising edge of the SCLK pin; SOUT data change at the rising edge of SCLK.

The output on/off data in the 16-bit shift register continue to transfer to the output on/off data latch while LAT is high. Therefore, if the data in the 16-bit shift register are changed when LAT is high, the data in the data latch are also changed. The data in the data latch are held when LAT is low. When the IC initially powers on, the data in the output on/off shift register and latch are not set to the default values; on/off control data must be written to the on/off control data latch before turning the constant-current output on. BLANK should be high when the IC is powered on because the constant-current may be turned on at that time as a result of random values in the on/off data latch. All constant-current outputs are forced off when BLANK is high. The OUTn on/off are controlled by the data in the output on/off data latch. The timing diagram and truth table for writing data are shown in Figure 17 and Table 3.

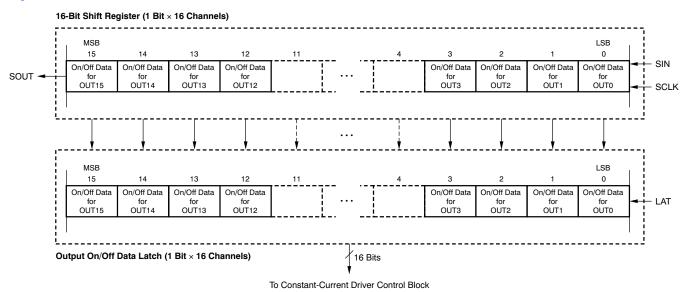


Figure 16. 16-Bit Shift Register and Output On/Off Data Latch Configuration



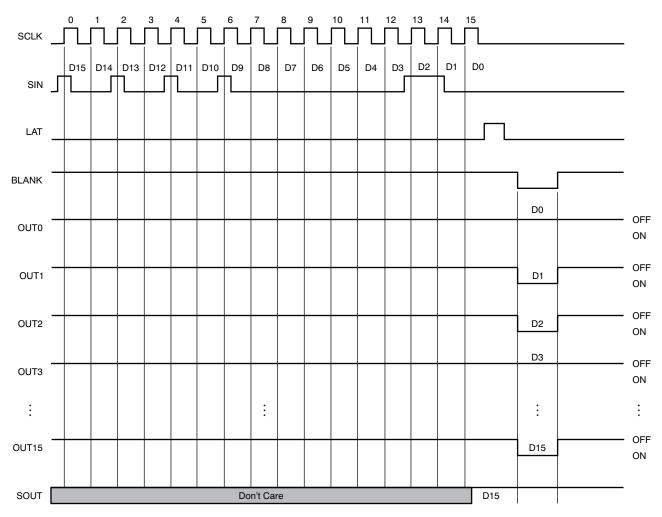


Figure 17. Operation Timing Diagram

SCLK LAT **BLANK** SIN OUT0...OUT7...OUT15 SOUT High Dn Dn...Dn - 7...Dn - 15 Dn - 15 Low 1 Low Low Dn + 1 No change Dn - 14 1 Dn + 2 Dn + 2...Dn - 5...Dn - 13 Dn - 13 High Low 1 Dn + 3 Dn + 2...Dn - 5...Dn - 13 Dn - 13 Low Dn + 3Dn - 13 High Off

Table 3. Truth Table in Operation

NOISE REDUCTION

Large surge currents may flow through the IC and the board if all 16 outputs turn on or off simultaneously. These large current surges could induce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC59282 independently turns on or off the outputs for each color group with a 20 ns (typ) delay time; see Figure 9. The output current sinks are grouped into four groups. The first group that is turned on/off are OUT0/7/8/15; the second group that is turned on/off are OUT1/6/9/14; the third group that is turned on/off are OUT2/5/10/13; and the fourth group is OUT3/4/11/12. Both turn-on and turn-off are delayed. However, the state of each output is controlled by the data in the output on-off data latch and BLANK level.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	hanges from Revision B (July 2011) to Revision C	Page
•	Added Low Saturation Voltage Features bullet	1
CI	hanges from Revision A (December 2010) to Revision B	Page
•	Changed Constant-Current Accuracy Features bullet	1
•	Added RGE package information to Package/Ordering Information table	2
•	Added RGE package to Thermal Information table	2
•	Changed Input current parameter test conditions in Electrical Characteristics table	4
•	Added RGE pin out and footnote to Device Information section	6
•	Added RGE information to Terminal Functions table	7
•	Deleted Figure 11, POWER DISSIPATION RATE vs FREE-AIR TEMPERATURE	11

11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)				(6)
						(4)	(5)		
TLC59282DBQ	Active	Production	SSOP (DBQ) 24	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59282
TLC59282DBQ.B	Active	Production	SSOP (DBQ) 24	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59282
TLC59282DBQR	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59282
TLC59282DBQR.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59282
TLC59282DBQRG4	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59282
TLC59282DBQRG4.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59282
TLC59282RGER	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC
									59282
TLC59282RGER.B	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC
			, , ,	·					59282
TLC59282RGET	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC
									59282
TLC59282RGET.B	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC
									59282

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59282DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC59282DBQRG4	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC59282RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC59282RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59282DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
TLC59282DBQRG4	SSOP	DBQ	24	2500	353.0	353.0	32.0
TLC59282RGER	VQFN	RGE	24	3000	353.0	353.0	32.0
TLC59282RGET	VQFN	RGE	24	250	213.0	191.0	35.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

	Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ĺ	TLC59282DBQ	DBQ	SSOP	24	50	506.6	8	3940	4.32
ĺ	TLC59282DBQ.B	DBQ	SSOP	24	50	506.6	8	3940	4.32

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AE.



PLASTIC QUAD FLATPACK - NO LEAD

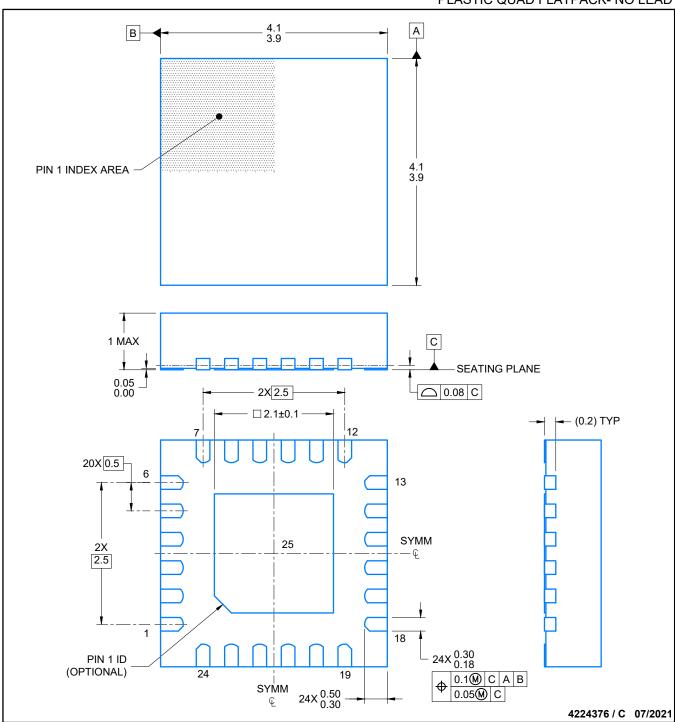


Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4204104/H



PLASTIC QUAD FLATPACK- NO LEAD

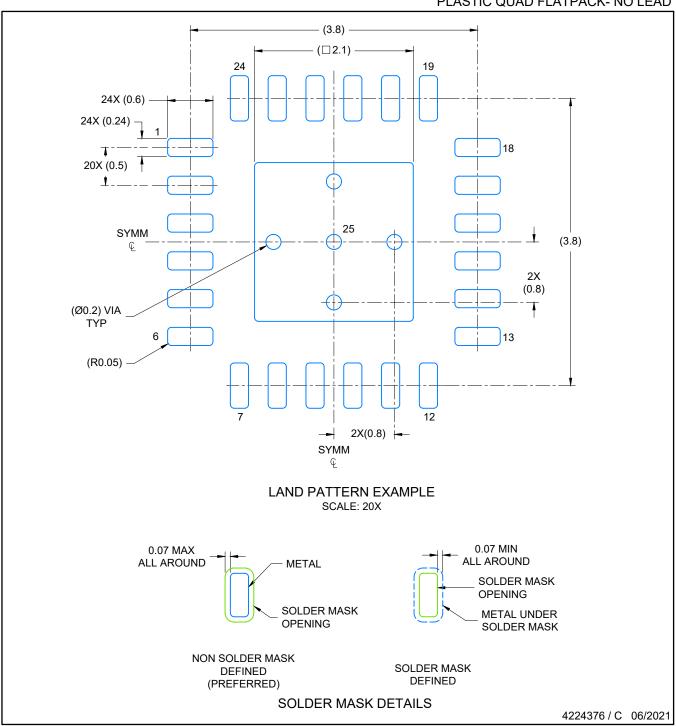


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK- NO LEAD

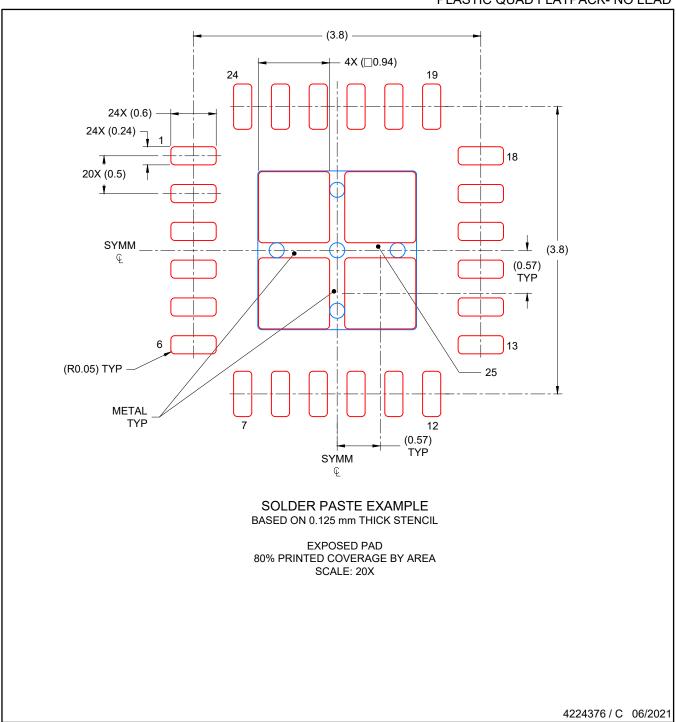


NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..



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