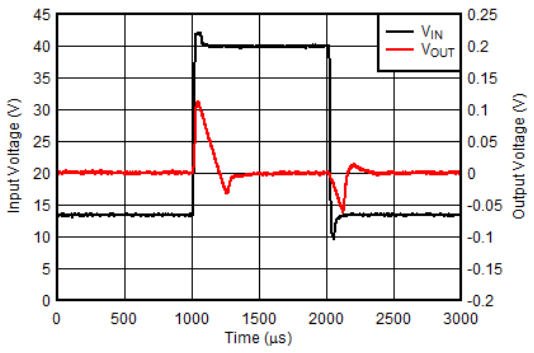
TL720M05-Q1 Automotive, 500mA, 40V, Low-Dropout Voltage Regulator

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Junction temperature: –40°C to +150°C, T_J
- Input voltage range:
  - Legacy chip: 5.5V to 42V (45V absolute maximum)
  - New chip: 3.0V to 40V (42V absolute maximum)
- Maximum output current: 500mA (new chip)
- Output voltage accuracy: ±2.0% (across line, load, and temperature)
- Low dropout voltage: 500mV (maximum) at 300mA
- Low quiescent current:
  - Legacy chip: 100µA (typical) at I_{OUT} = 1mA
  - New chip: 17µA (typical) at light loads
- Excellent line transient response (new chip):
  - ±2% V_{OUT} deviation during cold-crank
  - ±2% V_{OUT} deviation (1V/µs V_{IN} slew rate)
- Stable with a 2.2µF or larger capacitor (new chip)
- Reverse-polarity protection (legacy chip)
- Packages:
  - 3-pin TO-252 (KVU)
  - 3-pin DDPAK/TO-263 (KTT)
  - 20-pin HTSSOP (PWP) (legacy chip)

2 Applications

- Reconfigurable instrument clusters
- Body control modules (BCM)
- Always-on battery-connected applications:
  - Automotive gateways
  - Remote keyless entries (RKE)



Line Transient Response (3V/µs V_{IN} Slew Rate) (New Chip)

3 Description

The TL720M05-Q1 is a low-dropout linear regulator, designed to connect to the battery in automotive applications. The device has an input voltage range extending to 40V (new chip). This range allows the device to withstand transients (such as load dumps) that are anticipated in automotive systems. With low quiescent current consumption at light loads, the device is designed for powering always-on components. Examples of always-on components are microcontrollers (MCUs) and controller area network (CAN) transceivers in standby systems.

The device (new chip) has a state-of-the-art transient response that allows the output to quickly react to changes in load or line. For example, during cold-crank conditions. Additionally, the device has a novel architecture that minimizes output overshoot when recovering from dropout. During normal operation, the device has a tight DC accuracy of ±2% over line, load, and temperature.

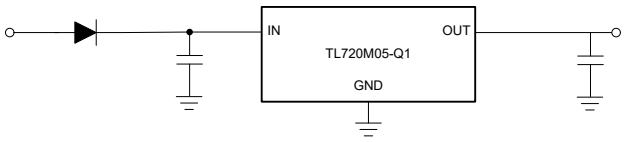
The device also incorporates a number of internal circuits for protection against overload and overtemperature. The legacy chip also provides protection against reverse polarity.

The TL720M05-Q1 is available in thermally conductive packaging to allow the device to efficiently transfer heat to the circuit board.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TL720M05-Q1	KTT (TO-263, 3)	10.16mm × 15.24mm
	KVU (TO-252, 3)	6.6mm × 10.11mm
	PWP (HTSSOP, 20) (legacy chip)	6.5mm × 6.4mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic (New Chip)

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4 Pin Configuration and Functions

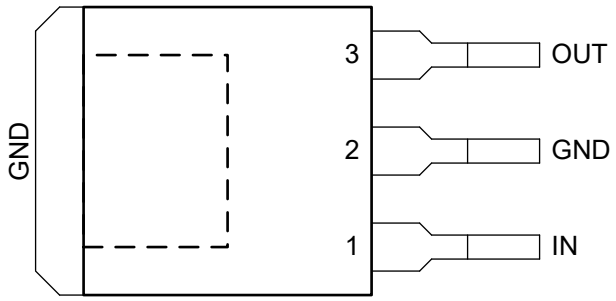


Figure 4-1. KTT Package, 3-Pin TO-263 (Top View)

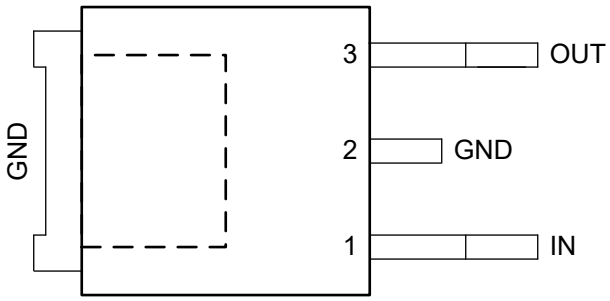


Figure 4-2. KVU Package, 3-Pin TO-252 (Top View)

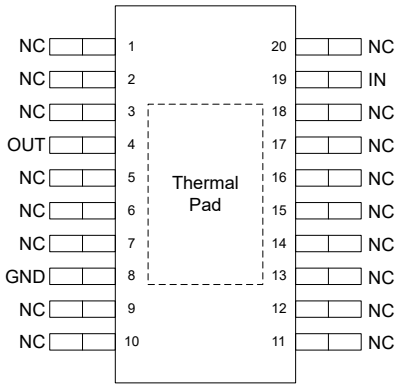


Figure 4-3. PWP Package(1), 20-Pin HTSSOP With PowerPAD (Top View)

Table 4-1. Pin Functions

PIN				TYPE(2)	DESCRIPTION
NAME	TO-263	TO-252	HTSSOP (Legacy Chip)		
GND	2	2	8	O	Ground. Internally connected to heat sink.
IN	1	1	19	I	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the input capacitor as close to the input of the device as possible
NC	—	—	1-3, 5-7, 9-18, 20	—	Not connected.
OUT	3	3	4	O	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the output capacitor as close to output of the device as possible.

(1) NC = No internal connection.
(2) I = input, O = output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Supply input voltage (for legacy chip)	–42	45	V
	Supply input voltage (for new chip)	–0.3	42	
V_{OUT}	Regulated output voltage (for legacy chip)	–1.0	40	
	Regulated output voltage (for new chip)	–0.3	V_{IN} + 0.3V(2)	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum rating is VIN + 0.3V or 20V, whichever is smaller

5.2 ESD Ratings

				VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)			±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	N/A	±500	
			Corner pins	N/A	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Supply input voltage (for legacy chip)	5.5		42	V
	Supply input voltage (for new chip)	3		40	
V_{OUT}	Output voltage		5.0		
I_{OUT}	Output current (for legacy chip)	0		400	mA
	Output current (for new chip)	0		500	
C_{OUT}	Output capacitor (for legacy chip)(1)	22			µF
	Output capacitor (for new chip)(1)	2.2		220	
C_{IN}	Input capacitor(2)		1		
ESR	Output capacitor ESR requirements (for legacy chip)	0.001		5	Ω
	Output capacitor ESR requirements (for new chip)	0.001		2	
T_J	Operating junction temperature	–40		150	°C

(1) Effective output capacitance of 1µF minimum required for stability.
(2) For robust EMI performance the minimum input capacitance is 500nF.

5.4 Thermal Information

THERMAL METRIC[1] [2]		TL720M05-Q1					UNIT
		KVU (TO-252-3)		KTT (TO-263-3)		PWP (HTSSOP-20)	
		Legacy Chip	New Chip	Legacy Chip	New Chip	Legacy Chip	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.3	30	34.2	22.6	39.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	39.5	38.2	6.0	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.8	8.6	44.9	30.9	19.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.8	2.6	6	2.0	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.2	8.6	44.5	3.4	18.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	1.3	0.8	5.8	1.5	°C/W

(1) The thermal data is based on the JEDEC standard high K profile, JESD 51-7. Two-signal, two-plane, four-layer board with 2oz copper. The copper pad is soldered to the thermal land pattern. Also, verify that correct attachment procedure is incorporated.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics (for KVU Package Only)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 0mA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted); typical values are at T_J = 25°C.

PARAMETER		Test Conditions		MIN	TYP	MAX	UNIT
V_{OUT}	Regulated output (for legacy chip)	V_{IN} = 6V to 28V, I_{OUT} = 5mA to 400mA		4.9	5.0	5.1	V
		V_{IN} = 6V to 40V, I_{OUT} = 5mA to 400mA		4.9	5.0	5.1	
	Regulated output (for new chip)	V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 100µA to 450mA, T_J = 25ºC[1]		–0.85		0.85	%
		V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 100µA to 500mA, T_J = 25ºC[1]		–0.85		0.85	
		V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 100µA to 450mA[1]		–1.15		1.15	
		V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 100µA to 500mA[1]		–1.15		1.15	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation (for legacy chip)	I_{OUT} = 5mA to 400mA			15	30	mV
	Load regulation (for new chip)	V_{IN} = V_{OUT} + 1V, I_{OUT} = 100µA to 450mA				0.425	%
$\Delta V_{OUT(\Delta VIN)}$	Line regulation (for legacy chip)	V_{IN} = 8V to 32V, I_{OUT} = 5mA		–15	5	15	mV
	Line regulation (for new chip)	V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 100µA				0.2	%
ΔV_{OUT}	Load transient response settling time (for new chip)[2]	t_R = t_F = 1µs; C_{OUT} = 10µF				100	µs
ΔV_{OUT}	Load transient response overshoot, undershoot (for new chip)[2]	t_R = t_F = 1µs; C_{OUT} = 10µF	I_{OUT} = 150mA to 350mA	–2%			%V_{OUT}
			I_{OUT} = 350mA to 150mA			10%	
			I_{OUT} = 0mA to 500mA	–10%			
I_Q	Quiescent current (for legacy chip) I_Q = I_{IN} – I_{OUT}	I_{OUT} = 1mA	T_J = 25ºC		100	220	µA
			T_J ≤ 85ºC		100	220	
		I_{OUT} = 250mA			5	10	mA
		I_{OUT} = 400mA			12	22	
	Quiescent current (for new chip)	V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 0mA, T_J = 25ºC[3]			17	21	µA
		V_{IN} = V_{OUT} + 1V to 40V, I_{OUT} = 0mA[3]				26	
		I_{OUT} = 500µA				35	
V_{DO}	Dropout voltage (for legacy chip)	I_{OUT} = 300mA			250	500	mV
	Dropout voltage (for new chip)	I_{OUT} ≤ 1mA, V_{IN} = $V_{OUT(NOM)}$ × 0.95				46	
		I_{OUT} = 315mA, V_{IN} = $V_{OUT(NOM)}$			275	400	
		I_{OUT} = 450mA, V_{IN} = $V_{OUT(NOM)}$			360	525	
		I_{OUT} = 500mA, V_{IN} = $V_{OUT(NOM)}$			390	575	
$V_{UVLO(RISING)}$	Rising input supply UVLO (for new chip)	V_{IN} rising		2.6	2.7	2.82	V
$V_{UVLO(FALLING)}$	Falling input supply UVLO (for new chip)	V_{IN} falling		2.38	2.5	2.6	V

5.5 Electrical Characteristics (for KVU Package Only) (continued)

specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 0mA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT} ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted); typical values are at T_J = 25°C.

PARAMETER		Test Conditions	MIN	TYP	MAX	UNIT
$V_{UVLO(HYST)}$	$V_{UVLO(IN)}$ hysteresis (for new chip)			230		mV
I_{CL}	Output current limit (for legacy chip)	V_{IN} = V_{OUT} + 1V, V_{OUT} short to 90% × $V_{OUT(NOM)}$	450	700	950	mA
	Output current limit (for new chip)	V_{IN} = V_{OUT} + 1V, V_{OUT} short to 90% × $V_{OUT(NOM)}$	540		780	
PSRR	Power-supply rejection ratio (for legacy chip)	V_{IN} - V_{OUT} = 1V, frequency = 100Hz, Vr = 0.5V_{pp}, I_{OUT} = 450mA		60		dB
	Power-supply rejection ratio (for new chip)	V_{IN} - V_{OUT} = 1V, frequency = 1kHz, I_{OUT} = 450mA		70		
T_J	Junction temperature		–40		150	°C
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature (for new chip)			175		
$T_{SD(HYST)}$	Hysteresis of thermal shutdown (for new chip)			20		
$\Delta V_{OUT}/\Delta T$	Temperature output voltage drift (for legacy chip)			0.5		mV/K

(1) Power dissipation is limited to 2W for device production testing purposes. The power dissipation is potentially higher during normal operation. See Section 8.1.4.1 for more information on how much power the device can dissipate while maintaining a junction temperature below 150°C.
(2) Specified by design.
(3) For the adjustable output this is tested in unity gain and resistor current is not included.

5.6 Electrical Characteristics (for KTT Package Only)

over recommended operating free-air temperature range, V_{IN} = 13.5V, T_J = −40°C to 150°C (unless otherwise noted) (see Section 6)

PARAMETER		Test Conditions		MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage	V_{IN} = 6V to 28V, I_{OUT} = 5mA to 400mA		4.9	5.0	5.1	V
		V_{IN} = 6V to 40V, I_{OUT} = 5mA to 200mA		4.9	5.0	5.1	
I_{CL}	Output current limit			450	700	950	mA
I_Q	Quiescent current I_Q = I_{IN} – I_{OUT} (for legacy chip)	I_{OUT} = 1mA	T_J = 25°C		100	220	µA
			T_J ≤ 85°C		100	220	
	Quiescent current I_Q = I_{IN} – I_{OUT} (for new chip)	I_{OUT} = 1mA	T_J = 25°C		28	50	
			T_J ≤ 85°C		28	55	
	Quiescent current I_Q = I_{IN} – I_{OUT}	I_{OUT} = 250mA			5	10	mA
		I_{OUT} = 400mA			12	22	mA
V_{DO}	Dropout voltage (1)	I_{OUT} = 300mA, V_{DO} = V_{IN} – V_{OUT}			250	500	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation (for legacy chip)	I_{OUT} = 5mA to 400mA			15	30	mV
	Load regulation (for new chip)	I_{OUT} = 5mA to 400mA, V_{IN} = 6V			15	30	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation (for legacy chip)	V_{IN} = 8V to 32V, I_{OUT} = 5mA		–15	5	15	mV
	Line regulation (for new chip)	V_{IN} = 6V to 40V, I_{OUT} = 5mA		–15	5	15	
PSRR	Power-supply rejection ratio	V_{IN} - V_{OUT} = 1V, frequency = 100Hz, Vr = 0.5V_{pp}, I_{OUT} = 450mA			60		dB
$\Delta V_{OUT}/\Delta T$	Temperature output voltage drift				0.5		mV/K

(1) Measured when the output voltage V_{OUT} has dropped 100mV from the nominal value obtained at V_{IN} = 13.5V.

5.7 Typical Characteristics

Specified for new chip at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT}, ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted).

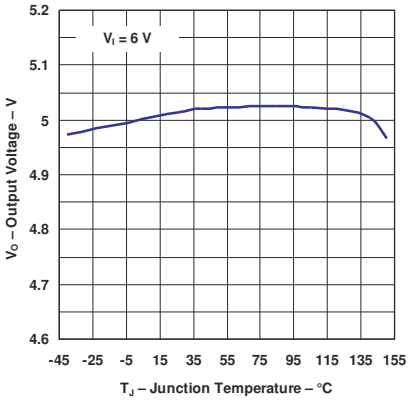


Figure 5-1. Output Voltage vs Junction Temperature (Legacy Chip)

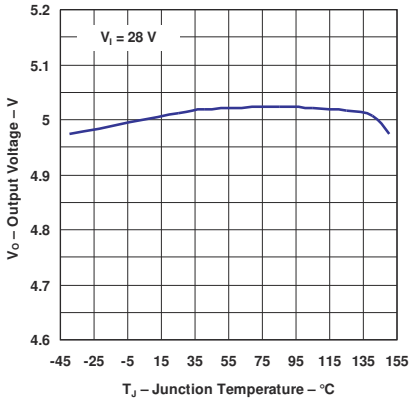


Figure 5-2. Output Voltage vs Junction Temperature (Legacy Chip)

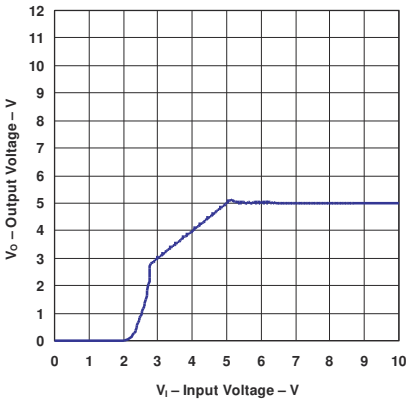


Figure 5-3. Output Voltage vs Input Voltage (Legacy Chip)

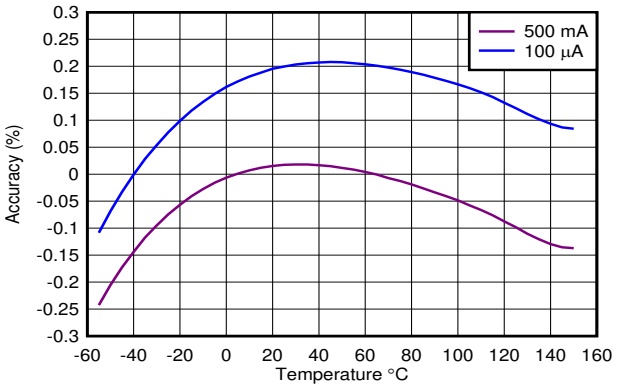
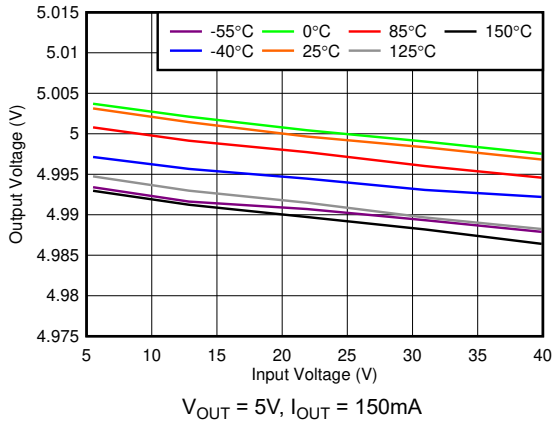
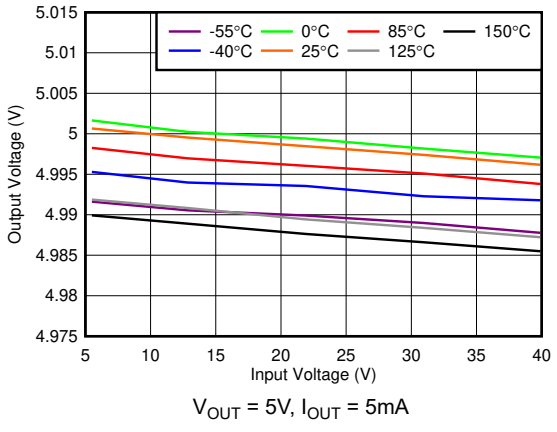


Figure 5-4. Output Accuracy vs Temperature (New Chip)



V_{OUT} = 5V, I_{OUT} = 150mA

Figure 5-5. Line Regulation vs V_{IN} (New Chip)

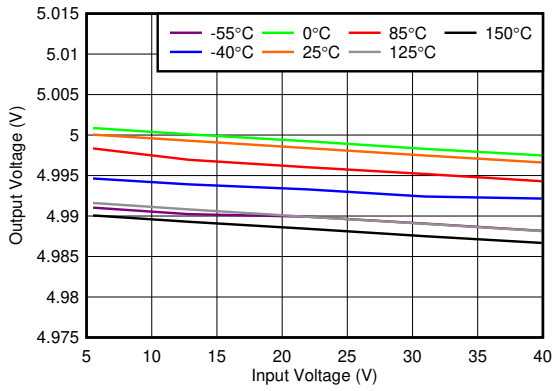


V_{OUT} = 5V, I_{OUT} = 5mA

Figure 5-6. Line Regulation vs V_{IN} (New Chip)

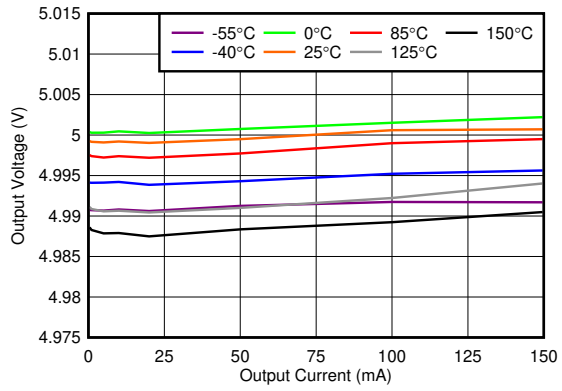
5.7 Typical Characteristics (continued)

Specified for new chip at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT}, ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted).



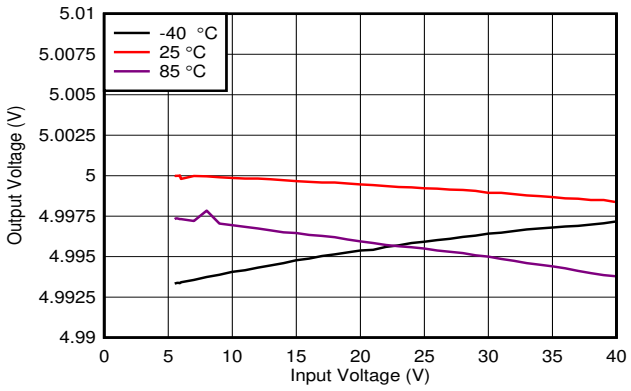
V_{OUT} = 5V, I_{OUT} = 1mA

Figure 5-7. Line Regulation vs V_{IN} (New Chip)



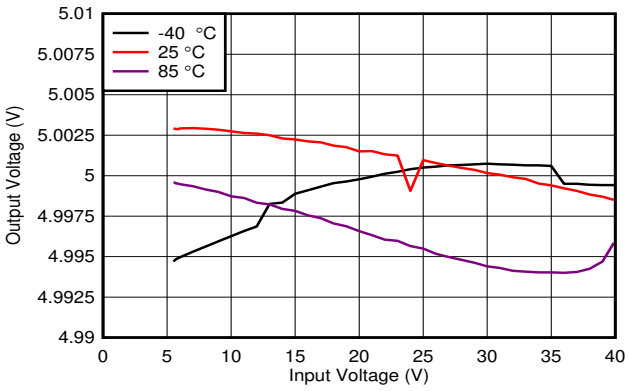
V_{OUT} = 5V

Figure 5-8. Load Regulation vs I_{OUT} (New Chip)



C_{OUT} = 10µF, V_{OUT} = 5V

Figure 5-9. Line Regulation at 50mA (New Chip)



C_{OUT} = 10µF, V_{OUT} = 5V

Figure 5-10. Line Regulation at 100mA (New Chip)

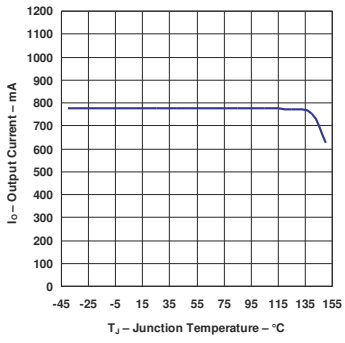


Figure 5-11. Output Current vs Junction Temperature (Legacy Chip)

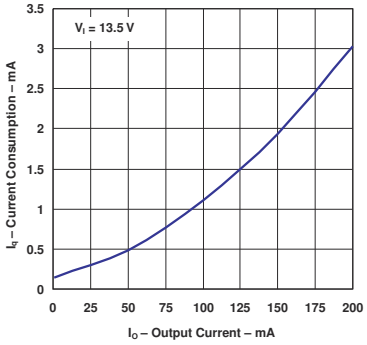


Figure 5-12. Current Consumption vs Output Current (Legacy Chip)

5.7 Typical Characteristics (continued)

Specified for new chip at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT}, ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted).

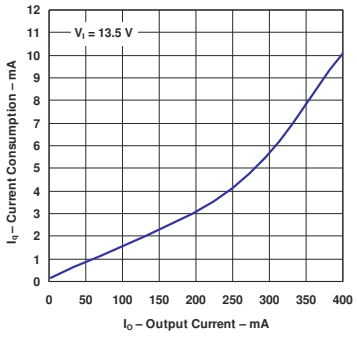


Figure 5-13. Current Consumption vs Output Current (Legacy Chip)

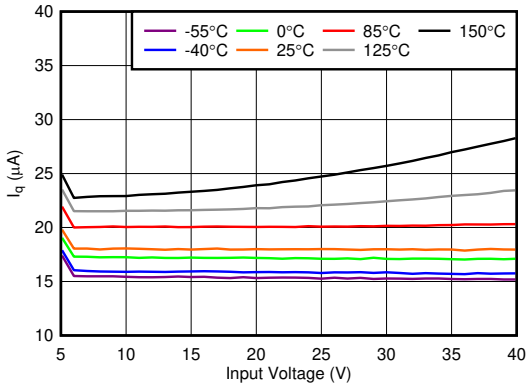


Figure 5-14. Quiescent Current (I_Q) vs V_{IN} (New Chip)

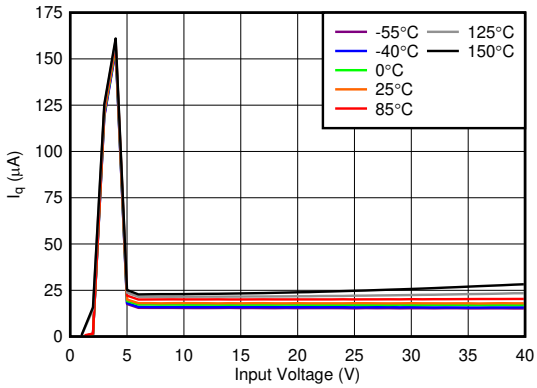


Figure 5-15. Quiescent Current (I_Q) vs V_{IN} (New Chip)

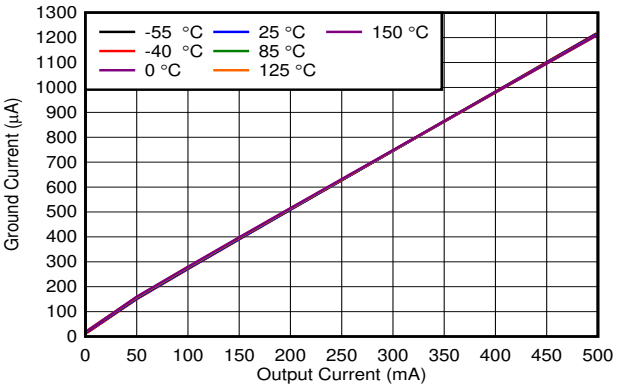


Figure 5-16. Ground Current (I_{GND}) vs I_{OUT} (New Chip)

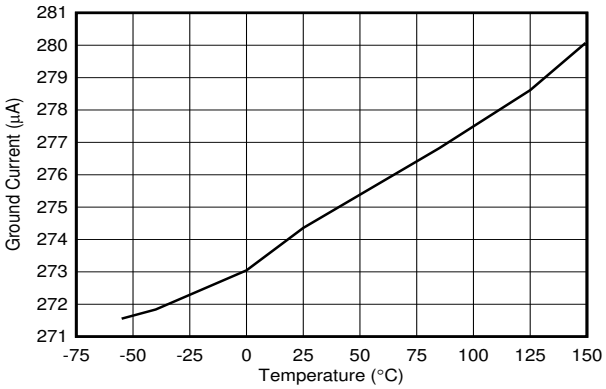


Figure 5-17. Ground Current at 100mA (New Chip)

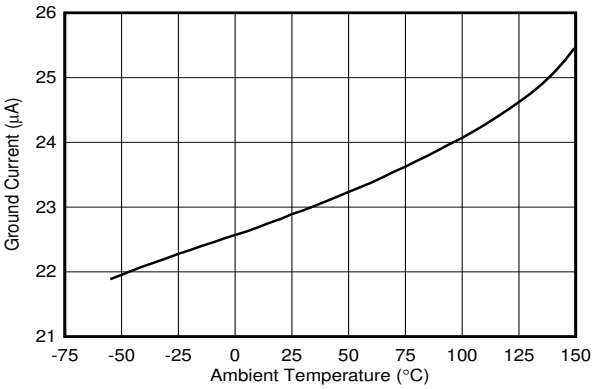


Figure 5-18. Ground Current at 500µA (New Chip)

5.7 Typical Characteristics (continued)

Specified for new chip at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT}, ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted).

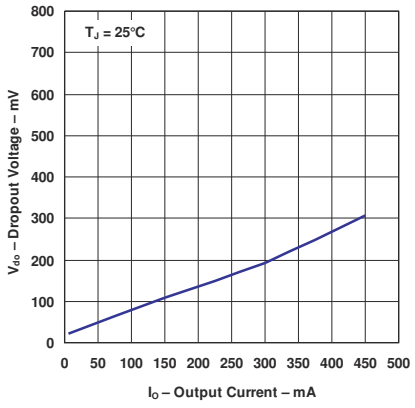
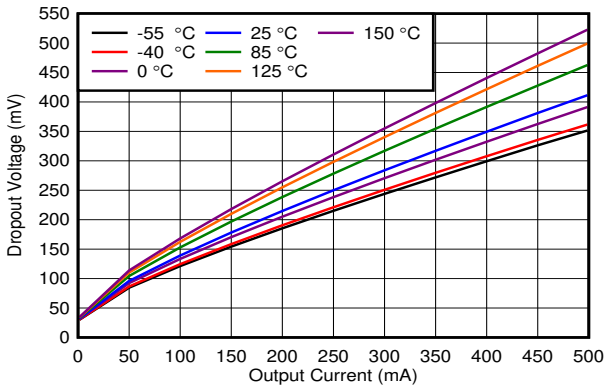


Figure 5-19. Dropout Voltage vs Output Current (Legacy Chip)



V_{IN} = 3V

Figure 5-20. Dropout Voltage (V_{DO}) vs I_{OUT} (New Chip)

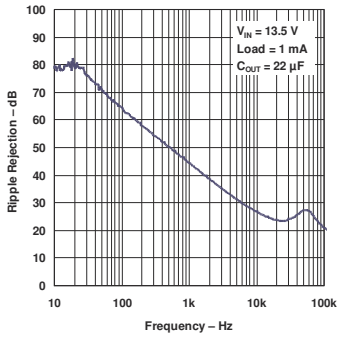


Figure 5-21. Power-Supply Ripple Rejection vs Frequency (Legacy Chip)

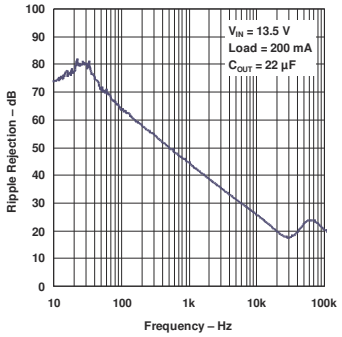


Figure 5-22. Power-Supply Ripple Rejection vs Frequency (Legacy Chip)

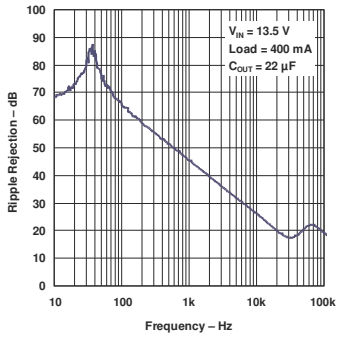
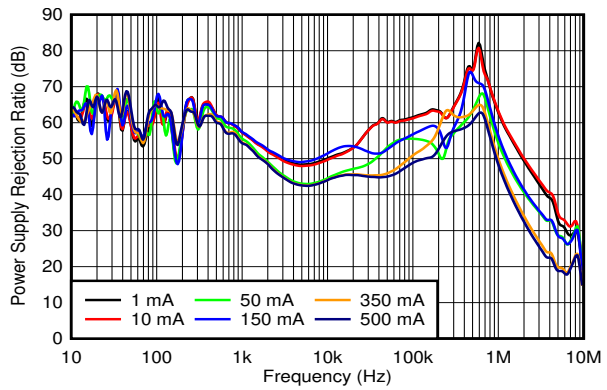


Figure 5-23. Power-Supply Ripple Rejection vs Frequency (Legacy Chip)

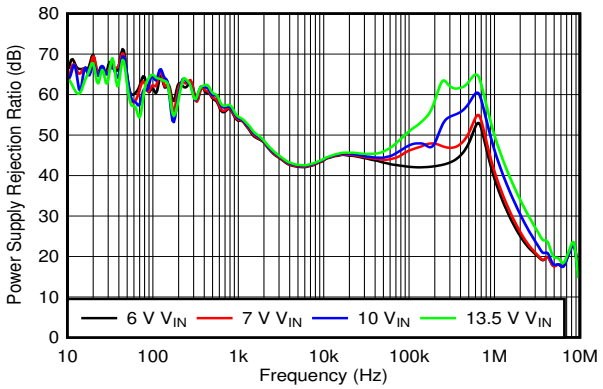


C_{OUT} = 10µF (X7R 50V), V_{OUT} = 5V

Figure 5-24. Power-Supply Ripple Rejection vs Frequency and I_{OUT} (New Chip)

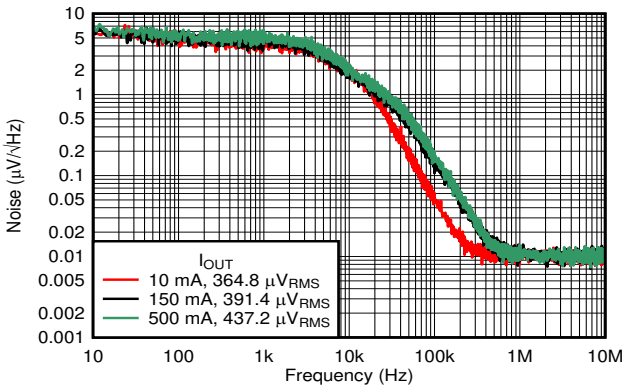
5.7 Typical Characteristics (continued)

Specified for new chip at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT}, ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted).



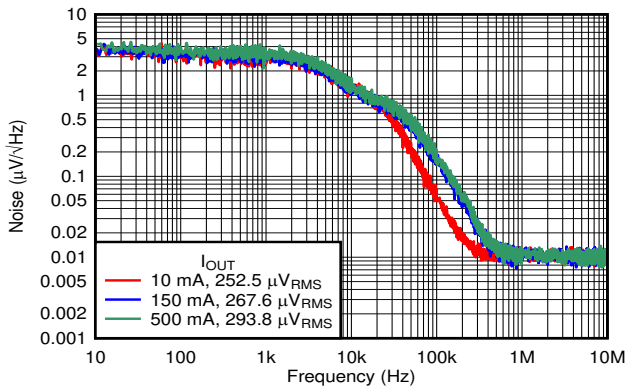
C_{OUT} = 10µF (X7R 50V), I_{OUT} = 500mA, V_{OUT} = 5V

Figure 5-25. Power-Supply Ripple Rejection vs Frequency and V_{IN} (New Chip)



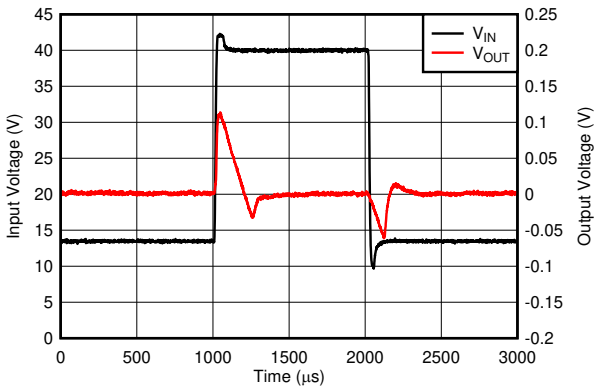
C_{OUT} = 10µF (X7R 50V), V_{OUT} = 5V

Figure 5-26. Noise vs Frequency (Legacy Chip)



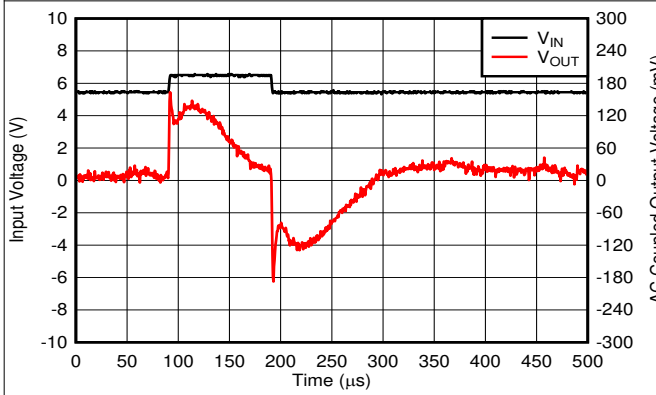
C_{OUT} = 10µF (X7R 50V), V_{OUT} = 3.3V

Figure 5-27. Noise vs Frequency (Legacy Chip)



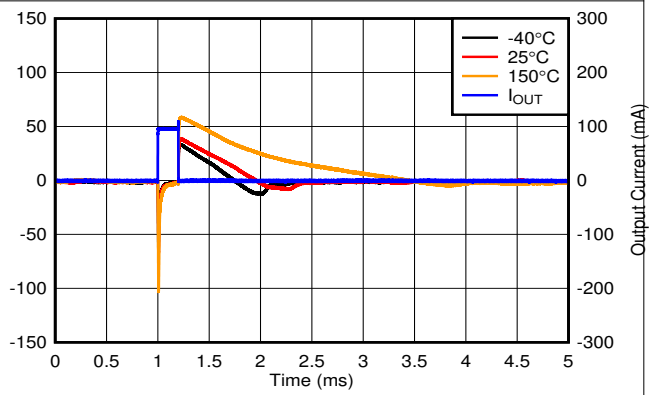
V_{OUT} = 5V, I_{OUT} = 1mA, V_{IN} = 13.5V to 45V, slew rate = 2.7V/µs

Figure 5-28. Line Transients (New Chip)



V_{OUT} = 5V, I_{OUT} = 100mA, V_{IN} = 5.5V to 6.5V, rise time = 1µs

Figure 5-29. Line Transients (New Chip)

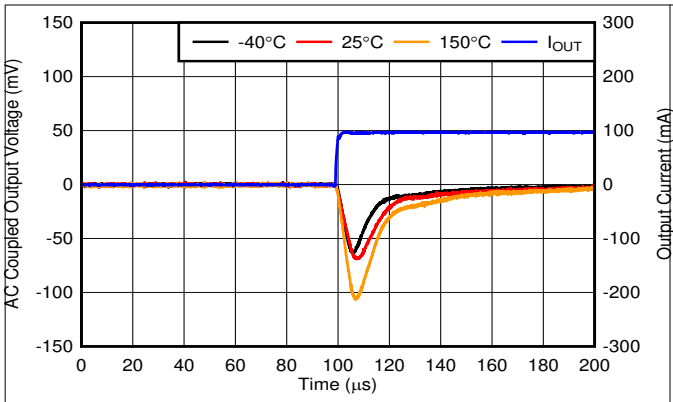


V_{OUT} = 5V, I_{OUT} = 0mA to 100mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-30. Load Transient, No Load to 100mA (New Chip)

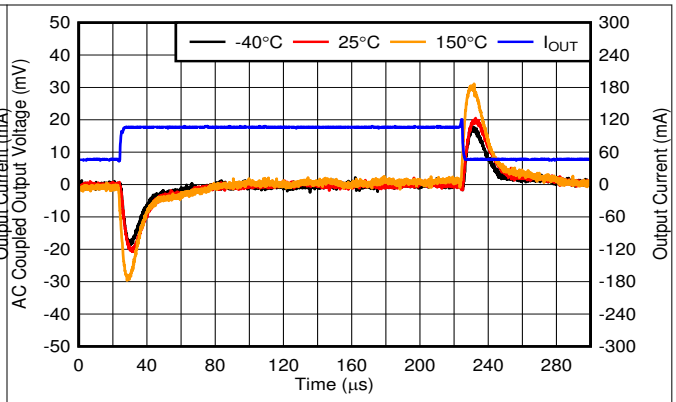
5.7 Typical Characteristics (continued)

Specified for new chip at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT}, ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted).



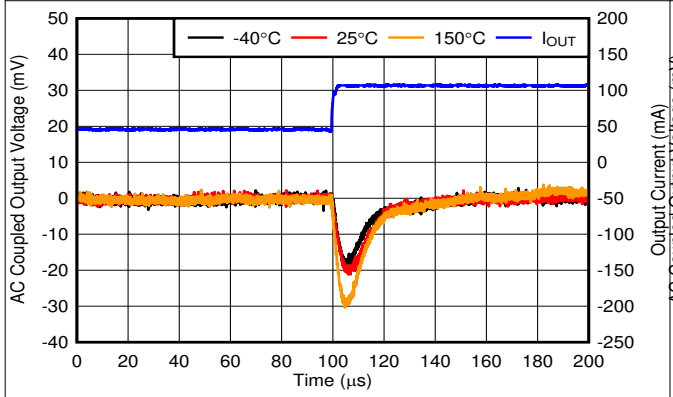
V_{OUT} = 5V, I_{OUT} = 0mA to 100mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-31. Load Transient, No Load to 100mA Rising Edge (New Chip)



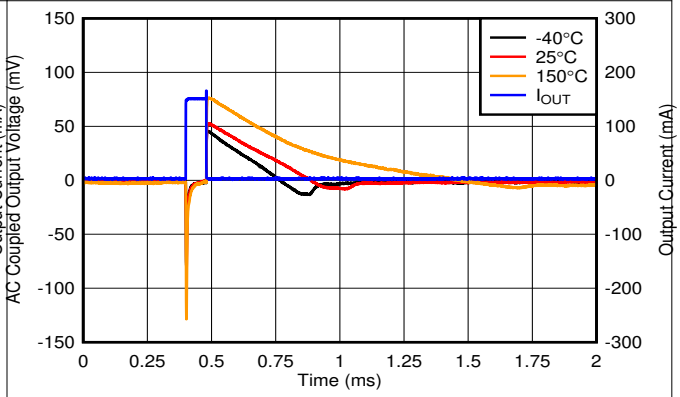
V_{OUT} = 5V, I_{OUT} = 45mA to 105mA, slew rate = 0.1A/µs, C_{OUT} = 10µF

Figure 5-32. Load Transient, 45mA to 105mA (New Chip)



V_{OUT} = 5V, I_{OUT} = 45mA to 105mA, slew rate = 0.1A/µs, C_{OUT} = 10µF

Figure 5-33. Load Transient, 45mA to 105mA Rising Edge (New Chip)

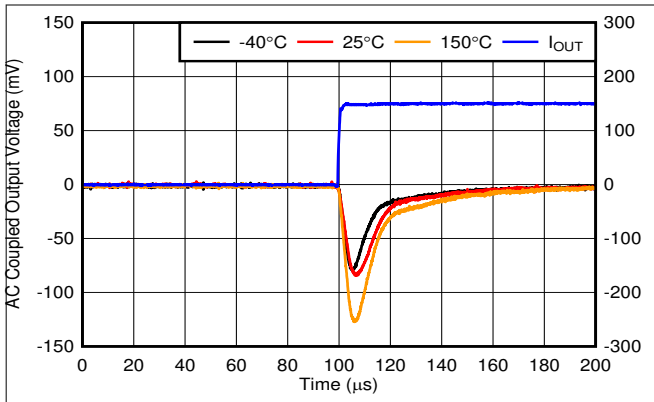


V_{OUT} = 5V, I_{OUT} = 0mA to 150mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-34. Load Transient, No Load to 150mA (New Chip)

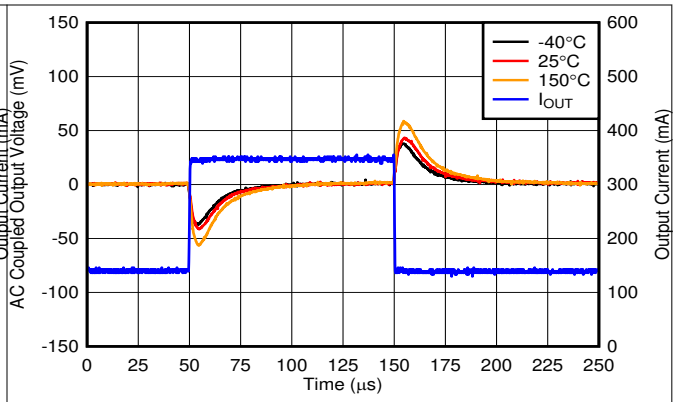
5.7 Typical Characteristics (continued)

Specified for new chip at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT}, ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted).



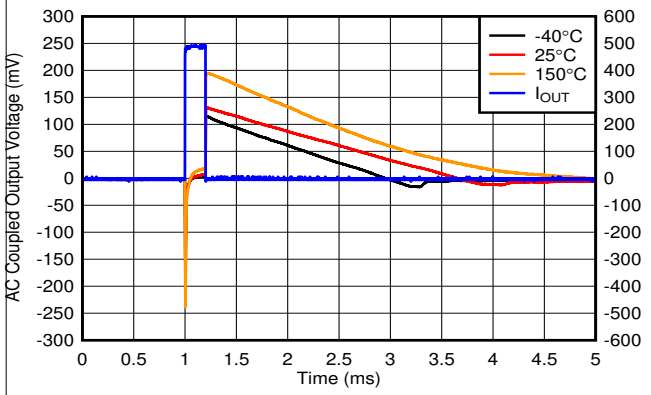
V_{OUT} = 5V, I_{OUT} = 0mA to 150mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-35. Load Transient, No Load to 150mA Rising Edge (New Chip)



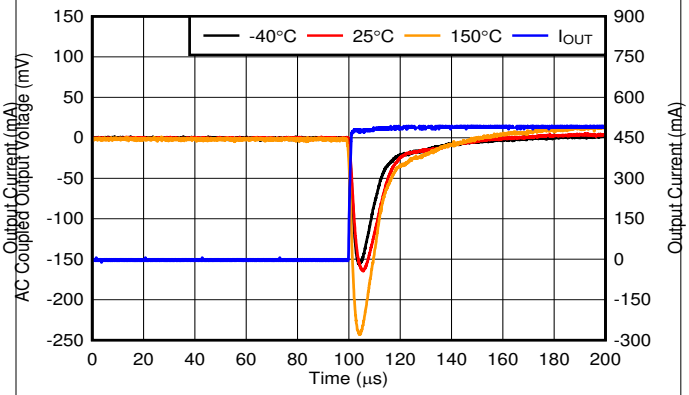
V_{OUT} = 5V, I_{OUT} = 150mA to 350mA, slew rate = 0.1A/µs, C_{OUT} = 10µF

Figure 5-36. Load Transient, 150mA to 350mA (New Chip)



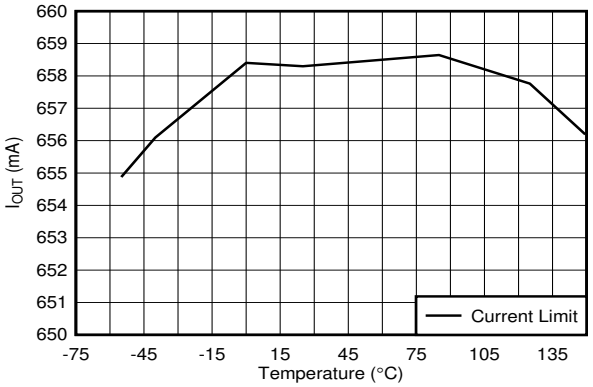
V_{OUT} = 5V, I_{OUT} = 0mA to 500mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-37. Load Transient, No Load to 500mA (New Chip)



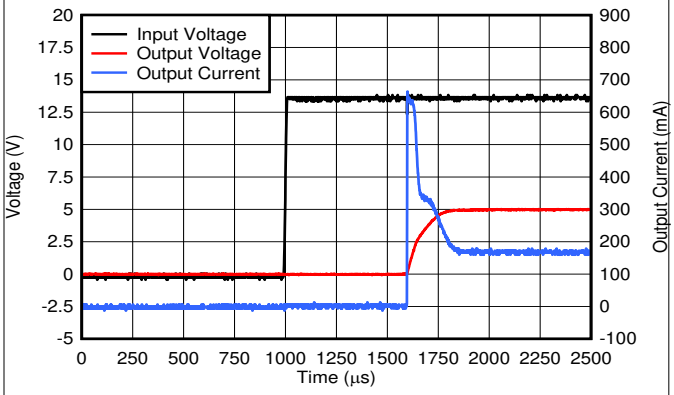
V_{OUT} = 5V, I_{OUT} = 0mA to 500mA, slew rate = 1A/µs, C_{OUT} = 10µF

Figure 5-38. Load Transient, No Load to 500mA Rising Edge (New Chip)



V_{IN} = V_{OUT} + 1V, V_{OUT} = 90% × $V_{OUT(NOM)}$

Figure 5-39. Output Current Limit vs Temperature (New Chip)



V_{IN} = V_{OUT} + 1V, V_{OUT} = 90% × $V_{OUT(NOM)}$

Figure 5-40. Start-Up Plot Inrush Current (New Chip)

5.7 Typical Characteristics (continued)

Specified for new chip at T_J = –40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 2.2µF, 1mΩ < C_{OUT}, ESR < 2Ω, and C_{IN} = 1µF (unless otherwise noted).

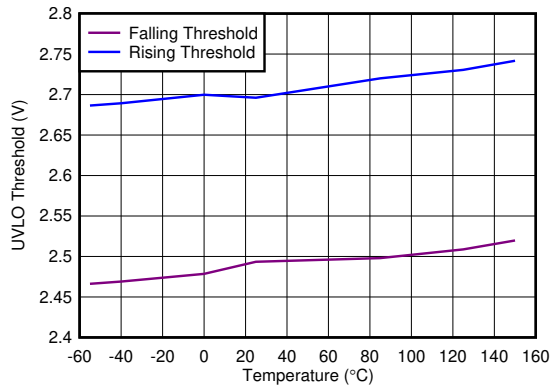


Figure 5-41. Undervoltage Lockout (UVLO) Threshold vs Temperature (New Chip)

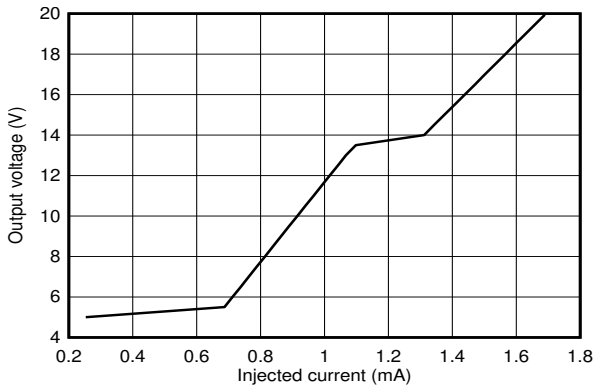


Figure 5-42. Output Voltage vs Injected Current (New Chip)

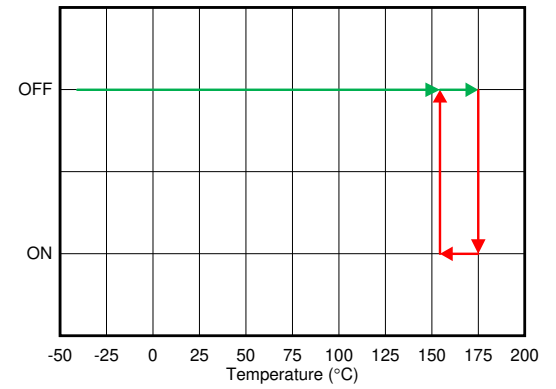


Figure 5-43. Thermal Shutdown (New Chip)

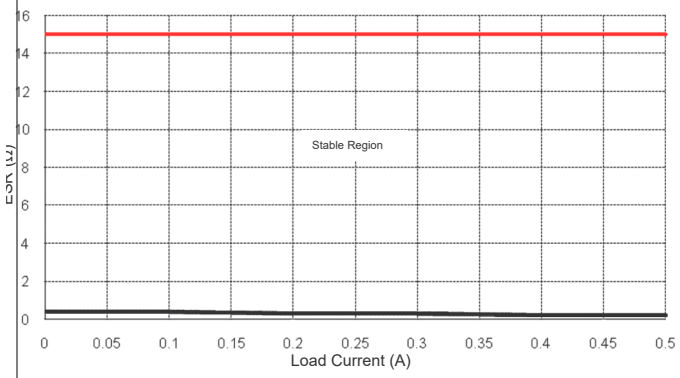


Figure 5-44. ESR Stability vs Load Current (Legacy Chip)

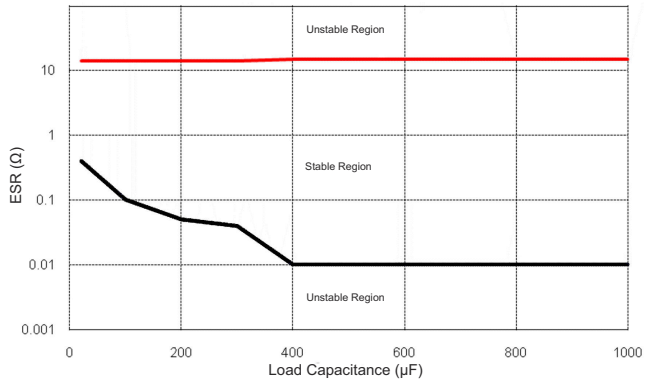


Figure 5-45. ESR Stability vs Load Capacitance (Legacy Chip)

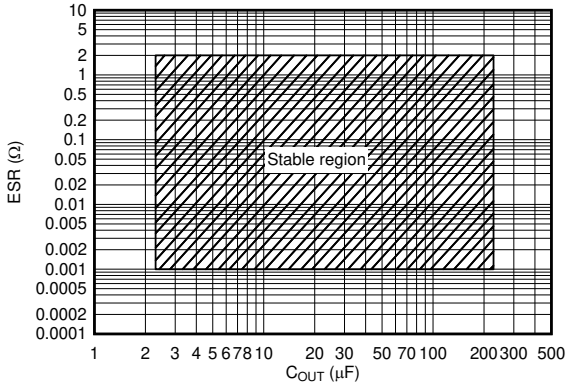


Figure 5-46. Stability, ESR vs C_{OUT} (New Chip)

6 Parameter Measurement Information

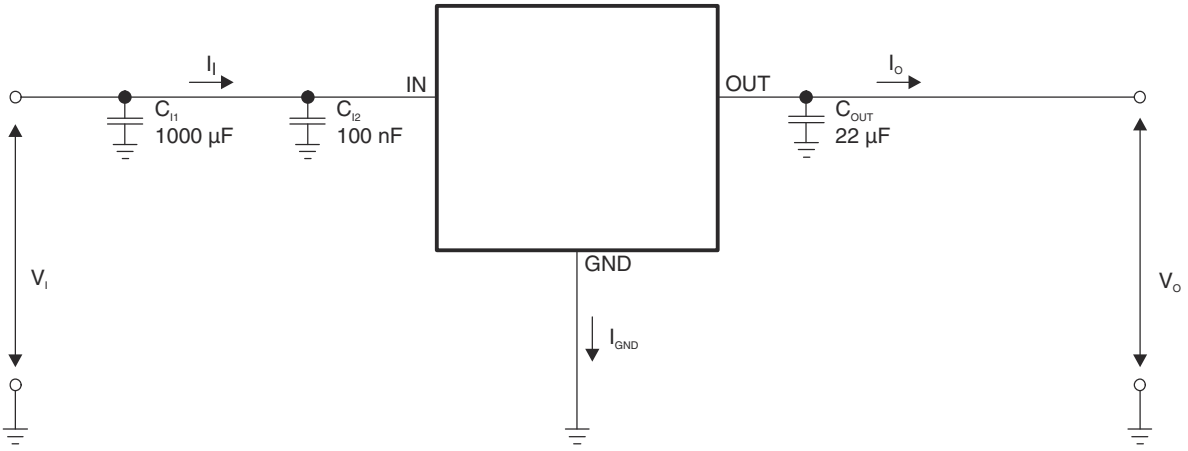


Figure 6-1. Test Circuit

7 Detailed Description

7.1 Overview

The TL720M05-Q1 is a low-dropout linear regulator (LDO) with improved transient performance that allows for quick response to changes in line or load conditions. The device also features a novel output overshoot reduction feature (new chip) that minimizes output overshoot during cold-crank conditions.

During normal operation, the device has a tight DC accuracy of ±2.0% over line, load, and temperature. The increased accuracy allows for the powering of sensitive analog loads or sensors.

The TL720M05-Q1 has overtemperature protection and overcurrent protection during a load-short or fault condition on the output.

7.2 Functional Block Diagrams

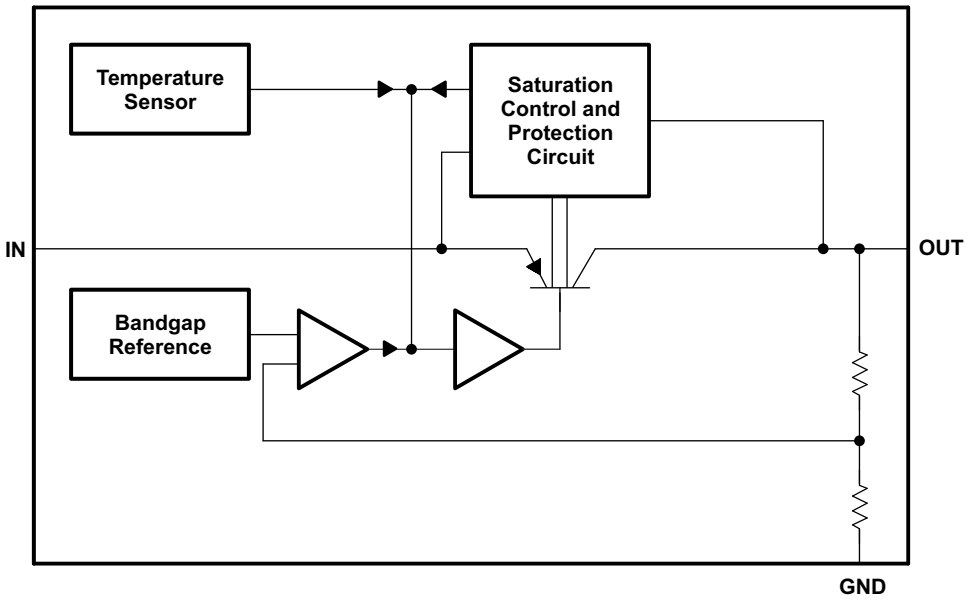


Figure 7-1. Functional Block Diagram (Legacy Chip)

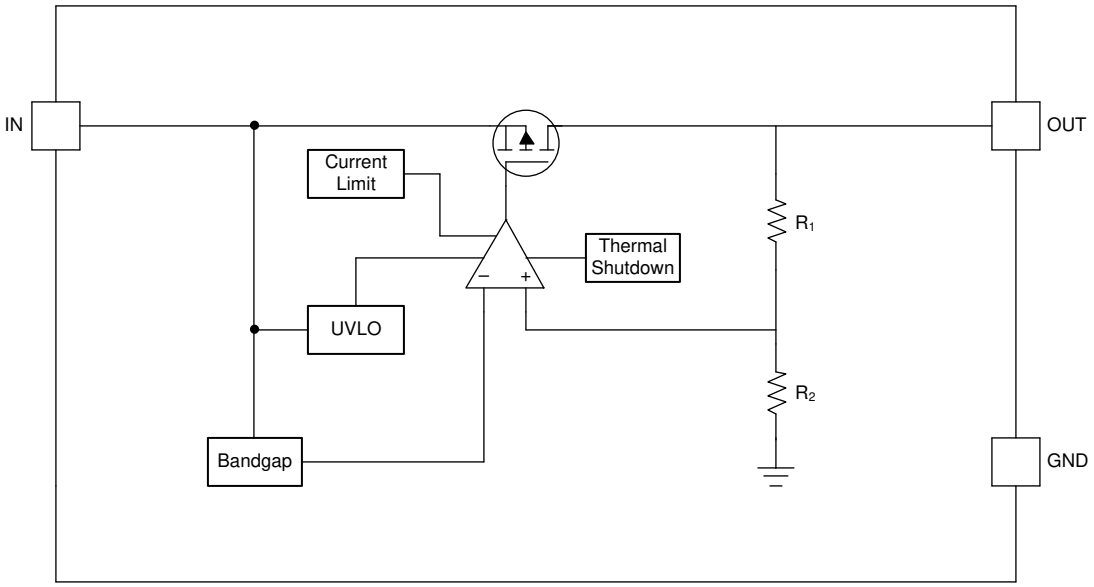


Figure 7-2. Functional Block Diagram (New Chip)

7.3 Feature Description

7.3.1 Undervoltage Lockout

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn-on and turn-off of the output voltage. To prevent the device from turning off if the input drops during turn-on, the UVLO has hysteresis as specified in the *Electrical Characteristics (for KVU Package Only)* table.

7.3.2 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus, the device cycles on and off when thermal shutdown is reached until power dissipation reduces. Power dissipation during start-up is high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above the maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics (for KVU Package Only)* and *Electrical Characteristics (for KTT package only)* tables.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 7-3 shows a diagram of the current limit.

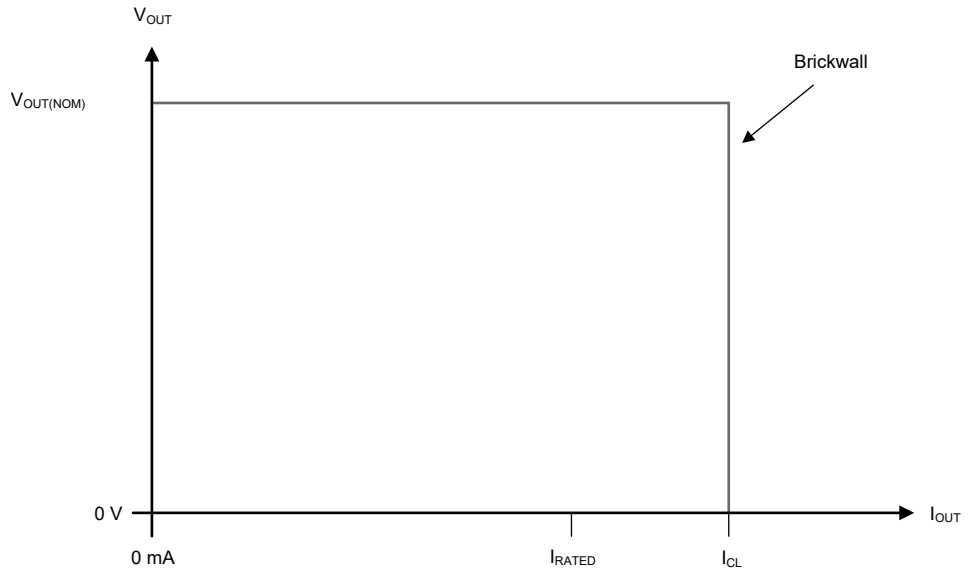


Figure 7-3. Current Limit

7.4 Device Functional Modes

Table 7-1 shows the conditions that lead to the different modes of operation. See tables in Section 5.5 and Section 5.6 for parameter values.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	V_{IN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In dropout mode, the output voltage tracks the input voltage. In dropout mode, the transient performance of the device becomes significantly degraded. During dropout mode, the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven fully on. The steady dropout state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start up. Dropout occurs when $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the input voltage returns to a value ≥ $V_{OUT(NOM)} + V_{DO}$, the output voltage potentially overshoots for a short period of time. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage. During dropout exit, the device pulls the pass transistor back into the linear region.

7.4.3 Disabled

Shut down the device output by forcing the input voltage below the UVLO falling threshold (see the *Electrical Characteristics (for KVU Package Only)* table). When disabled, the pass transistor turns off and internal circuits shut down.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Based on the end-application, different values of external components are available. In some cases, an application requires a larger output capacitor during fast load steps to prevent a reset from occurring. Use a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

8.1.1 Input and Output Capacitor Selection

8.1.1.1 Legacy Chip Capacitor Selection

The input capacitor (C_{IN}) compensates for line fluctuation. Using a resistor of approximately 1Ω in series with C_{IN} dampens the oscillation of input inductivity and input capacitance. The output capacitor (C_{OUT}) stabilizes the regulation circuit. The output is stable at C_{OUT} ≥ 22µF and ESR ≤ 5Ω, which is within the operating temperature range.

8.1.1.2 New Chip Output Capacitor

The new chip version of the TL720M05-Q1 requires a 2.2µF or larger output capacitor (1µF or larger capacitance) for stability. An equivalent series resistance (ESR) between 0.001Ω and 2Ω is also required. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220µF.

8.1.1.3 New Chip Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply is high impedance over a large range of frequencies, use several input capacitors in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as V_{IN} – V_{OUT} at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

8.1.3 Reverse Current

Excessive reverse current potentially damages this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current potentially occur are outlined in this section, all of which exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3V$.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

8.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the PCB, and correct sizing of the thermal plane. Verify that the printed circuit board (PCB) area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Note

Correctly select the system voltage rails to minimize power dissipation and achieve greater efficiency. For the lowest power dissipation, use the minimum input voltage that correct output regulation requires.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. Verify that the pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. Power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the ambient air temperature (T_A). $R_{\theta JA}$ is the junction-to-ambient thermal resistance. Equation 3 calculates this relationship.

$$T_J = T_A + \left(R_{\theta JA} \times P_D\right) \quad (3)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. Therefore, $R_{\theta JA}$ varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area. This resistance is used as a relative measure of package thermal performance.

8.1.4.1 Thermal Performance Versus Copper Area

The most used thermal resistance parameter $R_{\theta JA}$ is highly dependent on the heat-spreading capability built into the particular PCB design. Therefore, $R_{\theta JA}$ varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the table in Section 5.4 is determined by the JEDEC standard (see Figure 8-1), PCB, and copper-spreading area. $R_{\theta JA}$ is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of $R_{\theta JCbot}$ plus the thermal resistance contribution by the PCB copper. $R_{\theta JCbot}$ is the package junction-to-case (bottom) thermal resistance.

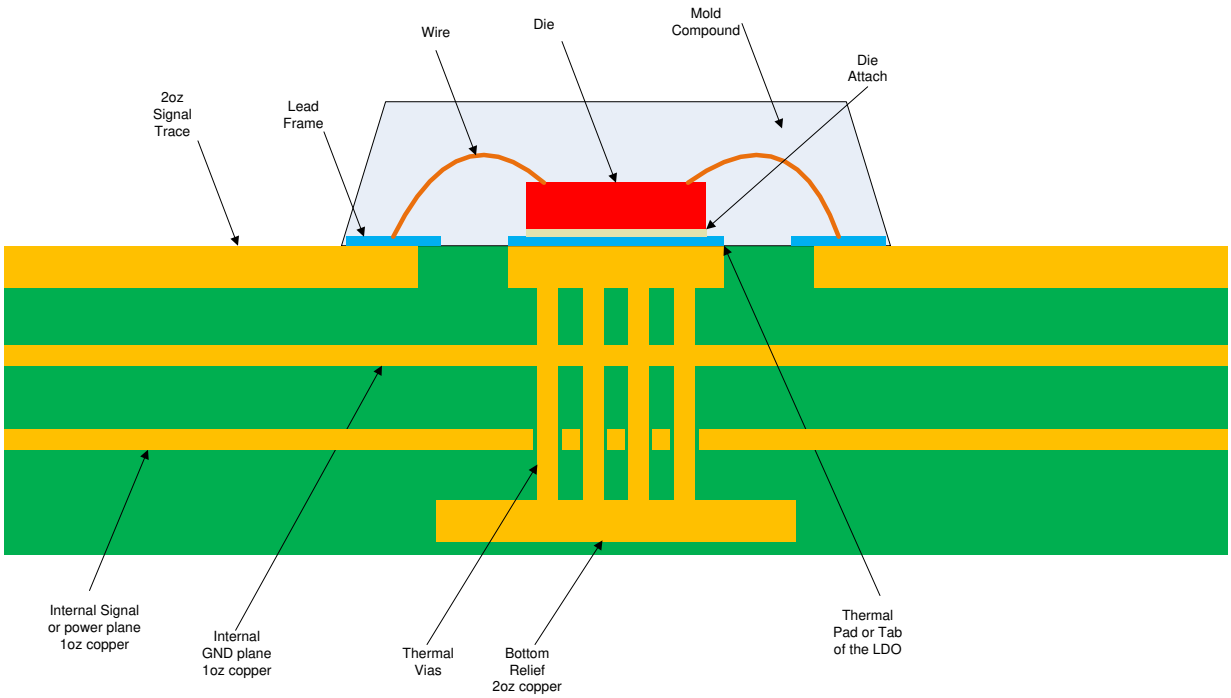


Figure 8-1. JEDEC Standard 2s2p PCB

Figure 8-2 and Figure 8-3 show the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness. These plots are generated with a 101.6mm × 101.6mm × 1.6mm PCB of two and four layers. For the 4-layer board, inner planes use 1oz copper thickness. Outer layers are simulated with both 1oz and 2oz copper thickness. A 3 × 4 (KVU package) array of thermal vias with a 300µm drill diameter and 25µm copper plating is located beneath the device thermal pad. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area.

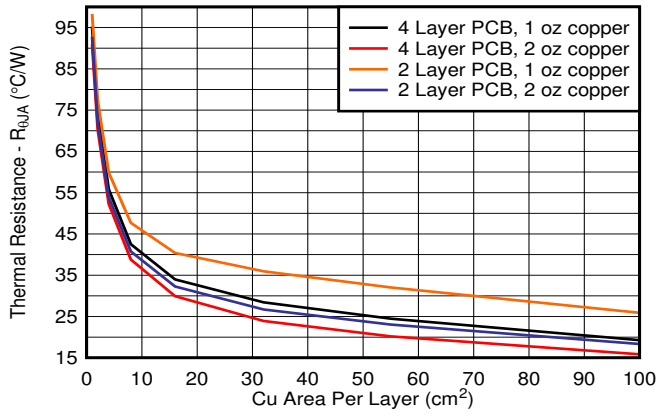


Figure 8-2. $R_{\theta JA}$ vs Copper Area (KVU Package)

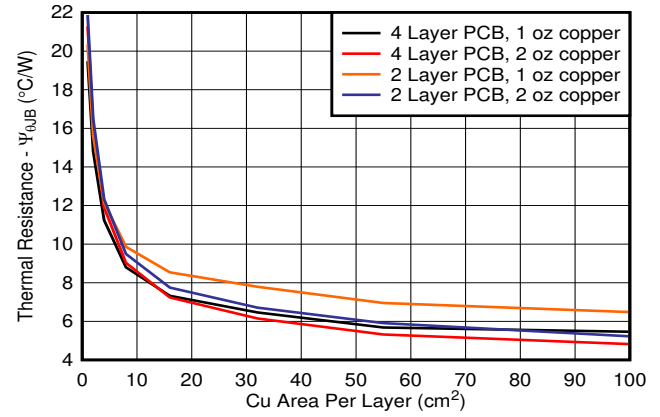


Figure 8-3. ψ_{JB} vs Copper Area (KVU Package)

8.1.4.2 Power Dissipation Versus Ambient Temperature

Figure 8-4 is based off of a JESD51-7 4-layer, high-K board. Estimate the allowable power dissipation with Equation 4. Add top layer copper and increase the number of thermal vias to improve thermal dissipation in the JEDEC high-K layout. See the *An empirical analysis of the impact of board layout on LDO thermal performance* application note. The allowable thermal dissipation improves by up to 50% if using a good thermal layout.

$$T_A + R_{\theta JA} \times P_D \leq 150°C \quad (4)$$

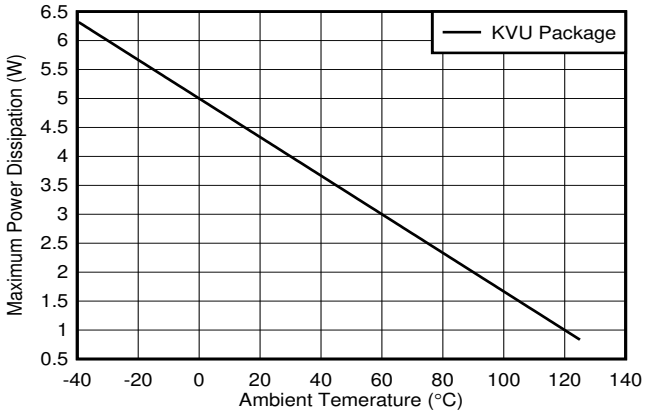


Figure 8-4. TL720M05-Q1 Allowable Power Dissipation

8.1.5 Estimating Junction Temperature

The JEDEC standard recommends using psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (5)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (6)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

8.2 Typical Application

Figure 8-5 shows a typical application circuit for the TL720M05-Q1.

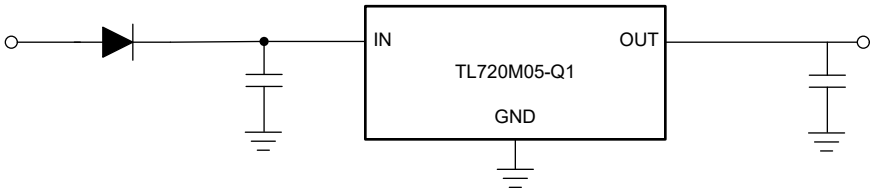


Figure 8-5. Typical Application Diagram (New Chip)

8.2.1 Design Requirements

Use the parameters listed in Table 8-1 for this design example.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4V to 40V
Output voltage	5V
Output current rating	400mA
Output capacitor range	10µF to 200µF

8.2.2 Detailed Design Procedure

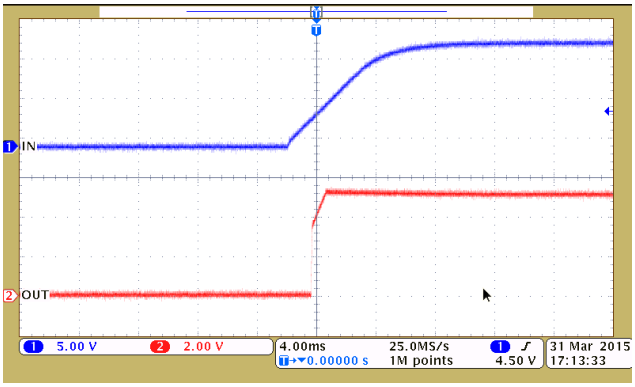
8.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 1µF. Establish that the voltage rating is greater than the maximum input voltage.

8.2.2.2 Output Capacitor

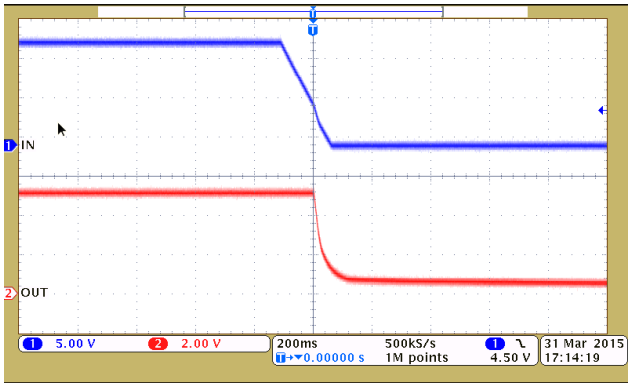
The device (new chip) requires an output capacitor to stabilize the output voltage. Verify that the capacitor value is between 2.2µF and 200µF and the ESR range is between 1mΩ and 2Ω. For this design, use a low ESR, 10µF ceramic capacitor to improve transient performance.

8.2.3 Application Curves



Channel 1: V_{IN}, channel 2: V_{OUT}

Figure 8-6. Power-Up Waveform (Load = 50mA) (Legacy Chip)



Channel 1: V_{IN}, channel 2: V_{OUT}

Figure 8-7. Power-Down Waveform (Load = 50mA) (Legacy Chip)

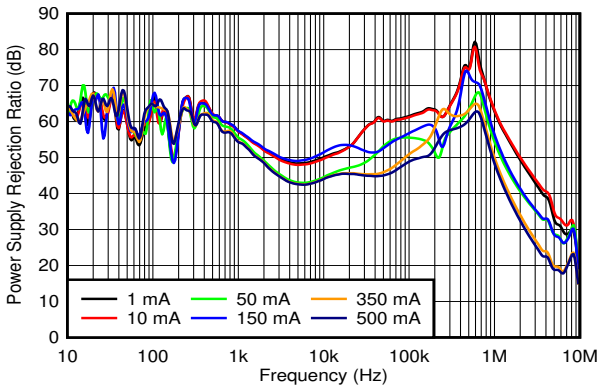
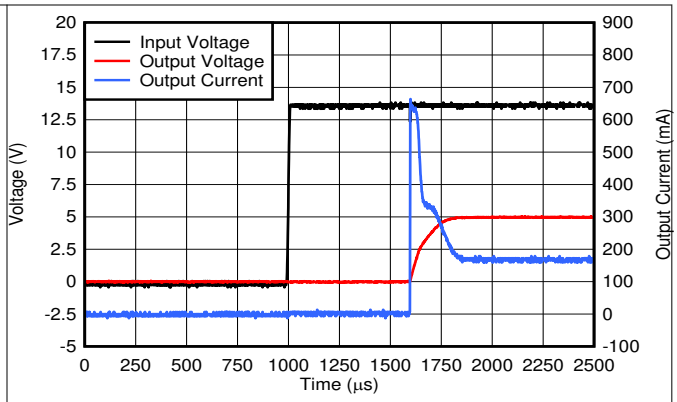


Figure 8-8. Power-Supply Ripple Rejection vs Frequency and I_{OUT} (New Chip)



V_{IN} = V_{OUT} + 1V, V_{OUT} = 90% × $V_{OUT(NOM)}$

Figure 8-9. Start-Up Plot Inrush Current (New Chip)

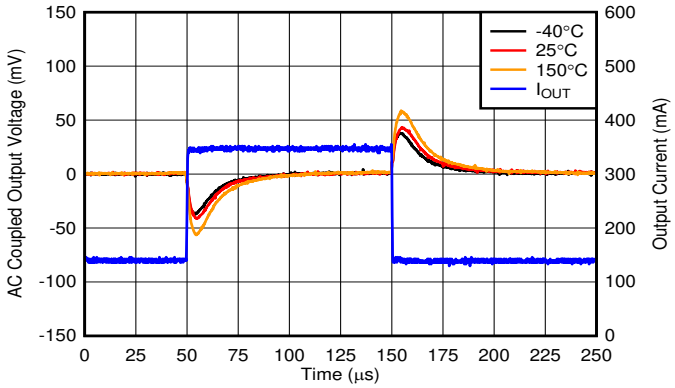


Figure 8-10. Transient Response (New Chip)

8.3 Power Supply Recommendations

This device is designed for operation from a 4V to 40V input voltage supply. Verify that the input supply is well regulated. Do not place the input supply more than a few inches from the TL720M05-Q1. If this location is unavoidable, add a 22µF electrolytic capacitor and a ceramic bypass capacitor at the input.

8.4 Layout

8.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board. Place the circuit components as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin, as close as possible to each other. Use wide, component-side, copper surface for the connections. Using vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. Place a ground reference plane embedded in the PCB or located on the bottom side of the PCB opposite the components. The reference plane provides output voltage accuracy and shields noise. This plane also behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, a ground plane is necessary to meet thermal requirements.

8.4.2 Layout Examples

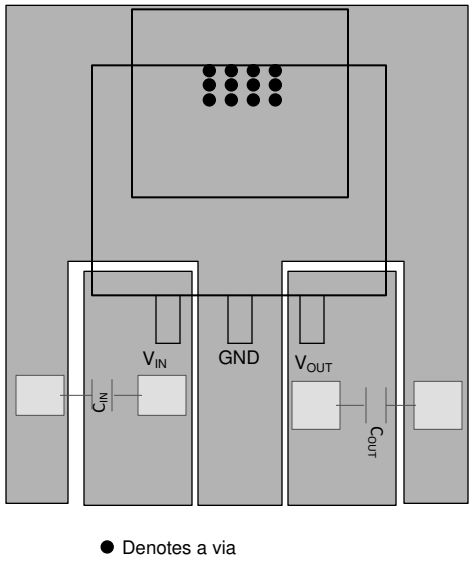


Figure 8-11. Layout Example Diagram for KVU, KTT Packages

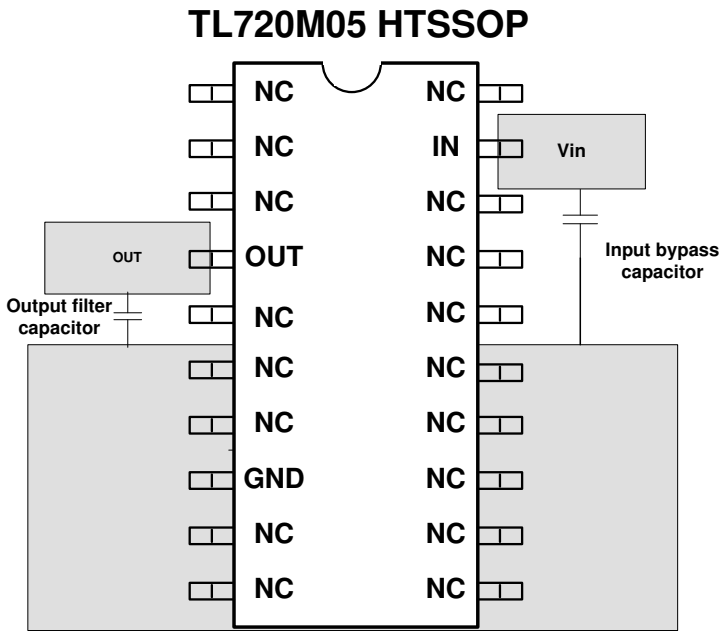


Figure 8-12. Layout Example Diagram for PWP Package (Legacy Chip)

9 Device and Documentation Support

9.1 Device Support

9.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV709. Request the MLTLDO2EVM evaluation module (and related user's guide) at the TI website through the product folders.

9.1.2 Device Nomenclature

Table 9-1. Device Nomenclature

PRODUCT(1)	V_{OUT}
TL720M05**Q xxx**R**Q1**	**xxx** is the package designation (for example, KVU = TO-252; KTT = DDPAK/TO-263; PWP = HTSSOP). **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

9.1.3 Development Support

For the PSpice® model, see Texas Instruments, *TPS7B88-Q1 PSpice Transient Model (5V Output)* simulation model

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *An empirical analysis of the impact of board layout on LDO thermal performance* application note
- Texas Instruments, *Know Your Limits* application note
- Texas Instruments, *LDO Noise Demystified* application note
- Texas Instruments, *LDO PSRR Measurement Simplified* application note
- Texas Instruments, *MLTLDO2EVM-037 EVM* user's guide
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (May 2024) to Revision J (August 2025)	Page
• Deleted new chip output voltage accuracy	1
• Deleted new chip low dropout voltage	1
• Deleted light load quiescent current data	1
• Updated normal operation DC accuracy from: ±1.15% to: ±2.0% throughout document	1
• Updated from: Electrical Characteristics to: Electrical Characteristics (for KVU Package Only)	5
• Added Electrical Characteristics (for KTT Package Only) section	6

Changes from Revision H (November 2014) to Revision I (May 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed entire document to align with current family format	1
• Added M3 devices to document	1
• Changed *package size* values in *Package Information* table	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL720M05GQKVURQ1	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	720M05Q
TL720M05GQKVURQ1.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	720M05Q
TL720M05GQKVURQ1M3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	720M05Q
TL720M05GQKVURQ1M3.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	720M05Q
TL720M05QKTTRM3Q1	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	T720M05Q
TL720M05QKTTRQ1	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	T720M05Q
TL720M05QKTTRQ1.A	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	T720M05Q
TL720M05QKVURQ1	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	720M05Q
TL720M05QKVURQ1.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	720M05Q
TL720M05QKVURQ1M3	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	720M05Q
TL720M05QKVURQ1M3.A	Active	Production	TO-252 (KVU) | 3	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	720M05Q
TL720M05QPWPRQ1	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	720M05Q
TL720M05QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	720M05Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

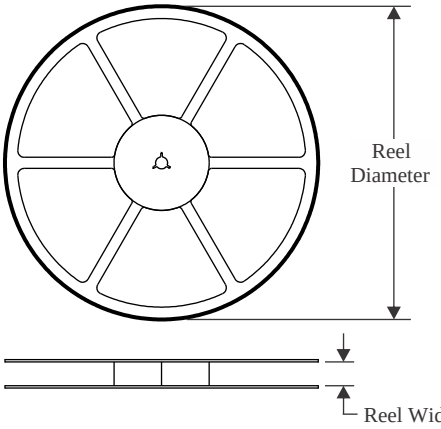
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

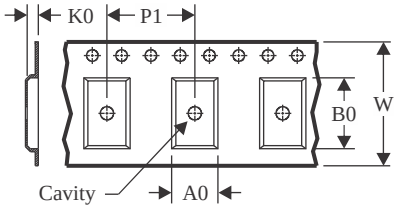
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

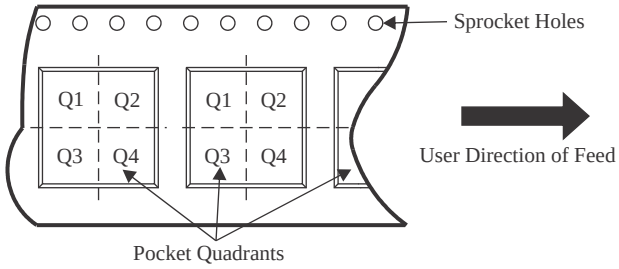


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

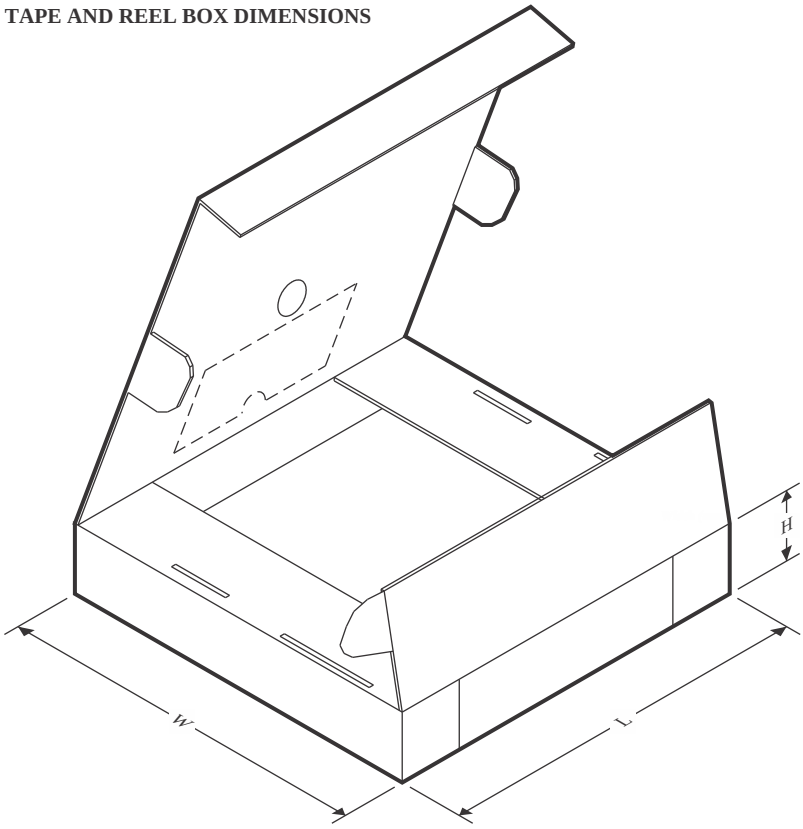
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL720M05GQKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL720M05GQKVURQ1M3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL720M05QKTTRM3Q1	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TL720M05QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL720M05QKVURQ1M3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL720M05QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL720M05GQKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TL720M05GQKVURQ1M3	TO-252	KVU	3	2500	340.0	340.0	38.0
TL720M05QKTTRM3Q1	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TL720M05QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TL720M05QKVURQ1M3	TO-252	KVU	3	2500	340.0	340.0	38.0
TL720M05QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

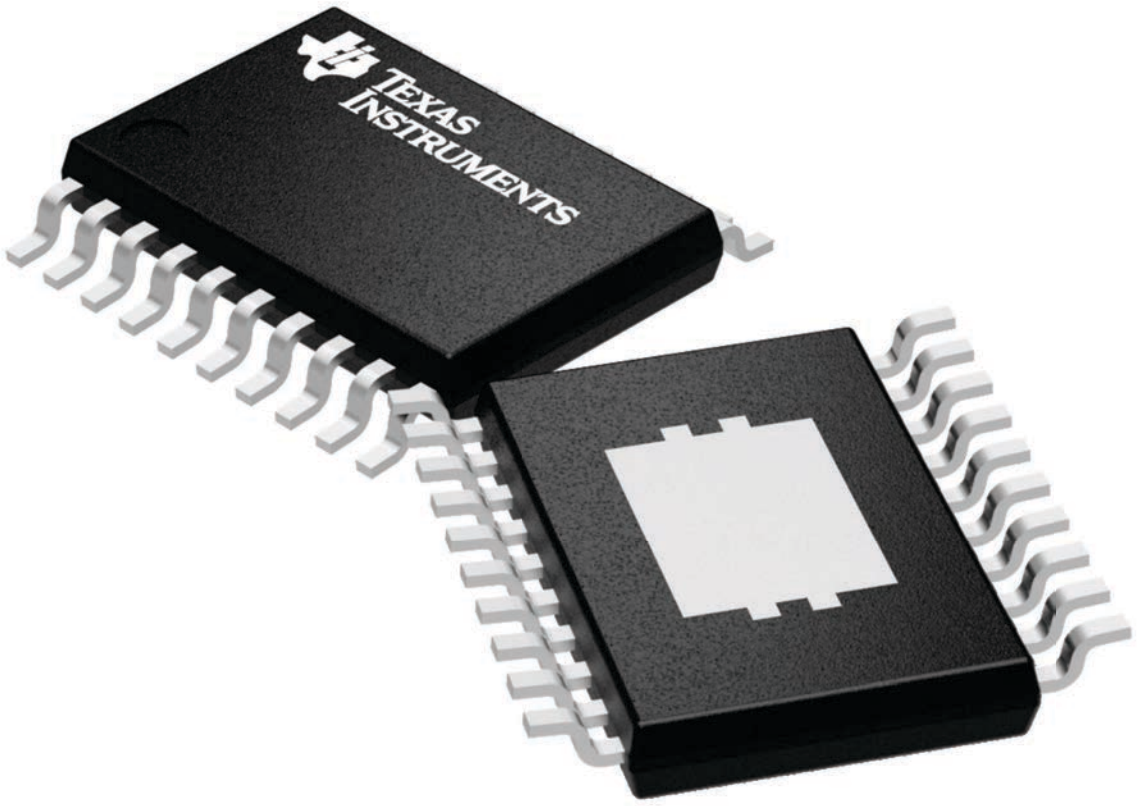
PWP 20

HTSSOP - 1.2 mm max height

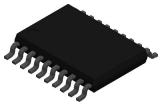
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

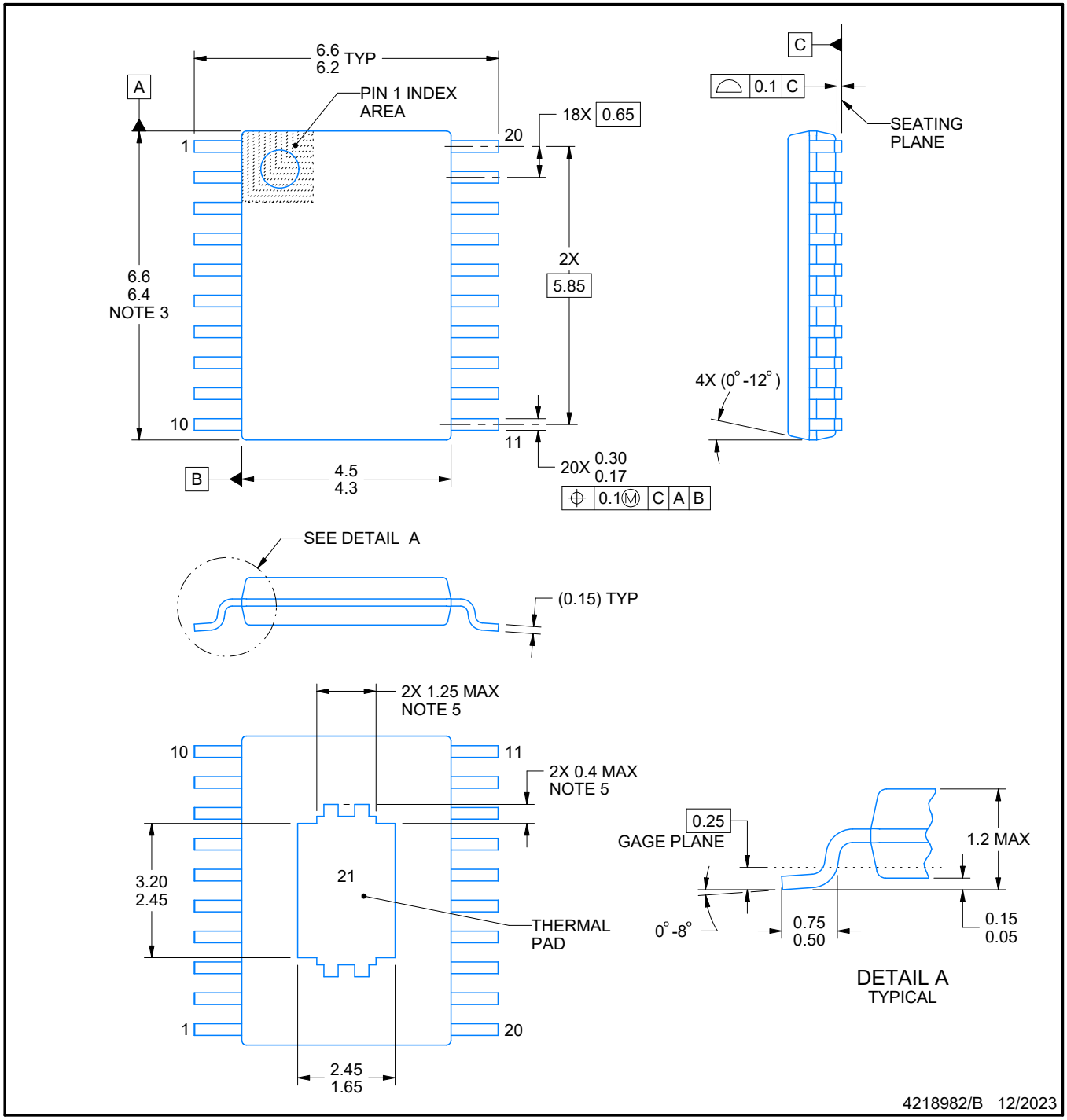


PACKAGE OUTLINE

PWP0020N

PowerPAD™ TSSOP - 1.2 mm max height

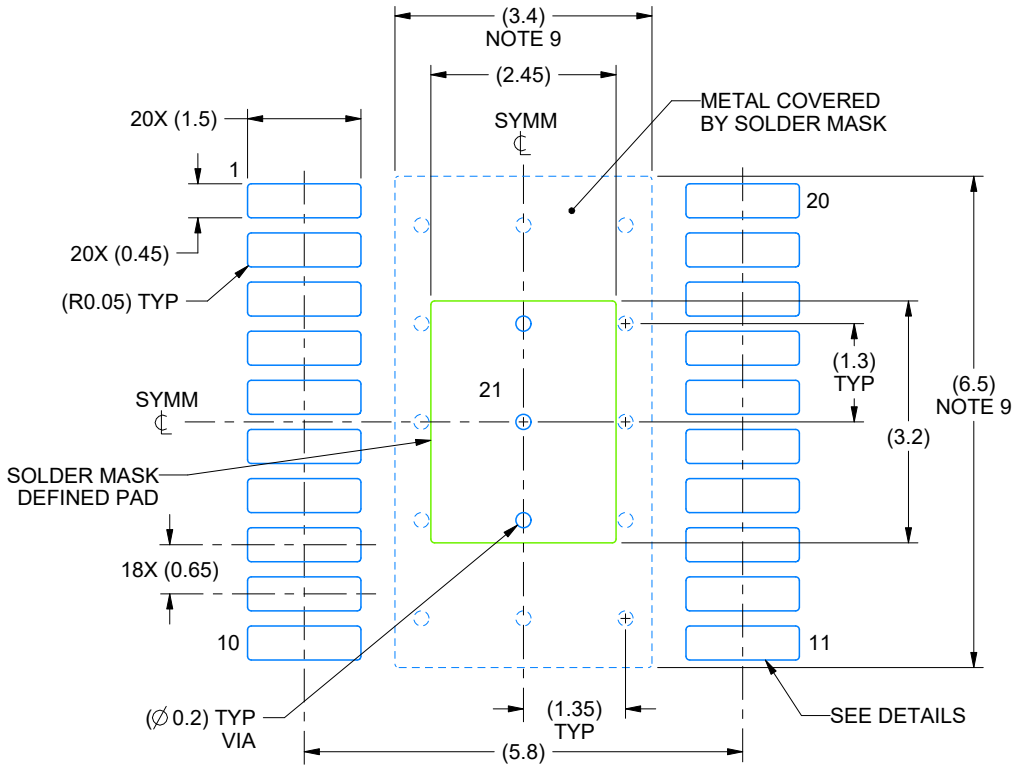
SMALL OUTLINE PACKAGE



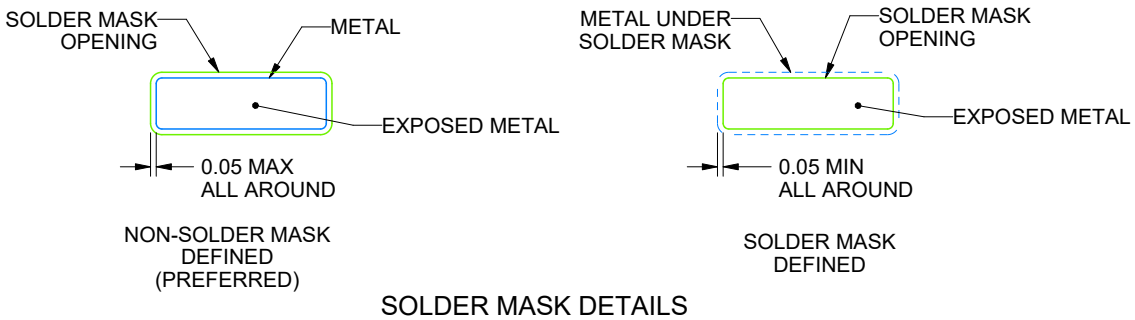
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

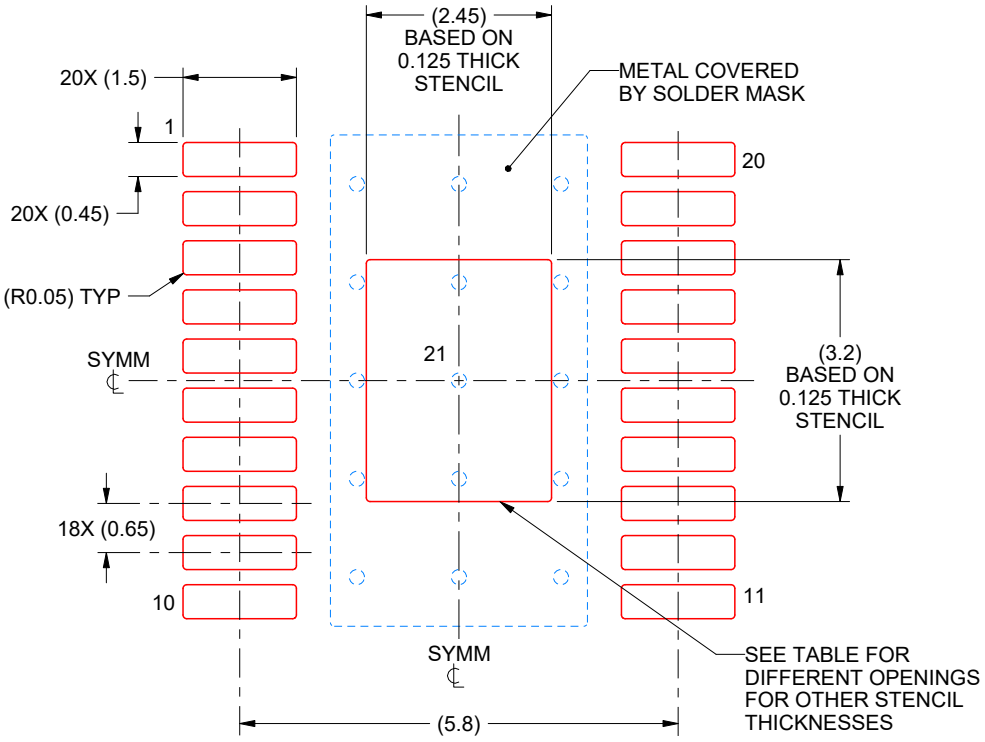


SOLDER MASK DETAILS

4218982/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.74 X 3.58
0.125	2.5 X 3.2 (SHOWN)
0.15	2.24 X 2.92
0.175	2.07 X 2.70

4218982/B 12/2023

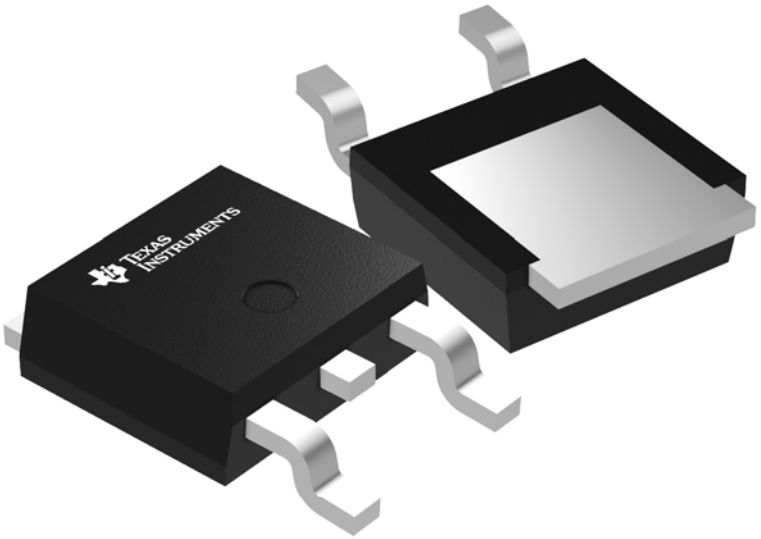
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



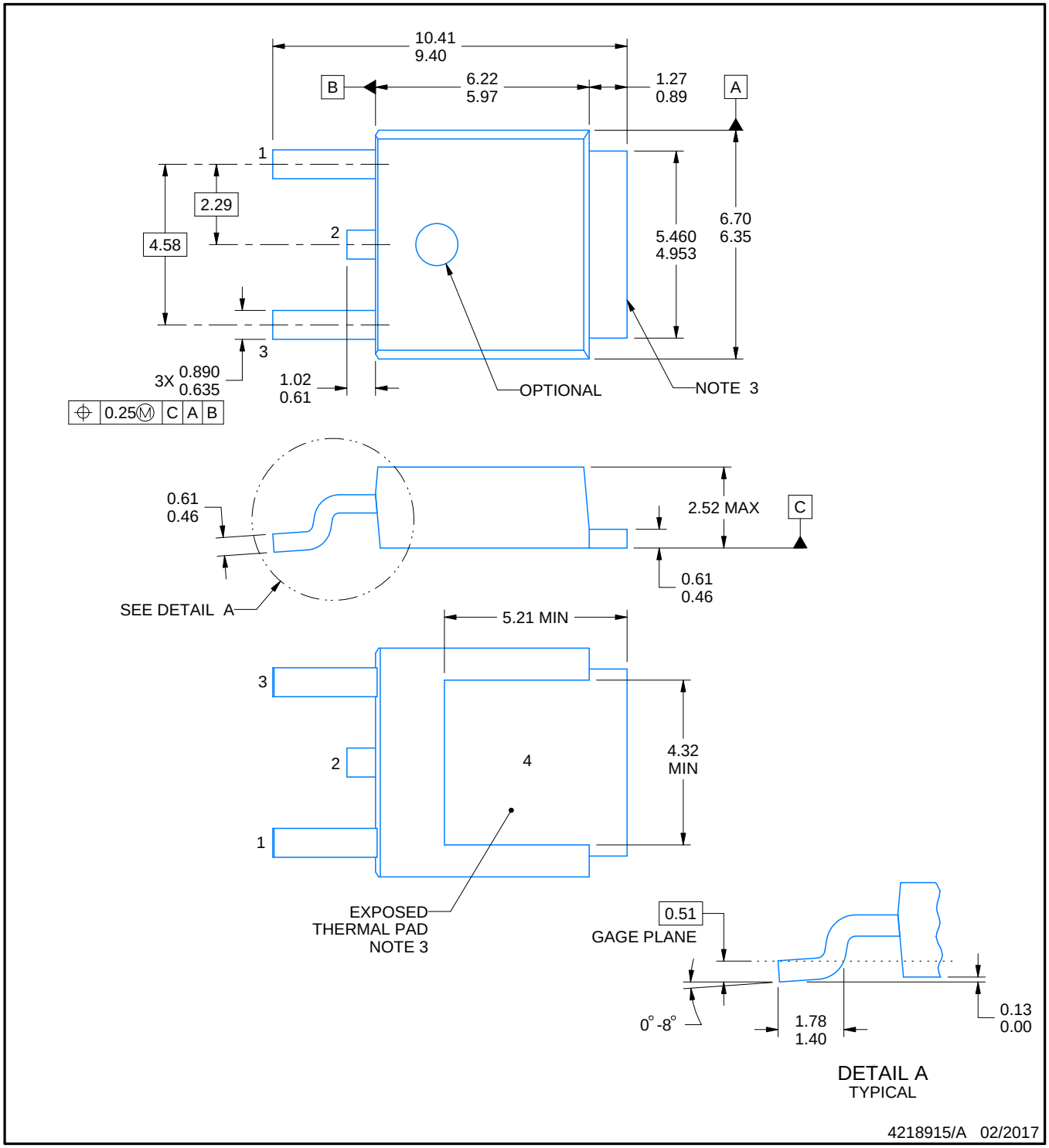
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

KVU0003A

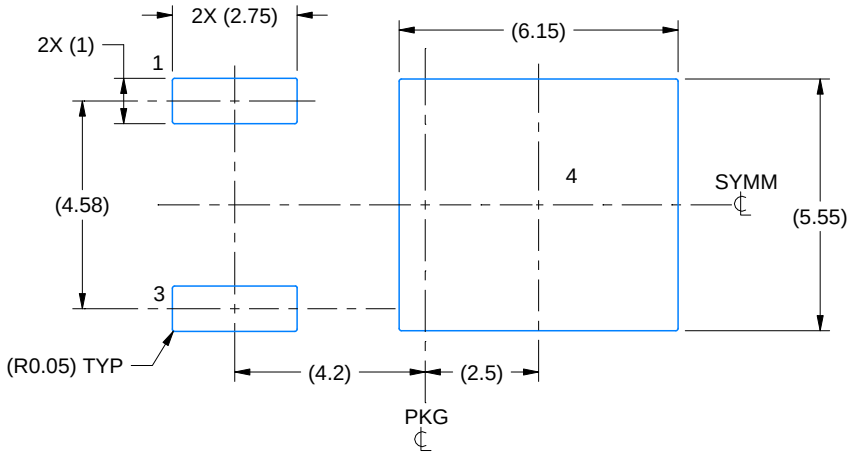
TO-252 - 2.52 mm max height

TO-252

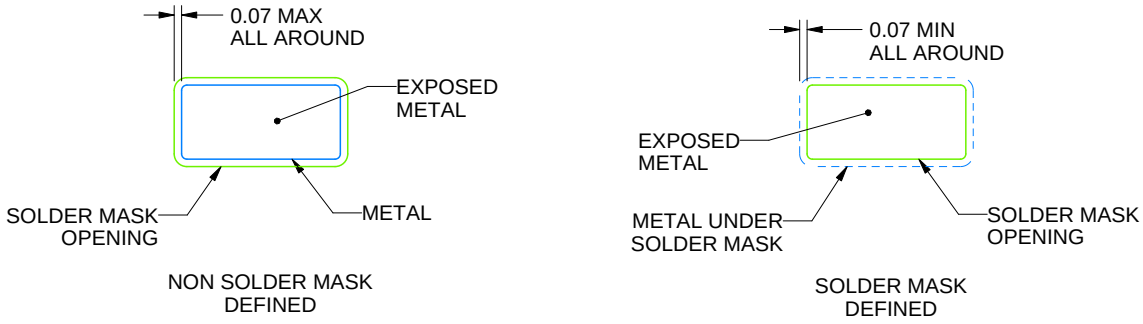


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

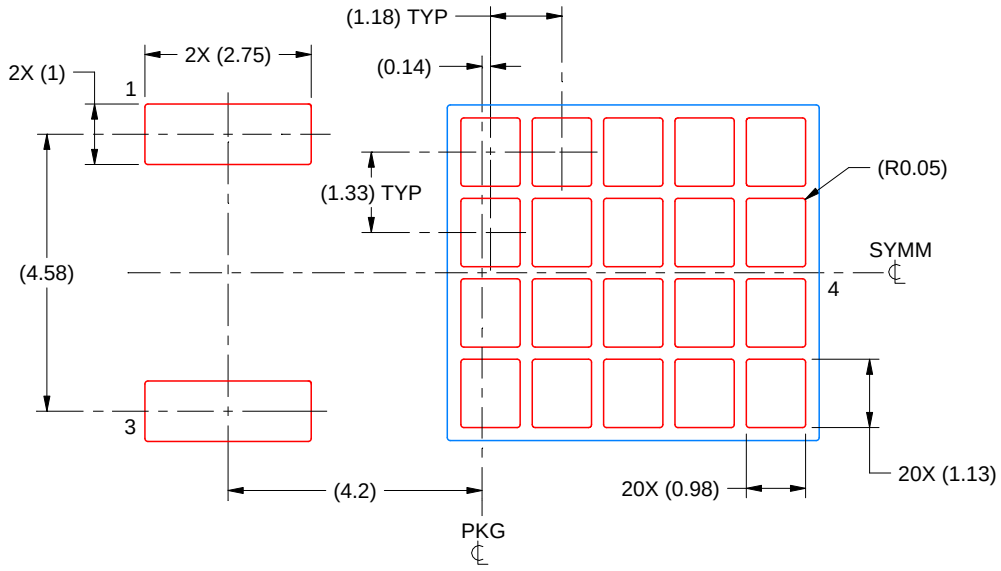
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

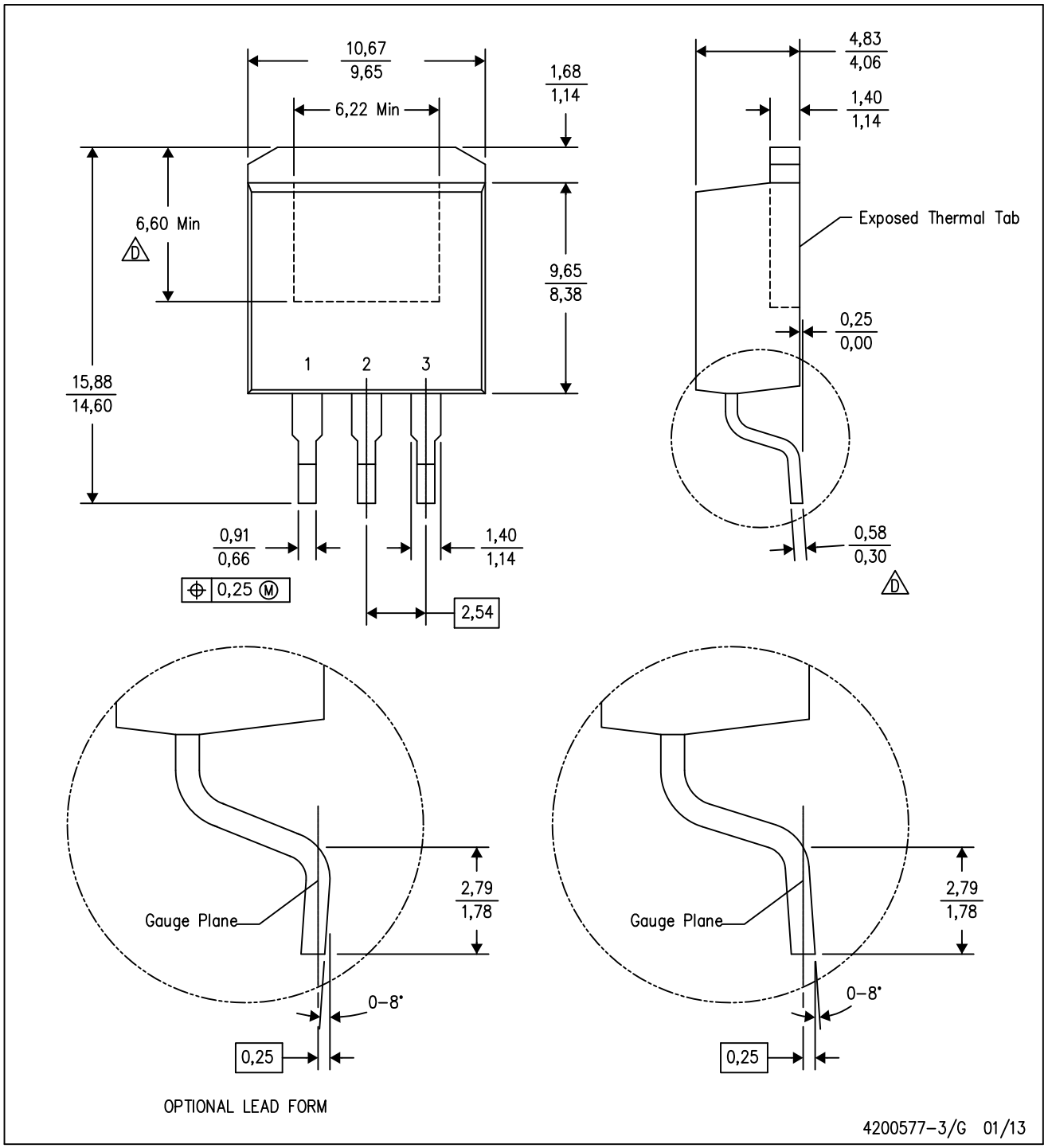
EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

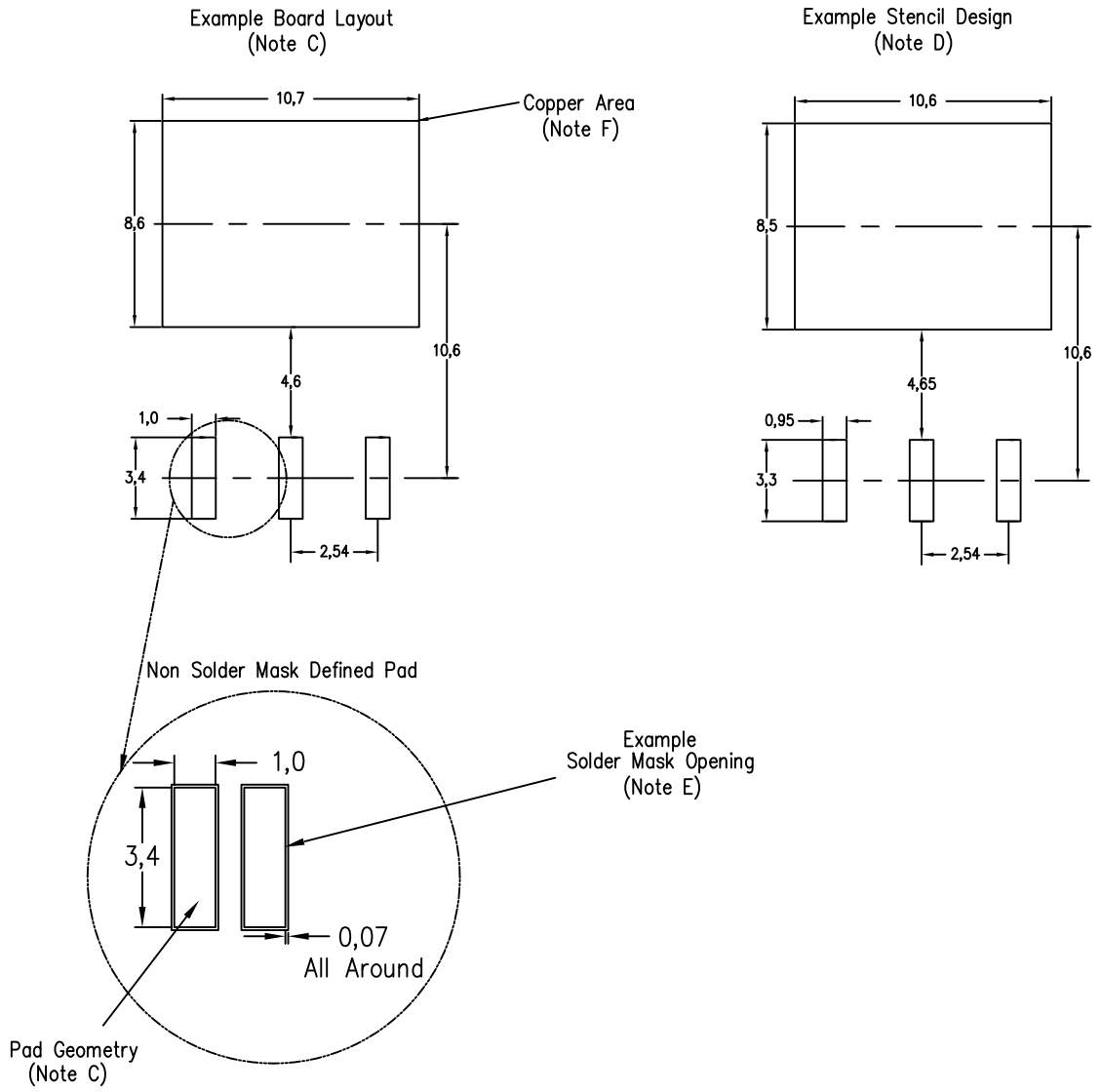
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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