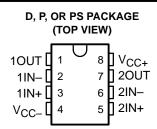
## TL4581 DUAL LOW-NOISE HIGH-DRIVE OPERATIONAL AMPLIFIER

SLVS457A - JANUARY 2003 - REVISED MARCH 2003

- Equivalent Input Noise Voltage
   5 nV/√Hz Typ at 1 kHz
- Unity-Gain Bandwidth . . . 10 MHz Typ
- High Slew Rate . . . 9 V/μs Typ
- Peak-to-Peak Output Voltage Swing
   32 V Typ, With V<sub>CC±</sub> = ±18 V and R<sub>L</sub> = 600 Ω
- Wide Supply-Voltage Range . . . ±3 V to ±20 V
- Common-Mode Rejection Ratio . . . 100 dB Typ
- High dc Voltage Gain . . . 100 V/mV Typ
- Applications: Audio PreAmps, Active Filters, Headphone Amps
- End Equipment: DVD/CD/CDRW Players;
   Set-Top Boxes



#### description/ordering information

The TL4581 is a dual operational amplifier that has been designed optimally for audio applications, such as improving tone control. It offers low noise, high-gain bandwidth, good slew, and high output current drive for driving capacitive loads. These features make the TL4581 ideally suited for audio applications, such as audio preamps and active filters. When high output current is required, the TL4581 also can be used as a headphone amplifier.

#### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – P	Tube of 50	TL4581P	TL4581P
0°C to 70°C	SOIC - D	Tube of 75	TL4581D	T4581
0 0 10 70 0	30IC - D	Reel of 2500		14361
	SOP – PS	Reel of 2000	TL4581PSR	T4581

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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# TL4581 DUAL LOW-NOISE HIGH-DRIVE OPERATIONAL AMPLIFIER

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V <sub>CC+</sub>		22 V
Input voltage, either input (see Notes 1 and 2)		V <sub>CC±</sub>
Input current (see Note 3)		±10 mA
Duration of output short circuit (see Note 4)		Unlimited
Operating virtual junction temperature, T <sub>J</sub>		150°C
Package thermal impedance, $\theta_{JA}$ (see Notes 5 and 6):	: D package	97°C/W
	P package	85°C/W
	PS package	95°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10	seconds	260°C
Storage temperature range, T <sub>stg</sub>		. −65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC-</sub>.

- 2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
- 3. Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
- 4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
- 5. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- 6. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions

		MIN	MAX	UNIT
V <sub>CC+</sub>	Supply voltage	5	15	V
VCC-	Supply voltage	<b>-</b> 5	-15	V
TA	Operating free-air temperature range	0	70	°C



## electrical characteristics, $V_{CC^{\pm}}$ = +15 V, $T_A$ = 25°C (unless otherwise noted)

	PARAMETER	TE	ST CONDITIONS		MIN	TYP	MAX	UNIT
\/	Input offset voltage	V <sub>O</sub> = 0	T <sub>A</sub> = 25°C			0.5	4	mV
VIO	input onset voltage	ΛQ = 0	$T_A = 0^{\circ}C$ to $70^{\circ}C$				5	IIIV
li a	Input offset current	T <sub>A</sub> = 25°C		10	150	nA		
lio	input onset current	$T_A = 0$ °C to $70$ °C	$T_A = 0$ °C to 70°C				200	ПА
I <sub>IB</sub>	Input bias current	T <sub>A</sub> = 25°C				200	800	nA
I JIR	input bias current	$T_A = 0^{\circ}C$ to $70^{\circ}C$					1000	ША
VICR	Common-mode input-voltage range				±12	±13		V
\/a==	Maximum peak-to-peak	R <sub>I</sub> ≥ 600 Ω	$V_{CC\pm} = \pm 15 \text{ V}$		24	26		٧
VOPP	output-voltage swing	KL 2 000 12	V <sub>CC±</sub> = ±18 V		30	32		V
		R <sub>L</sub> ≥ 600 Ω,	T <sub>A</sub> = 25°C		15	50		
۸ــ	Large-signal	$V_{O} = \pm 10 \text{ V}$	$T_A = 0$ °C to 70°C	10			V/mV	
AVD	differential-voltage amplification	$R_L \ge 2 \text{ k}\Omega$ , $T_A = 25^{\circ}\text{C}$			25	100		V/IIIV
		V <sub>O</sub> = ±10 V	$T_A = 0$ °C to 70°C		15			
A <sub>vd</sub>	Small-signal differential-voltage amplification	f = 10 kHz				2.2		V/mV
D	Maximum autout aving handwidth	R <sub>I</sub> = 600 Ω	V <sub>O</sub> = ±10 V			140		kHz
Вом	Maximum-output-swing bandwidth	K[ = 000 22	$V_{CC\pm} = \pm 18 \text{ V},$	V <sub>O</sub> = ±14 V		100		KΠZ
B <sub>1</sub>	Unity-gain bandwidth	$R_L = 600 \Omega$ ,	C <sub>L</sub> = 100 pF			10		MHz
rį	Input resistance				30	300		kΩ
z <sub>O</sub>	Output impedance	$A_{VD} = 30 \text{ dB},$	$R_L = 600 \Omega$ ,	f = 10 kHz		0.3		Ω
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICR</sub> min			70	100		dB
ksvr	Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	$V_{CC\pm} = \pm 9 \text{ V to } \pm$	15 V,	V <sub>O</sub> = 0	80	100		dB
los	Output short-circuit current				10	38	60	mA
ICC	Total supply curent	V <sub>O</sub> = 0,	No load			8	16	mA
	Crosstalk attenuation (VO1/VO2)	V <sub>01</sub> = 10 V peak,	f = 1 kHz			110		dB

<sup>†</sup> All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified.

## operating characteristics, $V_{CC\pm}$ = $\pm 15$ V, $T_A$ = $25^{\circ}C$

	PARAMETER	TEST CON	IDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain				9		V/μs
	Overshoot factor	$V_I$ = 100 mV, $R_L$ = 600 $\Omega$ ,	$A_{VD} = 1,$ $C_{L} = 100 \text{ pF}$		10		%
		f = 30 Hz			8		nV/√ <del>Hz</del>
V <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz			5		nv/vHz
In Equivalent input noise current		f = 30 Hz			2.7	, and the second	pA/√Hz
l'n	Equivalent input hoise current	f = 1 kHz			0.7	, and the second	p∧√√⊓Z

www.ti.com 11-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
TL4581D	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T4581
TL4581D.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T4581
TL4581DR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T4581
TL4581DR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T4581

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

### **PACKAGE MATERIALS INFORMATION**

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#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	U	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	` '	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL4581DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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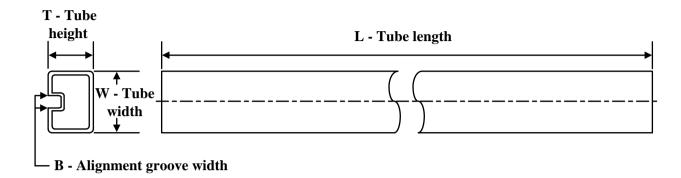
#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL4581DR	SOIC	D	8	2500	340.5	338.1	20.6

### **PACKAGE MATERIALS INFORMATION**

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#### **TUBE**



#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL4581D	D	SOIC	8	75	507	8	3940	4.32
TL4581D.A	D	SOIC	8	75	507	8	3940	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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