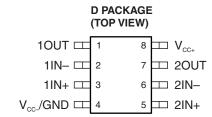


HIGH-SLEW-RATE SINGLE-SUPPLY OPERATIONAL AMPLIFIER

FEATURES

- Qualified for Automotive Applications
- Wide Gain-Bandwidth Product: 4 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.1%
- Wide-Range Single-Supply Operation:
 - 4 V to 36 V
- Wide Input Common-Mode Range Includes Ground (V_{CC}-)
- Low Total Harmonic Distortion: 0.02%

- Large-Capacitance Drive Capability: 10,000 pF
- Output Short-Circuit Protection



DESCRIPTION/ORDERING INFORMATION

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, $13\text{-V}/\mu s$ slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential (V_{CC-}). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

ORDERING INFORMATION(1)

T _A	PACK	AGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 125°C	SOIC - D	Reel of 2500	TL3472QDRQ1	T3472Q	

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

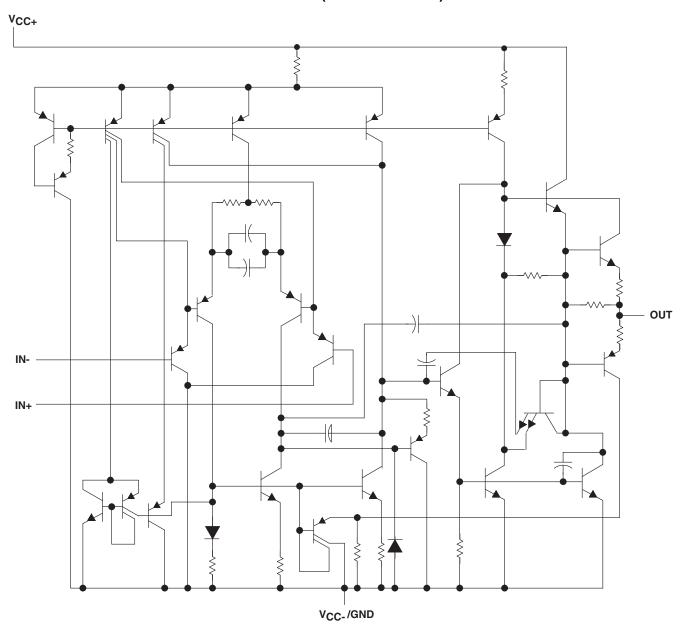


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

⁽²⁾ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



SCHEMATIC (EACH AMPLIFIER)





ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V _{CC+}	Supply voltage ⁽²⁾	18 V
V _{CC} -	Supply voltage -	-18 V
V_{ID}	Differential input voltage	±36 V
VI	Input voltage (any input)	V _{CC±}
II	Input current (each input)	±1 mA
Io	Output current	±80 mA
	Total current into V _{CC+}	80 mA
	Total current out of V _{CC}	80 mA
	Duration of short-circuit current at (or below) 25°C ⁽³⁾	Unlimited
θ_{JA}	Package thermal impedance ⁽⁴⁾⁽⁵⁾	97°C/W
TJ	Operating virtual junction temperature	150°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C
T _{stg}	Storage temperature range	−65°C to 150°C

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
$V_{\text{CC}\pm}$	Supply voltage		4	36	V
.,	Common mode input voltage	V _{CC} = 5 V	0	2.8	\/
V _{IC}	Common-mode input voltage	$V_{CC\pm} = \pm 15 \text{ V}$	-15	12.8	V
T_A	Operating free-air temperature	·	-40	125	°C

All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} . The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability. The package thermal impedance is calculated in accordance with JESD 51-7.



ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{CC\pm} = \pm 15 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDIT	T _A ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT		
			V _{CC} = 5 V	25°C		1.5	16		
V_{IO}	Input offset voltage	$V_{IC} = 0, V_{O} = 0, R_{S} = 50 \Omega$	V 45.V	25°C		1	17	mV	
			$V_{CC} = \pm 15 \text{ V}$	Full range			22		
α_{VIO}	Temperature coefficient of input offset voltage	$V_{IC} = 0, V_{O} = 0, R_{S} = 50 \Omega$	V _{CC} = ±15 V	Full range		10		μV/°C	
_	Input offset current	$V_{1C} = 0$, $V_{0} = 0$, $R_{s} = 50 \Omega$	$V_{CC} = \pm 15 \text{ V}$	25°C		6	75		
I _{IO}	input onset current	$V_{IC} = 0, V_{O} = 0, K_{S} = 50.12$	v _{CC} = ±15 v	Full range			300	nA	
-	lament bina annuant	V 0 V 0 D 50 0	V .45.V	25°C		100	500	^	
I _{IB}	Input bias current	$V_{IC} = 0, V_O = 0, R_S = 50 \Omega$ $V_{CC} = \pm 15 V$		Full range			700	nA	
V	Common-mode input	B 50.0		25°C		-15 to 12.8			
V _{ICR}	voltage range	$R_S = 50 \Omega$	Full range		-15 to 12.8		V		
		$V_{CC+} = 5 \text{ V}, V_{CC-} = 0, R_L = 2 \text{ kg}$	25°C	3.7	4		V		
V_{OH}	High-level output voltage	$R_L = 10 \text{ k}\Omega$	25°C	13.6	14				
		$R_L = 2 k\Omega$	Full range	13.4			ı		
		$V_{CC+} = 5 \text{ V}, V_{CC-} = 0, R_L = 2 \text{ kg}$	25°C		0.1	0.3			
V_{OL}	Low-level output voltage	$R_L = 10 \text{ k}\Omega$	25°C		-14.7	-14.3	V		
		$R_L = 2 k\Omega$	Full range			-13.5			
۸	Large-signal differential	V 40 V B 010		25°C	25	100) //> /	
A_{VD}	voltage amplification	$V_O = \pm 10 \text{ V}, R_L = 2 \text{ k}\Omega$	Full range	20			V/mV		
-	Short-circuit	Source: VID = 1 V, V _O = 0		2500	-10	-34		A	
los	output current	Sink: $VID = -1 V$, $V_O = 0$	25°C	20	27		mA		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}(min), R_S = 50 \Omega$	25°C	65	97		dB		
k _{SVR}	Supply-voltage rejection ratio $(\Delta V_{CC} \pm /\Delta V_{IO})$	$V_{CC\pm} = \pm 13.5 \text{ V to } \pm 16.5 \text{ V, R}_{S}$	25°C	70	97		dB		
	_	O. No local		25°C		3.5	4.5	_	
I_{CC}	Supply current (per channel)	$V_O = 0$, No load	Full range		4.5	5.5			
	(por orialino)	V _{CC+} = 5 V, V _O = 2.5 V, V _{CC-} =	25°C		3.5	4.5			

⁽¹⁾ Full range $T_A = -40^{\circ}\text{C}$ to 125°C (2) All typical values are at $T_A = 25^{\circ}\text{C}$.



OPERATING CHARACTERISTICS

 $V_{CC\pm} = \pm 15 \text{ V}, T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITI	TEST CONDITIONS				
SR+	Positive slew rate	$V_I = -10$ V to 10 V, $R_L = 2$ k Ω , $C_L = 300$ pF	A _V = 1	8	10		V/μs
SR-	Negative slew rate	$V_I = -10 \text{ V to } 10 \text{ V}, \text{ R}_L = 2 \text{ k}\Omega,$ $C_L = 300 \text{ pF}$	A _V = -1		13		V/μs
	Cottling time	A 4.40 V stop	To 0.1%		1.1		
ts	Settling time	$A_{VD} = -1$, 10-V step	To 0.01%		2.2		μs
V _n	Equivalent input noise voltage	$f = 1 \text{ kHz}, R_S = 100 \Omega$	·		49		nV/√ Hz
In	Equivalent input noise current	f = 1 kHz	f = 1 kHz				pA/√ Hz
THD	Total harmonic distortion	$V_{O(PP)} = 2 \text{ V to } 20 \text{ V}, R_L = 2 \text{ k}\Omega, A$		0.02		%	
GBW	Gain-bandwidth product	f =100 kHz	3	4		MHz	
BW	Power bandwidth	$V_{O(PP)} = 20 \text{ V}, R_L = 2 \text{ k}\Omega, A_{VD} = 1$, THD = 5.0%		160		kHz
4	Phone margin	B = 2 kO	C _L = 0		70		dog
φ _m	Phase margin	$R_L = 2 k\Omega$	$C_L = 300 pF$		50		deg
	Cain marain	B 210	C _L = 0		12		dB
	Gain margin	$R_L = 2 k\Omega$	C _L = 300 pF		4		uБ
r _i	Differential input resistance	V _{IC} = 0		150		ΜΩ	
C _i Input capacitance		V _{IC} = 0		2.5		pF	
	Channel separation f = 10 kHz			101		dB	
Z _O	Open-loop output impedance	f = 1 MHz, A _V = 1		20		Ω	

www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TL3472QDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3472Q
TL3472QDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3472Q

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL3472-Q1:

Catalog: TL3472

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

NOTE: Qualified Version Definitions:

 $_{\bullet}$ Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	U	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3472QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025



*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	TL3472QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0	



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025