SLOS200G - OCTOBER 1997 - REVISED JULY 2003

- Wide Gain-Bandwidth Product . . . 4 MHz
- High Slew Rate . . . 13 V/μs
- Fast Settling Time . . . 1.1 μs to 0.1%
- Wide-Range Single-Supply Operation . . . 4 V to 36 V
- Wide Input Common-Mode Range Includes Ground (V<sub>CC</sub>)
- Output Short-Circuit Protection



# 10UT [ 1 8 ] V<sub>CC+</sub> 1IN-[ 2 7 ] 20UT 1IN+[ 3 6 ] 2INV<sub>CC</sub>\_/GND [ 4 5 ] 2IN+

## description/ordering information

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product,  $13\text{-V}/\mu s$  slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential ( $V_{CC-}$ ). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

#### ORDERING INFORMATION

T <sub>A</sub>	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP (P)	Tube of 25	TL3472CP	TL3472CP	
0°C to 70°C	0010 (D)	Tube of 50	TL3472CD	0.4700	
	SOIC (D)	Reel of 2500	TL3472CDR	3472C	
	PDIP (P)	Tube of 25	TL3472IP	TL3472IP	
–40°C to 105°C	COIC (D)	Tube of 50	TL3472ID	70470	
	SOIC (D)	Reel of 2500	TL3472IDR	Z3472	

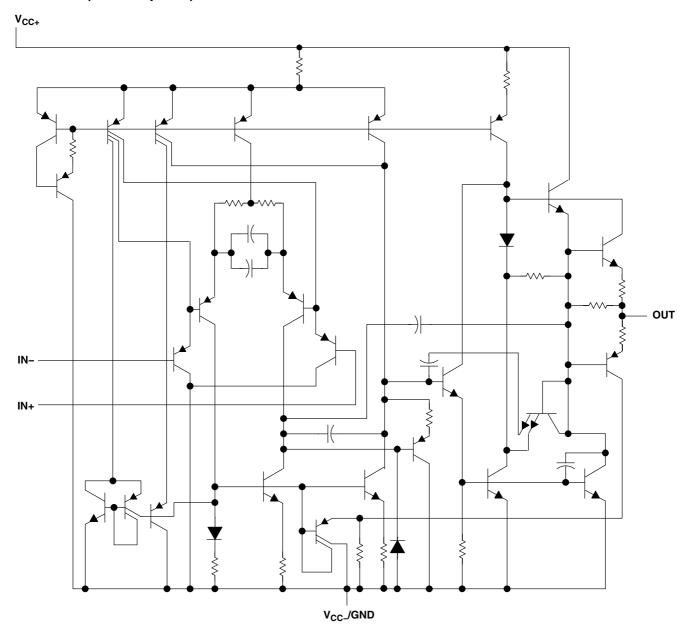
<sup>&</sup>lt;sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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# schematic (each amplifier)



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

18 V
18 V
36 V
√ <sub>CC±</sub>
l mA
) mA
) mA
) mA
nited
C/W
C/W
50°C
30°C
50°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC-}$  and  $V_{CC-}$ .

- 2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than V<sub>CC</sub> 0.3 V.
- 3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
- 4. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can impact reliability.
- 5. The package thermal impedance is calculated in accordance with JESD 51-7.

# recommended operating conditions

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		4	36	٧
	V <sub>CC</sub> = 5		0	2.8	
$V_{IC}$	Common-mode input voltage	$V_{CC\pm} = \pm 15 \text{ V}$	-15	12.8	V
_	Operating free air temperature	TL3472C	0	70	°C
T <sub>A</sub>	Operating free-air temperature	-40	105	C	

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# electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = $\pm 15$ V (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	T <sub>A</sub>	MIN	TYP†	MAX	UNIT		
			$V_{CC} = 5 V$		25°C		1.5	10		
V <sub>IO</sub>	Input offset voltage		V <sub>CC</sub> = ±15 V		25°C		1.0	10	mV	
					Full range <sup>‡</sup>			12		
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	$V_{IC} = 0,$ $V_{O} = 0,$	$V_{CC} = \pm 15$	/	Full range <sup>‡</sup>		10		μV/°C	
	land the state of	$R_S = 50 \Omega$	V 145.	,	25°C		6	75	4	
I <sub>IO</sub>	Input offset current		$V_{CC} = \pm 15$	/	Full range <sup>‡</sup>			300	nA	
	lanced bina accurant		V 145.	,	25°C		100	500	4	
I <sub>IB</sub>	Input bias current		$V_{CC} = \pm 15$	/	Full range <sup>‡</sup>			700	nA	
Common-mode		B 50.0	•				–15 to 12.8		,	
V <sub>ICR</sub> input voltage range	$R_S = 50 \Omega$			Full range <sup>‡</sup>		–15 to 12.8		V		
		$V_{CC+} = 5 V$ ,	$V_{CC-} = 0$ ,	$R_L = 2 k\Omega$	25°C	3.7	4			
V <sub>OH</sub>	High-level output voltage	$R_L = 10 \text{ k}\Omega$		25°C	13.6	14		V		
		$R_L = 2 k\Omega$		Full range <sup>‡</sup>	13.4					
		$V_{CC+} = 5 V$ ,	$V_{CC-} = 0$ ,	$R_L = 2 k\Omega$	25°C		0.1	0.3		
V <sub>OL</sub>	Low-level output voltage	$R_L = 10 \text{ k}\Omega$		25°C		-14.7	-14.3	V		
		$R_L = 2 k\Omega$			Full range <sup>‡</sup>			-13.5		
_	Large-signal differential	V 140 V	D OLO		25°C	25	100		\//ma\/	
A <sub>VD</sub>	voltage amplification	$V_{O} = \pm 10 \text{ V},$	$R_L = 2 k\Omega$		Full range <sup>‡</sup>	20			V/mV	
	Ob ant almost as desire as mount	Source: V <sub>ID</sub> = 1 V,	$V_O = 0$		0500	-10	-34			
los	Short-circuit output current	Sink: $V_{ID} = -1 V$ ,	$V_O = 0$		25°C	20	27		mA	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}(min),$	$R_S = 50 \Omega$		25°C	65	97		dB	
k <sub>SVR</sub>	Supply-voltage rejection ratio $(\Delta V_{CC\pm}\!/\!\Delta V_{IO})$	$V_{CC\pm} = \pm 13.5 \text{ V to } \pm$	16.5 V,	R <sub>S</sub> = 100 Ω	25°C	70	97		dB	
			No lood		25°C		3.5	4.5		
I <sub>CC</sub>	Supply current (per channel)	$V_O = 0$ ,	No load		Full range <sup>‡</sup>		4.5	5.5	mA	
		$V_{CC+} = 5 \text{ V}, V_O = 2.5$	$5 \text{ V}, V_{\text{CC}-} = 0,$	No load	25°C		3.5	4.5		

<sup>†</sup> All typical values are at T<sub>A</sub> = 25°C. ‡ Full range is 0°C to 70°C for the TL3472C device and -40°C to 105°C for the TL3472I device.

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# operating characteristics, $V_{CC^\pm}$ = $\pm 15$ V, $T_A$ = $25^{\circ}C$

	PARAMETER	TEST CO	ONDITIONS	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$V_I = -10 \text{ V to } 10 \text{ V},$	A <sub>V</sub> = 1	8	10		V/μs
SR-	Negative slew rate	$R_L = 2 \text{ k}\Omega, C_L = 300 \text{ pF}$	$A_V = -1$		13		V/μs
	O a Million at Manage	A 40 V stan	To 0.1%		1.1		_
t <sub>s</sub>	Settling time	$A_{VD} = -1$ , 10-V step	To 0.01%		2.2		μs
V <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz,	$R_S = 100 \Omega$		49		nV/√ <del>Hz</del>
In	Equivalent input noise current	f = 1 kHz			0.22		pA/√ <del>Hz</del>
THD	Total harmonic distortion	$V_{O(PP)} = 2 \text{ V to } 20 \text{ V}, R_L = 2$	$V_{O(PP)} = 2 \text{ V to } 20 \text{ V}, R_L = 2 \text{ k}\Omega, A_{VD} = 10, f = 10 \text{ kHz}$				
GBW	Gain-bandwidth product	f =100 kHz	f =100 kHz				
BW	Power bandwidth	$V_{O(PP)} = 20 \text{ V}, R_L = 2 \text{ k}\Omega, A_V$	<sub>D</sub> = 1, THD = 5.0%		160		kHz
		<b>D</b> 010	C <sub>L</sub> = 0		70		
φm	Phase margin	$R_L = 2 k\Omega$	C <sub>L</sub> = 300 pF	50			deg
	Only assessed	<b>D</b> 010	C <sub>L</sub> = 0		12		-10
	Gain margin	$R_L = 2 k\Omega$	C <sub>L</sub> = 300 pF	4			dB
rį	Differential input resistance	V <sub>IC</sub> = 0			150		MΩ
Ci	Input capacitance	V <sub>IC</sub> = 0			2.5		pF
	Channel separation	f = 10 kHz		101		dB	
z <sub>o</sub>	Open-loop output impedance	f = 1 MHz,	A <sub>V</sub> = 1		20	_	Ω

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TL3472CDR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3472C
TL3472CDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3472C
TL3472CP	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3472CP
TL3472CP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3472CP
TL3472IDR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3472
TL3472IDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3472
TL3472IP	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3472IP
TL3472IP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3472IP

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# PACKAGE OPTION ADDENDUM

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF TL3472:

Automotive : TL3472-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ı	TL3472CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
L	TL3472IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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## \*All dimensions are nominal

Device	Package Type Package Drawing		Pins SPQ		Length (mm)	Width (mm)	Height (mm)	
TL3472CDR	SOIC	D	8	2500	353.0	353.0	32.0	
TL3472IDR	SOIC	D	8	2500	353.0	353.0	32.0	

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



## \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL3472CP	Р	PDIP	8	50	506	13.97	11230	4.32
TL3472CP.A	Р	PDIP	8	50	506	13.97	11230	4.32
TL3472IP	Р	PDIP	8	50	506	13.97	11230	4.32
TL3472IP.A	Р	PDIP	8	50	506	13.97	11230	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



# P (R-PDIP-T8)

# PLASTIC DUAL-IN-LINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



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