











SLVS004I - APRIL 1979-REVISED AUGUST 2016

TL317

TL317 100-mA 3-Terminal Adjustable Positive Voltage Regulator

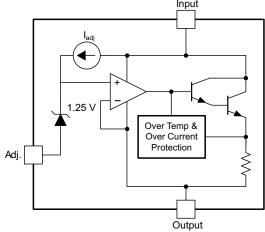
Features

- Output Voltage Range Adjustable From 1.25 V to 32 V When Used With an External Resistor Divider
- Output Current Capability of 100 mA
- Input Regulation Typically 0.01% Per Input-Voltage Change
- Output Regulation Typically 0.5%
- Ripple Rejection Typically 80 dB

Applications

- **Power Supplies**
- Portable Devices
- Computing and Servers
- **Telecommunications**
- HVAC: Heating, Ventilation, and Air Conditioning
- Desktop PC
- Digital Signage
- Programmable Logic Controller
- **Appliances**

Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

3 Description

The TL317 is an adjustable three-terminal positivevoltage regulator capable of supplying 100 mA over an output-voltage range of 1.25 V to 32 V. It is exceptionally easy to use and requires only two external resistors to set the output voltage.

This regulator offers full overload protection available only in integrated circuits. Included on the chip are current-limiting and thermal-overload protection. All overload-protection circuitry remains fully functional, even when ADJUSTMENT is disconnected. Normally, no capacitors are required unless the device is situated far from the input filter capacitors, in which case an input bypass is required. An optional output capacitor can be added to improve transient response. ADJUSTMENT can be bypassed to achieve very high ripple rejection.

In addition to replacing fixed regulators, the TL317 regulator is useful in a wide variety of other applications. Because the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. Its primary application is that of a programmable output regulator, but by connecting a fixed resistor between ADJUSTMENT and OUTPUT, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping ADJUSTMENT to ground, programming the output to 1.25 V, where most loads draw little current.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL317D	SOIC (8)	4.90 mm × 3.90 mm
TL317PW	TSSOP (8)	4.30 mm × 3.00 mm
TL317PS	SOP (8)	6.20 mm × 5.30 mm
TL317LP	TO-92 (3)	4.83 mm × 3.68 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Table of Contents

1	Features 1	7.4 Device Functional Modes
2	Applications 1	8 Application and Implementation
3	Description 1	8.1 Application Information
4	Revision History2	8.2 Typical Applications
5	Pin Configuration and Functions3	9 Power Supply Recommendations 13
6	Specifications4	10 Layout 13
	6.1 Absolute Maximum Ratings 4	10.1 Layout Guidelines1
	6.2 ESD Ratings	10.2 Layout Example1
	6.3 Recommended Operating Conditions 4	11 Device and Documentation Support 14
	6.4 Thermal Information	11.1 Receiving Notification of Documentation Updates 14
	6.5 Electrical Characteristics5	11.2 Community Resources14
	6.6 Typical Characteristic5	11.3 Trademarks 1
7	Detailed Description 6	11.4 Electrostatic Discharge Caution 14
	7.1 Overview	11.5 Glossary14
	7.2 Functional Block Diagrams	12 Mechanical, Packaging, and Orderable
	7.3 Feature Description	Information 14

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (September 2011) to Revision I

Page

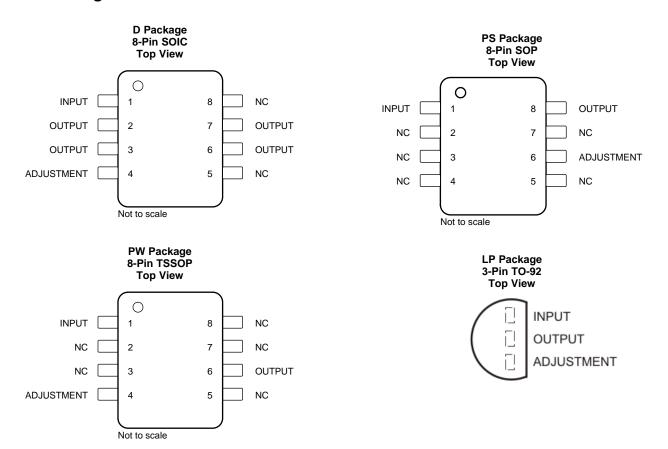
Changes from Revision G (September 2009) to Revision H

Page

- Changed datasheet format from QuickSilver to DocZone
 Changed low end output voltage range from 1.2 V to 1.25



5 Pin Configuration and Functions



Pin Functions

		PIN		NO DECODIDEION					
NAME	SOIC	TSSOP	SOP	TO-92	I/O	DESCRIPTION			
ADJUSTMENT	4	4	6	3	_	Supply reference voltage			
INPUT	1	1	1	1	I	Input supply voltage			
NC	5, 8	2, 3, 5, 7, 8	2, 3, 4, 5, 7	_	_	No internal connection			
OUTPUT	2, 3, 6, 7	6	8	2	0	Output voltage, output terminals are all internally connected.			

Copyright © 1979–2016, Texas Instruments Incorporated



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Input-to-output differential voltage, V _I – V _O		35	V
Operating virtual-junction temperature, T _J		150	°C
Storage temperature range, T _{stg}	-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
\/	Floatroatatia diaabaraa	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	\/
V _{(ES}	D) Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000 ⁽³⁾	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- (3) Tested on PW package.

6.3 Recommended Operating Conditions

			MIN	NOM MAX	UNIT
$V_I - V_O$	Input-to-output voltage differential		2.5	35	V
Io	Output current		2.5	100	mA
_	Operating virtual impation temperature	TL317C	0	125	ŝ
IJ	Operating virtual-junction temperature	TL317	-40	125	°C

6.4 Thermal Information

			TL3	317		
	THERMAL METRIC ⁽¹⁾	D (SOIC)	PW (TSSOP)	PS (SOP)	LP (TO-92)	UNIT
		8 PINS	8 PINS	8 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.9	170	115.3	157.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	51	67.1	81.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.5	101.5	64.4	_	°C/W
ΨЈТ	Junction-to-top characterization parameter	12.5	3.7	27.7	25.4	°C/W
ΨЈВ	Junction-to-board characterization parameter	57.9	99.1	63.5	137.1	°C/W

 For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Product Folder Links: TL317



6.5 Electrical Characteristics

over recommended operating virtual-junction temperature range (unless otherwise noted)(1)

PARAMETER	TEST CO	ONDITIONS	MIN	TYP	MAX	UNIT
Input voltage regulation (2)	\\ \\ - \E\\ to 2\E\\	T _J = 25°C		0.01%	0.02%	V
Input voltage regulation (2)	$V_1 - V_0 = 5 \text{ V to } 35 \text{ V}$	$I_O = 2.5 \text{ mA to } 100 \text{ mA}$		0.02%	0.05%	V
	V _O = 10 V, f = 120 Hz			65		
Ripple regulation	V _O = 10 V, 10-μF capacitor between ADJUSTMENT and grou		66	80		dB
	$V_1 = 5 V \text{ to } 35 V,$	V _O ≤ 5 V		25		mV
Output voltage regulation	$I_O = 2.5 \text{ mA to } 100 \text{ mA},$ $T_J = 25^{\circ}\text{C}$	V _O ≥ 5 V		5		mV/V
Catput Voltage Togalation	$V_1 = 5 \text{ V to } 35 \text{ V},$	V _O ≤ 5		50		mV
	$I_0 = 2.5 \text{ mA to } 100 \text{ mA}$	V _O ≥ 5 V		10		mV/V
Output voltage change with temperature	$T_J = 0$ °C to 125°C			10		mV/V
Output voltage long-term drift	After 1000 hours at T _J =	125°C and V _I – V _O = 35 V		3	10	mV/V
Output noise voltage	$f = 10 Hz$ to 10 kHz, $T_J =$	25°C		30		μV/V
Minimum output current to maintain regulation	$V_I - V_O = 35$			1.5	2.5	mA
Peak output current	$V_I - V_O \le 35 \text{ V}$		100	200		mA
ADJUSTMENT current				50	100	μΑ
Change in ADJUSTMENT current	$V_I - V_O = 2.5 \text{ V to } 35 \text{ V, I}$	O = 2.5 mA to 100 mA		0.2	5	μΑ
Reference voltage (output to ADJUSTMENT)	I _O = 2.5 mA to 100 mA, \P ≤ rated dissipation	$V_1 - V_0 = 5 \text{ V to } 35 \text{ V},$	1.2	1.25	1.3	V

⁽¹⁾ Unless otherwise noted, these specifications apply for the following test conditions: V_I – V_O = 5 V and I_O = 40 mA. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a 0.1-μF capacitor across the input and a 1-μF capacitor across the output.

6.6 Typical Characteristic

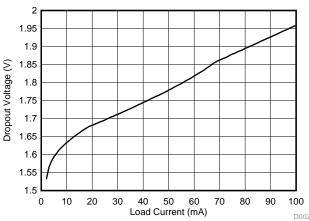


Figure 1. Dropout Voltage vs Load Current (T_J = 25°C)

⁽²⁾ Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

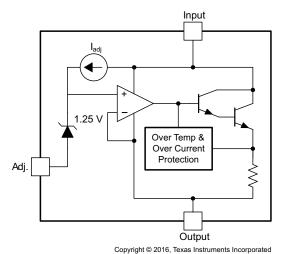


7 Detailed Description

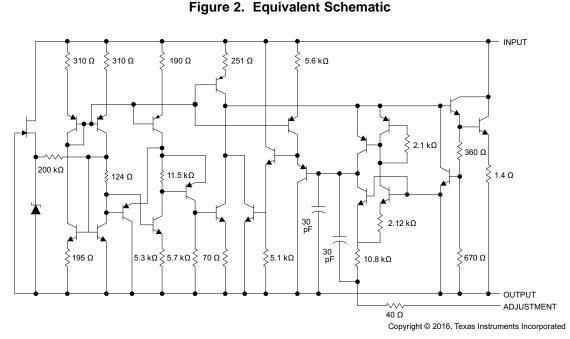
7.1 Overview

The TL317 device is an adjustable three-terminal positive-voltage regulator capable of supplying up to 100 mA over an output-voltage range of 1.25 V to 32 V. It requires only two external resistors to set the output voltage. The TL317 device is versatile in its applications, including uses in programmable output regulation and local oncard regulation. Also, by connecting a fixed resistor between the ADJUSTMENT and OUTPUT terminals, the TL317 device can function as a precision current regulator. An optional output capacitor can be added to improve transient response. The ADJUSTMENT terminal can be bypassed to achieve very high ripple-rejection ratios, which are difficult to achieve with standard three-terminal regulators.

7.2 Functional Block Diagrams



.,, 5



All component values shown are nominal

Figure 3. Detailed Schematic



7.3 Feature Description

7.3.1 NPN Darlington Output Drive

NPN Darlington output topology provides naturally low output impedance and an output capacitor is optional.

7.3.2 Programmable Feedback

An internal amplifier with 1.25-V offset input at the ADJUSTMENT terminal provides easy output voltage or current (not both) programming. For current regulation applications, a single resistor whose resistance value is $1.25 \text{ V} / I_0$ and power rating is greater than $(1.25 \text{ V})^2 / R$ must be used. For voltage regulation applications, two resistors set the output voltage as described in *Adjustable Voltage Regulator*.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device OUTPUT pin sources current necessary to make the OUTPUT pin 1.25 V greater than the ADJUSTMENT pin to provide output regulation

7.4.2 Operation With Low Input Voltage

The device requires 2.5 V of headroom (VI - VO) to regulate the OUTPUT. With less headroom, the OUTPUT voltage of the device may be below the desired setpoint.

7.4.3 Operation in Light Loads

The device passes its bias current to the OUTPUT pin. The load or feedback must consume this minimum current for regulation or the output may be too high. The minimum current require to regulate is provided in the *Electrical Characteristics*, so the series resistance used to set the output voltage is recommended to be $V_{\rm O}$ / $I_{\rm MIN}$ to ensure regulation at all times.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The flexibility of the TL317 allows it to be configured to take on many different functions in DC power applications.

8.2 Typical Applications

8.2.1 Adjustable Voltage Regulator

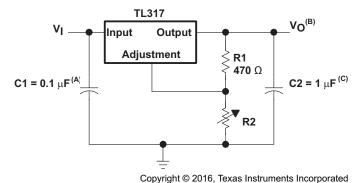


Figure 4. Adjustable Voltage Regulator

8.2.1.1 Design Requirements

- R1 and R2 are required to set the output voltage.
- C1 is recommended, particularly if the regulator is not in close proximity to the power-supply filter capacitors. A 0.1-µF ceramic or 1-µF tantalum capacitor provides sufficient bypassing for most applications, especially when adjustment and output capacitors are used.
- Use of an output capacitor, C2, improves transient response, but is optional.

8.2.1.2 Detailed Design Procedure

V_O is calculated as shown in Equation 1. I_{ADJ} is typically 50 μA and negligible in most applications.

Power dissipation for linear regulators is calculated as shown in Equation 2. I_{ADJ} is typically 50 μA and negligible in most applications, so a typical way to calculate power dissipation for linear regulators is simplified to Equation 3.

$$V_O = V_{REF} (1 + R2 / R1) + (I_{ADJ} \times R2)$$
 (1)

$$P = (V_1 - V_0) \times I_0 + (V_1 - V_{AD,J}) \times I_{AD,J}$$
 (2)

$$P = (V_1 - V_0) \times I_0 \tag{3}$$



8.2.1.3 Application Curve

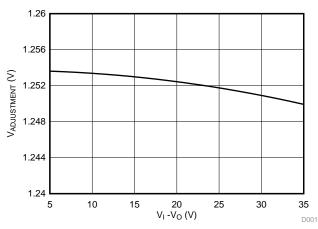


Figure 5. Line Regulation

8.2.2 0-V to 30-V Regulator Circuit

 V_{O} is calculated as shown in Equation 4, where V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages (approximately 1.25 V).

Copyright © 2016, Texas Instruments Incorporated

Figure 6. 0-V to 30-V Regulator Circuit Schematic

Copyright © 1979–2016, Texas Instruments Incorporated



8.2.3 Regulator Circuit With Improved Ripple Rejection

- Protection diode D1 is recommended if C2 is used. The diode provides a low-impedance discharge path to
 prevent the capacitor from discharging into the output of the regulator
- Use of an output capacitor, C2, improves transient response, but is optional.

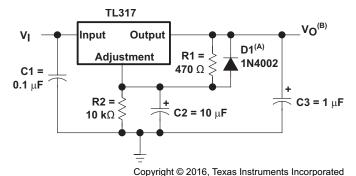


Figure 7. Regulator Circuit With Improved Ripple Rejection Schematic

8.2.4 Precision Current-Limiter Circuit

The use of the TL317 in this configuration limits the output current to I_{limit} shown in Figure 8.

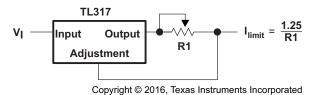


Figure 8. Precision Current-Limiter Circuit

8.2.5 Tracking Preregulator Circuit

This application keeps a constant voltage across the second TL317 in the circuit.

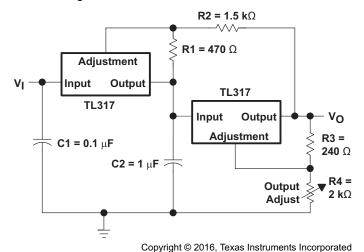


Figure 9. Tracking Preregulator Circuit Schematic

Submit Documentation Feedback

Copyright © 1979–2016, Texas Instruments Incorporated



8.2.6 Slow-Turnon 15-V Regulator Circuit

The capacitor C1, in combination with the PNP transistor, helps the circuit to slowly start supplying voltage. In the beginning, the capacitor is not charged. Therefore, output voltage starts at $V_{C1}+V_{BE}+1.25\ V=0\ V+0.65\ V+1.25\ V=1.9\ V$. As the capacitor voltage rises, V_{OUT} also rises at the same rate. When the output voltage reaches the value determined by R1 and R2, the PNP is turned off.

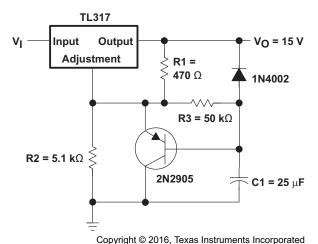


Figure 10. Slow-Turnon 15-V Regulator Circuit Schematic

8.2.7 50-mA Constant-Current Battery-Charger Circuit

The current limit operation mode can be used to trickle charge a battery at a fixed current. $I_{CHG} = 1.25 \text{ V} / 24 \Omega$. V_{I} must be greater than $V_{BAT} + 4.25 \text{ V}$ (1.25 V [V_{REF}] + 3 V [headroom]).

Power dissipation through resistor R1 is calculated as shown in Equation 5, so a resistor with the appropriate power rating must be chosen for this application.

$$P(R1) = I_0^2 \times R1[\Omega]$$

$$V_I \longrightarrow \begin{bmatrix} TL317 \\ Input & Output \\ Adjustment \end{bmatrix}$$

$$(5)$$

Copyright © 2016, Texas Instruments Incorporated

Figure 11. 50-mA Constant-Current Battery-Charger Circuit

Copyright © 1979–2016, Texas Instruments Incorporated

8.2.8 Current-Limited 6-V Charger

As the charge current increases, the voltage at the bottom resistor increases until the NPN starts sinking current from the adjustment pin. The voltage at the adjustment pin drops, and consequently the output voltage decreases until the NPN stops conducting.

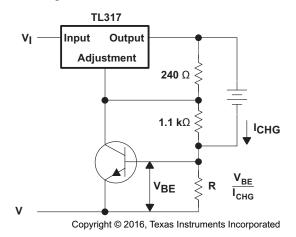
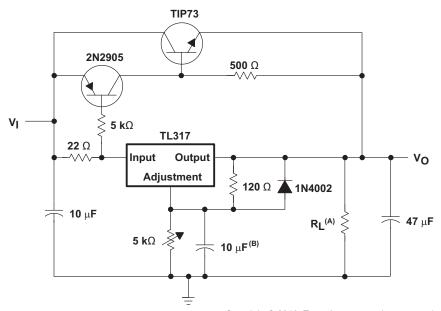


Figure 12. Current-Limited 6-V Charger Schematic

8.2.9 High-Current Adjustable Regulator

The NPNs at the top of the schematic allow higher currents at V_{OUT} than the LM317 can provide, while still keeping the output voltage at levels determined by the adjustment pin resistor divider of the LM317.



Copyright © 2016, Texas Instruments Incorporated

- A. Minimum load current is 30 mA.
- B. Optional capacitor improves ripples rejection.

Figure 13. High-Current Adjustable Regulator Schematic

Product Folder Links: *TL317*

12



9 Power Supply Recommendations

The TL317 is designed to operate from an input voltage supply range between 1.25 V to 35 V greater than the output voltage. If the device is more than six inches from the input filter capacitors, an input bypass capacitor, 0.1- μ F (or greater), of any type is required for stability.

10 Layout

10.1 Layout Guidelines

- It is recommended that the input terminal be bypassed to ground with a bypass capacitor.
- The optimum placement for the bypass capacitor is closest to the input terminal of the device and the system GND. Take care to minimize the loop area formed by the bypass-capacitor connection, the input terminal, and the system GND.
- For operation at full rated load, it is recommended to use wide trace lengths to eliminate I × R drop and heat dissipation.

10.2 Layout Example

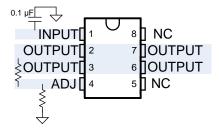


Figure 14. TL317D Layout Example

Copyright © 1979–2016, Texas Instruments Incorporated



11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com

10-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
TL317CD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	TL317C
TL317CD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	TL317C
TL317CDE4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	TL317C
TL317CDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	0 to 125	TL317C
TL317CDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	TL317C
TL317CDRE4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	TL317C
TL317CDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	TL317C
TL317CDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	TL317C
TL317CLP	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	TL317C
TL317CLP.A	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	TL317C
TL317CLPE3	Active	Production	TO-92 (LP) 3	1000 BULK	Yes	SN	N/A for Pkg Type	0 to 125	TL317C
TL317CLPR	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	TL317C
TL317CLPR.A	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	TL317C
TL317CLPRE3	Active	Production	TO-92 (LP) 3	2000 LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	TL317C
TL317CPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	0 to 125	T317
TL317CPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	T317
TL317PS	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T317
TL317PS.A	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T317
TL317PSR	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T317
TL317PSR.A	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T317

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.



PACKAGE OPTION ADDENDUM

www.ti.com 10-Nov-2025

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL317CDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TL317CDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL317CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL317PSR	so	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

www.ti.com 24-Jul-2025



*All dimensions are nominal

7 111 41111011010110 410 11011111141							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL317CDR	SOIC	D	8	2500	364.0	364.0	27.0
TL317CDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TL317CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL317PSR	so	PS	8	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL317CD	D	SOIC	8	75	507	8	3940	4.32
TL317CD.A	D	SOIC	8	75	507	8	3940	4.32
TL317CDE4	D	SOIC	8	75	507	8	3940	4.32
TL317PS	PS	SOP	8	80	530	10.5	4000	4.1
TL317PS.A	PS	SOP	8	80	530	10.5	4000	4.1



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



TO-92 - 5.34 mm max height

TO-92



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.
- 3. Lead dimensions are not controlled within this area. 4. Reference JEDEC TO-226, variation AA.
- 5. Shipping method:

 - a. Straight lead option available in bulk pack only.
 b. Formed lead option available in tape and reel or ammo pack.
 - c. Specific products can be offered in limited combinations of shipping medium and lead options.
 - d. Consult product folder for more information on available options.



TO-92





TO-92







SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025