









TL103W, TL103WA, TL103WB SLOS437R - APRIL 2004 - REVISED APRIL 2024

TL103Wx Dual Operational Amplifiers With Internal Reference

1 Features

- New TL103WB, a pin-compatible upgrade to the TL103W and TL103WA
- Improved specifications of B version amplifiers:
 - Supply range: 3V to 36V
 - Low maximum input offset voltage: ±2mV (25°C) and ±2.5mV (full temperature)
 - Gain bandwidth: 1.2MHz
 - Total supply current: 550µA
 - EMI rejection: integrated RF and EMI filter
 - Temperature range: –40°C to 125°C
- Improved specifications of B version reference:
 - Fixed 2.5V reference
 - Tight tolerance maximum of 0.44% (25°C) and 1.04% (full temperature)
 - Wide sink-current range: 0.2mA (typical) to 100mA

2 Applications

- **Battery chargers**
- Switch-mode power supplies
- Linear voltage regulation
- **Data-acquisition systems**
- Precision constant current sink

3 Description

The TL103Wx devices combine the building blocks of a dual operational amplifier and a fixed voltage reference - both of which are often used in the control circuitry of switch-mode and linear power supplies. OP AMP1 has the noninverting input internally tied to a fixed 2.5V reference, while OP AMP2 is independent, with both inputs uncommitted.

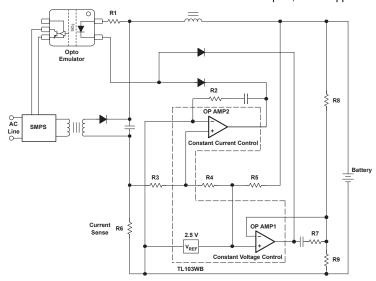
The upgraded TL103WB features improvements such as a wider supply range (up to 36V), lower supply current (275µA/amp) and tighter voltage regulation. This regulation can be achieved through low offset voltages for both operational amplifiers (0.3mV typical) and tight tolerances for the voltage reference (0.44% at 25°C and 1.04% over operating temperature range).

The TL103WB has a widened temperature range of -40°C to 125°C.

Package Information

PART NUMBER	CHANNEL COUNT	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)
TL103W TL103WA		D (SOIC, 8)	4.9mm × 6mm
TL103WB	Dual + Reference	D (SOIC, 8)	4.9mm × 6mm
TETOSWB		DDF (SOT-23, 8)	2.9mm × 2.8mm

- (1) For more information, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit



Table of Contents

1 Features1	6.3 Feature Description12
2 Applications1	6.4 Device Functional Modes1
3 Description1	7 Application and Implementation14
4 Pin Configuration and Functions3	7.1 Application Information14
5 Specifications4	7.2 Typical Applications14
5.1 Absolute Maximum Ratings4	7.3 Power Supply Recommendations1
5.2 ESD Ratings	7.4 Layout1
5.3 Recommended Operating Conditions4	8 Device and Documentation Support1
5.4 Thermal Information5	8.1 Documentation Support1
5.5 Electrical Characteristics: OP AMP1 (V _{REF} at	8.2 Receiving Notification of Documentation Updates1
Noninverting input)5	8.3 Support Resources1
5.6 Electrical Characteristics: OP AMP2	8.4 Trademarks1
(Independent Amplifier)6	8.5 Electrostatic Discharge Caution1
5.7 Typical Characteristics: TL103WB8	8.6 Glossary1
6 Detailed Description12	9 Revision History1
6.1 Overview	10 Mechanical, Packaging, and Orderable
6.2 Functional Block Diagram12	Information2
-	



4 Pin Configuration and Functions

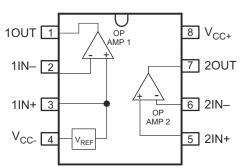


Figure 4-1. D and DDF Packages, 8-Pin SOIC and SOT-23-THN (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME			DESCRIPTION
10UT	1	0	Opamp 1 output
1IN-	2	I	Opamp 1 inverting input
1IN+	3	I	Opamp 1 non-inverting input and Shunt reference cathode terminal
V _{CC} -	4	I	Negative Supply Voltage
2IN+	5	I	Opamp 2 non-inverting input
2IN-	6	I	Opamp 2 inverting input
2OUT	7	0	Opamp 2 output
V _{CC+}	8	I	Positive Supply Voltage

(1) I = input, O = output



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V Complex calls as		TL103W/TL103WA	0	36	V
V _{CC±}	Supply voltage	TL103WB	0	40	V
V _{ID}	Operational amplifier input differential voltage			36	V
VI	Operational amplifier input voltage range ⁽²⁾		(V _{CC-}) - 0.3	V _{CC+}	V
I _{KA}	Voltage reference cathode current			100	mA
TJ	Maximum junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Not applicable to pin 4 (1IN+)

5.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
V _(ESD)	Liectiostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Supply voltage	TL103W/TL103WA	3	32	V
V _{CC±}	Supply voltage	TL103WB	3	36	V
V _{ICR}	Input common-mode voltage range		V _{CC-}	(V _{CC+}) - 2	V
L.	Cathode current	TL103W/TL103WA	0.5	100	mA
IK	Cathode Current	TL103WB	0.2	100	IIIA
т	Operating free air temperature	TL103W/TL103WA	-40	105	°C
I A	Operating free-air temperature	TL103WB	-40	125	C

⁽²⁾ JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.



5.4 Thermal Information

		TL10	TL103Wx			
	THERMAL METRIC(1)	SOIC (D)	SOT-23 (DDF)	UNIT		
		8 PINS	8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.4	170.1	°C/W		
R _{0JC(top)}	Junction-to-case (top) thermal resistance	77.3	89.7	°C/W		
R _{0JB}	Junction-to-board thermal resistance	78.9	87.5	°C/W		
Ψ_{JT}	Junction-to-top characterization parameter	27.4	7.5	°C/W		
Ψ_{JB}	Junction-to-board characterization parameter	78.1	87.3	°C/W		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	_	_	°C/W		

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics: OP AMP1 (V_{REF} at Noninverting input)

 V_{CC+} = 5V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

	PARAMETER	TES	T CONDITIONS		TA	MIN	TYP	MAX	UNIT
AMPLIFI	ER								
				TL103W			±1	±4	
					Full range			±5	
.,				TI 1001111			±0.5	±3.0	.,
V _{IO}	Input offset voltage	V _{ICM} = 0V		TL103WA	Full range			±5	mV
				TI 40014/D			±0.3	±2	
				TL103WB	Full range			±2.5	
.,				TL103W/TL103WA	Full range		±7		
αV _{IO}	Input offset-voltage drift			TL103WB	Full range		±2		μV/°C
				TL103W/TL103WA			-20		
I _{IB}	Input bias current (negative input)			TL103WB			-15		nA
				TL103W/TL103WA			100		
A_{VD}	Large-signal voltage gain	$V_{CC+} = 15V, R_L = 2k\Omega, V_{ICM} = 0 V$		TL103WB			210		V/mV
				TL103W/TL103WA		65	100		dB
PSRR	Supply-voltage rejection ratio	$V_{CC+} = 5V \text{ to } 30V, V_{ICM} = 0V$		TL103WB		99	114		
		Source			20	40			
		V _{CC+} = 15V, V _O = 2V, V _{ID} = 1V		TL103W/TL103WA		10	12		mA
I _O	Output current		Sink	TL103WB		10	24		
		45777 0 0777 477	OiI-	TL103W/TL103WA		12	50		
		$V_{CC+} = 15V, V_O = 0.2V, V_{ID} = -1V$	Sink	TL103WB		60	100		μA
I _{SC}	Short-circuit to GND	V _{CC+} = 15V					±40	±68	mA
				TI 400\A/TI 400\A/A		26	27		
		V 20V D 01/0	Desiring Dellar	TL103W/TL103WA	Full range	26			
		$V_{CC+} = 30V, R_L = 2k\Omega$	Positive Rail (V _{CC+})	TI 400\A/D		27.4	28.3		
				TL103WB	Full range	27.4			v
.,	Maltana autoritani faran mali			TI 400\A/TI 400\A/A		27	28		, v
Vo	Voltage output swing from rail	V 20V D 4010	Desiring Dellar	TL103W/TL103WA	Full range	27			
		$V_{CC+} = 30V$, $R_L = 10k\Omega$	Positive Rail (V _{CC+})	TI 10011/D		27.6	28.6		
				TL103WB	Full range	27.6			
		D 4010	No mating Ball () (5	20	
		$R_L = 10k\Omega$	Negative Rail (V _{CC-})		Full range			20	mV
0.0	Oleverate at write main	V 45V 0 400-5 D 310 V	0.51/401/	TL103W/TL103WA		0.2	0.4		\// ₁
SR	Slew rate at unity gain	$V_{CC+} = 15V, C_L = 100pF, R_L = 2k\Omega, V_I$	= 0.5V to 2V, unity gain	TL103WB		0.2	0.5		V/µs
CDW	Cain handwidth mades	V _{CC+} = 30V, V _I = 10mV, C _L = 100pF, F	R _L = 2kΩ, f = 100kHz	TL103W/TL103WA		0.5(1)	0.9		NAL I-
GBW	Gain bandwidth product	V _{CC+} = 36V, V _I = 10mV, C _L = 100pF, F	R _L = 2kΩ, f = 100kHz	TL103WB		0.7(1)	1.2		MHz



5.5 Electrical Characteristics: OP AMP1 (V_{REF} at Noninverting input) (continued)

 $V_{CC+} = 5V$, $V_{CC-} = GND$, $T_A = 25$ °C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		TA	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	V_{CC+} = 30V, V_O = 2V _{PP} , C_L = 100pF, R_L = 2k Ω , f = 1kHz, A_V = 20dB	TL103W/TL103WA			0.02		%
טחו	rotal narmonic distortion	V_{CC+} = 36V, V_O = 2V _{PP} , C_L = 100pF, R_L = 2k Ω , f = 1kHz, A_V = 20dB	TL103WB			0.005		70
		V _{CC+} = 5V, no load	- TL103W/TL103WA			0.7	1.2	
l	Total supply current, excluding cathode-current reference (both	V _{CC+} = 30V, no load	TE 103VV/TE 103VVA	Full range			2	mA
Icc	amplifiers)	V _{CC+} = 5V, no load	TL103WB			0.55	0.77	ША
		V _{CC+} = 36V, no load	TEIOSWB	Full range			1.35	
VOLTAG	E REFERENCE							
			TL103W		2.482	2.5	2.518	V
V _{ref}	Reference Voltage	I _K = 10mA	1110300	Full Range	2.465		2.535	V
V ref	Reference voltage	IK - TOTILA	TL103WA/TL103WB		2.489	2.5	2.511	V
			IL 103WA/ IL 103WB	Full Range	2.474		2.526	V
A\/	Reference input voltage deviation	L = 10mA	TL103W	Full Range		7	35 ⁽¹⁾	mV
ΔV_{ref}	over temperature range	I _K = 10mA	TL103WA/TL103WB	Full Range		7	26 ⁽¹⁾	mV
	Minimum cathode current for		TL103W/TL103Wx			0.5	1	mA
I _{min}	regulation		TL103WB			0.2	1	IIIA
Z _{KA}	Dynamic impedance	I _{KA} = 1mA to 100mA, f < 1kHz				0.45	0.8	Ω

⁽¹⁾ Not tested in production, limits set by characterization and simulation.

5.6 Electrical Characteristics: OP AMP2 (Independent Amplifier)

 V_{CC+} = 5V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		T _A	MIN	TYP	MAX	UNIT
			TI 4001M			±1	±4	
			TL103W	Full range			±5	
.,	Input offset voltage	\\\ - 0\\	TL103WA			±0.5	±3.0	\ /
V _{IO}	Input onset voltage V _{II}	pput offset voltage $V_{ICM} = 0V$	TLIUSWA	Full range			±5	mV
			TL103WB			±0.3	±2	
			I L 103WB	Full range			±2.5	
αV _{IO}	Input offset-voltage drift		TL103W/TL103WA	Full range		±7		μV/°C
uvio	input onset-voltage unit		TL103WB	Full range		±2		μν/ С
		TL103W/TL103WA			±2	±75		
L.	Input offset current		TE 103W/TE 103WA	Full range			±150	nA
I _{IO}	input onset current		TL103WB			±0.5	±4	шА
			TETOSWB	Full range			±5	
			TL103W/TL103WA			-20	-150	
			TE103W/TE103WA	Full range			-200	
I _{IB}	Input bias current		TL103WB			-15	-35	nA
				Full range			-50	
			TL103W/TL103WA		50	100		
۸	Large-signal voltage gain	 V _{CC+} = 15V, R _L = 2kΩ, VO = 1.4V to 11.4V	TE 103VV/TE 103VVA	Full range	25	100		V/mV
A_{VD}	Large-signal voltage gain	VCC+ - 13V, RL - 2K12, VO - 1.4V to 11.4V	TL103WB		77	210		V/IIIV
			TETOSWB	Full range	45	210		
PSRR	Supply-voltage rejection ratio	V _{CC+} = 5V to 30V	TL103W/TL103WA		65	100		dB
FOILIT	Supply-voltage rejection ratio	VCC+ - 34 to 304	TL103WB		99	114		uБ
V	Input common-mode voltage range	V _{CC+} = 30V			V _{CC-}		(V _{CC+}) - 1.5	V
V _{ICR}	input common-mode voltage range	VCC+ - 30V		Full range	V _{CC} -		(V _{CC+}) - 2	V
	TI 4021M/TI 4021M	TI 400\M/TI 400\MA		70	95			
CMRR	Common mode velection we!		TL103W/TL103WA	Full range	60			dB
CIVIKK	Common-mode rejection ratio	V _{CC+} = 30V	TI 40014/D		93	104		
			TL103WB	Full range	70			



5.6 Electrical Characteristics: OP AMP2 (Independent Amplifier) (continued)

 $V_{CC+} = 5V$, $V_{CC-} = GND$, $T_A = 25$ °C (unless otherwise noted)

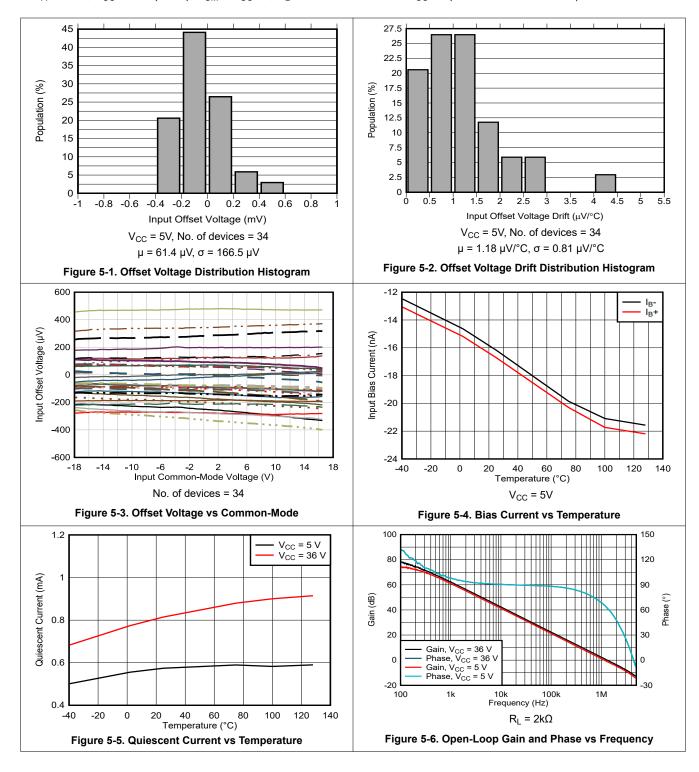
	PARAMETER	TEST	CONDITIONS		TA	MIN	TYP	MAX	UNIT
			Source			20	40		
		V _{CC+} = 15V, V _O = 2V, V _{ID} = 1V	OiI-	TL103W/TL103WA		10	12		mA
lo	Output current		Sink	TL103WB		10	24		
		V 45VV 00VV 4V	Sink	TL103W/TL103WA		12	50		
		V _{CC+} = 15V, V _O = 0.2V, V _{ID} = -1V Sink TL103WB		60	100		μA		
I _{SC}	Short-circuit to GND	V _{CC+} = 15V	•				±40	±68	mA
				TL103W/TL103WA		26	27		
		$V_{CC+} = 30V, R_1 = 2k\Omega$ Positive Rail (V_{CC+})	TE 103VV/TE 103VVA	Full range	26				
		V _{CC+} = 30V, R _L = 2KΩ	Positive Raii (V _{CC+})	TL103WB		27.4	28.3		
				ILIUSWB	Full range	27.4			V
V _O	Voltage output owing from roil	foltage output swing from rail $V_{CC+}=30V,R_L=10k\Omega \qquad \qquad \text{Positive Rail (V_{CC+})}$ $R_L=10k\Omega \qquad \qquad \text{Negative Rail (V_{CC-})}$		TL103W/TL103WA		27	28		V
v _O	voltage output swing from rail		Positive Pail (V)	TE103W/TE103WA	Full range	27			
			Positive Rail (VCC+)	TL103WB		27.6	28.6		
					Full range	27.6			
			Negative Reil (V				5	20	mV
				Full range			20	IIIV	
SR	Slew rate at unity gain	$V_{CC+} = 15V, C_1 = 100pF, R_1 = 2k\Omega, V_1 = 100pF$	- 0.5\/ to 2\/ unity gain	TL103W/TL103WA		0.2	0.4		V/µs
SIX	Siew rate at unity gain	VCC+ = 13V, CL = 100p1, INL = 2K32, V -	- 0.5V to 2V, utility gaili	TL103WB		0.2	0.5		ν/μ5
GBW	Gain bandwidth product	$V_{CC+} = 30V, V_I = 10mV, C_L = 100pF, R_I$	= 2kΩ, f = 100kHz	TL103W/TL103WA		0.5(1)	0.9		MHz
GDVV	Gain bandwidth product	$V_{CC+} = 36V, V_I = 10mV, C_L = 100pF, R_I$	= 2kΩ, f = 100kHz	TL103WB		0.7(1)	1.2		IVII IZ
THD	Total harmonic distortion	$V_{CC+} = 30V$, $V_O = 2V_{PP}$, $C_L = 100pF$, R_1 20dB	$_{\perp}$ = 2k Ω , f = 1kHz, A _V =	TL103W/TL103WA			0.02		- %
טחו	Total Harmonic distortion	$V_{CC+} = 36V$, $V_O = 2V_{PP}$, $C_L = 100pF$, $R_1 = 20dB$	$= 2k\Omega$, $f = 1kHz$, $A_V =$	TL103WB			0.005		70
V _n	Faviralent innut naise valtage	$V_{CC+} = 30V, R_S = 100 \Omega, f = 1kHz$		TL103W/TL103WA			50		nV/√Hz
v _n	Equivalent input noise voltage	$V_{CC+} = 36V, R_S = 100 \Omega, f = 1 \text{kHz}$ TL103WB	TL103WB			38		IIV/VIIZ	
		V _{CC+} = 5V, no load		TI 403\A//TI 403\A/A			0.7	1.2	
	Total supply current, excluding			TL103W/TL103WA	Full range			2	^
I _{CC}	amplifiers)	athode-current reference (both mplifiers) $V_{CC+} = 5V$, no load					0.55	0.77	- mA
		$V_{CC+} = 36V$, no load		TL103WB	Full range			1.35	1

⁽¹⁾ Not tested in production, limits set by characterization and simulation.



5.7 Typical Characteristics: TL103WB

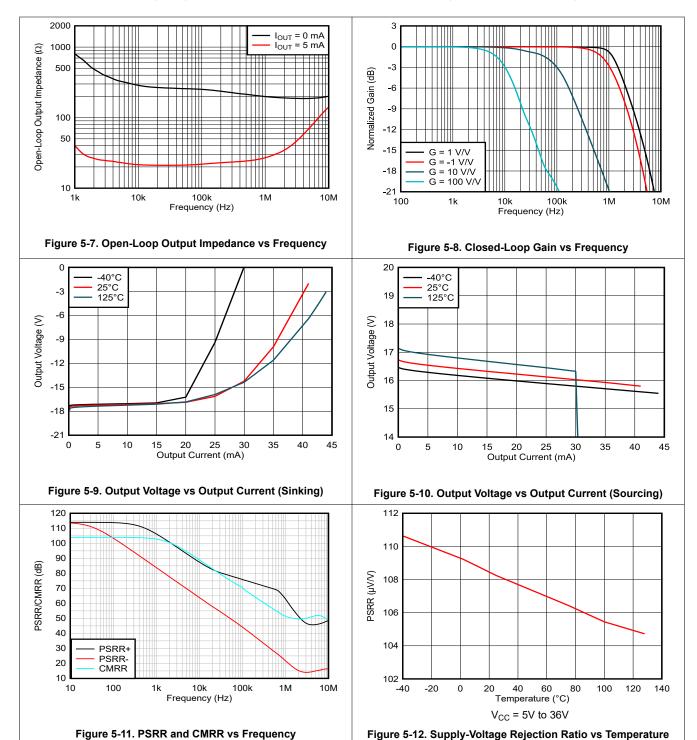
at $T_A \cong 25^{\circ}\text{C}$, $V_{CC} = 36\text{V}$ (±18V), $V_{CM} = V_{CC}$ / 2, $R_L = 10\text{k}\Omega$ connected to V_{CC} / 2 (unless otherwise noted)





5.7 Typical Characteristics: TL103WB (continued)

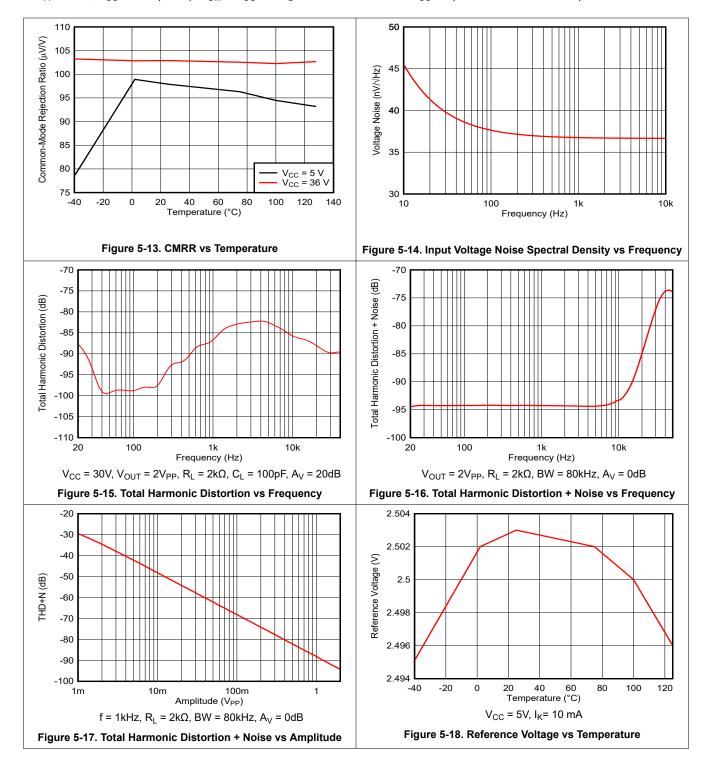
at $T_A \cong 25^{\circ}C$, $V_{CC} = 36V$ (±18V), $V_{CM} = V_{CC} / 2$, $R_L = 10k\Omega$ connected to $V_{CC} / 2$ (unless otherwise noted)





5.7 Typical Characteristics: TL103WB (continued)

at $T_A \cong 25^{\circ}C$, $V_{CC} = 36V$ (±18V), $V_{CM} = V_{CC} / 2$, $R_L = 10k\Omega$ connected to $V_{CC} / 2$ (unless otherwise noted)





5.7 Typical Characteristics: TL103WB (continued)

at $T_A \cong 25^{\circ}C$, $V_{CC} = 36V$ (±18V), $V_{CM} = V_{CC} / 2$, $R_L = 10k\Omega$ connected to $V_{CC} / 2$ (unless otherwise noted)

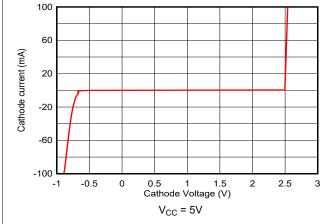


Figure 5-19. Cathode Current vs Cathode Voltage

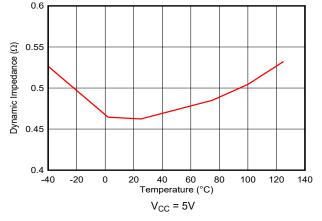


Figure 5-20. Reference Dynamic Impedance vs Temperature

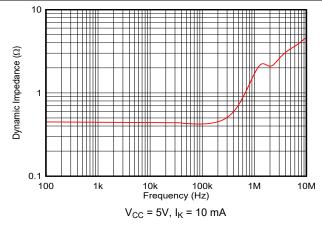
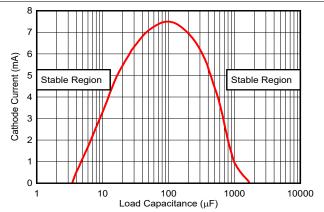


Figure 5-21. Reference Dynamic Impedance vs Frequency



The area under the curve represents typical conditions that can cause the device to oscillate

Figure 5-22. Reference Stability vs Capacitive Load

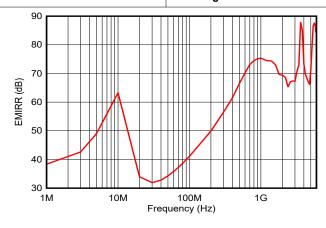


Figure 5-23. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

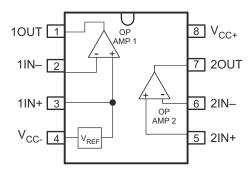
6 Detailed Description

6.1 Overview

The TL103Wx features two high-voltage amplifiers and a shunt voltage reference to allow for cost-sensitive and compact battery charger CC/CV feedback circuits. The upgraded TL103WB features is designed to provide a wide supply range (up to 36V), low offset voltage (±0.3mV typical) and a 1.2MHz bandwidth. The integrated voltage reference is tied to the non-inverting pin of one of OP AMP 1 and provides a fixed 2.5V referenced to the negative supply of the device. The shunt reference of the TL103WA/TL103WB features a tight tolerance of 0.44% at 25°C.

When a single supply voltage of 5V is used (or ±2.5V split supply), the TL103Wx internal reference allows for a more accurate and power-efficient mid-supply signal to be used throughout your circuit. The TL103W/TL103WA devices are characterized for operation from -40°C to 85°C, the TL103WB devices are characterized for operation from -40°C to 125°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Internal Reference

The TL103Wx family features an internal shunt reference, tied to the non-inverting pin of one of the devices amplifiers. When supplied with enough voltage headroom (≥ 2.5V) and cathode current (0.5mA typical), the reference of the TL103Wx is forced to a fixed 2.5V. To not exceed the maximum cathode current, be sure that the reference input is current limited. Unlike many linear regulators, the reference of the TL103W is internally compensated to be stable without an output capacitor between the cathode and anode. If the reference is used to supply a load, stability criteria shown in Figure 5-22 needs to be met.

Reference voltage tolerance varies based off the device grade chosen. At 25°C the TL103W features a reference tolerance of 0.72%, while the TL103WA/TL103WB both feature reference tolerances of 0.44%.

6.3.2 Input Common Mode Range

The valid common mode range is from device ground to $V_{CC+} - 1.5V$ ($V_{CC+} - 2V$ across temperature). Inputs may exceed V_{CC+} up to the absolute maximum voltage without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input is more than 0.3V below V_{CC-} then input current should be limited to 1mA and the output phase is undefined.



6.3.3 EMI Rejection

The TL103WB uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications (radio frequency interference - RFI) and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TL103WB benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-1 shows the results of this testing on the TL103WB. Table 6-1 shows the EMIRR IN+ values for the TL103WB at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance relating to op amps and is available for download from www.ti.com.

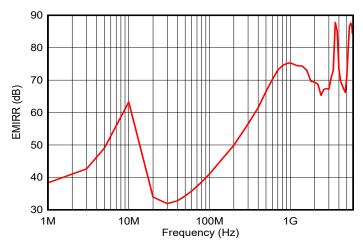


Figure 6-1. EMIRR Testing

Table 6-1. TL103WB EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION			
400MHz	400MHz Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications			
900MHz	900MHz Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications			
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2GHz)	70dB		
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	65dB		
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88dB		
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	71dB		

6.4 Device Functional Modes

This device has one mode of operation that applies when operated within the recommended operating conditions.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

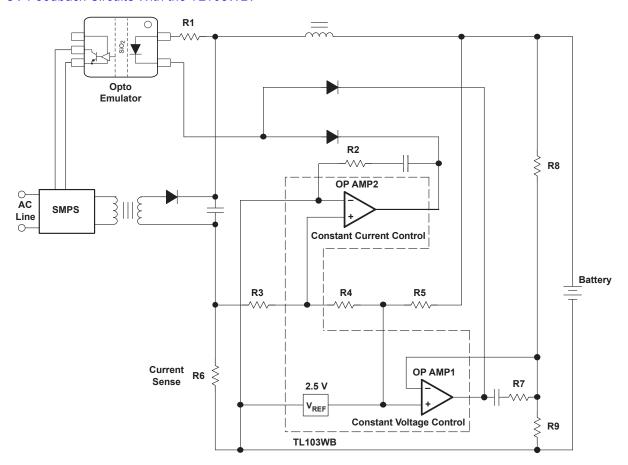
7.1 Application Information

The TL103Wx family offers a cost-effective and compact device for applications requiring both an accurate DC signal and signal conditioning. These devices offer a fixed 2.5V reference, wide bandwidth (1 to 1.2 MHz) and a low total supply current (0.55 to 0.7mA).

7.2 Typical Applications

7.2.1 Isolated Flyback CC/CV Feedback

As shown in Figure 7-1, the TL103Wx is often used alongside an opto-coupler/opto-emulator to provide feedback to an isolated flyback. Utilizing the TL103Wx in this way allows for both an accurate and cost-optimized battery charger design that can achieve a stable CC/CV (Constant Current/Constant Voltage) charging profile. In this example, a simplified design procedure will be discussed. Additional details can be found in *Designing CC-CV Feedback Circuits With the TL103WB*.



Typical Application Circuit



7.2.1.1 Design Requirements

The objective is to design an accurate CC-CV feedback circuit with the requirements provided in Table 7-1.

Table 7-1. Design Parameters

PARAMETER	VALUE
Maximum Charge Current	6A
Battery Voltage Range	6V to 20V

7.2.1.2 Detailed Design Procedure

To switch between CV control and CC control, diodes are utilized to achieve an OR logic function as shown in Figure 7-1. Designing the circuit in this way allows one of the amplifiers (configured in either CC or CV mode) to dominate the feedback in the design. In this design, *GND* refers to the negative node at the secondary side of the switch-mode power supply.

The fixed 2.5V of the TL103Wx reference provides a stable DC voltage that is used to specify the CC current and CV voltage. One of the requirements of achieving this fixed value, however, is that the cathode of the reference must be supplied with a voltage of 2.5V or above.

7.2.1.2.1 Constant Current Circuit

For the constant current feedback circuit, the amplifier is configured in a low-side current sense configuration. Resistor R6 is used as the current sensing resistor to sense the current flowing between the battery and flyback converter. This is shown in Equation 1, where I_{BAT} is the output current delivered to the battery. The voltage at the non-inverting input of the amplifier specifies the maximum current (or constant current) that is delivered to the battery.

$$V_{BAT} = I_{BAT} \times R6 \tag{1}$$

The reference of the TL103Wx is powered by the battery voltage. To be able to achieve a constant current, this reference needs to be provided with 2.5V or greater to provide a fixed 2.5V. The first step in designing a constant current circuit is to specify that 2.5V can be achieved at the battery's minimum voltage. The value of R5 must also be designed so that a sink-current between 0.5mA to 100 mA (for TL103W or TL103WA) is achieved across the specified range of the battery voltage. These two steps are shown below.

$$V_{BAT}(min) \times \frac{R4 + R3}{R4 + R3 + R5 + R6} \ge 2.5 \text{ V}$$
 (2)

$$0.5 \text{ mA} \le \frac{V_{BAT} - V_{REF}}{R5} \le 100 \text{ mA}$$
 (3)

For this design R5 is chosen to be $2k\Omega$. Knowing this and the specified battery range of 6V to 20V, we can calculate that the reference sinks anywhere from 1.75mA to 10mA using Equation 2.

Once a fixed 2.5V reference is achieved, we can use this accurate DC voltage to specify a constant current target on the non-inverting input of the amplifier. This can be done by calculating the voltage at the amplifier's inverting input when a constant current target is achieved. Specifying R6 to be $10m\Omega$ along with a constant current design target of 6A, we find that this voltage to be 60 mV using Equation 1. The voltage at the non-inverting pin of the amplifier is specified by Equation 4.

$$V_{IN+} = 2.5 V \times \frac{R3}{R4+R3} \tag{4}$$

Using the component values and design targets calculated so far, Equation 2 and Equation 4 can be updated to:

$$6 V \times \frac{R4 + R3}{R4 + R3 + 2 k\Omega + 10 m\Omega} \ge 2.5 V$$
 (5)



$$60 \ mV = 2.5 \ V \times \frac{R3}{R4 + R3} \tag{6}$$

Using both Equation 5 and Equation 6, we calculate that R3 needs to be greater than around 34.28 Ω . Adding additional headroom to this, we can calculate R3 = 36 Ω and R4 = 1464 Ω .

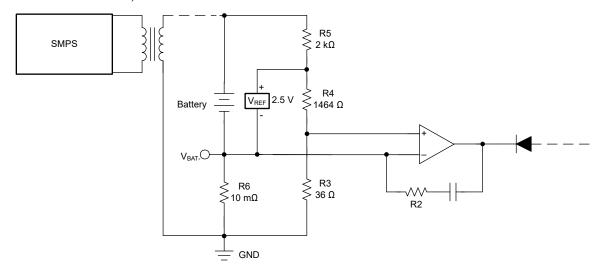


Figure 7-1. Constant Current Feedback Circuit

7.2.1.2.2 Constant Voltage Circuit

For the constant voltage feedback circuit, resistors R8 and R9 divide down the battery voltage to compare against the TL103Wx's reference. This is shown in Figure 7-2. The voltage at the inverting input of the amplifier is designed to equal 2.5V when the battery reaches its maximum specified voltage (or desired constant voltage value). This is shown in for a maximum voltage of 20V provided in Table 7-1.

$$V_{BAT} \times \frac{R9}{R8 + R9} = 2.5 V \tag{7}$$

$$20 V \times \frac{R9}{R8 + R9} = 2.5 V \tag{8}$$

To mimic the constant current circuit and achieve a total impedance and $2k\Omega$ across the battery, R8 is set to $1.96k\Omega$ and R9 to 280Ω .

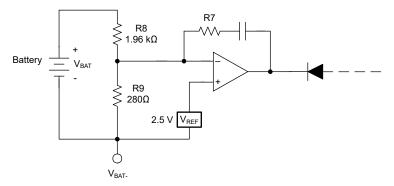


Figure 7-2. Constant Voltage Circuit



7.2.2 Constant Current Sink

Figure 7-3 shows the use of the TL103Wx along with a transistor to provide a constant current sink source. This type of circuit is common in LED drivers and can provide accurate performance and high bandwidth with minimal external components. Accuracy of this circuit is dominated by the reference voltage tolerance, amplifier offset voltage, and resistor tolerance. R_{LIM} is placed to limit the shunt current of the circuit's reference to a maximum of 100mA.

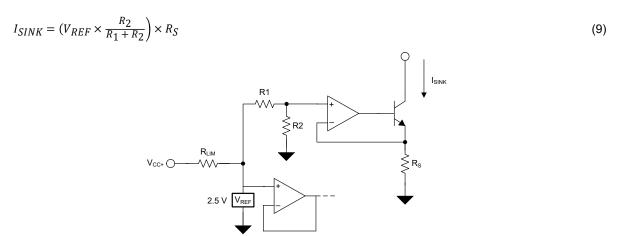


Figure 7-3. TL103Wx as Constant Current Sink

7.3 Power Supply Recommendations

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see Section 7.4

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the
 operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance
 power sources local to the analog circuitry.
 - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for singlesupply applications.
 - If a bypass capacitor is needed to help stabilize the reference, place this capacitor as close to the reference pin as possible.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective
 methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes.
 A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital
 and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If
 not possible to keep them separate, cross the sensitive trace perpendicular as opposed to in parallel with the
 noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in Section 7.4.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.



• For applications shunting high currents through the reference, pay attention to the cathode and anode traces. Ensure the width of these traces are designed with proper current density.

7.4.2 Layout Example

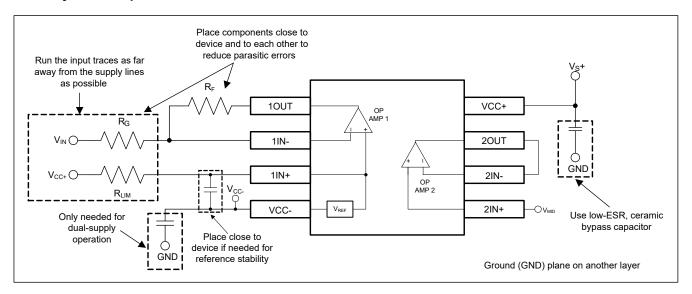


Figure 7-4. Operational Amplifier Board Layout for Inverting Configuration

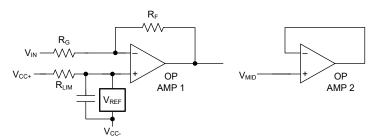


Figure 7-5. Operational Amplifier Schematic for Inverting Configuration



8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- · Texas Instruments, EMI Rejection Ratio of Operational Amplifiers application report
- Texas Instruments, Designing CC-CV Feedback Circuits With the TL103WB

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

 Changes from Revision Q (December 2023) to Revision R (April 2024) Changed TL103WB DDF (SOT-23, 8) status from advanced information (preview) to production 	Page data
(active)	
Changes from Revision P (November 2023) to Revision Q (December 2023)	Page
 Updated maximum dynamic impedance from 0.5 Ω to 0.8 Ω in <i>Electrical Characteristics</i> table Updated EMIRR IN+ values in <i>EMIRR IN+ for Frequencies of Interest</i> table 	
Changes from Revision O (October 2023) to Revision P (November 2023)	Page
Updated typical large-signal voltage gain of TL103WB from 140V/mV to 210 V/mV	5

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Updated minimum limit of supply-voltage rejection ratio of TL103WB from 80 dB to 99dB......5



•	Added footnote in Electrical Characteristics tables to specify specifications which have limits set by
	characterization.
•	Updated minimum limit of gain bandwidth product for TL103WB from 0.5MHz to 0.7MHz
•	
•	Updated maximum limit of total supply current for TL103WB at full temperature range from 1.6mA to
	1.35mA
•	Updated minimum limit of large-signal voltage gain for TL103WB at 25°C from 70V/mV to 77V/mV
•	Updated minimum limit of large-signal voltage gain for TL103WB at full temperature range from 35V/mV to 45V/mV6
•	Added new CMRR specifications for TL103WB
_	
C	hanges from Revision N (August 2023) to Revision O (October 2023) Page
•	Changed maximum input offset voltage, reference tolerance, total supply current and sink-current range in
	the Features section1
•	Changed Typical Application Circuit figure to include TL103WB and Opto-emulator1
•	Changed TL103WB D (SOIC, 8) status from advanced information (preview) to production data (active)1
•	Changed Thermal Information table to include latest thermal metrics
•	Added DDF information to Thermal Information table5
•	Updated k _{SVR} term to PSRR5
•	Changed maximum short circuit current from ±60mA to ±68 mA5
•	Maximum reference input voltage deviation over temperature range for TL103W was changed from 30mV to
	35mV5
•	Maximum reference input voltage deviation over temperature range for TL103WA was changed from 30mV to 26mV
•	Added figures to the <i>Typical Characteristics</i> section to highlight the TL103WB device
•	Added the Detailed Description and Application and Implementation sections
•	Added the Application and Implementation sections14
C	hanges from Revision M (October 2016) to Revision N (August 2023) Page Lindsted Footures section to highlight TI 102/MR
•	Updated <i>Features</i> section to highlight TL103WB1 Updated the numbering format for tables, figures, and cross-references throughout the document
•	Added the <i>TL103WB</i> device information throughout the document
•	
•	Updated <i>Description</i> section
•	Removed DRJ package details and added DDF package for preview
•	Updated formatting for <i>Electrical Characteristics</i> tables
•	Updated typical dynamic impedance from 0.2 Ω to 0.45 Ω in <i>Electrical Characteristics</i> tables
_	opuated typical dynamic impedance from 0.2 ½ to 0.45 ½ in Electrical Characteristics tables
С	hanges from Revision L (February 2016) to Revision M (October 2016) Page
•	Changed positive and negative terminals OP AMP 2 in the D Package image of <i>Pin Configuration and Functions</i>
_	
С	hanges from Revision K (October 2010) to Revision L (February 2016) Page
•	Added the Device Information table, Pin Configuration and Functions, ESD Ratings, Thermal Information,
	Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections1
•	Changed Features from: 2 kV ESD Protection (HBM) to: 2.5-kV ESD Protection (HBM)
•	Changed the Zener diode component to V _{REF} in the <i>Typical Application Circuit</i>



• Changed the Zener diode component to V_{REF} in the D Package of *Pin Configuration and Functions* 3

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TL103WAID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 105	Z103WA
TL103WAIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA
TL103WAIDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA
TL103WBIDDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T13DF
TL103WBIDDFR.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T13DF
TL103WBIDR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL103D
TL103WBIDR.A	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL103D
TL103WBIDR.B	Active	Production	SOIC (D) 8	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
TL103WID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 105	Z103W
TL103WIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W
TL103WIDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION

NSTRUMENTS



TAPE DIMENSIONS KO P1 BO W Cavity A0

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL103WAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WBIDDFR	SOT-23- THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL103WBIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL103WAIDR	SOIC	D	8	2500	353.0	353.0	32.0
TL103WAIDR	SOIC	D	8	2500	353.0	353.0	32.0
TL103WBIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TL103WBIDR	SOIC	D	8	3000	353.0	353.0	32.0
TL103WIDR	SOIC	D	8	2500	353.0	353.0	32.0
TL103WIDR	SOIC	D	8	2500	353.0	353.0	32.0



PLASTIC SMALL OUTLINE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 7. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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