TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

Check for Samples: TL082-N

FEATURES

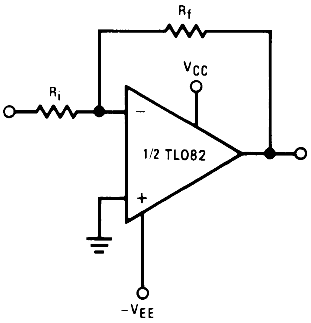
- **Internally Trimmed Offset Voltage: 15 mV**
- **Low Input Bias Current: 50 pA**
- **Low Input Noise Voltage: 16nV/√Hz**
- **Low Input Noise Current: 0.01 pA/√Hz**
- **Wide Gain Bandwidth: 4 MHz**
- **High Slew Rate: 13 V/μs**
- **Low Supply Current: 3.6 mA**
- **High Input Impedance: 10^{12}Ω**
- **Low Total Harmonic Distortion: ≤0.02%**
- **Low 1/f Noise Corner: 50 Hz**
- **Fast Settling Time to 0.01%: 2 μs**

DESCRIPTION

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Typical Connection



Connection Diagram

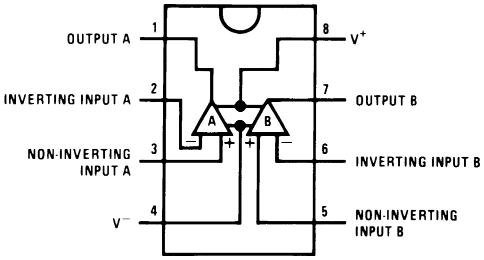


Figure 1. PDIP/SOIC Package (Top View)
See Package Number D0008A or P0008E

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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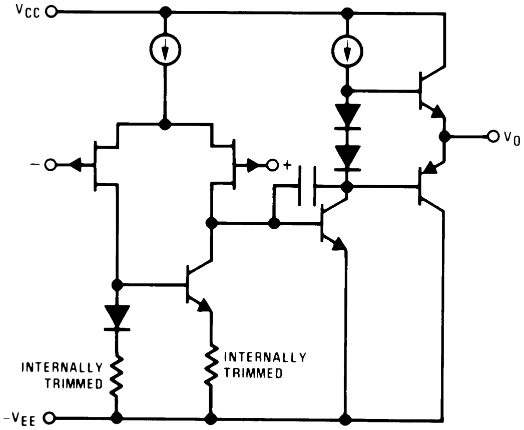
Simplified Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage	±18V
Power Dissipation (3)	(4)
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	150°C
Differential Input Voltage	±30V
Input Voltage Range (5)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C
ESD rating to be determined.	

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The power dissipation limit, however, cannot be exceeded.
(4) For operating at elevated temperature, the device must be derated based on a thermal resistance of 115°C/W junction to ambient for the P0008E package.
(5) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

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DC Electrical Characteristics (1)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		5	15	mV
		Over Temperature			20	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (1) (2)		25	200	pA
		$T_j \le$ 70°C			4	nA
I_B	Input Bias Current	T_j = 25°C, (1) (2)		50	400	pA
		$T_j \le$ 70°C			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C, V_O = ±10V, R_L = 2 kΩ	25	100		V/mV
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		V
				−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \le$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(3)	70	100		dB
I_S	Supply Current			3.6	5.6	mA

(1) These specifications apply for V_S = ±15V and 0°C $\le T_A \le$ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

(2) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

AC Electrical Characteristics (1)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1Hz-20 kHz (Input Referred)		−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C	8	13		V/μs
GBW	Gain Bandwidth Product	V_S = ±15V, T_A = 25°C		4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		25		nV/√Hz
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01		pA/√Hz
THD	Total Harmonic Distortion	A_V = +10, R_L = 10k, V_O = 20 Vp − p, BW = 20 Hz−20 kHz		<0.02		%

(1) These specifications apply for V_S = ±15V and 0°C $\le T_A \le$ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

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Typical Performance Characteristics

Input Bias Current

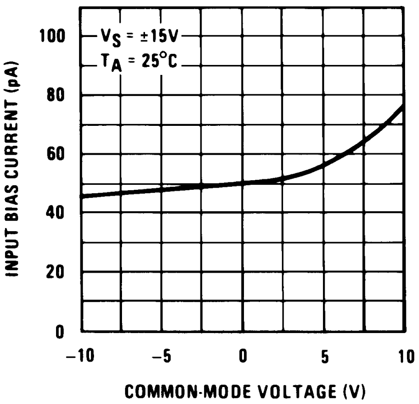

Figure 2.

Input Bias Current

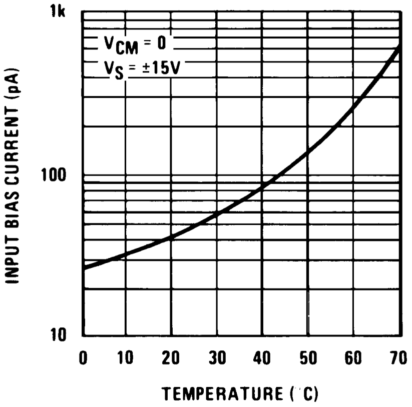

Figure 3.

Supply Current

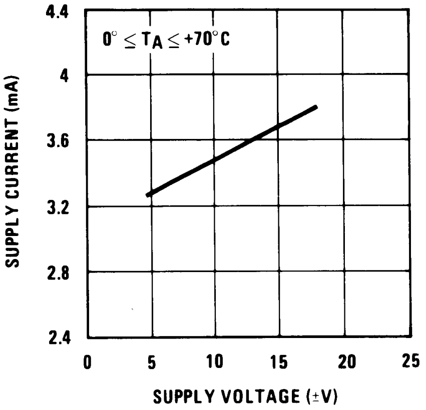

Figure 4.

Positive Common-Mode Input Voltage Limit

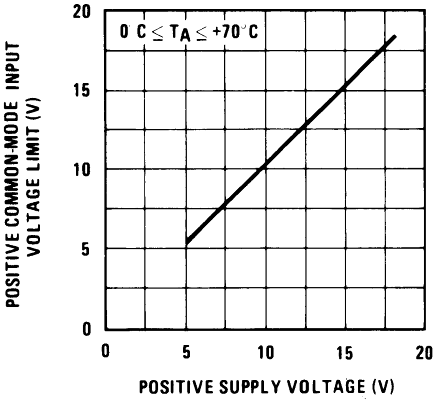

Figure 5.

Negative Common-Mode Input Voltage Limit

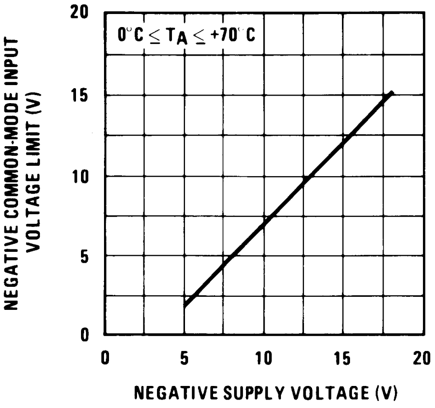

Figure 6.

Positive Current Limit

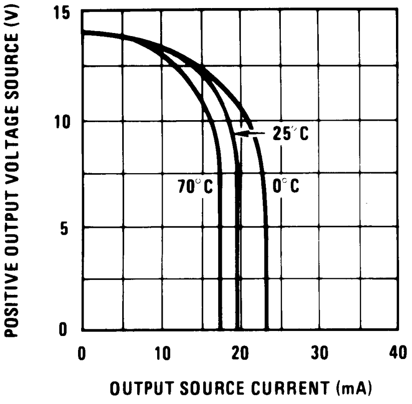

Figure 7.

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Typical Performance Characteristics (continued)

Negative Current Limit

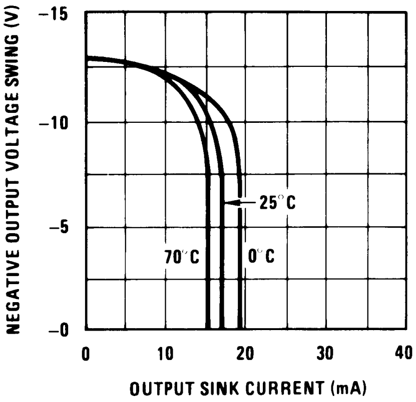

Figure 8.

Voltage Swing

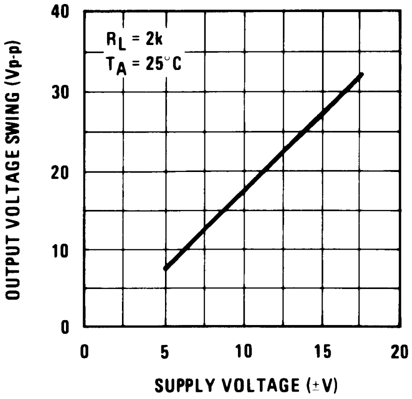

Figure 9.

Output Voltage Swing

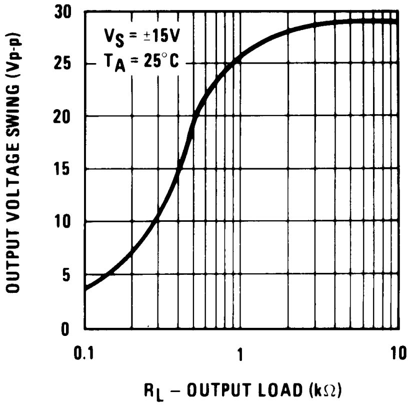

Figure 10.

Gain Bandwidth

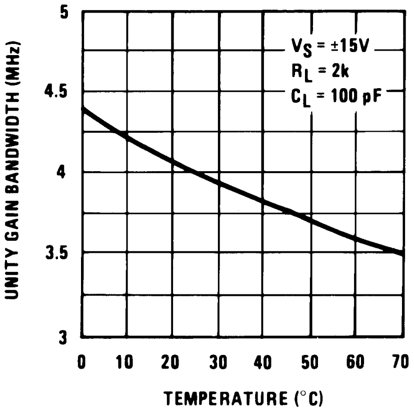

Figure 11.

Bode Plot

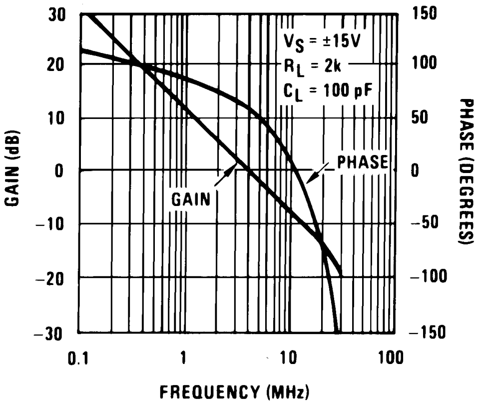

Figure 12.

Slew Rate

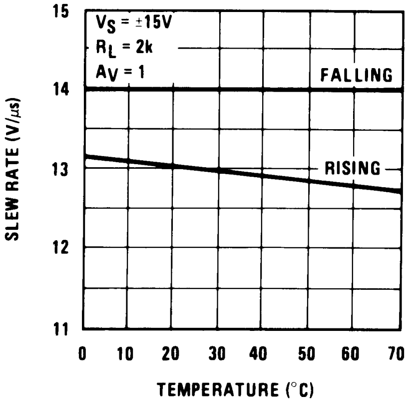

Figure 13.

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Typical Performance Characteristics (continued)

Distortion vs Frequency

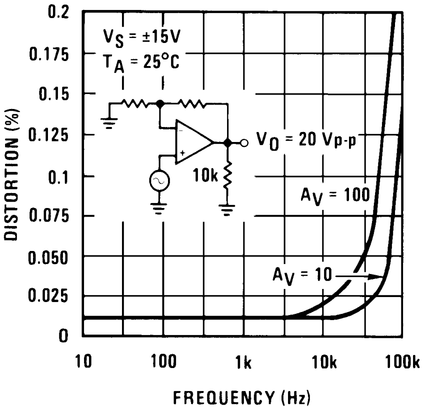

Figure 14.

Undistorted Output Voltage Swing

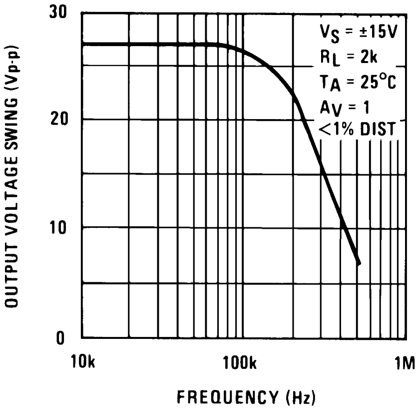

Figure 15.

Open Loop Frequency Response

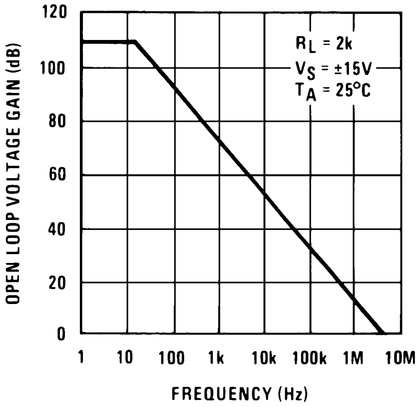

Figure 16.

Common-Mode Rejection Ratio

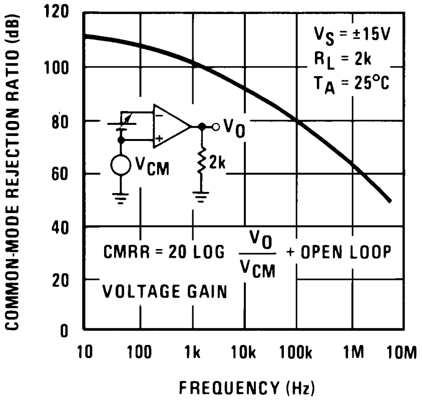

Figure 17.

Power Supply Rejection Ratio

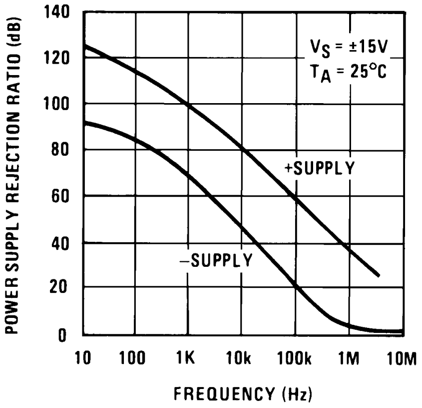

Figure 18.

Equivalent Input Noise Voltage

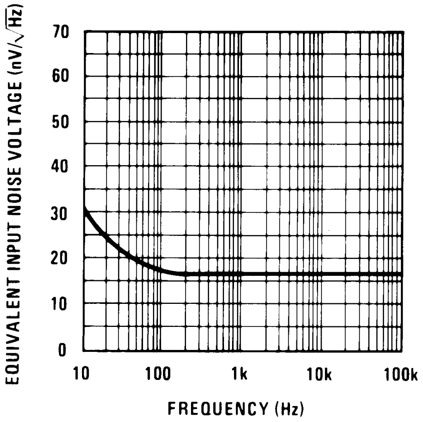

Figure 19.

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Typical Performance Characteristics (continued)

Open Loop Voltage Gain (V/V)

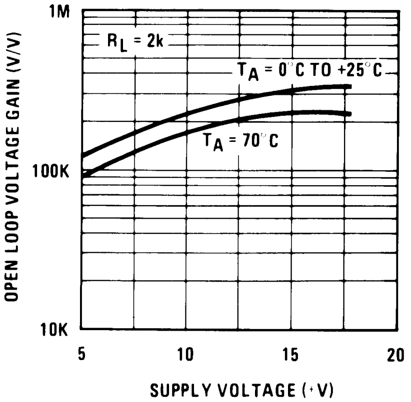

Figure 20.

Output Impedance

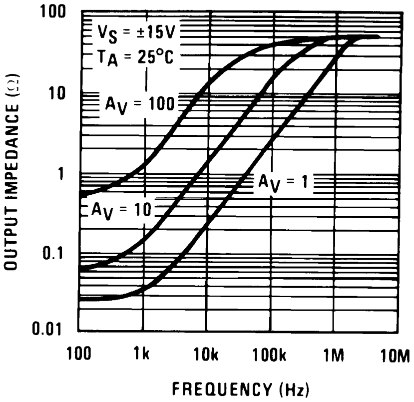

Figure 21.

Inverter Setting Time

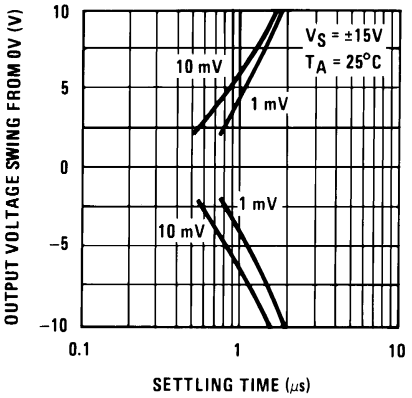

Figure 22.

Pulse Response

Small Signal Inverting

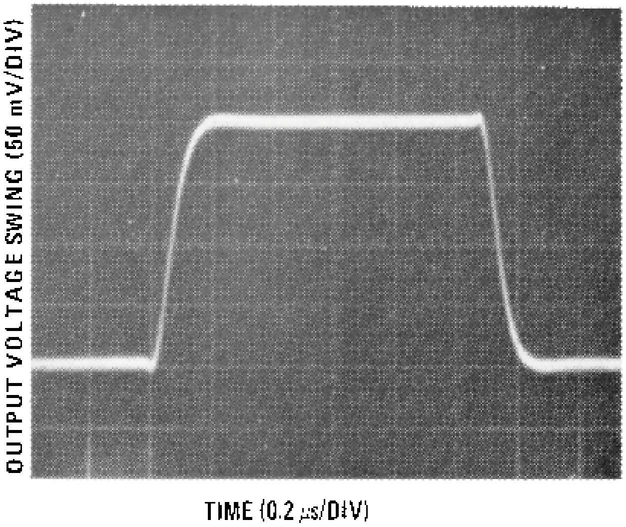

Figure 23.

Large Signal Inverting

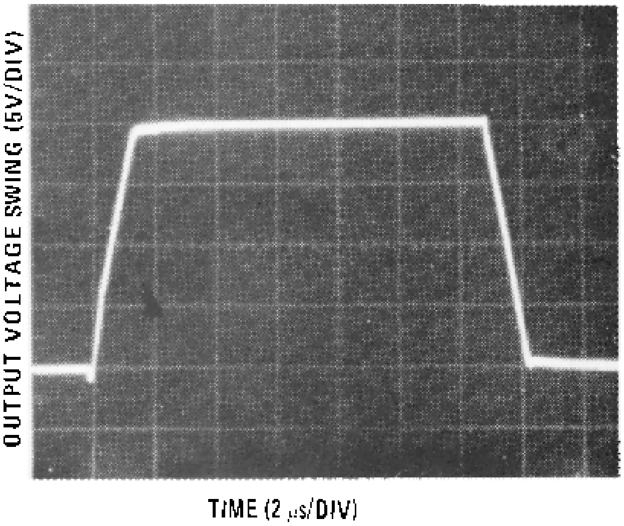

Figure 24.

Small Signal Non-Inverting

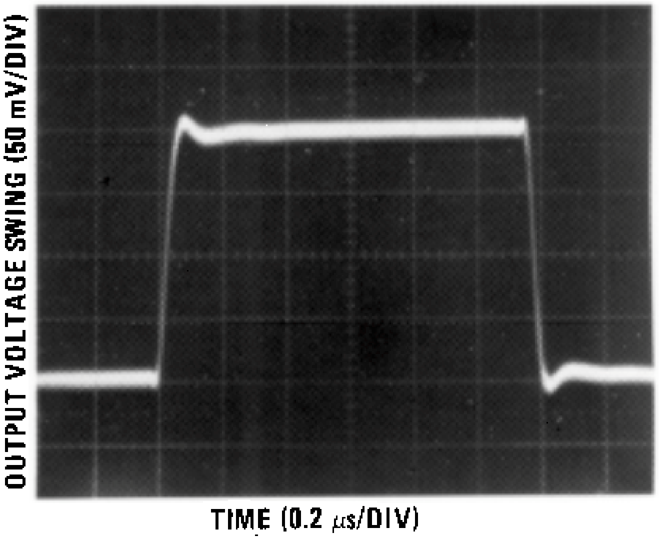

Figure 25.

Large Signal Non-Inverting

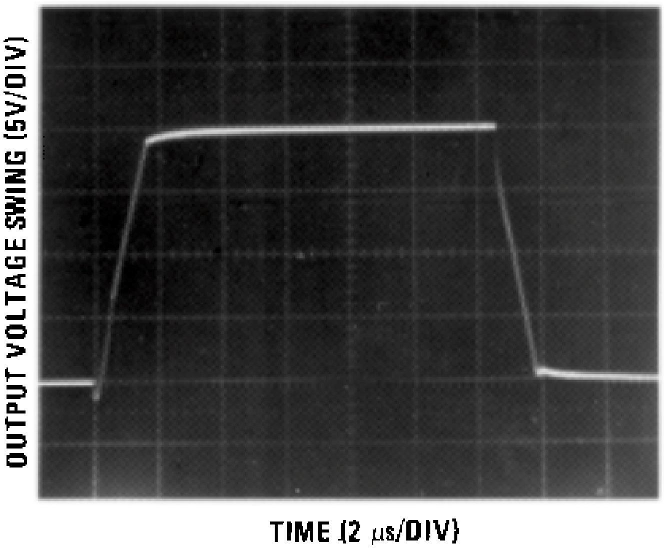

Figure 26.

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Pulse Response (continued)

Current Limit ($R_L = 100\Omega$)

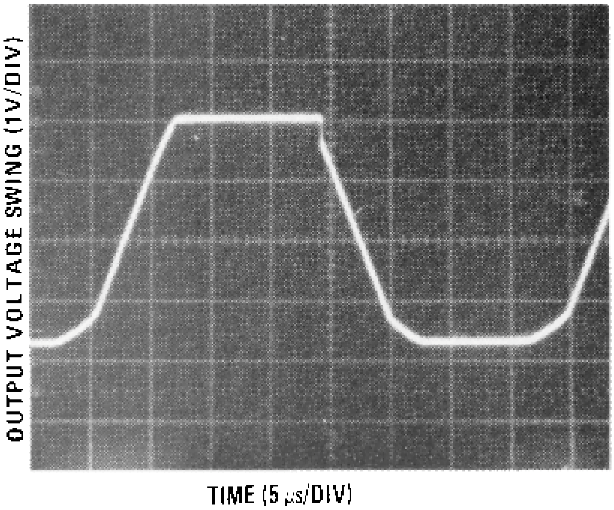

Figure 27.

APPLICATION HINTS

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

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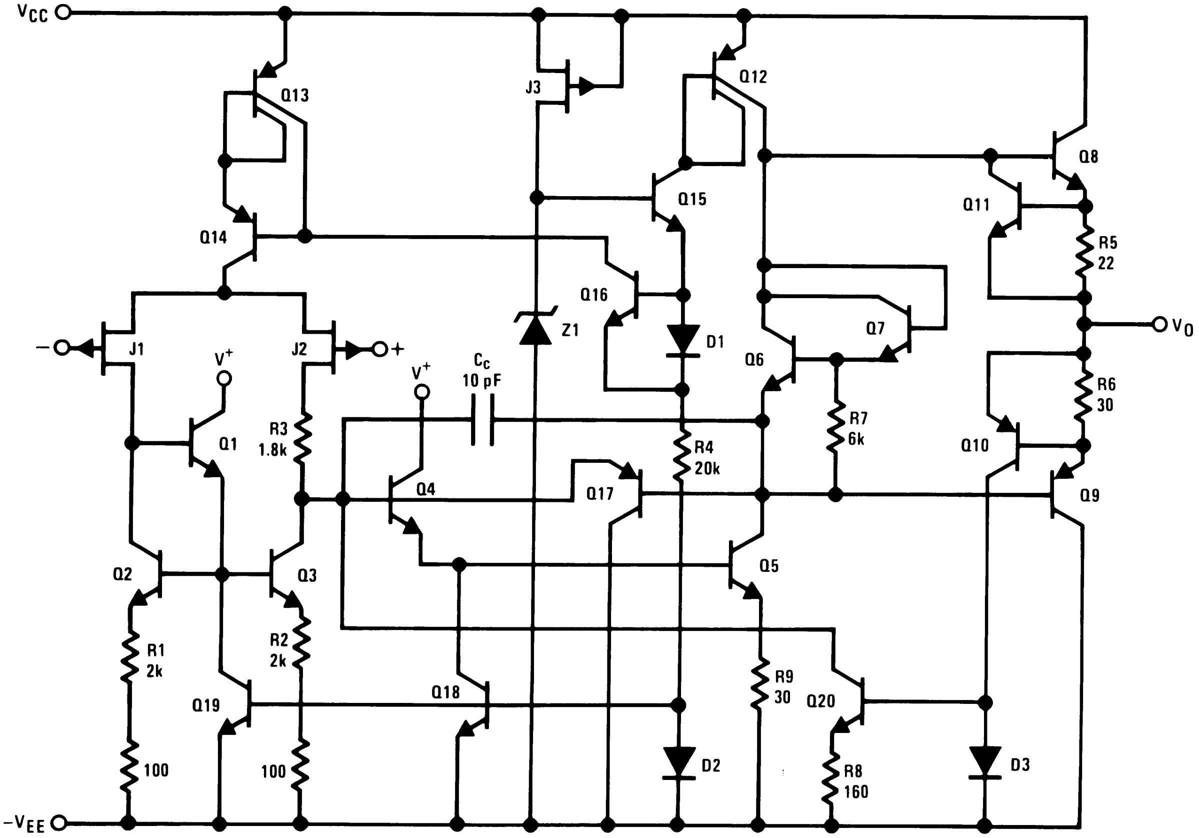
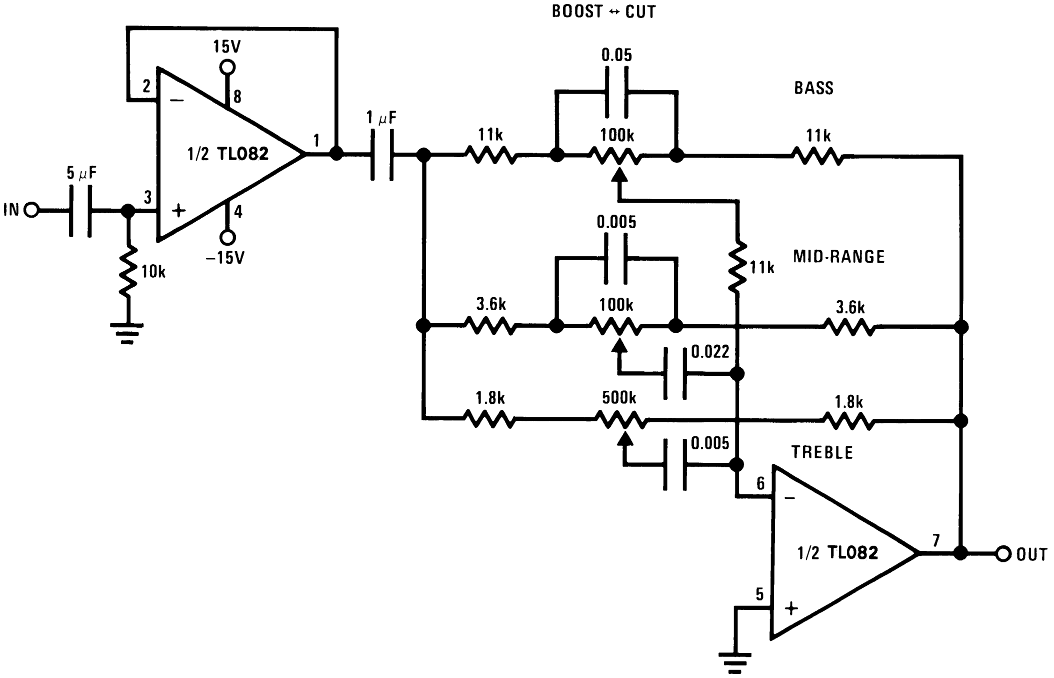
Detailed Schematic



Typical Applications



- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

All controls flat.

Bass and treble boost, mid flat.

Bass and treble cut, mid flat.

Mid boost, bass and treble flat.

Mid cut, bass and treble flat.

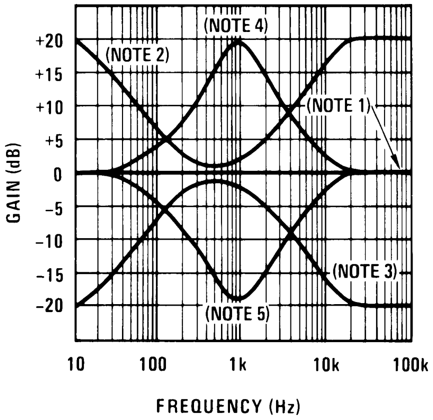


Figure 28. Three-Band Active Tone Control

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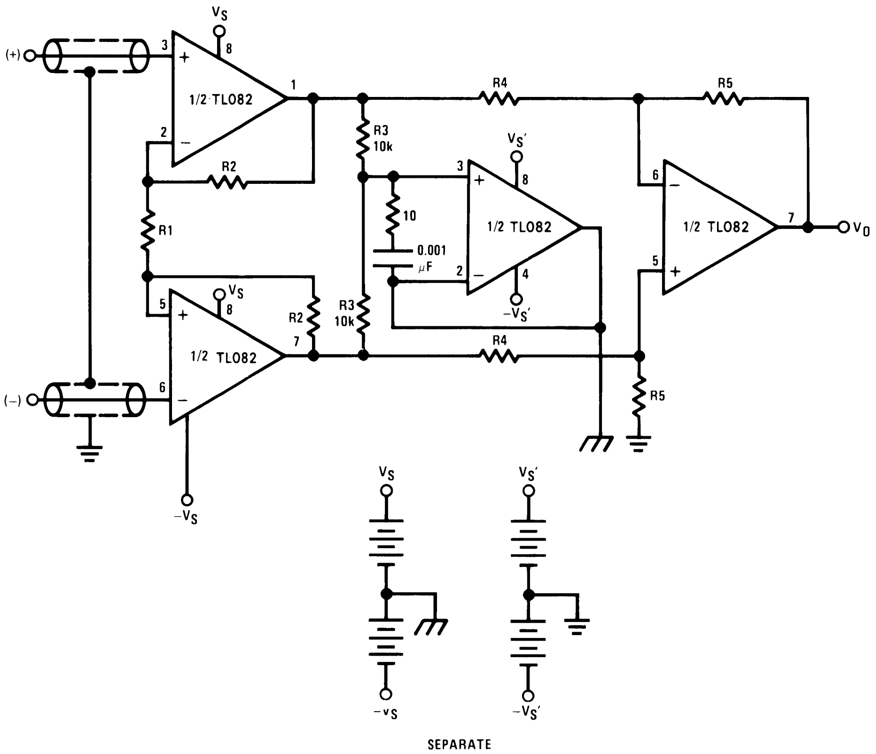
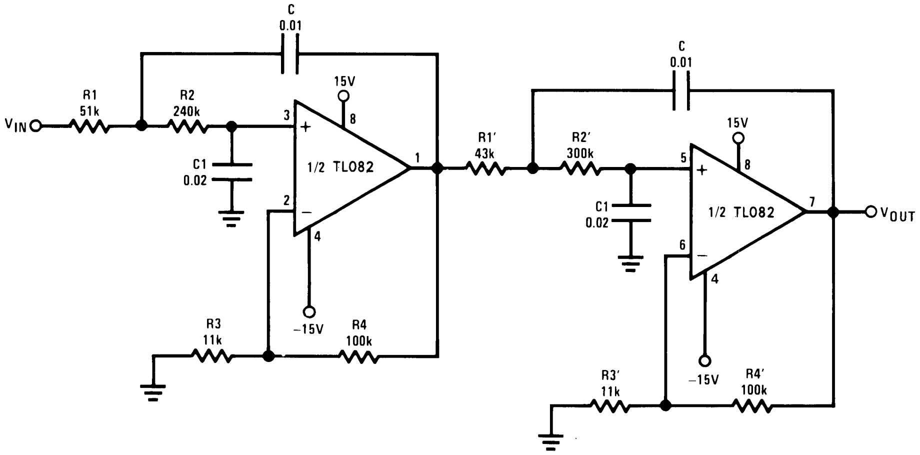


$$A_V = \left(\frac{2R2}{R1} + 1\right)\frac{R5}{R4}$$

⏚ and are separate isolated grounds
Matching of R2's, R4's and R5's control CMRR
With A_{VT} = 1400, resistor matching = 0.01%: CMRR = 136 dB

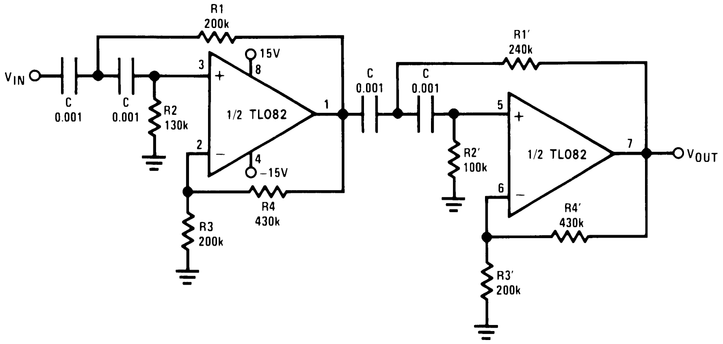
- Very high input impedance
- Super high CMRR

Figure 29. Improved CMRR Instrumentation Amplifier



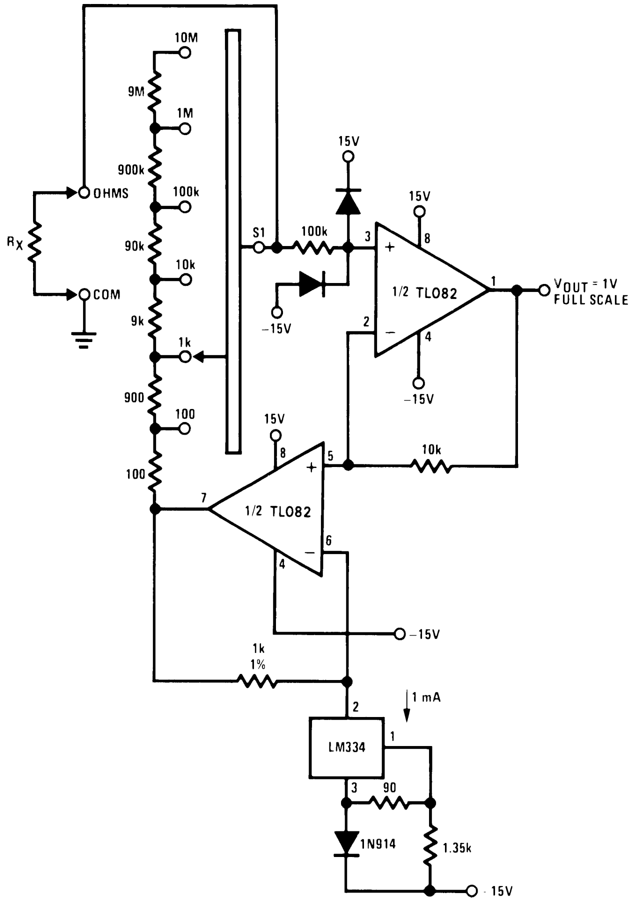
- Corner frequency (f_C) $= \sqrt{\frac{1}{R1R2CC1}} \bullet \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \bullet \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

Figure 30. Fourth Order Low Pass Butterworth Filter



- Corner frequency (f_C) $= \sqrt{\frac{1}{R1R2C^2}} \bullet \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \bullet \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Figure 31. Fourth Order High Pass Butterworth Filter



$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the TL082CP.

Figure 32. Ohms to Volts Converter

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	15

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL082CM/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	TL 082CM
TL082CM/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	TL 082CM
TL082CMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	TL 082CM
TL082CMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	TL 082CM
TL082CP/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	TL082 CP
TL082CP/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	TL082 CP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TL082-N :

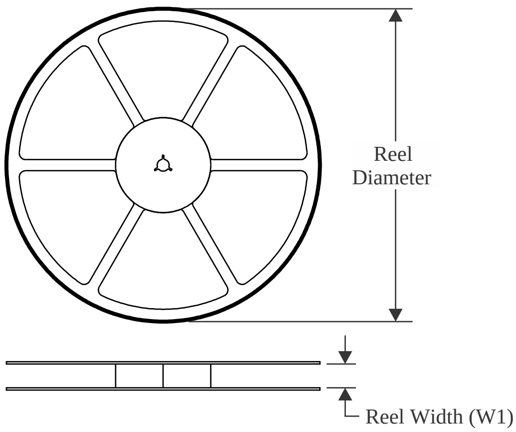
- Automotive : TL082-Q1

NOTE: Qualified Version Definitions:

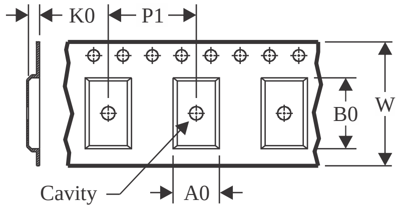
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

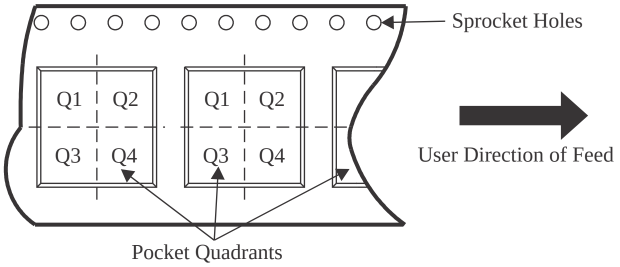


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

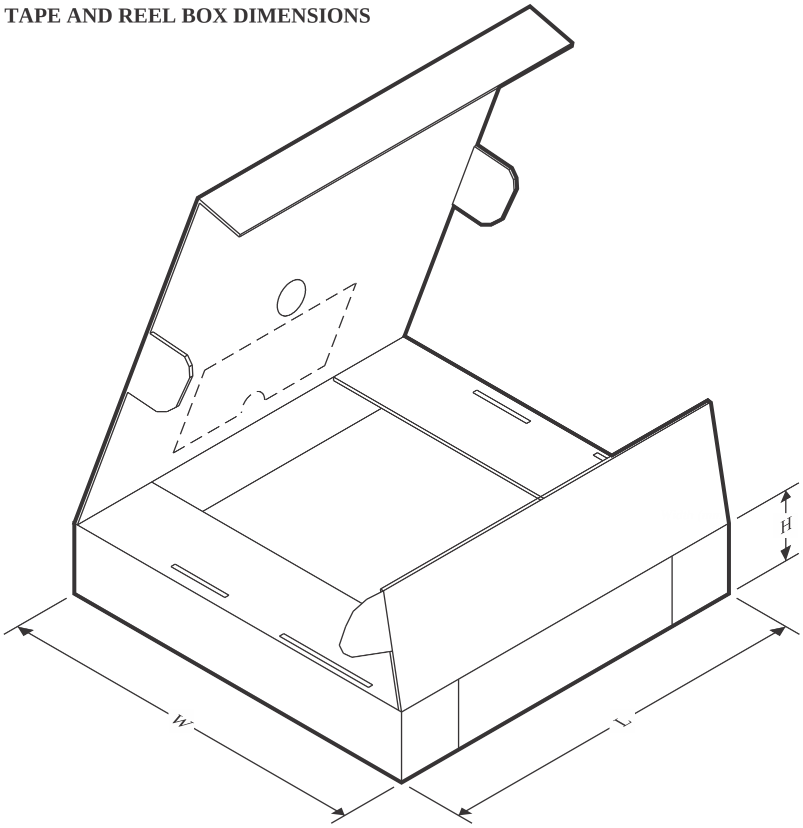
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL082CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

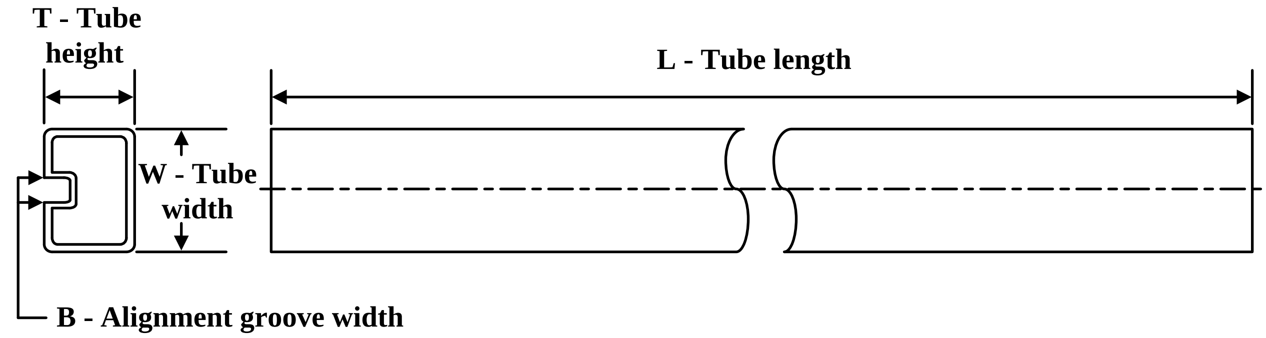
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



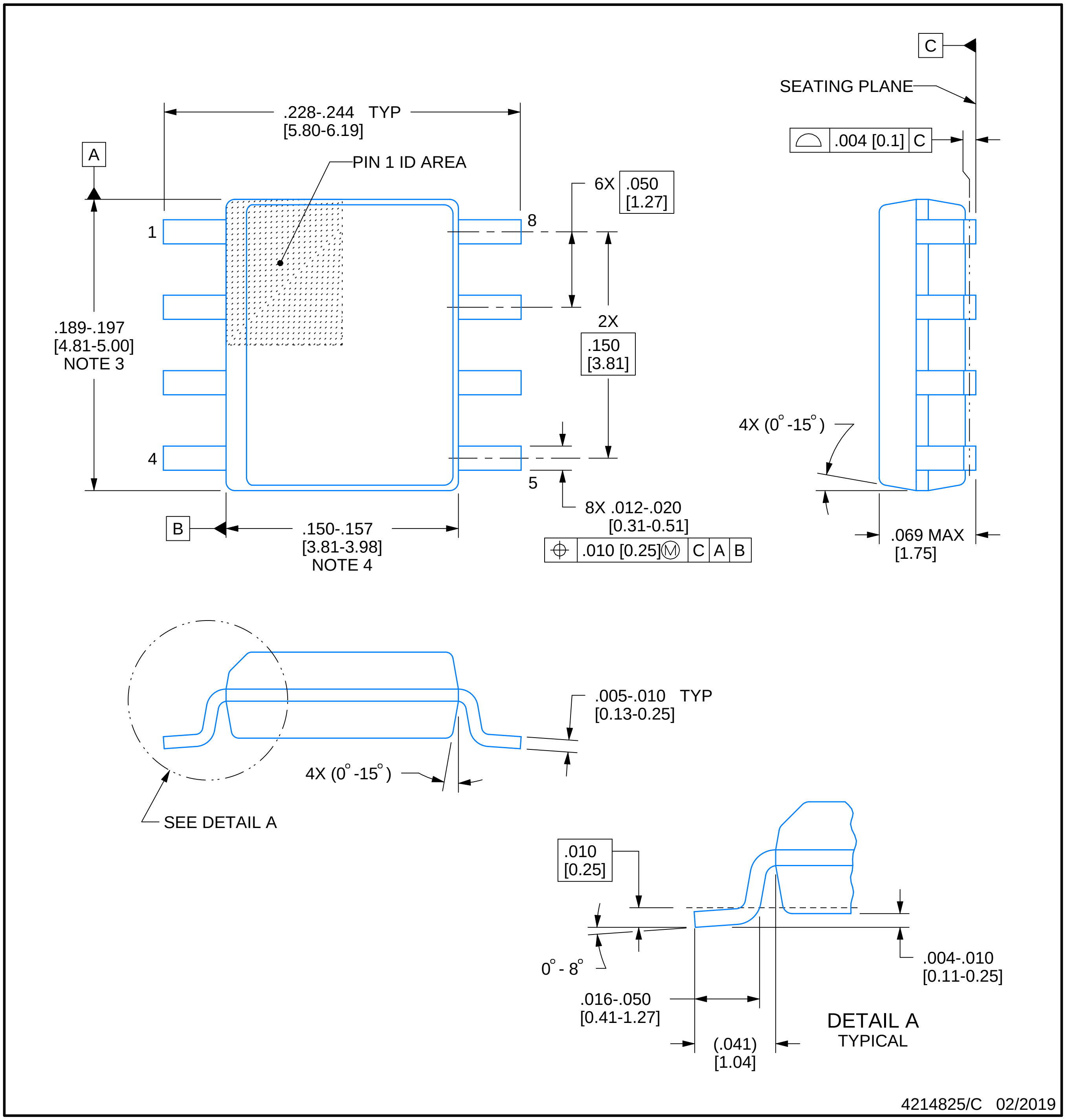
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL082CM/NOPB	D	SOIC	8	95	495	8	4064	3.05
TL082CM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
TL082CP/NOPB	P	PDIP	8	40	502	14	11938	4.32
TL082CP/NOPB.B	P	PDIP	8	40	502	14	11938	4.32

D0008A

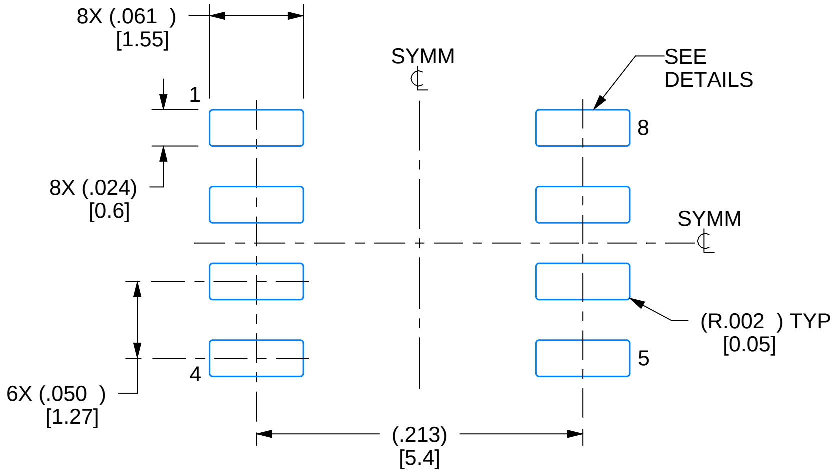
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

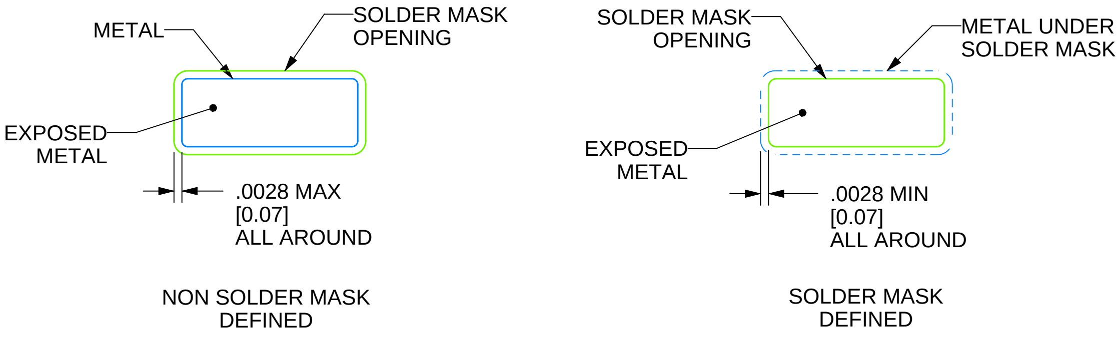


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



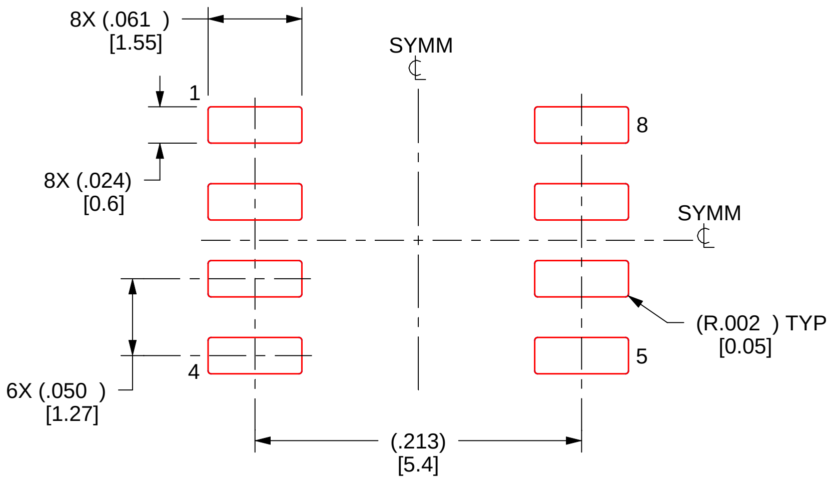
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

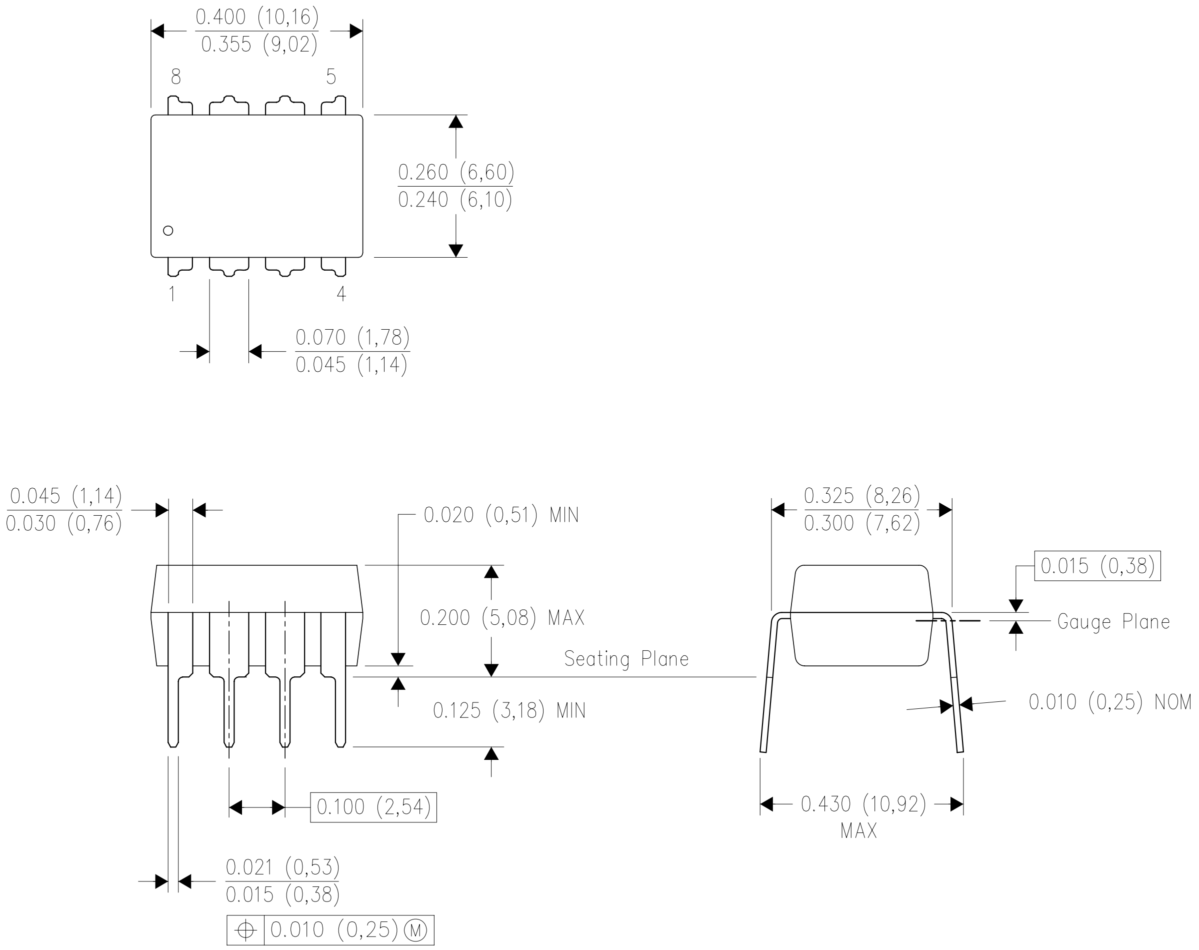


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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