# THVD8000T RS-485 Transceiver with OOK Modulation and Extended Temperature Range for Power Line Communication

## 1 Features

- 3V to 5.5V supply voltage
- Half-duplex communication
  - Up to 500kbps data rate with $f_0$ / bps = 10
  - Higher data rates are possible with $f_0$ / bps < 10
- RS-485 electrical signaling with on-off keying (OOK) modulation
- Pin selectable carrier frequency: 125kHz to 5MHz
- Spread spectrum clocking for excellent EMI performance
- Polarity free
- TX timeout to avoid stuck bus conditions
- Operational common-mode range: –7V to 12V
- Bus I/O protection
  - ± 18V DC fault protection
  - ± 16kV HBM ESD
  - ± 8kV IEC 61000-4-2 contact discharge
  - ± 15kV IEC 61000-4-2 air gap discharge
  - ± 4kV IEC 61000-4-4 fast transient burst
- Extended temperature range: −55°C to 125°C
- 8-Pin SOT-23 package for space constrained applications

## 2 Applications

- HVAC systems
- Building automation
- Factory automation & control
- Appliances
- Lighting
- Grid infrastructure
- Power delivery

## 3 Description

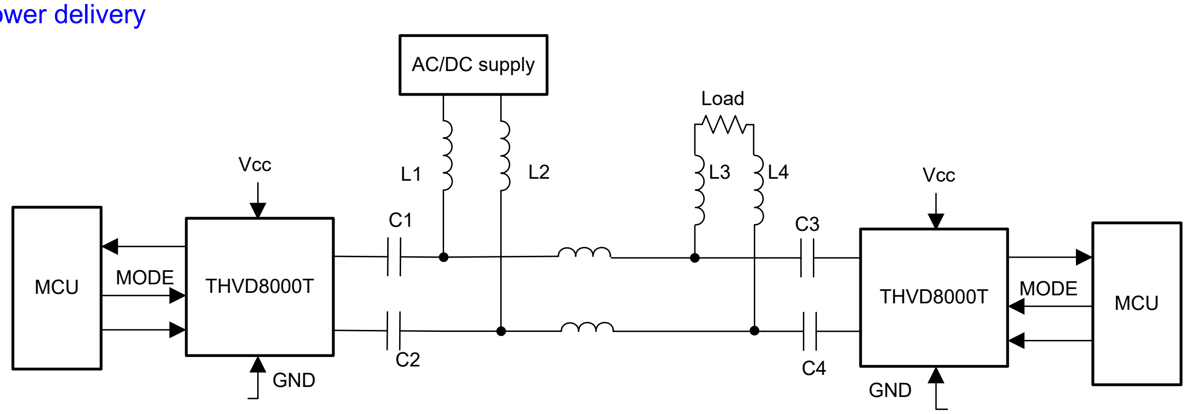
THVD8000T is an RS-485 transceiver with on-off keying (OOK) modulation and demodulation built in for power line communication. Modulating data onto existing power lines allows power delivery and data communication to share a common pair of wires, resulting in a reduction of the system cost.

A pin programmable interface simplifies the system design. The carrier frequency can be adjusted by changing an external resistor on the F_SET pin. A broad range of carrier frequencies gives the system designer the flexibility to choose the external inductors and capacitors. OOK modulation also operates with immunity to data polarity for ease of system installations.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| THVD8000T | SOT-23-THN (8) | 2.9mm × 2.8mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Simplified Schematic**

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# 4 Pin Configuration and Functions

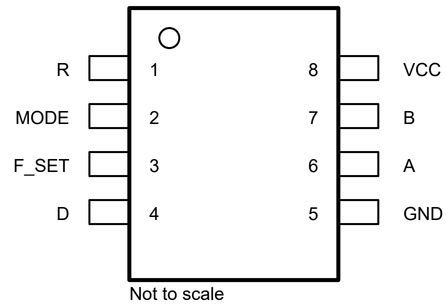



**Figure 4-1. DDF Package, 8-Pin SOT-23 (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| R | 1 | Digital output | In receiver mode, R pin operates as an output, in transmit mode, it enters a high impedance state. Pull-up resistor is recommended if the MODE pin is toggled. |
| MODE | 2 | Digital input | Transmit and receive mode selection. Low = receive mode; High = transmit mode. 2MΩ pull-down to GND |
| F_SET | 3 | Analog input | Carrier frequency selection. Use a resistor to GND to select a frequency. |
| D | 4 | Digital input | Driver data input, 2MΩ pull-up to $V_{CC}$ |
| GND | 5 | Ground | Device ground |
| A | 6 | Bus input/output | Bus I/O port A (complementary to B) |
| B | 7 | Bus input/output | Bus I/O port B (complementary to A) |
| $V_{CC}$ | 8 | Power | 3.3V to 5V device supply |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

see [(1)]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | –0.5 | 7 | V |
| $V_L$ | Input voltage at any logic pin (D, MODE or F_SET) | –0.3 | 5.7 | V |
| $V_A$, $V_B$ | Voltage at A or B inputs (differential or with respect to GND) | –18 | 18 | V |
| $I_O$ | Receiver output current | –24 | 24 | mA |
| $T_J$ | Junction temperature | | 170 | °C |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 5.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] | A and B pins to GND | ±16,000 | V |
| | | | All pins | ±4,000 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)] | All pins | ±1,500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 ESD Ratings - IEC Specifications

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | IEC 61000-4-2 ESD contact discharge, A and B pins to GND | ±8 | kV |
| | | IEC 61000-4-2 ESD air gap discharge, A and B pins to GND | ±15 | |
| | | IEC 61000-4-4 electrical fast transient, A and B pins to GND | ±4 | |

## 5.4 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 3 | | 5.5 | V |
| $V_{ID}$ | Input differential voltage (A and B pins) | | –7 | | 12 | V |
| $V_{CM}$ | Operational common mode voltage (A and B pins) | | –7 | | 12 | V |
| $V_{IH}$ | High-level input voltage (D and MODE pins) | | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage (D and MODE pins) | | 0 | | 0.8 | V |
| $I_O$ | Output current | Driver | –60 | | 60 | mA |
| | | Receiver | –4 | | 4 | |
| $R_{F\_SET}$ | Carrier frequency selection resistor | | 1.5 | | 80 | kΩ |
| $\Delta R_{F\_SET}$ | Carrier frequency selection resistor tolerance | | –2 | | 2 | % |
| $1/t_{UI}$ | Data rate | Modulation mode[(1)] | | | $f_0$ / 10 | bps |
| $C_{F\_SET}$ | Recommended load capacitance on F_SET pin | | | | 100 | pF |
| $T_A$ | Operating ambient temperature | | –55 | | 125 | °C |

(1) $f_0$ is the carrier frequency (in Hz) set by the external resistor between F_SET and GND pins.

## 5.5 Thermal Information

| THERMAL METRIC[(1)] | | THVD8000T DDF (SOT-23) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 106.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 38.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 29.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 29.5 | °C/W |
| $\Psi_{JB}$ | Junction-to-top characterization parameter | 29.5 | °C/W |

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.

## 5.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC}$ = 5 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Driver** | | | | | | | |
| $\lvert V_{OD}\rvert$ | Driver differential output voltage magnitude | OOK mode, $R_L$ = 60 Ω, –7 V ≤ $V_{test}$ ≤ 12 V, Measured at 2nd pulse | See Figure 6-1 | 1.5 | 3.5 | | V |
| | | OOK mode, $R_L$ = 100 Ω, $C_L$ = 50 pF, Measured at 2nd pulse | See Figure 6-1 | 2 | 4 | | |
| | | OOK mode, $R_L$ = 54 Ω, $C_L$ = 50 pF, Measured at 2nd pulse | See Figure 6-1 | 1.5 | 3.5 | | |
| $V_{OC}$ | Steady state common-mode output voltage | OOK mode, $R_L$ = 60 Ω, $C_L$ = 50 pF | See Figure 6-2 | 1 | $V_{CC}$ / 2 | 3 | V |
| $\Delta V_{OC}$ | Change in differential driver common-mode output voltage | OOK mode, $R_L$ = 60 Ω, $C_L$ = 50 pF | See Figure 6-2 | -160 | | 160 | mV |
| $V_{OC(PP)}$ | Peak-to-peak driver common-mode output voltage | OOK mode, $R_L$ = 60 Ω, $C_L$ = 50 pF, $V_{CC}$ = 3.3 V and $V_{CC}$ = 5V | See Figure 6-2 | | 425 | | mV |
| $I_{OS}$ | Driver short-circuit output current | OOK mode, MODE = $V_{CC}$, –7 V ≤ [$V_A$ or $V_B$] ≤ 12 V | | –250 | | 250 | mA |
| $f_0$ | Minimum carrier frequency[(1)] | $R_{F\_SET}$ = 77 kΩ | See Figure 6-3 | | 125 | | kHz |
| | Maximum carrier frequency[(1)] | $R_{F\_SET}$ = 1.5 kΩ | | | 5 | | MHz |
| $DCD_{f0}$ | Carrier frequency duty cycle distortion | Measured over the full range of $f_0$ | | –2 | | 2 | % |
| $\Delta f_0$ | Carrier frequency tolerance | Measured with a ±2% tolerant $R_{F\_SET}$ | | –25 | | 25 | % |
| $\Delta f_{SSC}$ | Variation of the carrier frequency for spread spectrum clocking | Measured across the full carrier frequency range | | | ±5 | | % |
| $f_{SSC}$ | Spread spectrum clock rate | | | | 30 | | kHz |

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC}$ = 5 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Receiver** | | | | | | | |
| $I_I$ | Bus input current in receive mode | MODE = GND, $V_{CC}$ = 0 V or 5.5 V | $V_I$ = 12 V | | 75 | 125 | μA |
| | | | $V_I$ = –7 V | –97 | –70 | | |
| $V_{MAG\_ZERO}$ | OOK signal differential swing (magnitude) to detect a zero at the R output | MODE = GND, over full common mode range | 125 kHz | | | 225 | mV |
| | | | 1 MHz | | | 150 | |
| | | | 5 MHz | | | 115 | |
| $V_{MAG\_ONE}$ | OOK signal differential swing (magnitude) to detect a one at the R output | | 125 kHz | 20 | | | mV |
| | | | 1 MHz | 10 | | | |
| | | | 5 MHz | 10 | | | |
| $V_{MAG\_HYS}$ | Receiver differential input voltage threshold hysteresis | | 125 kHz | 40 | | | mV |
| | | | 1 MHz | 20 | | | |
| | | | 5 MHz | 20 | | | |
| **Logic / Control Pins** | | | | | | | |
| $I_{IN}$ | Input current (D, MODE) | $V_O$ = 0 V or $V_{CC}$ | | –5 | | 5 | μA |
| $I_{IN}$ | Input current (F_SET) | $V_O$ = $V_{CC}$ | | | | 55 | μA |
| $V_O$ | Output voltage (F_SET) | $I_O$ = 0 mA | | | 1.4 | | V |
| | | 32 kΩ ≤ $R_{PD}$ ≤ 78 kΩ | | | 785 | | mV |
| $V_{OH}$ | Receiver high-level output voltage | $I_{OH}$ = –4 mA | | $V_{CC}$ – 0.4 | $V_{CC}$ – 0.2 | | V |
| $V_{OL}$ | Receiver low-level output voltage | $I_{OL}$ = 4 mA | | | 0.2 | 0.4 | V |
| $I_{OZ}$ | Receiver high-impedance output current | $V_O$ = 0 V or $V_{CC}$, MODE = 0 | | –1 | | 1 | μA |
| **Device** | | | | | | | |
| $I_{CC}$ | Supply current (quiescent) | OOK transmit mode | D = $V_{CC}$, MODE = $V_{CC}$, resistor between F_SET and GND, no load | | 3.1 | 5 | mA |
| | | OOK receive mode | D = $V_{CC}$, MODE = GND, resistor between F_SET and GND, no load | | 4 | 6 | |
| $T_{SD}$ | Thermal shutdown temperature | | | 160 | 170 | 185 | ℃ |
| $T_{HYS}$ | Thermal shutdown hysteresis | | | | 11 | 15 | ℃ |

(1) See OOK modulation section for the complete carrier frequency range

## 5.7 Power Dissipation Characteristics

Over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC}$ = 5 V.

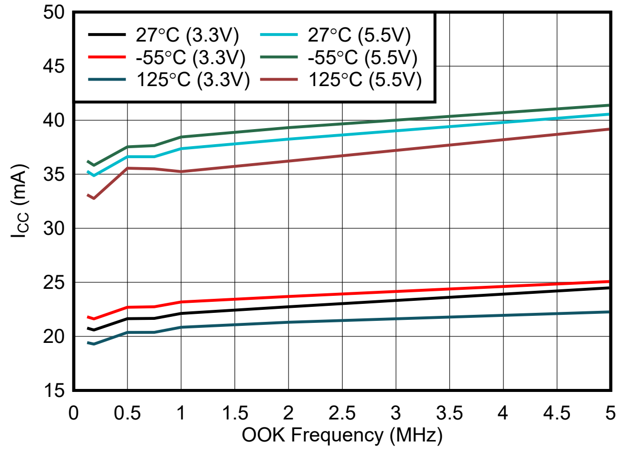
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $PD_{OOK}$ | Chip power dissipation in OOK mode | MODE = $V_{CC}$, $R_L$ = 60 Ω, no $C_L$ | $f_0$ = 125 kHz, 12.5 kHz (25 kbps) clock pattern as data | | 60 | 80 | mW |
| | | | $f_0$ = 5 MHz, 500 kHz (1 Mbps) clock pattern as data | | 90 | 125 | mW |

## 5.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC}$ = 5 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Driver** | | | | | | | |
| $t_r$, $t_f$ | Driver differential output rise and fall times | $R_L$ = 60 Ω, $C_L$ = 50 pF, See Figure 6-4 | | | 10 | 30 | ns |
| $t_{PHL}$, $t_{PLH}$ | Driver propagation delay | | | | 1.2 | 2.5 | Clocks |
| $t_{SK(P)}$ | Driver pulse skew, $\|t_{PHL} – t_{PLH}\|$ | | | | 0.3 | 2.5 | Clocks |
| **Receiver** | | | | | | | |
| $t_r$, $t_f$ | Receiver output rise and fall times | $C_L$ = 15 pF, See Figure 6-5 | | | 1.5 | 16 | ns |
| $t_{PHL}$, $t_{PLH}$ | Receiver propagation delay time | | | | 4 | 6.5 | Clocks |
| $t_{SK(P)}$ | Receiver pulse skew, $\|t_{PHL} – t_{PLH}\|$ | | | | 1.1 | 3 | |
| **Device** | | | | | | | |
| $t_{TX-RX\_OOK}$ | Transmit to receive mode change delay, OOK mode | For all $R_{FSET}$ | Worst case of $t_{TX-RX\_OOK\_ZERO}$ and $t_{TX-RX\_OOK\_ONE}$. See Figure 6-6and Figure 6-7 | | | 14 | clocks |
| $t_{RX-TX\_OOK}$ | Receive to transmit mode change delay, OOK mode | For all $R_{FSET}$ | See Figure 6-8 | | | 12 | clocks |
| $t_{TX\_TIMEOUT}$ | Transmit timeout delay | | | 60 | 110 | | s |

## 5.9 Typical Characteristics




$R_L$ = 60Ω Data rate = $f_0$/10 TX Enabled

**Figure 5-1. ICC vs OOK Frequency**

## 6 Parameter Measurement Information

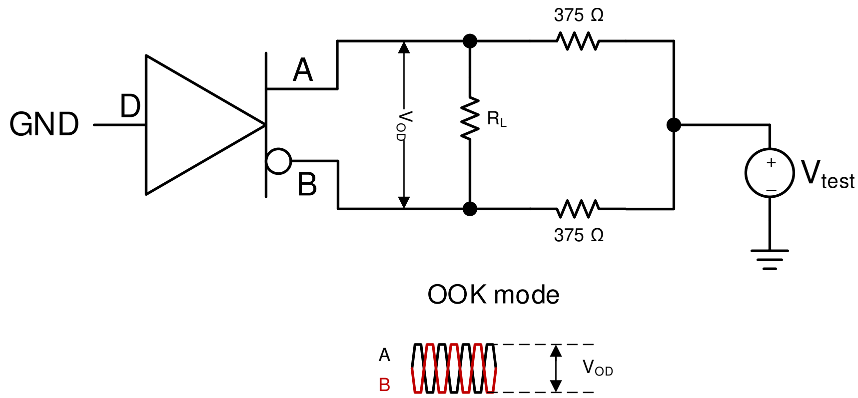



**Figure 6-1. Measurement of Driver Differential Output Voltage With Common-Mode Load**

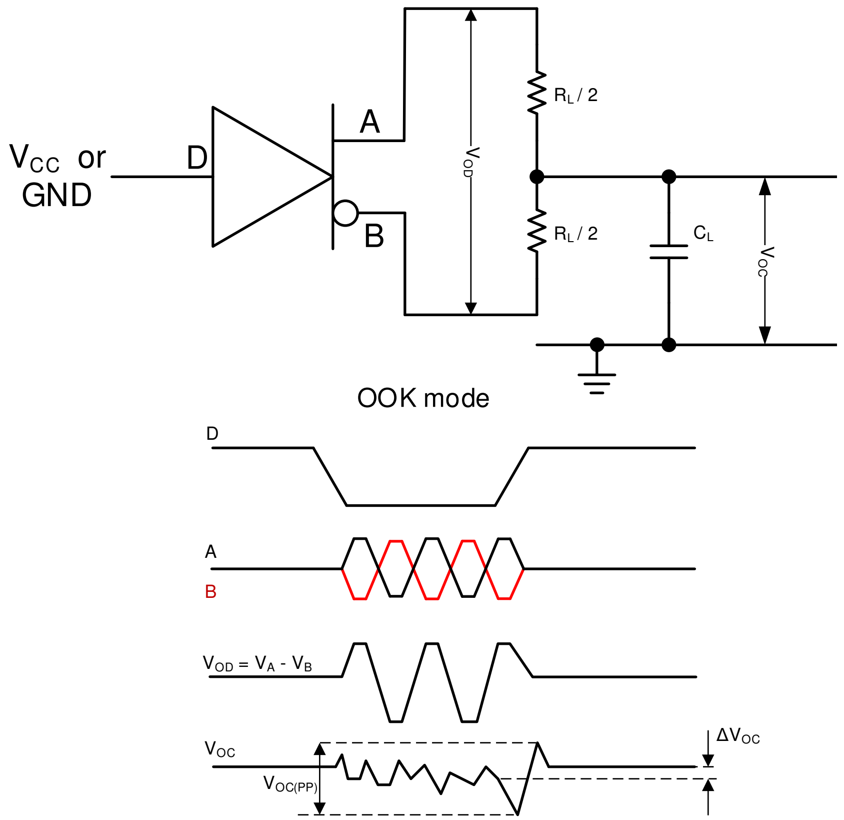



**Figure 6-2. Measurement of Driver Differential and Common-Mode Outputs**

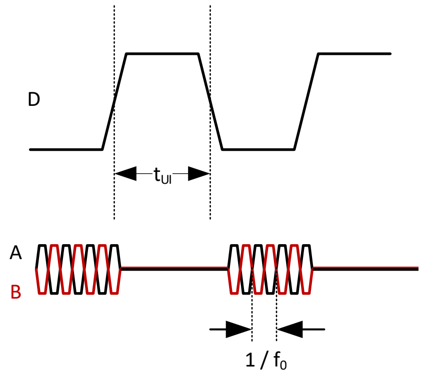



Figure 6-3. Measurement of Carrier Frequency

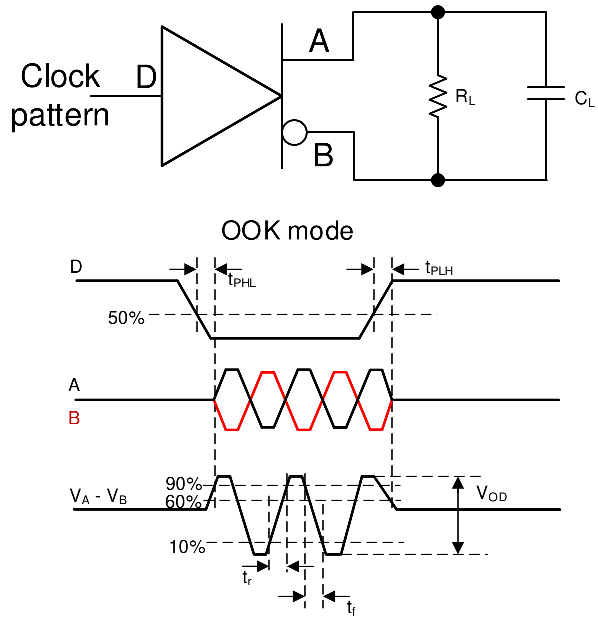



Figure 6-4. Measurement of Driver Switching Characteristics

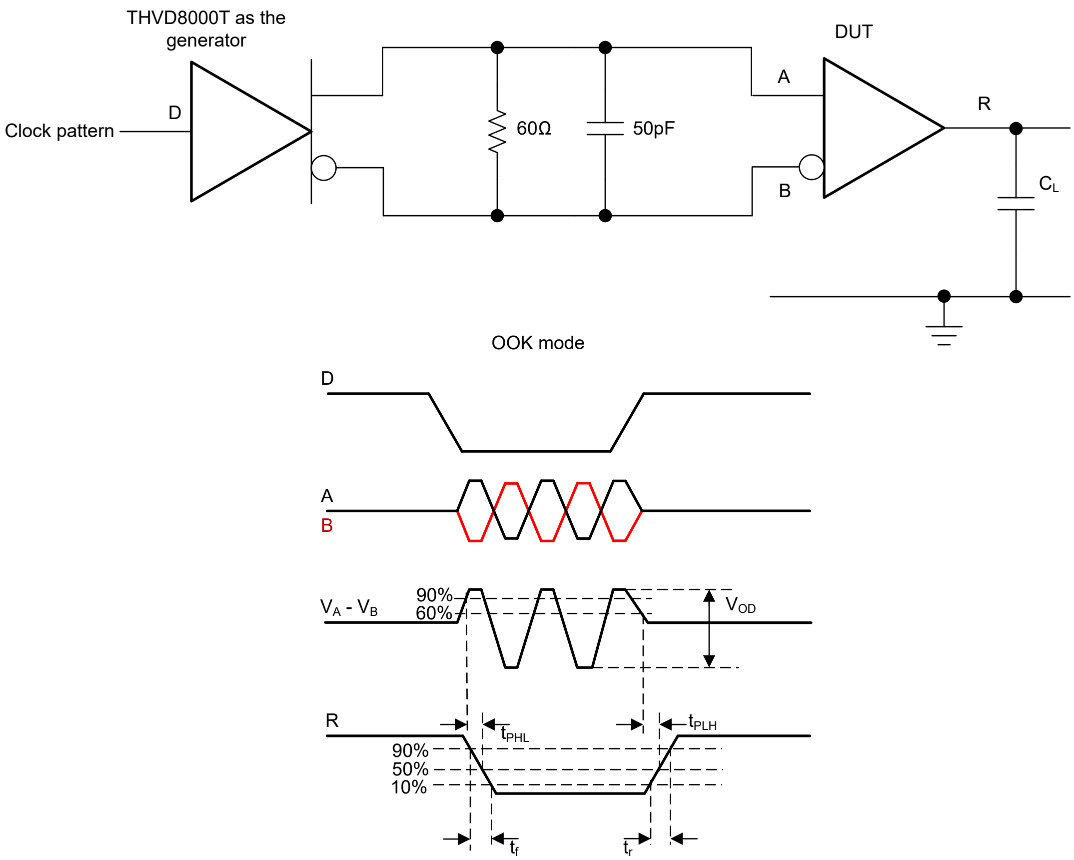



**Figure 6-5. Measurement of Receiver Characteristics**

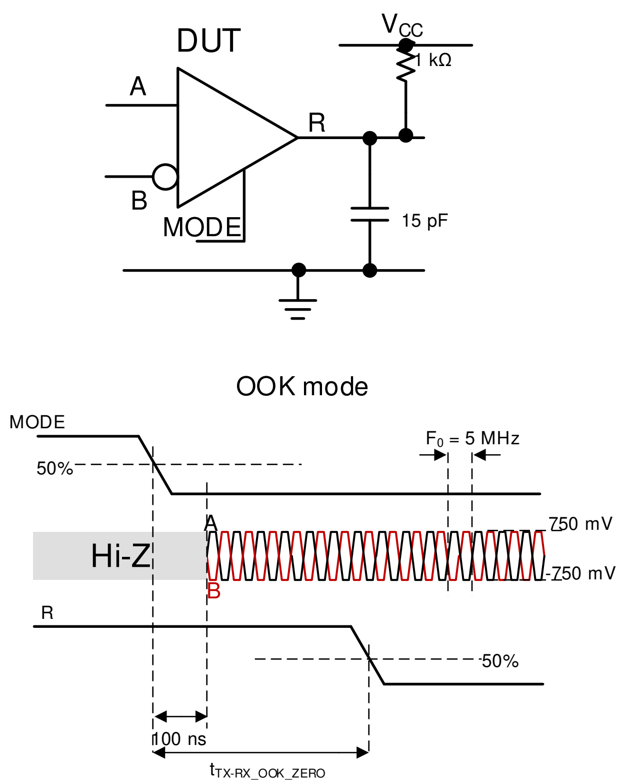



**Figure 6-6. Transmit to Receive Mode Change with Low Output**

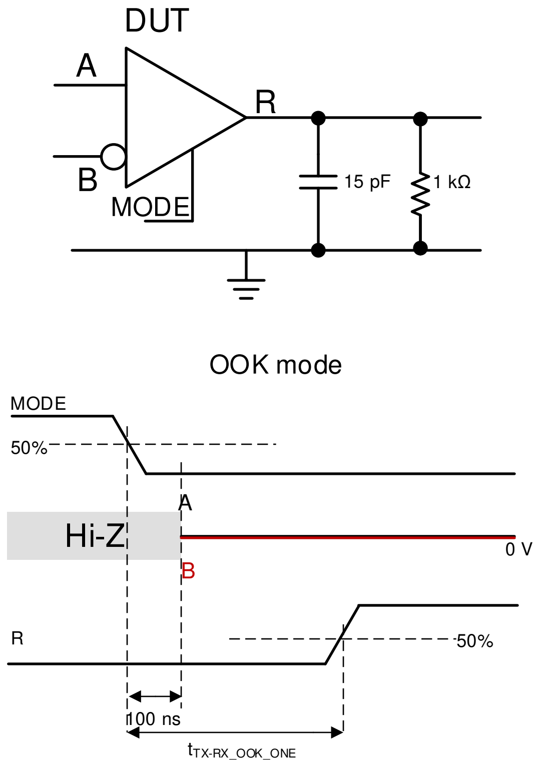



**Figure 6-7. Transmit to Receive Mode Change with High Output**

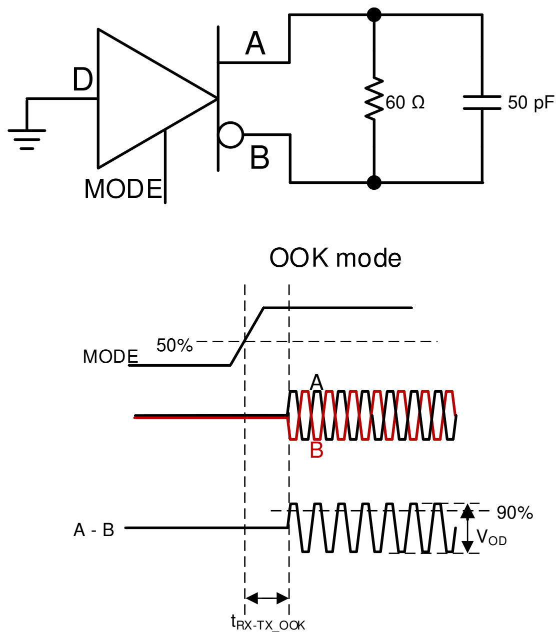


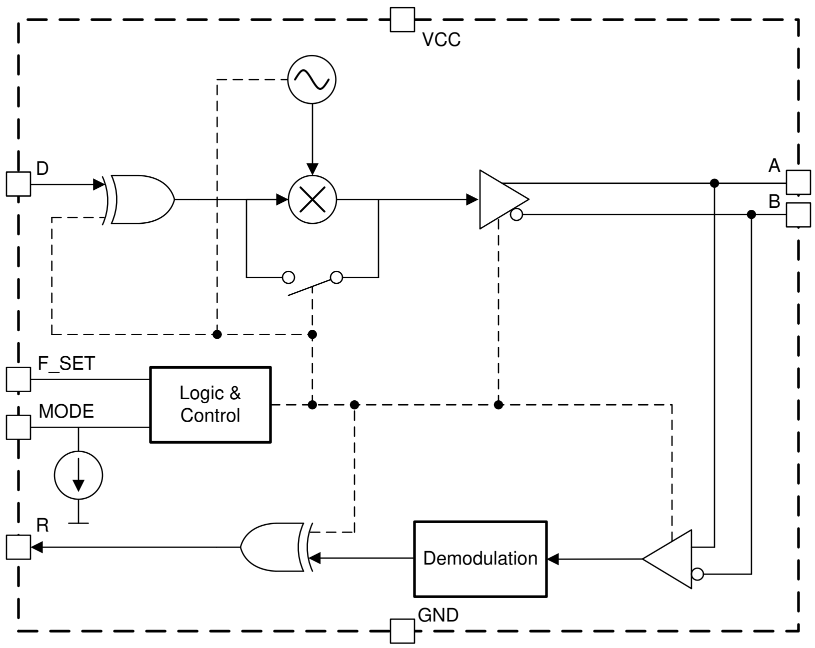

**Figure 6-8. Receive to Transmit Mode Change**

# 7 Detailed Description

## 7.1 Overview

THVD8000T enables power line communication using RS-485 physical layer signaling. An integrated OOK modulator enables RS-485 data to be directly coupled onto existing power cables via series capacitors without any updates to the MCU or the controller. The THVD8000T receiver extracts the data from the power cables through series capacitors by using a precise bandpass filter and a demodulator.

## 7.2 Functional Block Diagrams




## 7.3 Feature Description

### *7.3.1 OOK Modulation with F_SET pin*

Data at the D input is modulated with the carrier frequency ($f_0$) via the F_SET pin. Figure 7-1 illustrates the modulation scheme. A high level at the D input is driven to the mid-level with zero differential voltage ($V_{OD}$). A low level at the D input is modulated at the carrier frequency. The recommendation is to use a carrier frequency that is 10x higher than the data rate. Higher data rates are possible at the expense of increased pulse width distortion with the use of lower ratios.

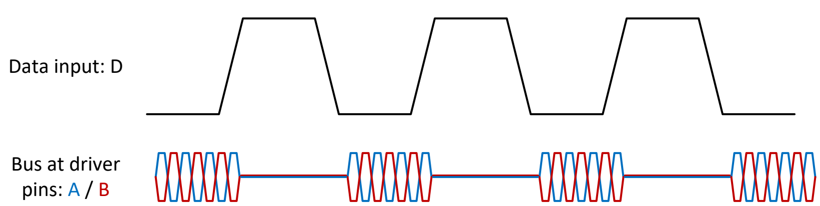



**Figure 7-1. OOK Modulation Scheme**

$f_0$ is programmable by changing the external resistor ($R_{F\_SET}$) value connected to ground. Table 7-1 shows the carrier frequency for the each recommended resistor value.

The oscillator used to generate the carrier frequency features spread spectrum clocking to reduce emissions.

**Table 7-1. OOK $f_0$ versus $R_{F\_SET}$**

| $R_{F\_SET}$ (kΩ) | OOK $f_0$ (kHz) |
|---|---|
| 77 | 125 |
| 50 | 187.5 |
| 19 | 500 |
| 12.5 | 750 |
| 9.3 | 1000 |
| 4.4 | 2000 |
| 1.5 | 5000 |

### 7.3.2 OOK Demodulation

The OOK signal received at the A and B inputs go through a bandpass filter and a peak detector to regenerate the original data stream. Figure 7-2 shows the OOK input and the R output waveforms. The bandpass filter characteristics adapts to optimal settings automatically based on the carrier frequency, set via $R_{F\_SET}$.

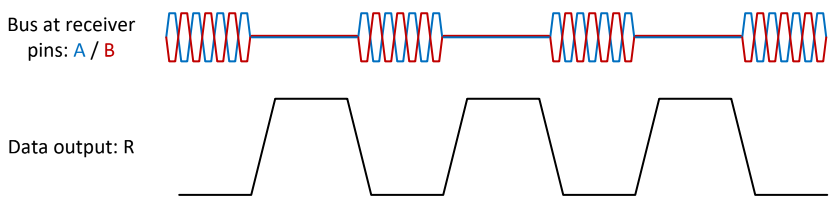



**Figure 7-2. OOK Demodulation**

### 7.3.3 Transmitter Timeout

The driver path incorporates a timeout feature to prevent a faulty node from occupying the bus indefinitely in a multi-drop application.

The driver stops transmitting and the outputs go high impedance if the D input does not detect an edge (either rising or falling) for longer than $t_{TX\_TIMEOUT}$. One of the following events brings the device back to normal operation.

- Any edge at D input
- Toggle MODE pin

The transmit path resumes operation within $t_{MODE}$.

### 7.3.4 Polarity Free Operation

THVD8000T is immune to A and B polarity at the receiver input in OOK mode. The receiver data comparator only checks for the receive input signal magnitude, ignoring the polarity, to determine the logic level. Note that reversing the polarity does result in degraded pulse width distortion.

### 7.3.5 Glitch Free Mode Change

The device incorporates a delay of up to $t_{MODE}$ when changing the state of the MODE pin. This feature makes sure there are no glitches at the A, B and R outputs when transitioning between transmit and receive modes.

### 7.3.6 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceiver against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±8kV contact and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4kV. This integrated protection eliminates the need of external components reducing the system BOM.

## 7.4 Device Functional Modes

**Table 7-2. THVD8000T Functional Modes**

| F_SET Configuration | Device Functional Mode |
|---|---|
| $R_{F\_SET}$ between F_SET and GND | OOK mode, $f_0$ set by the $R_{F\_SET}$ value |
| F_SET at high impedance | Invalid, not recommended for normal operation |
| F_SET at $V_{CC}$ | |
| F_SET short to GND | |

### *7.4.1 OOK Mode*

Data at the D input is modulated with the carrier frequency set by the $R_{F\_SET}$ value when the device is transmitting (MODE = $V_{CC}$). See Section 7.3.1 section for more details. In receiving (MODE = GND), the device expects an OOK modulated signal at the A and B inputs. The data is demodulated and sent out via R pin. See Section 7.3.2 section for more details.

**Table 7-3. Driver function table for OOK mode**

| INPUTS | | | OUTPUTS | | FUNCTION |
|---|---|---|---|---|---|
| F_SET | MODE | D | A | B | |
| $R_{F\_SET}$ (See Table 7-1) | H | H or Z | Bias to $V_{CM}$ | Bias to $V_{CM}$ | Driver is actively biased to $V_{CM}$ on the bus |
| | H | L | Oscillating | Oscillating | Bus actively driven at carrier frequency |
| | L or Z | X | Z | Z | Driver disabled, device in receive mode |

**Table 7-4. Receiver function table for OOK mode**

| INPUTS | | | OUTPUT | FUNCTION |
|---|---|---|---|---|
| F_SET | MODE | Input | R | |
| $R_{F\_SET}$ (See Table 7-1) | L or Z | Oscillating at F_SET and $V_{ID}$ > $V_{MAG\_ZERO}$ | L | Receive valid bus low |
| | L or Z | Oscillating at F_SET and $V_{MAG\_ONE}$ < $V_{ID}$ < $V_{MAG\_ZERO}$ | ? | Receive invalid bus, output indeterminate |
| | L or Z | Oscillating at F_SET and $V_{ID}$ < $V_{MAG\_ONE}$ | H | Receive valid bus high |
| | L or Z | Z / not oscillating | H | Receive valid bus high |
| | L or Z | OPEN, SHORT, IDLE ($V_{ID}$ = 0 V) | H | Failsafe high output |
| | H | X | Z | Receiver disabled, device in transmit mode |

### *7.4.2 Thermal shutdown (TSD)*

The THVD8000T has a protection feature called thermal shutdown. When the junction temperature reaches $T_{SD}$, the device enters thermal shutdown protection mode. This mode disables the driver and receiver outputs, which will halt all communication through the device. Normal operation resume once the junction temperature drops out of thermal shutdown, which is typically $T_{SD}$ - $T_{HYS}$.

# 8 Application Information Disclaimer

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application information

The THVD8000T is able to transmit data over an AC coupled power line pair using On-Off Keying (OOK).

## 8.2 Typical application (OOK mode)

To combine data and power over a single pair of wires, capacitors and inductors are used in a bias-tee configuration. High-frequency differential data is AC-coupled onto the bus lines via series capacitances while power is DC-coupled via series inductance. The values of these components depends on the carrier frequency, number of nodes on the bus, and the power delivery requirements (that is, voltage and total current sourced or consumed by a given node).

The transmitted differential communication signal is AC-coupled onto the power bus as shown below. This configuration provides the advantage that the power transmitted on the bus has little impact on the differential data, allowing for a wide range of voltage and current scenarios. Typical applications are realized with the THVD8000T transmitting over a power bus of 24VDC or 24VAC with currents from 100mA to 1A, but due to the AC-coupling the THVD8000T does not directly see these voltages. For more information, please refer to the THVD8000 design guide.

In Figure 8-1, there is an optional rectifier network pictured on the bus lines. This network of diodes makes sure the node is receives power correctly from the bus wires, even if the lines get swapped.

A termination resistance, $R_T$, is not required for device functionality but can be useful in improving signal integrity in some applications by reducing reflections that can occur at cable ends.

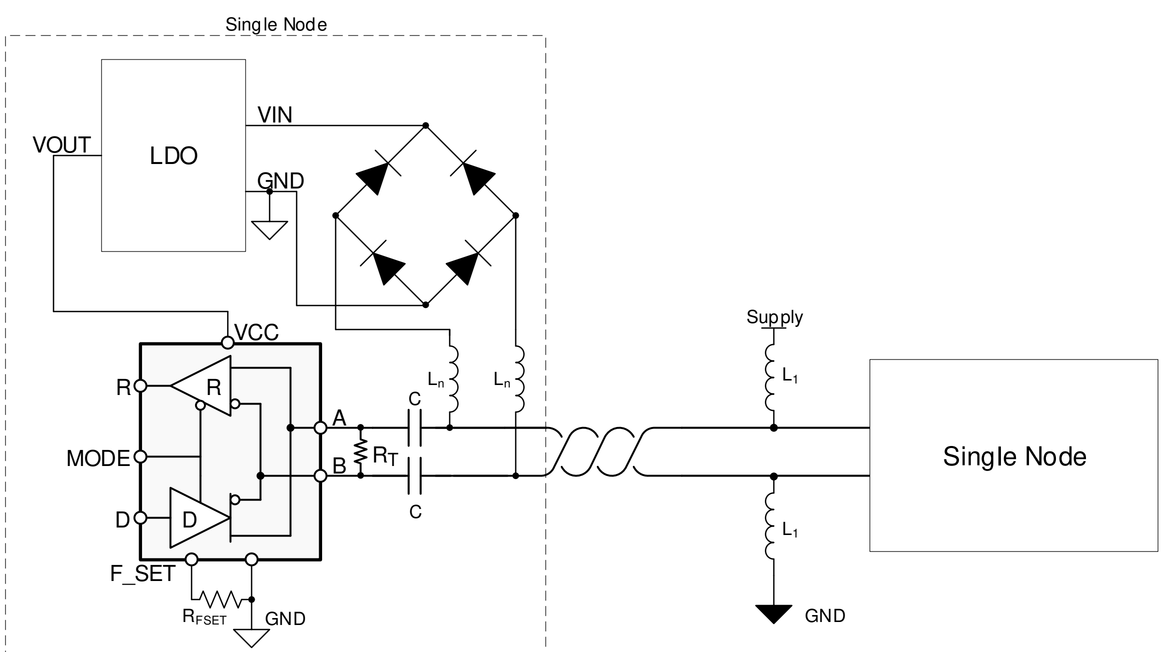



**Figure 8-1. Typical Power Line Network with 2 Nodes**

### 8.2.1 Design requirements

The main requirements are the values of the bus capacitors and the power inductors. Both of these values are dependant upon the carrier frequency selected.

#### 8.2.1.1 Carrier frequency

This device uses on-off-keying to transmit binary data on the bus. Please read Section 7.3.1 for detailed information. The modulation and demodulation of the data can result in pulse width distortion due to asymmetries in low-to-high and high-to-low transition times. These asymmetries are due to factors like synchronization of the data to the internal carrier oscillator in the transmit path and the response time of the band-pass filter in the receive path. The impact of these factors can be minimized by choosing a carrier frequency much higher than the data rate required. A frequency ratio of at least 10:1 is recommended.

### 8.2.2 Detailed design procedure

#### 8.2.2.1 Inductor value selection

Please note the inductor selected must also take power consumption into consideration. The inductor must be sized to handle the maximum anticipated current in addition to the inductance value.

The parallel aggregate impedance should be selected so the total equivalent impedance at the carrier frequency is Z ≥ 375Ω. This assumes RS-485 loading with 60Ω termination. If no termination is used in the application, then the total equivalent impedance at the carrier frequency could be reduced to Z ≥ 60Ω. These examples assume that termination is used. Equation 1 shows the parallel aggregate impedance equation for inductors $L_1$ to $L_n$. Since the inductance value for each node should be the same, the user determines that each nodes impedance is *n* times the total equivalent impedance. For example, if there are 4 nodes connected to the bus and the equivalent impedance is 375Ω, then each node impedance should be 1,500Ω.

$$Z = Z_1 \,||Z_2 \,|| \,..||\, Z_n \tag{1}$$

To determine the suggested inductance value, Equation 2 can be rearranged to determine $L_n$, as shown in Equation 3.

$$Z_n = 2\pi f_0 L_n \tag{2}$$

$$L_n = \frac{Z_n}{2\pi f_0} \tag{3}$$

$f_0$ is the carrier frequency (OOK frequency) used. If the previous 1.5kΩ impedance per node is assumed with a carrier frequency of 1MHz, the resulting inductance limit is approximately 240μH per node. Note that this is the minimum suggested value per node. Refer to Figure 8-2 as a quick reference on the minimum inductance value to achieve 375Ω of total aggregate impedance. The value can be multiplied by the number of nodes on the bus to get the minimum inductance per node. Referring to the previous example, with 4 nodes and a carrier frequency of 1MHz, the minimum aggregate inductance is about 60μH, which is 24μH when multiplied by 4.

#### 8.2.2.2 Capacitor value selection

Capacitor selection is easier than inductor selection, primarily because capacitance impedance is important to allow higher frequency signals through. However, the capacitor ratings for voltage must be carefully selected to meet the application requirements. Special considerations for hot plug nodes should be made to make sure the voltage transients during hot plugging do not exceed the absolute maximum values. See the *Absolute Maximum Ratings.*

The number of nodes on the bus does not play into the capacitance calculation. The impedance of a capacitor is shown in Equation 4.

$$Z = \frac{1}{2\pi f_0 C} \tag{4}$$

Maintaining Z ≤ 5Ω keeps the impedance low enough at the carrier frequency to allow data to pass through. If the equation is rearranged to calculate C, the result is shown in Equation 5.

$$C = \frac{1}{2\pi f_0 Z} \tag{5}$$

If the previous example of a 1MHz carrier frequency is used, then a minimum capacitance value of about 32nF. For a quick reference, refer to Figure 8-3.

#### 8.2.3 Application Curves

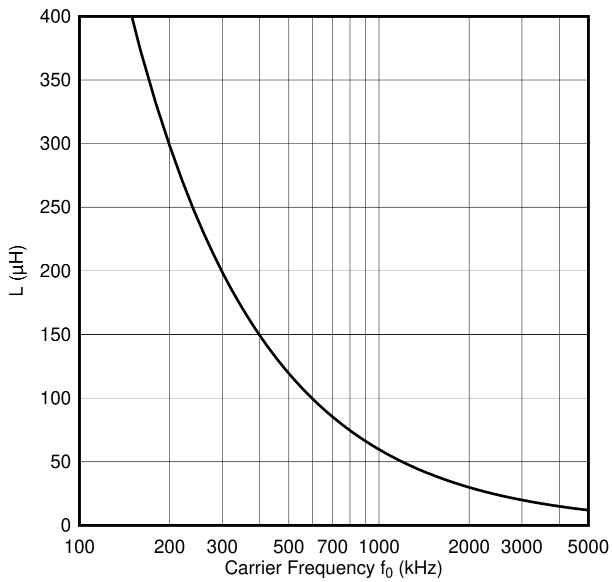



**Figure 8-2. Inductor selection (select values above the line)**

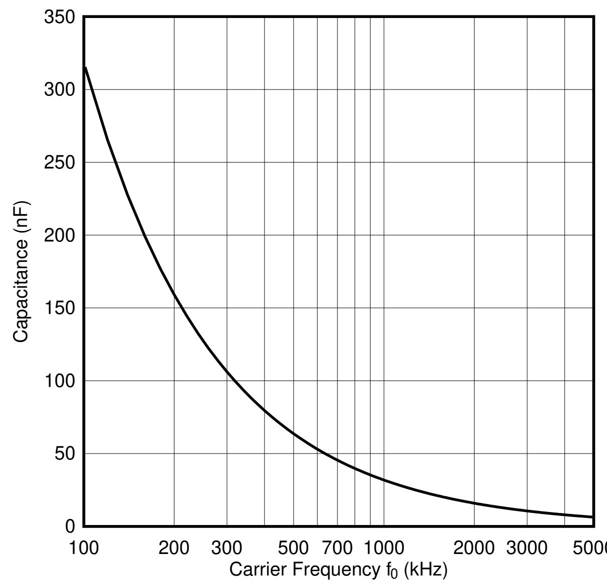



**Figure 8-3. Capacitor selection (select values above the line)**

## 8.3 Power supply recommendations

For reliable operation at all data rates and supply voltages, the supply should be decoupled with a 100nF to 220nF ceramic capacitor and a 1µF capacitor (for ESD sensitive designs) located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

## 8.4 Layout

### 8.4.1 Layout guidelines

Robust and reliable bus node design often requires the use of external transient protection devices to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3MHz to 300MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use $V_{CC}$ and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Place F_SET components near the pin to keep capacitance load below recommended value
4. Use a pull up or down resistor on mode to set a default state
5. Apply 100nF to 220nF decoupling capacitors as close as possible to the $V_{CC}$ pins of transceiver, UART and/or controller ICs on the board.
6. Use at least two vias for $V_{CC}$ and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
7. Use 1kΩ to 10kΩ pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.
8. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
9. While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1mA.

### 8.4.2 Layout Example

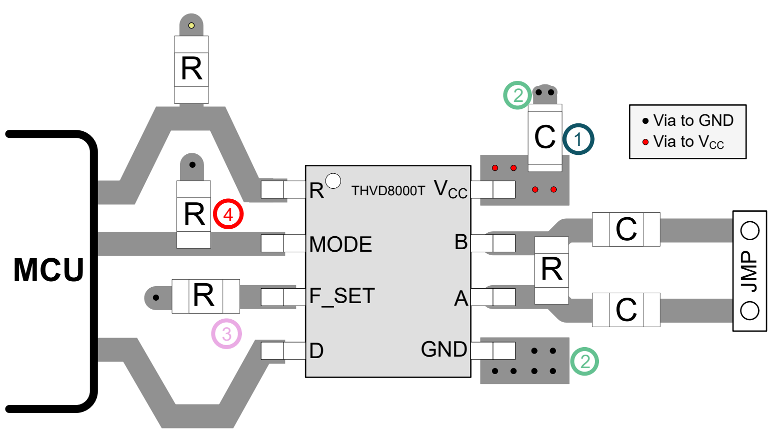



**Figure 8-4. Layout Example (OOK)**

# 9 Device and Documentation Support

## 9.1 Device Support

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

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## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| March 2025 | * | Initial Release |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| THVD8000TDDFR | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | - | 8000T |
| THVD8000TDDFR.A | Active | Production | SOT-23-THIN (DDF) \| 8 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -55 to 125 | 8000T |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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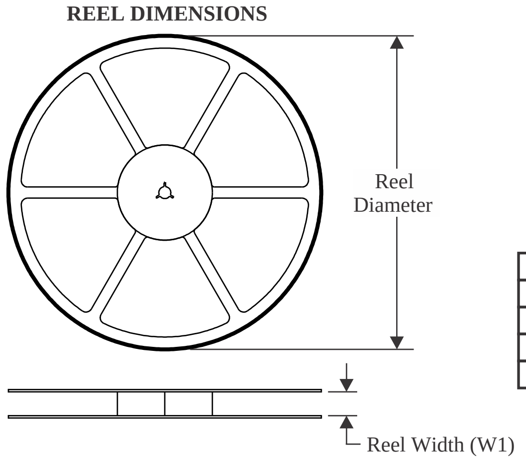
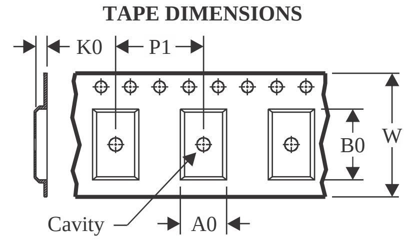
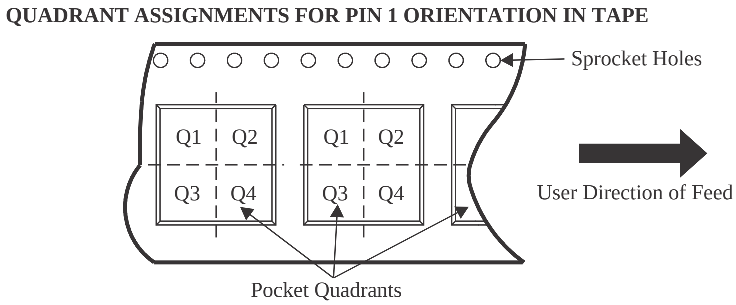
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



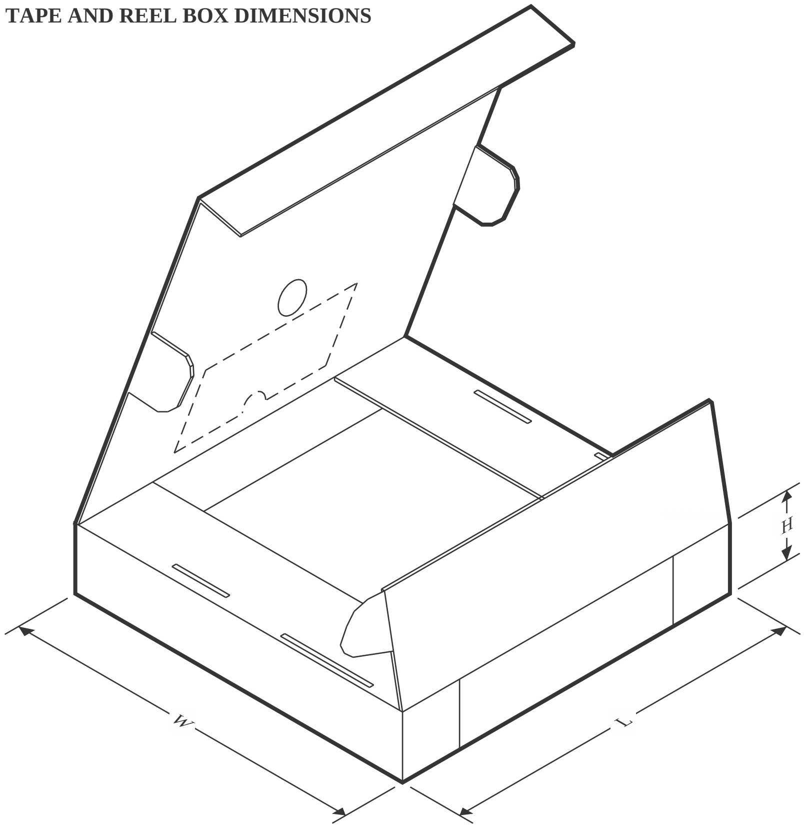

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |




*All dimensions are nominal

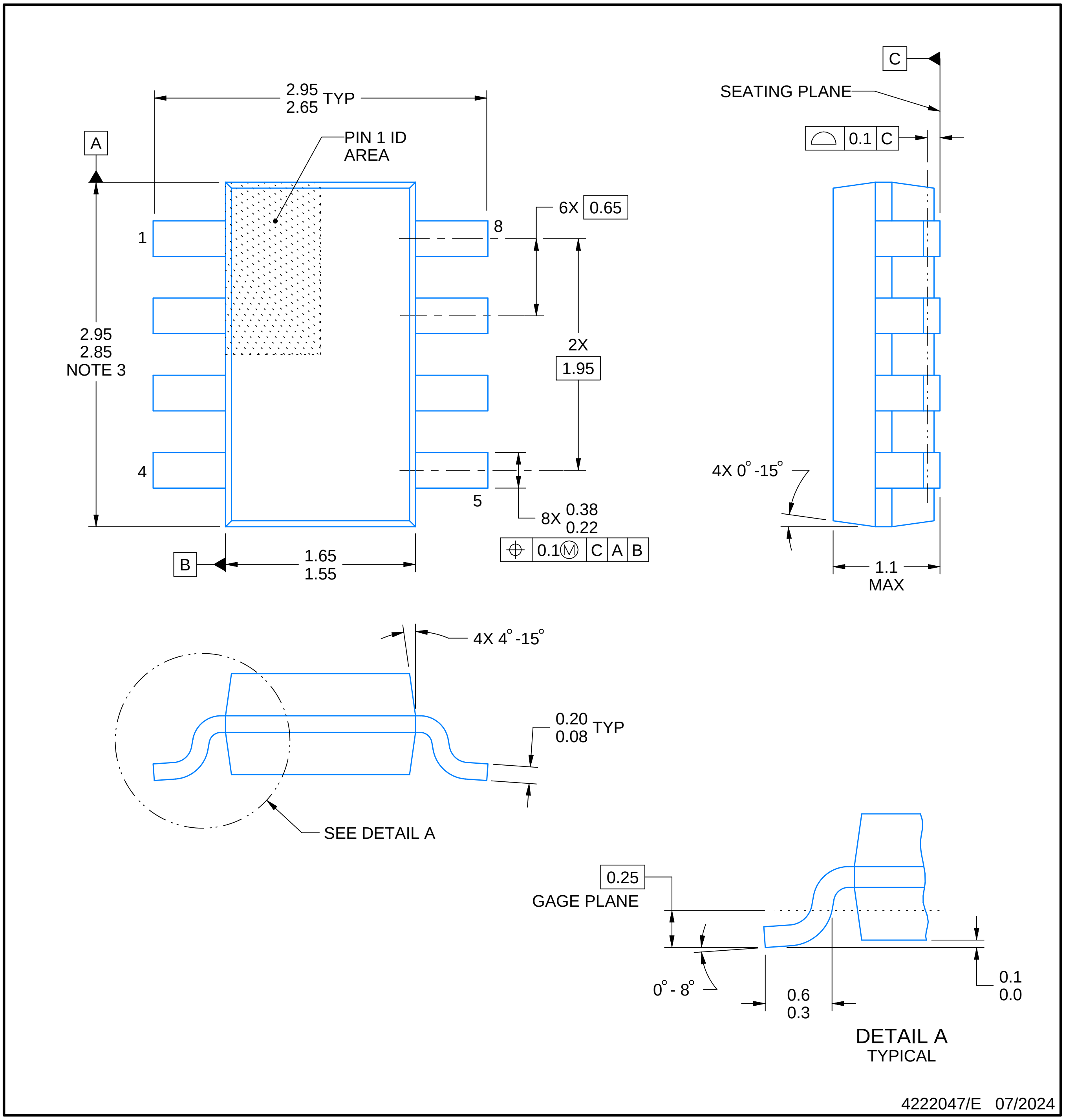
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THVD8000TDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 9.5 | 3.17 | 3.1 | 1.1 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS



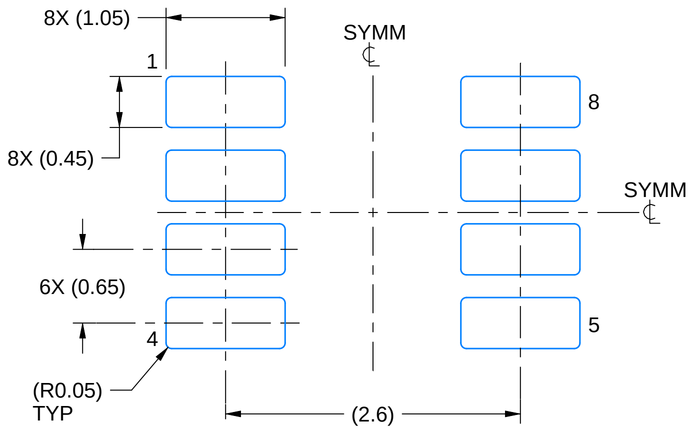

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| THVD8000TDDFR | SOT-23-THIN | DDF | 8 | 3000 | 184.0 | 184.0 | 19.0 |

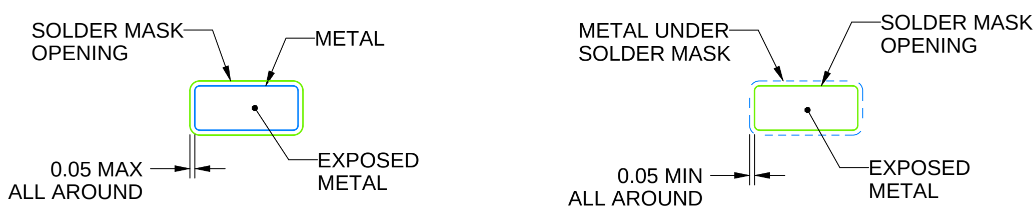



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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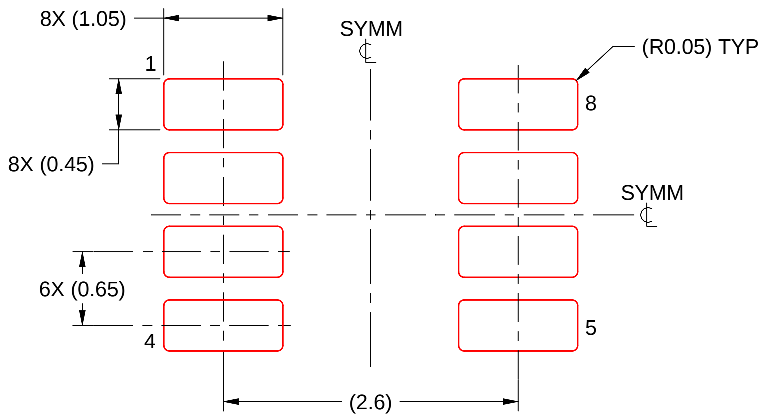
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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