







THVD2410V, THVD2412V THVD2450V, THVD2452V

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THVD24xxV ±70V Fault-Protected 3V to 5.5V RS-485 Transceivers with Flexible I/O Supply and IEC ESD

1 Features

- Meets or exceeds the requirements of the TIA/ EIA-485A and TIA/EIA-422B standards
- 3V to 5.5V RS-485 supply voltage
- Differential output exceeds 2.1V for PROFIBUS compatibility with 5V supply
- 1.65V to 5.5V Supply for logic signal interface
- SLR Pin Selectable Data Rates:
 - THVD2410V, THVD2412V: 250kbps and 1Mbps
 - THVD2450V, THVD2452V: 20Mbps and 50Mbps
- Bus I/O protection
 - ±70V DC bus fault
 - ±16kV HBM ESD
 - Half duplex devices: ±15kV IEC 61000-4-2 contact and air-gap discharge
 - Full duplex devices: ±8kV IEC 61000-4-2 contact and air-gap discharge
 - ±4kV IEC 61000-4-4 fast transient burst
- Half-duplex and Full-Duplex devices available in two speed grades
- Extended ambient temperature range: -40°C to
- Extended operational common-mode range: ±25V
- Enhanced receiver hysteresis for noise immunity
- Low power consumption
 - Low shutdown supply current: < 5μA
 - Quiescent current during operation: < 5.3mA
- Glitch-free power-up/down for hot plug-in capability
- Open, short, and idle bus failsafe
- Thermal shutdown
- 1/8 unit load (up to 256 bus nodes) in -7V to 12V common mode range
- Small 3mm x 3mm VSON package to save board space, or 14-SOIC for drop-in compatibility

2 Applications

- Motor drives
- Factory automation and control
- HVAC systems
- **Building automation**
- Grid infrastructure
- **Electricity meters**
- **Process analytics**
- Video surveillance

3 Description

THVD24xxV are ±70V fault-protected, half and fullduplex RS-422/RS-485 transceivers using a 1.65V to 5.5V supply for logic signal interface, and a 3V to 5.5V bus side supply. These devices have slew rate select feature that enables them to be used at two maximum speeds based on the SLR pin setting.

These devices feature integrated IEC ESD protection. eliminating the need for system-level protection components. Extended ±25V input common-mode range makes reliable data communication over longer cable run lengths and/or in the presence of large ground loop voltages. Enhanced 250-mV receiver hysteresis provides high noise rejection. In addition, the receiver fail-safe feature makes sure of a logic high when the inputs are open or shorted together.

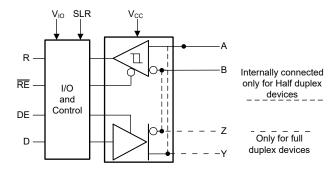
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
THVD2450V THVD2410V	VSON (10)	3mm × 3mm
THVD2412V THVD2452V	SOIC (14)	8.65mm × 3.91mm

- For more information, see Section 11.
- The package size (length × width) is a nominal value and includes pins, where applicable.

Table 3-1. Device Information

PART NUMBER	Duplex	Maximum data rate
THVD2410V	Half	SLR = High, 250kbps
THVD2412V	Full	SLR = Low, 1Mbps
THVD2450V	Half	SLR = High, 20Mbps
THVD2452V	Full	SLR = Low, 50Mbps



Simplified Schematic



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4 Pin Configuration and Functions

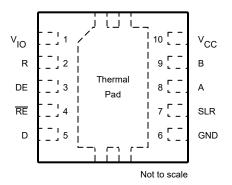


Figure 4-1. THVD2410V, THVD2450V 10-Pin DRC Package (VSON) Top View

Table 4-1. Pin Functions

NO.	NAME	TYPE	DESCRIPTION
1	V _{IO}	Logic Supply	Supply for logic I/O signals (R, RE, D, DE, and SLR)
2	R	Digital Output	Receive data output
3	DE	Digital Input	Driver enable input; integrated pull-down
4	RE	Digital Input	Receiver enable input; integrated pull-up
5	D	Digital Input	Transmission data input; integrated pull-up
6	GND	Reference Potential	Local device ground
7	SLR	Digital Input	Slew rate select. For THVD2410V: Low = 1 Mbps, High = 250 kbps. Defaults to 1 Mbps if SLR is left floating. For THVD2450V: Low = 50 Mbps, High = 20 Mbps. Defaults to 50 Mbps if left floating.
8	А	Bus I/O	RS 485 bus I/O, A
9	В	Bus I/O	RS 485 bus I/O, B
10	V _{CC}	Bus Supply	Bus supply
	Thermal Pad		Connect to GND for optimal thermal performance



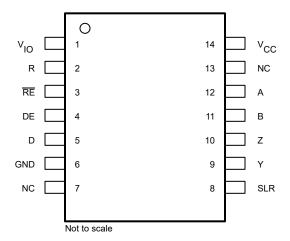


Figure 4-2. THVD2412V, THVD2452V 14-Pin SOIC Package (D) Top View

Table 4-2. Pin functions

NO.	NAME	TYPE	DESCRIPTION
1	V _{IO}	Logic supply	1.65 V to 5.5 V supply for logic I/O signals (R, RE, D, DE and SLR)
2	R	Digital output	Receive data output
3	RE	Digital input	Receiver enable input; integrated pull-up
4	DE	Digital input	Driver enable input; integrated pull-down
5	D	Digital input	Transmission data input; integrated pull-up
6	GND	Reference potential	Local device ground
7	NC	No connect	Not connected internally
8	SLR	Digital input	Slew rate select. For THVD2412V: Low = 1 Mbps, High = 250 kbps. Defaults to 1 Mbps if SLR is left floating. For THVD2452V: Low = 50 Mbps, High = 20 Mbps. Defaults to 50 Mbps if left floating.
9	Y	Bus output	RS 485 driver non-inverting output
10	Z	Bus output	RS 485 driver inverting output
11	В	Bus input	RS 485 receiver inverting input
12	А	Bus input	RS 485 receiver non-inverting input
13	NC	No connect	Not connected internally
14	V _{CC}	Bus supply	3 V to 5.5 V bus supply



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Logic supply voltage	V _{IO}	-0.5	V _{CC} + 0.2	V
Bus supply voltage	V _{CC}	-0.5	6.5	V
Bus voltage	Range at any bus pin as differential or common-mode with respect to GND	-70	70	V
Input voltage	Range at any logic pin (D, DE, SLR or RE)	-0.3	V _{IO} + 0.2	V
Receiver output current	Io	-24	24	mA
Storage temperature	T _{stg}	-65	170	°C

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
			Bus terminals and GND	±16,000	V
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾	All pins except bus terminals and GND	minals and GND ±16,000 except bus terminals H2,000 ±4,000	V
		Charged-device model (CDM), per JEDEC specifi	cation JESD22-C101 ⁽²⁾	±1,500	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings [IEC]

				VALUE	UNIT	
1	Electrostatic discharge, Half	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±15,000		
V _(ESD)	duplex devices THVD2410V/ 2450V (1)	Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±15,000	V	
	Electrostatic discharge, Full	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±8,000		
V _(ESD)	duplex devices THVD2412V/ 2452V	Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±8,000	V	
V _(EFT)	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V	

(1) For optimised IEC ESD performance, it is recommended to have series resistor (≥ 50 Ω) on all logic inputs to minimize transient currents going into or out of the logic pins.

²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		3		5.5	V
V _{IO}	I/O supply voltage		1.65		V _{CC}	V
VI	Input voltage at any bus termin	nal (separately or common mode) ⁽¹⁾	-25		25	V
V _{IH}	High-level input voltage (driver inputs)	ligh-level input voltage (driver, driver enable, receiver enable and slew rate select puts) ow-level input voltage (driver, driver enable, receiver enable and slew rate select			V _{IO}	V
V _{IL}	Low-level input voltage (driver, inputs)	driver enable, receiver enable and slew rate select	0		0.3*V _{IO}	V
V _{ID}	Differential input voltage bus p	ins	-25		25	V
Io	Output current, driver		-60		60	mA
I _{OR}	Output current, receiver	V _{IO} = 1.8 V or 2.5 V	-4		4	mA
I _{OR}	Output current, receiver	V _{IO} = 3.3 V or 5 V	-8		8	mA
R _L	Differential load resistance		54	60		Ω
		THVD2410V, THVD2412V with SLR = V _{IO}			250	kbps
1.4	Simpling rate	THVD2410V, THVD2412V with SLR = GND or floating			1	Mbps
1/t _{UI}	Signaling rate	THVD2450V, THVD2452V with SLR = V _{IO}			20	Mbps
		THVD2450V, THVD2452V with SLR = GND or floating			50	Mbps
T _A	Operating ambient temperature	е	-40		125	°C
T _J	Junction temperature		-40		150	°C

⁽¹⁾ The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

5.5 Thermal Information

		THVD2410V THVD2450V	THVD2412V THVD2452V	
	THERMAL METRIC ⁽¹⁾	DRC (VSON)	D (SOIC)	UNIT
		10 PINS	14 PINS	
R _{0JA}	Junction-to-ambient thermal resistance	46.7	87.5	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	47.7	41.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.1	43.7	°C/W
ΨЈТ	Junction-to-top characterization parameter	0.7	8.1	°C/W
ΨЈВ	Junction-to-board characterization parameter	19.1	43.3	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	4.6	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



5.6 Power Dissipation

	PARAMETER	TEST CONDITION	NS		VALUE	UNIT
			THVD2410V, THVD2412V	250 kbps	160	
		Unterminated	THVD2410V, THVD2412V	1Mbps	250	mW
		R_L = 300 Ω, C_L = 50 pF (driver)	THVD2450V, THVD2452V	20Mbps	310	IIIVV
			THVD2450V, THVD2452V	50 Mbps	630	
	Driver and receiver enabled, loopback for full duplex devices (A connected to Y, B connected to Z) $V_{CC} = 5.5 \text{ V, } T_A = 125 ^{\circ}\text{C,}$ square wave at 50% duty cycle	RS-422 load R _L = 100 Ω , C _L = 50 pF (driver)	THVD2410V, THVD2412V	250 kbps	170	- mW
			THVD2410V, THVD2412V	1Mbps	250	
P _D			THVD2450V, THVD2452V	20Mbps	290	
			THVD2450V, THVD2452V	50 Mbps	570	
			THVD2410V, THVD2412V	250 kbps	220	
		RS-485 load	THVD2410V, THVD2412V	1Mbps	280	mW
		$R_L = 54 \Omega$, $C_L = 50 pF (driver)$	THVD2450V, THVD2452V	20Mbps	325	IIIVV
			THVD2450V, THVD2452V	50 Mbps	560	



5.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V , unless otherwise noted. (1)

	PARAMETER	TEST CONDITIONS	3	MIN	TYP	MAX	UNIT
Driver							
		$R_L = 60 \Omega$, $-25 V \le V_{test} \le 25 V$ (See Figure 6-1)	1.5	3.3		V
IV I	Driver differential output	R_L = 60 Ω, -25 V ≤ V_{test} ≤ 25 V, 4.5 V ≤ V_{CC} ≤ 5	.5 V (See Figure 6-1)	2.1	3.3		V
V _{OD}	voltage magnitude	R_L = 100 Ω (See Figure 6-2)		2	4		V
		$R_L = 54 \Omega$ (See Figure 6-2)		1.5	3.5		V
$\Delta V_{OD} $	Change in differential output voltage	R_L = 54 Ω or 100 Ω (See Figure 6-2)		-50		50	mV
V _{oc}	Common-mode output voltage	R_L = 54 Ω or 100 Ω (See Figure 6-2)		1	V _{CC} /2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54 Ω or 100 Ω (See Figure 6-2)	- , , , , , , , , , , , , , , , , , , ,			50	mV
I _{OS}	Short-circuit output current	DE = V_{IO} , -70 V ≤ (V_A or V_B) ≤ 70 V, or A shorte terminals for half duplex, Y/Z are for full duplex)		-250		250	mA
Receiver						-	
			V _I = 12 V		90	125	μA
	Due insurt ou	DE - 0.4.4	V _I = 25 V		200	250	μA
l _l	Bus input current	DE = 0 V, V_{CC} and V_{IO} = 0 V or 5.5 V	V _I = -7 V	-100	-80	50 3 50 250	μA
			V _I = -25 V	-350	-220		μA
V _{TH+}	Positive-going input threshold voltage (2)	Over common-mode range of ± 25 V	THVD2410V, THVD2450V	40	125	200	mV
V _{TH-}	Negative-going input threshold voltage (2)	Over common-mode range of ± 25 V	THVD2410V, THVD2450V	-200	-125	-40	mV
V _{TH+}	Positive-going input threshold voltage (2)	Over common-mode range of ± 25 V	THVD2412V, THVD2452V	20	125	200	mV
V _{TH-}	Negative-going input threshold voltage (2)	Over common-mode range of ± 25 V	THVD2412V, THVD2452V	-200	-125	-20	mV
V _{HYS}	Input hysteresis	Over common-mode range of ± 25 V			250		mV
V _{TH_FSH}	Input fail-safe threshold	Over common-mode range of ± 25 V	THVD2410V, THVD2450V	-40		40	mV
V _{TH_FSH}	Input fail-safe threshold	Over common-mode range of ± 25 V	THVD2412V, THVD2452V	-20		20	mV
C _{A,B}	Input differential capacitance	Measured between A and B, f = 1 MHz			50		pF
V _{OH}	Output high voltage	$I_{OH} = -8 \text{ mA}, V_{IO} = 3 \text{ to } 3.6 \text{ V or } 4.5 \text{ V to } 5.5 \text{ V}$		V _{IO} - 0.4	V _{IO} – 0.2		V
V _{OL}	Output low voltage	I _{OL} = 8 mA, V _{IO} = 3 to 3.6 V or 4.5 V to 5.5 V			0.2	0.4	V
V _{OH}	Output high voltage	$I_{OH} = -4$ mA, $V_{IO} = 1.65$ to 1.95 V or 2.25 V to 2	2.75 V	V _{IO} - 0.4 \	V _{IO} – 0.2		V
V _{OL}	Output low voltage	I _{OL} = 4 mA, V _{IO} = 1.65 to 1.95 V or 2.25 V to 2.7	75 V		0.2	0.4	V
I _{OZ}	Output high-impedance current, R pin	$V_O = 0 \text{ V or } V_{IO}, \overline{RE} = V_{IO}$		-1		1	μA
Logic				-		I	
I _{IN}	Input current (DE , SLR)	$1.65 \text{ V} \le \text{V}_{\text{IO}} \le 5.5 \text{ V}, 0 \text{ V} \le \text{V}_{\text{IN}} \le \text{V}_{\text{IO}}$				5	μA
I _{IN}	Input current (D, RE)	$1.65 \text{ V} \le \text{V}_{\text{IO}} \le 5.5 \text{ V}, 0 \text{ V} \le \text{V}_{\text{IN}} \le \text{V}_{\text{IO}}$		-5			μA
Thermal	Protection	•					
T _{SHDN}	Thermal shutdown threshold	Temperature rising		150	180		°C
T _{HYS}	Thermal shutdown hysteresis				10		°C
Supply		1		I			-
UV _{VCC}	Rising under-voltage threshold on V _{CC}				2.3	2.6	V
UV _{VCC}	Falling under-voltage threshold on V _{CC}			1.95	2.2		V



5.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V , unless otherwise noted. (1)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
UV _{VCC(hys)}	Hysteresis on under-voltage of V _{CC}				170		mV
UV _{VIO} (rising)	Rising under-voltage threshold on V _{IO}				1.4	1.6	V
UV _{VIO} (falling)	Falling under-voltage threshold on V _{IO}			1.2	1.3		V
UV _{VIO(hys)}	Hysteresis on under-voltage of V _{IO}				120		mV
		Driver and receiver enabled	RE = 0 V, DE = V _{IO} , No load		3.5	1.6 5.3 4.2 2.4 1.2 4.1 3 2.2 1 8.4 8.4	mA
	Supply current (quiescent), V _{CC} = 4.5 V to 5.5 V	Driver enabled, receiver disabled	RE = V _{IO} , DE = V _{IO} , No load		2.5	4.2	mA
		Driver disabled, receiver enabled	RE = 0 V, DE = 0 V, No load		1.8	2.4	mA
		Driver and receiver disabled	RE = V _{IO} , DE = 0 V, D = open, No load		0.1	1.2	μA
		Driver and receiver enabled	RE = 0 V, DE = V _{IO} , No load		3		mA
	Supply current (quiescent),	Driver enabled, receiver disabled	RE = V _{IO} , DE = V _{IO} , No load		2	3	mA
Icc	V _{CC} = 3 V to 3.6 V	Driver disabled, receiver enabled	RE = 0 V, DE = 0 V, No load		1.6	2.2	mA
		Driver and receiver disabled	RE = V _{IO} , DE = 0 V, D = open, No load		0.1	1	μΑ
		Driver disabled, Receiver enabled, SLR = GND	DE = 0 V, RE = 0 V, No load		4.5	8.4	μΑ
	Logic supply current	Driver disabled, Receiver enabled, SLR = V _{IO}	DE = 0 V, RE = 0 V, No load		3.3	8.4	μA
lio	(quiescent), V _{IO} = 3 to 3.6 V	Driver disabled, Receiver disabled, SLR = GND	DE = 0 V, RE = V _{IO} , No load		0.1	1	μA
UVVICC(hys) of UVVIO Ris (rising) thr UVVIO Fa (falling) UVVIO(hys) of UVVIO(hys) of UVVIO(hys) of UVVIO(hys) Icc Su Vc		Driver disabled, Receiver disabled, SLR = V _{IO}	DE = 0 V, RE = V _{IO} , No load		1.8	4	μA

⁽¹⁾ A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex devices

⁽²⁾ Under any specific conditions, V_{TH+} is specified to be at least V_{HYS} higher than V_{TH-}



5.8 Switching Characteristics_250 kbps

250-kbps (THVD2410V, THVD2412V with SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V , V_{IO} = 3.3 V, unless otherwise noted. (1)

	PARAMETER	TEST COND	TIONS	MIN	TYP	MAX	UNIT
Driver			<u>'</u>				
t _r , t _f	Differential output rise/fall time		V _{CC} = 3 to 3.6 V, Typical at 3.3V	450	560	1200	ns
r, t _f Dille	Dinerential output rise/fail time		V _{CC} = 4.5 to 5.5 V, Typical at 5 V	500	625	1200	ns
	Propagation delay	$R_L = 54 \Omega, C_L = 50 pF$	V _{CC} = 3 to 3.6 V, Typical at 3.3V		500	720	ns
t _{PHL} , t _{PLH}	Propagation delay	See Figure 6-3	V _{CC} = 4.5 to 5.5 V, Typical at 5 V		540	770	ns
+	Pulso skow It tl		V _{CC} = 3 to 3.6 V, Typical at 3.3V		10	70	ns
		V _{CC} = 4.5 to 5.5 V, Typical at 5 V		10	70	ns	
t _{PHZ} , t _{PLZ}	Disable time	RE = X			40	75	ns
	Enable time	RE = 0 V	See Figure 6-4		70	280	ns
t _{PZH} , t _{PZL}	RE = V _{IO}		and Figure 6-5		2.5	4.5	μs
t _{SHDN}	Time to shutdown	RE = V _{IO}		50		500	ns
Receiver							
t _r , t _f	Output rise/fall time				7	20	ns
t _{PHL} , t _{PLH}	Propagation delay	Ē = V _{IO}	See Figure 6-6		800	1270	ns
t _{SK(P)}	Pulse skew, t _{PHL} - t _{PLH}				5	45	ns
t _{PHZ} , t _{PLZ}	Disable time	DE = X			30	40	ns
		V_{IO} = 3 V to 3.6 V; DE = V_{IO}			90	120	ns
t _{PZH(1)}	Enable time	V _{IO} = 1.65 V to 1.95 V, DE = V _{IO}	See Figure 6-7		100	130	ns
	Enable time	V _{IO} = 3 V to 3.6 V; DE = V _{IO}	See Figure 6-7		900	1320	ns
t _{PZL(1)}		V _{IO} = 1.65 V to 1.95 V; DE = V _{IO}	900		1320	ns	
t _{PZH(2)} , t _{PZL(2)}	Enable time	DE = 0 V	See Figure 6-8		3.3	5.4	μs
t _{D(OFS)}	Delay to enter fail-safe operation	0 - 45 - 5	See Figure 6.0	7	11	18	μs
t _{D(FSO)}	Delay to exit fail-safe operation	- C _L = 15 pF	See Figure 6-9	540	800	1260	ns
t _{SHDN}	Time to shutdown	DE = 0 V	See Figure 6-8	50		500	ns

⁽¹⁾ A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device



5.9 Switching Characteristics_1 Mbps

1Mbps (THVD2410V, THVD2412V with SLR = 0) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V , V_{IO} = 3.3 V, unless otherwise noted. (1)

	PARAMETER	TEST CONDI		MIN	TYP	MAX	UNIT
Driver			1				
	Differential output rise/fall time		V _{CC} = 3 to 3.6 V, Typical at 3.3 V	125	150	300	ns
t _r , t _f	Dinerential output rise/fail time		V _{CC} = 4.5 to 5.5 V, Typical at 5 V	130	160	300	ns
+ +	Propagation delay	$R_L = 54 \Omega, C_L = 50 pF$	V _{CC} = 3 to 3.6 V, Typical at 3.3 V		160	240	ns
t _{PHL} , t _{PLH}	Propagation delay	See Figure 6-3	V _{CC} = 4.5 to 5.5 V, Typical at 5 V		185	280	ns
+	Pulse skew, t _{PHL} - t _{PLH}		V _{CC} = 3 to 3.6 V, Typical at 3.3 V		2	20	ns
t _{SK(P)}	ruise skew, [tpHL - tpLH]		V _{CC} = 4.5 to 5.5 V, Typical at 5 V		2	15	ns
t _{PHZ} , t _{PLZ}	Disable time	RE = X			40	95	ns
	Enable time	RE = 0 V	See Figure 6-4		90	275	ns
lPZH, lPZL		RE = V _{IO}	= V _{IO} and Figure 6-5				μs
t _{SHDN}	Time to shutdown	RE = V _{IO}		50		500	ns
Receiver							
t _r , t _f	Output rise/fall time				7	15	ns
t _{PHL} , t _{PLH}	Propagation delay	C _L = 15 pF	See Figure 6-6		50	85	ns
t _{SK(P)}	Pulse skew, t _{PHL} - t _{PLH}				4	12.5	ns
t _{PHZ} , t _{PLZ}	Disable time	DE = X			30	40	ns
t _{PZH(1)} ,	Enable time	V_{IO} = 3 V to 3.6 V; DE = V_{IO}	Can Figure 6.7		90	120	ns
t _{PZL(1)}	Enable time	V _{IO} = 1.65 V to 1.95 V; DE = V _{IO}	See Figure 6-7		90	130	ns
t _{PZH(2)} , t _{PZL(2)}	Enable time	DE = 0 V	See Figure 6-8		3	4.5	μs
t _{D(OFS)}	Delay to enter fail-safe operation	C ₁ = 15 pF	See Figure 6-9	7	10	18	μs
t _{D(FSO)}	Delay to exit fail-safe operation	OL - 10 PF	See rigule 6-9	27	40	60	ns
t _{SHDN}	Time to shutdown	DE = 0 V	See Figure 6-8	50		500	ns

⁽¹⁾ A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device



5.10 Switching Characteristics_20 Mbps

20-Mbps (THVD2450V, THVD2452V with SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted. (1)

PARAMETER		TEST C	ONDITIONS	MIN	TYP	MAX	UNIT
Driver						<u>'</u>	
	Differential output rise/fall time		V _{CC} = 3 to 3.6 V, Typical at 3.3 V	4	8	15	ns
t _r , t _f	Dinerential output rise/fail time		V _{CC} = 4.5 to 5.5 V, Typical at 5 V	4	7	15	ns
	Propagation delay	$R_L = 54 \Omega, C_L = 50 pF$	V _{CC} = 3 to 3.6 V, Typical at 3.3 V	6	12	30	ns
t _{PHL} , t _{PLH}	Propagation delay	See Figure 6-3	V _{CC} = 4.5 to 5.5 V, Typical at 5 V	4	9	26	ns
	Pulse skew, t _{PHL} - t _{PLH}		V _{CC} = 3 to 3.6 V, Typical at 3.3 V		1	3	ns
t _{SK(P)}	ruise skew, [tpHL - tpLH]		V _{CC} = 4.5 to 5.5 V, Typical at 5 V		1	3	ns
t _{PHZ} , t _{PLZ}	Disable time	RE = X			17	35	ns
	Enable time	RE = 0 V	See Figure 6-4		14	39	ns
t_{PZH}, t_{PZL}	Enable time	RE = V _{IO}			3	4.5	μs
t _{SHDN}	Time to shutdown	RE = V _{IO}		50		500	ns
Receiver							
t _r , t _f	Output rise/fall time	C _L = 15 pF			1.5	6	ns
	December deles	V _{IO} = 3 V to 3.6 V	Con Firmer C. C.	25	33	58	ns
t _{PHL} , t _{PLH}	Propagation delay	V _{IO} = 1.65 V to 1.95 V	See Figure 6-6	25	35	60	ns
t _{SK(P)}	Pulse skew, t _{PHL} - t _{PLH}	C _L = 15 pF			0.5	5	ns
t _{PHZ} , t _{PLZ}	Disable time	DE = X			12	25	ns
t _{PZH(1)} , t _{PZL(1)}	Enable time	DE = V _{IO}	See Figure 6-7		50	82	ns
t _{PZH(2)} , t _{PZL(2)}	Enable time	DE = 0 V	See Figure 6-8		2.8	5	μs
t _{D(OFS)}	Delay to enter fail-safe operation	C _L = 15 pF	See Figure 6-9	7	10	18	μs
t _{D(FSO)}	Delay to exit fail-safe operation	OL - 19 ht	See Figure 0-9	19	32	50	ns
t _{SHDN}	Time to shutdown	DE = 0 V	See Figure 6-8	50		500	ns
		1					

A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device



5.11 Switching Characteristics_50 Mbps

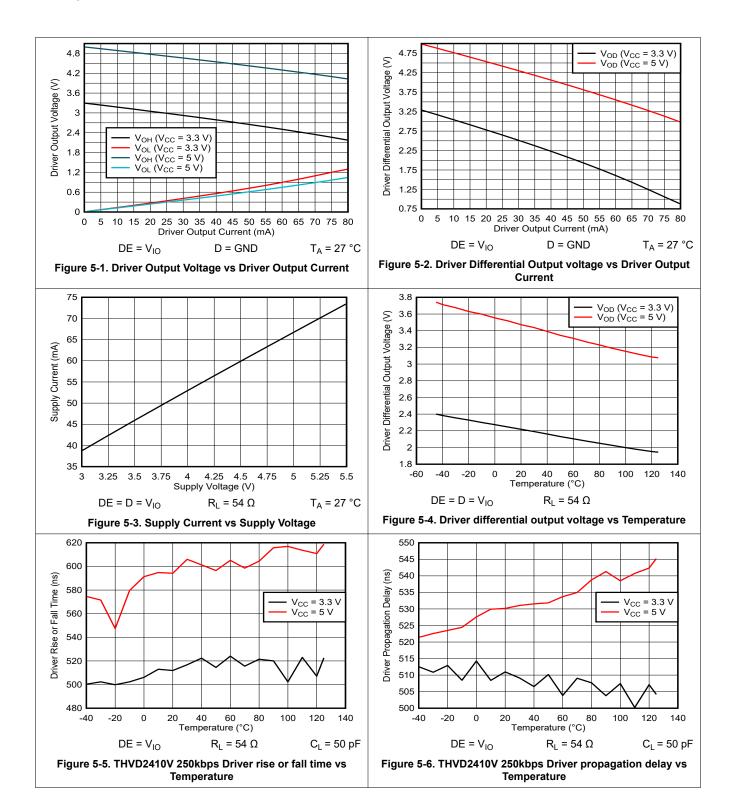
50-Mbps (THVD2450V, THVD2452V with SLR = 0) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted. (1)

	PARAMETER	TEST CONDI	TIONS	MIN	TYP	MAX	UNIT
Driver							
t _r , t _f	Differential output rise/fall time		V _{CC} = 3 to 3.6 V, Typical at 3.3 V	1	5	7	ns
ч, ч			V _{CC} = 4.5 to 5.5 V, Typical at 5 V	1	5	6	ns
			V _{IO} = 3 V to 3.6 V, V _{CC} = 3 to 3.6 V, Typical at 3.3 V	5	11	19	ns
t _{PHL} , t _{PLH} Propagation delay	Dropogation doloy	R _L = 54 Ω, C _L = 50 pF	V _{IO} = 1.65 V to 1.95 V, V _{CC} = 3 to 3.6 V, Typical at 3.3 V	7	12	22	ns
	гторадацоп четау	See Figure 6-3	V _{IO} = 3 V to 3.6 V, V _{CC} = 4.5 to 5.5 V, Typical at 5 V	4	8	15	ns
			V _{IO} = 1.65 V to 1.95 V, V _{CC} = 4.5 to 5.5 V, Typical at 5 V	6	10	19	ns
town	Pulse skew, t _{PHL} - t _{PLH}		V _{CC} = 3 to 3.6 V, Typical at 3.3 V		1	3	ns
t _{SK(P)}	т изе экем, јфнг – фгнј		V _{CC} = 4.5 to 5.5 V, Typical at 5 V		1	3	ns
t _{PHZ} , t _{PLZ}	Disable time	RE = X			14	30	ns
	RE = 0 V ; V _{IO} = 1.65 V t 2.25 V to 2.75 V	RE = 0 V; V _{IO} = 1.65 V to 1.95 V, 2.25 V to 2.75 V	See Figure 6-4		20	35	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE} = 0 \text{ V}$; $V_{IO} = 3 \text{ V}$ to $V_{CC} \text{ V}$	and Figure 6-5		15	32	ns
		RE = V _{IO}	1		2.5	4.5	μs
t _{SHDN}	Time to shutdown	RE = V _{IO}		50		500	ns
Receiver							
t _r , t _f	Output rise/fall time		See Figure 6-6		1.5	6	ns
t _{PHL} , t _{PLH}	Propagation delay	C _L = 15 pF	V _{IO} = 3 V to 3.6 V, See Figure 6-6	25	33	58	ns
t _{PHL} , t _{PLH}	Propagation delay		V _{IO} = 1.65 V to 1.95 V, See Figure 6-6	25	35	60	ns
t _{SK(P)}	Pulse skew, t _{PHL} - t _{PLH}	C _L = 15 pF	See Figure 6-6		0.5	5	ns
t _{PHZ} , t _{PLZ}	Disable time	DE = X			12	25	ns
t _{PZH(1)} ,	Enable time	DE = V _{IO}	V _{IO} = 1.65 V to 1.95 V, See Figure 6-7		50	82	ns
t _{PZL(1)}	Litable title	DC - VIO	V _{IO} = 3 V to 3.6 V, See Figure 6-7		50	75	ns
t _{PZH(2)} , t _{PZL(2)}	Enable time	DE = 0 V	See Figure 6-8		2.8	5	μs
t _{D(OFS)}	Delay to enter fail-safe operation	C = 15 pE	See Figure 6-9	7	10	18	μs
t _{D(FSO)}	Delay to exit fail-safe operation	- C _L = 15 pF	See Figure 0-9	19	32	50	ns
t _{SHDN}	Time to shutdown	DE = 0 V	See Figure 6-8	50		500	ns

⁽¹⁾ A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device

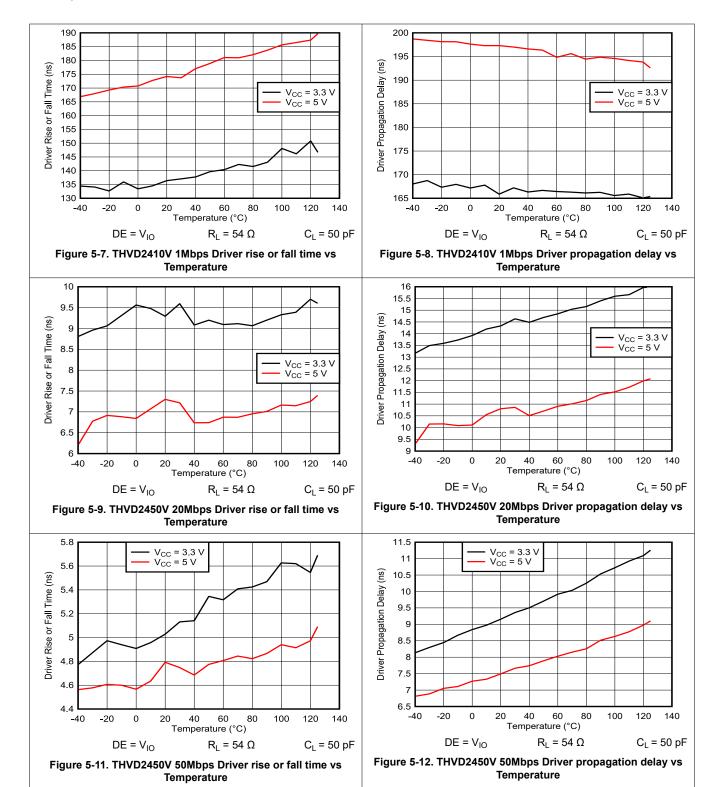


5.12 Typical Characteristics



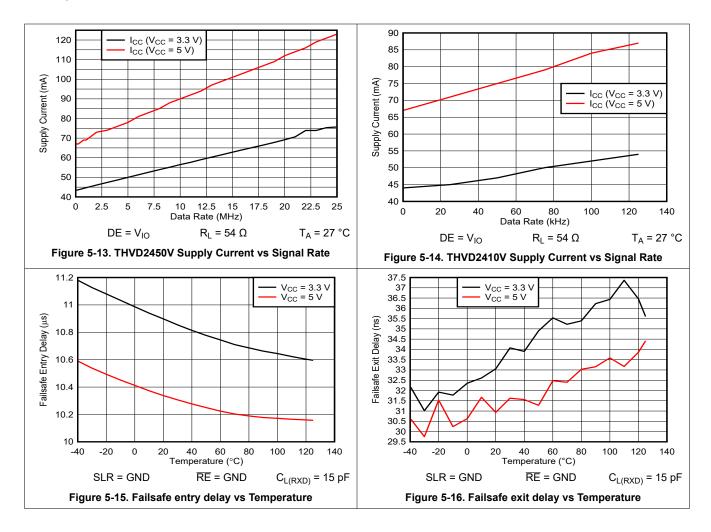


5.12 Typical Characteristics (continued)





5.12 Typical Characteristics (continued)





6 Parameter Measurement Information

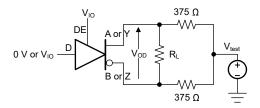


Figure 6-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

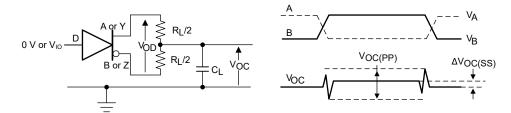


Figure 6-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

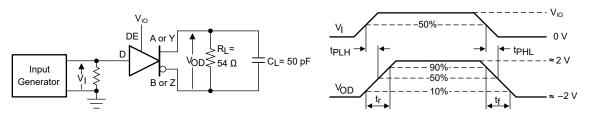


Figure 6-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

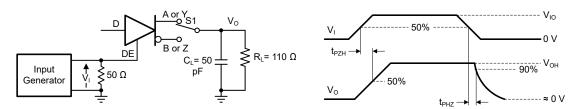


Figure 6-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

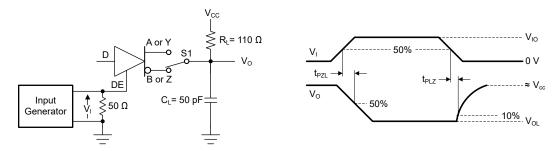


Figure 6-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load



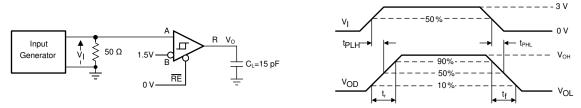


Figure 6-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

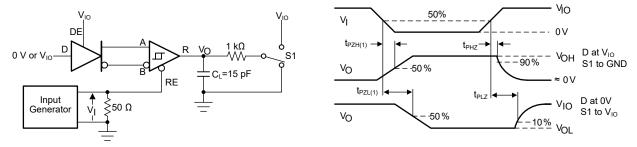


Figure 6-7. Measurement of Receiver Enable/Disable Times With Driver Enabled

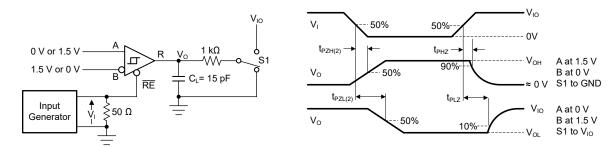


Figure 6-8. Measurement of Receiver Enable Times With Driver Disabled

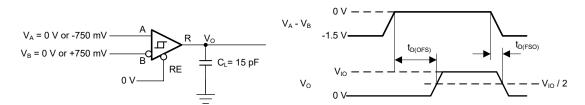


Figure 6-9. Measurement of Fail-Safe Delay



7 Detailed Description

7.1 Overview

THVD24xxV are ±70V bus fault-protected, ±25V common-mode voltage range capable half and full-duplex RS-485 transceivers. The devices have active-high driver enable and active-low receiver enable logic. Each device has SLR pin which allows it to be used for two different maximum speed settings. This is beneficial as customers can qualify one device and use it in two different end-applications. The devices also have flexible I/O supply pin V_{IO} which enables digital interface voltage range, from 1.65V to 5.5V, different from bus voltage supply 3V to 5.5V.

7.2 Functional Block Diagrams

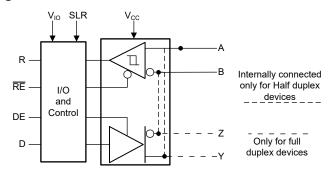


Figure 7-1. THVD2410 and THVD2450 Block Diagram

7.3 Feature Description

7.3.1 ±70 V Fault Protection

THVD24xxV transceivers have extended bus fault protection compared to standard RS-485 devices. Transceivers that operate in rugged industrial environments are often exposed to voltage transients greater than the -7 V to +12 V defined by the TIA/EIA-485A standard. To protect against such conditions, the generic RS-485 devices with lower absolute maximum ratings requires expensive external protection components. To simplify system design and reduce overall system cost, THVD24xxV devices are protected up to ±70 V without the need for any external components.

7.3.2 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceivers against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±15 kV contact and air discharge (for half-duplex devices) and up to ±8 kV contact and air discharge (for full-duplex devices). Bus structures also protect against electrical fast transients (EFT) according to IEC 61000-4-4 for up to ±4 kV. With careful system design, integrated bus structures can enable EFT Criterion A at the system level (minimum to no data loss when transient noise is present).

7.3.3 Driver Overvoltage and Overcurrent Protection

The THVD24xxV drivers are protected against any DC supply shorts in the range of -70 V to +70 V. The devices internally limit the short circuit current to ± 250 mA in order to comply with the TIA/EIA-485A standard. In addition, a fold-back current limiting circuit further reduces the driver short circuit current to less than ± 5 mA if the output fault voltage exceeds $|\pm 25$ V|.

All devices feature thermal shutdown protection that disables the driver and the receiver if the junction temperature exceeds the T_{SHDN} threshold due to excessive power dissipation.

7.3.4 Enhanced Receiver Noise Immunity

The differential receivers of THVD24xxV feature fully symmetric thresholds to maintain duty cycle of the signal even with small input amplitudes. In addition, 250 mV (typical) hysteresis provides noise immunity. When the device is in slew rate limited mode of 250 kbps, typical 700 ns of glitch filter in receiver signal chain prevents high frequency noise pulses from the bus to appear on R pin.



7.3.5 Receiver Fail-Safe Operation

The receivers are fail-safe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- · Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the receiver outputs a fail-safe logic high state if the input amplitude stays for longer than $t_{D(OFS)}$ at less than $|V_{TH\ FSH}|$.

7.3.6 Low-Power Shutdown Mode

Driving DE low and \overline{RE} high for longer than 500 ns puts the devices into the shutdown mode. If either DE goes high or \overline{RE} goes low, the counters reset. The devices does not enter the shutdown mode if the enable pins are in disable state for less than 50 ns. This feature prevents the devices from accidentally going into shutdown mode due to skew between DE and \overline{RE} .

7.4 Device Functional Modes

When the driver enable pin, DE, is logic high (H), the differential outputs A/Y and B/Z follow the logic states at data input D. A logic high at D causes A/Y to turn high and B/Z to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low (L), the output states reverse: B/Z turns high, A/Y becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant (X). The DE pin has an internal pull-down resistor to ground; thus, when left open the driver is disabled (Z = high-impedance) by default. The D pin has an internal pull-up resistor to V_{IO} ; thus, when left open while the driver is enabled, output A/Y turns high and B/Z turns low.

INPUT ENABLE OUTPUTS FUNCTION D DE A/Y B/Z Н Н Н L Actively drive bus high L L Н Actively drive bus low Ζ Χ L Ζ Driver disabled OPEN 7 Ζ Χ Driver disabled by default **OPEN** L Н Н Actively drive bus high by default

Table 7-1. Driver Function Table



When the receiver enable pin, \overline{RE} , is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is higher than the positive input threshold, V_{TH+} , the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-} , the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When \overline{RE} is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Ia	ole 7-2. Receiv	er runction i	able
DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	RE	R	FUNCTION
V _{TH+} < V _{ID}	L	Н	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
V _{ID} < V _{TH-}	L	L	Receive valid bus low
X	Н	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	Н	Fail-safe high output
Short-circuit bus	L	Н	Fail-safe high output
Idle (terminated) bus	L	Н	Fail-safe high output

Table 7-2. Receiver Function Table

Table 7-3 shows SLR (slew rate select) pin functionality. SLR has intergated pull-down, so the device remains in higher speed mode until SLR is pulled high which limits the slew rate and puts the device in slower speed mode.

Table 7-3. SER pill control						
Device	Functionality w.r.t SLR pin					
THVD2410V, THVD2412V	SLR = Low or floating: Both transmitter (TX) and receiver (RX) maximum speed is 1 Mbps SLR = High: Both TX and RX maximum speed is limited to 250 kbps					
THVD2450V, THVD2452V	SLR = Low or floating: Both transmitter (TX) and receiver (RX) maximum speed is 50 Mbps SLR = High: Both TX and RX maximum speed is limited to 20 Mbps					

Table 7-3. SLR pin control

Table shows the device behavior in undervoltage scenarios:

Table 7-4. Supply Function Table

	10000	rane i meappiy i amenen rane									
V _{CC}	V _{IO}	Driver Output	Receiver Output								
> UV _{VCC(rising)}	> UV _{VIO(rising)}	Determined by DE and D inputs	Determined by RE and A-B								
< UV _{VCC(falling)}	> UV _{VIO(rising)}	High impedance	High impedance								
> UV _{VCC(rising)}	< UV _{VIO(falling)}	High impedance	High impedance								
< UV _{VCC(falling)}	< UV _{VIO(falling)}	High impedance	High impedance								

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

THVD24xxV are fault-protected, half- and full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For these devices, the driver and receiver enable pins allow for the configuration of different operating modes.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T , whose value matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

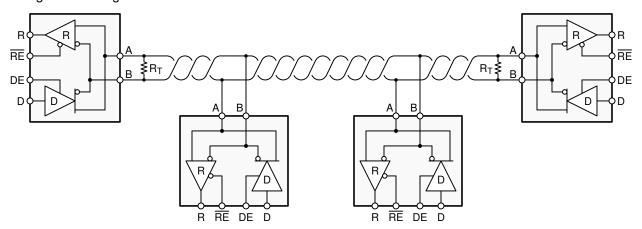


Figure 8-1. Typical RS-485 Network With Half-Duplex Transceivers

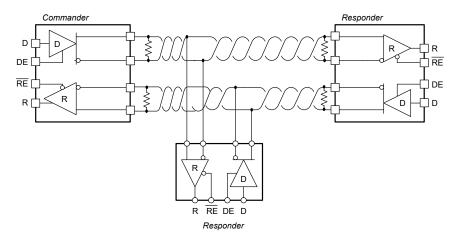


Figure 8-2. Typical RS-485 Network with Full-Duplex transceivers



8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

8.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

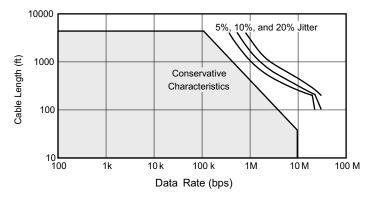


Figure 8-3. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 50 Mbps for the THVD24xxV) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

8.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \le 0.1 \times t_r \times v \times c \tag{1}$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light $(3 \times 10^8 \text{ m/s})$
- v is the signal velocity of the cable or trace as a factor of c

8.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 k Ω . Because the THVD24xxV devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible for a limited common mode range of - 7 V to 12 V.

8.2.1.4 Transient Protection

The bus pins of the THVD24xxV transceivers include on-chip ESD protection against ± 16 -kV HBM and ± 15 -kV IEC 61000-4-2 contact discharge for half-duplex devices ± 8 -kV for full-duplex devices. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

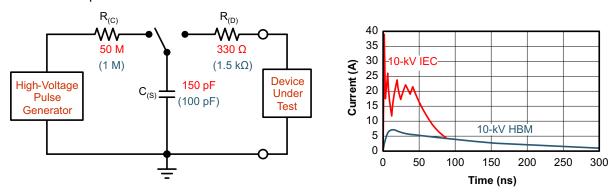


Figure 8-4. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 8-5 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left side of the diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which exceeds the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right side of the diagram shows the pulse power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are may occur in power generation and power-grid systems.

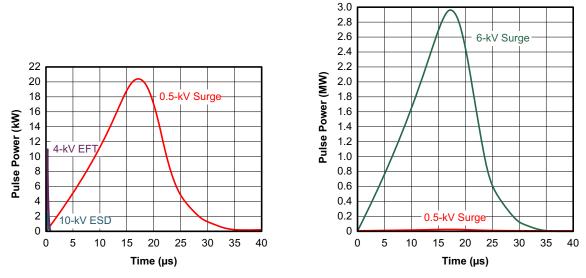


Figure 8-5. Power Comparison of ESD, EFT, and Surge Transients



For surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. Figure 8-6 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

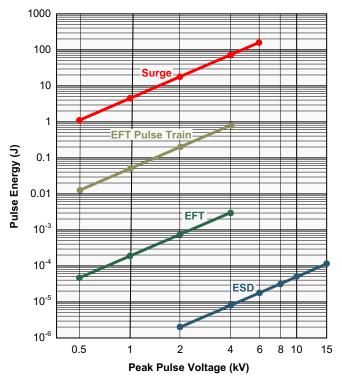


Figure 8-6. Comparison of Transient Energies



8.2.2 Detailed Design Procedure

Figure 8-7 suggests a protection circuit against 1kV surge (IEC 61000-4-5) transients. Table 8-1 shows the associated bill of materials. SMAJ30CA TVS diodes are rated to operate up to 30V. This makes sure the protection diodes do not conduct if a direct RS-485 bus shorts to 24V DC industrial power rail.

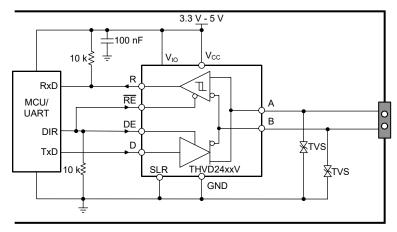


Figure 8-7. Transient Protection Against Surge Transients for Half-Duplex Devices

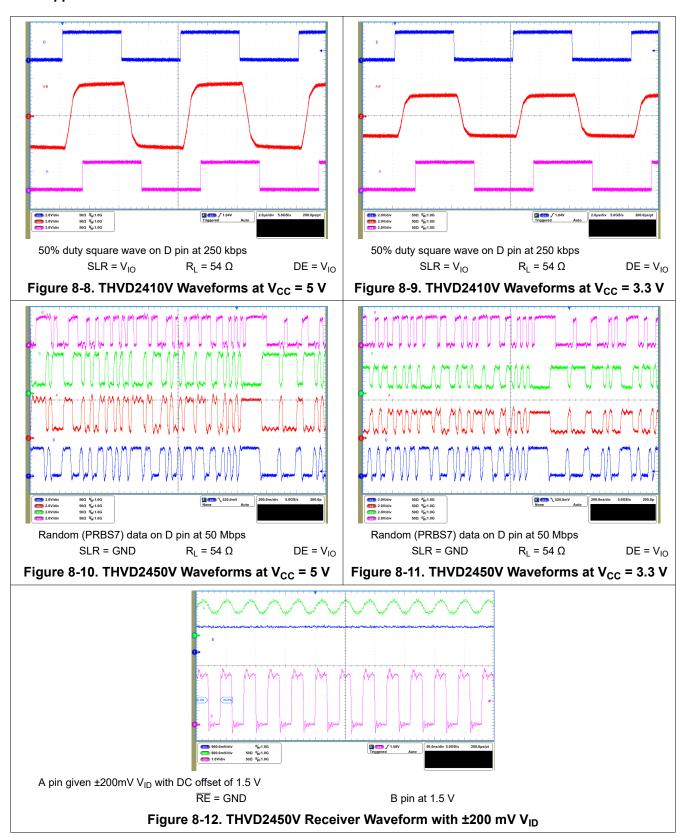
Table 8-1. Components List

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER ⁽¹⁾
XCVR	RS-485 transceiver	THVD2410V or THVD2450V	TI
TVS	Bidirectional 400W transient suppressor	SMAJ30CA	Littelfuse

(1) See Third-Party Products



8.2.3 Application Curves



8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be decoupled with a minimum of 100nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

8.4 Layout

8.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3MHz to 300MHz), high-frequency layout techniques should be applied during PCB design.

- 1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
- 2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
- 3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- 4. Apply 100nF to 220nF decoupling capacitors as close as possible to the V_{CC} and V_{IO} pins of transceiver, UART and/or controller ICs on the board.
- 5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
- 6. Use $1k\Omega$ to $10k\Omega$ pull-up and pull-down resistors for enable/SLR lines to limit noise currents in these lines during transient events.
- 7. Insert pulse-proof resistors into the A/Y and B/Z bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.

8.4.2 Layout Example

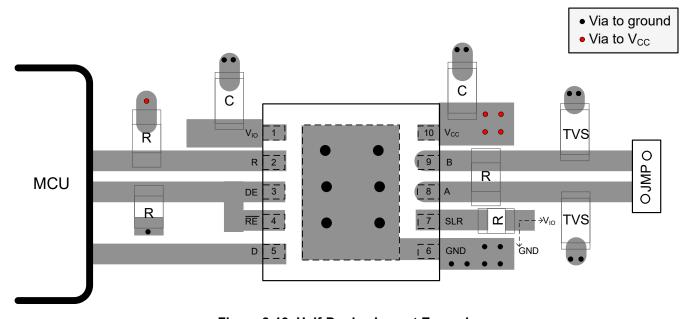


Figure 8-13. Half-Duplex Layout Example



9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
THVD2410VDRCR	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2410
THVD2410VDRCR.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2410
THVD2412VDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2412V
THVD2412VDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2412V
THVD2450VDRCR	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450VDRCR.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450VDRCRG4	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2450VDRCRG4.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450
THVD2452VDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2452V
THVD2452VDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2452V

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF THVD2410V, THVD2450V, THVD2452V:

● Enhanced Product: THVD2410V-EP, THVD2450V-EP, THVD2452V-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD2410VDRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THVD2412VDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
THVD2450VDRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THVD2450VDRCRG4	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THVD2452VDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1



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*All dimensions are nominal

7 and annotation and the financial							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD2410VDRCR	VSON	DRC	10	5000	367.0	367.0	35.0
THVD2412VDR	SOIC	D	14	2500	353.0	353.0	32.0
THVD2450VDRCR	VSON	DRC	10	5000	367.0	367.0	35.0
THVD2450VDRCRG4	VSON	DRC	10	5000	367.0	367.0	35.0
THVD2452VDR	SOIC	D	14	2500	353.0	353.0	32.0



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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