

THS4535 High-Precision, 60MHz, Fully Differential Amplifier

1 Features

Bandwidth: 60MHz (G = 1V/V)

Gain bandwidth product: 80MHz

External gain options:

 THS4535A offset voltage: 50µV (max) THS4535A offset drift: 1µV/°C (max) THS4535 offset voltage: 2mV (max)

THS4535 offset drift: 2µV/°C (max)

Internal gain options:

- Available gains: 0.5, 1, 2, 5

 CMRR: 129dB, 126dB, 123dB, 117dB - Gain error nonlinearity: 5, 4, 3, 1ppm

Gain error drift: 0.03, 0.03, 0.015, 0.005ppm/°C

Supply operating range: 2.7V to 5.5V

Low harmonic distortion:

 HD2: 124dBc at 2V_{PP}, 10kHz HD3: 115dBc at 2V_{PP}, 10kHz

Slew rate: 50V/µs

Low noise: 3.6nV/√Hz (10kHz)

1/f voltage noise corner: 2.5kHz

Supply current: 4.7mA

Negative rail input (NRI)

Rail-to-rail output (RRO)

Temperature range: -40°C to +125°C

2 Applications

- 16-bit to 20-bit, differential, SAR and $\Delta\Sigma$ drivers
- Differential active filters
- Motor drives
- **Battery testers**
- Power analyzers

3 Description

The THS4535 is a 60MHz fully differential amplifier (FDA) that is specifically designed to drive fully differential analog-to-digital converters (ADCs) up to 2MSPS. The THS4535 family offers multiple options: THS4535 (untrimmed external gain), THS4535A (trimmed external gain), and THS4535Axx (trimmed internal gain).

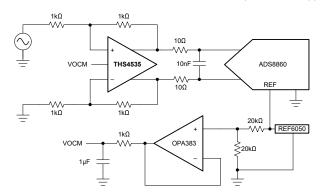
The THS4535 is an excellent choice for simple singleto-dual conversions. FDAs such as the THS4535 offer performance benefits over traditional dual op amps, including bandwidth and phase balance between outputs and a VOCM pin to easily adjust the output common-mode voltage. For higher dc precision applications, such as high-speed low-side current shunt measurements, the THS4535A provides package level trim for offset and offset drift. THS4535A also provides higher transient current output drive to meet the needs of successive approximation register (SAR) ADC charge injection and delta-sigma ($\Delta\Sigma$) ADC precharge buffers.

The THS4535Axx, with integrated SiCr resistors, is designed for data acquisition systems (DAQ) that require complete system-level precision. The THS4535Axx integrated resistors are specifically designed to minimize system level gain-error and temperature CMRR over and These temperature-stability and long-term-stability performance parameters, along with low signal-tonoise ratio (SNR) and low total harmonic distortion (THD), make the THS4535Axx an excellent choice for DAQ systems.

Package Information

PART NUMBER(1)	PACKAGE ⁽²⁾	PACKAGE SIZE(3)	
THS4535	DGK (VSSOP, 8)	3mm × 4.9mm	
	RUN (WQFN, 10)	2mm × 2mm	

- (1) See also Section 4
- (2) For more information, see Section 11.
- (3)The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic: Gain of 1V/V, Single-Ended-Input to Differential-Output Interface to SAR ADC



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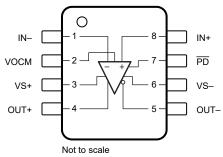
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4 Device Comparison Table

DEVICE	OFFSET VOLTAGE (MAX)	GAIN SETTING
THS4535DGKR	2mV	External resistors
THS4535ADGKR	50μV	External resistors
THS4535RUNR	2mV	F. the week and the week
THS4535ARUNR	50μV	External resistors
THS4535P5DGKR	2mV	G = 0.5, internal resistors
THS453501DGKR	2mV	G = 1, internal resistors
THS453502DGKR	2mV	G = 2, internal resistors
THS453505DGKR	2mV	G = 5, internal resistors
THS4535AP5DGKR	50μV	G = 0.5, internal resistors
THS4535A01DGKR	50μV	G = 1, internal resistors
THS4535A02DGKR	50μV	G = 2, internal resistors
THS4535A05DGKR	50μV	G = 5, internal resistors
THS4535P5RUNR	2mV	G = 0.5, internal resistors
THS453501RUNR	2mV	G = 1, internal resistors
THS453502RUNR	2mV	G = 2, internal resistors
THS453505RUNR	2mV	G = 5, internal resistors
THS4535AP5RUNR	50μV	G = 0.5, internal resistors
THS4535A01RUNR	50μV	G = 1, internal resistors
THS4535A02RUNR	50μV	G = 2, internal resistors
THS4535A05RUNR	50μV	G = 5, internal resistors



5 Pin Configuration and Functions



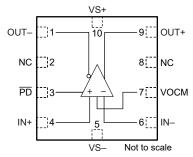
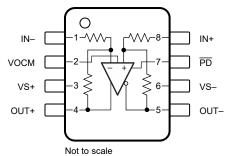


Figure 5-1. DGK Package, 8-Pin VSSOP (Top View), Figure 5-2. RUN Package, 10-Pin WQFN (Top View), External Gain



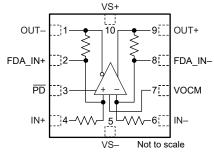


Figure 5-3. DGK Package, 8-Pin VSSOP (Top View), Figure 5-4. RUN Package, 10-Pin WQFN (Top View), Internal Gain

Table 5-1. Pin Functions

PIN					
	N	0.	TYPE	DESCRIPTION	
NAME	DGK (VSSOP)				
FDA_IN-	_	2	Input	Inverting (negative) amplifier input (internal gain)	
FDA_IN+	_	8	Input	Noninverting (positive) amplifier input (internal gain)	
IN-	1	6	Input	Inverting (negative) amplifier input	
IN+	8	4	Input	Noninverting (positive) amplifier input	
NC	_	2, 8	_	Leave unconnected (external gain)	
OUT-	5	1	Output	Inverting (negative) amplifier output	
OUT+	4	9	Output	Noninverting (positive) amplifier output	
PD	7	3	Input	Power down. \overline{PD} = logic low = power off mode; \overline{PD} = logic high = normal operation.	
VOCM	2	7	Input	Output common-mode voltage control input	
VS-	6	5	Power	Negative power-supply input	
VS+	3	10	Power	Positive power-supply input	



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V _S	Total supply voltage, $V_S = (V_{S+} - V_{S-})$		6	V
	Input, output, power down and common-mode pin voltage	$(V_{S-}) - 0.5$	$(V_{S+}) + 0.5$	V
I _{IN}	Continuous input current		±10	mA
I _{OUT}	Continuous output current ⁽²⁾		±50	mA
T _J	Junction temperature		150	°C
T _A	Free-air temperature	-40	125	°C
T _{stg}	Storage temperature	-65	150	°C

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾		V	
V(ESD)	Liectrostatic discriarge	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±1000	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Vs	Total supply voltage	2.7		5.5	V
TJ	Junction temperature	-40	25	125	°C

6.4 Thermal Information

		THS	THS4535			
	THERMAL METRIC ⁽¹⁾	DGK (VSSOP)	RUN (WQFN)	UNIT		
		8 PINS	10 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.8	147.1	°C/W		
R _{0JC(top)}	Junction-to-case (top) thermal resistance	46.4	86.9	°C/W		
$R_{\theta JB}$	Junction-to-board thermal resistance	86.1	85.2	°C/W		
Ψ_{JT}	Junction-to-top characterization parameter	1.4	8.2	°C/W		
Ψ_{JB}	Junction-to-board characterization parameter	84.7	84.9	°C/W		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W		

 For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



6.5 Electrical Characteristics for External Gain

at T_A = 25°C, V_{S+} – V_{S-} = 5V, V_{VOCM} ⁽¹⁾ = open (midsupply), R_F = 1k Ω , differential gain (G) = 1V/V, V_O = 2V_{PP}, R_L = 1k Ω , and \overline{PD} = logic high (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	MIN	TYP	MAX	UNIT
AC PER	RFORMANCE						
SSBW Small-signal bandwidth			G = 1V/V, < 2dB peaking		57		
	Small-signal bandwidth	$V_O = 100 \text{mV}_{PP}$	G = 2V/V		45		MHz
			G = 5V/V		16		
			G = 10V/V		8		
GBWP	Gain-bandwidth product	$V_O = 100 \text{mV}_{PP}, G$	= 20V/V		80		MHz
LSBW	Large-signal bandwidth	$V_{O} = 2V_{PP, G} = 1V$	'/V		17		MHz
	Bandwidth for 0.1dB flatness	$V_{O} = 2V_{PP}, G = 1V$	'/V		5		MHz
SR	Clay rate (200/ 000/)	\/ = 2\/ eten	Rising		47		Muo
SK	Slew rate (20%–80%)	V _O = 2V step	Falling		57		V/µs
	Overshoot and undershoot	V _O = 2V step, 8ns	input rise time		5		%
	Settling time	V _O = 2V step	To 0.1%		90		ns
t _S			To 0.01%		125		
	Rise and fall time (10%–90%)	V _O = 2V step, 8ns input rise time			32		ns
		tortion $V_{O} = 2V_{PP}$ $V_{O} = 8V_{PP}$	f = 1kHz		143		
			f = 10kHz		124		
LIDO			f = 1MHz		82		4D-
HD2	Second-order harmonic distortion		f = 1kHz		139		dBc
			f = 10kHz		123		
			f = 1MHz		76		
			f = 1kHz		135		
		$V_O = 2V_{PP}$	f = 10kHz		115		
LIDO	Third and a barrer wis distantion		f = 1MHz		74		4D-
HD3	Third-order harmonic distortion		f = 1kHz		122		dBc
		$V_O = 8V_{PP}$	f = 10kHz		102		
			f = 1MHz		57		
	land differential values as a size	f = 100kHz			3.6		nV/√Hz
e _n	Input differential voltage noise	1/f corner			2.5		kHz
	Innut ourrent noise	f≥50kHz			69		fA/√Hz
n	Input current noise	1/f corner			10		Hz
	Overdrive recovery time	G = 2V/V			800		ns
Z _{OUT}	Closed-loop output impedance	f = 100kHz (differe	ential)		0.26		Ω



6.5 Electrical Characteristics for External Gain (continued)

at T_A = 25°C, V_{S+} – V_{S-} = 5V, V_{VOCM} (1) = open (midsupply), R_F = 1k Ω , differential gain (G) = 1V/V, V_O = 2V_{PP}, R_L = 1k Ω , and \overline{PD} = logic high (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	MIN	TYP	MAX	UNIT
DC PE	RFORMANCE						
A _{OL}	Open-loop voltage gain	V _O = ±2V		100	115		dB
	loon to the standard	THS4535			±0.5	±2	mV
Vos	Input offset voltage	THS4535A			±3	±50	μV
	Input offset voltage drift		°C to +125°C		±0.3	±1.4	
	input offset voltage drift	THS4535A, T _A = -40°C to +125°C			±0.3	±1	μV/°C
	Input bigg gurrant(3)	T _A = 25°C			±0.2	±10	n 1
I _{B+} , I _B _	Input bias current ⁽³⁾	$T_A = -40^{\circ}C \text{ to } +125^{\circ}$	°C		±20	±200	рA
	Input offset current ⁽⁴⁾	Γ _A = 25°C			±0.2	±10	nΛ
los	input offset currents	$T_A = -40^{\circ}\text{C to } +125^{\circ}$	°C		±20	±200	pA
INPUT							
\/	Common-mode voltage	T _A = 25°C			V _{S-} - 0.2	V _{S-} - 0.1	V
V_{ICML}	input low	$T_A = -40^{\circ}C \text{ to } +125^{\circ}$	°C		V _{S-} - 0.2	V _{S-} - 0.1	V
\/	Common-mode voltage	T _A = 25°C		V _{S+} – 1.2	V _{S+} – 1.1		V
V_{ICMH}	input high	$T_A = -40^{\circ}C \text{ to } +125^{\circ}$	°C	V _{S+} – 1.2	V _{S+} – 1.1		V
CMRR	Common-mode rejection ratio	T _A = 25°C		108	140		dB
CIVITAIN	Common-mode rejection ratio	$T_A = -40^{\circ}C \text{ to } +125^{\circ}$	°C		100		uБ
	Differential input impedance				1 4.5		TΩ pF
	Common mode input impedance				1 1.2		TΩ pF
OUTPU	ĪT						
	Output voltage low	T _A = 25°C			$V_{S-} + 0.1$	$V_{S-} + 0.2$	V
	Output voltage low	$T_A = -40^{\circ}C \text{ to } +125^{\circ}$	°C		$V_{S-} + 0.1$	$V_{S-} + 0.2$	V
	Output voltage high	T _A = 25°C		$V_{S+} - 0.2$	$V_{S+} - 0.1$		V
	Output voltage riigir	$T_A = -40^{\circ}\text{C to } +125^{\circ}$	5°C	$V_{S+} - 0.2$	$V_{S+} - 0.1$		v
	Continuous output current (slam)	$V_0 = \pm 2.5 V, R_L = 40$	Ω	±80	±90		mA
	Continuous output outront (sium)	-	$\Omega_{\rm A}$, $T_{\rm A} = -40^{\circ}$ C to +125°C		±80		
	Line on the American	$V_{O} = \pm 2.3 V$	T _A = 25°C	±50	±60		
	Linear output current	$R_L = 40\Omega$, $A_{OL} > 80$ dB	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		±60		mA
OUTPU	JT COMMON-MODE VOLTAGE (V	OCM) CONTROL					
	V _{OCM} ⁽¹⁾ small-signal bandwidth	V _{VOCM} = 100mV _{PP}			40		MHz
	V _{OCM} large-signal bandwidth	V _{VOCM} = 1V _{PP}			15		MHz
	V _{OCM} slew rate ⁽²⁾ (20%–80%)	V _{VOCM} = 1V step			20		V/µs
	V _{OCM} voltage noise	f = 100kHz			22		nV/√Hz
	DC output balance	V _{VOCM} fixed midsup	oply, V _{OCM} /V _O , V _O = ±1V		92		dB
	Small-signal output balance	V _{VOCM} fixed midsup V _{OCM} /V _O (–3dB fror	oply, m dc), V _O = 100mV _{PP}		2000		Hz
	Large-signal output balance	V _{VOCM} fixed midsup V _{OCM} /V _O (–3dB fror			100		Hz
	Gain error	V _{VOCM} = 0V		0.997	1	1.003	V/V
	VOCM input bias current			-5	1	5	μA
	+PSRR to V _{OCM}	V _{VOCM} = midsupply		72	100		dB
	-PSRR to V _{OCM}	V _{VOCM} = midsupply		70	80		dB
	VOCM input impedance				200 1.5		kΩ pF

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6.5 Electrical Characteristics for External Gain (continued)

at T_A = 25°C, V_{S+} – V_{S-} = 5V, V_{VOCM} (1) = open (midsupply), R_F = 1k Ω , differential gain (G) = 1V/V, V_O = 2V_{PP}, R_L = 1k Ω , and \overline{PD} = logic high (unless otherwise noted)

	PARAMETER	TEST C	ONDITIONS	MIN	TYP	MAX	UNIT
	V offset voltage	VOCM pin floating	VOCM pin floating			10	mV
	V _{OCM} offset voltage	V _{VOCM} = midsupply	V _{VOCM} = midsupply		0.25	3.5	IIIV
	\/ offset voltage drift	$T_A = -40^{\circ}\text{C to } +125^{\circ}$	С	120	200	600	\//°C
	V _{OCM} offset voltage drift	$T_A = -40^{\circ}\text{C to } +125^{\circ}$	С	-10	3	10	μV/°C
	VOCM voltage low	< ±11mV shift from midsupply offset, T _A	= 25°C		V _{S-} + 0.4	V _{S-} + 0.45	V
	VOCIM Voltage low	< ±11mV shift from midsupply offset, T _A	= -40°C to +125°C			V _{S-} + 0.5	V
	VOCM voltage high	T _A = 25°C, < ±11mV shift from n	nidsupply offset	V _{S+} – 1.2	V _{S+} – 1.1		V
	VOCIM Voltage High	$T_A = -40$ °C to +125° < ±11mV shift from n	•	V _{S+} – 1.3			V
POWE	R SUPPLY						
		V _S = 5V, PD = logic high (active)	T _A = 25°C		4.7	5.1	mA
IQ	Quiescent current		$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		4.7	5.1	ША
-Q		$V_S = 5V$, $\overline{PD} = logic$ low (shutdown)	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		20		μΑ
PSRR	Power-supply rejection ratio	Either supply to inpu	t V _{OS}	90	110		dB
POWE	R DOWN						
	Enable voltage threshold	PD = logic high (activ	ve)	V _{S+} - 0.5			V
	Disable voltage threshold	PD = logic low (shute	down)			V _{S-} + 0.5	V
	Enable pin bias current	PD = high			0	6	
	Enable pili bias current	PD = low		-16	-10		μA
	Turn-on time delay	Time from PD = high value	Time from PD = high to V _O = 90% of final value		200		ns
	Turn-off time delay	Time from PD = low value	to V _O = 10% of original		20		ns

⁽¹⁾ V_{VOCM} refers to the voltage at VOCM pin. $V_{OCM} = [(V_{OUT+} + V_{OUT-})/2]$ refers to the average output voltage.

⁽²⁾ Average of the rising and falling slew rate.

⁽³⁾ Current out of the node is considered positive.

⁽⁴⁾ $I_{OS} = I_{B+} - I_{B-}$



6.6 Electrical Characteristics for Internal Gain

at T_A = 25°C, $V_{S+} - V_{S-}$ = 5V, V_{VOCM} (1) = open (midsupply), V_O = 2 V_{PP} , R_L = 1k Ω , and \overline{PD} = logic high (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	MIN	TYP	MAX	UNIT	
AC PER	RFORMANCE							
			G = 0.5V/V		70			
SSBW		$V_O = 100 \text{mV}_{PP}$	G = 1V/V		57			
	Small-signal bandwidth	(differential)	G = 2V/V		45		MHz	
			G = 5V/V		16			
			G = 0.5V/V		TBD			
		$V_O = 4V_{PP}$	G = 1V/V		TBD			
LSBW	Large-signal bandwidth	(differential)	G = 2V/V		TBD		MHz	
			G = 5V/V		TBD			
			G = 0.5V/V		TBD			
		0.1%, V _O = 4V _{PP}	G = 1V/V		TBD			
t _S	Settling time	(differential)	G = 2V/V		TBD		ns	
			G = 5V/V		TBD			
DC PEF	L RFORMANCE							
		G = 0.5V/V			2			
		G = 1V/V			1			
R_{IN}	Single-ended input resistance	G = 2V/V			0.5		kΩ	
		G = 5V/V			0.2			
R _F	Single-ended feedback resistance	All Gains			1		kΩ	
	redictande	G = 0.5V/V			129			
		G = 1V/V			126			
CMRR	Common-mode rejection ratio	G = 2V/V			123		dB	
		G = 5V/V			117			
		$G = 0.5V/V, V_{S+} = 5V, V_{S-} = 0V$		-0.6		11.4		
		$G = 1V/V, V_{S+} = 5V$		-0.4		7.6	V	
V _{CM}	Common-mode input voltage	$G = 2V/V, V_{S+} = 5V$		-0.3		5.7		
		$G = 5V/V, V_{S+} = 5V, V_{S-} = 0V$		-0.24		4.56		
		G = 0.5V/V	, 0		0.5			
		G = 1V/V			1			
G	Differential gain	G = 2V/V			2		V/V	
		G = 5V/V			5		-	
		G = 0.5V/V			0.015	0.075		
		G = 1V/V			0.015	0.075		
GE	Differential gain error	G = 2V/V			0.01	0.06	⊣ %	
		G = 5V/V			0.01	0.05		
		2 2	G = 0.5V/V		0.03	5.55		
	Differential gain error	T. = 40°C to	G = 1V/V		0.03			
	Differential gain error temperature drift	$T_A = -40^{\circ}C$ to +125°C	G = 2V/V		0.015		ppm/°C	
			G = 5V/V		0.015			

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6.6 Electrical Characteristics for Internal Gain (continued)

at T_A = 25°C, $V_{S+} - V_{S-}$ = 5V, V_{VOCM} (1) = open (midsupply), V_O = 2 V_{PP} , R_L = 1k Ω , and \overline{PD} = logic high (unless otherwise noted)

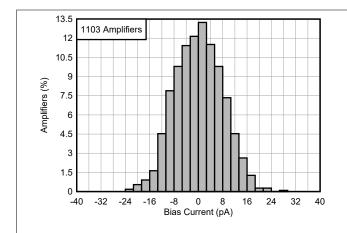
	PARAMETER	TE	ST CONDITIONS	MIN	TYP	MAX	UNIT
	Differential gain nonlinearity	G = 0.5V/V			5		
		G = 1V/V			4		ppm
		G = 2V/V			3		
		G = 5V/V			1		
	Differential gain error long-term drift	2000 hours	G = 0.5V/V		TBD		
			G = 1V/V		TBD		
			G = 2V/V		TBD		ppm
			G = 5V/V		TBD		

⁽¹⁾ V_{VOCM} refers to the voltage at VOCM pin. $V_{OCM} = [(V_{OUT+} + V_{OUT-})/2]$ refers to the average output voltage.



6.7 Typical Characteristics

at T_A = 25°C, V_{S+} – V_{S-} = 5V, V_{VOCM} = open (midsupply), R_F = 1k Ω , G = 1V/V, V_O = 2V_{PP}, R_L = 1k Ω , and \overline{PD} = logic high (unless otherwise noted)



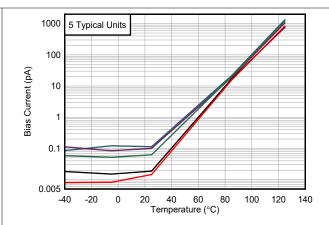
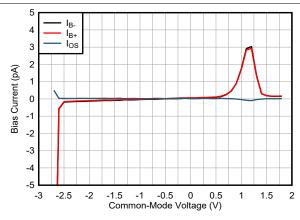


Figure 6-1. Input Bias Current Distribution

Figure 6-2. Input Bias Current vs Temperature



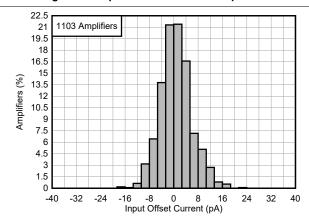
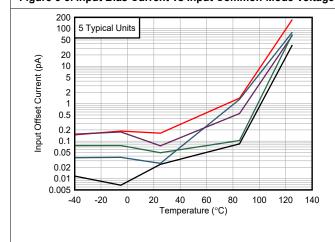


Figure 6-3. Input Bias Current vs Input Common-Mode Voltage

Figure 6-4. Input Offset Current Distribution



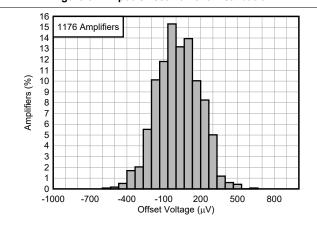


Figure 6-5. Input Offset Current vs Temperature

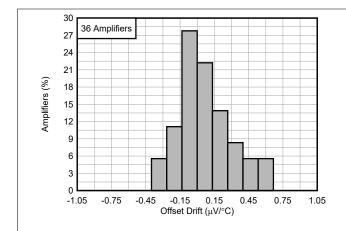
Figure 6-6. THS4535 Offset Voltage Distribution

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6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} – V_{S-} = 5V, V_{VOCM} = open (midsupply), R_F = 1k Ω , G = 1V/V, V_O = 2V_{PP}, R_L = 1k Ω , and \overline{PD} = logic high (unless otherwise noted)



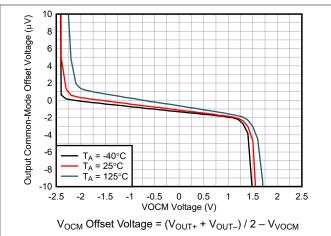
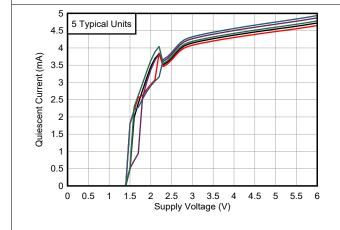


Figure 6-7. THS4535 Offset Voltage Drift Distribution

Figure 6-8. THS4535 Output Common-Mode Offset Voltage vs VOCM Voltage



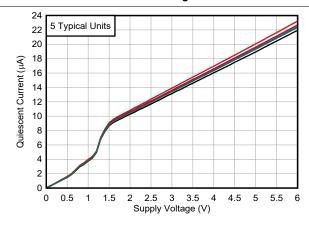
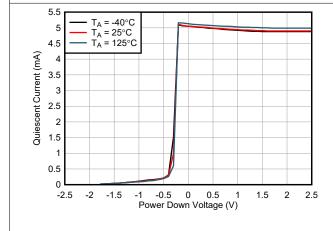


Figure 6-9. Quiescent Current vs Supply Voltage

Figure 6-10. Power-Down Quiescent Current vs Supply Voltage



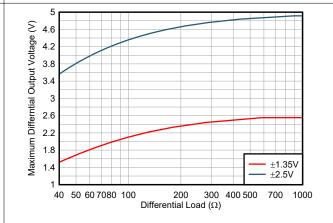


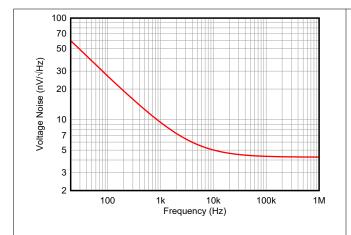
Figure 6-11. Quiescent Current vs PD Voltage

Figure 6-12. Maximum Differential Output Voltage vs Differential Load Resistance



6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{S^+} – V_{S^-} = 5V, V_{VOCM} = open (midsupply), R_F = 1k Ω , G = 1V/V, V_O = 2V_{PP}, R_L = 1k Ω , and \overline{PD} = logic high (unless otherwise noted)



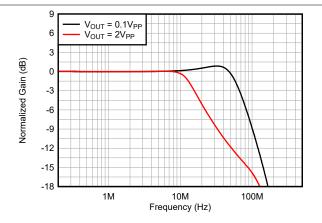
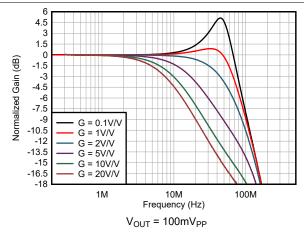


Figure 6-13. Input Voltage Noise vs Frequency

Figure 6-14. Small-Signal Bandwidth vs Frequency



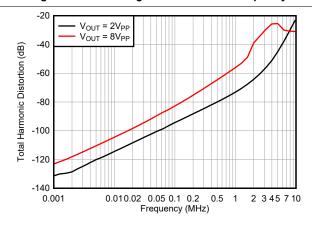
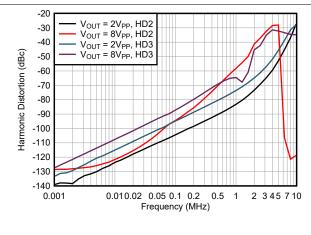


Figure 6-15. Small-Signal Bandwidth vs Frequency

Figure 6-16. Total Harmonic Distortion vs Frequency



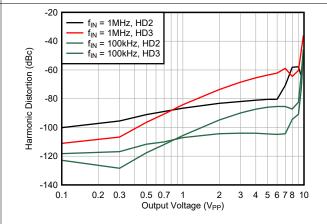


Figure 6-17. Harmonic Distortion vs Frequency

Figure 6-18. Harmonic Distortion vs Differential Output Voltage

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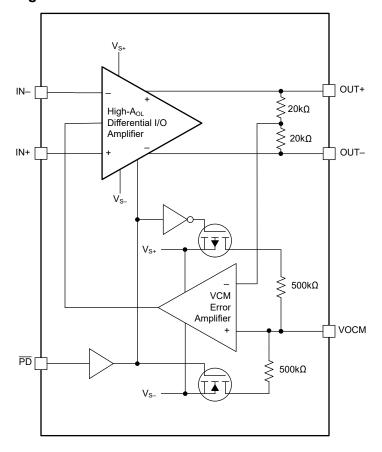


7 Detailed Description

7.1 Overview

The THS4535 is a fully differential CMOS amplifier designed to optimize dc and ac performance for driving < 2MSPS ADCs. The base version of this device, THS4535, is designed for single-ended to differential conversions in low-side current sensing or funnel amplifier applications. When dc precision is needed, the THS4535A provides a temperature trimmed version of the device. This temperature trimming, along with state of the art package construction, allows applications in data acquisition systems (DAQ) to minimize errors due to temperature drift, long-term drift, or applications that are sensitive to overtemperature shifts in bias current or input offset current. For the highest level of precision, the THS4535A offers four integrated SiCr resistors that are specifically designed to drift together over temperature and time. The result of these matched resistors is a system optimized for gain-error drift, CMRR drift, and long-term drift, providing a precision system without sacrificing ac output balance or distortion, and without the need for expensive laser trimmed resistors.

7.2 Functional Block Diagram





7.3 Feature Description

7.3.1 Output Common-Mode

The THS4535 output common-mode pin allows the FDA to servo the output pins (V_{OUT+} and V_{OUT-}) so that the average voltage of these two pins matches the VOCM pin. VOCM is especially useful when the input common-mode voltage does not match the desired output common-mode voltage, such as in ADC drive. For example, in the case of a high-side current sense measurement there is often a large common-mode voltage followed by a small differential voltage. If the high-side shunt resistor common-mode voltage is close to the positive supply (Figure 7-1), set the VOCM pin to $\frac{1}{2}$ the ADC reference voltage, and the differential output voltage is gained up and balanced around the V_{OCM} voltage.

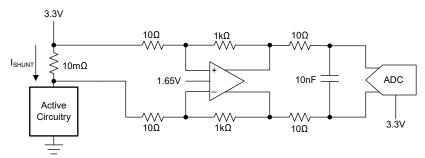


Figure 7-1. High-Side Current-Sense Example

Note

The THS4535 has an internal voltage divider with two $500k\Omega$ resistors, one connected to V_{S+} and one connected to V_{S-} , if no external bias is applied. To help protect against high-frequency transients coupling to this pin, connect a 1nF capacitor from V_{OCM} to ground to help stabilize the pin voltage internally.



7.4 Device Functional Modes

7.4.1 Power-Down Mode

Assert the power-down (\overline{PD}) pin to the desired voltage for proper power-down mode operation. A physical internal pullup resistor is not provided on the \overline{PD} pin so that if the pin is floated, the device defaults to the ON state. Tie the \overline{PD} pin to the positive supply voltage for applications that simply require the device to power on when the supplies are present. For single-supply operation, a minimum of 0.5V within the positive supply is required.

The disable operation is referenced from the positive supply. For an OFF state condition, the disable control pin must be 0.5V within the negative supply. Figure 7-2 shows how to use a microcontroller to toggle the power-down pin on the THS4535 by simply connecting a digital input/output (DIO) directly to the \overline{PD} pin.

Note

If using a microcontroller to enable the THS4535, ensure that the threshold voltages (VIH and VIL) in the *Electrical Characteristics* are satisfied.

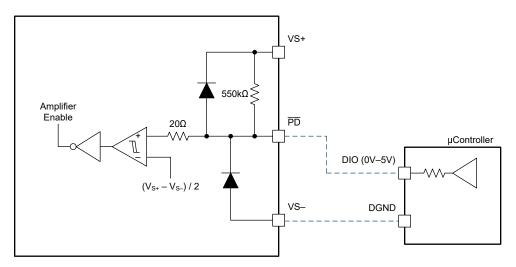


Figure 7-2. PD Pin Schematic



8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Most applications for the THS4535 strive to deliver the best dynamic range in a design that delivers the desired signal processing along with adequate phase margin for the amplifier. The following sections detail some of the design issues with analysis and guidelines for improved performance.

8.1.1 Output Common-Mode Voltage

The output common-mode voltage pin sets the dc output voltage of the THS4535. A voltage applied to the VOCM pin from a low-impedance source is used to directly set the output common-mode voltage. If left floating, then the VOCM pin defaults to the midrail voltage, defined as:

$$\frac{(V_{CC+}) + (V_{CC-})}{2}$$
 (1)

To minimize common-mode noise, connect a 0.1µF bypass capacitor to the VOCM pin. Output common-mode voltage causes additional current to flow in the feedback resistor network. This current is supplied by the output stage of the amplifier; therefore, additional power dissipation is created. For commonly-used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current is potentially significant in some applications, and dictates the use of the PowerPAD integrated circuit package to effectively control self-heating.

8.1.1.1 Resistor Matching

Resistor matching is important in FDAs to maintain good output balance. An ideal differential output signal implies the two outputs of the FDA are exactly equal in amplitude and shifted 180° in phase. Any imbalance in amplitude or phase between the two output signals results in an undesirable common-mode signal at the output. The output balance error is a measure of how well the outputs are balanced, and is defined as the ratio of the output common-mode voltage to the output differential signal.

Output Balance Error =
$$\frac{\left(\frac{V_{OUT} + -V_{OUT} -}{2}\right)}{V_{OUT} + -V_{OUT} -}$$
 (2)

At low frequencies, resistor mismatch is the primary contributor to output balance errors. Additionally CMRR, PSRR, and HD2 performance diminish if resistor mismatch occurs. Therefore, to optimize performance, use 1% tolerance resistors or better. Table 8-1 provides the recommended resistor values to use for a particular gain.

Table 8-1. Recommended Resistor Values

GAIN (V/V)	R _G (Ω)	R _F (Ω)
1	390	390
2	374	750
5	402	2010
10	402	4020

8.1.2 Data Converters

Driving data converters is one of the most popular applications for fully-differential amplifiers. Figure 8-1 shows a typical configuration of an FDA attached to a differential analog-to-digital converter (ADC).



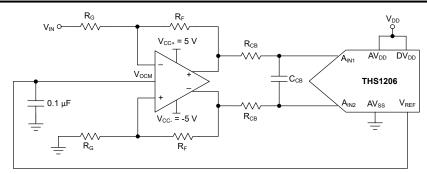


Figure 8-1. Fully-Differential Amplifier Attached to a Differential ADC

FDAs are able to operate with a single supply. V_{OCM} defaults to the midrail voltage, V_{CC} / 2. The differential output is fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{REF}), then connect V_{REF} directly to the V_{OCM} of the amplifier using a bypass capacitor to reduce broadband common-mode noise.

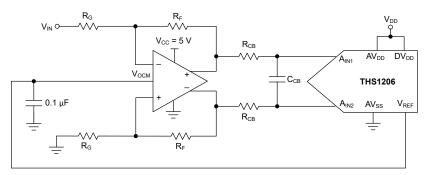


Figure 8-2. Fully-Differential Amplifier Using a Single Supply

8.1.3 Single-Supply Applications

For proper operation, do not exceed the common-mode input voltage range of the device. However, some single-supply applications require that the input voltage exceeds the common-mode input voltage range. In this case, to bring the common-mode input voltage within the specifications of the amplifier, use the circuit configuration of Figure 8-3.

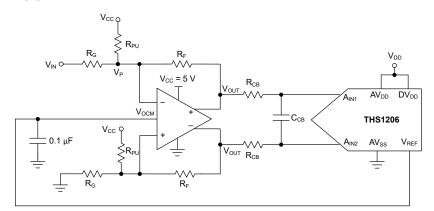


Figure 8-3. Circuit With Improved Common-Mode Input Voltage

Use Equation 3 to calculate R_{PU}:

$$R_{PU} = \frac{V_P - V_{CC}}{(V_{IN} - V_P)\frac{1}{R_G} + (V_{OUT} - V_P)\frac{1}{R_F}}$$
(3)



8.2 Typical Application

8.2.1 Typical Application

Single-to-differential conversion is a typical use-case for fully differential amplifiers (FDAs) as a result of the FDA output balance, output common-mode servo, and ADC output drive capabilities. Many higher-precision and higher-speed ADCs are moving towards differential inputs to improve common-mode noise immunity and to improve dynamic range. Figure 8-4 shows how the FDA architecture allows easy conversion by simply connecting the signal source to one input and grounding the other input.

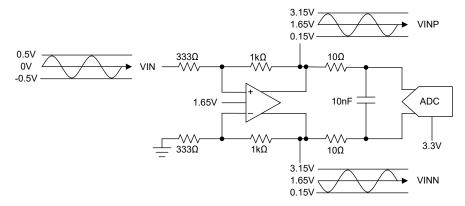


Figure 8-4. THS4535 Single-to-Differential Conversion

8.2.1.1 Design Requirements

Table 8-2. Design Parameters

DESIGN PARAMETERS	VALUE					
Input voltage	1V _{PP}					
ADC supply voltage	3.3V					
ADC input differential voltage	Balanced 6V _{PP}					
ADC input common-mode voltage	1.65V					

8.2.1.2 Detailed Design Procedure

The configuration shown in Figure 8-4 creates a differential gain of 3, while maintaining a balanced output at the middle of the ADC range. The differential gain (A_{V_DIFF}) is set by the ratio of the input resistors, $R_{IN} = 333\Omega$, and the feedback resistors, $R_{FB} = 1k\Omega$, for a total of 3V/V. The output common-mode is shifted to whatever voltage is specified on the V_{OUTCM} pin, which is ½ the ADC reference (1.65V for this example). The inherent architecture of the FDA makes two signals that are 180° out of phase with a maximum and minimum range of 0.15V to 3.15V. The total range of the ADC is not used in this example to provide headroom for the ADC or output range of the FDA if running on a 3.3V supply, but an alternative gain can be used to get an exact peak-to-peak voltage to match the ADC, if desired.

An alternative design to the FDA is a dual amplifier used in a two-op-amp instrumentation amplifier configuration. This design uses two amplifiers: one amplifier in a noninverting configuration that gains up the input signal, and one amplifier in an inverting configuration that inverts the output of the first amplifier. Figure 8-5 shows there are some sizable downsides to this approach. First, the output common-mode voltage depends on the input common-mode voltage because the noninverting amplifier output common-mode is dependent on the input common-mode voltage. This design shortcoming can be remedied by changing the dc bias of the gain resistor for the noninverting amplifier, as shown in Figure 8-5 with 0.075V, but an additional bias voltages is required. Failure to shift the output common-mode voltage correctly can result in signal loss due to output clipping on the noninverting amplifier when the input voltage is close to the negative rail. Second, there is a phase imbalance between the noninverting amplifier and the inverting amplifiers in this circuit. As more gain is required of this circuit, the noninverting amplifier gets slower as the gain increases while the inverting amplifier gain stays the



same. Such gain and phase imbalances potentially manifest as distortion errors, limit signal bandwidth, and are often exacerbated with loading.

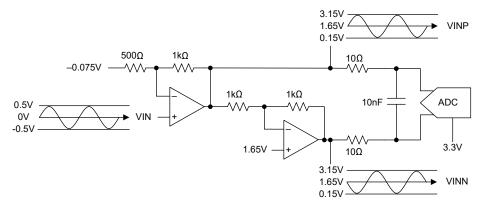


Figure 8-5. Dual Amplifier Single-to-Dual Conversion

8.3 Power Supply Recommendations

The THS4535 is designed to operate on power supplies ranging from ±1.35V to ±2.75V (single-ended supplies of 2.7V to 5.5V). Use a power-supply accuracy of 5% or better. When operated on a board with high-speed digital signals, provide isolation between digital signal noise and the analog input pins. The THS4535 is connected to power supplies through the VS+ and VS- pins. Decouple each supply pin to ground as close as possible to the device with a low-inductance, surface-mount ceramic capacitor of approximately 10nF. When vias are used to connect the bypass capacitors to a ground plane, configure the vias for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

To avoid undesirable signal transients, do not power on the THS4535 with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 Board Layout Recommendations

Similar to all high-speed devices, best system performance is achieved with close attention to board layout. The *THS4535DGKEVM* user's guide provides a good example of high-frequency layout techniques as a reference. This EVM includes numerous extra elements and features for characterization purposes that do not apply to some applications. General high-speed signal path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, both ground and power planes must be opened up around the capacitive sensitive input and output device pins. When the signal goes to a resistor, parasitic capacitance becomes more of a band-limiting issue and less of a stability issue.
- Good high-frequency decoupling capacitors (0.1µF) are required to a ground plane at the device power pins. Additional higher-value capacitors (2.2µF) are also required but can be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- Differential signal routing over any appreciable distance must use microstrip layout techniques with matched impedance traces.
- The input summing junctions are very sensitive to parasitic capacitance. Any R_G elements must connect into
 the summing junction with minimal trace length to the device pin side of the resistor. The other side of the R_G
 elements can have more trace length if needed to the source or to GND.



8.4.2 Layout Examples

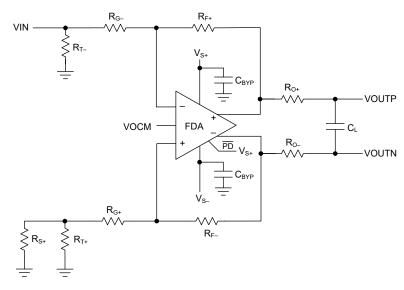


Figure 8-6. Representative Schematic for the Layout Recommendations

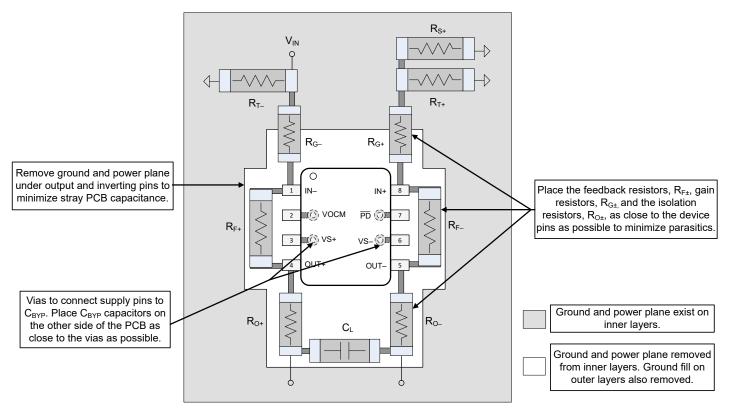


Figure 8-7. Layout Recommendations (DGK Package)



9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES			
June 2025	*	Initial Release			

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

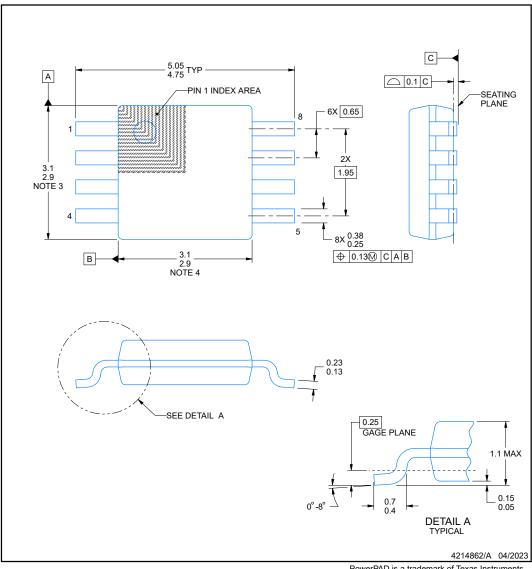


DGK0008A

PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.

 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

 5. Reference JEDEC registration MO-187.



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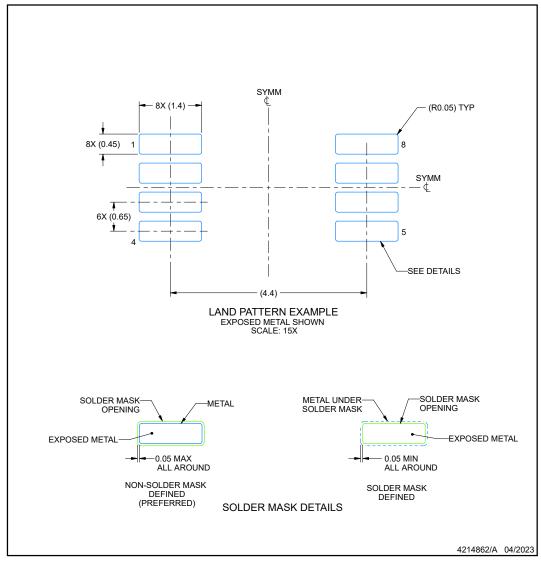


EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- Problication IPC-7351 may have alternate designs.
 Solder mask tolerances between and around signal pads can vary based on board fabrication site.
 Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
 Size of metal pad may vary due to creepage requirement.



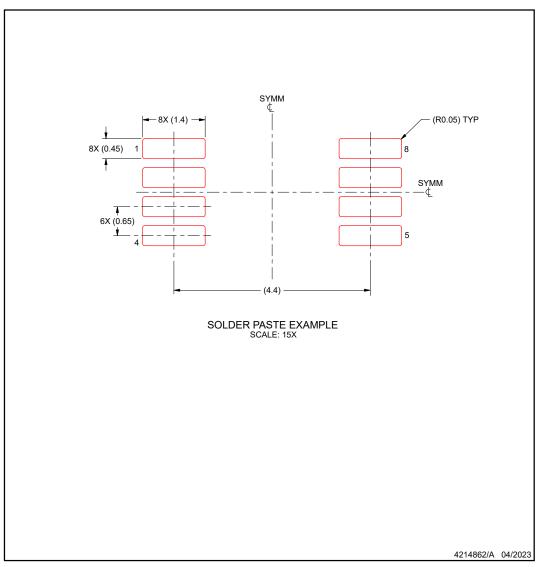


EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

 12. Board assembly site may have different recommendations for stencil design.



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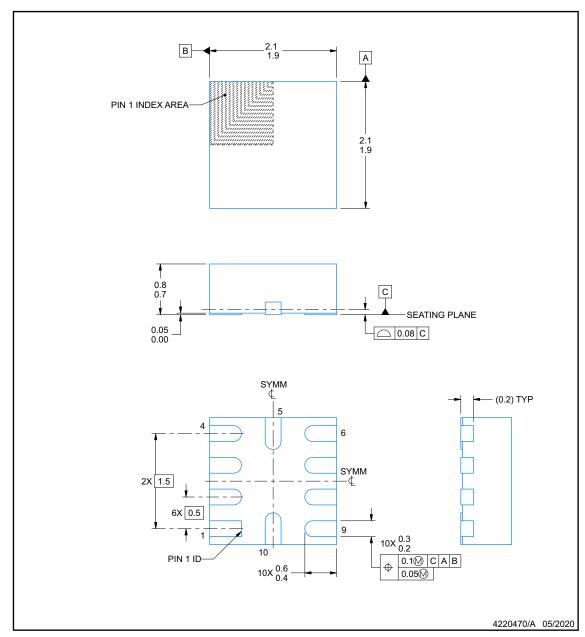


RUN0010A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.

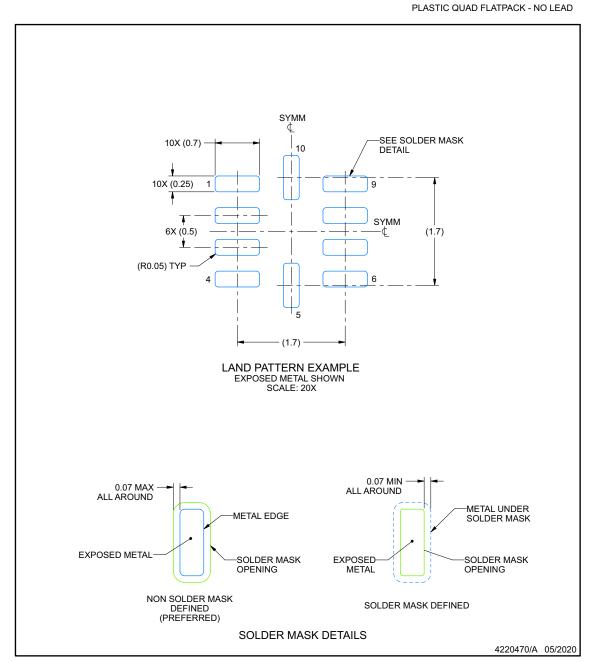




EXAMPLE BOARD LAYOUT

RUN0010A

WQFN - 0.8 mm max height



NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

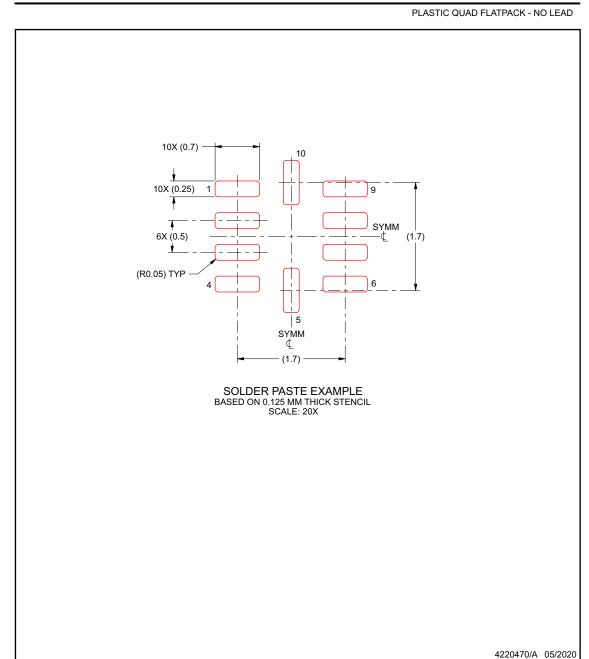




EXAMPLE STENCIL DESIGN

RUN0010A

WQFN - 0.8 mm max height



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



www.ti.com 14-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
PTHS4535DGKR	Active	Preproduction	VSSOP (DGK) 8	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	

⁽¹⁾ Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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SMALL OUTLINE PACKAGE



NOTES:

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- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.



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