











SLOS432B - APRIL 2004 - REVISED OCTOBER 2015

**THS4281** 

# THS4281 Very Low-Power, High-Speed, Rail-to-Rail Input and Output **Voltage-Feedback Operational Amplifier**

#### **Features**

- Very Low Quiescent Current: 750 µA (at 5 V)
- Rail-to-Rail Input and Output:
  - Common-Mode Input Voltage Extends 400 mV Beyond the Rails
  - Output Swings Within 150 mV From the Rails
- Wide -3-dB Bandwidth at 5 V:
  - 90 MHz at Gain = +1, 40 MHz at Gain = +2
- High Slew Rate: 35 V/µs
- Fast Settling Time (2-V Step):
  - 78 ns to 0.1%
  - 150 ns to 0.01%
- Low Distortion at Gain = +2,  $V_O = 2-V_{PP}$ , 5 V:
  - 91 dBc at 100 kHz, –67 dBc at 1 MHz
- Input Offset Voltage: 2.5 mV (Max at +25°C)
- Output Current > 30 mA (10- $\Omega$  Load, 5 V)
- Low Voltage Noise of 12.5 nV/√Hz
- Supply Voltages: +2.7 V, 3 V, +5 V, ±5 V, +15 V
- Packages: SOT23, MSOP, and SOIC

# **Applications**

- Portable/Battery-Powered Applications
- High Channel Count Systems
- **ADC Buffer**
- Active Filters
- Current Sensing

## 3 Description

Fabricated using the BiCom-II process, the THS4281 is a low-power, rail-to-rail input and output, voltagefeedback operational amplifier designed to operate over a wide power-supply range of 2.7-V to 15-V single supply, and ±1.35-V to ±7.5-V dual supply. Consuming only 750 µA with a unity gain bandwidth of 90 MHz and a high 35-V/µs slew rate, the THS4281 allows portable or other power-sensitive applications to realize high performance with minimal power. To ensure long battery life in portable applications, the quiescent current is trimmed to be less than 900 µA at +25°C, and 1 mA from -40°C to +85°C.

The THS4281 is a true single-supply amplifier with a specified common-mode input range of 400 mV beyond the rails. This allows for high-side current sensing applications without phase concerns. Its output swings to within 40 mV from the rails with  $10-k\Omega$  loads, and 150 mV from the rails with 1-kΩ loads.

The THS4281 has a good 0.1% settling time of 78 ns, and 0.01% settling time of 150 ns. The low THD of -87 dBc at 100 kHz, coupled with a maximum offset voltage of less than 2.5 mV, makes the THS4281 a good match for high-resolution ADCs sampling less than 2 MSPS.

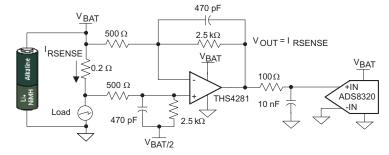
The THS4281 is offered in a space-saving SOT23-5 package, a small MSOP-8 package, and the industry standard SOIC-8 package.

# Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS4281	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

# High-side, Low Power Current-Sensing system



**Page** 



# **Table of Contents**

1	Features 1	7.3 Device Functional Modes	25
2	Applications 1	8 Application and Implementation	26
3	Description 1	8.1 Application Information	26
4	Revision History2	8.2 Typical Application	27
5	Pin Configuration and Functions	9 Power Supply Recommendations	29
6	Specifications4	9.1 Power-Supply Decoupling Techniques and Recommendations	29
	6.1 Absolute Maximum Ratings	10 Layout	29
	6.2 ESD Ratings	10.1 Layout Guidelines	
	6.3 Recommended Operating Conditions	10.2 Layout Examples	30
	6.4 Thermal Information	10.3 Thermal Considerations	
	6.5 Electrical Characteristics, V <sub>S</sub> = 3 V (V <sub>S+</sub> = 3 V, V <sub>S-</sub> = GND)	11 Device and Documentation Support	33
	6.6 Electrical Characteristics, $V_S = 5 \text{ V}$ ( $V_{S+} = 5 \text{ V}$ , $V_{S-} = 5 \text{ V}$	11.1 Documentation Support	33
	GND)	11.2 Community Resources	33
	6.7 Electrical Characteristics, V <sub>S</sub> = ±5 V9	11.3 Trademarks	33
	6.8 Dissipation Ratings 11	11.4 Electrostatic Discharge Caution	33
	6.9 Typical Characteristics	11.5 Glossary	33
7	Detailed Description24	12 Mechanical, Packaging, and Orderable	
	7.1 Overview	Information	33
	7.2 Feature Description24		

# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2009) to Revis	SION B

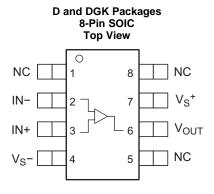
•	Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	. 1
•	Removed the Packaging/Ordering Information table	1
•	Removed Design Tools section	1
•	Updated Thermal Values	1
•	Removed the Applications Section Contents section	24
•	Removed the Bill of Materials section	24

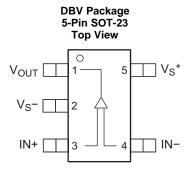
Changes from Original (April 2004) to Revision A		Page	÷
•	Updated document format to current standards	1	- 

•	Deleted Lead temperature specification from Absolute Maximum Ratings table	4
•	Revised Driving Capacitive Loads section	26
•	Changed Board Layout section; revised statements in fourth recommendation about how to make connections to	
	other wideband devices on the board	. 29



# 5 Pin Configuration and Functions





Note: NC Indicates there is no internal connection to these pins

## **Pin Functions**

	PIN					
NAME SOIC, VSSOP SOT-23		I/O	DESCRIPTION			
NC	1	_	_			
IN-	2	4	I	Negative input voltage pin		
IN+	3	3	I	Positive input voltage pin		
Vs-	4	2	I/O	Negative supply input voltage pin		
NC	5	_	_			
V <sub>out</sub>	6	1	0	Output voltage pin		
Vs+	7	5	I/O	Postive supply input voltage pin		
NC	8	_	_			



# 6 Specifications

#### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). (1)

	MIN	MAX	UNIT
Supply voltage, $V_{S-}$ to $V_{S+}$		16.5	V
Input voltage, V <sub>I</sub>		$\pm V_S \pm 0.5$	٧
Differential input voltage, V <sub>ID</sub>		±2	V
Output current, I <sub>O</sub>		±100	mA
Continuous power dissipation		pation Ratings Table	
Maximum junction temperature, any condition, <sup>(2)</sup> T <sub>J</sub>		+150	°C
Maximum junction temperature, continuous operation, long-term reliability (2) T <sub>J</sub>		125°	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

<sup>(1)</sup> The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

# 6.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3500	
V <sub>(ESD)</sub> Elec	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	V
		Machine Model (MM)	±100	

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

# 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Cumply voltage ()/ and )/ )	Dual supply	±1.35	±8.25	\/
Supply voltage, ( $V_{S+}$ and $V_{S-}$ )	Single supply	2.7	16.5	V

#### 6.4 Thermal Information

			THS4281			
THERMAL METRIC <sup>(1)</sup>		DBV (SOT-23)	D (SOIC)	DGK (VSSOP)	UNIT	
		5 PINS	8 PINS	8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	154.4	126.6	192.5	°C/W	
R <sub>0</sub> JC(top)	Junction-to-case (top) thermal resistance	115	69	77.7	°C/W	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.4	64.7	112.8	°C/W	
ΨЈТ	Junction-to-top characterization parameter	14.7	20.5	14.6	°C/W	
ΨЈВ	Junction-to-board characterization parameter	31	64.3	111.3	°C/W	
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W	

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

(2) This data was taken using the JEDEC standard High-K test PCB.

<sup>(2)</sup> The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device. recommended operating conditions.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



# 6.5 Electrical Characteristics, $V_S = 3 \text{ V (V}_{S+} = 3 \text{ V, V}_{S-} = \text{GND)}$

At G = +2,  $R_F$  = 2.49 k $\Omega$ , and  $R_L$  = 1 k $\Omega$  to 1.5 V,  $T_A$  = 25°C unless otherwise noted.

PARAMETER	TEST CO	ONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
	$G = +1, V_O = 100 \text{ mV}_{PP}, R_F =$	: 34 Ω		83		MHz
Consul Cinna I Dana davidah	$G = +2, V_O = 100 \text{ mV}_{PP}, R_F =$	$G = +2$ , $V_O = 100$ m $V_{PP}$ , $R_F = 1.65$ k $Ω$		40		MHz
Small-Signal Bandwidth	$G = +5$ , $V_O = 100 \text{ mV}_{PP}$ , $R_F =$	$G = +5$ , $V_O = 100 \text{ mV}_{PP}$ , $R_F = 1.65 \text{ k}\Omega$				MHz
	$G = +10, V_O = 100 \text{ mV}_{PP}, R_F$	$G = +10, V_O = 100 \text{ mV}_{PP}, R_F = 1.65 \text{ k}\Omega$				MHz
0.1-dB Flat Bandwidth	$G = +2, V_O = 100 \text{ mV}_{PP}, R_F =$	: 1.65 kΩ		20		MHz
Full-Power Bandwidth	G = +2, V <sub>O</sub> = 2 V <sub>PP</sub>			8		MHz
Slaw Pata	G = +1, V <sub>O</sub> = 2-V Step			26		V/µs
Slew Rate	G = −1, V <sub>O</sub> = 2-V Step			27		V/µs
Settling time to 0.1%	G = −1, V <sub>O</sub> = 1-V Step			80		ns
Settling time to 0.01%	G = -1, V <sub>O</sub> = 1-V Step			155		ns
Rise/Fall Times	G = +1, V <sub>O</sub> = 2-V Step			55		ns
AC PERFORMANCE— HARMONIC D	ISTORTION					
0 III : B: . ::	G = +2, V <sub>O</sub> = 2 V <sub>PP</sub> , f = 1 MH	$z, R_L = 1 k\Omega$		-52		ID.
Second Harmonic Distortion	G = +2, V <sub>O</sub> = 2 V <sub>PP</sub> , f = 100 k	Hz, RL = 1 kΩ		-52		aBc
Third Harmania Diay of	G = +2, V <sub>O</sub> = 2 V <sub>PP</sub> , f = 1 MH	z, RL = 1 kΩ		-69		-20
Third Harmonic Distortion	$G = +2$ , $V_O = 2 V_{PP}$ , $f = 100 k$	Hz, RL = 1 kΩ		-71	pA/√F dB	
	$G = +2, V_O = 2 V_{PP}, VO = 1 V_{PP}$	/PP, f = 10 kHz		0.003%		
THD + N	$G = +2, V_O = 2 V_{PP}, VO = 2 VPP, f = 10 kHz$ 0.03%					
Differential Gain (NTSC/PAL)	$G = +2, R_L = 150 \Omega$			0.05/0.08		
Differential Phase (NTSC/PAL)	G = +2, R <sub>1</sub> = 150 Ω			0.25/0.35		0
Input Voltage Noise	f = 100 kHz			12.5		nA/√ <del>Hz</del>
Input Current Noise	f = 100 kHz			1.5		pA/√ <del>Hz</del>
DC PERFORMANCE						•
Open-Loop Voltage Gain (AOL)				95		dB
· · · · · · · · · · · · · · · · · · ·		25°C		0.5	2.5	mV
Input Offset Voltage	V <sub>CM</sub> = 1.5 V	0°C to 70°C			3.5	
		-40°C to +85°C			3.5	
		0°C to 70°C			±7	
Average Offset Voltage Drift	$V_{CM} = 1.5 \text{ V}$	-40°C to +85°C			±7	μV/°C
		25°C		0.5	0.8	
Input Bias Current	V <sub>CM</sub> = 1.5 V	0°C to 70°C			1	μA
	S.M.	-40°C to +85°C			1	·
		0°C to 70°C		±2		
Average Bias Current Drift	V <sub>CM</sub> = 1.5 V	-40°C to +85°C		±2		nA/°C
		25°C		0.1	0.4	
Input Offset Current	V <sub>CM</sub> = 1.5 V	0°C to 70°C			0.5	μΑ
•	S.W.	-40°C to +85°C			0.5	•
		0°C to 70°C			±2	
Average Offset Current Drift	$V_{CM} = 1.5 \text{ V}$	-40°C to +85°C			±2	nA/°C
INPUT CHARACTERISTICS		<u> </u>	1			
	25°C		-0.3/3.3	-0.4/3.4		
Common-Mode Input Range	0°C to 70°C					V
,	-40°C to +85°C		-0.1/3.1 -0.1/3.1			-
		25°C	75	92		
Common-Mode Rejection Ratio	V <sub>CM</sub> = 0 V to 3 V	0°C to 70°C	70			dB
Common Mode Rejection Ratio	TOWN STEED	-40°C to +85°C	70			QD.
Input Resistance	Common-mode	10 0 10 100 0	70	100		ΜΩ
Input Capacitance	Common-mode/Differential		+	0.8/1.2		pF



# Electrical Characteristics, $V_S = 3 V (V_{S+} = 3 V, V_{S-} = GND)$ (continued)

At G = +2, R<sub>F</sub> = 2.49 k $\Omega$ , and R<sub>L</sub> = 1 k $\Omega$  to 1.5 V, T<sub>A</sub> = 25°C unless otherwise noted.

PARAMETER	TEST CONDITION	TEST CONDITIONS					
OUTPUT CHARACTERISTICS							
	$R_L = 10 \text{ k}\Omega$			0.04/2.96		V	
Output Valtage Suring		25°C	0.14/2.86	0.1/2.9			
Output Voltage Swing	$R_L = 1 k\Omega$	0°C to 70°C	0.2/2.8			V	
		-40°C to +85°C	0.2/2.8				
		25°C	18	23			
Output Current (Sourcing)	$R_L = 10 \Omega$	0°C to 70°C	15			mA	
		-40°C to +85°C	15				
		25°C	22	29			
Output Current (Sinking)	$R_L = 10 \Omega$	0°C to 70°C	19			mA	
		-40°C to +85°C	19				
Output Impedance	f = 1 MHz		1		Ω		
POWER SUPPLY							
	25°C	25°C					
Maximum Operating Voltage	0°C to 70°C	0°C to 70°C					
	-40°C to +85°C			16.5			
	25°C	2.7	3				
Minimum Operating Voltage	0°C to 70°C	0°C to 70°C				V	
	-40°C to +85°C	-40°C to +85°C					
	25°C	25°C					
Maximum Quiescent Current	0°C to 70°C	0°C to 70°C				mA	
	-40°C to +85°C				1		
	25°C	25°C					
Minimum Quiescent Current	0°C to 70°C		0.57			mA	
	-40°C to +85°C		0.55				
		25°C	70	90			
Power-Supply Rejection (+PSRR)	$V_{S+} = 3.25 \text{ V to } 2.75 \text{ V}, V_{S-} = 0 \text{ V}$	0°C to 70°C	65			dB	
		-40°C to +85°C	65				
		25°C	70	90			
Power-Supply Rejection (-PSRR)	$V_{S+} = 3 \text{ V}, V_{S-} = 0 \text{ V to } 0.65 \text{ V}$	0°C to 70°C	65			dB	
		-40°C to +85°C					

Product Folder Links: THS4281

Copyright © 2004–2015, Texas Instruments Incorporated



# 6.6 Electrical Characteristics, $V_S = 5 \text{ V} (V_{S+} = 5 \text{ V}, V_{S-} = \text{GND})$

At G = +2,  $R_F$  = 2.49 k $\Omega$ , and  $R_L$  = 1 k $\Omega$  to 2.5 V,  $T_A$  = 25°C unless otherwise noted.

PARAMETER	TEST CO	ONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
	$G = +1, V_O = 100 \text{ mV}_{PP},$	R <sub>F</sub> = 34 Ω		90		MHz
	$G = +2$ , $V_O = 100 \text{ mV}_{PP}$ ,	$R_F = 2 k\Omega$		40		MHz
Small-Signal Bandwidth	$G = +5, V_O = 100 \text{ mV}_{PP},$	$R_F = 2 k\Omega$		8		MHz
	$G = +10, V_O = 100 \text{ mV}_{PP}$			3.8		MHz
0.1-dB Flat Bandwidth	$G = +2$ , $V_O = 100 \text{ mV}_{PP}$ ,			20		MHz
Full-Power Bandwidth	$G = +2, V_O = 2 V_{PP}$	·		9		MHz
·	G = +1, V <sub>O</sub> = 2-V Step			31		V/µs
Slew Rate	G = -1, V <sub>O</sub> = 2-V Step			34		V/µs
Settling Time to 0.1%	G = -1, V <sub>O</sub> = 2-V Step			78		ns
Settling Time to 0.01%	G = -1, V <sub>O</sub> = 2-V Step			150		ns
Rise/Fall Times	G = +1, V <sub>O</sub> = 2-V Step			48		ns
AC PERFORMANCE— HARMON	IC DISTORTION					
0 111 : 5: : ::	$G = +2, V_O = 2 V_{PP}, f = 1$	MHz, $R_L = 1 k\Omega$		-67		in.
Second Harmonic Distortion	$G = +2, V_O = 2 V_{PP}, f = 1$	00 kHz, $R_L = 1$ kΩ		-92		dBc
Third Hannahai Distantia	$G = +2, V_O = 2 V_{PP}, f = 1$	MHz, $R_L = 1 k\Omega$		-76		JD.
Third Harmonic Distortion	$G = +2, V_O = 2 V_{PP}, f = 1$	00 kHz, $R_L = 1$ kΩ		-106		dBc
TUD . N	$G = +2, V_O = 2 V_{PP}, V_O =$		0.0009%			
THD + N	$G = +2, V_O = 2 V_{PP}, V_O =$	= 4 V <sub>PP</sub> , f = 10 kHz		0.0005%		
Differential Gain (NTSC/PAL)	0 0 0 450 0			0.11/0.17%		
Differential Phase (NTSC/PAL)	$G = +2$ , $R_L = 150 Ω$			0.11/0.14		0
Input Voltage Noise	f = 100 kHz			12.5		nV/√Hz
Input Current Noise	f = 100 kHz			1.5		pA/√Hz
DC PERFORMANCE	<u>'</u>		1		•	
	25°C	85	105			
Open-Loop Voltage Gain (AOL)	0°C to 70°C		80			dB
	-40°C to +85°C		80			
		25°C		2.5	0.5	
Input Offset Voltage	$V_{CM} = 2.5 \text{ V}$	0°C to 70°C			3.5	mV
		-40°C to +85°C			3.5	
Average Offset Voltage Drift	V - 2.5.V	0°C to 70°C		±7		μV/°C
Average Offset Voltage Difft	V <sub>CM</sub> = 2.5 V	-40°C to +85°C		±7		μν/ С
		25°C		0.5	0.8	
Input Bias Current	$V_{CM} = 2.5 \text{ V}$	0°C to 70°C			1	μΑ
		-40°C to +85°C			1	
Average Bias Current Drift	V 25 V	0°C to 70°C		±2		~ A /0 C
Average bias Current Dilit	V <sub>CM</sub> = 2.5 V	-40°C to +85°C		±2		nA/°C
		25°C		0.1	0.4	
Input Offset Current	V <sub>CM</sub> = 2.5 V	0°C to 70°C			0.5	μΑ
		-40°C to +85°C			0.5	
Average Offset Current Drift	V 25 V	0°C to 70°C		±2		nA/°C
Average Offset Current Drift	V <sub>CM</sub> = 2.5 V		±2		IIA/°C	
INPUT CHARACTERISTICS						
	25°C		-0.4/5.4	-0.3/5.3		
Common-Mode Input Range	0°C to 70°C		-0.1/5.1			V
, ,	-40°C to +85°C		-0.1/5.1			



# Electrical Characteristics, $V_S = 5 \text{ V}$ ( $V_{S+} = 5 \text{ V}$ , $V_{S-} = \text{GND}$ ) (continued)

At G = +2, R<sub>F</sub> = 2.49 k $\Omega$ , and R<sub>L</sub> = 1 k $\Omega$  to 2.5 V, T<sub>A</sub> = 25°C unless otherwise noted.

PARAMETER	TEST CONDI	MIN	TYP	MAX	UNIT		
		25°C	85	100			
Common-Mode Rejection Ratio	$V_{CM} = 0 V to 5 V$	0°C to 70°C	80			dB	
		-40°C to +85°C	80				
Input Resistance	Common-mode		100		МΩ		
Input Capacitance	Common-mode/Differential			0.8/1.2		pF	
OUTPUT CHARACTERISTICS			<b>-</b>		"		
	$R_L = 10 \text{ k}\Omega$			0.04/4.96		V	
0		25°C	0.2/4.8	0.15/4.85			
Output Voltage Swing	$R_L = 1 k\Omega$	0°C to 70°C	0.25/4.75			V	
		-40°C to +85°C	0.25/4.75				
		25°C	24	33			
Output Current (Sourcing)	R <sub>L</sub> = 10 Ω	0°C to 70°C	20			mA	
, , , ,		-40°C to +85°C	20				
		25°C	30	44		mA	
Output Current (Sinking)	R <sub>L</sub> = 10 Ω	0°C to 70°C	25				
		-40°C to +85°C	25				
Output Impedance		25°C		1			
	f = 1 MHz	0°C to 70°C				Ω	
		-40°C to +85°C					
POWER SUPPLY		1	<b>-</b>		"		
	25°C		5	16.5			
Maximum Operating Voltage	0°C to 70°C				16.5	V	
	-40°C to +85°C			16.5			
	25°C	2.7	5				
Minimum Operating Voltage	0°C to 70°C		2.7			V	
	-40°C to +85°C		2.7				
	25°C	25°C			0.9		
Maximum Quiescent Current	0°C to 70°C				0.98	mA	
	-40°C to +85°C						
	25°C		0.6	0.75			
Minimum Quiescent Current	0°C to 70°C		0.57			mA	
	-40°C to +85°C		0.55				
		25°C	80	100			
Power-Supply Rejection (+PSRR)	$V_{S+} = 5.5 \text{ V to } 4.5 \text{ V}, V_{S-} = 0$	0°C to 70°C	75			dB	
,	V	-40°C to +85°C	75				
		25°C	80	100			
Power-Supply Rejection (-PSRR)	$V_{S+} = 5 \text{ V}, V_{S-} = 0 \text{ V to } 1.0 \text{ V}$	0°C to 70°C	75			dB	
, , , , , , , , , , , , , , , , , ,		-40°C to +85°C	75				



# 6.7 Electrical Characteristics, $V_s = \pm 5 \text{ V}$

At G = +2,  $R_F$  = 2.49 k $\Omega$ , and  $R_L$  = 1 k $\Omega$ , unless otherwise noted

PARAMETER	TEST CO	NDITIONS	MIN	TYP	MAX	UNIT		
AC PERFORMANCE								
	$G = +1, V_O = 100 \text{ mV}_{PP},$	$R_F = 34 \Omega$		95		MHz		
O see III O's see al. De centro della	$G = +2, V_O = 100 \text{ mV}_{PP}$			40		MHz		
Small-Signal Bandwidth	$G = +5, V_O = 100 \text{ mV}_{PP}$			8		MHz		
	$G = +10, V_O = 100 \text{ mV}_{PP}$			3.8		MHz		
0.1-dB Flat Bandwidth	$G = +2, V_O = 100 \text{ mV}_{PP}$			20		MHz		
Full-Power Bandwidth	G = +1, V <sub>O</sub> = 2 V <sub>PP</sub>			9.5		MHz		
Olava Bata	G = +1, V <sub>O</sub> = 2-V Step			35		V/µs		
Slew Rate	$G = -1$ , $V_O = 2-V$ Step			35		V/µs		
Settling Time to 0.1%	$G = -1, V_O = 2-V Step$			78		ns		
Settling Time to 0.01%	G = -1, V <sub>O</sub> = 2-V Step			140		ns		
Rise/Fall Times	G = +1, V <sub>O</sub> = 2-V Step			45		ns		
AC PERFORMANCE— HARMONIC DIS	STORTION	1			'			
Second Harmonic Distortion	$G = +2, V_O = 2 V_{PP}, f = 1$	MHz, $R_L = 1 k\Omega$		-69		dBc		
	$G = +2$ , $V_O = 2 V_{PP}$ , $f = 10$	$00 \text{ kHz}, R_L = 1 \text{ k}Ω$		-76				
Third Harmonic Distortion	$G = +2, V_O = 2 V_{PP}, f = 1$	MHz, $R_L = 1 k\Omega$			dD.o			
	$G = +2$ , $V_O = 2 V_{PP}$ , $f = 100 \text{ kHz}$ , $R_L = 1 \text{ k}\Omega$					dBc		
THD + N	$G = +2, V_O = 2 V_{PP}, V_O =$	2 V <sub>PP</sub> , f = 10 kHz		0.0009				
	$G = +2, V_O = 2 V_{PP}, V_O =$	$G = +2, V_O = 2 V_{PP}, V_O = 4 V_{PP}, f = 10 \text{ kHz}$						
Differential Gain (NTSC/PAL)	C		(	0.03/0.03				
Differential Phase (NTSC/PAL)	$G = +2$ , $R_L = 150 Ω$			0.08/0.1		0		
Input Voltage Noise	f = 100 kHz			12.5		nV/√ <del>Hz</del>		
Input Current Noise	f = 100 kHz			1.5		pA/√Hz		
DC PERFORMANCE	1 - 100 M 12			1.0		p/ 0 11 12		
Open-Loop Voltage Gain (AOL)	25°C		90	108				
opon 200p vollage dam (, to2)	0°C to 70°C		85		dB			
	-40°C to +85°C		85			ab		
Input Offset Voltage	10 0 10 100 0	25°C		0.5	2.5			
par oncor rollage	$V_{CM} = 0 V$	0°C to 70°C		0.0	3.5	mV		
	CIVI	-40°C to +85°C			3.5			
Average Offset Voltage Drift		0°C to 70°C		±7				
Avoiago Giloot Voltago Dilit	$V_{CM} = 0 V$	-40°C to +85°C		±7		μV/°C		
Input Bias Current		25°C		0.5	0.8			
pat 2.do odo.it	$V_{CM} = 0 V$	0°C to 70°C		0.0	1	μA		
	- Civi	-40°C to +85°C			1	<b>P</b>		
Average Bias Current Drift		0°C to 70°C		±2				
,	$V_{CM} = 0 V$	-40°C to +85°C		±2		nA/°C		
Input Offset Current		25°C		0.1	0.4			
1	$V_{CM} = 0 V$	0°C to 70°C		0.1	0.5			
	GIVI	-40°C to +85°C			0.5	1		
Average Offset Current Drift		0°C to 70°C		±2	3.0			
	$V_{CM} = 0 V$		±2		nA/°C			



# Electrical Characteristics, $V_S = \pm 5 \text{ V}$ (continued)

At G = +2, R<sub>F</sub> = 2.49 k $\Omega$ , and R<sub>L</sub> = 1 k $\Omega$ , unless otherwise noted

PARAMETER	TEST CONDITIO	NS	MIN	TYP	MAX	UNIT	
INPUT CHARACTERISTICS							
Common-Mode Input Range	25°C	±5.3	±5.4				
	0°C to 70°C	0°C to 70°C					
	-40°C to +85°C		±5.1				
Common-Mode Rejection Ratio	$V_{CM} = -5 \text{ V to } +5 \text{ V}$	25°C	90	107			
		0°C to 70°C	85			dB	
		-40°C to +85°C	85				
Input Resistance	Common-mode			100		ΜΩ	
Input Capacitance	Common-mode/Differential			0.8/1.2		pF	
OUTPUT CHARACTERISTICS							
	$R_L = 10 \text{ k}\Omega$			±4.93		V	
Output Valtage Codes	$R_L = 1 k\Omega$	25°C	±4.6	±4.8			
Output Voltage Swing		0°C to 70°C	±4.5			V	
		-40°C to +85°C	±4.5				
Output Current (Sourcing)	R <sub>L</sub> = 10 Ω	25°C	35	48			
		0°C to 70°C	30			mA	
		-40°C to +85°C	30				
Output Current (Sinking)	R <sub>L</sub> = 10 Ω	25°C	45	60			
		0°C to 70°C	40			mA	
		-40°C to +85°C	40				
Output Impedance	f = 1 MHz			1		Ω	
POWER SUPPLY							
Maximum Operating Voltage	25°C		±5	±8.2 5			
	0°C to 70°C			±8.2 5	V		
	-40°C to +85°C			±8.2 5			
Minimum Operating Voltage	25°C	±1.35	±5				
	0°C to 70°C		±1.35			V	
	-40°C to +85°C	±1.35					
Maximum Quiescent Current	25°C			0.8	0.93		
	0°C to 70°C				1.0	mA	
	-40°C to +85°C				1.05		
Minimum Quiescent Current	25°C		0.67	0.8			
	0°C to 70°C		0.62			mA	
	-40°C to +85°C	0.6					
Power-Supply Rejection (+PSRR)	$V_{S+} = 5.5 \text{ V to } 4.5 \text{ V}, V_{S-} = 5.0 \text{ V}$	25°C	80	100			
		0°C to 70°C	75			dB	
		-40°C to +85°C	75				
Power-Supply Rejection (–PSRR)	$V_{S+} = 5 \text{ V}, V_{S-} = -5.5 \text{ V to } -4.5$	25°C	80	100			
,	V	0°C to 70°C	75			dB	
		-40°C to +85°C	75				



# 6.8 Dissipation Ratings

PACKAGE	POWER RATING <sup>(1)</sup>								
	T <sub>A</sub> < +25°C	T <sub>A</sub> = +85°C							
DBV (5)	391 mW	156 mW							
D (8)	1.02 W	410 mW							
DGK (8)	553 mW	221 mW							

<sup>(1)</sup> Power rating is determined with a junction temperature of +125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below +125°C for best performance and long term reliability.

 $V_S = 5 V$ 

# TEXAS INSTRUMENTS

# 6.9 Typical Characteristics

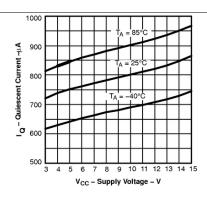


Figure 1. Quiescent Current vs Supply Voltage

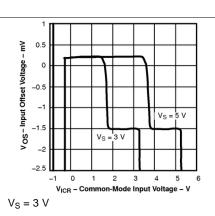


Figure 2. Input Offset Voltage vs Common-mode Input Voltage

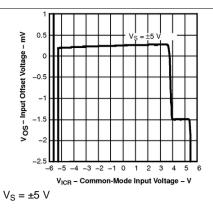


Figure 3. Input Offset Voltage vs Common-Mode Input Voltage

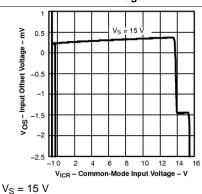


Figure 4. Input Offset Voltage vs Common-Mode Input Voltage

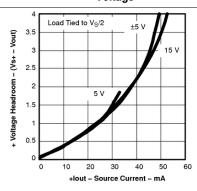


Figure 5. Positive Voltage Headroom vs Source Current

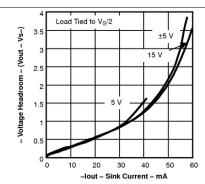


Figure 6. Negative Voltage Headroom vs Sink Current



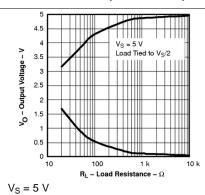


Figure 7. Output Voltage vs Load Resistance

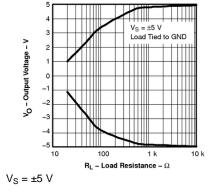


Figure 8. Output Voltage vs Load Resistance

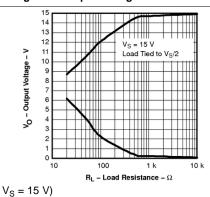


Figure 9. Output Voltage vs Load Resistance

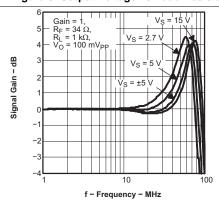


Figure 10. Frequency Response

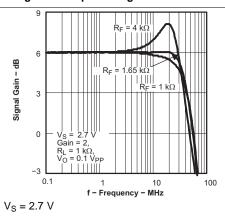


Figure 11. Frequency Response

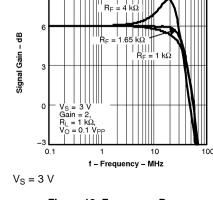
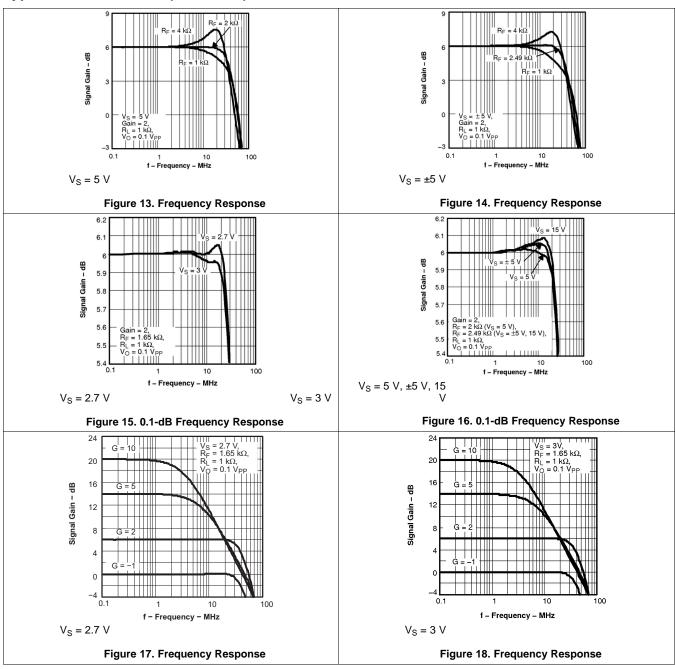


Figure 12. Frequency Response

# TEXAS INSTRUMENTS

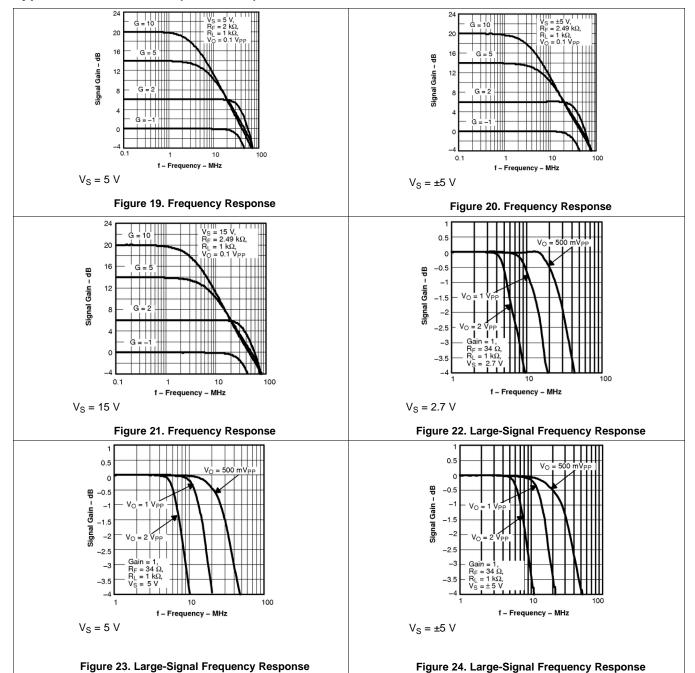
# **Typical Characteristics (continued)**



Submit Documentation Feedback

Copyright © 2004–2015, Texas Instruments Incorporated

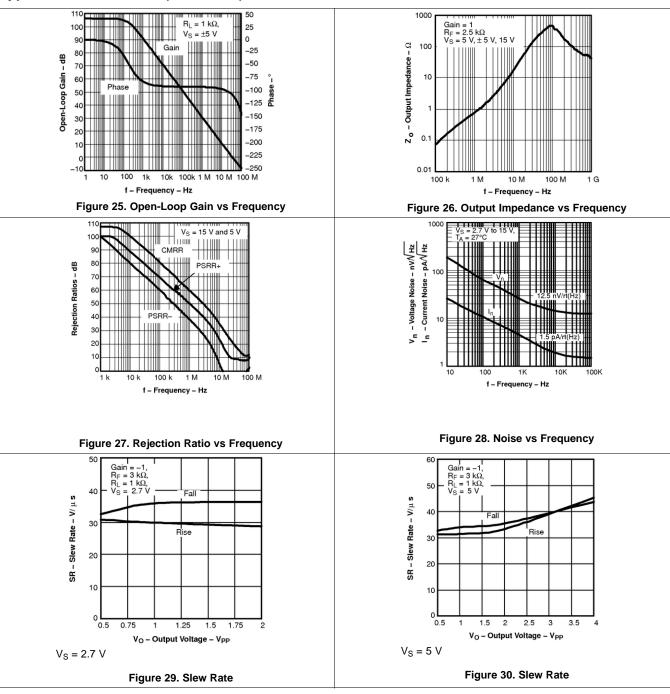




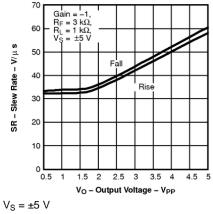
Submit Documentation Feedback

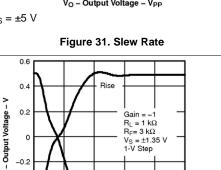
# TEXAS INSTRUMENTS

# **Typical Characteristics (continued)**





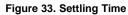




 $V_S = \pm 1.35 \text{ V}$ 

-0.4 -0.6

20



t - Time - ns

60

80

100

40

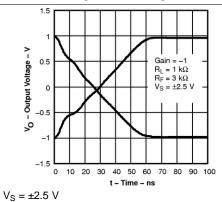


Figure 35. Settling Time

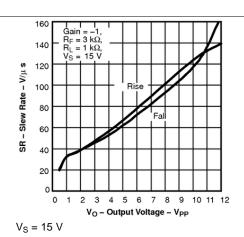
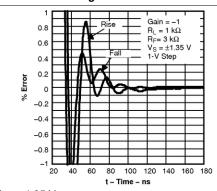
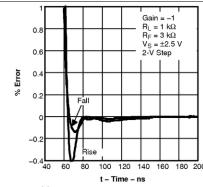


Figure 32. Slew Rate



 $V_S = \pm 1.35 \text{ V}$ 

## Figure 34. Settling Time

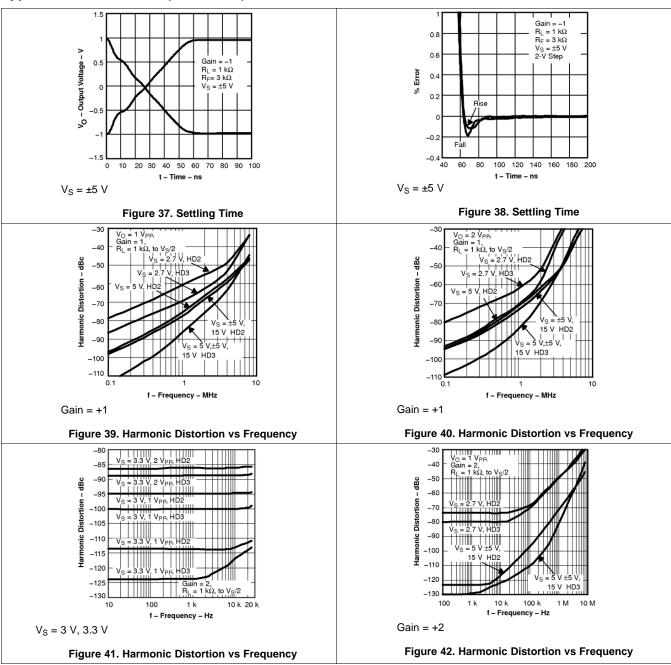


 $V_{S} = \pm 2.5 \ V$ 

Figure 36. Settling Time

Copyright © 2004–2015, Texas Instruments Incorporated







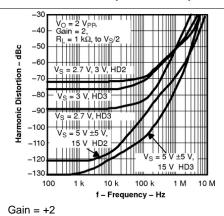


Figure 43. Harmonic Distortion vs Frequency

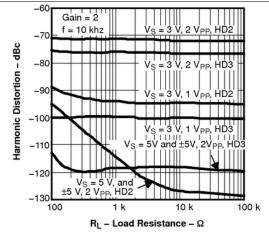
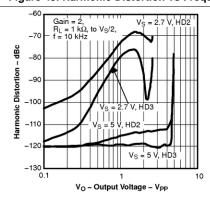


Figure 44. Harmonic Distortion vs Load Resistance



 $V_S = 2.7 V, 5 V$ 

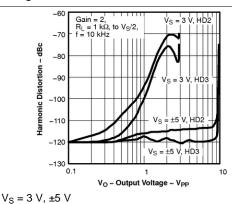
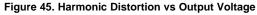


Figure 46. Harmonic Distortion vs Output Voltage



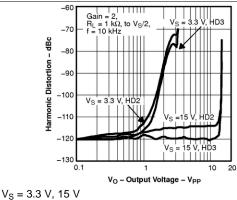


Figure 47. Harmonic Distortion vs Output Voltage

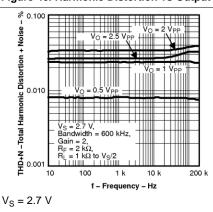


Figure 48. Total Harmonic Distortion + Noise vs Frequency

# TEXAS INSTRUMENTS

# **Typical Characteristics (continued)**

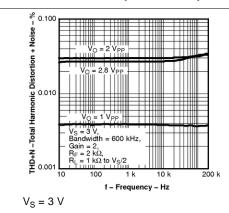


Figure 49. Total Harmonic Distortion + Noise vs Frequency

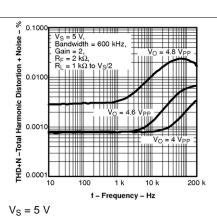


Figure 50. Total Harmonic Distortion + Noise vs Frequency

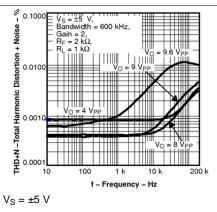


Figure 51. Total Harmonic Distortion + Noise vs Frequency

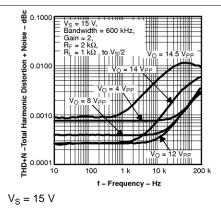


Figure 52. Total Harmonic Distortion + Noise vs Frequency

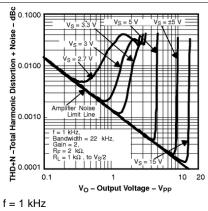


Figure 53. Total Harmonic Distortion + Noise vs Output Voltage

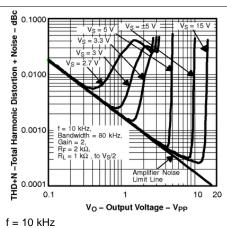


Figure 54. Total Harmonic Distortion + Noise vs Output Voltage

Submit Documentation Feedback

Copyright © 2004–2015, Texas Instruments Incorporated



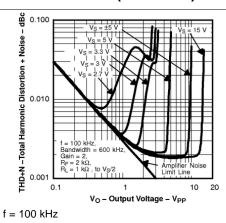


Figure 55. Total Harmonic Distortion + Noise vs Output Voltage

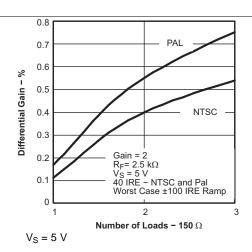


Figure 56. Differential Gain vs Number of Loads

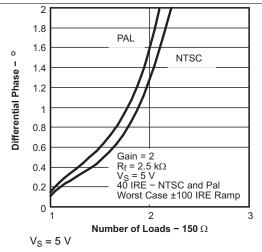


Figure 57. Differential Phase vs Number of Loads

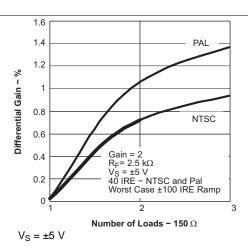


Figure 58. Differential Gain vs Number of Loads

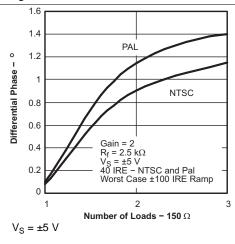


Figure 59. Differential Phase vs Number of Loads

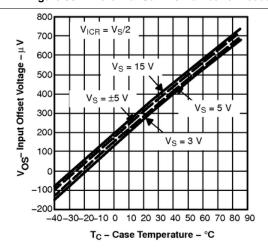


Figure 60. Input Offset Voltage vs Temperature

Copyright © 2004–2015, Texas Instruments Incorporated

# TEXAS INSTRUMENTS

# **Typical Characteristics (continued)**

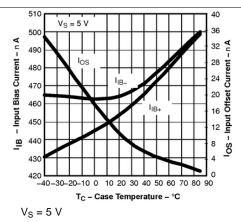


Figure 61. Input Bias and Offset Current vs Temperature

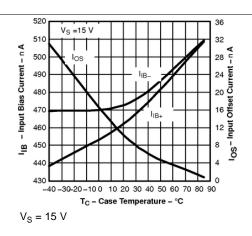


Figure 62. Input Bias and Offset Current vs Temperature

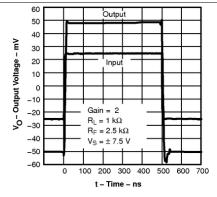


Figure 63. Small-Signal Transient Response

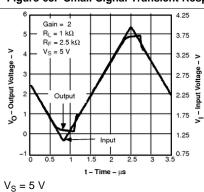


Figure 65. Overdrive Recovery Time

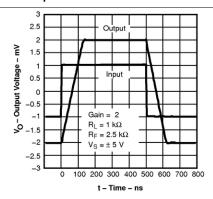


Figure 64. Large-Signal Transient Response

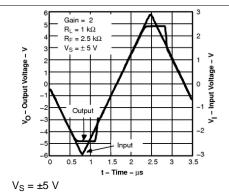
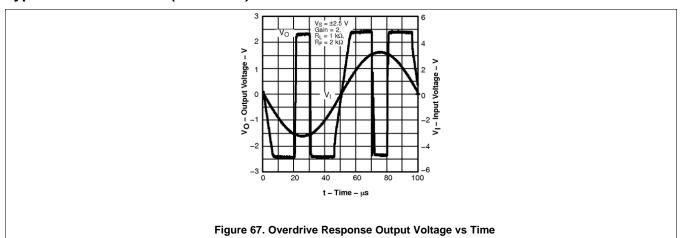


Figure 66. Overdrive Recovery Time

Submit Documentation Feedback





Product Folder Links: THS4281



# 7 Detailed Description

#### 7.1 Overview

#### 7.1.1 High-Speed Operational Amplifiers

The THS4281 is a unity gain stable, rail-to-rail input and output, voltage-feedback operational amplifier designed to operate from a single 2.7-V to 16.5-V power supply.

#### 7.2 Feature Description

#### 7.2.1 Wideband, Noninverting Operation

Figure 68 shows the noninverting gain configuration of 2 V/V used to demonstrate the typical performance curves.

Voltage feedback amplifiers can use a wide range of resistors values to set their gain with minimal impact on frequency response. Larger-valued resistors decrease loading of the feedback network on the output of the amplifier, but may cause peaking and instability. For a gain of +2, feedback resistor values between 1 k $\Omega$  and 4 k $\Omega$  are recommended for most applications. However, as the gain increases, the use of even higher feedback resistors can be used to conserve power. This is due to the inherent nature of amplifiers becoming more stable as the gain increases, at the expense of bandwidth. Figure 73 and Figure 74 show the THS4281 using feedback resistors of 10 k $\Omega$  and 100 k $\Omega$ . Be cautioned that using such high values with high-speed amplifiers is not typically recommended, but under certain conditions, such as high gain and good high-speed printed circuit board (PCB) layout practices, such resistances can be used.

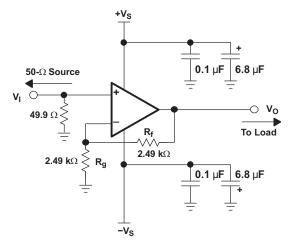


Figure 68. Wideband, Noninverting Gain Configuration

#### 7.2.2 Wideband, Inverting Operation

Figure 69 shows a typical inverting configuration where the input and output impedances and noise gain from Figure 68 are retained with an inverting circuit gain of -1 V/V.



#### Feature Description (continued)

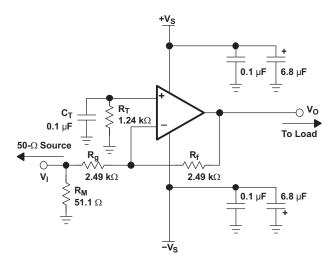


Figure 69. Wideband, Inverting Gain Configuration

In the inverting configuration, some key design considerations must be noted. One is that the gain resistor ( $R_g$ ) becomes part of the signal channel input impedance. If the input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PCB trace, or other transmission line conductors),  $R_g$  may be set equal to the required termination value and  $R_f$  adjusted to give the desired gain. However, care must be taken when dealing with low inverting gains, as the resulting feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2, setting  $R_g$  to 49.9  $\Omega$  for input matching, eliminates the need for  $R_M$  but requires a 100- $\Omega$  feedback resistor. The 100- $\Omega$  feedback resistor, in parallel with the external load, causes excessive loading on the amplifier output. To eliminate this excessive loading, it is preferable to increase both  $R_g$  and  $R_f$  values, as shown in Figure 69, and then achieve the input matching impedance with a third resistor ( $R_M$ ) to ground. The total input impedance is the parallel combination of  $R_g$  and  $R_M$ .

Another consideration in inverting amplifier design is setting the bias current cancellation resistor ( $R_T$ ) on the noninverting input. If the resistance is set equal to the total dc resistance presented to the device at the inverting terminal, the output dc error (due to the input bias currents) is reduced to the input offset current multiplied by  $R_T$ . In Figure 69, the dc source impedance presented at the inverting terminal is 2.49 k $\Omega$  || (2.49 k $\Omega$  + 25.3  $\Omega$ )  $\approx$  1.24 k $\Omega$ . To reduce the additional high-frequency noise introduced by the resistor at the noninverting input,  $R_T$  is bypassed with a 0.1- $\mu$ F capacitor to ground ( $C_T$ ).

#### 7.3 Device Functional Modes

This device has no specific function modes.



# 8 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

# 8.1 Application Information

#### 8.1.1 Single-Supply Operation

The THS4281 is designed to operate from a single 2.7-V to 16.5-V power supply. When operating from a single power supply, care must be taken to ensure the input signal and amplifier are biased appropriately to allow for the maximum output voltage swing and not violate  $V_{ICR}$ . The circuits shown in Figure 70 shows inverting and noninverting amplifiers configured for single-supply operation.

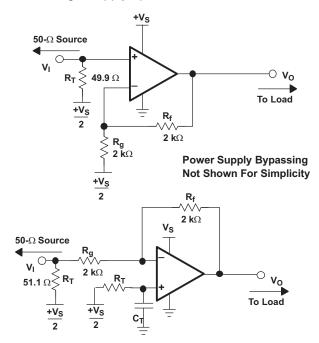


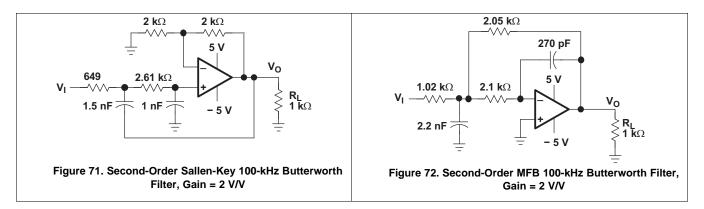
Figure 70. DC-Coupled Single Supply Operation

#### 8.1.2 Driving Capacitive Loads

One of the most demanding, and yet common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance, which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the THS4281 can be susceptible to instability and peaking when a capacitive load is placed directly on the output. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the feedback path that decreases the phase margin. When the primary considerations are frequency response flatness, pulse response fidelity, or distortion, a simple and effective solution is to isolate the capacitive load from the feedback loop by inserting a small series isolation resistor (for example,  $R_{(ISO)} = 100~\Omega$  for  $C_{LOAD} = 10~pF$  to  $R_{(ISO)} = 10~\Omega$  for  $C_{LOAD} = 1000~pF$ ) between the amplifier output and the capacitive load.



#### 8.2 Typical Application



#### 8.2.1 Design Requirements

Table 1 shows example design parameters and values for the typical application design example in Figure 71.

 DESIGN PARAMETERS
 VALUE

 Supply voltage
 ±5 V

 Amplifier topology
 Voltage feedback

 Gain
 2 V/V

 Filter requirement
 Second Order 100 KHz Sallen- Key Butterworth Filter

 Input/Output Requirements
 Rail to Rail

**Table 1. Design Parameters** 

# 8.2.2 Detailed Design Procedure

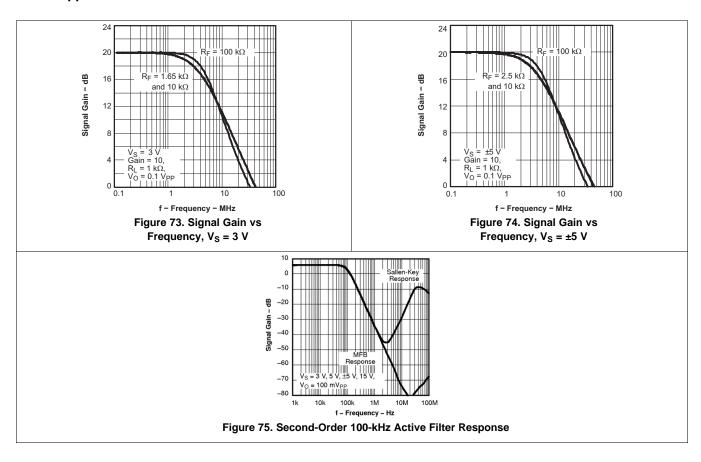
#### 8.2.2.1 Active Filtering With the THS4281

High-performance active filtering with the THS4281 is achievable due to the amplifier's good slew rate, wide bandwidth, and voltage-feedback architecture. Several options are available for high-pass, low-pass, bandpass, and bandstop filters of varying orders. Filters can be quite complex and time consuming to design. Several books and application reports are available to help design active filters. But, to help simplify the process and minimize the chance of miscalculations, Texas Instruments has developed a filter design program called FilterPro<sup>TM</sup>. FilterPro is available for download at no cost from TI's web site (www.ti.com).

The two most common low-pass filter circuits used are the Sallen-Key filter and the Multiple Feedback (MFB) – aka Rauch filter. FilterPro was used to determine a 2-pole Butterworth response filter with a corner (–3-dB) frequency of 100 kHz, which is shown in Figure 71 and Figure 72. One of the advantages of the MFB filter, a much better high-frequency rejection, is clearly shown in the response shown in Figure 75. This is due to the inherent R-C filter to ground being the first elements in the design of the MFB filter. The Sallen-Key design also has an R-C filter, but the capacitor connects directly to the output. At very high frequencies, where the amplifier's access loop gain is decreasing, the ability of the amplifier to reject high frequencies is severely reduced and allows the high-frequency signals to pass through the system. One other advantage of the MFB filter is the reduced sensitivity in component variation. This is important when using real-world components where capacitors can easily have ±10% variations.



#### 8.2.3 Application Curves





# 9 Power Supply Recommendations

# 9.1 Power-Supply Decoupling Techniques and Recommendations

Power-supply decoupling is a critical aspect of any high-performance amplifier design. Careful decoupling provides higher quality ac performance. The following guidelines ensure the highest level of performance.

- 1. Place decoupling capacitors as close to the power-supply inputs as possible, with the goal of minimizing the inductance.
- 2. Placement priority should put the smallest valued capacitors closest to the device.
- 3. Use of solid power and ground planes is recommended to reduce the inductance along power-supply return current paths (with the exception of the areas underneath the input and output pins as noted below).
- 4. A bulk decoupling capacitor is recommended (6.8 μF to 22 μF) within 1 inch, and a ceramic (0.1 μF) within 0.1 inch of the power input pins.

NOTE  The bulk capacitor may be shared by other operational amplifiers.	

#### 10 Layout

#### 10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the THS4281 requires careful attention to board layout parasitics and external component types. See the EVM layout figures (Figure 76 to Figure 79) in the Design Tools section.

Recommendations that optimize performance include:

- 1. Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability and on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- 2. Minimize the distance (< 0.1 inch) from the power-supply pins to high-frequency, 0.1-µF decoupling capacitors. Avoid narrow power and ground traces to minimize inductance. The power-supply connections should always be decoupled as described above.
- 3. Careful selection and placement of external components preserves the high-frequency performance of the THS4281. Resistors should be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film, axial-lead resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Excessively high resistor values can create significant phase lag that can degrade performance. Keep resistor values as low as possible, consistent with load-driving considerations. It is suggested that a good starting point for design is to set the  $R_f$  to 2 k $\Omega$  for low-gain, noninverting applications. Doing this automatically keeps the resistor noise terms reasonable and minimizes the effect of parasitic capacitance.
- 4. Connections to other wideband devices on the board should be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Low parasitic capacitive loads (< 4 pF) may not need an R<sub>(ISO)</sub>, because the THS4281 is nominally compensated to operate at unity gain (+1 V/V) with a 2-pF capacitive load. Higher capacitive loads without an R<sub>(ISO)</sub> are allowed as the signal gain increases. If a long trace is required, and the 6-dB signal loss intrinsic to a doubly terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A matching series resistor into the trace from the output of the THS4281 is used as well as a terminating shunt resistor at the input of the destination

Product Folder Links: THS4281

Copyright © 2004-2015, Texas Instruments Incorporated

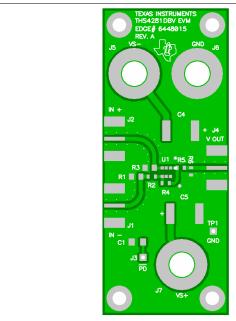


#### **Layout Guidelines (continued)**

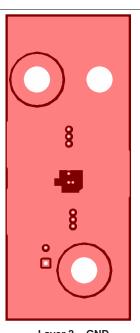
device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case, and use a series resistor ( $R_{(ISO)} = 10~\Omega$  to  $100~\Omega$ , as noted *Driving Capacitive Loads*) to isolate the capacitive load. If the input impedance of the destination device is low, there is signal attenuation due to the voltage divider formed by  $R_{(ISO)}$  into the terminating impedance. A  $50-\Omega$  environment is normally not necessary onboard, and in fact a higher impedance environment improves distortion as shown in the distortion versus load plots.

5. **Socketing a high-speed part like the THS4281 is not recommended.** The additional lead length and pinto-pin capacitance introduced by the socket can create a troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS4281 onto the board.

## 10.2 Layout Examples



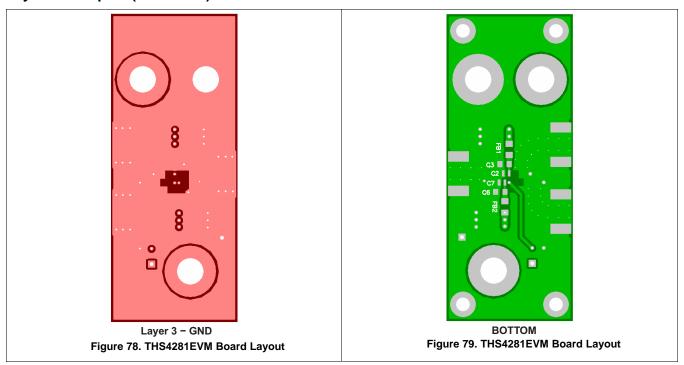
TOP
Figure 76. THS4281EVM Layout (Top Layer and Silkscreen



Layer 2 - GND Figure 77. THS4281EVM Board Layout



#### **Layout Examples (continued)**



## 10.3 Thermal Considerations

The THS4281 does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of +150°C is exceeded. For long-term dependability, the junction temperature should not exceed +125°C.

The thermal characteristics of the device are dictated by the package and the PCB. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = (T_{max} - T_A) / \theta_{JA}$$

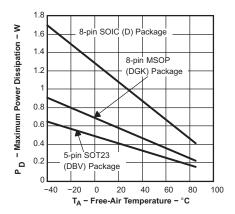
#### where

- P<sub>Dmax</sub> is the maximum power dissipation in the amplifier (W).
- T<sub>max</sub> is the absolute maximum junciton temperature (°C).
- T<sub>A</sub> is the ambient temperature (°C).
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ<sup>JC</sup> is the thermal coefficient from the silicon junctions to the case (°C/W).
- θ<sup>JA</sup> is the thermal coefficient from the case to ambient air (°C/W).

(1)



#### **Thermal Considerations (continued)**



 $\Theta_{JA}$  = 97.5°C/W for 8-Pin SOIC (D)

 $\Theta_{JA} = 180.8$ °C/W for 8-Pin MSOP (DGK)

 $\Theta_{JA}$  = 255.4°C/W for 5-Pin SOT-23 (DBV)

 $T_J = 125$ °C, No Airflow

Figure 80. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often maximum power dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS value can provide a reasonable analysis.



# 11 Device and Documentation Support

## 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation, see the following:

- PowerPAD Made Easy, application brief (SLMA004)
- PowerPAD Thermally Enhanced Package, technical brief (SLMA002)
- Active Low-Pass Filter Design, application report (SLOA049)
- FilterPro MFB and Sallen-Key Low-Pass Filter Design Program, application report (SBFA001)

#### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.3 Trademarks

FilterPro, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

# 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 11.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com

10-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
THS4281D	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4281
THS4281D.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4281
THS4281DBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AON
THS4281DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AON
THS4281DBVRG4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	-	Call TI	Call TI	-40 to 85	
THS4281DBVT	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AON
THS4281DBVT.A	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AON
THS4281DGK	Active	Production	VSSOP (DGK)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOO
THS4281DGK.A	Active	Production	VSSOP (DGK)   8	80   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOO
THS4281DGKR	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOO
THS4281DGKR.A	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOO
THS4281DR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4281
THS4281DR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4281

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

www.ti.com 10-Nov-2025

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

www.ti.com 23-May-2025

## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4281DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
THS4281DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
THS4281DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4281DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



www.ti.com 23-May-2025



#### \*All dimensions are nominal

7 III dilitoriolorio di o riorimica								
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
THS4281DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0	
THS4281DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0	
THS4281DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0	
THS4281DR	SOIC	D	8	2500	350.0	350.0	43.0	

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 23-May-2025

## **TUBE**



### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4281D	D	SOIC	8	75	505.46	6.76	3810	4
THS4281D.A	D	SOIC	8	75	505.46	6.76	3810	4



SMALL OUTLINE TRANSISTOR



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE PACKAGE



#### NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187.



SMALL OUTLINE PACKAGE



- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.



SMALL OUTLINE PACKAGE



- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025