



# 12-BIT 4 ANALOG INPUT, 6 MSPS, SIMULTANEOUS SAMPLING ANALOG-TO-DIGITAL CONVERTER

#### **FEATURES**

- Simultaneous Sampling of 4 Single-Ended Signals or 2 Differential Signals or Combination of Both
- Signal-to-Noise and Distortion Ratio:
   68 dB at f<sub>1</sub> = 2 MHz
- Differential Nonlinearity Error: ±1 LSB
- Integral Nonlinearity Error: ±1.5 LSB
- Auto-Scan Mode for 2, 3, or 4 Inputs
- 3-V or 5-V Digital Interface Compatible
- Low Power: 216 mW Max at 5 V
- Power Down: 1 mW Max
- 5-V Analog Single Supply Operation
- Internal Voltage References . . . 50 PPM/°C and ±5% Accuracy
- Glueless DSP Interface
- Parallel μC/DSP Interface

#### **APPLICATIONS**

- Radar Applications
- Communications
- Control Applications
- High-Speed DSP Front-End
- Automotive Applications

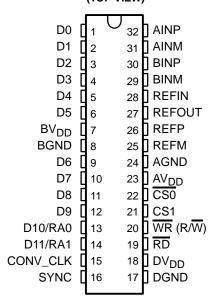
#### DESCRIPTION

The THS1207 is a CMOS, low-power, 12-bit, 6 MSPS analog-to-digital converter (ADC). The speed, resolution, bandwidth, and single-supply operation are suited for applications in radar, imaging, high-speed acquisition, and communications. A multistage pipelined architecture with output error correction logic provides for no missing codes over the full operating temperature range. Internal control registers are used

to program the ADC into the desired mode. The THS1207 consists of four analog inputs, which are sampled simultaneously. These inputs can be selected individually and configured to single-ended or differential-inputs. Internal reference voltages for the ADC (1.5 V and 3.5 V) are provided. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

The THS1207C is characterized for operation from 0°C to 70°C, the THS1207I is characterized for operation from –40°C to 85°C.

# DA PACKAGE (TOP VIEW)



#### **ORDERING INFORMATION**

	PACKAGED DEVICE
TA	TSSOP (DA)
0°C to 70°C	THS1207CDA
-40°C to 85°C	THS1207IDA



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### **ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range unless otherwise noted(1)

			UNITS
	DGND to DVD	)	–0.3 V to 6.5 V
Supply voltage range	BGND to BVDI	)	-0.3 V to 6.5 V
	AGND to AVD[	)	-0.3 V to 6.5 V
Analog input voltage ran	ge		AGND -0.3 V to AV <sub>DD</sub> + 1.5 V
Reference input voltage			$-0.3 \text{ V} + \text{ AGND to AV}_{DD} + 0.3 \text{ V}$
Digital input voltage rang	је		-0.3 V to BV <sub>DD</sub> /DV <sub>DD</sub> + 0.3 V
Operating virtual junction	n temperature rang	е, ТЈ	−40°C to 150°C
On another for a sintense		THS1207C	0°C to 70°C
Operating free-air temperature range, T <sub>A</sub>		THS1207I	−40°C to 85°C
Storage temperature range, T <sub>Stg</sub>			−65°C to 150°C
Lead temperature 1,6 m	260°C		

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### RECOMMENDED OPERATING CONDITIONS

POWER SUPPLY		MIN	NOM	MAX	UNIT
	$AV_{DD}$	4.75	5	5.25	
Supply voltage	$DV_DD$	4.75	5	5.25	V
	$BV_DD$	3		5.25	

ANALOG AND REFERENCE INPUTS	MIN	NOM	MAX	UNIT
Analog input voltage in single-ended configuration	VREFM		$V_{REFP}$	V
Common-mode input voltage V <sub>CM</sub> in differential configuration	1	2.5	4	V
External reference voltage, VREFP (optional)		3.5	AV <sub>DD</sub> -1.2	V
External reference voltage, V <sub>REFM</sub> (optional)	1.4	1.5		V
Input voltage difference, REFP – REFM		2		V

DIGITAL INPUTS	MIN	NOM	MAX	UNIT	
High level insert values V	BV <sub>DD</sub> = 3.3 V	2			V
High-level input voltage, V <sub>IH</sub>	BV <sub>DD</sub> = 5.25 V	2.6			V
Levelevelienstveltene Vo	BV <sub>DD</sub> = 3.3 V			0.6	V
Low-level input voltage, V <sub>IL</sub>	BV <sub>DD</sub> = 5.25 V			0.6	V
Input CONV_CLK frequency	$DV_{DD} = 4.75 \text{ V to } 5.25 \text{ V}$	0.1		6	MHz
CONV_CLK pulse duration, clock high, tw(CONV_CLKH)	DV <sub>DD</sub> = 4.75 V to 5.25 V	80	83	5000	ns
CONV_CLK pulse duration, clock low, tw(CONV_CLKL)	DV <sub>DD</sub> = 4.75 V to 5.25 V	80	83	5000	ns
On section from air to see section. To	THS1207CDA	0		70	°C
Operating free-air temperature, T <sub>A</sub>	THS1207IDA	-40		85	-0



## **ELECTRICAL CHARACTERISTICS**

over recommended operating conditions,  $AV_{DD} = DV_{DD} = 5 \text{ V}$ ,  $BV_{DD} = 3.3 \text{ V}$ ,  $V_{REWF} = \text{internal}$  (unless otherwise noted)

DIGITAL SPECIFICATIONS							
	PARAMETER TEST CONDITIONS				TYP	MAX	UNIT
Digital	inputs						
lн	High-level input current	DV <sub>DD</sub> = digital	inputs	-50		50	μΑ
Ι <sub>Ι</sub> L	Low-level input current	Digital input = 0	Digital input = 0 V			50	μΑ
Ci	Input capacitance				5		pF
Digital	outputs						
Vон	High-level output voltage	I <sub>OH</sub> = -50 μA	DV 00V5V	BV <sub>DD</sub> -0.5			V
VOL	Low-level output voltage	Ι <sub>Ο</sub> L = 50 μΑ	$BV_{DD} = 3.3 \text{ V}, 5 \text{ V}$			0.4	٧
loz	High-impedance-state output current	CS1 = DGND,	CS0 = DV <sub>DD</sub>	-10		10	μΑ
CO	Output capacitance				5		pF
CL	Load capacitance at databus D0 – D11					30	pF

#### **ELECTRICAL CHARACTERISTICS**

over recommended operating conditions, AVDD = DVDD = 5 V, BVDD = 3.3 V, f<sub>S</sub> = 6 MSPS, V<sub>RFF</sub> = internal (unless otherwise noted)

DC SPI	ECIFICATIONS					
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			12			Bits
Accura	су					
	Integral nonlinearity, INL				±1.5	LSB
	Differential nonlinearity, DNL				±1	LSB
	Official commen	After calibration in single-ended mode		20		LSB
	Offset error	After calibration in differential mode	-20		20	LSB
	Gain error		-20		20	LSB
Analog	input					
	Input capacitance			15		pF
	Input leakage current	VAIN = VREFM to VREFP			±10	μΑ
Interna	l voltage reference					
	Accuracy, V <sub>REFP</sub>		3.3	3.5	3.7	V
	Accuracy, V <sub>REFM</sub>		1.4	1.5	1.6	V
	Temperature coefficient			50		PPM/°C
	Reference noise			100		μV
	Accuracy, REFOUT		2.475	2.5	2.525	V
Power	supply					
I <sub>DDA</sub>	Analog supply current	$AV_{DD} = DV_{DD} = 5 \text{ V}, BV_{DD} = 3.3 \text{ V}$		36	40	mA
IDDD	Digital supply current	$AV_{DD} = DV_{DD} = 5 \text{ V},  BV_{DD} = 3.3 \text{ V}$		0.5	3	mA
I <sub>DDB</sub>	Buffer supply current	$AV_{DD} = DV_{DD} = 5 \text{ V},  BV_{DD} = 3.3 \text{ V}$		1.5	4	mA
	Power dissipation	$AV_{DD} = DV_{DD} = 5 \text{ V},  BV_{DD} = 3.3 \text{ V}$		186	216	mW
	Power dissipation in power down with conversion clock inactive	$AV_{DD} = DV_{DD} = 5 \text{ V},  BV_{DD} = 3.3 \text{ V}$			0.25	mW



## **ELECTRICAL CHARACTERISTICS**

over recommended operating conditions,  $V_{REF}$  = internal,  $f_S$  = 6 MSPS,  $f_I$  = 2 MHz at -1 dBFS (unless otherwise noted)

AC SPE	AC SPECIFICATIONS, AV <sub>DD</sub> = DV <sub>DD</sub> = 5 V, BV <sub>DD</sub> = 3.3 V, C <sub>L</sub> < 30 pF						
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
CINIAD	Cinnal to naise until a distantion	Differential mode	63	63		40	
SINAD	Signal-to-noise ratio + distortion	Single-ended mode	62	64		dB	
CNID	Cinnal to naise ratio	Differential mode	64	69		4D	
SNR	Signal-to-noise ratio	Single-ended mode	64	68		dB	
TUD	Total harmonia distantian	Differential mode		-70	-67	dB	
THD	Total harmonic distortion	Single-ended mode		-68	-64	ав	
ENOB E	Effective number of bits Differential mode 10.17 10.5 Single-ended mode 10 10.3		Bits				
		Single-ended mode	10	10.3		DIIS	
CEDD	Occasions for a description of	Differential mode	67	71		40	
SFDR	Spurious free dynamic range	Single-ended mode	65	69		dB	
Analog	Input						
	Full-power bandwidth with a source impedance of 150 $\Omega$ in differential configuration.	Full cools singulars 2 dB		96		N 41 1-	
	Full-power bandwidth with a source impedance of 150 $\Omega$ in single-ended configuration.	Full scale sinewave, –3 dB	54		MHz		
	Small-signal bandwidth with a source impedance of 150 $\Omega$ in differential configuration.	100 m)/nn cinquique 2 dD	96 54		MHz		
	Small-signal bandwidth with a source impedance of 150 $\Omega$ in single-ended configuration.	100 mVpp sinewave, –3 dB			IVI⊓Z		

## **TIMING REQUIREMENTS**

 $\mbox{AV}_{\mbox{DD}} = \mbox{DV}_{\mbox{DD}} = \mbox{5 V}, \mbox{ BV}_{\mbox{DD}} = \mbox{3.3 V}, \mbox{ V}_{\mbox{REF}} = \mbox{internal}, \mbox{ C}_{\mbox{L}} < \mbox{30 pF}$ 

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<sup>t</sup> pipe	Latency			5		CONV CLK
tsu(CONV_CLKL-READL)	Setup time, CONV_CLK low before CS valid		10			ns
tsu(READH-CONV_CLKL)	Setup time, CS invalid to CONV_CLK low		20			ns
td(CONV_CLKL-SYNCL)	Delay time, CONV_CLK low to SYNC low				10	ns
td(CONV_CLKL-SYNCH)	Delay time, CONV_CLK low to SYNC high				10	ns



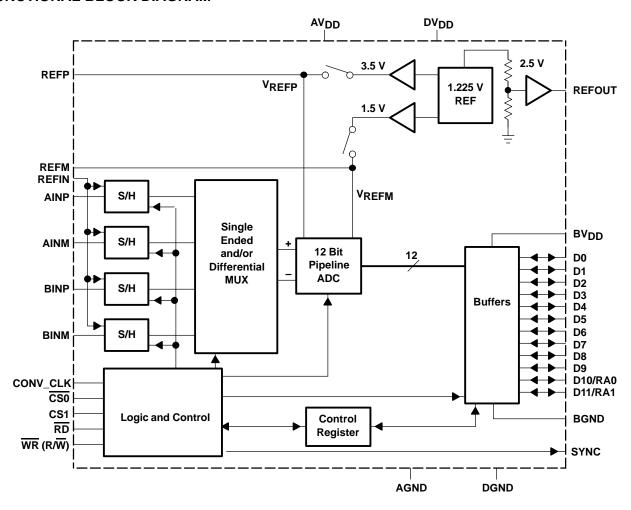
## **Terminal Functions**

TERMINAL			
NAME	NO.	1/0	DESCRIPTION
AINP	32	Ι	Analog input, single-ended or positive input of differential channel A
AINM	31	I	Analog input, single-ended or negative input of differential channel A
BINP	30	I	Analog input, single-ended or positive input of differential channel B
BINM	29	I	Analog input, single-ended or negative input of differential channel B
AV <sub>DD</sub>	23	I	Analog supply voltage
AGND	24	I	Analog ground
BV <sub>DD</sub>	7	I	Digital supply voltage for buffer
BGND	8	I	Digital ground for buffer
CONV_CLK	15	I	Digital input. This input is the conversion clock input.
CS0	22	I	Chip select input (active low)
CS1	21	I	Chip select input (active high)
DGND	17	I	Digital ground. Ground reference for digital circuitry.
DV <sub>DD</sub>	18	I	Digital supply voltage
D0 – D9	1–6, 9–12	I/O/Z	Digital input, output; D0 = LSB
D10/RA0	13	I/O/Z	Digital input, output. The data line D10 is also used as an address line (RA0) for the control register. This is required for writing to the control register 0 and control register 1. See Table 7.
D11/RA1	14	I/O/Z	Digital input, output (D11 = MSB). The data line D11 is also used as an address line (RA1) for the control register. This is required for writing to control register 0 and control register 1. See Table 7.
REFIN	28	I	Common-mode reference input for the analog input channels. It is recommended that this pin be connected to the reference output REFOUT.
REFP	26	I	Reference input, requires a bypass capacitor of 10 $\mu$ F to AGND in order to bypass the internal reference voltage. An external reference voltage at this input can be applied. This option can be programmed through control register 0. See Table 8.
REFM	25	I	Reference input, requires a bypass capacitor of 10 $\mu$ F to AGND in order to bypass the internal reference voltage. An external reference voltage at this input can be applied. This option can be programmed through control register 0. See Table 8.
REFOUT	27	0	Analog fixed reference output voltage of 2.5 V. Sink and source capability of 250 $\mu$ A. The reference output requires a capacitor of 10 $\mu$ F to AGND for filtering and stability.
RD(1)	19	I	The RD input is used only if the WR input is configured as a write only input. In this case, it is a digital input, active low as a data read select from the processor. See timing section.
SYNC	16	0	Synchronization output. This signal indicates in a multichannel operation that data of channel A is brought to the digital output and can therefore be used for synchronization.
WR (R/W)(1)	20	I	This input is programmable. It functions as a read-write input R/W and can also be configured as a write-only input WR, which is active low and used as data write select from the processor. In this case, the RD input is used as a read input from the processor. See timing section.

<sup>(1)</sup> The start-conditions of  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  (R/W) are unknown. The first access to the ADC has to be a write access to initialize the ADC.

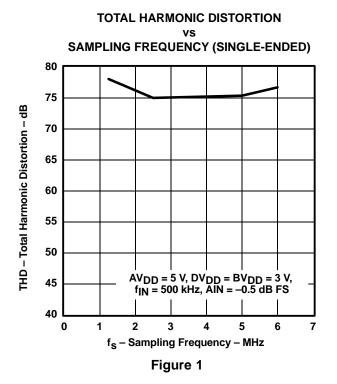


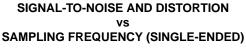
## **FUNCTIONAL BLOCK DIAGRAM**





SINAD - Signal-to-Noise and Distortion - dB





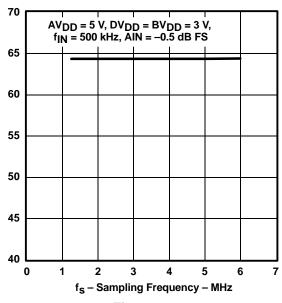
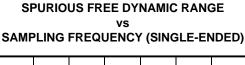


Figure 2



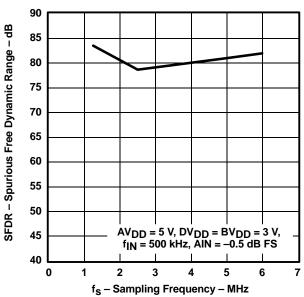


Figure 3

SIGNAL-TO-NOISE vs SAMPLING FREQUENCY (SINGLE-ENDED)

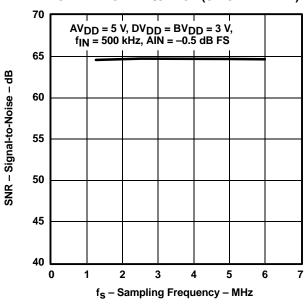
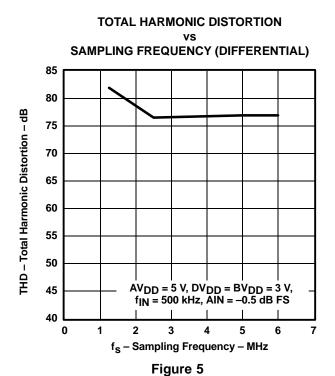
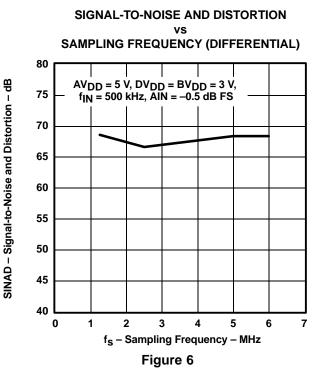


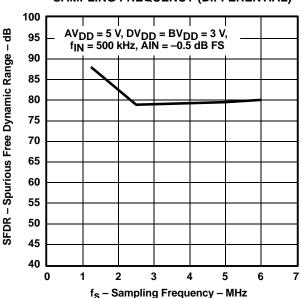
Figure 4

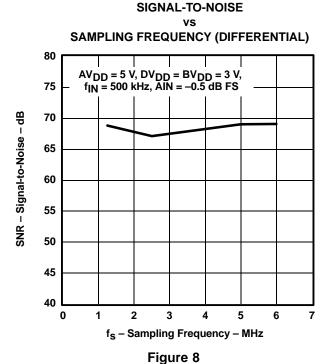








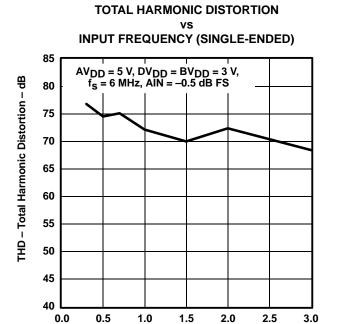




SIGNAL-TO-NOISE AND DISTORTION



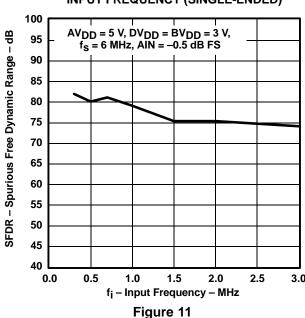
#### TYPICAL CHARACTERISTICS



 $f_i$  – Input Frequency – MHz Figure 9

#### **INPUT FREQUENCY (SINGLE-ENDED)** 80 $AV_{DD} = 5 \text{ V}, DV_{DD} = BV_{DD} = 3 \text{ V},$ $f_S = 6 \text{ MHz}, \text{ AIN} = -0.5 \text{ dB FS}$ SINAD - Signal-to-Noise and Distortion - dB 75 70 65 60 55 50 45 40 0.0 0.5 1.0 1.5 2.0 2.5 3.0 fi - Input Frequency - MHz Figure 10





SIGNAL-TO-NOISE
vs
INPUT FREQUENCY (SINGLE-ENDED)

80
AVDD = 5 V, DVDD = BVDD = 3 V,
f<sub>S</sub> = 6 MHz, AIN = -0.5 dB FS

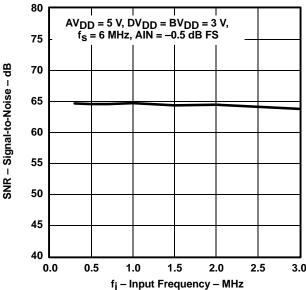
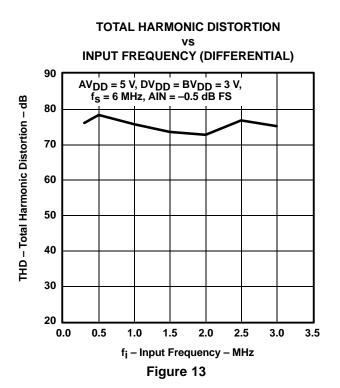
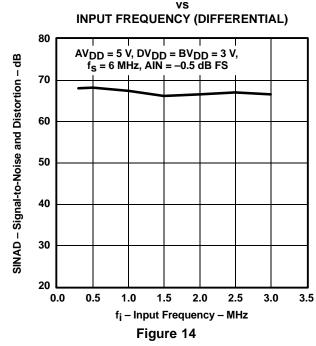


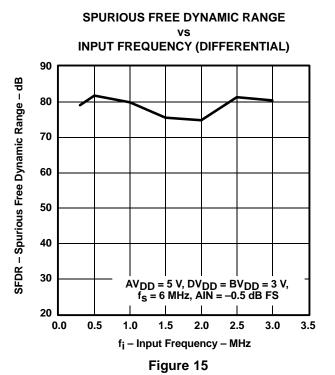
Figure 12

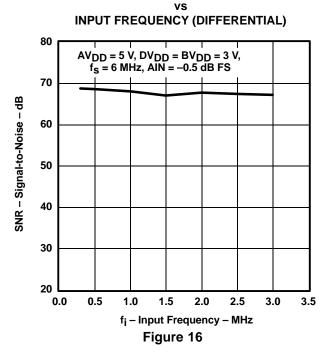






SIGNAL-TO-NOISE AND DISTORTION

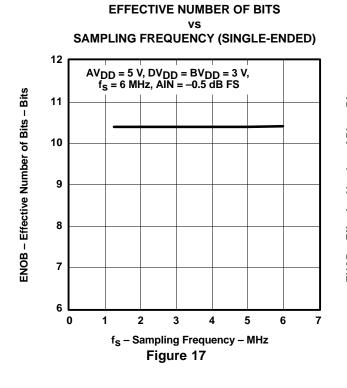


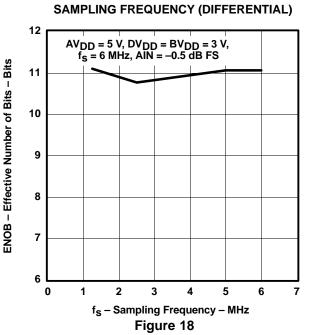


**SIGNAL-TO-NOISE** 

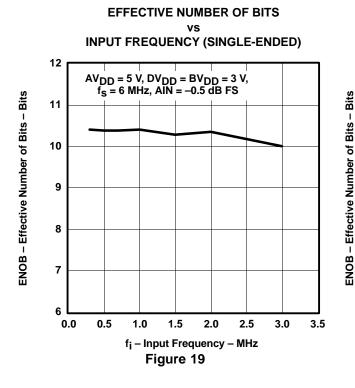
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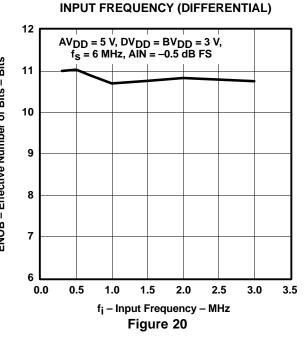






**EFFECTIVE NUMBER OF BITS** 



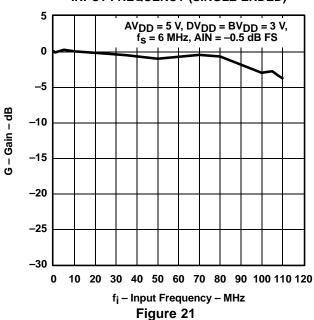


**EFFECTIVE NUMBER OF BITS** 

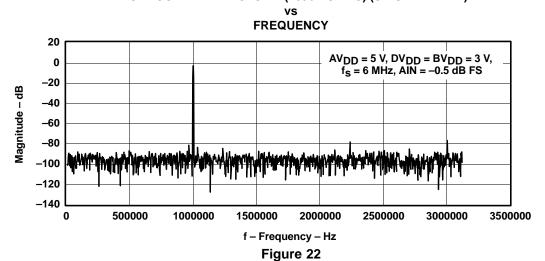
vs



GAIN vs INPUT FREQUENCY (SINGLE-ENDED)



## FAST FOURIER TRANSFORM (4096 POINTS) (SINGLE-ENDED)





## FAST FOURIER TRANSFORM (4096 POINTS) (DIFFERENTIAL)

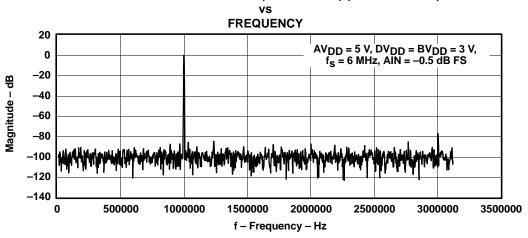


Figure 23

#### **DIFFERENTIAL NONLINEARITY**

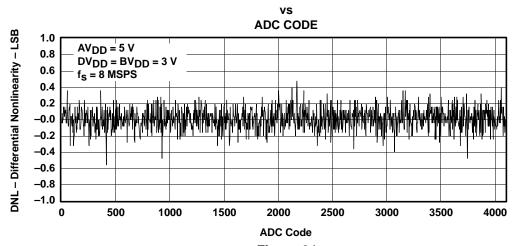


Figure 24

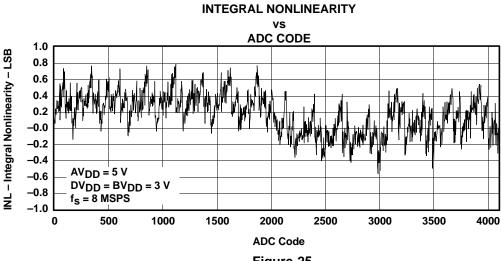


Figure 25



#### **DETAILED DESCRIPTION**

#### Reference Voltage

The THS1207 has a built-in reference, which provides the reference voltages for the ADC. VREFP is set to 3.5 V and VREFM is set to 1.5 V. An external reference can also be used through two reference input pins, REFP and REFM, if the reference source is programmed as external. The voltage levels applied to these pins establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively.

#### **Analog Inputs**

The THS1207 consists of 4 analog inputs, which are sampled simultaneously. These inputs can be selected individually and configured as single-ended or differential inputs. The desired analog input channel can be programmed.

#### Converter

The THS1207 uses a 12-bit pipelined multistaged architecture, which achieves a high sample rate with low power consumption. The THS1207 distributes the conversion over several smaller ADC sub-blocks, refining the conversion with progressively higher accuracy as the device passes the results from stage to stage. This distributed conversion requires a small fraction of the number of comparators used in a traditional flash ADC. A sample-and-hold amplifier (SHA) within each of the stages permits the first stage to operate on a new input sample while the second through the eighth stages operate on the seven preceding samples.

#### **Conversion Clock**

An external clock signal with a duty cycle of 50% has to be applied to the clock input (CONV\_CLK). A new conversion is started with every falling edge of the applied clock signal. The conversion values are available at the output with a latency of 5 clock cycles.

#### SYNC

In multichannel mode, the first SYNC signal is delayed by [7+ (# Channels Sampled)] cycles of the CONV\_CLK after a SYNC reset. This is due to the latency of the pipeline architecture of the THS1207.

#### Sampling Rate

The maximum possible conversion rate per channel is dependent on the selected analog input channels. Table 1 shows the maximum conversion rate in the continuous conversion mode for different combinations.

NUMBER OF **MAXIMUM CONVERSION CHANNEL CONFIGURATION CHANNELS RATE PER CHANNEL** 6 MSPS 1 single-ended channel 2 single-ended channels 2 3 MSPS 3 single-ended channels 3 2 MSPS 4 single-ended channels 4 1.5 MSPS 1 differential channel 1 6 MSPS 2 differential channels 2 3 MSPS 2 1 single-ended and 1 differential channel 3 MSPS 2 single-ended and 1 differential channels 3 2 MSPS

**Table 1. Maximum Conversion Rate** 

The maximum conversion rate in the continuous conversion mode per channel, fc, is given by:

$$fc = \frac{6 \text{ MSPS}}{\text{\# channels}}$$

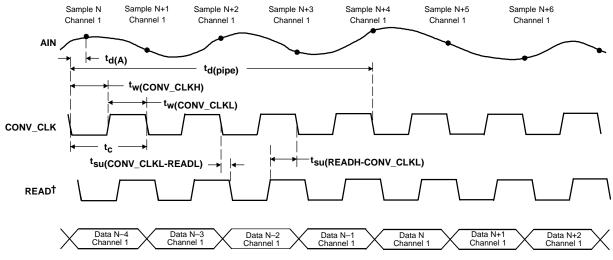
#### Conversion

During conversion the ADC operates with a free running external clock applied to the input CONV\_CLK. With every falling edge of the CONV\_CLK signal a new converted value is available to the databus with the corresponding read signal. The THS1207 allows up to four analog input to be selected. The inputs can be configured as two differential channels, four single-ended channels or a combination of differential and single-ended.



To provide the system with channel information, the THS1207 utilizes an active low SYNC signal. When operated in a multichannel configuration, the SYNC signal is active low when data from channel one is available to the databus. When operated in single-channel mode (single-ended or differential operation) the SYNC signal is disabled.

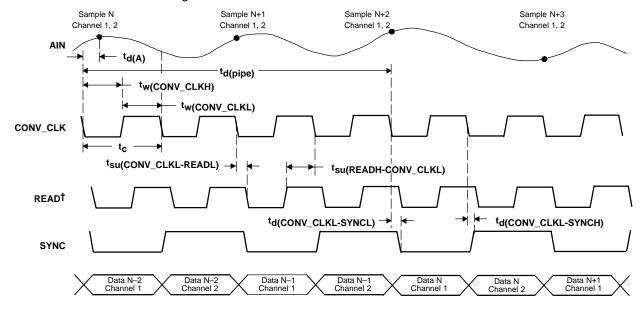
Figure 26 shows the timing of the conversion when one analog input channel is selected. The maximum throughput rate is 6 MSPS in this mode. There is a certain timing relationship required for the read signal with respect to the conversion clock. This can be seen in Figure 26 and in the read and SYNC timing table. A more detailed description of the timing is given in the timing section and signal description of the THS1207.



TREAD is the logical combination from CS0, CS1 and RD

Figure 26. Conversion Timing in 1-Channel Operation

Figure 27 shows the conversion timing when 2 analog input channels are selected. The maximum throughput rate per channel is 3 MSPS in this mode. The data flow in the bottom of the figure shows in which order the converted data is available to the databus. The signal SYNC is active low when data of channel one is available to the databus. The data of channel one is followed by the data of channel two before channel one is again available and the SYNC signal is active low.

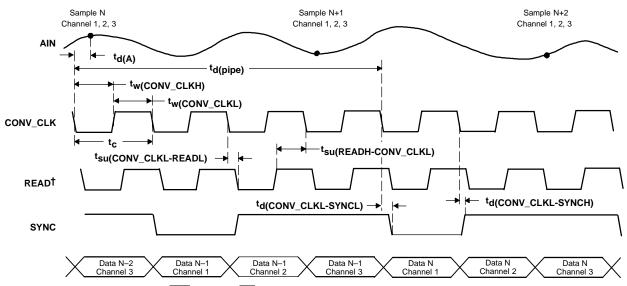


TREAD is the logical combination from CS0, CS1 and RD

Figure 27. Conversion Timing in 2-Channel Operation



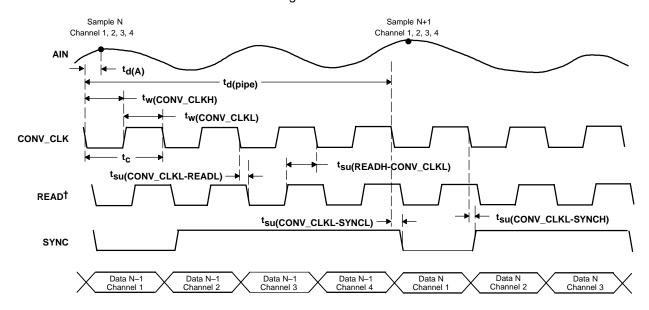
Figure 28 shows the conversion timing when 3 analog input channels are selected. The maximum throughput rate per channel is 2 MSPS in this mode. The data flow in the bottom of the figure shows in which order the converted data is available to the databus. The signal SYNC is always active low if data of channel one is available to the databus. The data of channel one is followed by the data of channel two and data of channel three before channel one is again available to the data bus and SYNC is active low.



TREAD is the logical combination from CS0, CS1 and RD

Figure 28. Conversion Timing in 3-Channel Operation

Figure 29 shows the timing of the conversion mode where 4 analog input channels are selected. The maximum throughput rate per channel is 1.5 MSPS in this mode. The data flow in the bottom of the figure shows in which order the converted data is available to the databus. The signal SYNC is active low when data of channel one is available to the databus. The data of channel one is followed by the data of channel two, data of channel three and data of channel 4 before channel one is again available to the data bus and SYNC is active low.



TREAD is the logical combination from CS0, CS1 and RD

Figure 29. Timing of Continuous Conversion Mode (4-channel operation)



## **DIGITAL OUTPUT DATA FORMAT**

The digital output data format of the THS1207 can either be in binary format or in twos complement format. The following tables list the digital outputs for the analog input voltages.

Table 2. Binary Output Format for Single-Ended Configuration

SINGLE-ENDED, BINARY OUTPUT					
ANALOG INPUT VOLTAGE DIGITAL OUTPUT CODE					
AIN = V <sub>REFP</sub>	FFFh				
$AIN = (V_{REFP} + V_{REFM})/2$	800h				
AIN = VREFM	000h				

Table 3. Twos Complement Output Format for Single-Ended Configuration

SINGLE-ENDED, TWOS COMPLEMENT					
ANALOG INPUT VOLTAGE DIGITAL OUTPUT CODE					
AIN = V <sub>REFP</sub>	7FFh				
$AIN = (V_{REFP} + V_{REFM})/2$	000h				
AIN = VREFM	800h				

**Table 4. Binary Output Format for Differential Configuration** 

DIFFERENTIAL, BINARY OUTPUT										
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE									
$V_{in} = AINP - AINM$ $V_{REF} = V_{REFP} - V_{REFM}$										
V <sub>in</sub> = V <sub>REF</sub>	FFFh									
$V_{in} = 0$	800h									
Vin = -VREF	000h									

Table 5. Twos Complement Output Format for Differential Configuration

DIFFERENTIAL, BINARY OUTPUT									
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE								
$V_{in} = AINP - AINM$ $V_{REF} = V_{REFP} - V_{REFM}$									
Vin = VREF	7FFh								
$V_{in} = 0$	000h								
Vin = -V <sub>REF</sub>	800h								



#### **ADC CONTROL REGISTER**

The THS1207 contains two 10-bit wide control registers (CR0, CR1) in order to program the device into the desired mode. The bit definitions of both control registers are shown in Table 6.

Table 6. Bit Definitions of Control Register CR0 and CR1

REG	BIT 9	BIT 8	BIT 7	BIT 6 BIT 5		BIT 7 BIT 6 BIT 5 BIT 4 BIT 3 BIT 2		BIT 1	BIT 0	
CR0	TEST1	TEST0	SCAN	DIFF1	DIFF1 DIFF0		CHSEL0	PD	RESERVED	VREF
CR1	RBACK	OFFSET	BIN/2's	R/W	RESERVED	RESERVED	RESERVED	RESERVED	SRST	RESET

#### Writing to Control Register 0 and Control Register 1

The 10-bit wide control register 0 and control register 1 can be programmed by addressing the desired control register and writing the register value to the ADC. The addressing is performed with the upper data bits D10 and D11, which function in this case as address lines RA0 and RA1. During this write process, the data bits D0 to D9 contain the desired control register value. Table 7 shows the addressing of each control register.

**Table 7. Control Register Addressing** 

D0 – D9	D10/RA0	D11/RA1	Addressed Control Register
Desired register value	0	0	Control register 0
Desired register value	1	0	Control register 1
Desired register value	0	1	Reserved for future
Desired register value	1	1	Reserved for future

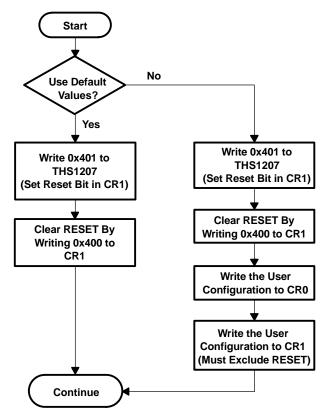


Figure 30. THS1207 Configuration Flow



## **Control Register 0 (see Table 7)**

BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	RESERVED	VREF

## Table 8. Control Register 0 Bit Functions

BITS	RESET VALUE	NAME	FUNCTION
0	0	VREF	Vref select: Bit $0 = 0 \rightarrow$ The internal reference is used Bit $0 = 1 \rightarrow$ The external reference voltage is used for the ADC
1	0	RESERVED	RESERVED
2	0	PD	Power down.  Bit $2 = 0 \rightarrow$ The ADC is active  Bit $2 = 1 \rightarrow$ Power down
			The reading and writing to and from the digital outputs is possible during power down.
3, 4	0,0	CHSEL0, CHSEL1	Channel select Bit 3 and bit 4 select the analog input channel of the ADC. Refer to Table 9.
5,6	1,0	DIFF0, DIFF1	Number of differential channels Bit 5 and bit 6 contain information about the number of selected differential channels. Refer to Table 9.
7	0	SCAN	Autoscan enable Bit 7 enables or disables the autoscan function of the ADC. Refer to Table 9.
8,9	0,0	TEST0, TEST1	Test input enable Bit 8 and bit 9 control the test function of the ADC. Three different test voltages can be measured. This feedback allows the check of all hardware connections and the ADC in its bits.  Refer to Table 10 for selection of the three different test voltages.



#### **ANALOG INPUT CHANNEL SELECTION**

The analog input channels of the THS1207 can be selected via bits 3 to 7 of control register 0. One channel (single-ended or differential) is selected via bit 3 and bit 4 of control register 0. Bit 5 controls the selection between single-ended and differential configuration. Bit 6 and bit 7 select the autoscan mode, if more than one input channel is selected. Table 9 shows the possible selections.

**Table 9. Analog Input Channel Configurations** 

BIT 7 SCAN	BIT 6 DIFF1	BIT 5 DIFF0	BIT 4 CHSEL1	BIT 3 CHSEL0	DESCRIPTION OF THE SELECTED INPUTS
0	0	0	0	0	Analog input AINP (single ended)
0	0	0	0	1	Analog input AINM (single ended)
0	0	0	1	0	Analog input BINP (single ended)
0	0	0	1	1	Analog input BINM (single ended)
0	0	1	0	0	Differential channel (AINP-AINM)
0	0	1	0	1	Differential channel (BINP-BINM)
1	0	0	0	1	Autoscan two single ended channels: AINP, AINM, AINP,
1	0	0	1	0	Autoscan three single ended channels: AINP, AINM, BINP, AINP,
1	0	0	1	1	Autoscan four single ended channels: AINP, AINM, BINP, BINM, AINP,
1	0	1	0	1	Autoscan one differential channel and one single ended channel AINP, (BINP–BINM), AINP, (BINP–BINM),
1	0	1	1	0	Autoscan one differential channel and two single ended channel AINP, AINM, (BINP-BINM), AINP,
1	1	0	0	1	Autoscan two differential channels (AINP-AINM), (BINP-BINM), (AINP-AINM),
0	0	1	1	0	Reserved
0	0	1	1	1	Reserved
1	0	0	0	0	Reserved
1	0	1	0	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved
1	1	0	1	0	Reserved
1	1	0	1	1	Reserved
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Reserved

#### **Test Mode**

The test mode of the ADC is selected via bit 8 and bit 9 of control register 0. The different selections are shown in Table 10.

Table 10. Test Mode

BIT 9 TEST1	BIT 8 TEST0	OUTPUT RESULT
0	0	Normal mode
0	1	VREFP
1	0	((VREFM)+(VREFP))/2
1	1	<sup>∨</sup> REFM

Three different options can be selected. This feature allows support testing of hardware connections between the ADC and the processor.



## **Control Register 1 (see Table 7)**

BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	1	RBACK	OFFSET	BIN/2s	R/W	RESERVED	RESERVED	RESERVED	RESERVED	SRST	RESET

## Table 11. Control Register 1 Bit Functions

BITS	RESET VALUE	NAME	FUNCTION
0	0	RESET	Reset
			Writing a 1 into this bit resets the device and sets the control register 0 and control register 1 to the reset values. To bring the device out of reset, a 0 has to be written into this bit.
1	0	SRST	Writing a 1 into this bit resets the sync generator. When running in multichannel mode, this must be set during the configuration cycle.
2, 3	0,0	RESERVED	Always write 0
4	1	RESERVED	Always write 0
5	1	RESERVED	Always write 0
6	0	R/W	R/W, RD/WR selection Bit 6 of control register 1 controls the function of the inputs RD and WR. When bit 6 in control register 1 is set to
			1, WR becomes a RW input and RD is disabled. From now on a read is signalled with RW high and a write with R/W as a low signal. If bit 6 in control register 1 is set to 0, the input RD becomes a read input and the input WR becomes a write input.
7	0	BIN/2s	Complement select
			If bit 7 of control register 1 is set to 0, the output value of the ADC is in twos complement. If bit 7 of control register 1 is set to 1, the output value of the ADC is in binary format. Refer to Table 2 through Table 5.
8	0	OFFSET	Offset cancellation mode Bit $8 = 0 \rightarrow$ normal conversion mode Bit $8 = 1 \rightarrow$ offset calibration mode
			If a 1 is written into bit 8 of control register 1, the device internally sets the inputs to zero and does a conversion. The conversion result is stored in an offset register and subtracted from all conversions in order to reduce the offset error.
9	0	RBACK	Debug mode Bit $9 = 0 \rightarrow$ normal conversion mode Bit $9 = 1 \rightarrow$ enable debug mode
			When bit 9 of control register 1 is set to 1, debug mode is enabled. In this mode, the contents of control register 0 and control register 1 can be read back. The first read after bit 9 is set to 1 contains the value of control register 0. The second read after bit 9 is set to 1 contains the value of control register 1. To bring the device back into normal conversion mode, this bit has to be set back to 0 by writing again to control register 1.



#### TIMING AND SIGNAL DESCRIPTION OF THE THS1207

The reading from the <u>THS1207</u> and writing to the THS1207 is performed by using the chip select inputs ( $\overline{CS0}$ , CS1), the write input WR and the read input  $\overline{RD}$ . The write input is configurable to a combined read/write input ( $R/\overline{W}$ ). This is desired in cases where the connected processor consists of a combined read/write output signal ( $R/\overline{W}$ ). The two chip select inputs can be used to interface easily to a processor.

Reading from the THS1207 takes place by an internal  $\overline{RD}_{int}$  signal, which is generated from the logical combination of the external signals  $\overline{CS0}$ , CS1 and  $\overline{RD}$  (see Figure 6). This signal is then used to strobe out the words and to enable the output buffers. The last external signal (either  $\overline{CS0}$ , CS1 or  $\overline{RD}$ ) to become valid makes  $\overline{RD}_{int}$  active while the write input ( $\overline{WR}$ ) is inactive. The first of those external signals switching to an inactive state deactivates  $\overline{RD}_{int}$  again.

Writing to the THS1207 takes place by an internal  $\overline{WR}_{int}$  signal, which is generated from the logical combination of the external signals  $\overline{CS0}$ , CS1 and  $\overline{WR}$ . This signal strobes the control words into the control registers 0 and 1. The last external signal (either  $\overline{CS0}$ , CS1 or  $\overline{WR}$ ) to become valid switches  $\overline{WR}_{int}$  active while the read input (RD) is inactive. The first of those external signals going to its inactive state deactivates  $\overline{WR}_{int}$  again.

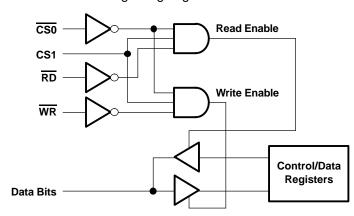


Figure 31. Logical Combination of CSO, CS1, RD, and WR



## Read Timing (using RD, RD-controlled)

Figure 32 shows the read-timing behavior when the  $\overline{WR}(R/\overline{W})$  input is programmed as a write-input only. The input  $\overline{RD}$  acts as the read-input in this configuration. This timing is called  $\overline{RD}$ -controlled because  $\overline{RD}$  is the last external signal of  $\overline{CSO}$ , CS1, and  $\overline{RD}$  which becomes valid.

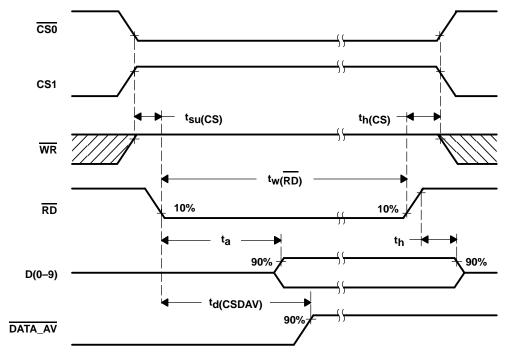


Figure 32. Read Timing Diagram Using RD (RD-controlled)

#### Read Timing Parameter (RD-controlled)

	PARAMETER	MIN	TYP	MAX	UNIT
t <sub>su(CS)</sub>	Setup time, RD low to last CS valid	0			ns
ta	Access time, last CS valid to data valid	0		10	ns
td(CSDAV)	Delay time, last CS valid to DATA_AV inactive		12		ns
th	Hold time, first CS invalid to data invalid	0		5	ns
th(CS)	Hold time, RD change to first CS invalid	5			ns
tw(RD)	Pulse duration, RD active	10			ns



## Write Timing (using WR, WR-controlled)

Figure 33 shows the write-timing behavior when the  $\overline{WR}(R/\overline{W})$  input is programmed as a write input  $\overline{WR}$  only. The input  $\overline{RD}$  acts as the read input in this configuration. This timing is called  $\overline{WR}$ -controlled because  $\overline{WR}$  is the last external signal of  $\overline{CSO}$ , CS1, and  $\overline{WR}$  which becomes valid.

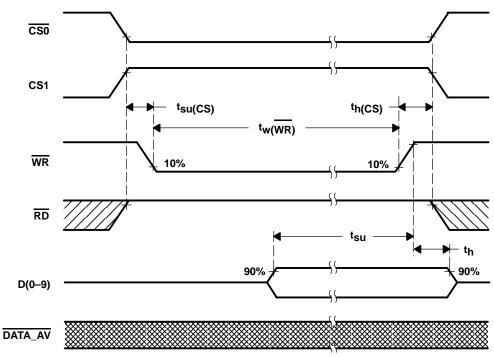


Figure 33. Write Timing Diagram Using WR (WR-controlled)

## Write Timing Parameter Using WR (WR-controlled)

	PARAMETER	MIN	TYP	MAX	UNIT
t <sub>su(CS)</sub>	Setup time, CS stable to last WR valid	0			ns
t <sub>su</sub>	Setup time, data valid to first WR invalid	5			ns
th	Hold time, WR invalid to data invalid	2			ns
th(CS)	Hold time, WR invalid to CS change	5			ns
tw(WR)	Pulse duration, WR active	10			ns



## Read Timing (using R/W, CS0-controlled)

Figure 34 shows the read-timing behavior when the  $\overline{WR}(R/\overline{W})$  input is programmed as a combined read-write input  $R/\overline{W}$ . The  $\overline{RD}$  input has to be tied to high-level in this configuration. This timing is called  $\overline{CSO}$ -controlled because  $\overline{CSO}$  is the last external signal of  $\overline{CSO}$ , CS1, and  $R/\overline{W}$  which becomes valid. The reading of the data must be done with a certain timing relative to the conversion clock CONV\_CLK, as illustrated in Figure 34.

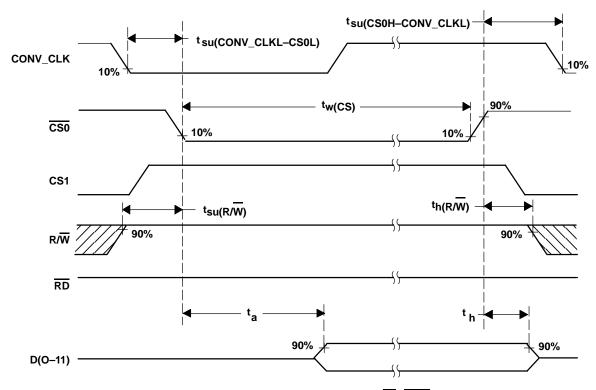


Figure 34. Read Timing Diagram Using R/W (CS0-controlled)

#### Read Timing Parameter (CSO-controlled)

	MIN	TYP	MAX	UNIT	
tsu(CONV_CLKL-CSOL)	Setup time, CONV_CLK low before CS valid	10			ns
t <sub>su(CSOH-CONV_CLKL)</sub>	Setup time, CS invalid to CONV_CLK low	20			ns
t <sub>su(R/W)</sub>	Setup time, $R/\overline{W}$ high to last CS valid	0			ns
ta	Access time, last CS valid to data valid	0		10	ns
th	Hold time, first CS invalid to data invalid	0		5	ns
th(R/W)	Hold time, first external CS invalid to R/W change	5			ns
t <sub>w(CS)</sub>	Pulse duration, CS active	10			ns



## Write Timing Diagram (using R/W, CSO-controlled)

Figure 35 shows the write-timing behavior when the  $\overline{WR}(R/\overline{W})$  input is programmed as a combined read-write input  $R/\overline{W}$ . The  $\overline{RD}$  input has to be tied to high-level in this configuration. This timing is called  $\overline{CSO}$ -controlled because  $\overline{CSO}$  is the last external signal of  $\overline{CSO}$ , CS1, and  $R/\overline{W}$  which becomes valid. The writing to the THS1207 can be performed irrespective of the conversion clock signal CONV\_CLK.

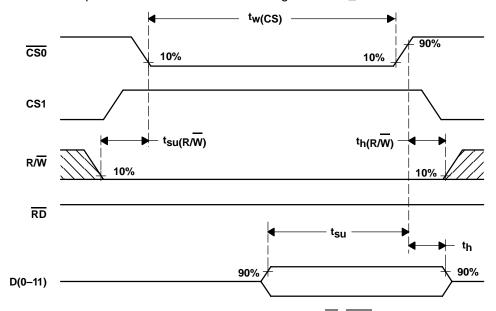


Figure 35. Write Timing Diagram Using R/W (CSO-controlled)

#### Write Timing Parameter (CSO-controlled)

	PARAMETER	MIN	TYP	MAX	UNIT
t <sub>su(R/W)</sub>	Setup time, R/W stable to last CS valid	0			ns
t <sub>su</sub>	Setup time, data valid to first CS invalid	5			ns
th	Hold time, first CS invalid to data invalid	2			ns
th(R/W)	Hold time, first CS invalid to R/W change	5			ns
tw(CS)	Pulse duration, CS active	10			ns



#### ANALOG INPUT CONFIGURATION AND REFERENCE VOLTAGE

The THS1207 features four analog input channels. These can be configured for either single-ended or differential operation. Figure 36 shows a simplified model, where a single-ended configuration for channel AINP is selected. The reference voltages for the ADC itself are  $V_{REFP}$  and  $V_{REFM}$  (either internal or external reference voltages). The analog input voltage range is between  $V_{REFM}$  to  $V_{REFP}$ . This means that  $V_{REFM}$  defines the minimum voltage, and  $V_{REFP}$  defines the maximum voltage, which can be applied to the ADC. The internal reference source provides the voltage  $V_{REFM}$  of 1.5 V and the voltage  $V_{REFP}$  of 3.5 V (see also section reference voltage). The resulting analog input voltage swing of 2 V can be expressed by:

$$V_{REFM} \le AINP \le V_{REFP}$$

AINP

 $V_{REFM}$ 

(1)

Figure 36. Single-Ended Input Stage

A differential operation is desired in many applications due to a better signal-to-noise ration. Figure 37 shows a simplified model for the analog inputs AINM and AINP, which are configured for differential operation. The differential operation mode provides in terms of performance benefits over single-ended mode and is therefore recommended for best performance. The THS1207 offers 2 differential analog inputs and in the single-ended mode 4 analog inputs. If the analog input architecture is differential, common mode noise and common mode voltages can be rejected. Additional details for both modes are given below.

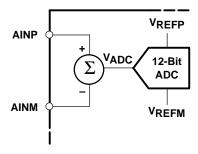


Figure 37. Differential Input Stage

In comparison to the single-ended configuration it can be seen that the voltage,  $V_{ADC}$ , which is applied at the input of the ADC is the difference between the input AINP and AINM. The voltage  $V_{ADC}$  can be calculated as follows:

$$V_{ADC} = ABS(AINP-AINM)$$
 (2)

The advantage to single-ended operation is that the common-mode voltage

$$V_{CM} = \frac{AINM + AINP}{2}$$
 (3)

can be rejected in the differential configuration, if the following condition for the analog input voltages is true:

$$AGND \le AINM, AINP \le AV_{DD}$$
 (4)

$$1 V \le V_{CM} \le 4 V \tag{5}$$



#### SINGLE-ENDED MODE OF OPERATION

The THS1207 can be configured for single-ended operation using dc or ac-coupling. In either case, the input of the THS1207 must be driven from an operational amplifier that does not degrade the ADC performance. Because the THS1207 operates from a single supply 5 V, it is necessary to level-shift ground-based bipolar signals to comply with its input requirements. This can be achieved with dc and ac-coupling.

#### **DC-COUPLING**

An operational amplifier can be configured to shift the signal level according to the analog input voltage range of the THS1207. The analog input voltage range of the THS1207 is between 1.5 V and 3.5 V. An operational amplifier can be used as shown in Figure 38.

Figure 38 shows an example where the analog input signal in the range between -1 V up to 1 V. This signal is shifted by an operational amplifier to the analog input range of the THS1207 (1.5 V to 3.5 V). The operational amplifier is configured as an inverting amplifier with a gain of -1. The required dc voltage of 1.25 V at the noninverting input is derived from the 2.5-V output reference REFOUT of the THS1207 by using a resistor divider. Therefore, the operational amplifier output voltage is centered at 2.5 V. The 10 µF tantalum capacitor is required for bypassing REFOUT. REFIN of the THS1207 must be connected directly to REFOUT in single-ended mode. The use of ratio matched, thin-film resistor networks minimizes gain and offset errors.

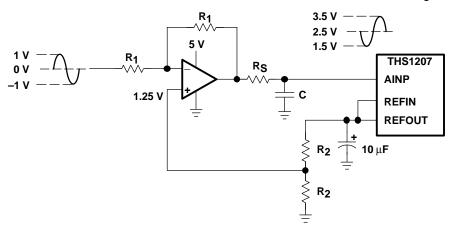


Figure 38. Level-Shift for DC-Coupled Input

#### **DIFFERENTIAL MODE OF OPERATION**

For the differential mode of operation, a conversion from single-ended to differential is required. A conversion to differential signals can be achieved by using an RF-transformer, which provides a center tap. Best performance is achieved in differential mode.

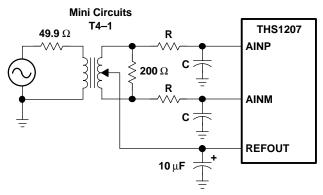


Figure 39. Transformer Coupled Input



#### **DEFINITIONS OF SPECIFICATIONS AND TERMINOLOGY**

#### **Integral Nonlinearity**

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

#### **Differential Nonlinearity**

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than  $\pm 1$  LSB ensures no missing codes.

#### **Zero Offset**

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

#### **Gain Error**

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

#### Signal-to-Noise Ratio + Distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

#### **Effective Number Of Bits (ENOB)**

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = \frac{(SINAD - 1.76)}{6.02}$$

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

#### **Total Harmonic Distortion (THD)**

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

#### Spurious Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
THS1207CDA	Active	Production	TSSOP (DA)   32	46   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	THS1207
THS1207CDA.A	Active	Production	TSSOP (DA)   32	46   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	THS1207
THS1207IDA	Active	Production	TSSOP (DA)   32	46   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS1207I
THS1207IDA.A	Active	Production	TSSOP (DA)   32	46   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS1207I

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE MATERIALS INFORMATION**

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#### **TUBE**



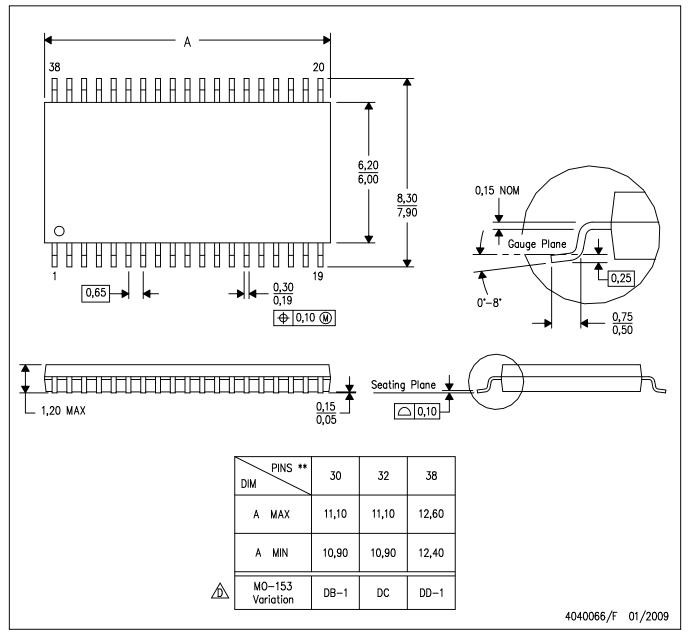
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS1207CDA	DA	TSSOP	32	46	530	11.89	3600	4.9
THS1207CDA.A	DA	TSSOP	32	46	530	11.89	3600	4.9
THS1207IDA	DA	TSSOP	32	46	530	11.89	3600	4.9
THS1207IDA.A	DA	TSSOP	32	46	530	11.89	3600	4.9

# DA (R-PDSO-G\*\*)

# PLASTIC SMALL-OUTLINE PACKAGE

38 PIN SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- ⚠ Falls within JEDEC MO−153, except 30 pin body length.



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