TDA4VEN, TDA4AEN Jacinto™ Processors

1 Features

Processor Cores:

- Up to Quad 64-bit Arm® Cortex®-A53 microprocessor subsystem at up to 1.4GHz
  - Quad-core Cortex-A53 cluster with 512KB L2 shared cache with SECDED ECC
  - Each A53 core has 32KB L1 DCache with SECDED ECC and 32KB L1 ICache with Parity protection
- Single-core Arm® Cortex®-R5F at up to 800MHz, integrated as part of MCU Channel with FFI
  - 32KB ICache, 32KB L1 DCache, and 64KB TCM with SECDED ECC on all memories
  - 512KB SRAM with SECDED ECC
- Single-core Arm® Cortex®-R5F at up to 800MHz, integrated to support Device Management
  - 32KB ICache, 32KB L1 DCache, and 64KB TCM with SECDED ECC on all memories
- Single-core Arm® Cortex®-R5F at up to 800MHz, integrated to support Run-time Management
  - 32KB ICache, 32KB L1 DCache, and 64KB TCM with SECDED ECC on all memories
- Two Deep Learning Accelerators (up to 4 TOPS total), each with:
  - C7x floating point, up to 40 GFLOPS, 256-bit Vector DSP at up to 1.0GHz
  - Matrix Multiply Accelerator (MMA), up to 2 TOPS (8b) at up to 1.0GHz
  - 32KB L1 DCache with SECDED ECC and 64KB L1 ICache with Parity protection
  - 2.25MB of L2 SRAM with SECDED ECC
- Depth and Motion Processing Accelerators (DMPAC)
  - Dense Optical Flow (DOF) Accelerator
  - Stereo Disparity Engine (SDE) Accelerator
- Vision Processing Accelerators (VPAC) with Image Signal Processor (ISP) and multiple vision assist accelerators:
  - 600 MP/s ISP
  - Support for 12-bit RGB-IR
  - Support for up to 16-bit input RAW format
  - Line support up to 4096
  - Wide Dynamic Range (WDR), Lens Distortion Correction (LDC), Vision Imaging Subsystem (VISS), and Multi-Scalar (MSC) support
    - Output color format : 8-bits, 12-bits, and YUV 4:2:2, YUV 4:2:0, RGB, HSV/HSL

Multimedia:

- Display subsystem
  - Triple display support over OLDI/LVDS (1x OLDI-DL, 1x or 2x OLDI-SL), DSI or DPI
    - OLDI-SL (Single Link): up to 1920 x 1080 at 60fps (165-MHz Pixel Clock)
    - OLDI-DL (Dual Link): up to 3840 x 1080 at 60fps (150-MHz Pixel Clock)
    - MIPI® DSI: with 4 Lane MIPI® D-PHY supports up to 3840 x 1080 at 60fps (300-MHz Pixel Clock)
    - DPI (24-bit RGB parallel interface): up to 1920 x 1080 at 60fps (165-MHz pixel clock)
  - Four display pipelines with hardware overlay support. A maximum of two display pipelines may be used per display.
  - Supports safety features such as freeze frame detection and data correctness check
- 3D Graphics Processing Unit (TDA4VEN)
  - IMG BXS-4-64 with 256KB cache
  - Up to 50 GFLOPS
  - Single shader core
  - OpenGL ES3.2 and Vulkan 1.2 API support
- Four Camera Serial Interface (CSI-2) Receiver with 4 Lane D-PHY
  - MIPI® CSI-2 v1.3 Compliant + MIPI® D-PHY 1.2
  - CSI-RX supports for 1,2,3, or 4 data lane mode up to 2.5Gbps per lane
  - CSI-TX supports for 1,2, or 4 data lane mode up to 2.5Gbps per lane
- One CSI2.0 Transmitter with 4 Lane D-PHY (shared with MIPI DSI)
- Video Encoder/Decoder
  - Support for HEVC (H.265) Main profiles at Level 5.1 High-tier
  - Support for H.264 BaseLine/Main/High Profiles at Level 5.2
  - Support for up to 4K UHD resolution (3840 × 2160)
    - Up to 400MPixels/s operation
- Motion JPEG encode at 416MPixels/s with resolutions up to 4K UHD (3840 × 2160)

Memory Subsystem:

- On-chip RAM dedicated to key processing cores
  - 256KB of On-Chip RAM (OCRAM) with SECDED ECC
  - 256KB of On-Chip RAM with SECDED ECC in SMS Subsystem

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

  - 512KB of On-chip RAM with SECDED ECC in Cortex-R5F MCU Subsystem
  - 64KB of On-chip RAM with SECDED ECC in R5F Device Manager Subsystem
  - 64KB of On-chip RAM with SECDED ECC in R5F Run-time Manager Subsystem
  - 2.25MB of L2 SRAM with SECDED ECC in each C7x Deep Learning Accelerator (up to 4.5MB total)
- DDR Subsystem (DDRSS)
  - Supports LPDDR4 memory types
  - 32-bit data bus with inline ECC
  - Supports speeds up to 4000 MT/s
  - Max LPDDR4 size of 8GB

Functional Safety:

- Functional Safety-Compliant targeted for Automotive (on select part numbers)
  - Developed for functional safety applications
  - Documentation will be available to aid ISO 26262 functional safety system design
  - Systematic capability up to ASIL D targeted
  - Hardware integrity up to ASIL B targeted
  - Safety-related certification
    - ISO 26262 planned
- AEC - Q100 qualified

Security:

- Secure boot supported
  - Hardware-enforced Root-of-Trust (RoT)
  - Support to switch RoT via backup key
  - Support for takeover protection, IP protection, and anti-roll back protection
- Trusted Execution Environment (TEE) supported
  - Arm TrustZone® based TEE
  - Extensive firewall support for isolation
  - Secure watchdog/timer/IPC
  - Secure storage support
  - Replay Protected Memory Block (RPMB) support
- Dedicated Security Controller with user programmable HSM core and dedicated security DMA & IPC subsystem for isolated processing
- Cryptographic acceleration supported
  - Session-aware cryptographic engine with ability to auto-switch key-material based on incoming data stream
- Supports cryptographic cores
  - AES – 128-/192-/256-Bit key sizes
  - SHA2 – 224-/256-/384-/512-Bit key sizes
  - DRBG with true random number generator
  - PKA (Public Key Accelerator) to Assist in RSA/ECC processing for secure boot
- Debugging security
  - Secure software controlled debug access
  - Security aware debugging

High-Speed Interfaces:

- PCI-Express® Gen3 single lane controller (PCIE)
  - Gen1 (2.5GT/s), Gen2 (5.0GT/s), and Gen3 (8.0GT/s) operation with auto-negotiation
- Integrated Ethernet switch supporting (total 2 external ports)
  - RMII(10/100) or RGMII (10/100/1000) **or** SGMII (1Gbps)
  - IEEE1588 (Annex D, Annex E, Annex F with 802.1AS PTP)
  - Clause 45 MDIO PHY management
  - Packet Classifier based on ALE engine with 512 classifiers
  - Priority based flow control
  - Time Sensitive Networking (TSN) support
  - Four CPU H/W interrupt Pacing
  - IP/UDP/TCP checksum offload in hardware
- USB3.1-Gen1 Port
  - One enhanced SuperSpeed Gen1 port
  - Port configurable as USB host, USB peripheral, or USB Dual-Role Device
  - Integrated USB VBUS detection
- USB2.0 Port
  - Port configurable as USB host, USB peripheral, or USB Dual-Role Device (DRD mode)
  - Integrated USB VBUS detection

General Connectivity and Automotive interfaces:

- 9x Universal Asynchronous Receiver-Transmitters (UART)
- 5x Serial Peripheral Interface (SPI) controllers
- 7x Inter-Integrated Circuit (I^2C) ports
- 5x Multichannel Audio Serial Ports (McASP)
- General-Purpose I/O (GPIO), All LVCMOS I/O can be configured as GPIO
- 4x Controller Area Network (CAN) modules with CAN-FD support

Media and Data Storage:

- 3x Secure Digital® (SD®) (4b+4b+8b) interfaces
  - 1x 8-bit eMMC interface up to HS400 speed
  - 2x 4-bit SD/SDIO interfaces up to UHS-I
  - Compliant with eMMC 5.1, SD 3.0, and SDIO Version 3.0

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- 1× General-Purpose Memory Controller (GPMC) up to 133MHz
- OSPI/QSPI with DDR / SDR support
  - Support for Serial NAND and Serial NOR Flash
  - 4GBytes memory address support
  - XIP mode with optional on-the-fly encryption

Technology / Package:

- 16-nm FinFET technology
- 18 mm x 18 mm, 0.65-mm pitch with VCA, 594-pin FCBGA (AMW)

Companion Power Management Solution:

- Functional Safety-Compliant support up to ASIL-B or SIL-2 targeted
- TPS6522x PMIC
- TPS6287x Stackable, Fast Transient Bucks

2 Applications

- Front camera systems
- Surround View and park assistance systems
- eMirror/Camera Mirror System (CMS)
- Radar and Lidar based automotive perception systems

3 Description

The TDA4VEN/TDA4AEN (aka, TDA4-Entry) processor family is an extension of the Jacinto™ 7 automotive-grade family of heterogeneous Arm® processors targeted at Advanced Driver Assistance System (ADAS) applications. With embedded Deep Learning (DL), Video, Vision Processing, and 3D Graphics acceleration, display interface and extensive automotive peripheral and networking options, TDA4VEN/TDA4AEN is built for a set of cost and power sensitive automotive applications such as NCAP front camera or entry-level park assistance systems. The cost optimized TDA4VEN/TDA4AEN provides an optimized performance compute for both traditional and deep learning algorithms at industry leading power/performance ratios with a high level of system integration to enable scalability and lower costs for advanced automotive platforms supporting multiple sensor modalities in stand-alone Electronic Control Units (ECUs).

TDA4VEN/TDA4AEN contains up to four Arm® Cortex®-A53 cores with 64-bit architecture, a Vision Processing Accelerator (VPAC) with Image Signal Processor (ISP) and multiple vision assist accelerators, Deep Learning (DL), Dense Optical Flow (DOF) video and 3D Graphics accelerators, a Cortex®-R5F MCU Island core and two Cortex®-R5F cores for Device and Run-time Management. The Cortex-A53s provide the powerful computing elements necessary for Linux applications as well as the implementation of traditional vision computing based algorithms. Building on the existing world-class ISP, TI's 7th generation ISP includes flexibility to process a broader sensor suite including RGB-InfraRed (RGB-IR), support for higher bit depth, and features targeting analytics applications. Key cores include TI's Dense Optical Flow (DOF) accelerator as well two "C7x" next generation DSP with scalar and vector cores, dedicated "MMA" deep learning accelerator combined with a large 2.25MB L2 memory enabling performance up to 4 TOPS within the lowest power envelope in the industry when operating at the typical automotive worst case junction temperature of 125°C.

TDA4VEN/TDA4AEN integrates high-speed IOs including a PCIe Gen-3 (1L) and 3-port Gigabit Ethernet switch with one internal port and two external ports with TSN support. In addition, an extensive peripherals set is included in TDA4VEN/TDA4AEN to enable system level connectivity such as USB, MMC/SD, four CSI2.0 Camera interface, OSPI, CAN-FD and GPMC for parallel host interface to an external ASIC/FPGA. TDA4VEN/TDA4AEN supports secure boot for IP protection with the built-in HSM (Hardware Security Module) and employs advanced power management support for power-sensitive applications. Integrated diagnostics and safety features support operations up to ASIL-B at SoC level, (ASIL-D systematic level).

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
XJ722S5	AMW (FCBGA, 594) with VCA	18mm x 18mm
TDA4VEN...Q1	AMW (FCBGA, 594) with VCA	18mm x 18mm
TDA4AEN...Q1	AMW (FCBGA, 594) with VCA	18mm x 18mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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3.1 Functional Block Diagram

Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the PROCESSOR-SDK-J722S Software Build Sheet.

Figure 3-1 is functional block diagram for the device.

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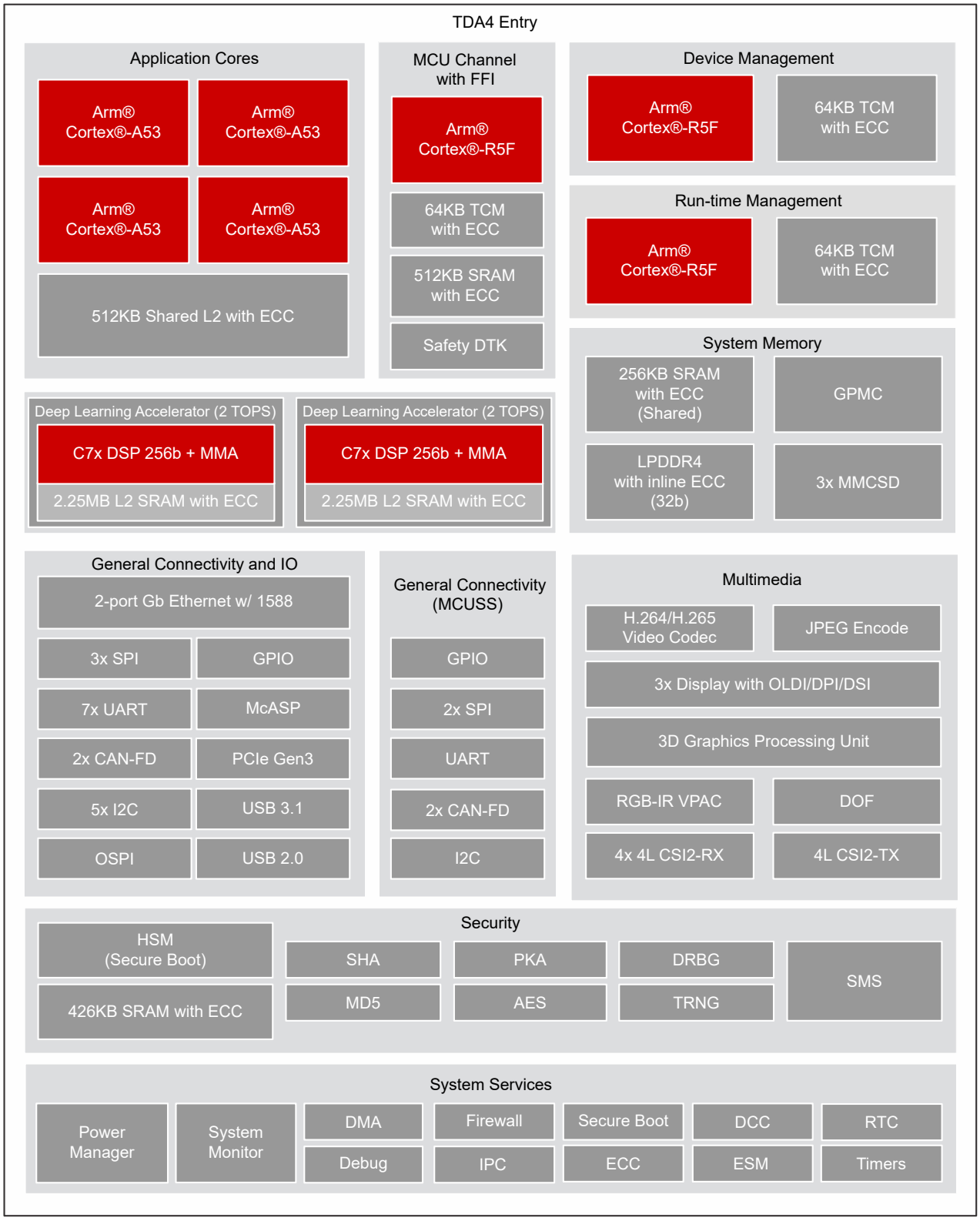

Figure 3-1. Functional Block Diagram

Table of Contents

1 Features....1
2 Applications....3
3 Description....3
3.1 Functional Block Diagram....4
4 Device Comparison....6
5 Terminal Configuration and Functions....8
5.1 Pin Diagrams....8
5.2 Pin Attributes....9
5.3 Signal Descriptions....47
5.4 Pin Connectivity Requirements....78
6 Specifications....81
6.1 Absolute Maximum Ratings....81
6.2 ESD Ratings for AEC - Q100 Qualified Devices in the AMW Package....83
6.3 Power-On Hours (POH)....83
6.4 Recommended Operating Conditions....84
6.5 Operating Performance Points....86
6.6 Electrical Characteristics....87
6.7 VPP Specifications for One-Time Programmable (OTP) eFuses....92
6.8 Thermal Resistance Characteristics....93
6.9 Timing and Switching Characteristics....94
7 Detailed Description....214
7.1 Overview....214
8 Applications, Implementation, and Layout....215
8.1 Device Connection and Layout Fundamentals....215
8.2 Peripheral- and Interface-Specific Design Information....216
8.3 Clock Routing Guidelines....223
9 Device and Documentation Support....224
9.1 Device Nomenclature....224
9.2 Tools and Software....227
9.3 Documentation Support....227
9.4 Support Resources....227
9.5 Trademarks....227
9.6 Electrostatic Discharge Caution....228
9.7 Glossary....228
10 Revision History....228
11 Mechanical, Packaging, and Orderable Information....230
11.1 Packaging Information....230

4 Device Comparison

Table 4-1 shows a comparison between devices, highlighting the differences.

Note

Availability of features listed in this table are a function of shared IO pins, where IO signals associated with many of the features are multiplexed to a limited number of pins. The SysConfig tool should be used to assign signal functions to pins. This will provide a better understanding of limitations associated with pin multiplexing.

Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the PROCESSOR-SDK-J722S Software Build Sheet.

Table 4-1. Device Comparison

FEATURES(1)	REFERENCE NAME	TDA4VEN8	TDA4AEN8
PROCESSORS AND ACCELERATORS			
Speed Grades (See Device Speed Grades)		J, K	
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Quad Core	
Arm Cortex-R5F in MCU domain	MCU_R5F	Single Core	
Arm Cortex-R5F in MAIN domain	R5FSS0	Single Core	
Device Management Subsystem	WKUP_R5F	Single Core	
Hardware Security Module	HSM	Yes	
Crypto Accelerators	Security	Yes	
C7x Floating Point, Vector DSP	C7x256V DSP	Dual Core	
Deep Learning Accelerator	MMA	Dual Core	
Graphics Processing Unit	GPU	Yes	No
Video Encoder / Decoder	VENC/VDEC	Yes	
Motion JPEG Encoder	JPEG	Yes	
Depth and Motion Processing Accelerators	DMPAC	Yes	

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Table 4-1. Device Comparison (continued)

FEATURES[1]	REFERENCE NAME	TDA4VEN8	TDA4AEN8
Vision Processing Accelerators	VPAC3L	Yes	
SAFETY AND SECURITY			
Safety Targeted	Safety	Optional[2]	
Device Security	Security	Optional[3]	
AEC-Q100 Qualified	Q1	Optional[4]	
PROGRAM AND DATA STORAGE			
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	256KB	
On-Chip Shared Memory (RAM) in MCU Domain	MCU_MSRAM	512KB	
LPDDR4 DDR Subsystem	DDRSS	32-bit data with inline ECC up to 8GB	
General-Purpose Memory Controller	GPMC	Up to 128MB with ECC	
PERIPHERALS			
Display Subsystem	DSS7UL	1x DPI	
		1x LVDS	
		1x DSI	
Modular Controller Area Network Interface	MCAN	4	
Full CAN-FD Support	CAN-FD	Yes	
General-Purpose I/O	GPIO	Up to 147	
Inter-Integrated Circuit Interface	I2C	7	
Multichannel Audio Serial Port	MCASP	5	
Multichannel Serial Peripheral Interface	MCSPI	5	
Multi-Media Card/Secure Digital Interface	MMC/SD	1x eMMC (8-bits)	
		2x SD/SDIO (4-bits)	
Flash Subsystem (FSS)[5]	OSPI0/QSPI0	Yes[5]	
Gigabit Ethernet Interface	CPSW3G[6]	2 Ports (RGMII/RMII/SGMII[6])	
General-Purpose Timers	TIMER	14 (4 in MCU and 2 in WKUP)	
Enhanced Pulse-Width Modulator Module	EPWM	3	
Enhanced Capture Module	ECAP	3	
Enhanced Quadrature Encoder Pulse Module	EQEP	3	
Universal Asynchronous Receiver and Transmitter	UART	9	
PCI Express Gen3 Port with Integrated PHY	PCIe[6]	Single Lane	
CSI2-RX Controller with DPHY	CSI-RX	4x4L	
CSI2-TX Controller	CSI-TX	1x4L	
USB2.0 Controller with PHY	USB 2.0	1	
USB3.0 Controller with PHY	USB 3.1 Gen 1[6]	1	

(1) J722S is the base part number for the superset device. Software should constrain the features used to match the intended production device.
(2) Safety features including SIL/ASIL ratings are only applicable to select part number variants as indicated by the Device Type (Y) identifier in the Device Naming Convention table.
(3) Device security features including Secure Boot and Customer Programmable Keys are applicable to select part number variants as indicated by the Device Type (Y) identifier in the Table 10-1, Nomenclature Description table
(4) AEC-Q100 qualification is applicable to select part number variants as indicated by the Automotive Designator (Q1) identifier in the Device Naming Convention table.
(5) One flash interface, configured as OSPI0 or QSPI0.
(6) PCIe, USB3.0 and SGMII share a total of 2 SERDES ports.

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5 Terminal Configuration and Functions

5.1 Pin Diagrams

Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

Figure 5-1 shows the ball locations for the 594-ball flip chip ball grid array (FCBGA) package to quickly locate signal names and ball grid numbering. This figure is used in conjuction with Section 5.2.1 through Section 5.4 (*Pin Attributes* table and all *Signal Descriptions* tables, including the *Pin Connectivity Requirements* table).

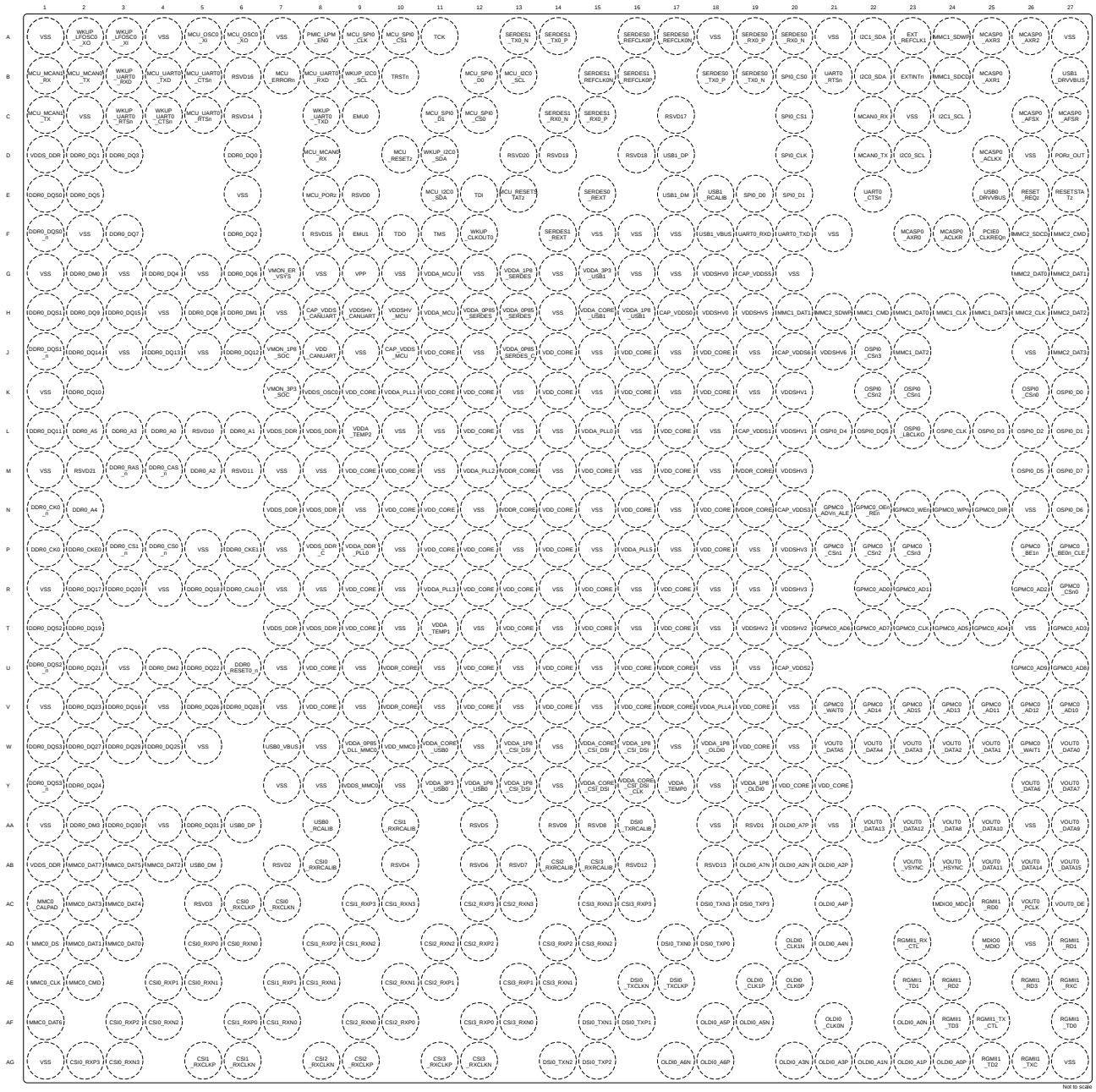

Figure 5-1. AMW FCBGA-N594 Pin Diagram (Top View)

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5.2 Pin Attributes

The following list describes the contents of each column in the Table 5-1, *Pin Attributes (AMW Package)* table:

1. **BALL NUMBER:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **BALL NAME:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **SIGNAL NAME:** Signal name(s) of all dedicated and pin multiplexed signal functions associated with a ball.

Note

Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

The Table 5-1, *Pin Attributes (AMW Package)* table only defines signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see *Pad Configuration Registers* section in *Device Configuration* chapter of the device TRM. Refer to the respective peripheral chapter in the device TRM for information associated with peripheral signal multiplexing.

4. **MUX MODE:** The MUXMODE value associated with each pin multiplexed signal function:
   a. MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.

Note

The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when MCU_PORz is deasserted.

   a. MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only valid values of MUXMODE should be used.
   b. Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz_OUT. These input signal functions are fixed to their respective pins and are not programable via MUXMODE.
   c. An empty box means Not Applicable.

Note

The following configurations of MUXMODE must be avoided for proper device operation.

- Configuring multiple pins operating as inputs to the same pin multiplexed signal function is not supported as it can yield unexpected results.
- Configuring a pin to an undefined pin multiplexing mode will cause the pin behavior to be undefined.

5. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog

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- PWR = Power
- GND = Ground
- CAP = LDO Capacitor.

6. **DSIS:** The deselected input state (DSIS) indicates the state driven to the subsystem input (logic "0", logic "1", or "pad" level) when the pin multiplexed signal function is not selected by MUXMODE.
   - 0: Logic 0 driven to the subsystem input.
   - 1: Logic 1 driven to the subsystem input.
   - pad: Logic state of the pad is driven to the subsystem input.
   - An empty box means Not Applicable.
7. **BALL STATE DURING RESET (RX/TX/PULL):** State of the terminal while MCU_PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is disabled.
     - On: The input buffer is enabled.
   - TX (Output buffer)
     - Off: The output buffer is disabled.
     - Low: The output buffer is enabled and drives V_{OL}.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned off.
     - Up: Internal pull-up resistor is turned on.
     - Down: Internal pull-down resistor is turned on.
     - NA: Not Applicable.
   - An empty box means Not Applicable.
8. **BALL STATE AFTER RESET (RX/TX/PULL):** State of the terminal after MCU_PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is disabled.
     - On: The input buffer is enabled.
   - TX (Output buffer)
     - Off: The output buffer is disabled.
     - SS: The subsystem selected with MUXMODE determines the output buffer state.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned off.
     - Up: Internal pull-up resistor is turned on.
     - Down: Internal pull-down resistor is turned on.
     - NA: Not Applicable.
   - An empty box means Not Applicable.
9. **MUX MODE AFTER RESET:** The value found in this column defines the default pin multiplexed signal function after MCU_PORz is deasserted.

   An empty box means Not Applicable.
10. **I/O VOLTAGE VALUE**: This column describes I/O operating voltage options of the respective power supply, when applicable.

    An empty box means Not Applicable.

    For more information, see valid operating voltage range(s) defined for each power supply in Section 6.4, *Recommended Operating Conditions*.
11. **POWER:** The power supply of the associated I/O, when applicable.

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An empty box means Not Applicable.

12. **HYS:** Indicates if the input buffer associated with this I/O has hysteresis:
    - Yes: With hysteresis
    - No: Without hysteresis
    - An empty box means Not Applicable.

    For more information, see the hysteresis values in Section 6.6, *Electrical Characteristics*.
13. **BUFFER TYPE:** This column defines the buffer type associated with a terminal. This information can be used to determine which Electrical Characteristics table is applicable.

    An empty box means Not Applicable.

    For electrical characteristics, refer to the appropriate buffer type table in Section 6.6, *Electrical Characteristics*.
14. **PULL UP/DOWN TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    - PU: Internal pull-up
    - PD: Internal pull-down
    - PU/PD: Internal pull-up and pull-down
    - An empty box means No internal pull.
15. **PADCONFIG Register:** Name of the IO pad configuration register associated with Ball.
16. **PADCONFIG Address:** Physical address of the IO pad configuration register associated with Ball.

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Table 5-1. Pin Attributes (AMW Package)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
H17	CAP_VDDS0	CAP_VDDS0		CAP									
L19	CAP_VDDS1	CAP_VDDS1		CAP									
U20	CAP_VDDS2	CAP_VDDS2		CAP									
N20	CAP_VDDS3	CAP_VDDS3		CAP									
G19	CAP_VDDS5	CAP_VDDS5		CAP									
J20	CAP_VDDS6	CAP_VDDS6		CAP									
H8	CAP_VDDS_CANUART	CAP_VDDS_CANUART		CAP									
J10	CAP_VDDS_MCU	CAP_VDDS_MCU		CAP									
AC7	CSI0_RXCLKN	CSI0_RXCLKN		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC6	CSI0_RXCLKP	CSI0_RXCLKP		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AB8	CSI0_RXRCALIB	CSI0_RXRCALIB		A					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AG6	CSI1_RXCLKN	CSI1_RXCLKN		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AG5	CSI1_RXCLKP	CSI1_RXCLKP		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AA10	CSI1_RXRCALIB	CSI1_RXRCALIB		A					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AG8	CSI2_RXCLKN	CSI2_RXCLKN		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AG9	CSI2_RXCLKP	CSI2_RXCLKP		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AB14	CSI2_RXRCALIB	CSI2_RXRCALIB		A					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AG12	CSI3_RXCLKN	CSI3_RXCLKN		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AG11	CSI3_RXCLKP	CSI3_RXCLKP		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AB15	CSI3_RXRCALIB	CSI3_RXRCALIB		A					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD6	CSI0_RXN0	CSI0_RXN0		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AE5	CSI0_RXN1	CSI0_RXN1		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AF4	CSI0_RXN2	CSI0_RXN2		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AG3	CSI0_RXN3	CSI0_RXN3		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD5	CSI0_RXP0	CSI0_RXP0		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AE4	CSI0_RXP1	CSI0_RXP1		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AF3	CSI0_RXP2	CSI0_RXP2		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AG2	CSI0_RXP3	CSI0_RXP3		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AF7	CSI1_RXN0	CSI1_RXN0		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AE8	CSI1_RXN1	CSI1_RXN1		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD9	CSI1_RXN2	CSI1_RXN2		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC10	CSI1_RXN3	CSI1_RXN3		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AF6	CSI1_RXP0	CSI1_RXP0		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AE7	CSI1_RXP1	CSI1_RXP1		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD8	CSI1_RXP2	CSI1_RXP2		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC9	CSI1_RXP3	CSI1_RXP3		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AF9	CSI2_RXN0	CSI2_RXN0		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AE10	CSI2_RXN1	CSI2_RXN1		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD11	CSI2_RXN2	CSI2_RXN2		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC13	CSI2_RXN3	CSI2_RXN3		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AF10	CSI2_RXP0	CSI2_RXP0		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AE11	CSI2_RXP1	CSI2_RXP1		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD12	CSI2_RXP2	CSI2_RXP2		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC12	CSI2_RXP3	CSI2_RXP3		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AF13	CSI3_RXN0	CSI3_RXN0		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AE14	CSI3_RXN1	CSI3_RXN1		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD15	CSI3_RXN2	CSI3_RXN2		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC15	CSI3_RXN3	CSI3_RXN3		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AF12	CSI3_RXP0	CSI3_RXP0		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AE13	CSI3_RXP1	CSI3_RXP1		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD14	CSI3_RXP2	CSI3_RXP2		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC16	CSI3_RXP3	CSI3_RXP3		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
M4	DDR0_CAS_n	DDR0_CAS_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M3	DDR0_RAS_n	DDR0_RAS_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L4	DDR0_A0	DDR0_A0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L6	DDR0_A1	DDR0_A1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M5	DDR0_A2	DDR0_A2		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L3	DDR0_A3	DDR0_A3		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N2	DDR0_A4	DDR0_A4		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L2	DDR0_A5	DDR0_A5		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
R6	DDR0_CAL0	DDR0_CAL0		A					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P1	DDR0_CK0	DDR0_CK0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N1	DDR0_CK0_n	DDR0_CK0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P2	DDR0_CKE0	DDR0_CKE0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P6	DDR0_CKE1	DDR0_CKE1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
P4	DDR0_CS0_n	DDR0_CS0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P3	DDR0_CS1_n	DDR0_CS1_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G2	DDR0_DM0	DDR0_DM0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H6	DDR0_DM1	DDR0_DM1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U4	DDR0_DM2	DDR0_DM2		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AA2	DDR0_DM3	DDR0_DM3		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D6	DDR0_DQ0	DDR0_DQ0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D2	DDR0_DQ1	DDR0_DQ1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F6	DDR0_DQ2	DDR0_DQ2		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D3	DDR0_DQ3	DDR0_DQ3		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G4	DDR0_DQ4	DDR0_DQ4		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E2	DDR0_DQ5	DDR0_DQ5		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G6	DDR0_DQ6	DDR0_DQ6		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F3	DDR0_DQ7	DDR0_DQ7		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H5	DDR0_DQ8	DDR0_DQ8		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H2	DDR0_DQ9	DDR0_DQ9		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K2	DDR0_DQ10	DDR0_DQ10		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L1	DDR0_DQ11	DDR0_DQ11		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J6	DDR0_DQ12	DDR0_DQ12		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J4	DDR0_DQ13	DDR0_DQ13		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J2	DDR0_DQ14	DDR0_DQ14		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H3	DDR0_DQ15	DDR0_DQ15		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
V3	DDR0_DQ16	DDR0_DQ16		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
R2	DDR0_DQ17	DDR0_DQ17		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
R5	DDR0_DQ18	DDR0_DQ18		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
T2	DDR0_DQ19	DDR0_DQ19		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
R3	DDR0_DQ20	DDR0_DQ20		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U2	DDR0_DQ21	DDR0_DQ21		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U5	DDR0_DQ22	DDR0_DQ22		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
V2	DDR0_DQ23	DDR0_DQ23		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
Y2	DDR0_DQ24	DDR0_DQ24		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
W4	DDR0_DQ25	DDR0_DQ25		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
V5	DDR0_DQ26	DDR0_DQ26		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
W2	DDR0_DQ27	DDR0_DQ27		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
V6	DDR0_DQ28	DDR0_DQ28		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
W3	DDR0_DQ29	DDR0_DQ29		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AA3	DDR0_DQ30	DDR0_DQ30		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AA5	DDR0_DQ31	DDR0_DQ31		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E1	DDR0_DQS0	DDR0_DQS0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F1	DDR0_DQS0_n	DDR0_DQS0_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H1	DDR0_DQS1	DDR0_DQS1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J1	DDR0_DQS1_n	DDR0_DQS1_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
T1	DDR0_DQS2	DDR0_DQS2		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U1	DDR0_DQS2_n	DDR0_DQS2_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
W1	DDR0_DQS3	DDR0_DQS3		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
Y1	DDR0_DQS3_n	DDR0_DQS3_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U6	DDR0_RESET0_n	DDR0_RESET0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AE16	DSI0_TXCLKN	DSI0_TXCLKN		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AE17	DSI0_TXCLKP	DSI0_TXCLKP		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AA16	DSI0_TXRCALIB	DSI0_TXRCALIB		A					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD17	DSI0_TXN0	DSI0_TXN0		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AF15	DSI0_TXN1	DSI0_TXN1		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AG14	DSI0_TXN2	DSI0_TXN2		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC18	DSI0_TXN3	DSI0_TXN3		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD18	DSI0_TXP0	DSI0_TXP0		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AF16	DSI0_TXP1	DSI0_TXP1		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AG15	DSI0_TXP2	DSI0_TXP2		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC19	DSI0_TXP3	DSI0_TXP3		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
C9	EMU0 PADCONFIG MCU_PADCONFIG30 0x04084078	EMU0	0	IO	0	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
F9	EMU1 PADCONFIG MCU_PADCONFIG31 0x0408407C	EMU1	0	IO	0	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
B23	EXTINTn PADCONFIG PADCONFIG125 0x000F41F4	EXTINTn	0	I	1	Off / Off / NA	Off / Off / NA	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OPEN DRAIN	
		GPIO1_31	7	IOD	pad								
A23	EXT_REFCLK1 PADCONFIG PADCONFIG124 0x000F41F0	EXT_REFCLK1	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SYNC1_OUT	1	O									
		SPI2_CS3	2	IO	1								
		SYSCLKOUT0	3	O									
		TIMER_IO4	4	IO	0								
		CLKOUT0	5	O									
		CP_GEMAC_CPTS0_RFT_CLK	6	I	0								
		GPIO1_30	7	IO	pad								
		ECAP0_IN_APWM_OUT	8	IO	0								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
N21	GPMC0_ADVn_ALE PADCONFIG PADCONFIG33 0x000F4084	GPMC0_ADVn_ALE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_AXR2	2	IO	0								
		TRC_DATA7	6	O									
		GPIO0_32	7	IO	pad								
T23	GPMC0_CLK PADCONFIG PADCONFIG31 0x000F407C	GPMC0_CLK	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_AXR3	2	IO	0								
		GPMC0_FCLK_MUX	3	O									
		TRC_DATA6	6	O									
		GPIO0_31	7	IO	pad								
N25	GPMC0_DIR PADCONFIG PADCONFIG41 0x000F40A4	GPMC0_DIR	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR13	3	IO	0								
		MAIN_ERRORn	5	IO	1								
		TRC_DATA14	6	O									
		GPIO0_40	7	IO	pad								
		EQEP2_S	8	IO	0								
N22	GPMC0_OEn_REn PADCONFIG PADCONFIG34 0x000F4088	GPMC0_OEn_REn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_AXR1	2	IO	0								
		TRC_DATA8	6	O									
		GPIO0_33	7	IO	pad								
N23	GPMC0_WEn PADCONFIG PADCONFIG35 0x000F408C	GPMC0_WEn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_AXR0	2	IO	0								
		TRC_DATA9	6	O									
		GPIO0_34	7	IO	pad								
N24	GPMC0_WPn PADCONFIG PADCONFIG40 0x000F40A0	GPMC0_WPn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		AUDIO_EXT_REFCLK1	1	IO	0								
		GPMC0_A22	2	OZ									
		UART6_TXD	3	O									
		TRC_DATA13	6	O									
		GPIO0_39	7	IO	pad								
R22	GPMC0_AD0 PADCONFIG PADCONFIG15 0x000F403C	GPMC0_AD0	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR4	3	IO	0								
		TRC_CLK	6	O									
		GPIO0_15	7	IO	pad								
		BOOTMODE00	Bootstrap	I									

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
R23	GPMC0_AD1 PADCONFIG PADCONFIG16 0x000F4040	GPMC0_AD1	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR5	3	IO	0								
		TRC_CTL	6	O									
		GPIO0_16	7	IO	pad								
		BOOTMODE01	Bootstrap	I									
R26	GPMC0_AD2 PADCONFIG PADCONFIG17 0x000F4044	GPMC0_AD2	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR6	3	IO	0								
		TRC_DATA0	6	O									
		GPIO0_17	7	IO	pad								
		BOOTMODE02	Bootstrap	I									
T27	GPMC0_AD3 PADCONFIG PADCONFIG18 0x000F4048	GPMC0_AD3	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR7	3	IO	0								
		TRC_DATA1	6	O									
		GPIO0_18	7	IO	pad								
		BOOTMODE03	Bootstrap	I									
T25	GPMC0_AD4 PADCONFIG PADCONFIG19 0x000F404C	GPMC0_AD4	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR8	3	IO	0								
		TRC_DATA2	6	O									
		GPIO0_19	7	IO	pad								
		BOOTMODE04	Bootstrap	I									
T24	GPMC0_AD5 PADCONFIG PADCONFIG20 0x000F4050	GPMC0_AD5	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR9	3	IO	0								
		TRC_DATA3	6	O									
		GPIO0_20	7	IO	pad								
		BOOTMODE05	Bootstrap	I									
T21	GPMC0_AD6 PADCONFIG PADCONFIG21 0x000F4054	GPMC0_AD6	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR10	3	IO	0								
		TRC_DATA4	6	O									
		GPIO0_21	7	IO	pad								
		BOOTMODE06	Bootstrap	I									
T22	GPMC0_AD7 PADCONFIG PADCONFIG22 0x000F4058	GPMC0_AD7	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR11	3	IO	0								
		TRC_DATA5	6	O									
		GPIO0_22	7	IO	pad								
		BOOTMODE07	Bootstrap	I									

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
U27	GPMC0_AD8 PADCONFIG PADCONFIG23 0x000F405C	GPMC0_AD8	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA16	1	O									
		UART2_RXD	2	I	1								
		MCASP2_AXR0	3	IO	0								
		GPIO0_23	7	IO	pad								
		BOOTMODE08	Bootstrap	I									
U26	GPMC0_AD9 PADCONFIG PADCONFIG24 0x000F4060	GPMC0_AD9	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA17	1	O									
		UART2_TXD	2	O									
		MCASP2_AXR1	3	IO	0								
		GPIO0_24	7	IO	pad								
		BOOTMODE09	Bootstrap	I									
V27	GPMC0_AD10 PADCONFIG PADCONFIG25 0x000F4064	GPMC0_AD10	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA18	1	O									
		UART3_RXD	2	I	1								
		MCASP2_AXR2	3	IO	0								
		GPIO0_25	7	IO	pad								
		OBSCLK0	8	O									
		BOOTMODE10	Bootstrap	I									
V25	GPMC0_AD11 PADCONFIG PADCONFIG26 0x000F4068	GPMC0_AD11	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA19	1	O									
		UART3_TXD	2	O									
		MCASP2_AXR3	3	IO	0								
		TRC_DATA23	6	O									
		GPIO0_26	7	IO	pad								
		BOOTMODE11	Bootstrap	I									
V26	GPMC0_AD12 PADCONFIG PADCONFIG27 0x000F406C	GPMC0_AD12	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA20	1	O									
		UART4_RXD	2	I	1								
		MCASP2_AFSX	3	IO	0								
		TRC_DATA22	6	O									
		GPIO0_27	7	IO	pad								
		BOOTMODE12	Bootstrap	I									

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
V24	GPMC0_AD13 PADCONFIG PADCONFIG28 0x000F4070	GPMC0_AD13	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA21	1	O									
		UART4_TXD	2	O									
		MCASP2_ACLKX	3	IO	0								
		TRC_DATA21	6	O									
		GPIO0_28	7	IO	pad								
		BOOTMODE13	Bootstrap	I									
V22	GPMC0_AD14 PADCONFIG PADCONFIG29 0x000F4074	GPMC0_AD14	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA22	1	O									
		UART5_RXD	2	I	1								
		MCASP2_AFSR	3	IO	0								
		MCASP2_AXR4	4	IO	0								
		TRC_DATA20	6	O									
		GPIO0_29	7	IO	pad								
		UART2_CTSn	8	I	1								
		BOOTMODE14	Bootstrap	I									
V23	GPMC0_AD15 PADCONFIG PADCONFIG30 0x000F4078	GPMC0_AD15	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA23	1	O									
		UART5_TXD	2	O									
		MCASP2_ACLKR	3	IO	0								
		MCASP2_AXR5	4	IO	0								
		TRC_DATA19	6	O									
		GPIO0_30	7	IO	pad								
		UART2_RTSn	8	O									
		BOOTMODE15	Bootstrap	I									
P27	GPMC0_BE0n_CLE PADCONFIG PADCONFIG36 0x000F4090	GPMC0_BE0n_CLE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_ACLKX	2	IO	0								
		TRC_DATA10	6	O									
		GPIO0_35	7	IO	pad								
P26	GPMC0_BE1n PADCONFIG PADCONFIG37 0x000F4094	GPMC0_BE1n	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR12	3	IO	0								
		TRC_DATA11	6	O									
		GPIO0_36	7	IO	pad								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
R27	GPMC0_CSn0 PADCONFIG PADCONFIG42 0x000F40A8	GPMC0_CSn0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C4_SCL	1	IOD	1								
		MCASP2_AXR14	3	IO	0								
		TRC_DATA15	6	O									
		GPIO0_41	7	IO	pad								
P21	GPMC0_CSn1 PADCONFIG PADCONFIG43 0x000F40AC	GPMC0_CSn1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C4_SDA	1	IOD	1								
		MCASP2_AXR15	3	IO	0								
		TRC_DATA16	6	O									
		GPIO0_42	7	IO	pad								
P22	GPMC0_CSn2 PADCONFIG PADCONFIG44 0x000F40B0	GPMC0_CSn2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C2_SCL	1	IOD	1								
		MCASP1_AXR4	2	IO	0								
		UART4_RXD	3	I	1								
		MCAN1_TX	5	O									
		TRC_DATA17	6	O									
		GPIO0_43	7	IO	pad								
		MCASP1_AFSR	8	IO	0								
P23	GPMC0_CSn3 PADCONFIG PADCONFIG45 0x000F40B4	GPMC0_CSn3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C2_SDA	1	IOD	1								
		GPMC0_A20	2	OZ									
		UART4_TXD	3	O									
		MCASP1_AXR5	4	IO	0								
		MCAN1_RX	5	I	1								
		TRC_DATA18	6	O									
		GPIO0_44	7	IO	pad								
		MCASP1_ACLKR	8	IO	0								
V21	GPMC0_WAIT0 PADCONFIG PADCONFIG38 0x000F4098	GPMC0_WAIT0	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_AFSX	2	IO	0								
		TRC_DATA12	6	O									
		GPIO0_37	7	IO	pad								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
W26	GPMC0_WAIT1 PADCONFIG PADCONFIG39 0x000F409C	GPMC0_WAIT1	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_EXTPCLKIN	1	I	0								
		GPMC0_A21	2	OZ									
		UART6_RXD	3	I	1								
		AUDIO_EXT_REFCLK2	4	IO	0								
		GPIO0_38	7	IO	pad								
		EQEP2_I	8	IO	0								
D23	I2C0_SCL PADCONFIG PADCONFIG120 0x000F41E0	I2C0_SCL	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SYNC0_OUT	2	O									
		OBSCLK1	3	O									
		UART1_DCDn	4	I	1								
		EQEP2_A	5	I	0								
		EHRPWM_SOCA	6	O									
		GPIO1_26	7	IO	pad								
		ECAP1_IN_APWM_OUT	8	IO	0								
		SPI2_CS0	9	IO	1								
B22	I2C0_SDA PADCONFIG PADCONFIG121 0x000F41E4	I2C0_SDA	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS2	2	IO	1								
		TIMER_IO5	3	IO	0								
		UART1_DSRn	4	I	1								
		EQEP2_B	5	I	0								
		EHRPWM_SOCB	6	O									
		GPIO1_27	7	IO	pad								
		ECAP2_IN_APWM_OUT	8	IO	0								
C24	I2C1_SCL PADCONFIG PADCONFIG122 0x000F41E8	I2C1_SCL	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_RXD	1	I	1								
		TIMER_IO0	2	IO	0								
		SPI2_CS1	3	IO	1								
		EHRPWM0_SYNCI	4	I	0								
		GPIO1_28	7	IO	pad								
		EHRPWM2_A	8	IO	0								
		MMC2_SDCD	9	I	0								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A22	I2C1_SDA PADCONFIG PADCONFIG123 0x000F41EC	I2C1_SDA	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_TXD	1	O									
		TIMER_IO1	2	IO	0								
		SPI2_CLK	3	IO	0								
		EHRPWM0_SYNCO	4	O									
		GPIO1_29	7	IO	pad								
		EHRPWM2_B	8	IO	0								
		MMC2_SDWP	9	I	0								
C22	MCAN0_RX PADCONFIG PADCONFIG119 0x000F41DC	MCAN0_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART5_TXD	1	O									
		TIMER_IO3	2	IO	0								
		SYNC3_OUT	3	O									
		UART1_RIn	4	I	1								
		EQEP2_S	5	IO	0								
		I2C4_SDA	6	IOD	1								
		GPIO1_25	7	IO	pad								
		MCASP2_AXR1	8	IO	0								
		EHRPWM_TZn_IN4	9	I	0								
D22	MCAN0_TX PADCONFIG PADCONFIG118 0x000F41D8	MCAN0_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART5_RXD	1	I	1								
		TIMER_IO2	2	IO	0								
		SYNC2_OUT	3	O									
		UART1_DTRn	4	O									
		EQEP2_I	5	IO	0								
		I2C4_SCL	6	IOD	1								
		GPIO1_24	7	IO	pad								
		MCASP2_AXR0	8	IO	0								
		EHRPWM_TZn_IN3	9	I	0								
F24	MCASP0_ACLKR PADCONFIG PADCONFIG108 0x000F41B0	MCASP0_ACLKR	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CLK	1	IO	0								
		UART1_TXD	2	O									
		EHRPWM0_B	6	IO	0								
		GPIO1_14	7	IO	pad								
		EQEP1_I	8	IO	0								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
D25	MCASP0_ACLKX PADCONFIG PADCONFIG105 0x000F41A4	MCASP0_ACLKX	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS1	1	IO	1								
		ECAP2_IN_APWM_OUT	2	IO	0								
		GPIO1_11	7	IO	pad								
		EQEP1_A	8	I	0								
C27	MCASP0_AFSR PADCONFIG PADCONFIG107 0x000F41AC	MCASP0_AFSR	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS0	1	IO	1								
		UART1_RXD	2	I	1								
		EHRPWM0_A	6	IO	0								
		GPIO1_13	7	IO	pad								
		EQEP1_S	8	IO	0								
C26	MCASP0_AFSX PADCONFIG PADCONFIG106 0x000F41A8	MCASP0_AFSX	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS3	1	IO	1								
		AUDIO_EXT_REFCLK1	2	IO	0								
		GPIO1_12	7	IO	pad								
		EQEP1_B	8	I	0								
F23	MCASP0_AXR0 PADCONFIG PADCONFIG104 0x000F41A0	MCASP0_AXR0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		AUDIO_EXT_REFCLK0	2	IO	0								
		EHRPWM1_B	6	IO	0								
		GPIO1_10	7	IO	pad								
		EQEP0_I	8	IO	0								
B25	MCASP0_AXR1 PADCONFIG PADCONFIG103 0x000F419C	MCASP0_AXR1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS2	1	IO	1								
		ECAP1_IN_APWM_OUT	2	IO	0								
		MAIN_ERRORn	5	IO	1								
		EHRPWM1_A	6	IO	0								
		GPIO1_9	7	IO	pad								
		EQEP0_S	8	IO	0								
A26	MCASP0_AXR2 PADCONFIG PADCONFIG102 0x000F4198	MCASP0_AXR2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_D1	1	IO	0								
		UART1_RTSn	2	O									
		UART6_TXD	3	O									
		ECAP2_IN_APWM_OUT	5	IO	0								
		GPIO1_8	7	IO	pad								
		EQEP0_B	8	I	0								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A25	MCASP0_AXR3 PADCONFIG PADCONFIG101 0x000F4194	MCASP0_AXR3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_D0	1	IO	0								
		UART1_CTSn	2	I	1								
		UART6_RXD	3	I	1								
		ECAP1_IN_APWM_OUT	5	IO	0								
		GPIO1_7	7	IO	pad								
		EQEP0_A	8	I	0								
B7	MCU_ERRORn PADCONFIG MCU_PADCONFIG24 0x04084060	MCU_ERRORn	0	IO		Off / Off / Down	On / SS / Down	0	1.8 V	VDDS_OSC0	Yes	LVCMOS	PU/PD
B13	MCU_I2C0_SCL PADCONFIG MCU_PADCONFIG17 0x04084044	MCU_I2C0_SCL	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OPEN DRAIN	
		MCU_GPIO0_17	7	IOD	pad								
E11	MCU_I2C0_SDA PADCONFIG MCU_PADCONFIG18 0x04084048	MCU_I2C0_SDA	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OPEN DRAIN	
		MCU_GPIO0_18	7	IOD	pad								
D8	MCU_MCAN0_RX PADCONFIG MCU_PADCONFIG14 0x04084038	MCU_MCAN0_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO0	1	IO	0								
		MCU_SPI1_CS3	2	IO	1								
		MCU_GPIO0_14	7	IO	pad								
B2	MCU_MCAN0_TX PADCONFIG MCU_PADCONFIG13 0x04084034	MCU_MCAN0_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		WKUP_TIMER_IO0	1	IO	0								
		MCU_SPI0_CS3	2	IO	1								
		MCU_GPIO0_13	7	IO	pad								
B1	MCU_MCAN1_RX PADCONFIG MCU_PADCONFIG16 0x04084040	MCU_MCAN1_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO3	1	IO	0								
		MCU_SPI0_CS2	2	IO	1								
		MCU_SPI1_CS2	3	IO	1								
		MCU_SPI1_CLK	4	IO	0								
		MCU_GPIO0_16	7	IO	pad								
C1	MCU_MCAN1_TX PADCONFIG MCU_PADCONFIG15 0x0408403C	MCU_MCAN1_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO2	1	IO	0								
		MCU_SPI1_CS1	3	IO	1								
		MCU_EXT_REFCLK0	4	I	0								
		MCU_GPIO0_15	7	IO	pad								
A5	MCU_OSC0_XI	MCU_OSC0_XI		I					1.8 V	VDDS_OSC0	Yes	HFXOSC	

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A6	MCU_OSC0_XO	MCU_OSC0_XO		O					1.8 V	VDDS_OSC0	Yes	HFXOSC	
E8	MCU_PORz PADCONFIG MCU_PADCONFIG22 0x04084058	MCU_PORz	0	I				0	1.8 V	VDDS_OSC0	Yes	FS_RESET	
E13	MCU_RESETSTATz	MCU_RESETSTATz	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG MCU_PADCONFIG23 0x0408405C	MCU_GPIO0_21	7	IO	pad								
D10	MCU_RESETz PADCONFIG MCU_PADCONFIG21 0x04084054	MCU_RESETz	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
A9	MCU_SPI0_CLK	MCU_SPI0_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG MCU_PADCONFIG2 0x04084008	MCU_GPIO0_2	7	IO	pad								
C12	MCU_SPI0_CS0	MCU_SPI0_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG MCU_PADCONFIG0 0x04084000	WKUP_TIMER_IO1	4	IO	0								
		MCU_GPIO0_0	7	IO	pad								
A10	MCU_SPI0_CS1 PADCONFIG MCU_PADCONFIG1 0x04084004	MCU_SPI0_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_OBSCLK0	1	O									
		MCU_SYSCLKOUT0	2	O									
		MCU_EXT_REFCLK0	3	I	0								
		MCU_TIMER_IO1	4	IO	0								
		MCU_GPIO0_1	7	IO	pad								
B12	MCU_SPI0_D0	MCU_SPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG MCU_PADCONFIG3 0x0408400C	MCU_GPIO0_3	7	IO	pad								
C11	MCU_SPI0_D1	MCU_SPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG MCU_PADCONFIG4 0x04084010	MCU_GPIO0_4	7	IO	pad								
B5	MCU_UART0_CTSn	MCU_UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
	PADCONFIG MCU_PADCONFIG7 0x0408401C	MCU_TIMER_IO0	1	IO	0								
		MCU_SPI1_D0	3	IO	0								
		MCU_GPIO0_7	7	IO	pad								
C5	MCU_UART0_RTSn	MCU_UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
	PADCONFIG MCU_PADCONFIG8 0x04084020	MCU_TIMER_IO1	1	IO	0								
		MCU_SPI1_D1	3	IO	0								
		MCU_GPIO0_8	7	IO	pad								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
B8	MCU_UART0_RXD	MCU_UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
	PADCONFIG MCU_PADCONFIG5 0x04084014	MCU_GPIO0_5	7	IO	pad								
B4	MCU_UART0_TXD	MCU_UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
	PADCONFIG MCU_PADCONFIG6 0x04084018	MCU_GPIO0_6	7	IO	pad								
AC24	MDIO0_MDC	MDIO0_MDC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
	PADCONFIG PADCONFIG88 0x000F4160	GPIO0_86	7	IO	pad								
AD25	MDIO0_MDIO	MDIO0_MDIO	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
	PADCONFIG PADCONFIG87 0x000F415C	GPIO0_85	7	IO	pad								
AC1	MMC0_CALPAD	MMC0_CALPAD		A					1.8 V	VDDS_MMC0		eMMCPHY	
AE1	MMC0_CLK	MMC0_CLK		IO	0	On / Low / Off	On / SS / Off		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AE2	MMC0_CMD	MMC0_CMD		IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AD1	MMC0_DS	MMC0_DS		IO	1	On / Off / Down	On / Off / Down		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
H24	MMC1_CLK PADCONFIG PADCONFIG141 0x000F4234	MMC1_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		TIMER_IO4	2	IO	0								
		UART3_RXD	3	IO	0								
		SPI1_CS0	5	IO	0								
		SPI2_CS2	6	IO	0								
		GPIO1_46	7	IO	0								
H22	MMC1_CMD PADCONFIG PADCONFIG143 0x000F423C	MMC1_CMD	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		TIMER_IO5	2	IO	1								
		UART3_TXD	3	IO	1								
		SPI1_CLK	5	IO	1								
		SPI2_CS0	6	IO	1								
		GPIO1_47	7	IO	1								
B24	MMC1_SDCD PADCONFIG PADCONFIG144 0x000F4240	MMC1_SDCD	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART6_RXD	1	I	0								
		TIMER_IO6	2	I	0								
		UART3_RTSn	3	I	0								
		MCAN1_TX	4	I	0								
		SPI1_CS3	5	I	0								
		SPI2_CLK	6	I	0								
		GPIO1_48	7	I	0								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A24	MMC1_SDWP PADCONFIG PADCONFIG145 0x000F4244	MMC1_SDWP	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART6_TXD	1	I	0								
		TIMER_IO7	2	I	0								
		UART3_CTSn	3	I	0								
		MCAN1_RX	4	I	0								
		SPI1_CS1	5	I	0								
		GPIO1_49	7	I	0								
H26	MMC2_CLK PADCONFIG PADCONFIG70 0x000F4118	MMC2_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_ACLKR	1	IO	0								
		MCASP1_AXR5	2	IO	0								
		UART6_RXD	3	I	1								
		EHRPWM0_SYNCI	4	I	0								
		I2C3_SCL	6	IOD	1								
		GPIO0_69	7	IO	pad								
F27	MMC2_CMD PADCONFIG PADCONFIG72 0x000F4120	MMC2_CMD	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_AFSR	1	IO	0								
		MCASP1_AXR4	2	IO	0								
		UART6_TXD	3	O									
		EHRPWM0_SYNCO	4	O									
		EHRPWM_TZn_IN0	5	I	0								
		I2C3_SDA	6	IOD	1								
		GPIO0_70	7	IO	pad								
F26	MMC2_SDCD PADCONFIG PADCONFIG73 0x000F4124	MMC2_SDCD	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	LVCMOS	PU/PD
		MCASP1_ACLKX	1	IO	0								
		UART4_RXD	3	I	1								
		EHRPWM2_A	4	IO	0								
		EHRPWM_TZn_IN1	5	I	0								
		GPIO0_71	7	IO	pad								
H21	MMC2_SDWP PADCONFIG PADCONFIG74 0x000F4128	MMC2_SDWP	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	LVCMOS	PU/PD
		MCASP1_AFSX	1	IO	0								
		UART4_TXD	3	O									
		EHRPWM2_B	4	IO	0								
		EHRPWM_TZn_IN2	5	I	0								
		GPIO0_72	7	IO	pad								
AD3	MMC0_DAT0	MMC0_DAT0		IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AD2	MMC0_DAT1	MMC0_DAT1		IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AB4	MMC0_DAT2	MMC0_DAT2		IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AC2	MMC0_DAT3	MMC0_DAT3		IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AC3	MMC0_DAT4	MMC0_DAT4		IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AB3	MMC0_DAT5	MMC0_DAT5		IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AF1	MMC0_DAT6	MMC0_DAT6		IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AB2	MMC0_DAT7	MMC0_DAT7		IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
H23	MMC1_DAT0 PADCONFIG PADCONFIG140 0x000F4230	MMC1_DAT0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_HW2TSPUSH	1	IO	1								
		TIMER_IO3	2	IO	1								
		UART2_CTSn	3	IO	1								
		ECAP2_IN_APWM_OUT	4	IO	1								
		SPI2_D1	6	IO	1								
		GPIO1_45	7	IO	1								
H20	MMC1_DAT1 PADCONFIG PADCONFIG139 0x000F422C	MMC1_DAT1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_HW1TSPUSH	1	IO	1								
		TIMER_IO2	2	IO	1								
		UART2_RTSn	3	IO	1								
		ECAP1_IN_APWM_OUT	4	IO	1								
		SPI1_CS2	5	IO	1								
		SPI2_D0	6	IO	1								
		GPIO1_44	7	IO	1								
J23	MMC1_DAT2 PADCONFIG PADCONFIG138 0x000F4228	MMC1_DAT2	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_TS_SYNC	1	IO	1								
		TIMER_IO1	2	IO	1								
		UART2_TXD	3	IO	1								
		MCAN1_RX	4	IO	1								
		SPI1_D1	5	IO	1								
		SPI2_CS3	6	IO	1								
		GPIO1_43	7	IO	1								
H25	MMC1_DAT3 PADCONFIG PADCONFIG137 0x000F4224	MMC1_DAT3	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_TS_COMP	1	IO	1								
		TIMER_IO0	2	IO	1								
		UART2_RXD	3	IO	1								
		MCAN1_TX	4	IO	1								
		SPI1_D0	5	IO	1								
		SPI2_CS1	6	IO	1								
		GPIO1_42	7	IO	1								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
G26	MMC2_DAT0 PADCONFIG PADCONFIG69 0x000F4114	MMC2_DAT0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_AXR0	1	IO	0								
		EHRPWM1_B	4	IO	0								
		I2C2_SCL	5	IOD	1								
		MCASP4_AXR9	6	IO	0								
		GPIO0_68	7	IO	pad								
G27	MMC2_DAT1 PADCONFIG PADCONFIG68 0x000F4110	MMC2_DAT1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_AXR1	1	IO	0								
		EHRPWM1_A	4	IO	0								
		I2C2_SDA	5	IOD	1								
		MCASP4_AXR8	6	IO	0								
		GPIO0_67	7	IO	pad								
H27	MMC2_DAT2 PADCONFIG PADCONFIG67 0x000F410C	MMC2_DAT2	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_AXR2	1	IO	0								
		UART5_TXD	3	O									
		EHRPWM0_B	4	IO	0								
		I2C2_SDA	5	IOD	1								
		MCASP3_AXR9	6	IO	0								
		GPIO0_66	7	IO	pad								
J27	MMC2_DAT3 PADCONFIG PADCONFIG66 0x000F4108	MMC2_DAT3	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_AXR3	1	IO	0								
		UART5_RXD	3	I	1								
		EHRPWM0_A	4	IO	0								
		MCASP3_AXR8	6	IO	0								
		GPIO0_65	7	IO	pad								
AF23	OLDI0_A0N PADCONFIG PADCONFIG152 0x000F4260	OLDI0_A0N	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
		GPIO1_53	7	IO	pad								
AG24	OLDI0_A0P PADCONFIG PADCONFIG151 0x000F425C	OLDI0_A0P	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
		GPIO1_52	7	IO	pad								
AG22	OLDI0_A1N PADCONFIG PADCONFIG154 0x000F4268	OLDI0_A1N	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
		GPIO1_55	7	IO	pad								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AG23	OLDI0_A1P	OLDI0_A1P	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG153 0x000F4264	GPIO1_54	7	IO	pad								
AB20	OLDI0_A2N	OLDI0_A2N	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG156 0x000F4270	GPIO1_57	7	IO	pad								
AB21	OLDI0_A2P	OLDI0_A2P	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG155 0x000F426C	GPIO1_56	7	IO	pad								
AG20	OLDI0_A3N	OLDI0_A3N	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG158 0x000F4278	GPIO1_59	7	IO	pad								
AG21	OLDI0_A3P	OLDI0_A3P	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG157 0x000F4274	GPIO1_58	7	IO	pad								
AD21	OLDI0_A4N	OLDI0_A4N	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG160 0x000F4280	GPIO1_61	7	IO	pad								
AC21	OLDI0_A4P	OLDI0_A4P	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG159 0x000F427C	GPIO1_60	7	IO	pad								
AF19	OLDI0_A5N	OLDI0_A5N	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG162 0x000F4288	GPIO1_63	7	IO	pad								
AF18	OLDI0_A5P	OLDI0_A5P	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG161 0x000F4284	GPIO1_62	7	IO	pad								
AG17	OLDI0_A6N	OLDI0_A6N	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG164 0x000F4290	GPIO1_65	7	IO	pad								
AG18	OLDI0_A6P	OLDI0_A6P	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG163 0x000F428C	GPIO1_64	7	IO	pad								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AB19	OLDI0_A7N	OLDI0_A7N	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG166 0x000F4298	GPIO1_67	7	IO	pad								
AA20	OLDI0_A7P	OLDI0_A7P	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG165 0x000F4294	GPIO1_66	7	IO	pad								
AF21	OLDI0_CLK0N	OLDI0_CLK0N	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG168 0x000F42A0	GPIO1_69	7	IO	pad								
AE20	OLDI0_CLK0P	OLDI0_CLK0P	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG167 0x000F429C	GPIO1_68	7	IO	pad								
AD20	OLDI0_CLK1N	OLDI0_CLK1N	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG170 0x000F42A8	GPIO1_71	7	IO	pad								
AE19	OLDI0_CLK1P	OLDI0_CLK1P	0	IO	0	Off / Off / NA	Off / Off / NA	0	1.8 V	VDDA_1P8_OLDI0		MLB_LVDS	
	PADCONFIG PADCONFIG169 0x000F42A4	GPIO1_70	7	IO	pad								
L24	OSPI0_CLK	OSPI0_CLK	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
	PADCONFIG PADCONFIG0 0x000F4000	GPIO0_0	7	IO	pad								
L22	OSPI0_DQS	OSPI0_DQS	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
	PADCONFIG PADCONFIG2 0x000F4008	UART5_CTSn	5	I	1								
		GPIO0_2	7	IO	pad								
L23	OSPI0_LBCLKO	OSPI0_LBCLKO	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
	PADCONFIG PADCONFIG1 0x000F4004	UART5_RTSn	5	O									
		GPIO0_1	7	IO	pad								
K26	OSPI0_CSn0	OSPI0_CSn0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
	PADCONFIG PADCONFIG11 0x000F402C	GPIO0_11	7	IO	pad								
K23	OSPI0_CSn1	OSPI0_CSn1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
	PADCONFIG PADCONFIG12 0x000F4030	GPIO0_12	7	IO	pad								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
K22	OSPI0_CSn2 PADCONFIG PADCONFIG13 0x000F4034	OSPI0_CSn2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_CS1	1	IO	1								
		OSPI0_RESET_OUT1	2	O									
		MCASP1_AFSR	3	IO	0								
		MCASP1_AXR2	4	IO	0								
		UART5_RXD	5	I	1								
		GPIO0_13	7	IO	pad								
J22	OSPI0_CSn3 PADCONFIG PADCONFIG14 0x000F4038	OSPI0_CSn3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		OSPI0_RESET_OUT0	1	O									
		OSPI0_ECC_FAIL	2	I	1								
		MCASP1_ACLKR	3	IO	0								
		MCASP1_AXR3	4	IO	0								
		UART5_TXD	5	O									
		GPIO0_14	7	IO	pad								
K27	OSPI0_D0 PADCONFIG PADCONFIG3 0x000F400C	OSPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_3	7	IO	pad								
L27	OSPI0_D1 PADCONFIG PADCONFIG4 0x000F4010	OSPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_4	7	IO	pad								
L26	OSPI0_D2 PADCONFIG PADCONFIG5 0x000F4014	OSPI0_D2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_5	7	IO	pad								
L25	OSPI0_D3 PADCONFIG PADCONFIG6 0x000F4018	OSPI0_D3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_6	7	IO	pad								
L21	OSPI0_D4 PADCONFIG PADCONFIG7 0x000F401C	OSPI0_D4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_CS0	1	IO	1								
		MCASP1_AXR1	2	IO	0								
		UART6_RXD	3	I	1								
		GPIO0_7	7	IO	pad								
M26	OSPI0_D5 PADCONFIG PADCONFIG8 0x000F4020	OSPI0_D5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_CLK	1	IO	0								
		MCASP1_AXR0	2	IO	0								
		UART6_TXD	3	O									
		GPIO0_8	7	IO	pad								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
N27	OSPI0_D6 PADCONFIG PADCONFIG9 0x000F4024	OSPI0_D6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_D0	1	IO	0								
		MCASP1_ACLKX	2	IO	0								
		UART6_RTSn	3	O									
		GPIO0_9	7	IO	pad								
M27	OSPI0_D7 PADCONFIG PADCONFIG10 0x000F4028	OSPI0_D7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_D1	1	IO	0								
		MCASP1_AFSX	2	IO	0								
		UART6_CTSn	3	I	1								
		GPIO0_10	7	IO	pad								
F25	PCIE0_CLKREQn PADCONFIG PADCONFIG171 0x000F42AC	PCIE0_CLKREQn	0	IOD	0	On / Low / NA	On / SS / NA	0	1.8 V/3.3 V	VDDSHV0	Yes	I2C OPEN DRAIN	
		GPIO1_72	7	IOD	pad								
A8	PMIC_LPM_EN0 PADCONFIG MCU_PADCONFIG32 0x04084080	PMIC_LPM_EN0	0	O		Off / Off / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_GPIO0_22	7	IO	pad								
D27	PORz_OUT PADCONFIG PADCONFIG148 0x000F4250	PORz_OUT	0	O		Off / Low / Off	Off / SS / Off		1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
E27	RESETSTATz PADCONFIG PADCONFIG147 0x000F424C	RESETSTATz	0	O		Off / Low / Off	Off / SS / Off		1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
E26	RESET_REQz PADCONFIG PADCONFIG146 0x000F4248	RESET_REQz	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
AE27	RGMII1_RXC PADCONFIG PADCONFIG82 0x000F4148	RGMII1_RXC	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_REF_CLK	1	I	0								
		GPIO0_80	7	IO	pad								
AD23	RGMII1_RX_CTL PADCONFIG PADCONFIG81 0x000F4144	RGMII1_RX_CTL	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_RX_ER	1	I	0								
		GPIO0_79	7	IO	pad								
AG26	RGMII1_TXC PADCONFIG PADCONFIG76 0x000F4130	RGMII1_TXC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_CRS_DV	1	I	0								
		GPIO0_74	7	IO	pad								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AF25	RGMII1_TX_CTL PADCONFIG PADCONFIG75 0x000F412C	RGMII1_TX_CTL	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_TX_EN	1	O									
		GPIO0_73	7	IO	pad								
AC25	RGMII1_RD0 PADCONFIG PADCONFIG83 0x000F414C	RGMII1_RD0	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_RXD0	1	I	0								
		GPIO0_81	7	IO	pad								
AD27	RGMII1_RD1 PADCONFIG PADCONFIG84 0x000F4150	RGMII1_RD1	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_RXD1	1	I	0								
		GPIO0_82	7	IO	pad								
AE24	RGMII1_RD2 PADCONFIG PADCONFIG85 0x000F4154	RGMII1_RD2	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_83	7	IO	pad								
AE26	RGMII1_RD3 PADCONFIG PADCONFIG86 0x000F4158	RGMII1_RD3	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_84	7	IO	pad								
AF27	RGMII1_TD0 PADCONFIG PADCONFIG77 0x000F4134	RGMII1_TD0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_TXD0	1	O									
		GPIO0_75	7	IO	pad								
AE23	RGMII1_TD1 PADCONFIG PADCONFIG78 0x000F4138	RGMII1_TD1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_TXD1	1	O									
		GPIO0_76	7	IO	pad								
AG25	RGMII1_TD2 PADCONFIG PADCONFIG79 0x000F413C	RGMII1_TD2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_77	7	IO	pad								
AF24	RGMII1_TD3 PADCONFIG PADCONFIG80 0x000F4140	RGMII1_TD3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		CLKOUT0	1	O									
		GPIO0_78	7	IO	pad								
E9	RSVD0	RSVD0		N/A									
AA19	RSVD1	RSVD1		N/A									
AB7	RSVD2	RSVD2		N/A									
AC5	RSVD3	RSVD3		N/A									
AB10	RSVD4	RSVD4		N/A									
AA12	RSVD5	RSVD5		N/A									
AB12	RSVD6	RSVD6		N/A									
AB13	RSVD7	RSVD7		N/A									

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AA15	RSVD8	RSVD8		N/A									
AA14	RSVD9	RSVD9		N/A									
L5	RSVD10	RSVD10		N/A									
M6	RSVD11	RSVD11		N/A									
AB16	RSVD12	RSVD12		N/A									
AB18	RSVD13	RSVD13		N/A									
C6	RSVD14	RSVD14		N/A									
F8	RSVD15	RSVD15		N/A									
B6	RSVD16	RSVD16		N/A									
C17	RSVD17	RSVD17		N/A									
D16	RSVD18	RSVD18		N/A									
D14	RSVD19	RSVD19		N/A									
D13	RSVD20	RSVD20		N/A									
M2	RSVD21	RSVD21		N/A									
E15	SERDES0_REXT	SERDES0_REXT		A					1.8 V	VDDA_1P8_SERDES		4L_PHY	
F14	SERDES1_REXT	SERDES1_REXT		A					1.8 V	VDDA_1P8_SERDES		4L_PHY	
A17	SERDES0_REFCLK0N	SERDES0_REFCLK0N		IO					1.8 V	VDDA_1P8_SERDES		4L_PHY	
A16	SERDES0_REFCLK0P	SERDES0_REFCLK0P		IO					1.8 V	VDDA_1P8_SERDES		4L_PHY	
A20	SERDES0_RX0_N	SERDES0_RX0_N		I					1.8 V	VDDA_1P8_SERDES		4L_PHY	
A19	SERDES0_RX0_P	SERDES0_RX0_P		I					1.8 V	VDDA_1P8_SERDES		4L_PHY	
B19	SERDES0_TX0_N	SERDES0_TX0_N		O					1.8 V	VDDA_1P8_SERDES		4L_PHY	
B18	SERDES0_TX0_P	SERDES0_TX0_P		O					1.8 V	VDDA_1P8_SERDES		4L_PHY	
B15	SERDES1_REFCLK0N	SERDES1_REFCLK0N		IO					1.8 V	VDDA_1P8_SERDES		4L_PHY	
B16	SERDES1_REFCLK0P	SERDES1_REFCLK0P		IO					1.8 V	VDDA_1P8_SERDES		4L_PHY	
C14	SERDES1_RX0_N	SERDES1_RX0_N		I					1.8 V	VDDA_1P8_SERDES		4L_PHY	
C15	SERDES1_RX0_P	SERDES1_RX0_P		I					1.8 V	VDDA_1P8_SERDES		4L_PHY	
A13	SERDES1_TX0_N	SERDES1_TX0_N		O					1.8 V	VDDA_1P8_SERDES		4L_PHY	
A14	SERDES1_TX0_P	SERDES1_TX0_P		O					1.8 V	VDDA_1P8_SERDES		4L_PHY	
D20	SPI0_CLK PADCONFIG PADCONFIG111 0x000F41BC	SPI0_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_TS_SYNC	1	O									
		EHRPWM1_A	2	IO	0								
		GPIO1_17	7	IO	pad								
B20	SPI0_CS0 PADCONFIG PADCONFIG109 0x000F41B4	SPI0_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		EHRPWM0_A	2	IO	0								
		GPIO1_15	7	IO	pad								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
C20	SPI0_CS1 PADCONFIG PADCONFIG110 0x000F41B8	SPI0_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_TS_COMP	1	O									
		EHRPWM0_B	2	IO	0								
		ECAP0_IN_APWM_OUT	3	IO	0								
		MAIN_ERRORn	5	IO	1								
		GPIO1_16	7	IO	pad								
		EHRPWM_TZn_IN5	9	I	0								
E19	SPI0_D0 PADCONFIG PADCONFIG112 0x000F41C0	SPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_HW1TSPUSH	1	I	0								
		EHRPWM1_B	2	IO	0								
		GPIO1_18	7	IO	pad								
E20	SPI0_D1 PADCONFIG PADCONFIG113 0x000F41C4	SPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_HW2TSPUSH	1	I	0								
		EHRPWM_TZn_IN0	2	I	0								
		GPIO1_19	7	IO	pad								
A11	TCK PADCONFIG MCU_PADCONFIG25 0x04084064	TCK	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
E12	TDI PADCONFIG MCU_PADCONFIG27 0x0408406C	TDI	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
F10	TDO PADCONFIG MCU_PADCONFIG28 0x04084070	TDO	0	OZ		Off / Off / Up	Off / SS / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
F11	TMS PADCONFIG MCU_PADCONFIG29 0x04084074	TMS	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
B10	TRSTn PADCONFIG MCU_PADCONFIG26 0x04084068	TRSTn	0	I		On / Off / Down	On / Off / Down	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
E22	UART0_CTSn PADCONFIG PADCONFIG116 0x000F41D0	UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI0_CS2	1	IO	1								
		I2C3_SCL	2	IOD	1								
		UART2_RXD	3	I	1								
		TIMER_IO6	4	IO	0								
		AUDIO_EXT_REFCLK0	5	IO	0								
		GPIO1_22	7	IO	pad								
		MCASP2_AFSX	8	IO	0								
		MMC2_SDCD	9	I	0								
B21	UART0_RTSn PADCONFIG PADCONFIG117 0x000F41D4	UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI0_CS3	1	IO	1								
		I2C3_SDA	2	IOD	1								
		UART2_TXD	3	O									
		TIMER_IO7	4	IO	0								
		AUDIO_EXT_REFCLK1	5	IO	0								
		GPIO1_23	7	IO	pad								
		MCASP2_ACLKX	8	IO	0								
		MMC2_SDWP	9	I	0								
F19	UART0_RXD PADCONFIG PADCONFIG114 0x000F41C8	UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		ECAP1_IN_APWM_OUT	1	IO	0								
		SPI2_D0	2	IO	0								
		EHRPWM2_A	3	IO	0								
		GPIO1_20	7	IO	pad								
F20	UART0_TXD PADCONFIG PADCONFIG115 0x000F41CC	UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		ECAP2_IN_APWM_OUT	1	IO	0								
		SPI2_D1	2	IO	0								
		EHRPWM2_B	3	IO	0								
		GPIO1_21	7	IO	pad								
AB5	USB0_DM	USB0_DM		IO					1.8 V/3.3 V	VDDA_1P8_USB0, VDDA_3P3_USB0		USB2PHY	
AA6	USB0_DP	USB0_DP		IO					1.8 V/3.3 V	VDDA_1P8_USB0, VDDA_3P3_USB0		USB2PHY	
E25	USB0_DRVVBUS PADCONFIG PADCONFIG149 0x000F4254	USB0_DRVVBUS	0	O		Off / Off / Down	Off / Off / Down	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		GPIO1_50	7	IO	pad								
AA8	USB0_RCALIB	USB0_RCALIB		A					1.8 V/3.3 V	VDDA_1P8_USB0, VDDA_3P3_USB0		USB2PHY	

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
W7	USB0_VBUS	USB0_VBUS		A					1.8 V/3.3 V	VDDA_1P8_USB0, VDDA_3P3_USB0		USB2PHY	
E17	USB1_DM	USB1_DM		IO					1.8 V/3.3 V	VDDA_1P8_USB1, VDDA_3P3_USB1		USB2PHY	
D17	USB1_DP	USB1_DP		IO					1.8 V/3.3 V	VDDA_1P8_USB1, VDDA_3P3_USB1		USB2PHY	
B27	USB1_DRVVBUS	USB1_DRVVBUS	0	O		Off / Off / Down	Off / Off / Down	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
	PADCONFIG PADCONFIG150 0x000F4258	GPIO1_51	7	IO	pad								
E18	USB1_RCALIB	USB1_RCALIB		A					1.8 V/3.3 V	VDDA_1P8_USB1, VDDA_3P3_USB1		USB2PHY	
F18	USB1_VBUS	USB1_VBUS		A					1.8 V/3.3 V	VDDA_1P8_USB1, VDDA_3P3_USB1		USB2PHY	
H12, H13	VDDA_0P85_SERDES	VDDA_0P85_SERDES		PWR									
J13	VDDA_0P85_SERDES_C	VDDA_0P85_SERDES_C		PWR									
W9	VDDA_0P85_DLL_MMC0	VDDA_0P85_DLL_MMC0		PWR									
W13, W16, Y13	VDDA_1P8_CSI_DSI	VDDA_1P8_CSI_DSI		PWR									
G13	VDDA_1P8_SERDES	VDDA_1P8_SERDES		PWR									
W18, Y19	VDDA_1P8_OLDI0	VDDA_1P8_OLDI0		PWR									
Y12	VDDA_1P8_USB0	VDDA_1P8_USB0		PWR									
H16	VDDA_1P8_USB1	VDDA_1P8_USB1		PWR									
Y11	VDDA_3P3_USB0	VDDA_3P3_USB0		PWR									
G15	VDDA_3P3_USB1	VDDA_3P3_USB1		PWR									
W15, Y15	VDDA_CORE_CSI_DSI	VDDA_CORE_CSI_DSI		PWR									
Y16	VDDA_CORE_CSI_DSI_CLK	VDDA_CORE_CSI_DSI_CLK		PWR									
W11	VDDA_CORE_USB0	VDDA_CORE_USB0		PWR									
H15	VDDA_CORE_USB1	VDDA_CORE_USB1		PWR									
P9	VDDA_DDR_PLL0	VDDA_DDR_PLL0		PWR									
G11, H11	VDDA_MCU	VDDA_MCU		PWR									
L15	VDDA_PLL0	VDDA_PLL0		PWR									
K10	VDDA_PLL1	VDDA_PLL1		PWR									
M12	VDDA_PLL2	VDDA_PLL2		PWR									
R11	VDDA_PLL3	VDDA_PLL3		PWR									
V18	VDDA_PLL4	VDDA_PLL4		PWR									
P16	VDDA_PLL5	VDDA_PLL5		PWR									
Y17	VDDA_TEMP0	VDDA_TEMP0		PWR									
T11	VDDA_TEMP1	VDDA_TEMP1		PWR									
L9	VDDA_TEMP2	VDDA_TEMP2		PWR									

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
M13, M19, N13, N19, U10, U17, V10, V17	VDDR_CORE	VDDR_CORE		PWR									
G18, H18	VDDSHV0	VDDSHV0		PWR									
K20, L20	VDDSHV1	VDDSHV1		PWR									
T19, T20	VDDSHV2	VDDSHV2		PWR									
M20, P20, R20	VDDSHV3	VDDSHV3		PWR									
H19	VDDSHV5	VDDSHV5		PWR									
J21	VDDSHV6	VDDSHV6		PWR									
H9	VDDSHV_CANUART	VDDSHV_CANUART		PWR									
H10	VDDSHV_MCU	VDDSHV_MCU		PWR									
AB1, D1, L7, L8, N7, N8, T7, T8	VDDS_DDR	VDDS_DDR		PWR									
P8	VDDS_DDR_C	VDDS_DDR_C		PWR									
Y9	VDDS_MMC0	VDDS_MMC0		PWR									
K8	VDDS_OSC0	VDDS_OSC0		PWR									
J8	VDD_CANUART	VDD_CANUART		PWR									
J11, J14, J16, J18, K11, K12, K14, K16, K18, K9, L12, L17, M10, M15, M17, M9, N10, N11, N14, N16, N18, P11, P12, P14, P18, R12, R13, R15, R17, R9, T13, T15, T17, T9, U12, U14, U16, U8, V12, V14, V16, V19, V8, W19, Y20, Y21	VDD_CORE	VDD_CORE		PWR									
W10	VDD_MMC0	VDD_MMC0		PWR									
J7	VMON_1P8_SOC	VMON_1P8_SOC		A									
K7	VMON_3P3_SOC	VMON_3P3_SOC		A									
G7	VMON_ER_VSYS	VMON_ER_VSYS		A									

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AC27	VOUT0_DE PADCONFIG PADCONFIG63 0x000F40FC	VOUT0_DE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A17	1	OZ									
		RGMII2_RD1	2	I	0								
		RMII2_RXD1	3	I	0								
		UART3_CTSn	4	I	1								
		MCASP4_AXR5	6	IO	0								
		GPIO0_62	7	IO	pad								
AB24	VOUT0_HSYNC PADCONFIG PADCONFIG62 0x000F40F8	VOUT0_HSYNC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A16	1	OZ									
		RGMII2_RD0	2	I	0								
		RMII2_RXD0	3	I	0								
		UART3_RTSn	4	O									
		MCASP4_AXR4	6	IO	0								
		GPIO0_61	7	IO	pad								
AC26	VOUT0_PCLK PADCONFIG PADCONFIG65 0x000F4104	VOUT0_PCLK	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A19	1	OZ									
		RGMII2_RD3	2	I	0								
		UART2_CTSn	4	I	1								
		MCASP4_AFSX	6	IO	0								
		GPIO0_64	7	IO	pad								
AB23	VOUT0_VSYNC PADCONFIG PADCONFIG64 0x000F4100	VOUT0_VSYNC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A18	1	OZ									
		RGMII2_RD2	2	I	0								
		UART2_RTSn	4	O									
		MCASP4_ACLKX	6	IO	0								
		GPIO0_63	7	IO	pad								
W27	VOUT0_DATA0 PADCONFIG PADCONFIG46 0x000F40B8	VOUT0_DATA0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A0	1	OZ									
		UART2_RXD	4	I	1								
		MCASP3_ACLKX	6	IO	0								
		GPIO0_45	7	IO	pad								
W25	VOUT0_DATA1 PADCONFIG PADCONFIG47 0x000F40BC	VOUT0_DATA1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A1	1	OZ									
		UART2_TXD	4	O									
		MCASP3_AFSX	6	IO	0								
		GPIO0_46	7	IO	pad								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
W24	VOUT0_DATA2 PADCONFIG PADCONFIG48 0x000F40C0	VOUT0_DATA2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A2	1	OZ									
		UART3_RXD	4	I	1								
		MCASP3_AXR0	6	IO	0								
		GPIO0_47	7	IO	pad								
W23	VOUT0_DATA3 PADCONFIG PADCONFIG49 0x000F40C4	VOUT0_DATA3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A3	1	OZ									
		UART3_TXD	4	O									
		AUDIO_EXT_REFCLK0	5	IO	0								
		MCASP3_AXR1	6	IO	0								
		GPIO0_48	7	IO	pad								
W22	VOUT0_DATA4 PADCONFIG PADCONFIG50 0x000F40C8	VOUT0_DATA4	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A4	1	OZ									
		UART4_RXD	4	I	1								
		EQEP2_I	5	IO	0								
		MCASP3_AXR2	6	IO	0								
		GPIO0_49	7	IO	pad								
W21	VOUT0_DATA5 PADCONFIG PADCONFIG51 0x000F40CC	VOUT0_DATA5	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A5	1	OZ									
		UART4_TXD	4	O									
		EQEP2_S	5	IO	0								
		MCASP3_AXR3	6	IO	0								
		GPIO0_50	7	IO	pad								
Y26	VOUT0_DATA6 PADCONFIG PADCONFIG52 0x000F40D0	VOUT0_DATA6	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A6	1	OZ									
		UART5_RXD	4	I	1								
		EQEP2_A	5	I	0								
		MCASP3_AXR6	6	IO	0								
		GPIO0_51	7	IO	pad								
		MCASP3_ACLKR	8	IO	0								
Y27	VOUT0_DATA7 PADCONFIG PADCONFIG53 0x000F40D4	VOUT0_DATA7	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A7	1	OZ									
		UART5_TXD	4	O									
		EQEP2_B	5	I	0								
		MCASP3_AXR7	6	IO	0								
		GPIO0_52	7	IO	pad								
		MCASP3_AFSR	8	IO	0								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AA24	VOUT0_DATA8 PADCONFIG PADCONFIG54 0x000F40D8	VOUT0_DATA8	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A8	1	OZ									
		RGMII2_TX_CTL	2	O									
		RMII2_TX_EN	3	O									
		UART6_RXD	4	I	1								
		MCASP3_AXR4	6	IO	0								
		GPIO0_53	7	IO	pad								
AA27	VOUT0_DATA9 PADCONFIG PADCONFIG55 0x000F40DC	VOUT0_DATA9	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A9	1	OZ									
		RGMII2_TXC	2	O									
		RMII2_CRS_DV	3	I	0								
		UART6_TXD	4	O									
		MCASP3_AXR5	6	IO	0								
		GPIO0_54	7	IO	pad								
AA25	VOUT0_DATA10 PADCONFIG PADCONFIG56 0x000F40E0	VOUT0_DATA10	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A10	1	OZ									
		RGMII2_TD0	2	O									
		RMII2_TXD0	3	O									
		UART6_RTSn	4	O									
		MCASP4_AXR6	6	IO	0								
		GPIO0_55	7	IO	pad								
		MCASP4_ACLKR	8	IO	0								
AB25	VOUT0_DATA11 PADCONFIG PADCONFIG57 0x000F40E4	VOUT0_DATA11	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A11	1	OZ									
		RGMII2_TD1	2	O									
		RMII2_TXD1	3	O									
		UART6_CTSn	4	I	1								
		MCASP4_AXR7	6	IO	0								
		GPIO0_56	7	IO	pad								
		MCASP4_AFSR	8	IO	0								
AA23	VOUT0_DATA12 PADCONFIG PADCONFIG58 0x000F40E8	VOUT0_DATA12	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A12	1	OZ									
		RGMII2_TD2	2	O									
		UART5_RTSn	4	O									
		MCASP4_AXR0	6	IO	0								
		GPIO0_57	7	IO	pad								

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AA22	VOUT0_DATA13 PADCONFIG PADCONFIG59 0x000F40EC	VOUT0_DATA13	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A13	1	OZ									
		RGMII2_TD3	2	O									
		CLKOUT0	3	O									
		UART5_CTSn	4	I	1								
		MCASP4_AXR1	6	IO	0								
		GPIO0_58	7	IO	pad								
AB26	VOUT0_DATA14 PADCONFIG PADCONFIG60 0x000F40F0	VOUT0_DATA14	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A14	1	OZ									
		RGMII2_RX_CTL	2	I	0								
		RMII2_RX_ER	3	I	0								
		UART4_RTSn	4	O									
		MCASP4_AXR2	6	IO	0								
		GPIO0_59	7	IO	pad								
AB27	VOUT0_DATA15 PADCONFIG PADCONFIG61 0x000F40F4	VOUT0_DATA15	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A15	1	OZ									
		RGMII2_RXC	2	I	0								
		RMII2_REF_CLK	3	I	0								
		UART4_CTSn	4	I	1								
		MCASP4_AXR3	6	IO	0								
		GPIO0_60	7	IO	pad								
G9	VPP	VPP		PWR									

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Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A1, A18, A21, A27, A4, A7, AA1, AA18, AA21, AA26, AA4, AD26, AG1, AG27, C2, C23, D26, E6, F15, F16, F17, F2, F21, G1, G10, G12, G14, G16, G17, G20, G3, G5, G8, H14, H4, H7, J12, J15, J17, J19, J26, J3, J5, J9, K1, K13, K15, K17, K19, L10, L11, L13, L14, L16, L18, M1, M11, M14, M16, M18, M7, M8, N12, N15, N17, N26, N9, P10, P13, P15, P17, P19, P5, P7, R1, R10, R14, R16, R18, R19, R4, R7, R8, T10, T12, T14, T16, T18, T26, U11, U13, U15, U18, U19, U3, U7, U9, V1, V11, V13, V15, V20, V4, V7, V9, W12, W14, W17, W20, W5, W8, Y10, Y14, Y18, Y7, Y8	VSS	VSS		GND									
F12	WKUP_CLKOUT0 PADCONFIG MCU_PADCONFIG33 0x04084084	WKUP_CLKOUT0 MCU_GPIO0_23	0 7	O IO	pad	Off / Off / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD

Table 5-1. Pin Attributes (AMW Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
B9	WKUP_I2C0_SCL PADCONFIG MCU_PADCONFIG19 0x0408404C	WKUP_I2C0_SCL	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OPEN DRAIN	
		MCU_GPIO0_19	7	IOD	pad								
D11	WKUP_I2C0_SDA PADCONFIG MCU_PADCONFIG20 0x04084050	WKUP_I2C0_SDA	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OPEN DRAIN	
		MCU_GPIO0_20	7	IOD	pad								
A3	WKUP_LFOSC0_XI	WKUP_LFOSC0_XI		I					1.8 V	VDDS_OSC0		LFXOSC	
A2	WKUP_LFOSC0_XO	WKUP_LFOSC0_XO		O					1.8 V	VDDS_OSC0		LFXOSC	
C4	WKUP_UART0_CTSn PADCONFIG MCU_PADCONFIG11 0x0408402C	WKUP_UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		WKUP_TIMER_IO0	1	IO	0								
		MCU_SPI1_CS0	3	IO	1								
		MCU_GPIO0_11	7	IO	pad								
C3	WKUP_UART0_RTSn PADCONFIG MCU_PADCONFIG12 0x04084030	WKUP_UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		WKUP_TIMER_IO1	1	IO	0								
		MCU_SPI1_CLK	3	IO	0								
		MCU_GPIO0_12	7	IO	pad								
B3	WKUP_UART0_RXD PADCONFIG MCU_PADCONFIG9 0x04084024	WKUP_UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_SPI0_CS2	2	IO	1								
		MCU_GPIO0_9	7	IO	pad								
C8	WKUP_UART0_TXD PADCONFIG MCU_PADCONFIG10 0x04084028	WKUP_UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_SPI1_CS2	2	IO	1								
		MCU_GPIO0_10	7	IO	pad								

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5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via PADCONFIG registers. Device subsystems may provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor
3. **DESCRIPTION:** Description of the signal
4. **BALL:** Ball number(s) associated with signal

5.3.1 CPSW3G

5.3.1.1 MAIN Domain

Table 5-2. CPSW3G0 RGMII1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
RGMII1_RXC	I	RGMII Receive Clock	AE27
RGMII1_RX_CTL	I	RGMII Receive Control	AD23
RGMII1_TXC	O	RGMII Transmit Clock	AG26
RGMII1_TX_CTL	O	RGMII Transmit Control	AF25
RGMII1_RD0	I	RGMII Receive Data 0	AC25
RGMII1_RD1	I	RGMII Receive Data 1	AD27
RGMII1_RD2	I	RGMII Receive Data 2	AE24
RGMII1_RD3	I	RGMII Receive Data 3	AE26
RGMII1_TD0	O	RGMII Transmit Data 0	AF27
RGMII1_TD1	O	RGMII Transmit Data 1	AE23
RGMII1_TD2	O	RGMII Transmit Data 2	AG25
RGMII1_TD3	O	RGMII Transmit Data 3	AF24

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Table 5-3. CPSW3G0 RGMII2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
RGMII2_RXC	I	RGMII Receive Clock	AB27
RGMII2_RX_CTL	I	RGMII Receive Control	AB26
RGMII2_TXC	O	RGMII Transmit Clock	AA27
RGMII2_TX_CTL	O	RGMII Transmit Control	AA24
RGMII2_RD0	I	RGMII Receive Data 0	AB24
RGMII2_RD1	I	RGMII Receive Data 1	AC27
RGMII2_RD2	I	RGMII Receive Data 2	AB23
RGMII2_RD3	I	RGMII Receive Data 3	AC26
RGMII2_TD0	O	RGMII Transmit Data 0	AA25
RGMII2_TD1	O	RGMII Transmit Data 1	AB25
RGMII2_TD2	O	RGMII Transmit Data 2	AA23
RGMII2_TD3	O	RGMII Transmit Data 3	AA22

Table 5-4. CPSW3G0 RMII1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
RMII1_CRS_DV	I	RMII Carrier Sense / Data Valid	AG26
RMII1_REF_CLK	I	RMII Reference Clock	AE27
RMII1_RX_ER	I	RMII Receive Data Error	AD23
RMII1_TX_EN	O	RMII Transmit Enable	AF25
RMII1_RXD0	I	RMII Receive Data 0	AC25
RMII1_RXD1	I	RMII Receive Data 1	AD27
RMII1_TXD0	O	RMII Transmit Data 0	AF27
RMII1_TXD1	O	RMII Transmit Data 1	AE23

Table 5-5. CPSW3G0 RMII2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
RMII2_CRS_DV	I	RMII Carrier Sense / Data Valid	AA27
RMII2_REF_CLK	I	RMII Reference Clock	AB27
RMII2_RX_ER	I	RMII Receive Data Error	AB26
RMII2_TX_EN	O	RMII Transmit Enable	AA24
RMII2_RXD0	I	RMII Receive Data 0	AB24
RMII2_RXD1	I	RMII Receive Data 1	AC27
RMII2_TXD0	O	RMII Transmit Data 0	AA25
RMII2_TXD1	O	RMII Transmit Data 1	AB25

5.3.2 CPTS

5.3.2.1 MAIN Domain

Table 5-6. CPTS Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
CP_GEMAC_CPTS0_RFT_CLK	I	CPTS Reference Clock Input	A23
CP_GEMAC_CPTS0_TS_COMP	O	CPTS Time Stamp Counter Compare Output from CPSW3G0 CPTS	C20, H25

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Table 5-6. CPTS Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
CP_GEMAC_CPTS0_TS_SYNC	IO	CPTS Time Stamp Counter Bit Output from CPSW3G0 CPTS	D20, J23
CP_GEMAC_CPTS0_HW1TSPUSH	IO	CPTS Hardware Time Stamp Push Input to Time Sync Router	E19, H20
CP_GEMAC_CPTS0_HW2TSPUSH	IO	CPTS Hardware Time Stamp Push Input to Time Sync Router	E20, H23

5.3.3 CSI-2

5.3.3.1 MAIN Domain

Table 5-7. CSIRX0 Signal Descriptions

SIGNAL NAME [1] ((2))	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
CSI0_RXCLKN	I	CSI Differential Receive Clock Input (negative)	AC7
CSI0_RXCLKP	I	CSI Differential Receive Clock Input (positive)	AC6
CSI0_RXRCALIB (1)	A	CSI pin connected to external resistor for on-chip resistor calibration	AB8
CSI0_RXN0	I	CSI Differential Receive Input (negative)	AD6
CSI0_RXN1	I	CSI Differential Receive Input (negative)	AE5
CSI0_RXN2	I	CSI Differential Receive Input (negative)	AF4
CSI0_RXN3	I	CSI Differential Receive Input (negative)	AG3
CSI0_RXP0	I	CSI Differential Receive Input (positive)	AD5
CSI0_RXP1	I	CSI Differential Receive Input (positive)	AE4
CSI0_RXP2	I	CSI Differential Receive Input (positive)	AF3
CSI0_RXP3	I	CSI Differential Receive Input (positive)	AG2

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.
(2) CSI TX functionality is available on the DSI pins. For more information, refer to Section 5.3.5.1.1, *DSITX0 Signal Descriptions*.

Table 5-8. CSIRX1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
CSI1_RXCLKN	I	CSI Differential Receive Clock Input (negative)	AG6
CSI1_RXCLKP	I	CSI Differential Receive Clock Input (positive)	AG5
CSI1_RXRCALIB (1)	A	CSI pin connected to external resistor for on-chip resistor calibration	AA10
CSI1_RXN0	I	CSI Differential Receive Input (negative)	AF7
CSI1_RXN1	I	CSI Differential Receive Input (negative)	AE8
CSI1_RXN2	I	CSI Differential Receive Input (negative)	AD9
CSI1_RXN3	I	CSI Differential Receive Input (negative)	AC10
CSI1_RXP0	I	CSI Differential Receive Input (positive)	AF6
CSI1_RXP1	I	CSI Differential Receive Input (positive)	AE7
CSI1_RXP2	I	CSI Differential Receive Input (positive)	AD8
CSI1_RXP3	I	CSI Differential Receive Input (positive)	AC9

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.

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Table 5-9. CSIRX2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
CSI2_RXCLKN	I	CSI Differential Receive Clock Input (negative)	AG8
CSI2_RXCLKP	I	CSI Differential Receive Clock Input (positive)	AG9
CSI2_RXRCALIB (1)	A	CSI pin connected to external resistor for on-chip resistor calibration	AB14
CSI2_RXN0	I	CSI Differential Receive Input (negative)	AF9
CSI2_RXN1	I	CSI Differential Receive Input (negative)	AE10
CSI2_RXN2	I	CSI Differential Receive Input (negative)	AD11
CSI2_RXN3	I	CSI Differential Receive Input (negative)	AC13
CSI2_RXP0	I	CSI Differential Receive Input (positive)	AF10
CSI2_RXP1	I	CSI Differential Receive Input (positive)	AE11
CSI2_RXP2	I	CSI Differential Receive Input (positive)	AD12
CSI2_RXP3	I	CSI Differential Receive Input (positive)	AC12

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.

Table 5-10. CSIRX3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
CSI3_RXCLKN	I	CSI Differential Receive Clock Input (negative)	AG12
CSI3_RXCLKP	I	CSI Differential Receive Clock Input (positive)	AG11
CSI3_RXRCALIB (1)	A	CSI pin connected to external resistor for on-chip resistor calibration	AB15
CSI3_RXN0	I	CSI Differential Receive Input (negative)	AF13
CSI3_RXN1	I	CSI Differential Receive Input (negative)	AE14
CSI3_RXN2	I	CSI Differential Receive Input (negative)	AD15
CSI3_RXN3	I	CSI Differential Receive Input (negative)	AC15
CSI3_RXP0	I	CSI Differential Receive Input (positive)	AF12
CSI3_RXP1	I	CSI Differential Receive Input (positive)	AE13
CSI3_RXP2	I	CSI Differential Receive Input (positive)	AD14
CSI3_RXP3	I	CSI Differential Receive Input (positive)	AC16

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.

5.3.4 DDRSS

5.3.4.1 MAIN Domain

Table 5-11. DDRSS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
DDR0_CAS_n (1)	O	DDRSS Column Address Strobe / LPDDR4 Chip Select 1B	M4
DDR0_RAS_n (1)	O	DDRSS Row Address Strobe / LPDDR4 Chip Select 0B	M3
DDR0_A0	O	DDRSS Address Bus	L4
DDR0_A1	O	DDRSS Address Bus	L6
DDR0_A2	O	DDRSS Address Bus	M5
DDR0_A3	O	DDRSS Address Bus	L3
DDR0_A4	O	DDRSS Address Bus	N2
DDR0_A5	O	DDRSS Address Bus	L2
DDR0_CAL0 (2)	A	IO Pad Calibration Resistor	R6

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Table 5-11. DDRSS0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
DDR0_CK0	O	DDRSS Clock	P1
DDR0_CK0_n	O	DDRSS Negative Clock	N1
DDR0_CKE0	O	DDRSS Clock Enable	P2
DDR0_CKE1	O	DDRSS Clock Enable	P6
DDR0_CS0_n (1)	O	DDRSS Chip Select 0 / LPDDR4 Chip Select 0A	P4
DDR0_CS1_n (1)	O	DDRSS Chip Select 1 / LPDDR4 Chip Select 1A	P3
DDR0_DM0	IO	DDRSS Data Mask	G2
DDR0_DM1	IO	DDRSS Data Mask	H6
DDR0_DM2	IO	DDRSS Data Mask	U4
DDR0_DM3	IO	DDRSS Data Mask	AA2
DDR0_DQ0	IO	DDRSS Data	D6
DDR0_DQ1	IO	DDRSS Data	D2
DDR0_DQ2	IO	DDRSS Data	F6
DDR0_DQ3	IO	DDRSS Data	D3
DDR0_DQ4	IO	DDRSS Data	G4
DDR0_DQ5	IO	DDRSS Data	E2
DDR0_DQ6	IO	DDRSS Data	G6
DDR0_DQ7	IO	DDRSS Data	F3
DDR0_DQ8	IO	DDRSS Data	H5
DDR0_DQ9	IO	DDRSS Data	H2
DDR0_DQ10	IO	DDRSS Data	K2
DDR0_DQ11	IO	DDRSS Data	L1
DDR0_DQ12	IO	DDRSS Data	J6
DDR0_DQ13	IO	DDRSS Data	J4
DDR0_DQ14	IO	DDRSS Data	J2
DDR0_DQ15	IO	DDRSS Data	H3
DDR0_DQ16	IO	DDRSS Data	V3
DDR0_DQ17	IO	DDRSS Data	R2
DDR0_DQ18	IO	DDRSS Data	R5
DDR0_DQ19	IO	DDRSS Data	T2
DDR0_DQ20	IO	DDRSS Data	R3
DDR0_DQ21	IO	DDRSS Data	U2
DDR0_DQ22	IO	DDRSS Data	U5
DDR0_DQ23	IO	DDRSS Data	V2
DDR0_DQ24	IO	DDRSS Data	Y2
DDR0_DQ25	IO	DDRSS Data	W4
DDR0_DQ26	IO	DDRSS Data	V5
DDR0_DQ27	IO	DDRSS Data	W2
DDR0_DQ28	IO	DDRSS Data	V6
DDR0_DQ29	IO	DDRSS Data	W3
DDR0_DQ30	IO	DDRSS Data	AA3
DDR0_DQ31	IO	DDRSS Data	AA5
DDR0_DQS0	IO	DDRSS Data Strobe	E1
DDR0_DQS0_n	IO	DDRSS Complimentary Data Strobe	F1

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Table 5-11. DDRSS0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
DDR0_DQS1	IO	DDRSS Data Strobe	H1
DDR0_DQS1_n	IO	DDRSS Complimentary Data Strobe	J1
DDR0_DQS2	IO	DDRSS Data Strobe	T1
DDR0_DQS2_n	IO	DDRSS Complimentary Data Strobe	U1
DDR0_DQS3	IO	DDRSS Data Strobe	W1
DDR0_DQS3_n	IO	DDRSS Complimentary Data Strobe	Y1
DDR0_RESET0_n	O	DDRSS Reset	U6

(1) DDRSS implements different signal functions on Column Address Strobe, Row Address Strobe, Chip Select 0, and Chip Select 1 when configured to operate with LPDDR4 memory devices. These signals function as Chip Select 1B, Chip Select 0B, Chip Select 0A, and Chip Select 1A respectively when DDRSS is configured to operate with LPDDR4 memory devices. For more information, refer to Section 8.2.1, *DDR Board Design and Layout Guidelines*.
(2) An external 240 Ω ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

5.3.5 DSI

5.3.5.1 MAIN Domain

Table 5-12. DSITX0 Signal Descriptions

SIGNAL NAME [1] ((2))	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
DSI0_TXCLKN	IO	DSI Differential Transmit Clock Ouput (negative)	AE16
DSI0_TXCLKP	IO	DSI Differential Transmit Clock Ouput (positive)	AE17
DSI0_TXRCALIB (1)	A	DSI pin connected to external resistor for on-chip resistor calibration	AA16
DSI0_TXN0	IO	DSI Differential Transmit Ouput (negative)	AD17
DSI0_TXN1	IO	DSI Differential Transmit Ouput (negative)	AF15
DSI0_TXN2	IO	DSI Differential Transmit Ouput (negative)	AG14
DSI0_TXN3	IO	DSI Differential Transmit Ouput (negative)	AC18
DSI0_TXP0	IO	DSI Differential Transmit Ouput (positive)	AD18
DSI0_TXP1	IO	DSI Differential Transmit Ouput (positive)	AF16
DSI0_TXP2	IO	DSI Differential Transmit Ouput (positive)	AG15
DSI0_TXP3	IO	DSI Differential Transmit Ouput (positive)	AC19

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.
(2) The functionality of these pins is controlled by DPHY_TX0_CTRL[1:0] LANE_FUNC_SEL. 0x0 = DSI PPI, 0x1 = CSI0 TX.

5.3.6 DSS

5.3.6.1 MAIN Domain

Table 5-13. DSS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
VOUT0_DE	O	Video Output Data Enable	AC27
VOUT0_EXTPCLKIN	I	Video Output External Pixel Clock Input	W26
VOUT0_HSYNC	O	Video Output Horizontal Sync	AB24
VOUT0_PCLK	O	Video Output Pixel Clock Output	AC26
VOUT0_VSYNC	O	Video Output Vertical Sync	AB23
VOUT0_DATA0	O	Video Output Data 0	W27
VOUT0_DATA1	O	Video Output Data 1	W25
VOUT0_DATA2	O	Video Output Data 2	W24
VOUT0_DATA3	O	Video Output Data 3	W23

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Table 5-13. DSS0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
VOUT0_DATA4	O	Video Output Data 4	W22
VOUT0_DATA5	O	Video Output Data 5	W21
VOUT0_DATA6	O	Video Output Data 6	Y26
VOUT0_DATA7	O	Video Output Data 7	Y27
VOUT0_DATA8	O	Video Output Data 8	AA24
VOUT0_DATA9	O	Video Output Data 9	AA27
VOUT0_DATA10	O	Video Output Data 10	AA25
VOUT0_DATA11	O	Video Output Data 11	AB25
VOUT0_DATA12	O	Video Output Data 12	AA23
VOUT0_DATA13	O	Video Output Data 13	AA22
VOUT0_DATA14	O	Video Output Data 14	AB26
VOUT0_DATA15	O	Video Output Data 15	AB27
VOUT0_DATA16	O	Video Output Data 16	U27
VOUT0_DATA17	O	Video Output Data 17	U26
VOUT0_DATA18	O	Video Output Data 18	V27
VOUT0_DATA19	O	Video Output Data 19	V25
VOUT0_DATA20	O	Video Output Data 20	V26
VOUT0_DATA21	O	Video Output Data 21	V24
VOUT0_DATA22	O	Video Output Data 22	V22
VOUT0_DATA23	O	Video Output Data 23	V23

5.3.7 ECAP

5.3.7.1 MAIN Domain

Table 5-14. ECAP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
ECAP0_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	A23, C20

Table 5-15. ECAP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
ECAP1_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	A25, B25, D23, F19, H20

Table 5-16. ECAP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
ECAP2_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	A26, B22, D25, F20, H23

5.3.8 Emulation and Debug

5.3.8.1 MAIN Domain

Table 5-17. Trace Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
TRC_CLK	O	Trace Clock	R22

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Table 5-17. Trace Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
TRC_CTL	O	Trace Control	R23
TRC_DATA0	O	Trace Data 0	R26
TRC_DATA1	O	Trace Data 1	T27
TRC_DATA2	O	Trace Data 2	T25
TRC_DATA3	O	Trace Data 3	T24
TRC_DATA4	O	Trace Data 4	T21
TRC_DATA5	O	Trace Data 5	T22
TRC_DATA6	O	Trace Data 6	T23
TRC_DATA7	O	Trace Data 7	N21
TRC_DATA8	O	Trace Data 8	N22
TRC_DATA9	O	Trace Data 9	N23
TRC_DATA10	O	Trace Data 10	P27
TRC_DATA11	O	Trace Data 11	P26
TRC_DATA12	O	Trace Data 12	V21
TRC_DATA13	O	Trace Data 13	N24
TRC_DATA14	O	Trace Data 14	N25
TRC_DATA15	O	Trace Data 15	R27
TRC_DATA16	O	Trace Data 16	P21
TRC_DATA17	O	Trace Data 17	P22
TRC_DATA18	O	Trace Data 18	P23
TRC_DATA19	O	Trace Data 19	V23
TRC_DATA20	O	Trace Data 20	V22
TRC_DATA21	O	Trace Data 21	V24
TRC_DATA22	O	Trace Data 22	V26
TRC_DATA23	O	Trace Data 23	V25

5.3.8.2 MCU Domain

Table 5-18. JTAG Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
EMU0	IO	Emulation Control 0	C9
EMU1	IO	Emulation Control 1	F9
TCK	I	JTAG Test Clock Input	A11
TDI	I	JTAG Test Data Input	E12
TDO	OZ	JTAG Test Data Output	F10
TMS	I	JTAG Test Mode Select Input	F11
TRSTn	I	JTAG Reset	B10

5.3.9 EPWM

5.3.9.1 MAIN Domain

Table 5-19. EPWM Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
EHRPWM_SOCA	O	EHRPWM Start of Conversion A	D23
EHRPWM_SOCB	O	EHRPWM Start of Conversion B	B22

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Table 5-19. EPWM Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
EHRPWM_TZn_IN0	I	EHRPWM Trip Zone Input 0 (active low)	E20, F27
EHRPWM_TZn_IN1	I	EHRPWM Trip Zone Input 1 (active low)	F26
EHRPWM_TZn_IN2	I	EHRPWM Trip Zone Input 2 (active low)	H21
EHRPWM_TZn_IN3	I	EHRPWM Trip Zone Input 3 (active low)	D22
EHRPWM_TZn_IN4	I	EHRPWM Trip Zone Input 4 (active low)	C22
EHRPWM_TZn_IN5	I	EHRPWM Trip Zone Input 5 (active low)	C20

Table 5-20. EPWM0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
EHRPWM0_A	IO	EHRPWM Output A	B20, C27, J27
EHRPWM0_B	IO	EHRPWM Output B	C20, F24, H27
EHRPWM0_SYNCI	I	Sync Input to EHRPWM module from an external pin	C24, H26
EHRPWM0_SYNCO	O	Sync Input to EHRPWM module from an external pin	A22, F27

Table 5-21. EPWM1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
EHRPWM1_A	IO	EHRPWM Output A	B25, D20, G27
EHRPWM1_B	IO	EHRPWM Output B	E19, F23, G26

Table 5-22. EPWM2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
EHRPWM2_A	IO	EHRPWM Output A	C24, F19, F26
EHRPWM2_B	IO	EHRPWM Output B	A22, F20, H21

5.3.10 EQEP

5.3.10.1 MAIN Domain

Table 5-23. EQEP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
EQEP0_A (1)	I	EQEP Quadrature Input A	A25
EQEP0_B (1)	I	EQEP Quadrature Input B	A26
EQEP0_I (1)	IO	EQEP Index	F23
EQEP0_S (1)	IO	EQEP Strobe	B25

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

Table 5-24. EQEP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
EQEP1_A (1)	I	EQEP Quadrature Input A	D25
EQEP1_B (1)	I	EQEP Quadrature Input B	C26
EQEP1_I (1)	IO	EQEP Index	F24

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Table 5-24. EQEP1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
EQEP1_S (1)	IO	EQEP Strobe	C27

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

Table 5-25. EQEP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
EQEP2_A (1)	I	EQEP Quadrature Input A	D23, Y26
EQEP2_B (1)	I	EQEP Quadrature Input B	B22, Y27
EQEP2_I (1)	IO	EQEP Index	D22, W22, W26
EQEP2_S (1)	IO	EQEP Strobe	C22, N25, W21

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

5.3.11 GPIO

5.3.11.1 MAIN Domain

Table 5-26. GPIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
GPIO0_0	IO	General Purpose Input/Output	L24
GPIO0_1	IO	General Purpose Input/Output	L23
GPIO0_2	IO	General Purpose Input/Output	L22
GPIO0_3	IO	General Purpose Input/Output	K27
GPIO0_4	IO	General Purpose Input/Output	L27
GPIO0_5	IO	General Purpose Input/Output	L26
GPIO0_6	IO	General Purpose Input/Output	L25
GPIO0_7	IO	General Purpose Input/Output	L21
GPIO0_8	IO	General Purpose Input/Output	M26
GPIO0_9	IO	General Purpose Input/Output	N27
GPIO0_10	IO	General Purpose Input/Output	M27
GPIO0_11	IO	General Purpose Input/Output	K26
GPIO0_12	IO	General Purpose Input/Output	K23
GPIO0_13 (1)	IO	General Purpose Input/Output	K22
GPIO0_14 (1)	IO	General Purpose Input/Output	J22
GPIO0_15	IO	General Purpose Input/Output	R22
GPIO0_16	IO	General Purpose Input/Output	R23
GPIO0_17	IO	General Purpose Input/Output	R26
GPIO0_18	IO	General Purpose Input/Output	T27
GPIO0_19	IO	General Purpose Input/Output	T25
GPIO0_20	IO	General Purpose Input/Output	T24
GPIO0_21	IO	General Purpose Input/Output	T21
GPIO0_22	IO	General Purpose Input/Output	T22
GPIO0_23	IO	General Purpose Input/Output	U27
GPIO0_24	IO	General Purpose Input/Output	U26
GPIO0_25	IO	General Purpose Input/Output	V27
GPIO0_26	IO	General Purpose Input/Output	V25
GPIO0_27	IO	General Purpose Input/Output	V26

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Table 5-26. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
GPIO0_28	IO	General Purpose Input/Output	V24
GPIO0_29	IO	General Purpose Input/Output	V22
GPIO0_30	IO	General Purpose Input/Output	V23
GPIO0_31	IO	General Purpose Input/Output	T23
GPIO0_32	IO	General Purpose Input/Output	N21
GPIO0_33	IO	General Purpose Input/Output	N22
GPIO0_34	IO	General Purpose Input/Output	N23
GPIO0_35	IO	General Purpose Input/Output	P27
GPIO0_36	IO	General Purpose Input/Output	P26
GPIO0_37	IO	General Purpose Input/Output	V21
GPIO0_38	IO	General Purpose Input/Output	W26
GPIO0_39	IO	General Purpose Input/Output	N24
GPIO0_40	IO	General Purpose Input/Output	N25
GPIO0_41	IO	General Purpose Input/Output	R27
GPIO0_42	IO	General Purpose Input/Output	P21
GPIO0_43 (1)	IO	General Purpose Input/Output	P22
GPIO0_44 (1)	IO	General Purpose Input/Output	P23
GPIO0_45	IO	General Purpose Input/Output	W27
GPIO0_46	IO	General Purpose Input/Output	W25
GPIO0_47	IO	General Purpose Input/Output	W24
GPIO0_48	IO	General Purpose Input/Output	W23
GPIO0_49	IO	General Purpose Input/Output	W22
GPIO0_50	IO	General Purpose Input/Output	W21
GPIO0_51	IO	General Purpose Input/Output	Y26
GPIO0_52	IO	General Purpose Input/Output	Y27
GPIO0_53	IO	General Purpose Input/Output	AA24
GPIO0_54	IO	General Purpose Input/Output	AA27
GPIO0_55	IO	General Purpose Input/Output	AA25
GPIO0_56	IO	General Purpose Input/Output	AB25
GPIO0_57	IO	General Purpose Input/Output	AA23
GPIO0_58	IO	General Purpose Input/Output	AA22
GPIO0_59	IO	General Purpose Input/Output	AB26
GPIO0_60	IO	General Purpose Input/Output	AB27
GPIO0_61	IO	General Purpose Input/Output	AB24
GPIO0_62	IO	General Purpose Input/Output	AC27
GPIO0_63	IO	General Purpose Input/Output	AB23
GPIO0_64	IO	General Purpose Input/Output	AC26
GPIO0_65 (1)	IO	General Purpose Input/Output	J27
GPIO0_66 (1)	IO	General Purpose Input/Output	H27
GPIO0_67 (1)	IO	General Purpose Input/Output	G27
GPIO0_68 (1)	IO	General Purpose Input/Output	G26
GPIO0_69 (1)	IO	General Purpose Input/Output	H26
GPIO0_70 (1)	IO	General Purpose Input/Output	F27
GPIO0_71 (1)	IO	General Purpose Input/Output	F26

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Table 5-26. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
GPIO0_72 (1)	IO	General Purpose Input/Output	H21
GPIO0_73	IO	General Purpose Input/Output	AF25
GPIO0_74	IO	General Purpose Input/Output	AG26
GPIO0_75	IO	General Purpose Input/Output	AF27
GPIO0_76	IO	General Purpose Input/Output	AE23
GPIO0_77	IO	General Purpose Input/Output	AG25
GPIO0_78	IO	General Purpose Input/Output	AF24
GPIO0_79	IO	General Purpose Input/Output	AD23
GPIO0_80	IO	General Purpose Input/Output	AE27
GPIO0_81	IO	General Purpose Input/Output	AC25
GPIO0_82	IO	General Purpose Input/Output	AD27
GPIO0_83	IO	General Purpose Input/Output	AE24
GPIO0_84	IO	General Purpose Input/Output	AE26
GPIO0_85	IO	General Purpose Input/Output	AD25
GPIO0_86	IO	General Purpose Input/Output	AC24

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

Table 5-27. GPIO1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
GPIO1_7	IO	General Purpose Input/Output	A25
GPIO1_8	IO	General Purpose Input/Output	A26
GPIO1_9	IO	General Purpose Input/Output	B25
GPIO1_10	IO	General Purpose Input/Output	F23
GPIO1_11	IO	General Purpose Input/Output	D25
GPIO1_12	IO	General Purpose Input/Output	C26
GPIO1_13	IO	General Purpose Input/Output	C27
GPIO1_14	IO	General Purpose Input/Output	F24
GPIO1_15	IO	General Purpose Input/Output	B20
GPIO1_16 (1)	IO	General Purpose Input/Output	C20
GPIO1_17	IO	General Purpose Input/Output	D20
GPIO1_18	IO	General Purpose Input/Output	E19
GPIO1_19	IO	General Purpose Input/Output	E20
GPIO1_20	IO	General Purpose Input/Output	F19
GPIO1_21	IO	General Purpose Input/Output	F20
GPIO1_22	IO	General Purpose Input/Output	E22
GPIO1_23	IO	General Purpose Input/Output	B21
GPIO1_24	IO	General Purpose Input/Output	D22
GPIO1_25	IO	General Purpose Input/Output	C22
GPIO1_26	IO	General Purpose Input/Output	D23
GPIO1_27	IO	General Purpose Input/Output	B22
GPIO1_28	IO	General Purpose Input/Output	C24
GPIO1_29	IO	General Purpose Input/Output	A22
GPIO1_30	IO	General Purpose Input/Output	A23
GPIO1_31 (1)	IOD	General Purpose Input/Output	B23

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Table 5-27. GPIO1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
GPIO1_42 (1)	IO	General Purpose Input/Output	H25
GPIO1_43 (1)	IO	General Purpose Input/Output	J23
GPIO1_44 (1)	IO	General Purpose Input/Output	H20
GPIO1_45 (1)	IO	General Purpose Input/Output	H23
GPIO1_46 (1)	IO	General Purpose Input/Output	H24
GPIO1_47 (1)	IO	General Purpose Input/Output	H22
GPIO1_48 (1)	I	General Purpose Input/Output	B24
GPIO1_49 (1)	I	General Purpose Input/Output	A24
GPIO1_50	IO	General Purpose Input/Output	E25
GPIO1_51	IO	General Purpose Input/Output	B27
GPIO1_52	IO	General Purpose Input/Output	AG24
GPIO1_53	IO	General Purpose Input/Output	AF23
GPIO1_54	IO	General Purpose Input/Output	AG23
GPIO1_55	IO	General Purpose Input/Output	AG22
GPIO1_56	IO	General Purpose Input/Output	AB21
GPIO1_57	IO	General Purpose Input/Output	AB20
GPIO1_58	IO	General Purpose Input/Output	AG21
GPIO1_59	IO	General Purpose Input/Output	AG20
GPIO1_60	IO	General Purpose Input/Output	AC21
GPIO1_61	IO	General Purpose Input/Output	AD21
GPIO1_62	IO	General Purpose Input/Output	AF18
GPIO1_63	IO	General Purpose Input/Output	AF19
GPIO1_64	IO	General Purpose Input/Output	AG18
GPIO1_65	IO	General Purpose Input/Output	AG17
GPIO1_66	IO	General Purpose Input/Output	AA20
GPIO1_67	IO	General Purpose Input/Output	AB19
GPIO1_68	IO	General Purpose Input/Output	AE20
GPIO1_69	IO	General Purpose Input/Output	AF21
GPIO1_70	IO	General Purpose Input/Output	AE19
GPIO1_71	IO	General Purpose Input/Output	AD20
GPIO1_72	IOD	General Purpose Input/Output	F25

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

5.3.11.2 MCU Domain

Table 5-28. MCU_GPIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCU_GPIO0_0 (1)	IO	General Purpose Input/Output	C12
MCU_GPIO0_1 (1)	IO	General Purpose Input/Output	A10
MCU_GPIO0_2	IO	General Purpose Input/Output	A9
MCU_GPIO0_3	IO	General Purpose Input/Output	B12
MCU_GPIO0_4	IO	General Purpose Input/Output	C11
MCU_GPIO0_5	IO	General Purpose Input/Output	B8
MCU_GPIO0_6	IO	General Purpose Input/Output	B4
MCU_GPIO0_7 (1)	IO	General Purpose Input/Output	B5

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Table 5-28. MCU_GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCU_GPIO0_8 (1)	IO	General Purpose Input/Output	C5
MCU_GPIO0_9	IO	General Purpose Input/Output	B3
MCU_GPIO0_10	IO	General Purpose Input/Output	C8
MCU_GPIO0_11 (1)	IO	General Purpose Input/Output	C4
MCU_GPIO0_12 (1)	IO	General Purpose Input/Output	C3
MCU_GPIO0_13	IO	General Purpose Input/Output	B2
MCU_GPIO0_14	IO	General Purpose Input/Output	D8
MCU_GPIO0_15 (1)	IO	General Purpose Input/Output	C1
MCU_GPIO0_16 (1)	IO	General Purpose Input/Output	B1
MCU_GPIO0_17	IOD	General Purpose Input/Output	B13
MCU_GPIO0_18	IOD	General Purpose Input/Output	E11
MCU_GPIO0_19	IOD	General Purpose Input/Output	B9
MCU_GPIO0_20	IOD	General Purpose Input/Output	D11
MCU_GPIO0_21	IO	General Purpose Input/Output	E13
MCU_GPIO0_22	IO	General Purpose Input/Output	A8
MCU_GPIO0_23	IO	General Purpose Input/Output	F12

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

5.3.12 GPMC

5.3.12.1 MAIN Domain

Table 5-29. GPMC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
GPMC0_ADVn_ALE	O	GPMC Address Valid (active low) or Address Latch Enable	N21
GPMC0_CLK	O	GPMC clock	T23
GPMC0_DIR	O	GPMC Data Bus Signal Direction Control	N25
GPMC0_FCLK_MUX	O	GPMC functional clock output	T23
GPMC0_OEn_REn	O	GPMC Output Enable (active low) or Read Enable (active low)	N22
GPMC0_WEn	O	GPMC Write Enable (active low)	N23
GPMC0_WPn	O	GPMC Flash Write Protect (active low)	N24
GPMC0_A0	OZ	GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories	W27
GPMC0_A1	OZ	GPMC address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode	W25
GPMC0_A2	OZ	GPMC address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode	W24
GPMC0_A3	OZ	GPMC address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode	W23
GPMC0_A4	OZ	GPMC address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode	W22
GPMC0_A5	OZ	GPMC address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode	W21
GPMC0_A6	OZ	GPMC address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode	Y26
GPMC0_A7	OZ	GPMC address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode	Y27

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Table 5-29. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
GPMC0_A8	OZ	GPMC address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode	AA24
GPMC0_A9	OZ	GPMC address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode	AA27
GPMC0_A10	OZ	GPMC address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode	AA25
GPMC0_A11	OZ	GPMC address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AB25
GPMC0_A12	OZ	GPMC address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA23
GPMC0_A13	OZ	GPMC address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA22
GPMC0_A14	OZ	GPMC address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AB26
GPMC0_A15	OZ	GPMC address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AB27
GPMC0_A16	OZ	GPMC address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AB24
GPMC0_A17	OZ	GPMC address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AC27
GPMC0_A18	OZ	GPMC address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AB23
GPMC0_A19	OZ	GPMC address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AC26
GPMC0_A20	OZ	GPMC address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	P23
GPMC0_A21	OZ	GPMC address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	W26
GPMC0_A22	OZ	GPMC address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	N24
GPMC0_AD0	IO	GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode	R22
GPMC0_AD1	IO	GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode	R23
GPMC0_AD2	IO	GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	R26
GPMC0_AD3	IO	GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	T27
GPMC0_AD4	IO	GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	T25
GPMC0_AD5	IO	GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	T24
GPMC0_AD6	IO	GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	T21
GPMC0_AD7	IO	GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	T22

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Table 5-29. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
GPMC0_AD8	IO	GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	U27
GPMC0_AD9	IO	GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	U26
GPMC0_AD10	IO	GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode	V27
GPMC0_AD11	IO	GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode	V25
GPMC0_AD12	IO	GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode	V26
GPMC0_AD13	IO	GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode	V24
GPMC0_AD14	IO	GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode	V22
GPMC0_AD15	IO	GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode	V23
GPMC0_BE0n_CLE	O	GPMC Lower-Byte Enable (active low) or Command Latch Enable	P27
GPMC0_BE1n	O	GPMC Upper-Byte Enable (active low)	P26
GPMC0_CSn0	O	GPMC Chip Select 0 (active low)	R27
GPMC0_CSn1	O	GPMC Chip Select 1 (active low)	P21
GPMC0_CSn2	O	GPMC Chip Select 2 (active low)	P22
GPMC0_CSn3	O	GPMC Chip Select 3 (active low)	P23
GPMC0_WAIT0	I	GPMC External Indication of Wait	V21
GPMC0_WAIT1	I	GPMC External Indication of Wait	W26

5.3.13 I2C

5.3.13.1 MAIN Domain

Table 5-30. I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
I2C0_SCL	IOD	I2C Clock	D23
I2C0_SDA	IOD	I2C Data	B22

Table 5-31. I2C1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
I2C1_SCL	IOD	I2C Clock	C24
I2C1_SDA	IOD	I2C Data	A22

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Table 5-32. I2C2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
I2C2_SCL	IOD	I2C Clock	G26, P22
I2C2_SDA	IOD	I2C Data	G27, H27, P23

Table 5-33. I2C3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
I2C3_SCL	IOD	I2C Clock	E22, H26
I2C3_SDA	IOD	I2C Data	B21, F27

Table 5-34. I2C4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
I2C4_SCL	IOD	I2C Clock	D22, R27
I2C4_SDA	IOD	I2C Data	C22, P21

5.3.13.2 MCU Domain

Table 5-35. MCU_I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCU_I2C0_SCL	IOD	I2C Clock	B13
MCU_I2C0_SDA	IOD	I2C Data	E11

5.3.13.3 WKUP Domain

Table 5-36. WKUP_I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
WKUP_I2C0_SCL	IOD	I2C Clock	B9
WKUP_I2C0_SDA	IOD	I2C Data	D11

5.3.14 MCAN

5.3.14.1 MAIN Domain

Table 5-37. MCAN0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCAN0_RX	I	MCAN Receive Data	C22
MCAN0_TX	O	MCAN Transmit Data	D22

Table 5-38. MCAN1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCAN1_RX	I	MCAN Receive Data	A24, J23, P23
MCAN1_TX	O	MCAN Transmit Data	B24, H25, P22

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5.3.14.2 MCU Domain

Table 5-39. MCU_MCAN0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCU_MCAN0_RX	I	MCAN Receive Data	D8
MCU_MCAN0_TX	O	MCAN Transmit Data	B2

Table 5-40. MCU_MCAN1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCU_MCAN1_RX	I	MCAN Receive Data	B1
MCU_MCAN1_TX	O	MCAN Transmit Data	C1

5.3.15 MCASP

5.3.15.1 MAIN Domain

Table 5-41. MCASP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCASP0_ACLKR	IO	MCASP Receive Bit Clock	F24
MCASP0_ACLKX	IO	MCASP Transmit Bit Clock	D25
MCASP0_AFSR	IO	MCASP Receive Frame Sync	C27
MCASP0_AFSX	IO	MCASP Transmit Frame Sync	C26
MCASP0_AXR0	IO	MCASP Serial Data (Input/Output)	F23
MCASP0_AXR1	IO	MCASP Serial Data (Input/Output)	B25
MCASP0_AXR2	IO	MCASP Serial Data (Input/Output)	A26
MCASP0_AXR3	IO	MCASP Serial Data (Input/Output)	A25

Table 5-42. MCASP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCASP1_ACLKR	IO	MCASP Receive Bit Clock	H26, J22, P23
MCASP1_ACLKX	IO	MCASP Transmit Bit Clock	F26, N27, P27
MCASP1_AFSR	IO	MCASP Receive Frame Sync	F27, K22, P22
MCASP1_AFSX	IO	MCASP Transmit Frame Sync	H21, M27, V21
MCASP1_AXR0	IO	MCASP Serial Data (Input/Output)	G26, M26, N23
MCASP1_AXR1	IO	MCASP Serial Data (Input/Output)	G27, L21, N22
MCASP1_AXR2	IO	MCASP Serial Data (Input/Output)	H27, K22, N21
MCASP1_AXR3	IO	MCASP Serial Data (Input/Output)	J22, J27, T23
MCASP1_AXR4	IO	MCASP Serial Data (Input/Output)	F27, P22
MCASP1_AXR5	IO	MCASP Serial Data (Input/Output)	H26, P23

Table 5-43. MCASP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCASP2_ACLKR	IO	MCASP Receive Bit Clock	V23
MCASP2_ACLKX	IO	MCASP Transmit Bit Clock	B21, V24
MCASP2_AFSR	IO	MCASP Receive Frame Sync	V22
MCASP2_AFSX	IO	MCASP Transmit Frame Sync	E22, V26

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Table 5-43. MCASP2 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCASP2_AXR0	IO	MCASP Serial Data (Input/Output)	D22, U27
MCASP2_AXR1	IO	MCASP Serial Data (Input/Output)	C22, U26
MCASP2_AXR2	IO	MCASP Serial Data (Input/Output)	V27
MCASP2_AXR3	IO	MCASP Serial Data (Input/Output)	V25
MCASP2_AXR4	IO	MCASP Serial Data (Input/Output)	R22, V22
MCASP2_AXR5	IO	MCASP Serial Data (Input/Output)	R23, V23
MCASP2_AXR6	IO	MCASP Serial Data (Input/Output)	R26
MCASP2_AXR7	IO	MCASP Serial Data (Input/Output)	T27
MCASP2_AXR8	IO	MCASP Serial Data (Input/Output)	T25
MCASP2_AXR9	IO	MCASP Serial Data (Input/Output)	T24
MCASP2_AXR10	IO	MCASP Serial Data (Input/Output)	T21
MCASP2_AXR11	IO	MCASP Serial Data (Input/Output)	T22
MCASP2_AXR12	IO	MCASP Serial Data (Input/Output)	P26
MCASP2_AXR13	IO	MCASP Serial Data (Input/Output)	N25
MCASP2_AXR14	IO	MCASP Serial Data (Input/Output)	R27
MCASP2_AXR15	IO	MCASP Serial Data (Input/Output)	P21

Table 5-44. MCASP3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCASP3_ACLKR	IO	MCASP Receive Bit Clock	Y26
MCASP3_ACLKX	IO	MCASP Transmit Bit Clock	W27
MCASP3_AFSR	IO	MCASP Receive Frame Sync	Y27
MCASP3_AFSX	IO	MCASP Transmit Frame Sync	W25
MCASP3_AXR0	IO	MCASP Serial Data (Input/Output)	W24
MCASP3_AXR1	IO	MCASP Serial Data (Input/Output)	W23
MCASP3_AXR2	IO	MCASP Serial Data (Input/Output)	W22
MCASP3_AXR3	IO	MCASP Serial Data (Input/Output)	W21
MCASP3_AXR4	IO	MCASP Serial Data (Input/Output)	AA24
MCASP3_AXR5	IO	MCASP Serial Data (Input/Output)	AA27
MCASP3_AXR6	IO	MCASP Serial Data (Input/Output)	Y26
MCASP3_AXR7	IO	MCASP Serial Data (Input/Output)	Y27
MCASP3_AXR8	IO	MCASP Serial Data (Input/Output)	J27
MCASP3_AXR9	IO	MCASP Serial Data (Input/Output)	H27

Table 5-45. MCASP4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCASP4_ACLKR	IO	MCASP Receive Bit Clock	AA25
MCASP4_ACLKX	IO	MCASP Transmit Bit Clock	AB23
MCASP4_AFSR	IO	MCASP Receive Frame Sync	AB25
MCASP4_AFSX	IO	MCASP Transmit Frame Sync	AC26
MCASP4_AXR0	IO	MCASP Serial Data (Input/Output)	AA23
MCASP4_AXR1	IO	MCASP Serial Data (Input/Output)	AA22
MCASP4_AXR2	IO	MCASP Serial Data (Input/Output)	AB26

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Table 5-45. MCASP4 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCASP4_AXR3	IO	MCASP Serial Data (Input/Output)	AB27
MCASP4_AXR4	IO	MCASP Serial Data (Input/Output)	AB24
MCASP4_AXR5	IO	MCASP Serial Data (Input/Output)	AC27
MCASP4_AXR6	IO	MCASP Serial Data (Input/Output)	AA25
MCASP4_AXR7	IO	MCASP Serial Data (Input/Output)	AB25
MCASP4_AXR8	IO	MCASP Serial Data (Input/Output)	G27
MCASP4_AXR9	IO	MCASP Serial Data (Input/Output)	G26

5.3.16 MCSPI

5.3.16.1 MAIN Domain

Table 5-46. MCSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
SPI0_CLK	IO	SPI Clock	D20
SPI0_CS0	IO	SPI Chip Select 0	B20
SPI0_CS1	IO	SPI Chip Select 1	C20
SPI0_CS2	IO	SPI Chip Select 2	E22
SPI0_CS3	IO	SPI Chip Select 3	B21
SPI0_D0	IO	SPI Data 0	E19
SPI0_D1	IO	SPI Data 1	E20

Table 5-47. MCSPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
SPI1_CLK	IO	SPI Clock	H22, M26
SPI1_CS0	IO	SPI Chip Select 0	H24, L21
SPI1_CS1	IO	SPI Chip Select 1	A24, K22
SPI1_CS2	IO	SPI Chip Select 2	H20
SPI1_CS3	I	SPI Chip Select 3	B24
SPI1_D0	IO	SPI Data 0	H25, N27
SPI1_D1	IO	SPI Data 1	J23, M27

Table 5-48. MCSPI2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
SPI2_CLK	IO	SPI Clock	A22, B24, F24
SPI2_CS0	IO	SPI Chip Select 0	C27, D23, H22
SPI2_CS1	IO	SPI Chip Select 1	C24, D25, H25
SPI2_CS2	IO	SPI Chip Select 2	B22, B25, H24
SPI2_CS3	IO	SPI Chip Select 3	A23, C26, J23
SPI2_D0	IO	SPI Data 0	A25, F19, H20
SPI2_D1	IO	SPI Data 1	A26, F20, H23

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5.3.16.2 MCU Domain

Table 5-49. MCU_MCSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCU_SPI0_CLK	IO	SPI Clock	A9
MCU_SPI0_CS0	IO	SPI Chip Select 0	C12
MCU_SPI0_CS1	IO	SPI Chip Select 1	A10
MCU_SPI0_CS2	IO	SPI Chip Select 2	B1, B3
MCU_SPI0_CS3	IO	SPI Chip Select 3	B2
MCU_SPI0_D0	IO	SPI Data 0	B12
MCU_SPI0_D1	IO	SPI Data 1	C11

Table 5-50. MCU_MCSPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCU_SPI1_CLK	IO	SPI Clock	B1, C3
MCU_SPI1_CS0	IO	SPI Chip Select 0	C4
MCU_SPI1_CS1	IO	SPI Chip Select 2	C1
MCU_SPI1_CS2	IO	SPI Chip Select 2	B1, C8
MCU_SPI1_CS3	IO	SPI Chip Select 3	D8
MCU_SPI1_D0	IO	SPI Data 0	B5
MCU_SPI1_D1	IO	SPI Data 1	C5

5.3.17 MDIO

5.3.17.1 MAIN Domain

Table 5-51. MDIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MDIO0_MDC	O	MDIO Clock	AC24
MDIO0_MDIO	IO	MDIO Data	AD25

5.3.18 MMC

5.3.18.1 MAIN Domain

Table 5-52. MMC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MMC0_CALPAD (1)	A	MMC/SD/SDIO Calibration Resistor	AC1
MMC0_CLK	IO	MMC/SD/SDIO Clock	AE1
MMC0_CMD	IO	MMC/SD/SDIO Command	AE2
MMC0_DS	IO	MMC Data Strobe	AD1
MMC0_DAT0	IO	MMC/SD/SDIO Data	AD3
MMC0_DAT1	IO	MMC/SD/SDIO Data	AD2
MMC0_DAT2	IO	MMC/SD/SDIO Data	AB4
MMC0_DAT3	IO	MMC/SD/SDIO Data	AC2
MMC0_DAT4	IO	MMC/SD/SDIO Data	AC3
MMC0_DAT5	IO	MMC/SD/SDIO Data	AB3
MMC0_DAT6	IO	MMC/SD/SDIO Data	AF1

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Table 5-52. MMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MMC0_DAT7	IO	MMC/SD/SDIO Data	AB2

(1) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

Table 5-53. MMC1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MMC1_CLK	IO	MMC/SD/SDIO Clock	H24
MMC1_CMD	IO	MMC/SD/SDIO Command	H22
MMC1_SDCD	I	SD Card Detect	B24
MMC1_SDWP	I	SD Write Protect	A24
MMC1_DAT0	IO	MMC/SD/SDIO Data	H23
MMC1_DAT1	IO	MMC/SD/SDIO Data	H20
MMC1_DAT2	IO	MMC/SD/SDIO Data	J23
MMC1_DAT3	IO	MMC/SD/SDIO Data	H25

Table 5-54. MMC2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MMC2_CLK	IO	MMC/SD/SDIO Clock	H26
MMC2_CMD	IO	MMC/SD/SDIO Command	F27
MMC2_SDCD	I	SD Card Detect	C24, E22, F26
MMC2_SDWP	I	SD Write Protect	A22, B21, H21
MMC2_DAT0	IO	MMC/SD/SDIO Data	G26
MMC2_DAT1	IO	MMC/SD/SDIO Data	G27
MMC2_DAT2	IO	MMC/SD/SDIO Data	H27
MMC2_DAT3	IO	MMC/SD/SDIO Data	J27

5.3.19 OLDI

5.3.19.1 MAIN Domain

Table 5-55. OLDI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
OLDI0_A0N	IO	OLDI Differential Data (negative)	AF23
OLDI0_A0P	IO	OLDI Differential Data (positive)	AG24
OLDI0_A1N	IO	OLDI Differential Data (negative)	AG22
OLDI0_A1P	IO	OLDI Differential Data (positive)	AG23
OLDI0_A2N	IO	OLDI Differential Data (negative)	AB20
OLDI0_A2P	IO	OLDI Differential Data (positive)	AB21
OLDI0_A3N	IO	OLDI Differential Data (negative)	AG20
OLDI0_A3P	IO	OLDI Differential Data (positive)	AG21
OLDI0_A4N	IO	OLDI Differential Data (negative)	AD21
OLDI0_A4P	IO	OLDI Differential Data (positive)	AC21
OLDI0_A5N	IO	OLDI Differential Data (negative)	AF19
OLDI0_A5P	IO	OLDI Differential Data (positive)	AF18
OLDI0_A6N	IO	OLDI Differential Data (negative)	AG17
OLDI0_A6P	IO	OLDI Differential Data (positive)	AG18

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Table 5-55. OLDI0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
OLDI0_A7N	IO	OLDI Differential Data (negative)	AB19
OLDI0_A7P	IO	OLDI Differential Data (positive)	AA20
OLDI0_CLK0N	IO	OLDI Differential Clock (negative)	AF21
OLDI0_CLK0P	IO	OLDI Differential Clock (positive)	AE20
OLDI0_CLK1N	IO	OLDI Differential Clock (negative)	AD20
OLDI0_CLK1P	IO	OLDI Differential Clock (positive)	AE19

5.3.20 OSPI

5.3.20.1 MAIN Domain

Table 5-56. OSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
OSPI0_CLK	O	OSPI Clock	L24
OSPI0_DQS	I	OSPI Data Strobe (DQS) or Loopback Clock Input	L22
OSPI0_ECC_FAIL	I	OSPI ECC Status	J22
OSPI0_LBCLKO	IO	OSPI Loopback Clock Output	L23
OSPI0_CSn0	O	OSPI Chip Select 0 (active low)	K26
OSPI0_CSn1	O	OSPI Chip Select 1 (active low)	K23
OSPI0_CSn2	O	OSPI Chip Select 2 (active low)	K22
OSPI0_CSn3	O	OSPI Chip Select 3 (active low)	J22
OSPI0_D0	IO	OSPI Data 0	K27
OSPI0_D1	IO	OSPI Data 1	L27
OSPI0_D2	IO	OSPI Data 2	L26
OSPI0_D3	IO	OSPI Data 3	L25
OSPI0_D4	IO	OSPI Data 4	L21
OSPI0_D5	IO	OSPI Data 5	M26
OSPI0_D6	IO	OSPI Data 6	N27
OSPI0_D7	IO	OSPI Data 7	M27
OSPI0_RESET_OUT0	O	OSPI Reset	J22
OSPI0_RESET_OUT1	O	OSPI Reset	K22

5.3.21 Power Supply

Table 5-57. Power Supply Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
CAP_VDDS0 (1)	CAP	External capacitor connection for IO group 0	H17
CAP_VDDS1 (1)	CAP	External capacitor connection for IO group 1	L19
CAP_VDDS2 (1)	CAP	External capacitor connection for IO group 2	U20
CAP_VDDS3 (1)	CAP	External capacitor connection for IO group 3	N20
CAP_VDDS5 (1)	CAP	External capacitor connection for IO group 5	G19
CAP_VDDS6 (1)	CAP	External capacitor connection for IO group 6	J20
CAP_VDDS_CANUART (1)	CAP	External capacitor connection for IO CANUART	H8
CAP_VDDS_MCU (1)	CAP	External capacitor connection for IO MCU	J10
VDDA_0P85_SERDES	PWR	SERDES analog supply	H12, H13
VDDA_0P85_SERDES_C	PWR	SERDES clock analog supply	J13

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Table 5-57. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
VDDA_0P85_DLL_MMC0	PWR	MMC0 DLL analog supply	W9
VDDA_1P8_CSI_DSI	PWR	CSIRX and DSITX 1.8 V analog supply	W13, W16, Y13
VDDA_1P8_SERDES	PWR	SERDES 1.8 V analog supply	G13
VDDA_1P8_OLDI0	PWR	OLDI analog supply	W18, Y19
VDDA_1P8_USB0	PWR	USB 1.8 V analog supply	Y12
VDDA_1P8_USB1	PWR	USB 1.8 V analog supply	H16
VDDA_3P3_USB0	PWR	USB 3.3 V analog supply	Y11
VDDA_3P3_USB1	PWR	USB 3.3 V analog supply	G15
VDDA_CORE_CSI_DSI	PWR	CSIRX and DSITX Core supply	W15, Y15
VDDA_CORE_CSI_DSI_CLK	PWR	CSIRX and DSITX clock Core supply	Y16
VDDA_CORE_USB0	PWR	USB Core Supply	W11
VDDA_CORE_USB1	PWR	USB Core Supply	H15
VDDA_DDR_PLL0	PWR	DDR Deskew PLL analog supply	P9
VDDA_MCU	PWR	POR and MCU PLL analog supply	G11, H11
VDDA_PLL0	PWR	MAIN PLL analog supply	L15
VDDA_PLL1	PWR	PER0 PLL and PER1 PLL analog supply	K10
VDDA_PLL2	PWR	VIDEO PLL analog supply	M12
VDDA_PLL3	PWR	C7x PLL and DSS PLL analog supply	R11
VDDA_PLL4	PWR	ARM0 PLL and SMS PLL analog supply	V18
VDDA_PLL5	PWR	DDR PLL analog supply	P16
VDDA_TEMP0	PWR	TEMP0 analog supply	Y17
VDDA_TEMP1	PWR	TEMP1 analog supply	T11
VDDA_TEMP2	PWR	TEMP2 analog supply	L9
VDDR_CORE	PWR	Core Supply	M13, M19, N13, N19, U10, U17, V10, V17
VDDSHV0	PWR	IO supply for IO group 0	G18, H18
VDDSHV1	PWR	IO supply for IO group 1	K20, L20
VDDSHV2	PWR	IO supply for IO group 2	T19, T20
VDDSHV3	PWR	IO supply for IO group 3	M20, P20, R20
VDDSHV5	PWR	IO supply for IO group 5	H19
VDDSHV6	PWR	IO supply for IO group 6	J21
VDDSHV_CANUART	PWR	IO supply for IO CANUART	H9
VDDSHV_MCU	PWR	IO supply for IO MCU	H10
VDDS_DDR	PWR	DDR PHY IO supply	AB1, D1, L7, L8, N7, N8, T7, T8
VDDS_DDR_C	PWR	DDR clock IO supply	P8
VDDS_MMC0	PWR	MMC0 PHY IO supply	Y9
VDDS_OSC0	PWR	MCU_OSC0 supply	K8
VDD_CANUART	PWR	CANUART Core Supply	J8

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Table 5-57. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
VDD_CORE	PWR	Core supply	J11, J14, J16, J18, K11, K12, K14, K16, K18, K9, L12, L17, M10, M15, M17, M9, N10, N11, N14, N16, N18, P11, P12, P14, P18, R12, R13, R15, R17, R9, T13, T15, T17, T9, U12, U14, U16, U8, V12, V14, V16, V19, V8, W19, Y20, Y21
VDD_MMC0	PWR	MMC0 PHY core supply	W10
VPP	PWR	eFuse ROM programming supply	G9
VSS	GND	Ground	A1, A18, A21, A27, A4, A7, AA1, AA18, AA21, AA26, AA4, AD26, AG1, AG27, C2, C23, D26, E6, F15, F16, F17, F2, F21, G1, G10, G12, G14, G16, G17, G20, G3, G5, G8, H14, H4, H7, J12, J15, J17, J19, J26, J3, J5, J9, K1, K13, K15, K17, K19, L10, L11, L13, L14, L16, L18, M1, M11, M14, M16, M18, M7, M8, N12, N15, N17, N26, N9, P10, P13, P15, P17, P19, P5, P7, R1, R10, R14, R16, R18, R19, R4, R7, R8, T10, T12, T14, T16, T18, T26, U11, U13, U15, U18, U19, U3, U7, U9, V1, V11, V13, V15, V20, V4, V7, V9, W12, W14, W17, W20, W5, W8, Y10, Y14, Y18, Y7, Y8

(1) This pin must always be connected via a 1-µF capacitor to VSS.

5.3.22 Reserved

Table 5-58. Reserved Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
RSVD0	N/A	Reserved, must be left unconnected	E9
RSVD1	N/A	Reserved, must be left unconnected	AA19
RSVD2	N/A	Reserved, must be left unconnected	AB7
RSVD3	N/A	Reserved, must be left unconnected	AC5
RSVD4	N/A	Reserved, must be left unconnected	AB10
RSVD5	N/A	Reserved, must be left unconnected	AA12
RSVD6	N/A	Reserved, must be left unconnected	AB12
RSVD7	N/A	Reserved, must be left unconnected	AB13

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Table 5-58. Reserved Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
RSVD8	N/A	Reserved, must be left unconnected	AA15
RSVD9	N/A	Reserved, must be left unconnected	AA14
RSVD10	N/A	Reserved, must be left unconnected	L5
RSVD11	N/A	Reserved, must be left unconnected	M6
RSVD12	N/A	Reserved, must be left unconnected	AB16
RSVD13	N/A	Reserved, must be left unconnected	AB18
RSVD14	N/A	Reserved, must be left unconnected	C6
RSVD15	N/A	Reserved, must be left unconnected	F8
RSVD16	N/A	Reserved, must be left unconnected	B6
RSVD17	N/A	Reserved, must be left unconnected	C17
RSVD18	N/A	Reserved, must be left unconnected	D16
RSVD19	N/A	Reserved, must be left unconnected	D14
RSVD20	N/A	Reserved, must be left unconnected	D13
RSVD21	N/A	Reserved, must be left unconnected	M2

5.3.23 SERDES

5.3.23.1 MAIN Domain

Table 5-59. PCIE0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
PCIE0_CLKREQn	IOD	PCIE Clock Request Signal	F25

Table 5-60. SERDES0 Signal Descriptions

SIGNAL NAME [1] ([2])	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
SERDES0_REXT (1)	A	SERDES PHY External Calibration Resistor	E15
SERDES0_REFCLK0N	IO	SERDES PHY Reference Clock Input/Output (negative)	A17
SERDES0_REFCLK0P	IO	SERDES PHY Reference Clock Input/Output (positive)	A16
SERDES0_RX0_N	I	SERDES PHY Differential Receive Data (negative)	A20
SERDES0_RX0_P	I	SERDES PHY Differential Receive Data (positive)	A19
SERDES0_TX0_N	O	SERDES PHY Differential Transmit Data (negative)	B19
SERDES0_TX0_P	O	SERDES PHY Differential Transmit Data (positive)	B18

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.
(2) The functionality of these pins is controlled by SERDES0_LN0_CTRL.

Table 5-61. SERDES1 Signal Descriptions

SIGNAL NAME [1] ([2])	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
SERDES1_REXT (1)	A	SERDES PHY External Calibration Resistor	F14
SERDES1_REFCLK0N	IO	SERDES PHY Reference Clock Input/Output (negative)	B15
SERDES1_REFCLK0P	IO	SERDES PHY Reference Clock Input/Output (positive)	B16
SERDES1_RX0_N	I	SERDES PHY Differential Receive Data (negative)	C14
SERDES1_RX0_P	I	SERDES PHY Differential Receive Data (positive)	C15
SERDES1_TX0_N	O	SERDES PHY Differential Transmit Data (negative)	A13
SERDES1_TX0_P	O	SERDES PHY Differential Transmit Data (positive)	A14

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

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(2) The functionality of these pins is controlled by SERDES1_LN0_CTRL.

5.3.24 System and Miscellaneous

5.3.24.1 Boot Mode Configuration

5.3.24.1.1 MAIN Domain

Table 5-62. Sysboot Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
BOOTMODE00	I	Bootmode pin 0	R22
BOOTMODE01	I	Bootmode pin 1	R23
BOOTMODE02	I	Bootmode pin 2	R26
BOOTMODE03	I	Bootmode pin 3	T27
BOOTMODE04	I	Bootmode pin 4	T25
BOOTMODE05	I	Bootmode pin 5	T24
BOOTMODE06	I	Bootmode pin 6	T21
BOOTMODE07	I	Bootmode pin 7	T22
BOOTMODE08	I	Bootmode pin 8	U27
BOOTMODE09	I	Bootmode pin 9	U26
BOOTMODE10	I	Bootmode pin 10	V27
BOOTMODE11	I	Bootmode pin 11	V25
BOOTMODE12	I	Bootmode pin 12	V26
BOOTMODE13	I	Bootmode pin 13	V24
BOOTMODE14	I	Bootmode pin 14	V22
BOOTMODE15	I	Bootmode pin 15	V23

5.3.24.2 Clock

5.3.24.2.1 MCU Domain

Table 5-63. MCU Clock Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCU_OSC0_XI	I	High frequency oscillator input	A5
MCU_OSC0_XO	O	High frequency oscillator output	A6

5.3.24.2.2 WKUP Domain

Table 5-64. WKUP Clock Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
WKUP_LFOSC0_XI	I	Low frequency (32.768 KHz) oscillator input	A3
WKUP_LFOSC0_XO	O	Low frequency (32.768 KHz) oscillator output	A2

5.3.24.3 System

5.3.24.3.1 MAIN Domain

Table 5-65. System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
AUDIO_EXT_REFCLK0	IO	External clock input to McASP or output from McASP	E22, F23, W23
AUDIO_EXT_REFCLK1	IO	External clock input to McASP or output from McASP	B21, C26, N24
AUDIO_EXT_REFCLK2	IO	External clock input to McASP or output from McASP	W26

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Table 5-65. System Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
CLKOUT0	O	RMII Clock Output (50 MHz). This pin is used for clock source to the external RMII PHY and must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.	A23, AA22, AF24
EXTINTn	I	External Interrupt	B23
EXT_REFCLK1	I	External clock input to Main Domain	A23
MAIN_ERRORn	IO	Error signal output from MAIN Domain ESM	B25, C20, N25
OBSCLK0	O	Main Domain Observation clock output for test and debug purposes only	V27
OBSCLK1	O	Main Domain Observation clock output for test and debug purposes only	D23
PORz_OUT	O	Main Domain POR status output	D27
RESETSTATz	O	Main Domain warm reset status output	E27
RESET_REQz	I	Main Domain external warm reset request input	E26
SYNC0_OUT	O	CPTS Time Stamp Generator Bit 0 Output from Time Sync Router	D23
SYNC1_OUT	O	CPTS Time Stamp Generator Bit 1 Output from Time Sync Router	A23
SYNC2_OUT	O	CPTS Time Stamp Generator Bit 2 Output from Time Sync Router	D22
SYNC3_OUT	O	CPTS Time Stamp Generator Bit 3 Output from Time Sync Router	C22
SYSCLKOUT0	O	Main Domain system clock output (divided by 4) for test and debug purposes only	A23

5.3.24.3.2 MCU Domain

Table 5-66. MCU System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCU_ERRORn	IO	Error signal output from MCU Domain ESM	B7
MCU_EXT_REFCLK0	I	External input to MCU Domain	A10, C1
MCU_OBSCLK0	O	MCU Domain Observation clock output for test and debug purposes only	A10
MCU_PORz	I	MCU and Main Domain cold reset	E8
MCU_RESETSTATz	O	MCU Domain warm reset status output	E13
MCU_RESETz	I	MCU and Main Domain warm reset	D10
MCU_SYSCLKOUT0	O	MCU Domain system clock output (divided by 4) for test and debug purposes only	A10

5.3.24.3.3 WKUP Domain

Table 5-67. WKUP System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
PMIC_LPM_EN0	O	Dual-function PMIC control output, Low Power Mode (active low) or PMIC Enable (active high)	A8
WKUP_CLKOUT0	O	WKUP Domain CLKOUT0 output	F12

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5.3.24.4 VMON

Table 5-68. VMON Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
VMON_1P8_SOC	A	Voltage monitor input for 1.8 V SoC power supply	J7
VMON_3P3_SOC	A	Voltage monitor input for 3.3 V SoC power supply	K7
VMON_ER_VSYS	A	Voltage monitor input, fixed 0.45 V (+/-3%) threshold. Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply.	G7

5.3.25 TIMER

5.3.25.1 MAIN Domain

Table 5-69. TIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	C24, H25
TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	A22, J23
TIMER_IO2	IO	Timer Inputs and Outputs (not tied to single timer instance)	D22, H20
TIMER_IO3	IO	Timer Inputs and Outputs (not tied to single timer instance)	C22, H23
TIMER_IO4	IO	Timer Inputs and Outputs (not tied to single timer instance)	A23, H24
TIMER_IO5	IO	Timer Inputs and Outputs (not tied to single timer instance)	B22, H22
TIMER_IO6	I	Timer Inputs and Outputs (not tied to single timer instance)	B24, E22
TIMER_IO7	IO	Timer Inputs and Outputs (not tied to single timer instance)	A24, B21

5.3.25.2 MCU Domain

Table 5-70. MCU_TIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCU_TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	B5, D8
MCU_TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	A10, C5
MCU_TIMER_IO2	IO	Timer Inputs and Outputs (not tied to single timer instance)	C1
MCU_TIMER_IO3	IO	Timer Inputs and Outputs (not tied to single timer instance)	B1

5.3.25.3 WKUP Domain

Table 5-71. WKUP_TIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
WKUP_TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	B2, C4

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Table 5-71. WKUP_TIMER Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
WKUP_TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	C12, C3

5.3.26 UART

5.3.26.1 MAIN Domain

Table 5-72. UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
UART0_CTSn	I	UART Clear to Send (active low)	E22
UART0_RTSn	O	UART Request to Send (active low)	B21
UART0_RXD	I	UART Receive Data	F19
UART0_TXD	O	UART Transmit Data	F20

Table 5-73. UART1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
UART1_CTSn	I	UART Clear to Send (active low)	A25
UART1_DCDn	I	UART Clear to Send (active low)	D23
UART1_DSRn	I	UART Data Set Ready (active low)	B22
UART1_DTRn	O	UART Data Terminal Ready (active low)	D22
UART1_RIn	I	UART Ring Indicator	C22
UART1_RTSn	O	UART Request to Send (active low)	A26
UART1_RXD	I	UART Receive Data	C24, C27
UART1_TXD	O	UART Transmit Data	A22, F24

Table 5-74. UART2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
UART2_CTSn	I	UART Clear to Send (active low)	AC26, H23, V22
UART2_RTSn	IO	UART Request to Send (active low)	AB23, H20, V23
UART2_RXD	I	UART Receive Data	E22, H25, U27, W27
UART2_TXD	IO	UART Transmit Data	B21, J23, U26, W25

Table 5-75. UART3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
UART3_CTSn	I	UART Clear to Send (active low)	A24, AC27
UART3_RTSn	I	UART Request to Send (active low)	AB24, B24
UART3_RXD	I	UART Receive Data	H24, V27, W24
UART3_TXD	IO	UART Transmit Data	H22, V25, W23

Table 5-76. UART4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
UART4_CTSn	I	UART Clear to Send (active low)	AB27
UART4_RTSn	O	UART Request to Send (active low)	AB26
UART4_RXD	I	UART Receive Data	F26, P22, V26, W22

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Table 5-76. UART4 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
UART4_TXD	O	UART Transmit Data	H21, P23, V24, W21

Table 5-77. UART5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
UART5_CTSn	I	UART Clear to Send (active low)	AA22, L22
UART5_RTSn	O	UART Request to Send (active low)	AA23, L23
UART5_RXD	I	UART Receive Data	D22, J27, K22, V22, Y26
UART5_TXD	O	UART Transmit Data	C22, H27, J22, V23, Y27

Table 5-78. UART6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
UART6_CTSn	I	UART Clear to Send (active low)	AB25, M27
UART6_RTSn	O	UART Request to Send (active low)	AA25, N27
UART6_RXD	I	UART Receive Data	A25, AA24, B24, H26, L21, W26
UART6_TXD	O	UART Transmit Data	A24, A26, AA27, F27, M26, N24

5.3.26.2 MCU Domain

Table 5-79. MCU_UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
MCU_UART0_CTSn	I	UART Clear to Send (active low)	B5
MCU_UART0_RTSn	O	UART Request to Send (active low)	C5
MCU_UART0_RXD	I	UART Receive Data	B8
MCU_UART0_TXD	O	UART Transmit Data	B4

5.3.26.3 WKUP Domain

Table 5-80. WKUP_UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
WKUP_UART0_CTSn	I	UART Clear to Send (active low)	C4
WKUP_UART0_RTSn	O	UART Request to Send (active low)	C3
WKUP_UART0_RXD	I	UART Receive Data	B3
WKUP_UART0_TXD	O	UART Transmit Data	C8

5.3.27 USB

5.3.27.1 MAIN Domain

Table 5-81. USB0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
USB0_DM	IO	USB 2.0 Differential Data (negative)	AB5
USB0_DP	IO	USB 2.0 Differential Data (positive)	AA6

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Table 5-81. USB0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
USB0_DRVVBUS	O	USB VBUS control output (active high)	E25
USB0_RCALIB (1)	A	Pin to connect to calibration resistor	AA8
USB0_VBUS (2)	A	USB Level-shifted VBUS Input	W7

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.
(2) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see Section 8.2.3, *USB VBUS Design Guidelines*.

Table 5-82. USB1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMW PIN [4]
USB1_DM	IO	USB 2.0 Differential Data (negative)	E17
USB1_DP	IO	USB 2.0 Differential Data (positive)	D17
USB1_DRVVBUS	O	USB VBUS control output (active high)	B27
USB1_RCALIB (1)	A	Pin to connect to calibration resistor	E18
USB1_VBUS (2)	A	USB Level-shifted VBUS Input	F18

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.
(2) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see Section 8.2.3, *USB VBUS Design Guidelines*.

5.4 Pin Connectivity Requirements

This section describes connectivity requirements for package balls that have specific connectivity requirements and unused package balls.

Note

All power pins must be supplied with the voltages specified in *Recommended Operating Conditions*, unless otherwise specified.

Note

For additional clarification, "leave unconnected" or "no connect" (NC) means **no** signal traces can be connected to these device ball numbers.

Table 5-83. Connectivity Requirements

AMW BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
B10	TRSTn	Each of these balls must be connected to VSS through separate external pull resistors to ensure these balls are held to a valid logic-low level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-down can be used to hold a valid logic-low level if no PCB signal trace is connected to the ball.
A11 E12 F11	TCK TDI TMS	Each of these balls must be connected to the corresponding power supply(1) through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic-high level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-up can be used to hold a valid logic-high level if no PCB signal trace is connected to the ball.

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Table 5-83. Connectivity Requirements (continued)

AMW BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
C9 F9 D10 E26 E8 B23 B13 E11 B9 D11 F1 J1 U1 T1	EMU0 EMU1 MCU_RESETz RESET_REQz MCU_PORz EXTINTN MCU_I2C0_SCL MCU_I2C0_SDA WKUP_I2C0_SCL WKUP_I2C0_SDA DDR0_DQS0_n DDR0_DQS1_n DDR0_DQS2_n DDR0_DQS3_n	Each of these balls must be connected to the corresponding power supply(1) through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic-high level, if unused.
R22 R23 R26 T27 T25 T24 T21 T22 U27 U26 V27 V25 V26 V24 V22 V23	GPMC0_AD0 GPMC0_AD1 GPMC0_AD2 GPMC0_AD3 GPMC0_AD4 GPMC0_AD5 GPMC0_AD6 GPMC0_AD7 GPMC0_AD8 GPMC0_AD9 GPMC0_AD10 GPMC0_AD11 GPMC0_AD12 GPMC0_AD13 GPMC0_AD14 GPMC0_AD15	Each of these balls must be connected to the corresponding power supply(1) or VSS through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic-high or logic-low level as appropriate to select the desired device boot mode.
E1 H1 T1 W1 G7 J7 K7 A3	DDR0_DQS0 DDR0_DQS1 DDR0_DQS2 DDR0_DQS3 VMON_ER_VSYS VMON_1P8_SOC VMON_3P3_SOC WKUP_LFOSC0_XI	Each of these balls must be connected to VSS through separate external pull resistors to ensure these balls are held to a valid logic-low level, if unused.
E15 F14 AB8 AA10 AB14 AB15 AA16 AA8 E18	SERDES0_REXT SERDES1_REXT CSI0_RXRCALIB CSI1_RXRCALIB CSI2_RXRCALIB CSI3_RXRCALIB DSI0_TXRCALIB USB0_RCALIB USB1_RCALIB	Each of these balls must be connected to VSS through an appropriate external pull resistor to ensure these balls are held to a valid logic-low level, if unused. Refer to *Signal Descriptions* footnote for appropriate value of pull resistor for each signal.
G9 AC1	VPP MMC0_CALPAD	Each of these balls must be left unconnected, if unused.

(1) To determine which power supply is associated with any IO, see the POWER column of the *Pin Attributes* table.

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Note

All other unused signal balls with a Pad Configuration Register can be left unconnected with their multiplexing mode set to GPIO input and internal pull-down resistor enabled. Unused balls are defined as those which only connect to a PCB solder pad. This is the only use case where internal pull resistors are allowed as the only source/sink to hold a valid logic level. Any balls connected to a via, test point, or PCB trace are consider used and must not depend on the internal pull resistor to hold a valid logic level.

Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This can be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors are recommended to hold a valid logic level on balls with external connections.

Many of the device IOs are turned off by default and external pull resistors may be required to hold inputs of any attached device in a valid logic state until software initializes the respective IOs. The state of configurable device IOs are defined in the BALL STATE DURING RESET RX/TX/PULL and BALL STATE AFTER RESET RX/TX/PULL columns of the *Pin Attributes* table. Any IO with its input buffer (RX) turned off is allowed to float without damaging the device. However, any IO with its input buffer (RX) turned on shall never be allowed to float to any potential between V_{ILSS} and V_{IHSS}. The input buffer can enter a high-current state which could damage the IO cell if allowed to float between these levels.

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6 Specifications

Note

All specifications listed are preliminary and may change during device characterization.

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1] [2]

PARAMETER		MIN	MAX	UNIT
VDD_CORE	Core supply	-0.3	1.05	V
VDDR_CORE	RAM core supply	-0.3	1.05	V
VDD_CANUART	CANUART core supply	-0.3	1.05	V
VDDA_CORE_CSI_DSI	CSIRX0 and DSITX0 core supply	-0.3	1.05	V
VDDA_CORE_CSI_DSI_CLK	CSIRX0 and DSITX0 clock core supply	-0.3	1.05	V
VDDA_CORE_USB0 VDDA_CORE_USB1	USB0 and USB1 core supply	-0.3	1.05	V
VDDA_DDR_PLL0	DDR deskew PLL supply	-0.3	1.05	V
VDD_MMC0	MMC0 PHY core supply	-0.3	1.05	V
VDDA_0P85_DLL_MMC0	MMC0 DLL analog supply	-0.3	1.05	V
VDDA_0P85_SERDES VDDA_0P85_SERDES_C	SERDES analog supply	-0.3	1.05	V
VDDS_DDR	DDR PHY IO supply	-0.3	1.57	V
VDDS_DDR_C	DDR clock IO supply	-0.3	1.57	V
VDDA_1P8_SERDES	SERDES PHY IO supply	-0.3	1.98	V
VDDS_MMC0	MMC0 PHY IO supply	-0.3	1.98	V
VDDS_OSC0	MCU_OSC0 and WKUP_LFOSC0 supply	-0.3	1.98	V
VDDA_MCU	RCOSC, POR, POK, and MCU PLL analog supply	-0.3	1.98	V
VDDA_PLL0	SMS PLL analog supply	-0.3	1.98	V
VDDA_PLL1	MAIN PLL, PER0 PLL, and PER1 PLL analog supply	-0.3	1.98	V
VDDA_PLL2	DDR PLL and ARM0 PLL analog supply	-0.3	1.98	V
VDDA_PLL3	VIDEO PLL and GPU PLL analog supply	-0.3	1.98	V
VDDA_PLL4	DSS PLL0, DSS PLL1, and DSS PLL2 analog supply	-0.3	1.98	V
VDDA_PLL5	C7x PLL analog supply	-0.3	1.98	V
VDDA_1P8_CSI_DSI	CSIRX0 and DSITX0 1.8 V analog supply	-0.3	1.98	V
VDDA_1P8_OLDI0	OLDI0 1.8 V analog supply	-0.3	1.98	V
VDDA_1P8_USB0 VDDA_1P8_USB1	USB0 and USB1 1.8 V analog supply	-0.3	1.98	V
VDDA_TEMP0	TEMP0 analog supply	-0.3	1.98	V
VDDA_TEMP1	TEMP1 analog supply	-0.3	1.98	V
VDDA_TEMP2	TEMP2 analog supply	-0.3	1.98	V
VPP	eFuse ROM programming supply	-0.3	1.98	V
VDDSHV_MCU	IO supply for IO group MCU	-0.3	3.63	V
VDDSHV_CANUART	IO supply for IO group CANUART	-0.3	3.63	V
VDDSHV0	IO supply for IO group 0	-0.3	3.63	V
VDDSHV1	IO supply for IO group 1	-0.3	3.63	V
VDDSHV2	IO supply for IO group 2	-0.3	3.63	V
VDDSHV3	IO supply for IO group 3	-0.3	3.63	V
VDDSHV5	IO supply for IO group 5	-0.3	3.63	V
VDDSHV6	IO supply for IO group 6	-0.3	3.63	V

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over operating junction temperature range (unless otherwise noted)(1) (2)

PARAMETER			MIN	MAX	UNIT
VDDA_3P3_USB0 VDDA_3P3_USB1	USB0 and USB1 3.3 V analog supply		-0.3	3.63	V
Steady-state max voltage at all fail-safe IO pins		MCU_PORz	-0.3	3.63	V
		MCU_I2C0_SCL, MCU_I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, EXTINTn When operating at 1.8V	-0.3	1.98(3)	V
		MCU_I2C0_SCL, MCU_I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, EXTINTn When operating at 3.3V	-0.3	3.63(3)	
		VMON_1P8_SOC	-0.3	1.98	V
		VMON_3P3_SOC	-0.3	3.63	V
		VMON_VSYS(4)	-0.3	1.98	V
Steady-state max voltage at all other IO pins(5)		USB0_VBUS, USB1_VBUS(6)	-0.3	3.6	V
		All other IO pins	-0.3	IO supply voltage + 0.3	V
Transient overshoot and undershoot at IO pin		20% of IO supply voltage for up to 20% of the signal period (see Figure 6-1)		0.2 × VDD(7)	V
Latch-up performance(8)		I-Test	-100	100	mA
		Over-Voltage (OV) Test		1.5 x VDD(7)	V
T_{STG}	Storage temperature		-55	+150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) The absolute maximum ratings for these fail-safe pins depends on their IO supply operating voltage. Therefore, this value is also defined by the maximum V_{IH} value found in the I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics section, where the electrical characteristics table has separate parameter values for 1.8-V mode and 3.3-V mode.
(4) The VMON_VSYS pin provides a way to monitor the system power supply. For more information, see System Power Supply Monitor Design Guidelines.
(5) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
(6) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see the USB VBUS Design Guidelines.
(7) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
(8) For current pulse injection (I-Test):

- Pins stressed per JEDEC JESD78 (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

For over-voltage performance (Over-Voltage (OV) Test):

- Supplies stressed per JEDEC JESD78 (Class II) and passed specified voltage injection.

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The MCU_I2C0_SCL, MCU_I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, EXTINTn, VMON_1P8_SOC, VMON_3P3_SOC, and MCU_PORz are the only fail-safe IO terminals. All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in Section 6.1.

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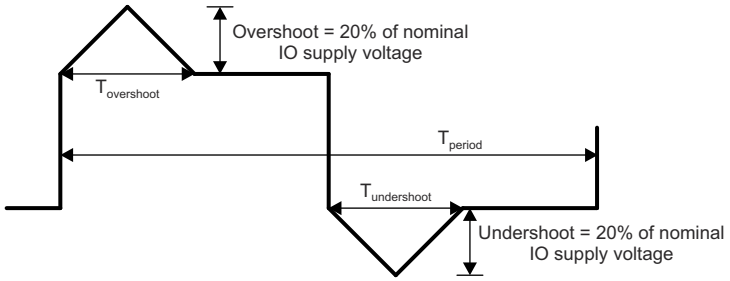

A. $T_{overshoot} + T_{undershoot} < 20\%$ of T_{period}

Figure 6-1. IO Transient Voltage Ranges

6.2 ESD Ratings for AEC - Q100 Qualified Devices in the AMW Package

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC - Q100-002(1)		±1000	V
		Charged-device model (CDM), per AEC - Q100-011	Corner pins (A1, A25, AE1, and AE25)	±750	
			All other pins	±250	

(1) AEC - Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Power-On Hours (POH)

POWER ON HOURS (POH)(1) (2) (3)	
JUNCTION TEMPERATURE RANGE (T_J)(4)	LIFETIME (POH)
–40°C to 105°C	100000
–40°C to 125°C	20000(5)

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
(3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.
(4) Either –40 to 105C or –40 to 125C profile should be chosen and applied through the lifetime of the application. Mixing of these profiles for the purposes of extending temperature and/or POH may result in increased reliability failure risk and is not recommended.
(5) The –40 to 125C profile is defined as 20000 power on hours with a junction temperature as follows: 5%@–40°C, 65%@70°C, 20%@110°C, and 10%@125°C.

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6.4 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN[1]	NOM	MAX[1]	UNIT
VDD_CORE[2] VDDA_CORE_CSI_DSI[2] VDDA_CORE_CSI_DSI_CLK[2] VDDA_CORE_USB0[2] VDDA_CORE_USB1[2] VDDA_DDR_PLL0[2]	Core supply CSIRX0 and DSITX0 core supply DSITX0 clock core supply USB0 and USB1 core supply DDR deskew PLL supply	0.75-V operation	0.715	0.75	0.79	V
		0.85-V operation	0.81	0.85	0.895	V
VDD_CANUART[3]	CANUART core supply	0.75-V operation	0.715	0.75	0.79	V
		0.85-V operation	0.81	0.85	0.895	V
VDDR_CORE	RAM core supply		0.81	0.85	0.895	V
VDD_MMC0[4] VDDA_0P85_DLL_MMC0[4]	MMC0 PHY core supply MMC0 DLL analog supply		0.81	0.85	0.895	V
VDDA_0P85_SERDES VDDA_0P85_SERDES_C	SERDES PHY core supply SERDES analog supply		0.81	0.85	0.895	V
VDDS_DDR[5] VDDS_DDR_C[5]	DDR PHY IO supply DDR clock IO supply	1.1-V operation	1.06	1.1	1.17	V
VDDA_1P8_SERDES	SERDES analog supply		1.71	1.8	1.89	V
VDDS_MMC0	MMC0 PHY IO supply		1.71	1.8	1.89	V
VDDS_OSC0	MCU_OSC0 and WKUP_LFOSC0 supply		1.71	1.8	1.89	V
VDDA_MCU	RCOSC, POR, POK, and MCU PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL0	SMS PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL1	MAIN PLL, PER0 PLL, and PER1 PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL2	DDR PLL and ARM0 PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL3	VIDEO PLL and GPU PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL4	DSS PLL0, DSS PLL1, and DSS PLL2 analog supply		1.71	1.8	1.89	V
VDDA_PLL5	C7x PLL analog supply		1.71	1.8	1.89	V
VDDA_1P8_CSI_DSI	CSIRX0 and DSITX0 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_1P8_OLDI0	OLDI0 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_1P8_USB0 VDDA_1P8_USB1	USB0 and USB1 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_TEMP0	TEMP0 analog supply		1.71	1.8	1.89	V
VDDA_TEMP1	TEMP1 analog supply		1.71	1.8	1.89	V
VDDA_TEMP2	TEMP2 analog supply		1.71	1.8	1.89	V
VPP	eFuse ROM programming supply		see[6]	see[6]	see[6]	V
VMON_1P8_SOC	Voltage monitor for 1.8 V SoC power supply		1.71	1.8	1.89	V
VDDA_3P3_USB0	USB0 3.3 V analog supply		3.135	3.3	3.465	V
VDDA_3P3_USB1	USB1 3.3 V analog supply					
VMON_3P3_SOC	Voltage monitor for 3.3 V SoC power supply		3.135	3.3	3.465	V
VMON_ER_VSYS	Voltage monitor for system power supply		0	see[7]	1	V
USB0_VBUS	USB0 Level-shifted VBUS Input		0	see[8]	3.465	V
USB1_VBUS	USB1 Level-shifted VBUS Input		0	see[8]	3.465	V
VDDSHV_CANUART[9]	Dual-voltage IO supply for IO group CANUART	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV_MCU	Dual-voltage IO supply for IO group MCU	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V

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over operating junction temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN(1)	NOM	MAX(1)	UNIT
VDDSHV0	Dual-voltage IO supply for IO group 0	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV1	Dual-voltage IO supply for IO group 1	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV2	Dual-voltage IO supply for IO group 2	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV3	Dual-voltage IO supply for IO group 3	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV5	Dual-voltage IO supply for IO group 5	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV6	Dual-voltage IO supply for IO group 6	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
T_J	Operating junction temperature range	Automotive Q100	–40		125	°C
		Extended Industrial	–40		105	°C

(1) The voltage at the device ball must never drop below the MIN voltage or rise above the MAX voltage for any amount of time during normal device operation.
(2) VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 shall be sourced from the same power source. Care should be taken to ensure that voltage differential between VDD_CORE and VDDA_CORE_USB is within +/- 1%.
(3) VDD_CANUART shall be connected to an always on power source when using Partial IO or IO Only + DDR Self-refresh low power modes. VDD_CANUART shall be connected to the same power source as VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_USB, and VDDA_DDR_PLL0 when not using Partial IO or IO Only + DDR Self-refresh low power modes.
(4) VDD_MMC0 and VDDA_0P85_DLL_MMC0 must be connected to the same power source as VDD_CORE when MMC0 is not used. In this case, VDD_MMC0 and VDDA_0P85_DLL_MMC0 may be operated at a nominal voltage of 0.75 or 0.85.
(5) VDDS_DDR and VDDS_DDR_C shall be sourced from the same power source.
(6) Refer to the Recommended Operating Conditions for OTP eFuse Programming table for VPP supply voltages based on eFuse usage.
(7) The VMON_VSYS pin provides a way to monitor the system power supply. For more information, see System Power Supply Monitor Design Guidelines.
(8) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see USB VBUS Design Guidelines.
(9) VDDSHV_CANUART shall be connected to an always on power source when using Partial IO or IO Only + DDR Self-refresh low power modes. VDDSHV_CANUART shall be connected to any valid IO power source when not using Partial IO or IO Only + DDR Self-refresh low power modes.

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6.5 Operating Performance Points

Table 6-1 defines the maximum operating frequency of the clocks for each device speed grade and Table 6-2 defines the only valid Operating Performance Points (OPPs) for the device subsystem and core clocks..

Table 6-1. Device Speed Grades

Speed Grade	VDD_CORE (V)(1)	MAXIMUM OPERATING FREQUNCY (MHz)													MAXIMUM DATA RATE (MT/s)(2)
		A53SS (Cortex-A53x)	C7/MMA	R5FSS0	MAIN DOMAIN SYSCLK	MCU R5F	MCU DOMAIN SYSCLK	DEVICE MGR R5F	DEVICE MGR DOMAIN CLK	HSM	GPU	VPAC	DMPAC	VPU	LPDDR4
J	0.75	1250	912.5	800	500	800	400	800	400	400	720	600	428.5	500	3200 to 3733
K	0.85	1400	1000								800				3466 to 4000

(1) Nominal operating voltage, see Section 6.4.
(2) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to LPDDR4 Board Design and Layout Guidelines for the proper PCB implementation to achieve maximum DDR frequency. It is recommended that software uses the minimum required LPDDR4 transfer rate that satisfies the performance requirements of the system.

Table 6-2. Device Operating Performance Points

OPP	A53SS(1)	C7/MMA	FIXED OPERATING FREQUENCY OPTIONS (MHz)(2)											MT/s(3)
			R5FSS0	MAIN DOMAIN SYSCLK	MCU R5F	MCU DOMAIN SYSCLK	DEVICE MGR R5F	DEVICE MGR DOMAIN CLK	HSM	GPU	VPAC	DMPAC	VPU	LPDDR4
High	From PLL BP to Speed Grade Max	From PLL BP to Speed Grade Max	800	500	800	400	800	400	400	Speed Grade Max	600	428.5	500, 400, 200, or 100	From PLL BP to Speed Grade Max
Low			400	250	400	200	400	133	133					

(1) Default operating frequency, set by software at boot. Supports Dynamic Frequency Scaling after boot.
(2) Fixed operating frequency, set by software at boot.
(3) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to LPDDR4 Board Design and Layout Guidelines for the proper PCB implementation to achieve maximum DDR frequency.

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6.6 Electrical Characteristics

Note

The interfaces or signals described in Section 6.6 correspond to the interfaces or signals available in multiplexing mode 0 (Primary Signal Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

6.6.1 I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8V MODE						
V_{IL}	Input Low Voltage				0.3 × VDD [1]	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD [1]	V
V_{IH}	Input High Voltage		0.7 × VDD [1]		1.98[2]	V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDD [1]			V
V_{HYS}	Input Hysteresis Voltage		0.1 × VDD [1]			mV
I_{IN}	Input Leakage Current.	V_I = 1.8V or V_I = 0V			±10	µA
V_{OL}	Output Low Voltage				0.2 × VDD [1]	V
I_{OL} [3]	Low Level Output Current	$V_{OL(MAX)}$	10			mA
SR_I [5]	Input Slew Rate		18f[4] or 1.8E+6			V/s
3.3V MODE [6]						
V_{IL}	Input Low Voltage				0.3 × VDD [1]	V
V_{ILSS}	Input Low Voltage Steady State				0.25 × VDD [1]	V
V_{IH}	Input High Voltage		0.7 × VDD [1]		3.63[2]	V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDD [1]			V
V_{HYS}	Input Hysteresis Voltage		0.05 × VDD [1]			mV
I_{IN}	Input Leakage Current.	V_I = 3.3V or V_I = 0V			±10	µA
V_{OL}	Output Low Voltage				0.4	V
I_{OL} [3]	Low Level Output Current	$V_{OL(MAX)}$	10			mA
SR_I [5]	Input Slew Rate		33f[4] or 3.3E+6		8E+7	V/s

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
(2) This value also defines the Absolute Maximum Ratings value the IO.
(3) The I_{OL} parameter defines the minimum Low Level Output Current for which the device is able to maintain the specified V_{OL} value. The value defined by this parameter should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} value for attached components.
(4) f = toggle frequency of the input signal in Hz.
(5) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.
(6) I2C Hs-mode is not supported when operating the IO in 3.3V mode.

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6.6.2 Fail-Safe Reset (FS RESET) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.3 × VDDS_OSC0	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.7 × VDDS_OSC0			V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage		200			mV
I_{IN}	Input Leakage Current.	V_I = 1.8V or V_I = 0V			±10	µA
SR_I (2)	Input Slew Rate		18f(1) or 1.8E+6			V/s

(1) f = toggle frequency of the input signal in Hz.
(2) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

6.6.3 High-Frequency Oscillator (HFOSC) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.35 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.65 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage			49		mV
I_{IN}	Input Leakage Current.	V_I = 1.8V or V_I = 0.0V			±10	µA

6.6.4 Low-Frequency Oscillator (LFXOSC) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.30 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.70 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage	Active Mode		85		mV
		Bypass Mode		324		mV
I_{IN}	Input Leakage Current.	V_I = 1.8V or V_I = 0.0V			±10	µA

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6.6.5 SDIO Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8V MODE						
V_{IL}	Input Low Voltage				0.58	V
V_{ILSS}	Input Low Voltage Steady State				0.58	V
V_{IH}	Input High Voltage		1.27			V
V_{IHSS}	Input High Voltage Steady State		1.7			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 1.8V or V_I = 0V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDD(1) - 0.45			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	4			mA
I_{OH} (2)	High Level Output Current	$V_{OH(MIN)}$	4			mA
SR_I (4)	Input Slew Rate		18f(3) or 1.8E+6			V/s
3.3V MODE						
V_{IL}	Input Low Voltage				0.25 × VDD(1)	V
V_{ILSS}	Input Low Voltage Steady State				0.15 × VDD(1)	V
V_{IH}	Input High Voltage		0.625 × VDD(1)			V
V_{IHSS}	Input High Voltage Steady State		0.625 × VDD(1)			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 3.3V or V_I = 0V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output Low Voltage				0.125 × VDD(1)	V
V_{OH}	Output High Voltage		0.75 × VDD(1)			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	6			mA
I_{OH} (2)	High Level Output Current	$V_{OH(MIN)}$	10			mA
SR_I (4)	Input Slew Rate		33f(3) or 3.3E+6			V/s

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
(2) The I_{OL} and I_{OH} parameters define the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V_{OL} and V_{OH} values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} and V_{OH} values for attached components.
(3) f = toggle frequency of the input signal in Hz.
(4) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

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6.6.6 LVCMOS Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8V MODE						
V_{IL}	Input Low Voltage				0.35 × VDD(1)	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD(1)	V
V_{IH}	Input High Voltage		0.65 × VDD(1)			V
V_{IHSS}	Input High Voltage Steady State		0.85 × VDD(1)			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 1.8V or V_I = 0.0V			±10	µA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDD(1) - 0.45			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	3			mA
I_{OH} (2)	High Level Output Current	$V_{OH(MIN)}$	3			mA
SR_I (4)	Input Slew Rate		18f(3) or 1.8E+6			V/s
3.3V MODE						
V_{IL}	Input Low Voltage				0.8	V
V_{ILSS}	Input Low Voltage Steady State				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{IHSS}	Input High Voltage Steady State		2.0			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 3.3V or V_I = 0.0V			±10	µA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	5			mA
I_{OH} (2)	High Level Output Current	$V_{OH(MIN)}$	9			mA
SR_I (4)	Input Slew Rate		33f(3) or 3.3E+6			V/s

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
(2) The I_{OL} and I_{OH} parameters define the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V_{OL} and V_{OH} values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} and V_{OH} values for attached components.
(3) f = toggle frequency of the input signal in Hz.
(4) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

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6.6.7 CSI-2 (D-PHY) Electrical Characteristics

Note

CSIRX0 is compliant with MIPI DPHY v1.2 dated August 1, 2014, including ECNs and Errata as applicable.

6.6.8 USB2PHY Electrical Characteristics

Note

The USB0 and USB1 interfaces are compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

6.6.9 DDR Electrical Characteristics

Note

The DDR interface is compatible with LPDDR4 devices that are **JESD209-4B standard-compliant**

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6.7 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses .

6.7.1 Recommended Operating Conditions for OTP eFuse Programming

over operating junction temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VDD_CORE	Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)	See *Recommended Operating Conditions*			V
VPP	Supply voltage range for the eFuse ROM domain during normal operation without hardware support to program eFuse ROM		NC(1)		V
	Supply voltage range for the eFuse ROM domain during normal operation with hardware support to program eFuse ROM		0		V
	Supply voltage range for the eFuse ROM domain during OTP programming(2)	1.71	1.8	1.89	V
$I_{(VPP)}$	VPP current			400	mA
$SR_{(VPP)}$	VPP Power-up Slew Rate			6E + 4	V/s
Tj	Operating junction temperature range while programming eFuse ROM.	0	25	85	°C

(1) NC indicates No Connect.
(2) Supply voltage range includes DC errors and peak-to-peak noise.

6.7.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.
- The VPP power supply must be ramped up after the proper device power-up sequence (for more details, see Section 6.9.2.2, *Power Supply Sequencing*).

6.7.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP terminal according to the specification in Section 6.7.1.
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP terminal.

6.7.4 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

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6.8 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in Recommended Operating Conditions.

6.8.1 Thermal Resistance Characteristics for AMW Package TBD

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

NO.	PARAMETER	DESCRIPTION	AMW PACKAGE	
			°C/W(1) (3)	AIR FLOW (m/s)(2)
T1	$R\Theta_{JC}$	Junction-to-case	0.50	N/A
T2	$R\Theta_{JB}$	Junction-to-board	2.4	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	12.6	0
T4		Junction-to-moving air	8.0	1
T5			6.9	2
T6			6.4	3
T7	Ψ_{JT}	Junction-to-package top	0.25	0
T8			0.26	1
T9			0.27	2
T10			0.27	3
T11	Ψ_{JB}	Junction-to-board	2.3	0
T12			2.0	1
T13			1.9	2
T14			1.9	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [RΘJC] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second.
(3) °C/W = degrees Celsius per watt.

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6.9 Timing and Switching Characteristics

Note

The Timing Requirements and Switching Characteristics values may change following the silicon characterization result.

Note

The default SLEWRATE settings in each pad configuration register must be used to ensure timings, unless specific instructions are given otherwise.

6.9.1 Timing Parameters and Information

The timing parameter symbols used in Section 6.9, *Timing and Switching Characteristics* are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in Table 6-3:

Table 6-3. Timing Parameters Subscripts

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

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6.9.2 Power Supply Requirements

This section describes the power supply requirements to ensure proper device operation.

Note

All power balls must be supplied with the voltages specified in the *Recommended Operating Conditions* section, unless otherwise specified in *Signal Descriptions* and *Pin Connectivity Requirements*.

6.9.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 18mV/µs. For instance, as shown in Figure 6-2, TI recommends having the supply ramp slew for a 1.8V supply of more than 100µs.

Figure 6-2 describes the Power Supply Slew Rate Requirement in the device.

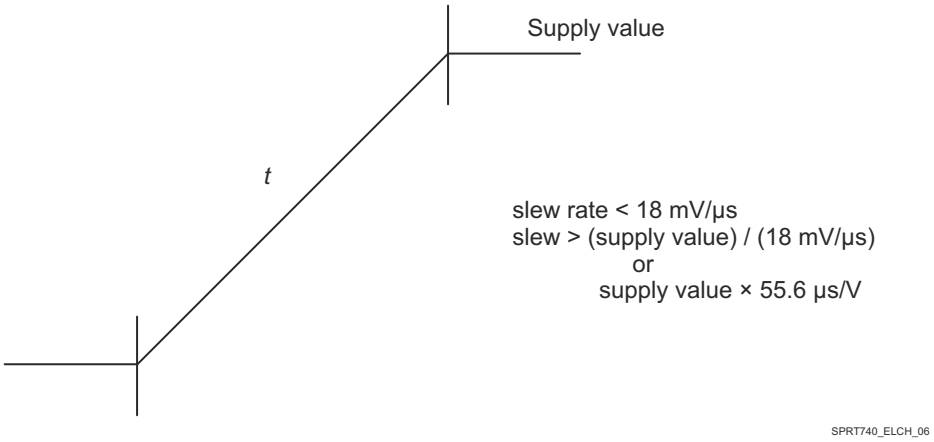

Figure 6-2. Power Supply Slew and Slew Rate

6.9.2.2 Power Supply Sequencing

This section describes power sequence requirements using power sequence diagrams and associated notes. Each power sequence diagram demonstrates the sequential order expected for each device power rail. This is done by assigning each device power rail to one or more waveform. A dual-voltage power rail may be associated with more than one waveform and the associated note will describe which waveform is applicable. Each waveform defines a transition region for the associated power rails and shows its sequential relationship to the transition regions of other power rails. The notes associated with the power sequence diagram provides further detail of these requirements. See the *Power-up Sequence* section for details on power-up requirements, and the *Power-down Sequence* section for details on power-down requirements.

Two types of power supply transition regions are used to simplify the power supply sequencing diagrams. The legends shown in Figure 6-3 and Figure 6-4 along with their descriptions are provided to clarify what each transition regions represents.

Figure 6-3 defines a transition region with multiple power rails which may be sourced from multiple power supplies or a single power supply. Transitions shown within the transition region represent a use case where multiple power supplies are used to source power rails associated with this waveform, and these power supplies are allowed to ramp at different times within the region since they do not have any specific sequence requirement relative to each other.

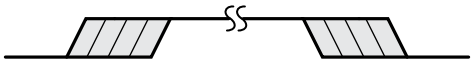

Figure 6-3. Multiple Power Supply Transition Legend

Figure 6-4 defines a transition region with one or more power rails which must be sourced from a single common power supply. No transitions are shown within the region to represent a single ramp within the transition region.

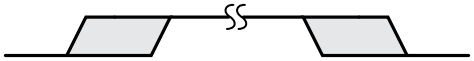

Figure 6-4. Single Common Power Supply Transition Legend

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6.9.2.2.1 Power-Up Sequencing

Table 6-4 and Figure 6-5 describes the device power-up sequencing.

Note

The power supply sequencing requirements defined in this section does not include entry or exit from low power modes. See the Partial IO Power Sequencing section for more information on the requirements for entering or exiting from Partial IO low power mode.

Note

All power rails must be turned off and decay below 300mV before initiating a new power-up sequence anytime a power rail drops below the minimum value defined in *Recommended Operating Conditions*. The only exception is when entering/exiting Partial IO low power mode with VDDSHV_CANUART and VDD_CANUART sourced from an always on power source. For this use case the VDDSHV_CANUART and VDD_CANUART power rails are allowed to remain on.

Table 6-4. Power-Up Sequencing – Supply / Signal Assignments

See: Figure 6-5

WAVEFORM	SUPPLY / SIGNAL NAME
A	VSYS(1), VMON_VSYS(2)
B	VDDSHV_CANUART(3), VDDSHV_MCU(3), VDDSHV0(3), VDDSHV1(3), VDDSHV2(3), VDDSHV3(3), VDDA_3P3_USB, VMON_3P3_SOC(4)
C	VDDSHV_CANUART(5), VDDSHV_MCU(5), VDDSHV0(5), VDDSHV1(5), VDDSHV2(5), VDDSHV3(5), VDDS_MMC0, VDDA_MCU, VDDS_OSC0, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_CSI_DSI, VDDA_1P8_OLDI0, VDDA_1P8_USB, VDDA_TEMP0, VDDA_TEMP1, VMON_1P8_SOC(6)
D	VDDSHV5(7), VDDSHV6(7)
E	VDDS_DDR(8), VDDS_DDR_C(8)
F	VDD_CANUART(9)
G	VDD_CANUART(10), VDD_CORE(10) (12), VDDA_CORE_CSI_DSI(10), VDDA_CORE_DSI_CLK(10), VDDA_CORE_USB0(10), VDDA_DDR_PLL0(10)
H	VDD_CANUART(11), VDD_CORE(11) (12), VDDA_CORE_CSI_DSI(11), VDDA_CORE_DSI_CLK(11), VDDA_CORE_USB0(11), VDDA_DDR_PLL0(11), VDDR_CORE(12), VDD_MMC0, VDDA_0P85_DLL_MMC0
I	VPP(13)
J	MCU_PORz
K	MCU_OSC0_XI, MCU_OSC0_XO

(1) VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.

(2) VMON_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see the Section 8.2.4, *System Power Supply Monitor Design Guidelines*.

(3) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

VDDSHV_CANUART shall be connected to an always-on power source when using Partial IO low power mode, or connected to any valid IO power source when not using Partial IO low power mode. When VDDSHV_CANUART is not connected to an always-on power source and is operating at 3.3V, it shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.

When any of the VDDSHV_MCU and VDDSHVx [x=0-3] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.

(4) The VMON_3P3_SOC input is used to monitor supply voltage and shall be connected to the respective 3.3V supply source.

(5) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

VDDSHV_CANUART shall be connected to an always-on power source when using Partial IO low power mode, or connected to any valid IO power source when not using Partial IO low power mode. When VDDSHV_CANUART is not connected to an always-on power source and is operating at 1.8V, it shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.

When any of the VDDSHV_MCU and VDDSHVx [x=0-3] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.

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(6) The VMON_1P8_SOC input is used to monitor supply voltage and shall be connected to the respective 1.8V supply source.

(7) VDDSHV5, and VDDSHV6 were designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

(8) VDDS_DDR and VDDS_DDR_C are expected to be powered by the same source such that they ramp together.

(9) VDD_CANUART shall be connected to an always-on power source when using Partial IO low power mode.

When VDD_CANUART is connected to an always-on power source, the potential applied to VDD_CORE must never be greater than the potential applied to VDD_CANUART + 0.18V during power-up or power-down. This requires VDD_CANUART to ramp up before and ramp down after VDD_CORE. VDD_CANUART does not have any ramp requirements beyond the one defined for VDD_CORE.

(10) VDD_CANUART shall be connected to the same power source as VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 when not using Partial IO low power mode.

VDD_CANUART, VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 can be operated at 0.75V or 0.85V. When these supplies are operating at 0.75V, they shall be ramped up prior to VDDR_CORE as defined by this waveform.

(11) VDD_CANUART shall be connected to the same power source as VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 when not using Partial IO low power mode.

VDD_CANUART, VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 can be operated at 0.75V or 0.85V. When these supplies are operating at 0.85V, they shall be powered from the same source as VDDR_CORE and ramped during the 0.85V ramp period defined by this waveform.

(12) The potential applied to VDDR_CORE must never be greater than the potential applied to VDD_CORE + 0.18V during power-up or power-down. This requires VDD_CORE to ramp up before and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V. VDD_CORE does not have any ramp requirements beyond the one defined for VDDR_CORE.

VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V.

(13) VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.

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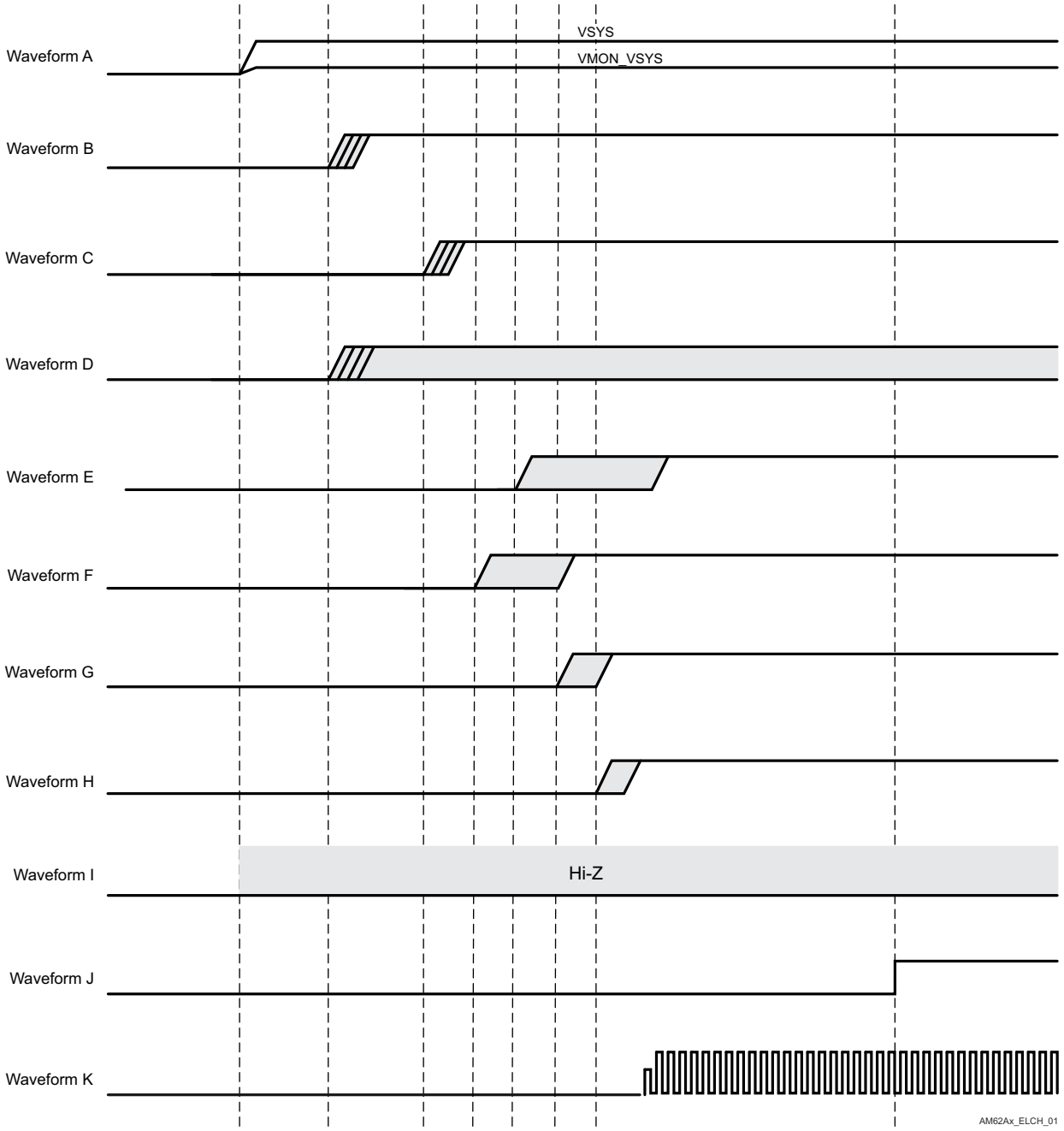

Figure 6-5. Power-Up Sequencing

6.9.2.2.2 Power-Down Sequencing

Table 6-5 and Figure 6-6 describes the device power-down sequencing.

Note

The power supply sequencing requirements defined in this section does not include entry or exit from low power modes. See the Partial IO Power Sequencing section for more information on the requirements for entering or exiting from Partial IO low power mode.

Note

All power rails must be turned off and decay below 300mV before initiating a new power-up sequence anytime a power rail drops below the minimum value defined in *Recommended Operating Conditions*. The only exception is when entering/exiting Partial IO low power mode with VDDSHV_CANUART and VDD_CANUART sourced from an always on power source. For this use case the VDDSHV_CANUART and VDD_CANUART power rails are allowed to remain on.

Table 6-5. Power-Down Sequencing – Supply / Signal Assignments

See: Figure 6-6

WAVEFORM	SUPPLY / SIGNAL NAME
A	VSYS, VMON_VSYS
B	VDDSHV_CANUART(1), VDDSHV_MCU(1), VDDSHV0(1), VDDSHV1(1), VDDSHV2(1), VDDSHV3(1), VDDA_3P3_USB, VMON_3P3_SOC
C	VDDSHV_CANUART(2), VDDSHV_MCU(2), VDDSHV0(2), VDDSHV1(2), VDDSHV2(2), VDDSHV3(2), VDDS_MMC0, VDDA_MCU, VDDS_OSC0, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_CSI_DSI, VDDA_1P8_OLDI0, VDDA_1P8_USB, VDDA_TEMP0, VDDA_TEMP1, VMON_1P8_SOC
D	VDDSHV5(3), VDDSHV6(3)
E	VDDS_DDR, VDDS_DDR_C
F	VDD_CANUART(4)
G	VDD_CANUART(5), VDD_CORE(5), VDDA_CORE_CSI_DSI(5), , VDDA_CORE_DSI_CLK(5), VDDA_CORE_USB0(5), VDDA_DDR_PLL0(5)
H	VDD_CANUART(6), VDD_CORE(6), VDDA_CORE_CSI_DSI(6), , VDDA_CORE_DSI_CLK(6), VDDA_CORE_USB0(6), VDDA_DDR_PLL0(6), VDDR_CORE, VDD_MMC0, VDDA_0P85_DLL_MMC0
I	VPP
J	MCU_PORz
K	MCU_OSC0_XI, MCU_OSC0_XO

(1) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] when operating at 3.3V.

(2) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] when operating at 1.8V.

(3) VDDSHV5, and VDDSHV6 were designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

(4) VDD_CANUART when connected to an always-on power source for Partial IO low power mode.

(5) VDD_CANUART, VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB0, and VDDA_DDR_PLL0 when operating at 0.75V

(6) VDD_CANUART, VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB0, and VDDA_DDR_PLL0 when operating at 0.85V

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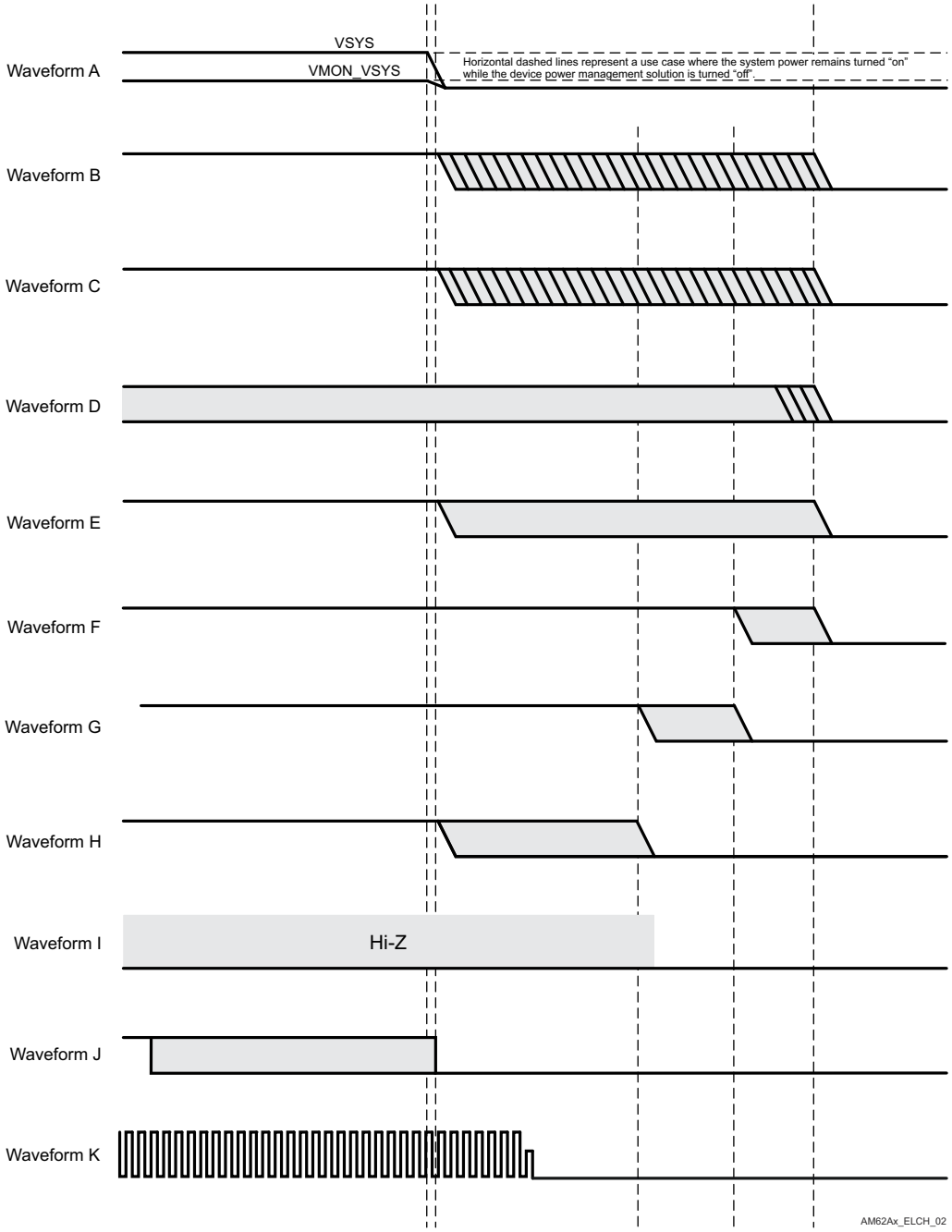

Figure 6-6. Power-Down Sequencing

6.9.2.2.3 Partial IO Power Sequencing

This section describes power supply sequence requirements when entering or exiting low power modes.

For more information on low power modes supported by this device and the names assigned to each low power mode, see the Power Modes section in the Device Configuration chapter of the Technical Reference Manual.

Partial IO is the only low power mode that requires power supply changes to the device power rails. All power supply rails except VDD_CANUART and VDDSHV_CANUART are turned off when operating in Partial IO mode. The power sequence required to enter Partial IO is the same sequence defined in Section 6.9.2.2.2, *Power-Down Sequencing* with the exception of VDD_CANUART and VDDSHV_CANUART, which remain powered. The power sequence required to exit Partial IO is the same sequence defined in Section 6.9.2.2.1, *Power-Up Sequencing* with the exception of VDD_CANUART and VDDSHV_CANUART, which are already powered.

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6.9.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.9.3.1 Reset Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for reset related signals.

Table 6-6. Reset Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD(1) = 1.8V	0.0018		V/ns
		VDD(1) = 3.3V	0.0033		V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance			30	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

Table 6-7. MCU_PORz Timing Requirements

see Figure 6-7

NO.	PARAMETER		MIN	MAX	UNIT
RST1	$t_{h(SUPPLIES\_VALID - MCU\_PORz)}$	Hold time, MCU_PORz active (low) at Power-up after supplies valid (using external crystal circuit)	9500000		ns
RST2		Hold time, MCU_PORz active (low) at Power-up after supplies valid and external clock stable (using external LVCMOS clock source)	1200		ns
RST3	$t_{w(MCU\_PORzL)}$	Pulse Width, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)	1200		ns

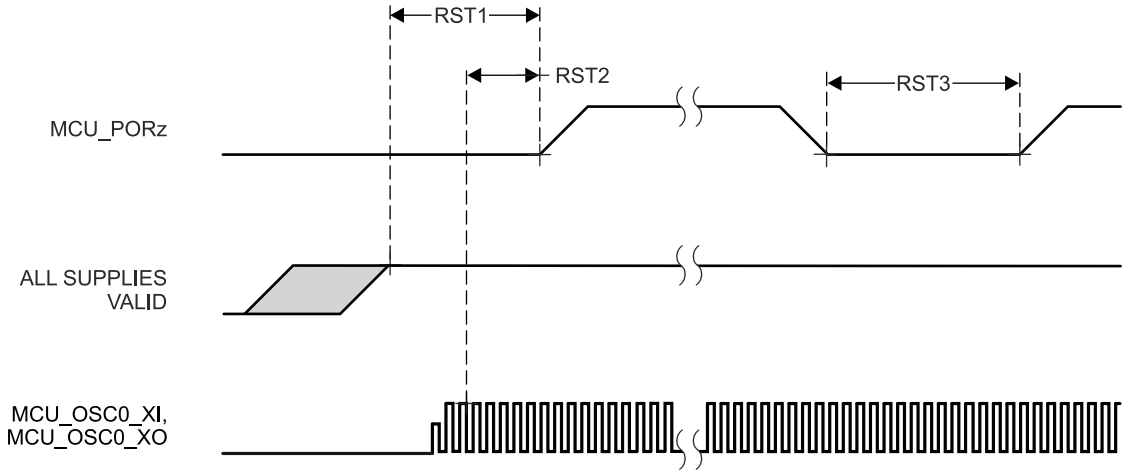

Figure 6-7. MCU_PORz Timing Requirements

Table 6-8. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see Figure 6-8

NO.	PARAMETER		MIN	MAX	UNIT
RST4	$t_{d(MCU\_PORzL-MCU\_RESETSTATzL)}$	Delay time, MCU_PORz active (low) to MCU_RESETSTATz active (low)	0		ns
RST5	$t_{d(MCU\_PORzH-MCU\_RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to MCU_RESETSTATz inactive (high)	6120*S(1)		ns
RST6	$t_{d(MCU\_PORzL-RESETSTATzL)}$	Delay time, MCU_PORz active (low) to RESETSTATz active (low)	0		ns
RST7	$t_{d(MCU\_PORzH-RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to RESETSTATz inactive (high)	9195*S(1)		ns
RST8	$t_{w(MCU\_RESETSTATzL)}$	Pulse Width, MCU_RESETSTATz low (SW_MCU_WARMRST)	966*S(1)		ns
RST9	$t_{w(RESETSTATzL)}$	Pulse Width, RESETSTATz low (SW_MCU_WARMRST, SW_MAIN_PORz, or SW_MAIN_WARMRST)	4040*S		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

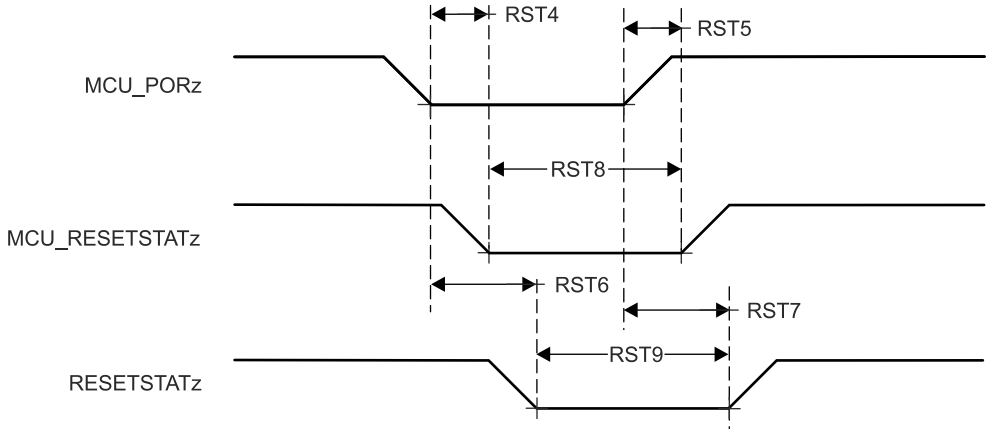

Figure 6-8. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

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Table 6-9. MCU_RESETz Timing Requirements

see Figure 6-9

NO.	PARAMETER		MIN	MAX	UNIT
RST10	$t_{w(MCU\_RESETzL)}$ (1)	Pulse Width, MCU_RESETz active (low)	1200		ns

(1) This timing parameter is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

Table 6-10. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see Figure 6-9

NO.	PARAMETER		MIN	MAX	UNIT
RST11	$t_{d(MCU\_RESETzL-MCU\_RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)	0		ns
RST12	$t_{d(MCU\_RESETzH-MCU\_RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high)	966*S(1)		ns
RST13	$t_{d(MCU\_RESETzL-RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to RESETSTATz active (low)	960		ns
RST14	$t_{d(MCU\_RESETzH-RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)	4040*S(1)		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

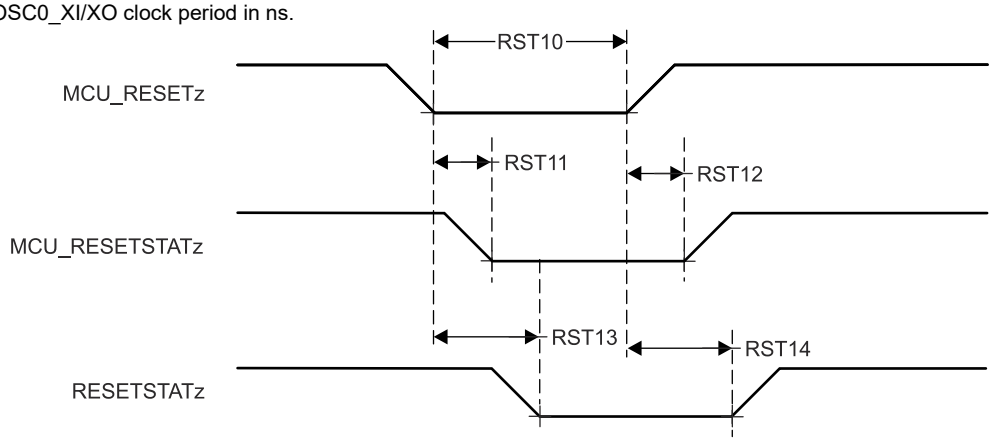

Figure 6-9. MCU_RESETz, MCU_RESETSTATz, and RESETSTATz Timing Requirements and Switching Characteristics

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Table 6-11. RESET_REQz Timing Requirements

see Figure 6-10

NO.	PARAMETER		MIN	MAX	UNIT
RST15	$t_{w(RESET\_REQzL)}$ (1)	Pulse Width, RESET_REQz active (low)	1200		ns

(1) This timing parameter is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

Table 6-12. RESETSTATz Switching Characteristics

see Figure 6-10

NO.	PARAMETER		MIN	MAX	UNIT
RST16	$t_{d(RESET\_REQzL-RESETSTATzL)}$	Delay time, RESET_REQz active (low) to RESETSTATz active (low)	900*T(1)		ns
RST17	$t_{d(RESET\_REQzH-RESETSTATzH)}$	Delay time, RESET_REQz inactive (high) to RESETSTATz inactive (high)	4040*S(2)		ns

(1) T = Reset Isolation Time (Software Dependent)
(2) S = MCU_OSC0_XI/XO clock period in ns.

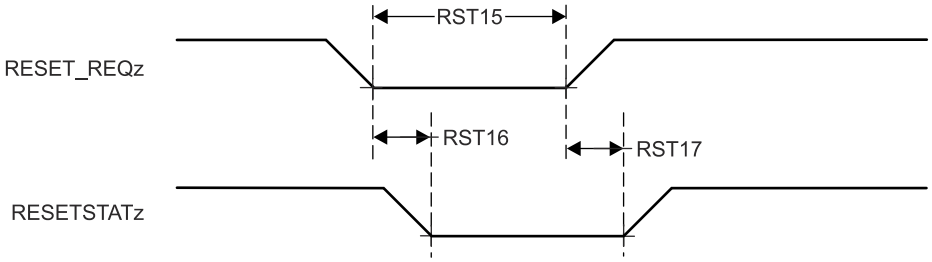

Figure 6-10. RESET_REQz and RESETSTATz Timing Requirements and Switching Characteristics

Table 6-13. EMUx Timing Requirements

see Figure 6-11

NO.	PARAMETER		MIN	MAX	UNIT
RST18	$t_{su(EMUx-MCU\_PORz)}$	Setup time, EMU[1:0] before MCU_PORz inactive (high)	3*S(1)		ns
RST19	$t_{h(MCU\_PORz - EMUx)}$	Hold time, EMU[1:0] after MCU_PORz inactive (high)	10		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

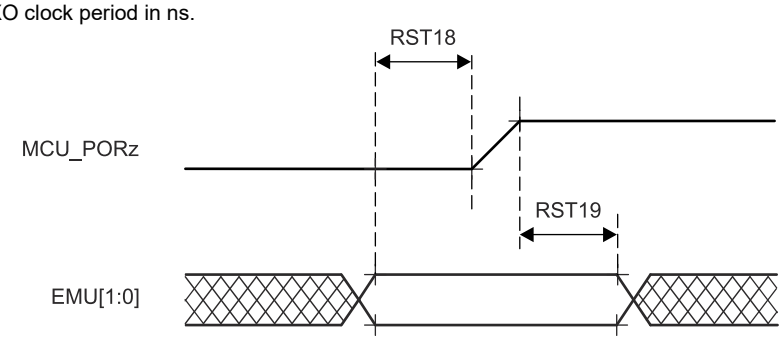

Figure 6-11. EMUx Timing Requirements

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Table 6-14. BOOTMODE Timing Requirements

see Figure 6-12

NO.	PARAMETER		MIN	MAX	UNIT
RST23	$t_{su(BOOTMODE-PORz\_OUT)}$	Setup time, BOOTMODE[15:00] valid before PORz_OUT high (External MCU PORz event or Software SW_MAIN_PORz)	3*S(1)		ns
RST24	$t_{h(PORz\_OUT - BOOTMODE)}$	Hold time, BOOTMODE[15:00] valid after PORz_OUT high (External MCU PORz event, or Software SW_MAIN_PORz)	0		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

Table 6-15. PORz_OUT Switching Characteristics

see Figure 6-12

NO.	PARAMETER		MIN	MAX	UNIT
RST25	$t_{d(MCU\_PORzL-PORz\_OUT)}$	Delay time, MCU_PORz active (low) to PORz_OUT active (low)	0		ns
RST26	$t_{d(MCU\_PORzH-PORz\_OUT)}$	Delay time, MCU_PORz inactive (high) to PORz_OUT inactive (high)	1840		ns
RST27	$t_{w(PORz\_OUTL)}$	Pulse Width, PORz_OUT low (MCU_PORz or SW_MAIN_PORz)	1200		ns

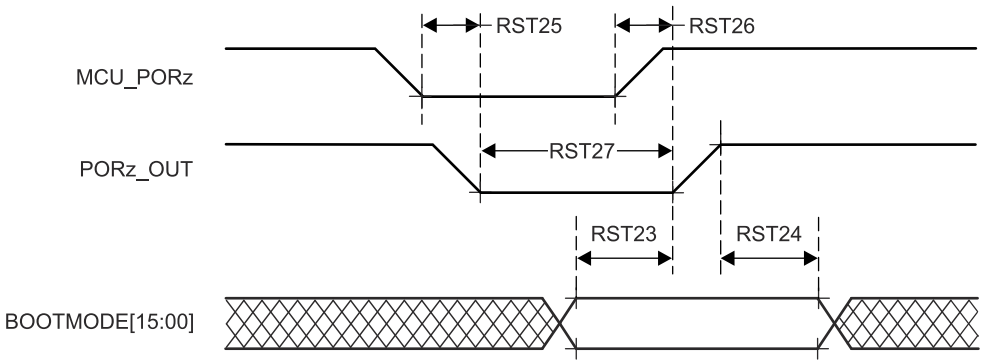

Figure 6-12. BOOTMODE Timing Requirements and PORz_OUT Switching Characteristics

6.9.3.2 Error Signal Timing

Tables and figures provided in this section define timing conditions and switching characteristics for MCU_ERRORn.

Table 6-16. Error Signal Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output load capacitance		30	pF

Table 6-17. MCU_ERRORn Switching Characteristics

see Figure 6-13

NO.	PARAMETER		MIN	MAX	UNIT
ERR1	$t_{c(MCU\_ERRORn)}$	Cycle time minimum, MCU_ERRORn (PWM mode enabled)	(P*H)+(P*L)(1) (3) (4)		ns
ERR2	$t_{w(MCU\_ERRORn)}$	Pulse width minimum, MCU_ERRORn active (PWM mode disabled)(5)	P*R(1) (2)		ns
ERR3	$t_{d\ (ERROR\_CONDITION-MCU\_ERRORnL)}$	Delay time, ERROR CONDITION to MCU_ERRORn active(5)	50*P(1)		ns

(1) P = ESM functional clock period in ns.
(2) R = Error Pin Counter Pre-Load Register count value.
(3) H = Error Pin PWM High Pre-Load Register count value.
(4) L = Error Pin PWM Low Pre-Load Register count value.
(5) When PWM mode is enabled, MCU_ERRORn stops toggling after ERR3 and will maintain its value (either high or low) until the error is cleared. When PWM mode is disabled, MCU_ERRORn is active low.

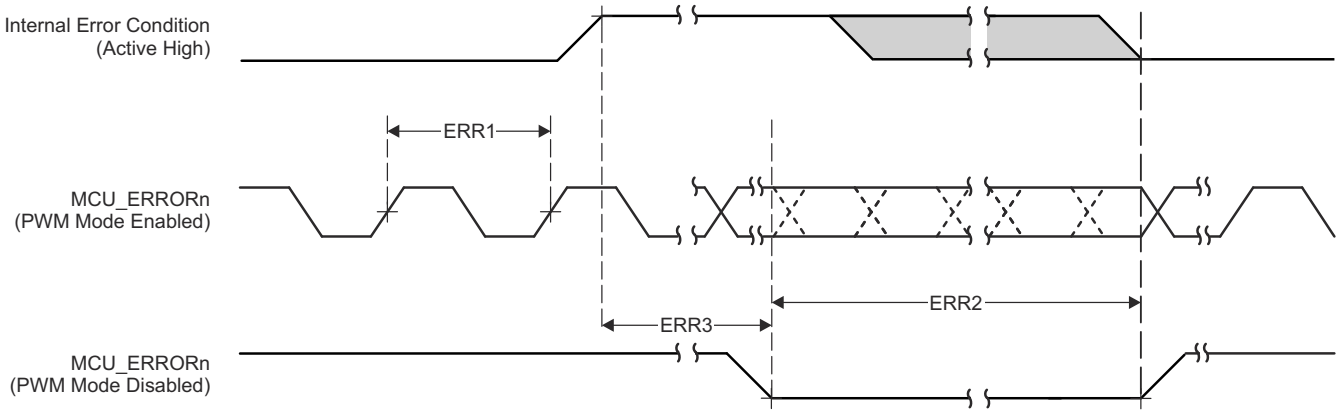

Figure 6-13. MCU_ERRORn Timing Requirements and Switching Characteristics

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6.9.3.3 Clock Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for clock signals.

Table 6-18. Clock Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		0.5		V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	5ns ≤ t_c < 8ns		5	pF
		8ns ≤ t_c < 20ns		10	pF
		20ns ≤ t_c		30	pF

Table 6-19. Clock Timing Requirements

see Figure 6-14

NO.			MIN	MAX	UNIT
CLK1	$t_{c(EXT\_REFCLK1)}$	Cycle time minimum, EXT_REFCLK1	10		ns
CLK2	$t_{w(EXT\_REFCLK1H)}$	Pulse Duration, EXT_REFCLK1 high	E*0.45(1)	E*0.55(1)	ns
CLK3	$t_{w(EXT\_REFCLK1L)}$	Pulse Duration, EXT_REFCLK1 low	E*0.45(1)	E*0.55(1)	ns
CLK1	$t_{c(MCU\_EXT\_REFCLK0)}$	Cycle time minimum, MCU_EXT_REFCLK0	10		ns
CLK2	$t_{w(MCU\_EXT\_REFCLK0H)}$	Pulse Duration, MCU_EXT_REFCLK0 high	F*0.45(2)	F*0.55(2)	ns
CLK3	$t_{w(MCU\_EXT\_REFCLK0L)}$	Pulse Duration, MCU_EXT_REFCLK0 low	F*0.45(2)	F*0.55(2)	ns
CLK1	$t_{c(AUDIO\_EXT\_REFCLK0)}$	Cycle time minimum, AUDIO_EXT_REFCLK0	20		ns
CLK2	$t_{w(AUDIO\_EXT\_REFCLK0H)}$	Pulse Duration, AUDIO_EXT_REFCLK0 high	G*0.45(3)	G*0.55(3)	ns
CLK3	$t_{w(AUDIO\_EXT\_REFCLK0L)}$	Pulse Duration, AUDIO_EXT_REFCLK0 low	G*0.45(3)	G*0.55(3)	ns
CLK1	$t_{c(AUDIO\_EXT\_REFCLK1)}$	Cycle time minimum, AUDIO_EXT_REFCLK1	20		ns
CLK2	$t_{w(AUDIO\_EXT\_REFCLK1H)}$	Pulse Duration, AUDIO_EXT_REFCLK1 high	H*0.45(4)	H*0.55(4)	ns
CLK3	$t_{w(AUDIO\_EXT\_REFCLK1L)}$	Pulse Duration, AUDIO_EXT_REFCLK1 low	H*0.45(4)	H*0.55(4)	ns

(1) E = EXT_REFCLK1 cycle time in ns.
(2) F = MCU_EXT_REFCLK0 cycle time in ns.
(3) G = AUDIO_EXT_REFCLK0 cycle time in ns.
(4) H = AUDIO_EXT_REFCLK1 cycle time in ns.

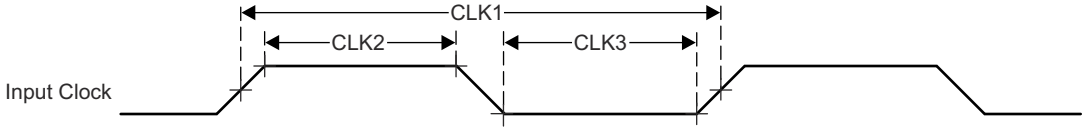

Figure 6-14. Clock Timing Requirements

Table 6-20. Clock Switching Characteristics

see Figure 6-15

NO.	PARAMETER		MIN	MAX	UNIT
CLK4	$t_{c(SYSCLKOUT0)}$	Cycle time minimum,SYSCLKOUT0	8		ns
CLK5	$t_{w(SYSCLKOUT0H)}$	Pulse Duration, SYSCLKOUT0 high	A*0.4(1)	A*0.6(1)	ns
CLK6	$t_{w(SYSCLKOUT0L)}$	Pulse Duration, SYSCLKOUT0 low	A*0.4(1)	A*0.6(1)	ns
CLK4	$t_{c(OBSCLK0)}$	Cycle time minimum, OBSCLK0	5		ns
CLK5	$t_{w(OBSCLK0H)}$	Pulse Duration, OBSCLK0 high	B*0.45(2)	B*0.55(2)	ns
CLK6	$t_{w(OBSCLK0L)}$	Pulse Duration, OBSCLK0 low	B*0.45(2)	B*0.55(2)	ns
CLK4	$t_{c(OBSCLK1)}$	Cycle time minimum, OBSCLK1	5		ns
CLK5	$t_{w(OBSCLK1H)}$	Pulse Duration, OBSCLK1 high	F*0.45(3)	F*0.55(3)	ns
CLK6	$t_{w(OBSCLK1L)}$	Pulse Duration, OBSCLK1 low	F*0.45(3)	F*0.55(3)	ns
CLK4	$t_{c(CLKOUT0)}$	Cycle time minimum, CLKOUT0	20		ns
CLK5	$t_{w(CLKOUT0H)}$	Pulse Duration, CLKOUT0 high	C*0.4(4)	C*0.6(4)	ns
CLK6	$t_{w(CLKOUT0L)}$	Pulse Duration, CLKOUT0 low	C*0.4(4)	C*0.6(4)	ns
CLK4	$t_{c(MCU\_SYSCLKOUT0)}$	Cycle time minimum, MCU_SYSCLKOUT0	10		ns
CLK5	$t_{w(MCU\_SYSCLKOUT0H)}$	Pulse Duration, MCU_SYSCLKOUT0 high	E*0.4(5)	E*0.6(5)	ns
CLK6	$t_{w(MCU\_SYSCLKOUT0L)}$	Pulse Duration, MCU_SYSCLKOUT0 low	E*0.4(5)	E*0.6(5)	ns
CLK4	$t_{c(MCU\_OBSCLK0)}$	Cycle time minimum, MCU_OBSCLK0	5		ns
CLK5	$t_{w(MCU\_OBSCLK0H)}$	Pulse Duration, MCU_OBSCLK0 high	D*0.45(6)	D*0.55(6)	ns
CLK6	$t_{w(MCU\_OBSCLK0L)}$	Pulse Duration, MCU_OBSCLK0 low	D*0.45(6)	D*0.55(6)	ns
CLK4	$t_{c(WKUP\_CLKOUT0)}$	Cycle time minimum, WKUP_CLKOUT0	5		ns
CLK5	$t_{w(WKUP\_CLKOUT0H)}$	Pulse Duration, WKUP_CLKOUT0 high	W*0.4(7)	W*0.6(7)	ns
CLK6	$t_{w(WKUP\_CLKOUT0L)}$	Pulse Duration, WKUP_CLKOUT0 low	W*0.4(7)	W*0.6(7)	ns
CLK4	$t_{c(AUDIO\_EXT\_REFCLK0\ )}$	Cycle time minimum, AUDIO_EXT_REFCLK0 (McASP Clock Source)	20		ns
		Cycle time minimum, AUDIO_EXT_REFCLK0 (PLL Clock Source)	10		ns
CLK5	$t_{w(AUDIO\_EXT\_REFCLK0\ H)}$	Pulse Duration, AUDIO_EXT_REFCLK0 high	G*0.4(8)	G*0.6(8)	ns
CLK6	$t_{w(AUDIO\_EXT\_REFCLK0\ L)}$	Pulse Duration, AUDIO_EXT_REFCLK0 low	G*0.4(8)	G*0.6(8)	ns
CLK4	$t_{c(AUDIO\_EXT\_REFCLK1\ )}$	Cycle time minimum, AUDIO_EXT_REFCLK1 (McASP Clock Source)	20		ns
		Cycle time minimum, AUDIO_EXT_REFCLK1 (PLL Clock Source)	10		ns
CLK5	$t_{w(AUDIO\_EXT\_REFCLK1\ H)}$	Pulse Duration, AUDIO_EXT_REFCLK1 high	J*0.4(9)	J*0.6(9)	ns
CLK6	$t_{w(AUDIO\_EXT\_REFCLK1\ L)}$	Pulse Duration, AUDIO_EXT_REFCLK1 low	J*0.4(9)	J*0.6(9)	ns

(1) A = SYSCLKOUT0 cycle time in ns.
(2) B = OBSCLK0 cycle time in ns.
(3) F = OBSCLK1 cycle time in ns.
(4) C = CLKOUT0 cycle time in ns.
(5) E = MCU_SYSCLKOUT0 cycle time in ns.
(6) D = MCU_OBSCLK0 cycle time in ns.
(7) W = WKUP_CLKOUT0 cycle time in ns.
(8) G = AUDIO_EXT_REFCLK0 cycle time in ns.
(9) J = AUDIO_EXT_REFCLK1 cycle time in ns.

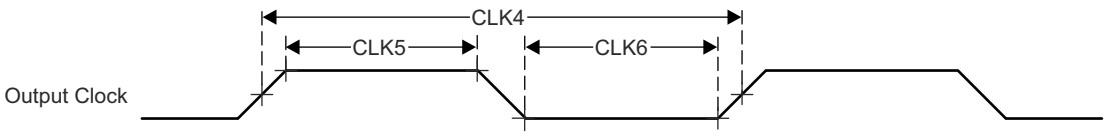

Figure 6-15. Clock Switching Characteristics

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6.9.4 Clock Specifications

6.9.4.1 Input Clocks / Oscillators

Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- MCU_OSC0_XO/MCU_OSC0_XI — external main crystal interface pins connected to the internal high-frequency oscillator (MCU_HFOSC0), which is the default clock source for internal reference clock HFOSC0_CLKOUT.
- WKUP_LFOSC0_XO/WKUP_LFOSC0_XI — external crystal interface pins connected to internal low-frequency oscillator (WKUP_LFOSC0), which sources optional 32768Hz reference clock.
- General purpose clock inputs
  - MCU_EXT_REFCLK0 — optional external system clock.
  - EXT_REFCLK1 — optional external system clock.
- External CPTS reference clock input
  - CP_GEMAC_CPTS0_RFT_CLK — optional reference clock input for CPTS_RFT_CLK.
- External audio reference clock inputs/outputs
  - AUDIO_EXT_REFCLK[1:0] — optional McASP high-frequency input clocks when configured to operate as an input.

For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

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6.9.4.1.1 MCU_OSC0 Internal Oscillator Clock Source

Figure 6-16 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit must be placed as close as possible to the MCU_OSC0_XI and MCU_OSC0_XO pins.

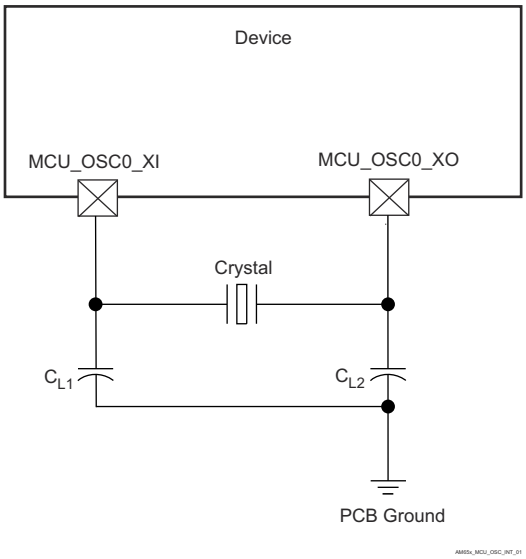

Figure 6-16. MCU_OSC0 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-21 summarizes the required electrical constraints.

Table 6-21. MCU_OSC0 Crystal Circuit Requirements

PARAMETER				MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency				25		MHz
F_{xtal}	Crystal Frequency Stability and Tolerance		Ethernet RGMII and RMII not used			±100	ppm
			Ethernet RGMII and RMII using derived clock			±50	
$C_{L1+PCBXI}$	Capacitance of C_{L1} + C_{PCBXI}			12		24	pF
$C_{L2+PCBXO}$	Capacitance of C_{L2} + C_{PCBXO}			12		24	pF
C_L	Crystal Load Capacitance			6		12	pF
C_{shunt}	Crystal Circuit Shunt Capacitance	ESR_{xtal} = 30Ω	25MHz			7	pF
		ESR_{xtal} = 40Ω	25MHz			5	pF
		ESR_{xtal} = 50Ω	25MHz			5	pF
ESR_{xtal}	Crystal Effective Series Resistance					(1)	Ω

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C_{shunt} parameter.

When selecting a crystal, the system design must consider temperature and aging characteristics of the crystal based on worst case environment and expected life expectancy of the system.

Table 6-22 details the switching characteristics of the oscillator.

Table 6-22. MCU_OSC0 Switching Characteristics - Crystal Mode

PARAMETER		MIN	TYP	MAX	UNIT
C_{XI}	XI Capacitance			2.04	pF
C_{XO}	XO Capacitance			1.91	pF
C_{XIXO}	XI to XO Mutual Capacitance			0.01	pF

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Table 6-22. MCU_OSC0 Switching Characteristics - Crystal Mode (continued)

PARAMETER		MIN	TYP	MAX	UNIT
t_s	Start-up Time		4		ms

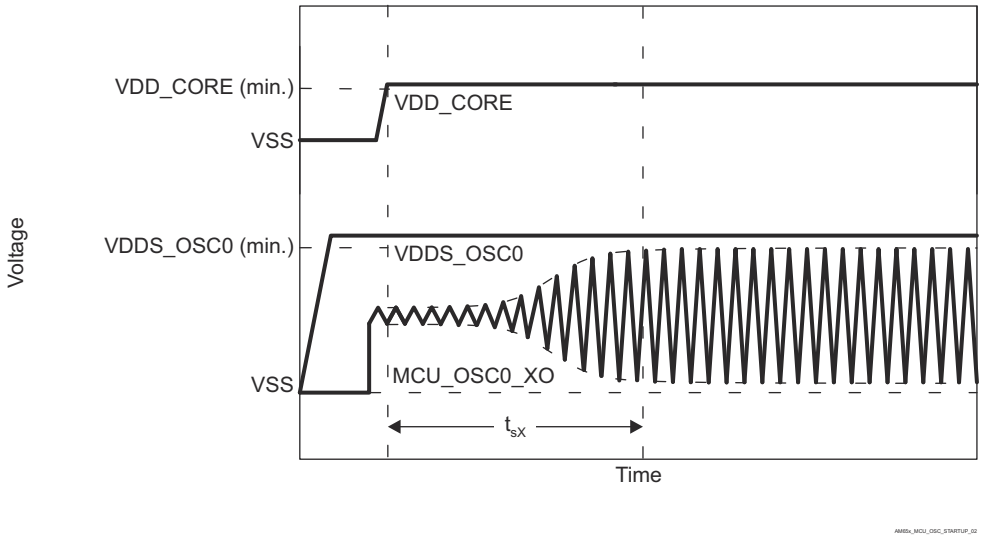

Figure 6-17. MCU_OSC0 Start-up Time

6.9.4.1.1.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C_L, of this circuit is a combination of discrete capacitors C_{L1}, C_{L2}, and several parasitic contributions. PCB signal traces which connect crystal circuit components to MCU_OSC0_XI and MCU_OSC0_XO have parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where the PCB designer should be able to extract parasitic capacitance for each signal trace. The MCU_OSC0 circuits and device package have combined parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where these parasitic capacitance values are defined in Table 6-22.

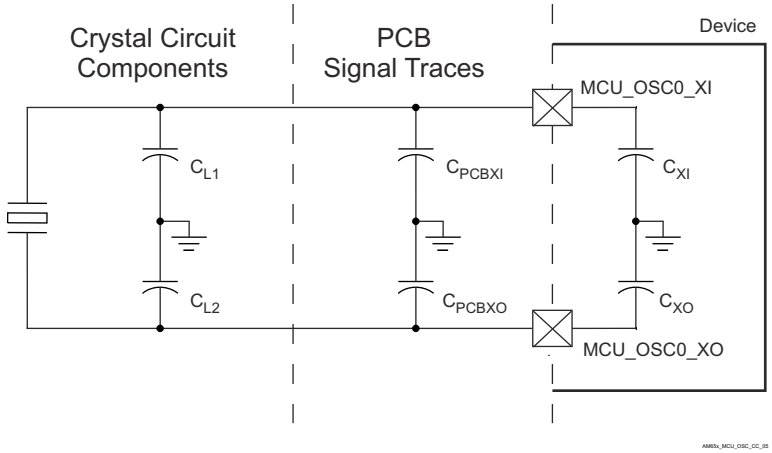

Figure 6-18. Load Capacitance

Load capacitors, C_{L1} and C_{L2} in Figure 6-16, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

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To determine the value of C_{L1} and C_{L2}, multiply the capacitive load value C_L by 2. Using this result, subtract the combined values of C_{PCBXI} + C_{XI} to determine the value of C_{L1} and the combined values of C_{PCBXO} + C_{XO} to determine the value of C_{L2}. For example, if C_L = 10pF, C_{PCBXI} = 2.9pF, C_{XI} = 0.5pF,C_{PCBXO} = 3.7pF, C_{XO} = 0.5pF, the value of C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 × 10pF) - 2.9pF - 0.5pF)] = 16.6pF and C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 × 10pF) - 3.7pF - 0.5pF)] = 15.8pF

6.9.4.1.1.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for MCU_OSC0 operating conditions defined in Table 6-21. Shunt capacitance, C_{shunt}, of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to MCU_OSC0 have mutual parasitic capacitance to each other, $C_{PCBXIXO}$, where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance, C_{XIXO}, where this mutual parasitic capacitance value is defined in Table 6-22.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

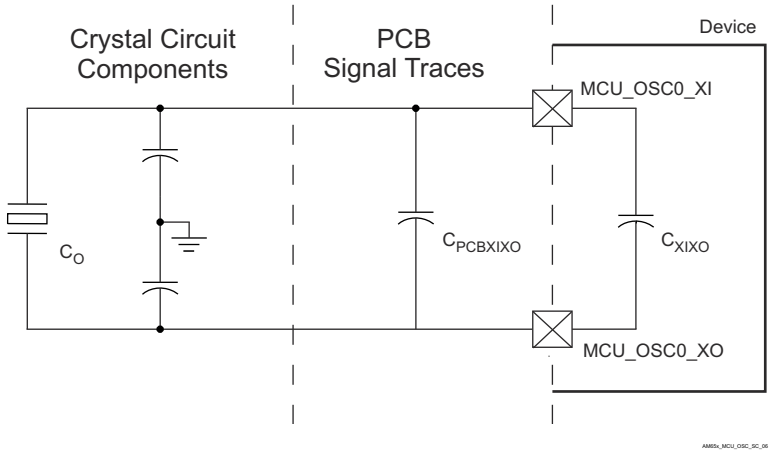

Figure 6-19. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied. C_O in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$

For example, the equation would be satisfied when the crystal being used is 25MHz with an ESR = 30Ω, $C_{PCBXIXO}$ = 0.04pF, C_{XIXO} = 0.01pF, and shunt capacitance of the crystal is less than or equal to 6.95pF.

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6.9.4.1.2 MCU_OSC0 LVCMOS Digital Clock Source

Figure 6-20 shows the recommended oscillator connections when MCU_OSC0_XI is connected to a 1.8V LVCMOS square-wave digital clock source.

Note

1. A DC steady-state condition is not allowed on MCU_OSC0_XI when the oscillator is powered up. This is not allowed because MCU_OSC0_XI is internally AC coupled to a comparator that can enter an unknown state when DC is applied to the input. Therefore, application software must power down MCU_OSC0 any time MCU_OSC0_XI is not toggling between logic states.

2. The LVCMOS clock signal sourcing the MCU_OSC0_XI input must have monotonic transitions. The clock source should be connected to MCU_OSC0_XI with a point-to-point connection, via a series termination resistor placed near the clock source. The series termination resistor value should match the clock source output impedance to the transmission line impedance. For example, the series termination resistor value needs to be 20 ohms if the clock source has an output impedance of 30 ohms and the PCB signal trace has a characteristic impedance of 50 ohms. This allows the reflection that returns from the far end of the un-terminated transmission line to be completely absorbed such that is does not introduce any non-monotonic events on the signal.

3. The PCB trace length connecting the LVCMOS clock source to MCU_OSC0_XI should be minimized. This reduces capacitive loading and decreases probability of external noise sources coupling into the clock signal. Reduced capacitive loading improves rise/fall times of the clock signal which reduces the probability of jitter being introduced in the system.

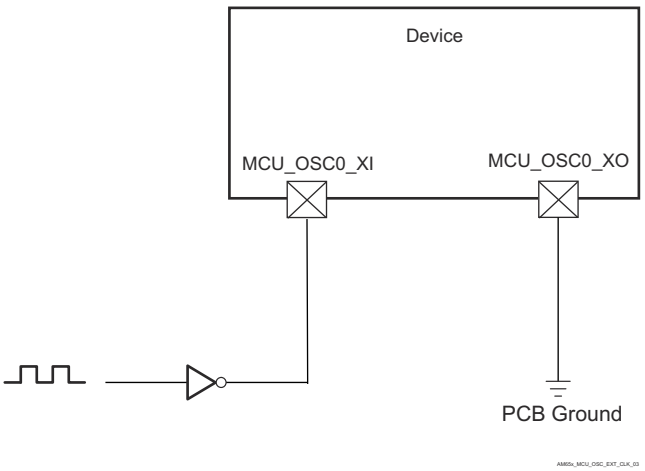

Figure 6-20. 1.8V LVCMOS-Compatible Clock Input

Table 6-23. MCU_OSC0 LVCMOS Digital Clock Source Requirements

PARAMETER			MIN	TYP	MAX	UNIT
F_{xtal}	Frequency			25		MHz
	Frequency Stability and Tolerance	Ethernet RGMII and RMII not used			±100	ppm
		Ethernet RGMII and RMII using derived clock			±50	
DC	Duty Cycle		45		55	%
$t_{R/F}$	Rise/Fall Time (10%-90% rise, 90%-10% fall)				4(1)	ns
$J_{Period(RMS)}$	Period Jitter, RMS (100k samples)				20	ps
$J_{Period(PK-PK)}$	Period Jitter, Peak to Peak (100k samples)				300	ps
$J_{Phase(RMS)}$	Phase Jitter, RMS (BW 100Hz to 1MHz)				10(2)	ps

(1) Most LVCMOS oscillator datasheets define their maximum Output Rise/Fall times with a capacitive load much larger than the actual load that will be applied by the combined PCB trace capacitance and MCU_OSC0_XI input capacitance. It should not be difficult to find a LVCMOS oscillator that meets this requirement. However, the system designer must confirm the LVCMOS oscillator selected will provide the appropriate rise/fall time to MCU_OSC0_XI input.

(2) Most LVCMOS oscillator datasheets define their max RMS Phase Jitter using a larger bandwidth integration range than required by this device. To get a more appropriate value, it may be necessary to contact the LVCMOS oscillator manufacture and ask them to provide a maximum RMS Phase Jitter using the same bandwidth integration range that has been defined for this parameter.

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6.9.4.1.3 WKUP_LFOSC0 Internal Oscillator Clock Source

Figure 6-21 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors R_{bias} and R_d in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, R_{bias} is not required and R_d is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

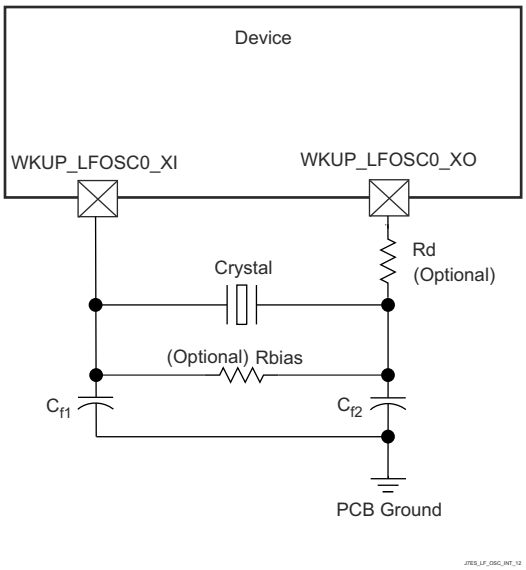

Figure 6-21. WKUP_LFOSC0 Crystal Implementation

Table 6-24 presents LFXOSC modes of operation.

Table 6-24. LFXOSC Modes of Operation

MODE	BP_C	PD_C	XI	XO	CLK_OUT	DESCRIPTION
ACTIVE	0	0	XTAL	XTAL	CLK_OUT	Active oscillator mode providing 32kHz
PWRDN	0	1	X	PD	LOW	Output will be pulled down to LOW. PAD to be tri-stated. Active mode disabled
BYPASS	1	0	CLK	PD	CLK	XI is driven by external clock source. XO is pulled down to LOW. Due to ESD diode to supply, XI should not be driven unless oscillator supply is present.

Note

User should set CTRLMMR_WKUP_LFXOSC_TRIM[18:16] i_mult = 3b'001 for CL in the range 6pf to 9.5pf. CTRLMMR_WKUP_LFXOSC_TRIM [18:16] i_mult = 3b'010 for CL in the range 8.5pf to 12pf. Default setting is 3b'010.

Note

The load capacitors, C_{f1} and C_{f2} in Figure 6-22, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator WKUP_LFOSC0_XI, WKUP_LFOSC0_XO, and VSS pins.

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$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

JTES_CL_MATH_03

Figure 6-22. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-25 summarizes the required electrical constraints.

Table 6-25. WKUP_LFOSC0 Crystal Electrical Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency			32768		Hz
	Crystal Frequency Stability and Tolerance				±100	PPM
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
C_{shunt}	Shunt capacitance	ESRxtal – 40 kΩ			4	pF
		ESRxtal – 60 kΩ			3	pF
		ESRxtal – 80 kΩ			2	pF
		ESRxtal – 100 kΩ			1	pF
ESR	Crystal effective series resistance				(1)	Ω

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C_{shunt} parameter.

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

Table 6-26 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 6-26. WKUP_LFOSC0 Switching Characteristics – Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_{xtal}	Oscillation frequency		32768		Hz
t_{sX}	Start-up time			96.5	ms

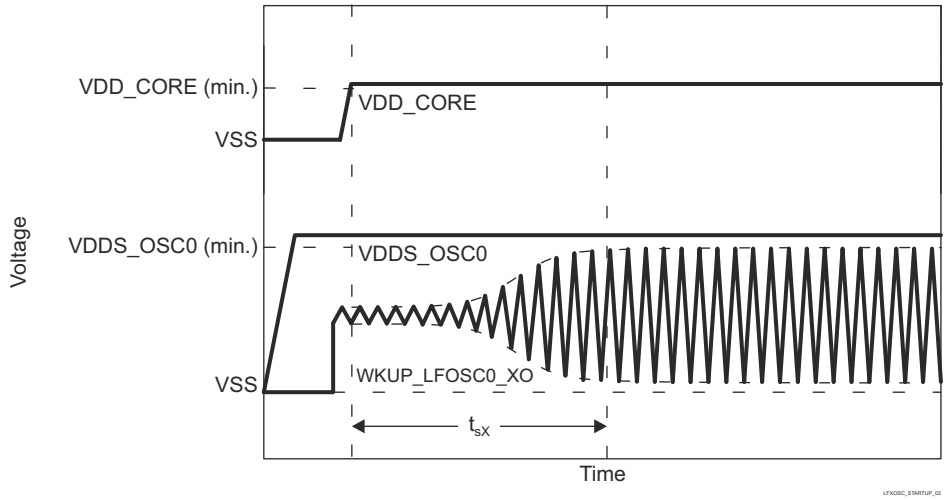

Figure 6-23. WKUP_LFOSC0 Start-up Time

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6.9.4.1.4 WKUP_LFOSC0 LVCMOS Digital Clock Source

Figure 6-24 shows the recommended oscillator connections when WKUP_LFOSC0_XI is connected to a 1.8V LVCMOS square-wave digital clock source.

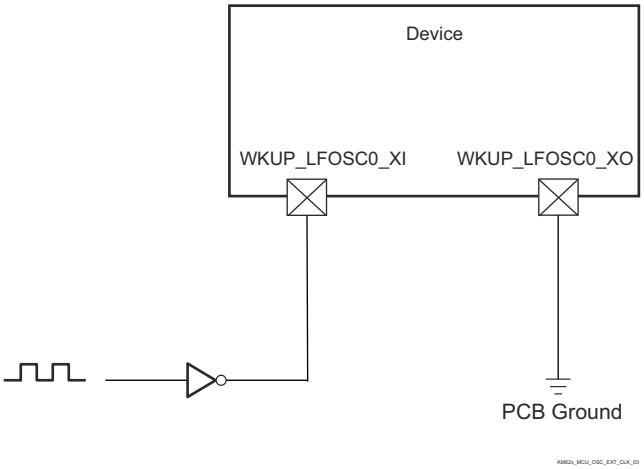

Figure 6-24. 1.8V LVCMOS-Compatible Clock Input

6.9.4.1.5 WKUP_LFOSC0 Not Used

Figure 6-25 shows the recommended oscillator connections when WKUP_LFOSC0 is not used.

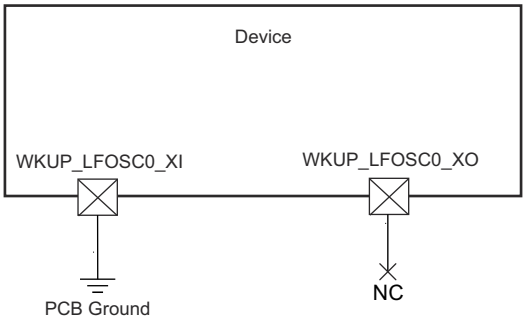

Figure 6-25. WKUP_LFOSC0 Not Used

6.9.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU_SYSCLKOUT0**
  - MCU_PLL0_HSDIV0_CLKOUT (MCU_SYSCLKOUT0) divided by 4 and sent out of the device as MCU_SYSCLKOUT0. This clock output is provided for test and debug purposes only.
- **MCU_OBSCLK0**
  - Observation clock output for test and debug purposes only.
- **WKUP_CLKOUT0**
  - WKUP domain CLKOUT0 output.
- **SYSCLKOUT0**
  - MAIN_PLL0_HSDIV0_CLKOUT (SYSCLKOUT0) divided by 4 and then sent out of the device as SYSCLKOUT0. This clock output is provided for test and debug purposes only.
- **CLKOUT0**
  - CLKOUT0 is the Ethernet subsystem clock (MAIN_PLL2_HSDIV1_CLKOUT) divided-by-5 or divided-by-10. This clock output was provided as an optional source to the external PHY. When configured to operate as the RMII Clock source (50MHz) the signal must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.
- **OBSCLK[1:0]**
  - Observation clock outputs for test and debug purposes only.
- **AUDIO_EXT_REFCLK[1:0]**
  - Option of sourcing one of six McASP high-frequency audio reference clocks, MAIN_PLL1_HSDIV6_CLKOUT, or MAIN_PLL2_HSDIV8_CLKOUT when configured to operate as an output.

6.9.4.3 PLLs

Power is supplied to the Phase-Locked Loop circuits (PLLs) by internal regulators that derive their power from off-chip power-sources.

There is one PLL in the MCU domain:

- MCU PLL

There are nine PLLs in the MAIN domain:

- MAIN PLL
- PER0 PLL
- PER1 PLL
- GPU PLL
- ARM0 PLL
- DDR PLL
- SMS PLL
- DSS PLL0
- DSS PLL1
- DSS PLL2

The system designer should consider the reference clock source start-up time and the PLL lock requirements before configuring and using any of the PLL outputs as clock sources. The device reference clock input requirements are defined in Section 6.9.4.1, *Input Clocks / Oscillators*. PLL configuration details are described in the device TRM.

For more information on PLLs, see the *PLL* subsection in the *Clocking* subsection of the *Device Configuration* section in the device TRM.

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6.9.4.4 Recommended System Precautions for Clock and Control Signal Transitions

All clock and strobe signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Monotonic transitions are more likely to occur with fast signal transitions. It is easy for noise to create non-monotonic events on a signal with slow transitions. Therefore, avoid slow signal transitions on all clock and control signals since they are more likely to generate glitches inside the device.

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6.9.5 Peripherals

6.9.5.1 ATL

The device contains ATL module that can be used for asynchronous sample rate conversion of audio. The ATL calculates the error between two time bases, such as audio syncs, and optionally generates an averaged clock using cycle stealing via software.

Note

For more information about ATL, see *Audio Tracking Logic (ATL)* section in *Peripherals* chapter in the device TRM.

Table 6-27 represents ATL timing conditions.

Table 6-27. ATL Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	External reference CLK	0.5	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	Internal reference CLK	1	10	pF

Section 6.9.5.1.1, Section 6.9.5.1.2, Section 6.9.5.1.3, and Section 6.9.5.1.4 present timing requirements and switching characteristics for ATL.

6.9.5.1.1 ATL_PCLK Timing Requirements

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D1	$t_{c(pclk)}$	Cycle time, ATL_PCLK	External reference CLK	5		ns
D2	$t_{w(pclkL)}$	Pulse Duration, ATL_PCLK low	External reference CLK	0.45 × M(1) + 2.5		ns
D3	$t_{w(pclkH)}$	Pulse Duration, ATL_PCLK high	External reference CLK	0.45 × M(1) + 2.5		ns

(1) M = ATL_CLK[x] period

6.9.5.1.2 ATL_AWS[x] Timing Requirements

NO.			MODE	MIN	MAX	UNIT
D4	$t_{c(aws)}$	Cycle Time, ATL_AWS[x](3)	External reference CLK	2 × M(1)		ns
D5	$t_{w(awsL)}$	Pulse Duration, ATL_AWS[x](3) low	External reference CLK	0.45 × A(2) + 2.5		ns
D6	$t_{w(awsH)}$	Pulse Duration, ATL_AWS[x](3) high	External reference CLK	0.45 × A(2) + 2.5		ns

(1) M = ATL_CLK[x] period
(2) A = ATL_AWS[x] period
(3) x = 0 to 3

6.9.5.1.3 ATL_BWS[x] Timing Requirements

NO.			MODE	MIN	MAX	UNIT
D7	$t_{c(bws)}$	Cycle Time, ATL_BWS[x](3)	External reference clock	2 × M(1)		ns
D8	$t_{w(bwsL)}$	Pulse Duration, ATL_BWS[x] low(3)	External reference clock	0.45 × B(2) + 2.5		ns

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NO.			MODE	MIN	MAX	UNIT
D9	$t_{w(bwsH)}$	Pulse Duration, ATL_BWS[x] high(3)	External reference clock	0.45 × B(2) + 2.5		ns

(1) M = ATL_CLK[x] period
(2) B = ATL_BWS[x] period
(3) x = 0 to 3

6.9.5.1.4 ATCLK[x] Switching Characteristics

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D10	$t_{c(atclk)}$	Cycle time, ATCLK[x](3)	Internal reference CLK	20		ns
D11	$t_{w(atclkL)}$	Pulse Duration, ATCLK[x] low(3)	Internal reference CLK	0.45 × P(2) - M(1) - 0.3		ns
D12	$t_{w(atclkH)}$	Pulse Duration, ATCLK[x] high(3)	Internal reference CLK	0.45 × P(2) - M(1) - 0.3		ns

(1) M = ATL_CLK[x] period
(2) P = ATCLK[x] period
(3) x = 0 to 3

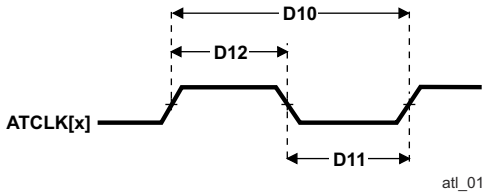

Figure 6-26. ATCLK[x] Timing

6.9.5.2 CPSW3G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.9.5.2.1 CPSW3G MDIO Timing

Table 6-28, Table 6-29, Table 6-30, and Figure 6-27 present timing conditions, timing requirements, and switching characteristics for CPSW3G MDIO.

Table 6-28. CPSW3G MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	10	470	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	0	5	ns
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		1	ns

Table 6-29. CPSW3G MDIO Timing Requirements

see Figure 6-27

NO.	PARAMETER		MIN	MAX	UNIT
MDIO1	$t_{su(MDIO\_MDC)}$	Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high	45		ns
MDIO2	$t_{h(MDC\_MDIO)}$	Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high	0		ns

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Table 6-30. CPSW3G MDIO Switching Characteristics

see Figure 6-27

NO.	PARAMETER		MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO[x]_MDC	400		ns
MDIO4	$t_{w(MDCH)}$	Pulse Duration, MDIO[x]_MDC high	160		ns
MDIO5	$t_{w(MDCL)}$	Pulse Duration, MDIO[x]_MDC low	160		ns
MDIO7	$t_{d(MDC\_MDIO)}$	Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid	-10	10	ns

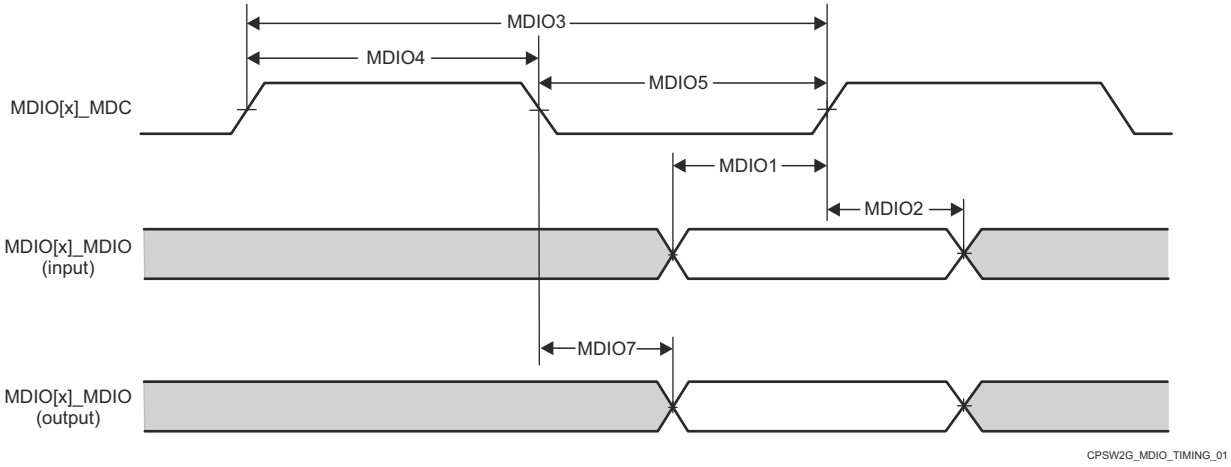

Figure 6-27. CPSW3G MDIO Timing Requirements and Switching Characteristics

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6.9.5.2.2 CPSW3G RMII Timing

Table 6-31, Table 6-32, Figure 6-28, Table 6-33, Figure 6-29, Table 6-34, and Figure 6-30 present timing conditions, timing requirements, and switching characteristics for CPSW3G RMII.

Table 6-31. CPSW3G RMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD(1) = 1.8V	0.18	0.54	V/ns
		VDD(1) = 3.3V	0.4	1.2	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	25	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

Table 6-32. RMII[x]_REF_CLK Timing Requirements – RMII Mode

see Figure 6-28

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	$t_{c(REF\_CLK)}$	Cycle time, RMII[x]_REF_CLK	19.999	20.001	ns
RMII2	$t_{w(REF\_CLKH)}$	Pulse Duration, RMII[x]_REF_CLK High	7	13	ns
RMII3	$t_{w(REF\_CLKL)}$	Pulse Duration, RMII[x]_REF_CLK Low	7	13	ns

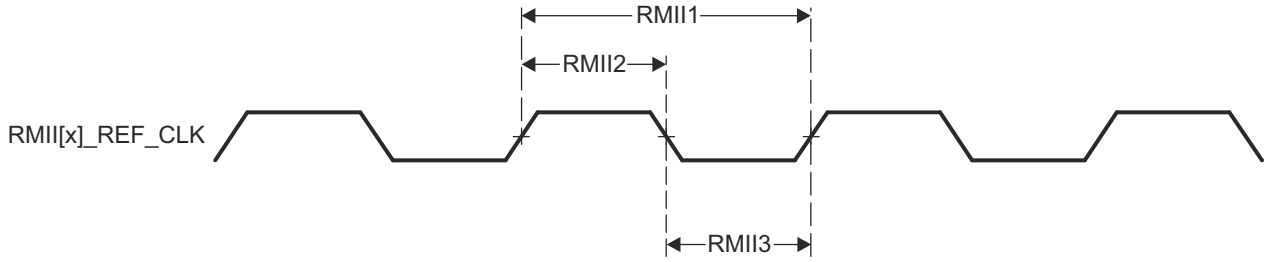

Figure 6-28. CPSW3G RMII[x]_REF_CLK Timing Requirements – RMII Mode

Table 6-33. RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RX_ER Timing Requirements – RMII Mode

see Figure 6-29

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII4	$t_{su(RXD-REF\_CLK)}$	Setup time, RMII[x]_RXD[1:0] valid before RMII[x]_REF_CLK	4		ns
	$t_{su(CRS\_DV-REF\_CLK)}$	Setup time, RMII[x]_CRS_DV valid before RMII[x]_REF_CLK	4		ns
	$t_{su(RX\_ER-REF\_CLK)}$	Setup time, RMII[x]_RX_ER valid before RMII[x]_REF_CLK	4		ns
RMII5	$t_{h(REF\_CLK-RXD)}$	Hold time RMII[x]_RXD[1:0] valid after RMII[x]_REF_CLK	2		ns
	$t_{h(REF\_CLK-CRS\_DV)}$	Hold time, RMII[x]_CRS_DV valid after RMII[x]_REF_CLK	2		ns
	$t_{h(REF\_CLK-RX\_ER)}$	Hold time, RMII[x]_RX_ER valid after RMII[x]_REF_CLK	2		ns

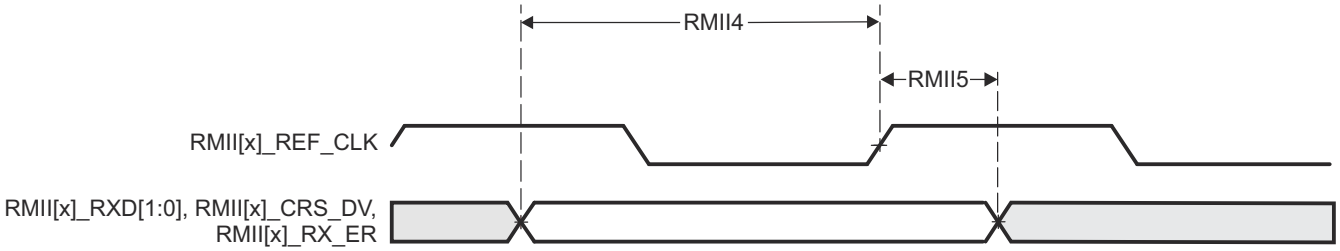

Figure 6-29. CPSW3G RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RX_ER Timing Requirements – RMII Mode

Table 6-34. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

see Figure 6-30

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII6	$t_{d(REF\_CLK-TXD)}$	Delay time, RMII[x]_REF_CLK High to RMII[x]_TXD[1:0] valid	2	10	ns
	$t_{d(REF\_CLK-TX\_EN)}$	Delay time, RMII[x]_REF_CLK to RMII[x]_TX_EN valid	2	10	ns

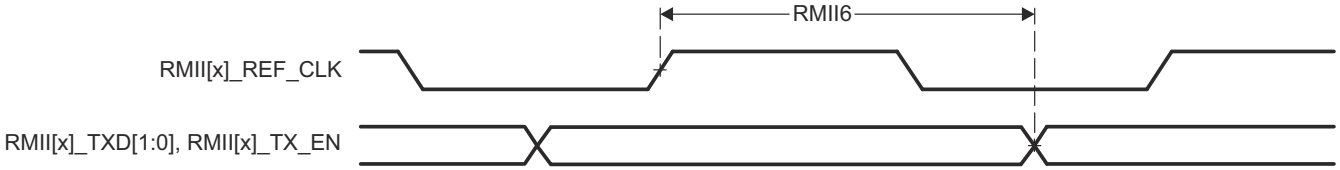

Figure 6-30. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

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6.9.5.2.3 CPSW3G RGMII Timing

Table 6-35, Table 6-36, Table 6-37, Figure 6-31, Table 6-38, Table 6-39, and Figure 6-32 present timing conditions, timing requirements, and switching characteristics for CPSW3G RGMII.

Table 6-35. CPSW3G RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD(1) = 1.8V	1.44	5	V/ns
		VDD(1) = 3.3V	2.64	5	
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC, RGMII[x]_TD[3:0], RGMII[x]_TX_CTL		50	ps

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

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Table 6-36. RGMII[x]_RXC Timing Requirements – RGMII Mode

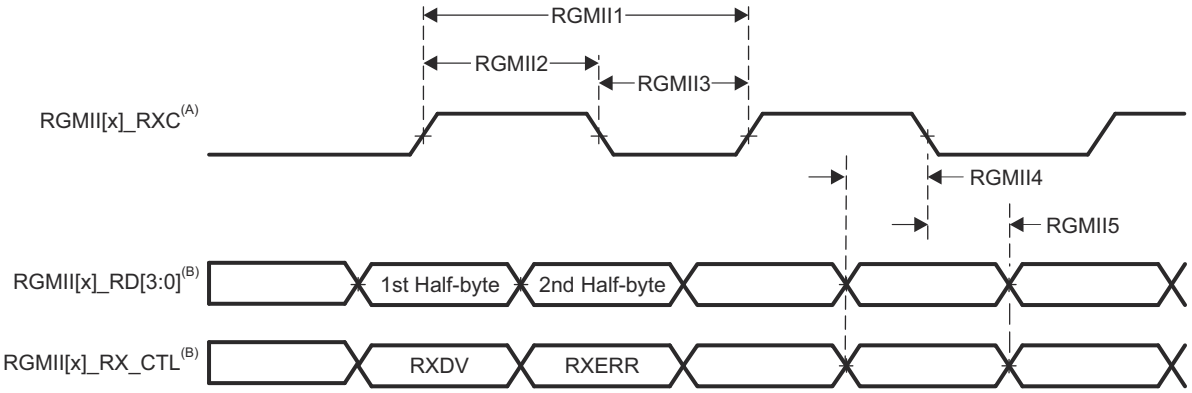
see Figure 6-31

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, RGMII[x]_RXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII2	$t_{w(RXCH)}$	Pulse duration, RGMII[x]_RXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII3	$t_{w(RXCL)}$	Pulse duration, RGMII[x]_RXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

Table 6-37. RGMII[x]_RD[3:0], and RGMII[x]_RX_CTL Timing Requirements – RGMII Mode

see Figure 6-31

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII4	$t_{su(RD-RXC)}$	Setup time, RGMII[x]_RD[3:0] valid before RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{su(RX\_CTL-RXC)}$	Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
RGMII5	$t_{h(RXC-RD)}$	Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{h(RXC-RX\_CTL)}$	Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns



A. RGMII[x]_RXC must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. RGMII[x]_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_RXC and data bits 7-4 on the falling edge of RGMII[x]_RXC. Similarly, RGMII[x]_RX_CTL carries RXDV on rising edge of RGMII[x]_RXC and RXERR on falling edge of RGMII[x]_RXC.

Figure 6-31. CPSW3G RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL Timing Requirements - RGMII Mode

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Table 6-38. RGMII[x]_TXC Switching Characteristics – RGMII Mode

see Figure 6-32

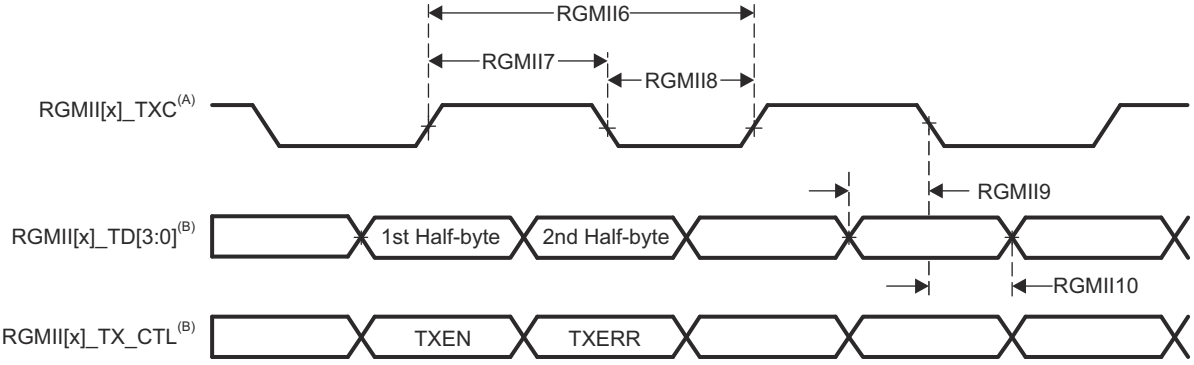
NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII6	$t_{c(TXC)}$	Cycle time, RGMII[x]_TXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII7	$t_{w(TXCH)}$	Pulse duration, RGMII[x]_TXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII8	$t_{w(TXCL)}$	Pulse duration, RGMII[x]_TXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

Table 6-39. RGMII[x]_TD[3:0] and RGMII[x]_TX_CTL Switching Characteristics – RGMII Mode

see Figure 6-32

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(TD-TXC)}$	Output setup time(1), RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{osu(TX\_CTL-TXC)}$	Output setup time(1), RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
RGMII10	$t_{oh(TXC-TD)}$	Output hold time(1), RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{oh(TXC-TX\_CTL)}$	Output hold time(1), RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns

(1) Output setup/hold times are defining a delay relationship of the transmit data and control outputs relative to the transmit clock output, but this output relationship is being presented as the minimum setup/hold times provided to the attached receiver. This approach matches how the output timing relationships are defined in the RGMII specification.



A. TXC is delayed internally before being driven to the RGMII[x]_TXC pin. This internal delay is always enabled.

B. Data and control information is received using both edges of the clocks. RGMII[x]_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_TXC and data bits 7-4 on the falling edge of RGMII[x]_TXC. Similarly, RGMII[x]_TX_CTL carries TXEN on rising edge of RGMII[x]_TXC and TXERR on falling edge of RGMII[x]_TXC.

Figure 6-32. CPSW3G RGMII[x]_TXC, RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics - RGMII Mode

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6.9.5.3 CPTS

Table 6-40, Table 6-41, Figure 6-33, Table 6-42, and Figure 6-34 present timing conditions, timing requirements, and switching characteristics for CPTS.

Table 6-40. CPTS Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	10	pF

Table 6-41. CPTS Timing Requirements

see Figure 6-33

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T1	$t_{w(HWTSPUSHH)}$	Pulse duration, HWnTSPUSH high	12P(1) + 2		ns
T2	$t_{w(HWTSPUSHL)}$	Pulse duration, HWnTSPUSH low	12P(1) + 2		ns
T3	$t_{c(RFT\_CLK)}$	Cycle time, RFT_CLK	5	8	ns
T4	$t_{w(RFT\_CLKH)}$	Pulse duration, RFT_CLK high	0.45T(2)		ns
T5	$t_{w(RFT\_CLKL)}$	Pulse duration, RFT_CLK low	0.45T(2)		ns

(1) P = functional clock period in ns.
(2) T = RFT_CLK cycle time in ns.

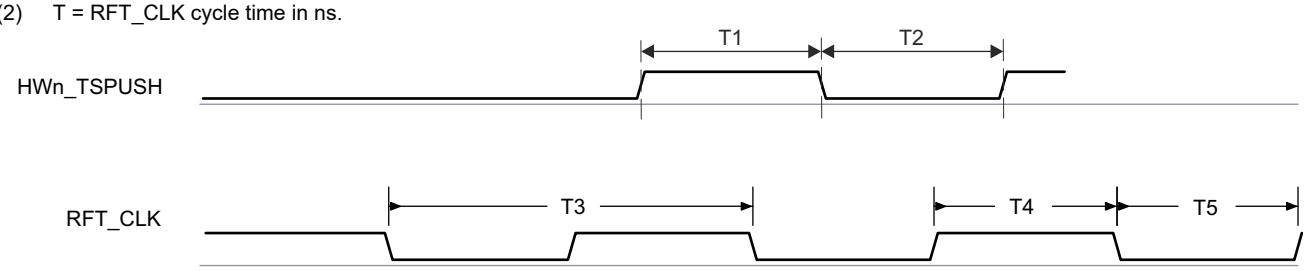

Figure 6-33. CPTS Timing Requirements

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Table 6-42. CPTS Switching Characteristics

see Figure 6-34

NO.	PARAMETER	DESCRIPTION	SOURCE	MIN	MAX	UNIT
T6	$t_{w(TS\_COMPH)}$	Pulse duration, TS_COMP high		36P(1) - 2		ns
T7	$t_{w(TS\_COMPL)}$	Pulse duration, TS_COMP low		36P(1) - 2		ns
T8	$t_{w(TS\_SYNCH)}$	Pulse duration, TS_SYNC high		36P(1) - 2		ns
T9	$t_{w(TS\_SYNCL)}$	Pulse duration, TS_SYNC low		36P(1) - 2		ns
T10	$t_{w(SYNC\_OUTH)}$	Pulse duration, SYNCn_OUT high	TS_SYNC	36P(1) - 2		ns
			GENF	5P(1) - 2		ns
T11	$t_{w(SYNC\_OUTL)}$	Pulse duration, SYNCn_OUT low	TS_SYNC	36P(1) - 2		ns
			GENF	5P(1) - 2		ns

(1) P = functional clock period in ns.

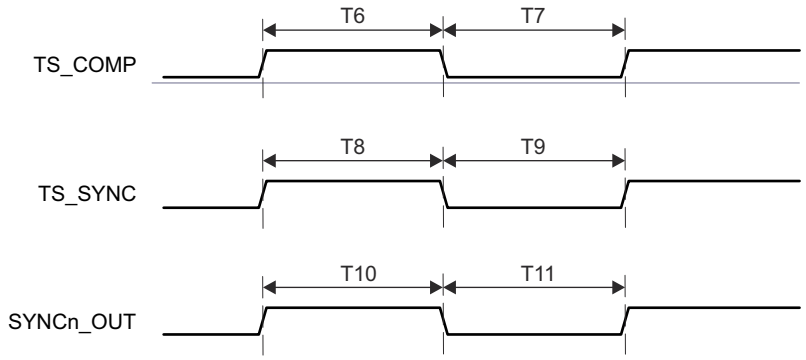

Figure 6-34. CPTS Switching Characteristics

For more information, see *Data Movement Architecture (DMA)* chapter in the device TRM.

6.9.5.4 CSI-2

Note

For more information, see the *Camera Serial Interface Receiver (CSI_RX_IF)* section in the device TRM. The CSI_RX_IF is connected to device port instances named CSIRXn, where n is the instance number.

The CSI_RX_IF and associated D-PHY implements a CSI-2 port (CSIRX0) compliant with the MIPI D-PHY specification v1.2 and the MIPI CSI-2 specification v1.3, with 4 differential data lanes plus 1 differential clock lane operating in synchronous double data rate mode. For CSI-2 timing details, see the respective MIPI specifications mentioned above.

- Support for 1-, 2-, 3- or 4-lane data transfer modes up to 1.5Gbps

6.9.5.5 CSI-2 TX

TBD

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6.9.5.6 DDRSS

For more details about features and additional description information on the device LPDDR4 Memory Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 6-43 and Figure 6-35 present switching characteristics for DDRSS.

Table 6-43. DDRSS Switching Characteristics

see Figure 1-1

NO.	PARAMETER		DDR TYPE	CORE VOLTAGE	MIN	MAX	UNIT
1	$t_{c(DDR\_CKP/DDR\_CKN)}$	Cycle time, DDR_CKP and DDR_CKN	LPDDR	0.75-V Operation	0.536(1)	20	ns
				0.85-V Operation	.500(1)	20	ns

(1) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. TI strongly recommends all designs to follow the TI LPDDR4 EVM PCB layout exactly in every detail (routing, spacing, vias/backdrill, PCB material, etc.) in order to achieve the full specified clock frequency. Refer to the **Jacinto 7 LPDDR4 Board Design and Layout Guidelines** for details.

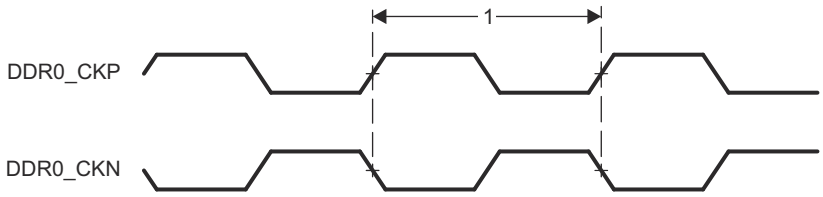

Figure 6-35. DDRSS Switching Characteristics

For more information, see *DDR Subsystem (DDRSS)* section in *Memory Controllers* chapter in the device TRM.

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6.9.5.7 DSS

Table 6-44, Table 6-45, Figure 6-36, Table 6-46 and Figure 6-37 present timing conditions, timing requirements, and switching characteristics for DSS.

Table 6-44. DSS Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1.44	26.4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1.5	5	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

Table 6-45. DSS External Pixel Clock Timing Requirements

see Figure 6-36

NO.			MIN	MAX	UNIT
D6	$t_{c(extpclkin)}$	Cycle time, VOUT(x)_EXTPCLKIN(2)	6.06		ns
D7	$t_{w(extpclkinL)}$	Pulse duration, VOUT(x)_EXTPCLKIN(2) low	0.475P(1)		ns
D8	$t_{w(extpclkinH)}$	Pulse duration, VOUT(x)_EXTPCLKIN(2) high	0.475P(1)		ns

(1) P = VOUT(x)_EXTPCLKIN cycle time in ns
(2) x in VOUT(x) = 0

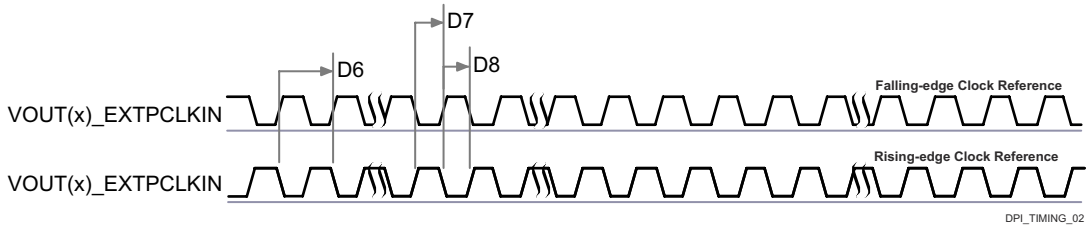


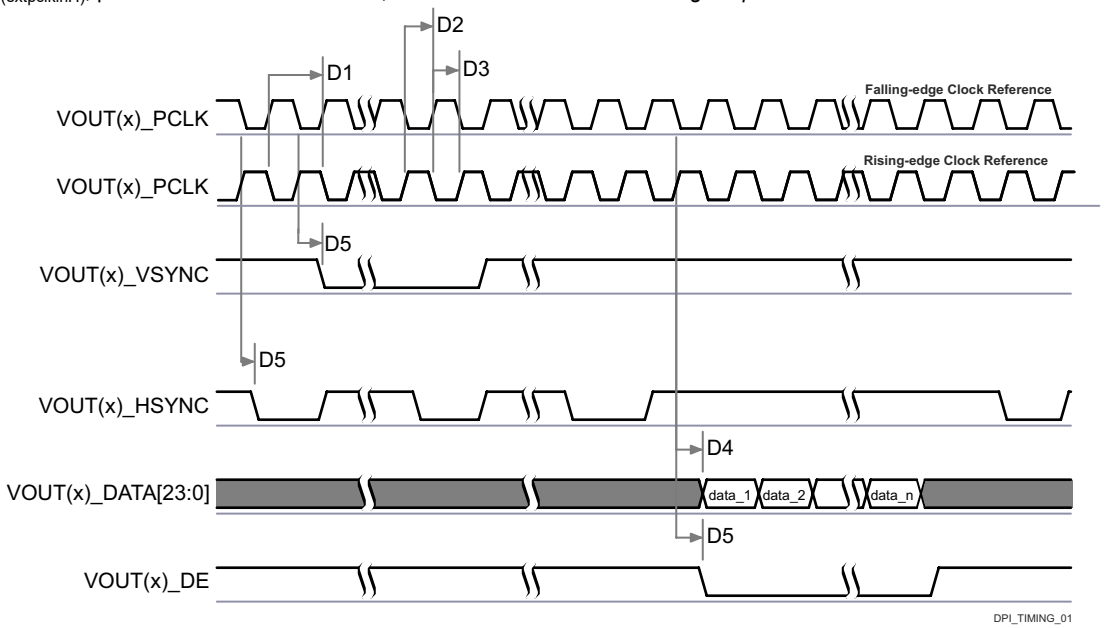
Figure 6-36. DSS External Pixel Clock Timing Requirements

Table 6-46. DSS Switching Characteristics

see Figure 6-37

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D1	$t_{c(pclk)}$	Cycle time, VOUT(x)_PCLK(2)		6.06		ns
D2	$t_{w(pclkL)}$	Pulse duration, VOUT(x)_PCLK(2) low	Internal PLL	0.475P(1) - 0.3		ns
			EXTPCLKIN	Y(3) - 0.45		ns
D3	$t_{w(pclkH)}$	Pulse duration, VOUT(x)_PCLK(2) high	Internal PLL	0.475P(1) -0.3		ns
			EXTPCLKIN	Z(4) - 0.45		ns
D4	$t_{d(pclkV-dataV)}$	Delay time, VOUT(x)_PCLK(2) transition to VOUT(x)_DATA[23:0](2) transition	Internal PLL	-0.68	1.78	ns
			EXTPCLKIN	-0.68	1.78	ns
D5	$t_{d(pclkV-ctrlL)}$	Delay time, VOUT(x)_PCLK(2) transition to control signals VOUT(x)_VSYNC(2), VOUT(x)_HSYNC(2), VOUT(x)_DE(2) falling edge	Internal PLL	-0.68	1.78	ns
			EXTPCLKIN	-0.68	1.78	ns

(1) P = VOUT(x)_PCLK cycle time in ns
(2) x in VOUT(x) = 0
(3) Y = $t_{w(extpclkinL)}$, parameter D7 from Table 6-45, *DSS External Pixel Clock Timing Requirements*
(4) Z = $t_{w(extpclkinH)}$, parameter D8 from Table 6-45, *DSS External Pixel Clock Timing Requirements*



A. The assertion of data can be programmed to occur on the falling or rising edge of the pixel clock. Refer to *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.
B. The polarity and pulse width of VOUT(x)_HSYNC and VOUT(x)_VSYNC are programmable, refer to *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.
C. The VOUT(x)_PCLK frequency is configurable, refer to *Display Subsystem* section in *Peripherals* chapter in the device TRM.

Figure 6-37. DSS Switching Characteristics

For more information, see *Display Subsystem (DSS) and Peripherals* section in *Peripherals* chapter of the device TRM.

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6.9.5.8 ECAP

Table 6-47, Table 6-48, Figure 6-38, Table 6-49, and Figure 6-39 present timing conditions, timing requirements, and switching characteristics for ECAP.

Table 6-47. ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

Table 6-48. ECAP Timing Requirements

see Figure 6-38

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP1	$t_{w(CAP)}$	Pulse duration, CAP (asynchronous)	2P(1) + 2		ns

(1) P = sysclk period in ns.

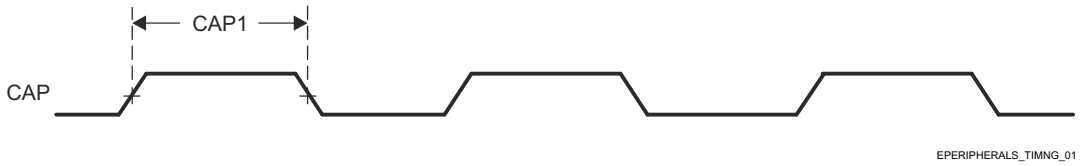

Figure 6-38. ECAP Timings Requirements

Table 6-49. ECAP Switching Characteristics

see Figure 6-39

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP2	$t_{w(APWM)}$	Pulse duration, APWMx high/low	2P(1) - 2		ns

(1) P = sysclk period in ns.

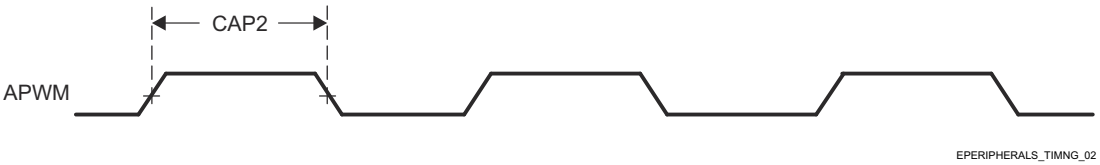

Figure 6-39. ECAP Switching Characteristics

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

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6.9.5.9 Emulation and Debug

For more details about features and additional description information on the device Trace and JTAG interfaces, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.9.5.9.1 Trace

Table 6-50. Trace Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	5	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Mismatch)}$	Propagation delay mismatch across all traces		200	ps

Table 6-51. Trace Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1.8V Mode					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	6.83		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	2.66		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	2.66		ns
DBTR4	$t_{osu(TRC\_DATAV-TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	0.85		ns
DBTR5	$t_{oh(TRC\_CLK-TRC\_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	0.85		ns
DBTR6	$t_{osu(TRC\_CTLV-TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	0.85		ns
DBTR7	$t_{oh(TRC\_CLK-TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	0.85		ns
3.3V Mode					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	8.78		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	3.64		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	3.64		ns
DBTR4	$t_{osu(TRC\_DATAV-TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	1.10		ns
DBTR5	$t_{oh(TRC\_CLK-TRC\_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	1.10		ns
DBTR6	$t_{osu(TRC\_CTLV-TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	1.10		ns
DBTR7	$t_{oh(TRC\_CLK-TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	1.10		ns

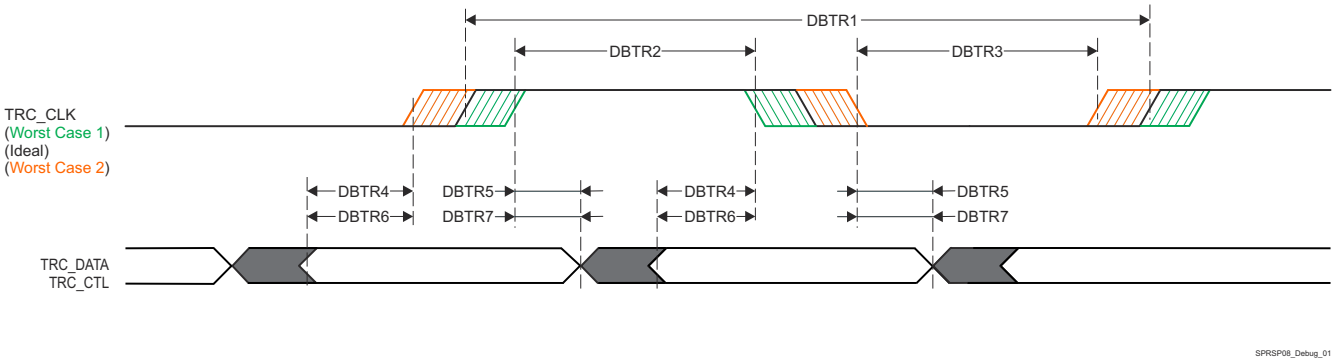

Figure 6-40. Trace Switching Characteristics

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6.9.5.9.2 JTAG

Table 6-52. JTAG Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	2.0	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	5	15	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	83.5	1000(1)	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

(1) Maximum propagation delay associated with the JTAG signal traces has a significant impact on maximum TCK operating frequency. It may be possible to increase the trace delay beyond this value, but the operating frequency of TCK must be reduced to account for the additional trace delay.

Table 6-53. JTAG Timing Requirements

see Figure 6-41

NO.			MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time minimum, TCK	40(1)		ns
J2	$t_{w(TCKH)}$	Pulse width minimum, TCK high	0.4P(2)		ns
J3	$t_{w(TCKL)}$	Pulse width minimum, TCK low	0.4P(2)		ns
J4	$t_{su(TDI-TCK)}$	Input setup time minimum, TDI valid to TCK high	2		ns
	$t_{su(TMS-TCK)}$	Input setup time minimum, TMS valid to TCK high	2		ns
J5	$t_{h(TCK-TDI)}$	Input hold time minimum, TDI valid from TCK high	3		ns
	$t_{h(TCK-TMS)}$	Input hold time minimum, TMS valid from TCK high	3		ns

(1) The maximum TCK operating frequency assumes the following timing requirements and switching characteristis for the attached debugger. The operating frequency of TCK must be reduced to provide appropriate timing margin if the debugger exceeds any of these assumptions.
- Minimum TDO setup time of 2ns relative to the rising edge of TCK
- TDI and TMS output delay in the range of -12.9ns to 13.9ns relative to the falling edge of TCK

(2) P = TCK cycle time in ns

Table 6-54. JTAG Switching Characteristics

see Figure 6-41

NO.	PARAMETER		MIN	MAX	UNIT
J6	$t_{d(TCKL-TDOI)}$	Delay time minimum, TCK low to TDO invalid	0		ns
J7	$t_{d(TCKL-TDOV)}$	Delay time maximum, TCK low to TDO valid		12	ns

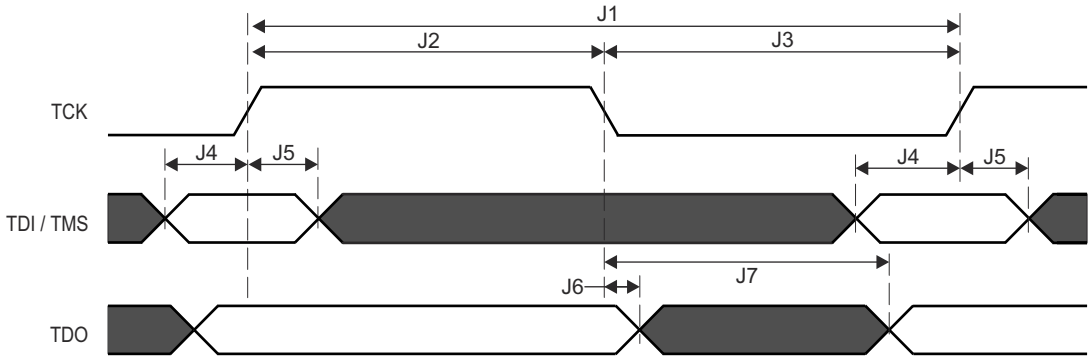

Figure 6-41. JTAG Timing Requirements and Switching Characteristics

6.9.5.10 EPWM

Table 6-55, Table 6-56, Figure 6-42, Table 6-57, Figure 6-43, Figure 6-44, and Figure 6-45 present timing conditions, timing requirements, and switching characteristics for EPWM.

Table 6-55. EPWM Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

Table 6-56. EPWM Timing Requirements

see Figure 6-42

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM6	$t_{w(SYNCIN)}$	Pulse duration, EHRPWM_SYNCI	2P(1) + 2		ns
PWM7	$t_{w(TZ)}$	Pulse duration, EHRPWM_TZn_IN low	3P(1) + 2		ns

(1) P = sysclk period in ns.

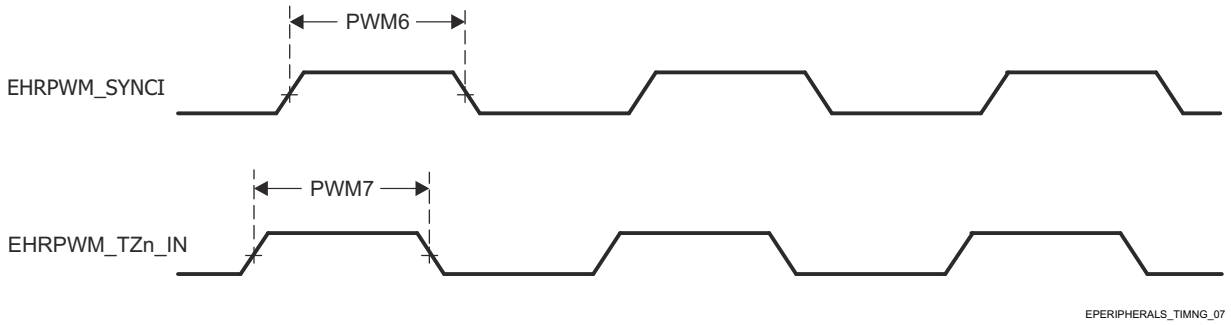

Figure 6-42. EPWM Timing Requirements

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Table 6-57. EPWM Switching Characteristics

see Figure 6-43, Figure 6-44, and Figure 6-45

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM1	$t_{w(PWM)}$	Pulse duration, EHRPWM_A/B high/low	P(1) - 3		ns
PWM2	$t_{w(SYNCOUT)}$	Pulse duration, EHRPWM_SYNCO	P(1) - 3		ns
PWM3	$t_{d(TZ-PWM)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B forced high/low		11	ns
PWM4	$t_{d(TZ-PWMZ)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B Hi-Z		11	ns
PWM5	$t_{w(SOC)}$	Pulse duration, EHRPWM_SOCA/B output	P(1) - 3		ns

(1) P = sysclk period in ns.

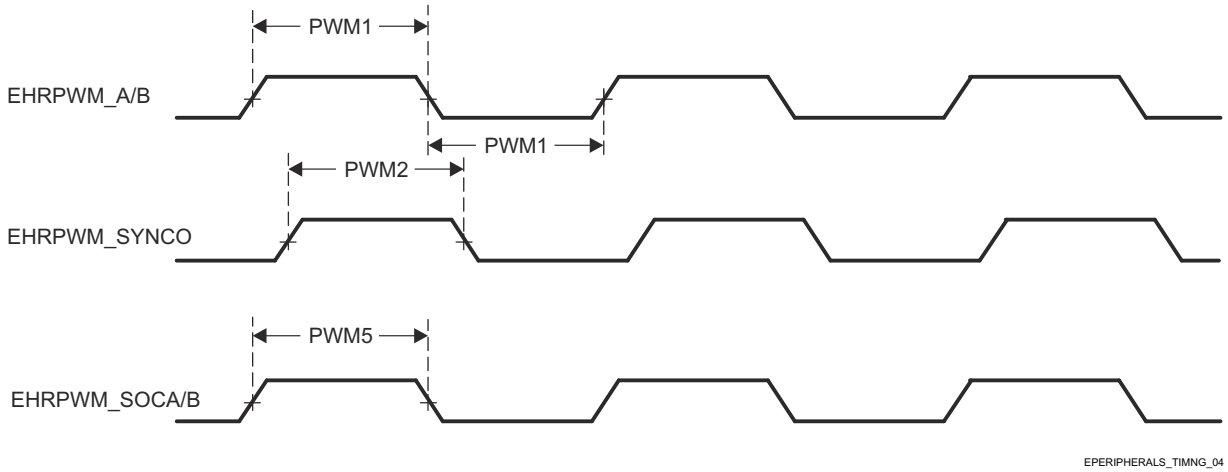

Figure 6-43. EHRPWM Switching Characteristics

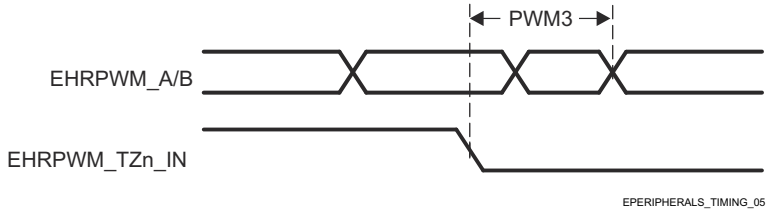

Figure 6-44. EHRPWM_TZn_IN to EHRPWM_A/B Forced Switching Characteristics

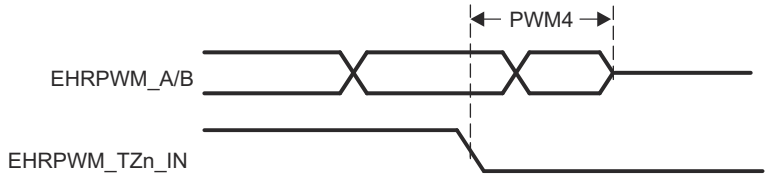

Figure 6-45. EHRPWM_TZn_IN to EHRPWM_A/B Hi-Z Switching Characteristics

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

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6.9.5.11 EQEP

Table 6-58, Table 6-59, Figure 6-46, and Table 6-60 present timing conditions, timing requirements, and switching characteristics for EQEP.

Table 6-58. EQEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

Table 6-59. EQEP Timing Requirements

see Figure 6-46

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP1	$t_{w(QEP)}$	Pulse duration, QEP_A/B	2P(1) + 2		ns
QEP2	$t_{w(QEPIH)}$	Pulse duration, QEP_I high	2P(1) + 2		ns
QEP3	$t_{w(QEPIL)}$	Pulse duration, QEP_I low	2P(1) + 2		ns
QEP4	$t_{w(QEPSH)}$	Pulse duration, QEP_S high	2P(1) + 2		ns
QEP5	$t_{w(QEPSL)}$	Pulse duration, QEP_S low	2P(1) + 2		ns

(1) P = sysclk period in ns

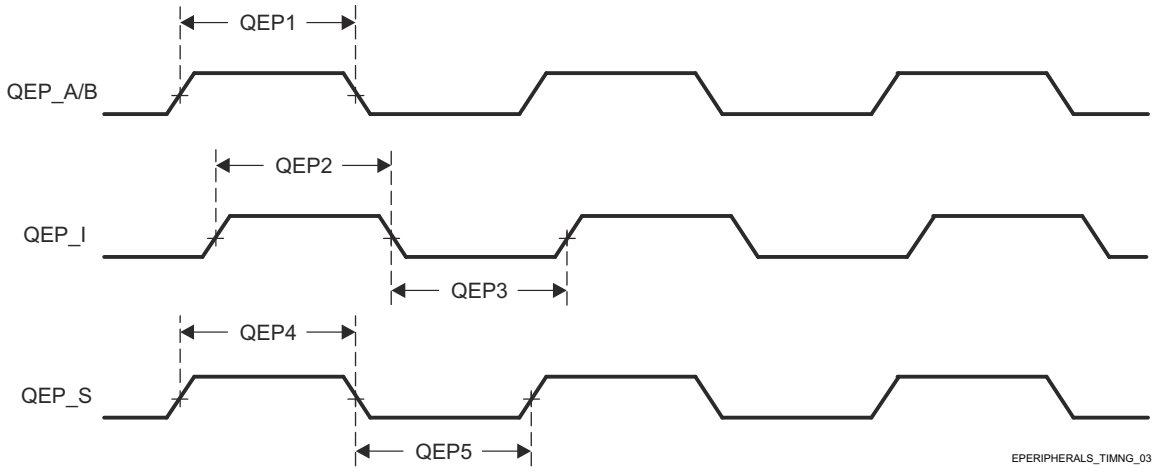

Figure 6-46. EQEP Timing Requirements

Table 6-60. EQEP Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP6	$t_{d(QEP-CNTR)}$	Delay time, external clock to counter increment		24	ns

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

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6.9.5.12 GPIO

Table 6-61, Table 6-62, and Table 6-63 present timing conditions, timing requirements, and switching characteristics for GPIO.

The device has three instances of the GPIO module.

- MCU_GPIO0
- GPIO0
- GPIO1

Note

GPIOn_x is generic name used to describe a GPIO signal, where n represents the specific GPIO module and x represents one of the input/output signals associated with the module.

For additional description information on the device GPIO, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 6-61. GPIO Timing Conditions

PARAMETER		BUFFER TYPE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	LVCMOS (VDD(1) = 1.8V)	0.0018	6.6	V/ns
		LVCMOS (VDD(1) = 3.3V)	0.0033	6.6	V/ns
		I2C OD FS (VDD(1) = 1.8V)	0.0018	6.6	V/ns
		I2C OD FS (VDD(1) = 3.3V)	0.0033	0.08	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	LVCMOS	3	10	pF
		I2C OD FS	3	100	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

Table 6-62. GPIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
GPIO1	$t_{w(GPIO\_IN)}$	Pulse width, GPIOn_x	2P(1) + 30		ns

(1) P = functional clock period in ns.

Table 6-63. GPIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
GPIO2	$t_{w(GPIO\_OUT)}$	Pulse width, GPIOn_x	LVCMOS	0.975P(1) - 3.6		ns
			I2C OD FS	160		ns

(1) P = functional clock period in ns.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

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6.9.5.13 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 6-64 presents timing conditions for GPMC.

Table 6-64. GPMC Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		1.65	4	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	133MHz Synchronous Mode	140	360	ps
		All other modes	140	720	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces			200	ps

For more information, see *General-Purpose Memory Controller (GPMC)* section in *Peripherals* chapter in the device TRM.

6.9.5.13.1 GPMC and NOR Flash — Synchronous Mode

Table 6-65 and Table 6-66 present timing requirements and switching characteristics for GPMC and NOR Flash - Synchronous Mode.

Table 6-65. GPMC and NOR Flash Timing Requirements — Synchronous Mode

see Figure 6-47, Figure 6-48, and Figure 6-51

NO.	PARAMETER	DESCRIPTION	MODE[4]	MIN MAX GPMC_FCLK = 100MHz[1]	MIN MAX GPMC_FCLK = 133MHz[1]	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.61	0.92	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.86	3.41	ns
F13	$t_{h(clkH-dV)}$	Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns
F21	$t_{su(waitV-clkH)}$	Setup time, input wait GPMC_WAIT[j][2] [3] valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.61	0.92	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.86	3.41	ns
F22	$t_{h(clkH-waitV)}$	Hold time, input wait GPMC_WAIT[j][2] [3] valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns

(1) GPMC_FCLK select

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- gpmc_fclk_sel[1:0] = 2b01 to select the 100MHz GPMC_FCLK
- gpmc_fclk_sel[1:0] = 2b00 to select the 133MHz GPMC_FCLK

(2) In GPMC_WAIT[j], j is equal to 0 or 1.

(3) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see *General-Purpose Memory Controller (GPMC)* section in the device TRM.

(4) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For not_div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 1h to 3h:
  - GPMC_CLK frequency = GPMC_FCLK frequency / (2 to 4)

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

Table 6-66. GPMC and NOR Flash Switching Characteristics – Synchronous Mode

see Figure 6-47, Figure 6-48, Figure 6-49, Figure 6-50, and Figure 6-51

NO. (2)	PARAMETER	DESCRIPTION	MODE(16)	MIN	MAX	MIN	MAX	UNIT
				100MHz		133MHz		
F0	1 / tc(clk)	Period, output clock GPMC_CLK(15)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	10.00		7.52		ns
F1	$t_{w(clkH)}$	Typical pulse duration, output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475P - 0.3(14)		0.475P - 0.3(14)		ns
F1	$t_{w(clkL)}$	Typical pulse duration, output clock GPMC_CLK low	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475P - 0.3(14)		0.475P - 0.3(14)		ns
F2	$t_{d(clkH-csnV)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] transition(13)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	F - 2.2 (5)	F + 3.75	F - 2.2 (5)	F + 3.75	ns
F3	$t_{d(clkH-CSn[i]V)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] invalid(13)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	E - 2.2 (4)	E + 3.18	E - 2.2 (4)	E + 4.5	ns
F4	$t_{d(aV-clk)}$	Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2.3 (2)	B + 4.5	B - 2.3 (2)	B + 4.5	ns
F5	$t_{d(clkH-aIV)}$	Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	-2.3	4.5	-2.3	4.5	ns
F6	$t_{d(be[x]nV-clk)}$	Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2.3 (2)	B + 1.9	B - 2.3 (2)	B + 1.9	ns
F7	$t_{d(clkH-be[x]nIV)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid(10)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3(3)	D + 1.9	D - 2.3 (3)	D + 1.9	ns

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Table 6-66. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (continued)

see Figure 6-47, Figure 6-48, Figure 6-49, Figure 6-50, and Figure 6-51

NO. (2)	PARAMETER	DESCRIPTION	MODE(16)	MIN MAX 100MHz	MIN MAX 133MHz	UNIT
F7	$t_{d(clkL-be[x]nIV)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3 D + 1.9 (3)	D - 2.3 D + 1.9 (3)	ns
F7	$t_{d(clkL-be[x]nIV).}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3 D + 1.9 (3)	D - 2.3 D + 1.9 (3)	ns
F8	$t_{d(clkH-advn)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	G - 2.3(6) G + 4.5	G - 2.3 G + 4.5 (6)	ns
F9	$t_{d(clkH-advnIV)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	D - 2.3 D + 4.5 (3)	D - 2.3 D + 4.5 (3)	ns
F10	$t_{d(clkH-oen)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	H - 2.3 H + 3.5 (7)	H - 2.3 H + 3.5 (7)	ns
F11	$t_{d(clkH-oenIV)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	H - 2.3 H + 3.5 (7)	H - 2.3 H + 3.5 (7)	ns
F14	$t_{d(clkH-wen)}$	Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	I - 2.3 I + 4.5 (8)	I - 2.3 I + 4.5 (8)	ns
F15	$t_{d(clkH-do)}$	Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition(10)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 J + 2.7 (9)	J - 2.3 J + 2.7 (9)	ns
F15	$t_{d(clkL-do)}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 J + 2.7 (9)	J - 2.3 J + 2.7 (9)	ns
F15	$t_{d(clkL-do).}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 J + 2.7 (9)	J - 2.3 J + 2.7 (9)	ns
F17	$t_{d(clkH-be[x]n)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition(10)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 J + 1.9 (9)	J - 2.3 J + 1.9 (9)	ns
F17	$t_{d(clkL-be[x]n)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 J + 1.9 (9)	J - 2.3 J + 1.9 (9)	ns
F17	$t_{d(clkL-be[x]n).}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 J + 1.9 (9)	J - 2.3 J + 1.9 (9)	ns
F18	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i](13) low	Read	A	A	ns
			Write	A	A	ns
F19	$t_{w(be[x]nV)}$	Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low	Read	C	C	ns
			Write	C	C	ns

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Table 6-66. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (continued)

see Figure 6-47, Figure 6-48, Figure 6-49, Figure 6-50, and Figure 6-51

NO. (2)	PARAMETER	DESCRIPTION	MODE(16)	MIN MAX 100MHz	MIN MAX 133MHz	UNIT
F20	$t_{w(advnV)}$	Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low	Read	K	K	ns
			Write	K	K	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
With n being the page burst access number.

(2) B = ClkActivationTime × GPMC_FCLK(14)

(3) For single read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: D = (WrCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(4) For single read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: E = (CSWrOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(5) For csn falling edge (CS activated):

- Case GPMCFCLKDIVIDER = 0:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(14) if ((CSOnTime - ClkActivationTime) is a multiple of 3)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(14) if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
  - F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK(14) if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(6) For ADV falling edge (ADV activated):

- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14)

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- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(7) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For WE falling edge (WE activated):

- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK (14)
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if ((WEOffTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) J = GPMC_FCLK(14)

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(10) First transfer only for CLK DIV 1 mode.
(11) Half cycle; for all data after initial transfer for CLK DIV 1 mode.
(12) Half cycle of GPMC_CLKOUT; for all data for modes other than CLK DIV 1 mode. GPMC_CLKOUT divide down from GPMC_FCLK.
(13) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
(14) P = GPMC_CLK period in ns
(15) Related to the GPMC_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_i configuration register bit field GPMCFCLKDIVIDER.
(16) For div_by_1_mode:

- GPMC_CONFIG1_i register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

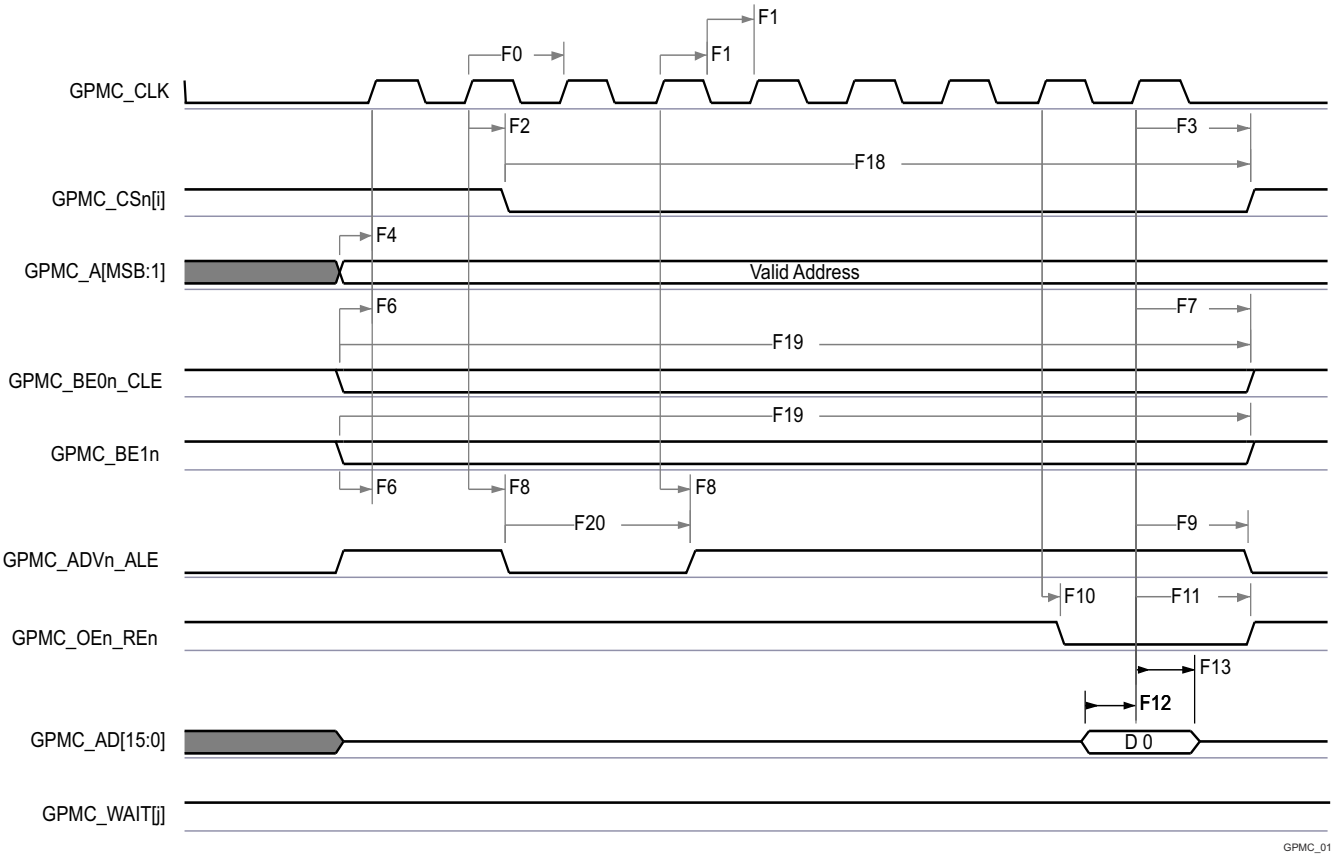
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

For no extra_delay:

- GPMC_CONFIG2_i Register: CSEXTRADELAY = 0h = CSn Timing control signal is not delayed
- GPMC_CONFIG4_i Register: WEEXTRADELAY = 0h = nWE timing control signal is not delayed
- GPMC_CONFIG4_i Register: OEEXTRADELAY = 0h = nOE timing control signal is not delayed
- GPMC_CONFIG3_i Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-47. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)

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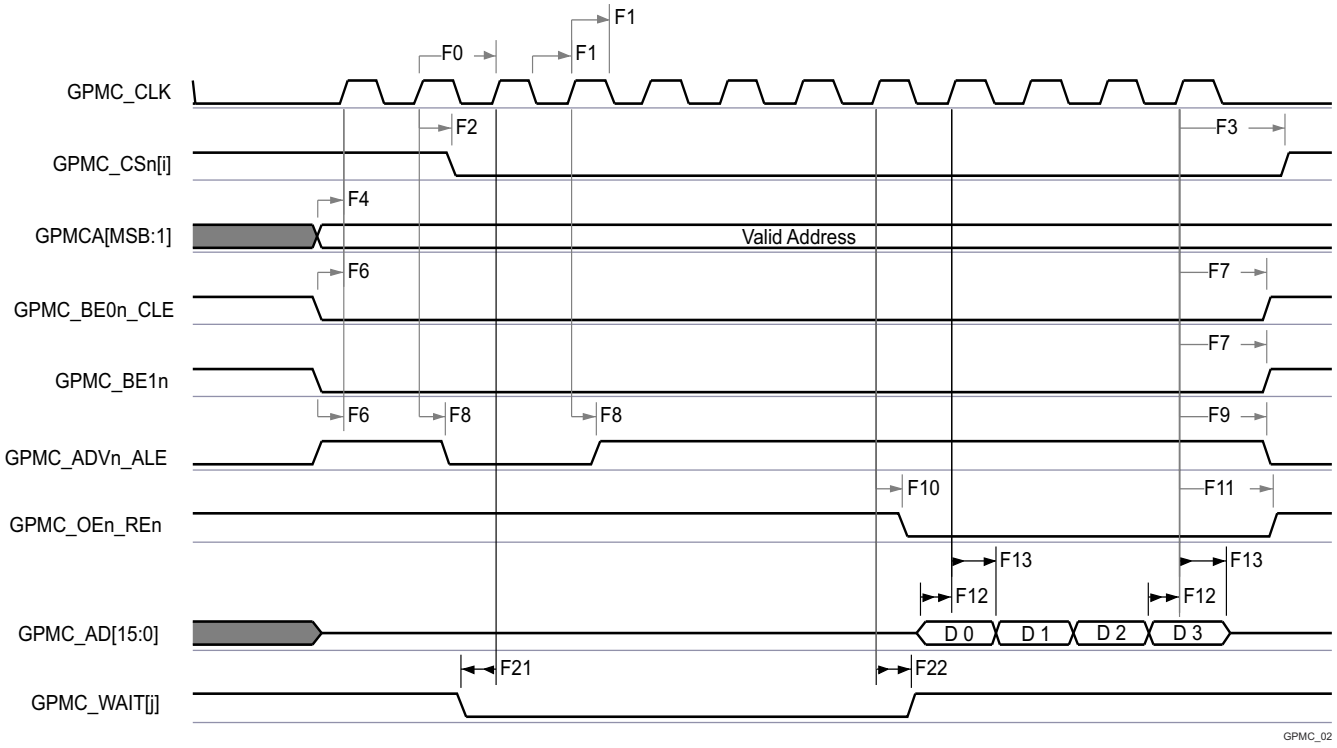
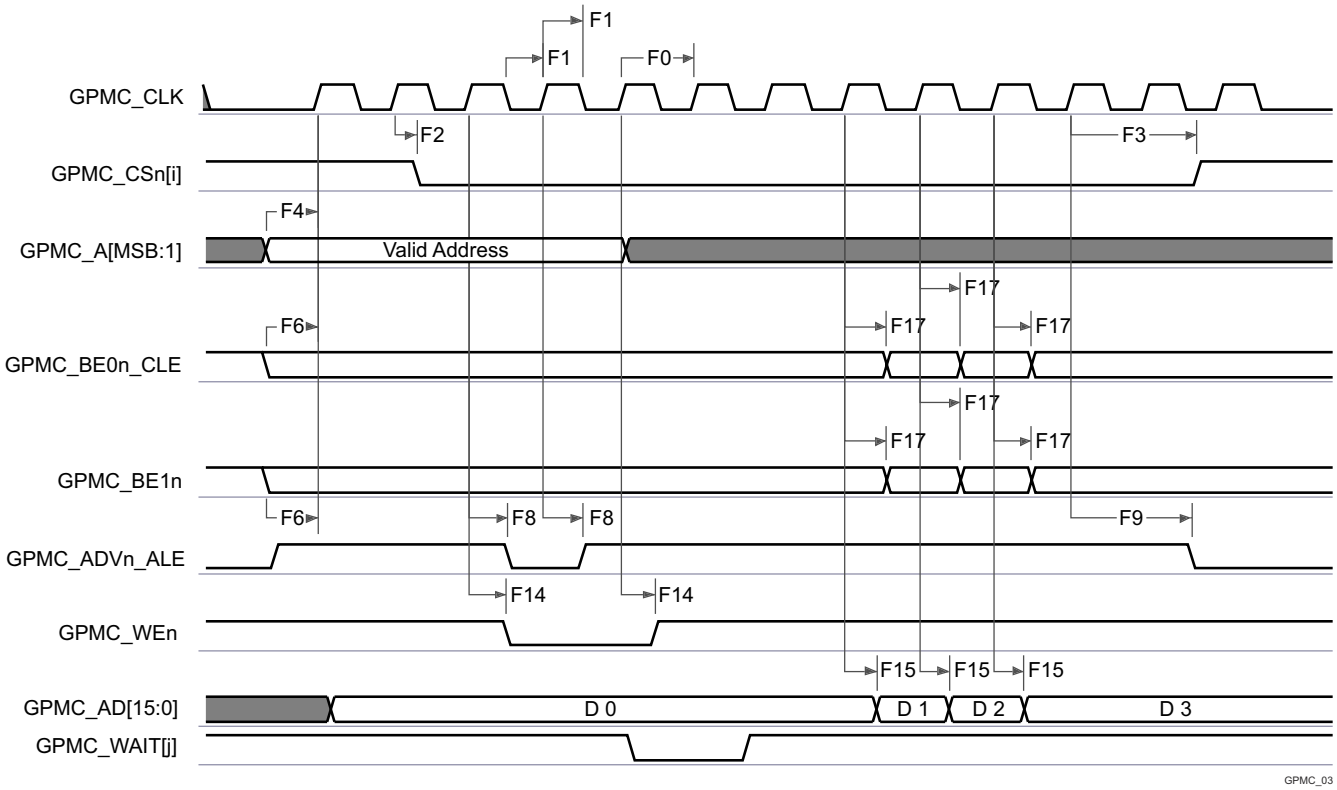


A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-48. GPMC and NOR Flash — Synchronous Burst Read — 4x16–bit (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

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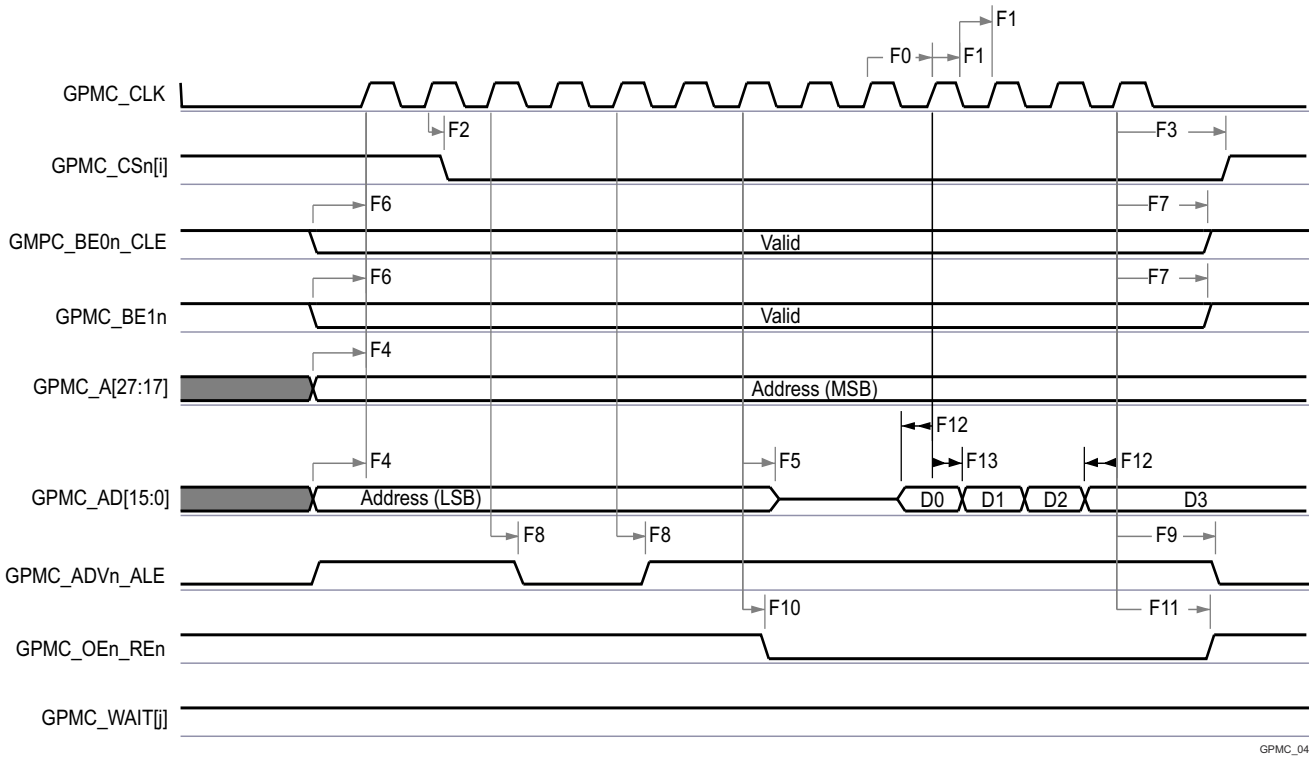
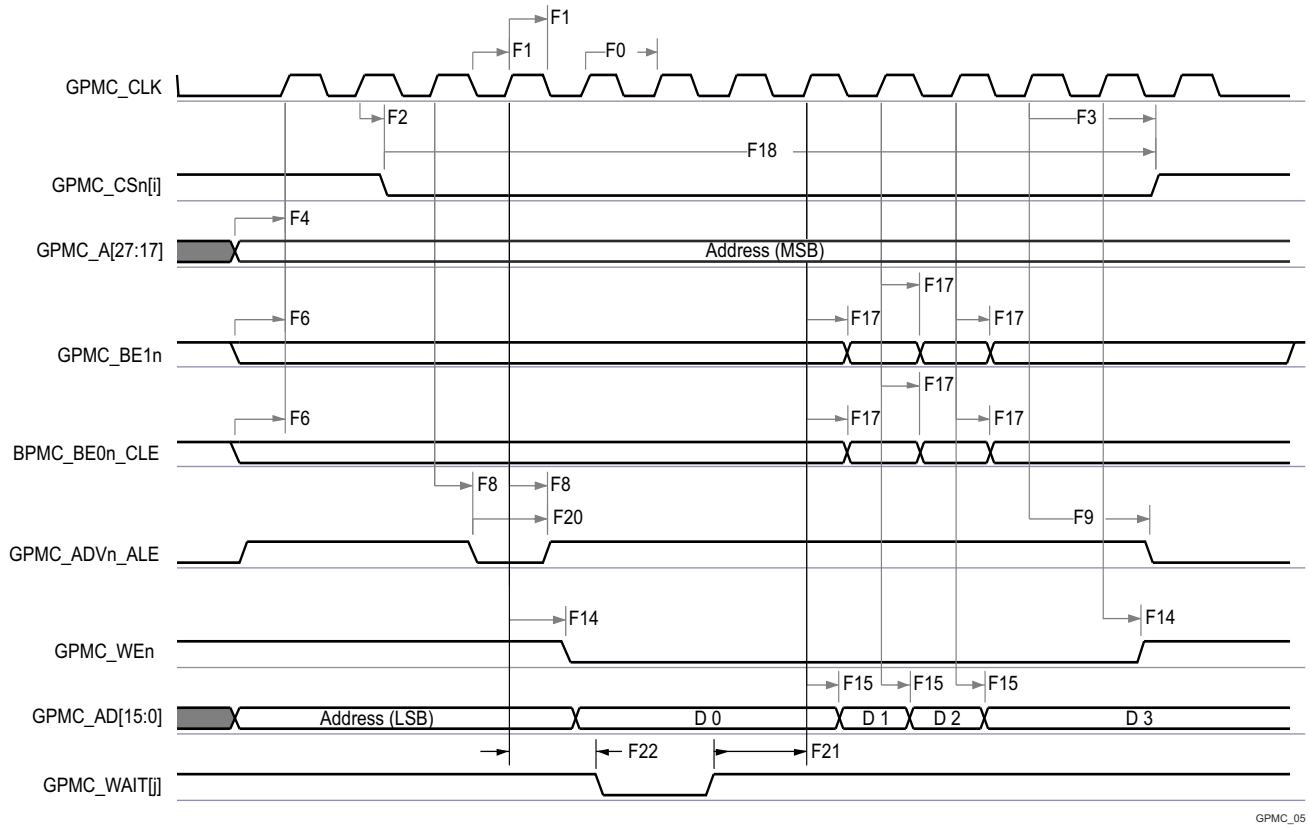
B. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-49. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-50. GPMC and Multiplexed NOR Flash — Synchronous Burst Read



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-51. GPMC and Multiplexed NOR Flash — Synchronous Burst Write

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6.9.5.13.2 GPMC and NOR Flash — Asynchronous Mode

Table 6-67 and Table 6-68 present timing requirements and switching characteristics for GPMC and NOR Flash — Asynchronous Mode.

Table 6-67. GPMC and NOR Flash Timing Requirements – Asynchronous Mode

see Figure 6-52, Figure 6-53, Figure 6-54, and Figure 6-56

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
FA5 (1)	$t_{acc(d)}$	Data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H (4)	ns
FA20 (2)	$t_{acc1-pgmode(d)}$	Page mode successive data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		P (3)	ns
FA21 (1)	$t_{acc2-pgmode(d)}$	Page mode first data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H (4)	ns

(1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
(2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
(3) P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(5)
(4) H = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(5)
(5) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

Table 6-68. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode

see Figure 6-52, Figure 6-53, Figure 6-54, Figure 6-55, Figure 6-56, and Figure 6-57

NO.	PARAMETER	DESCRIPTION	MODE (15)	MIN	MAX	UNIT
				133MHz		
FA0	$t_{w(be[x]nV)}$	Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time	Read		N (12)	ns
			Write		N (12)	
FA1	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i](13) low	Read		A (1)	ns
			Write		A (1)	
FA3	$t_{d(csnV-advnIV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output address valid and address latch enable GPMC_ADVn_ALE invalid	Read	B - 2 (2)	B + 2(2)	ns
			Write	B - 2(2)	B + 2(2)	
FA4	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output enable GPMC_OEn_REn invalid (Single read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2(3)	C + 2(3)	ns
FA9	$t_{d(aV-csnV)}$	Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CSn[i](13) valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2(9)	J + 2(9)	ns
FA10	$t_{d(be[x]nV-csnV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CSn[i](13) valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2(9)	J + 2(9)	ns
FA12	$t_{d(csnV-advnV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output address valid and address latch enable GPMC_ADVn_ALE valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	K - 2(10)	K + 2(10)	ns
FA13	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L - 2(11)	L + 2(11)	ns
FA16	$t_{w(aIV)}$	Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G (7)		ns

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Table 6-68. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode (continued)

see Figure 6-52, Figure 6-53, Figure 6-54, Figure 6-55, Figure 6-56, and Figure 6-57

NO.	PARAMETER	DESCRIPTION	MODE [15]	MIN	MAX	UNIT
				133MHz		
FA18	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn invalid (Burst read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I - 2[8]	I + 2[8]	ns
FA20	$t_{w(aV)}$	Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D [4]		ns
FA25	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E - 2[5]	E + 2[5]	ns
FA27	$t_{d(csnV-wenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2[6]	F + 2[6]	ns
FA28	$t_{d(wenV-dV)}$	Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2	ns
FA29	$t_{d(dV-csnV)}$	Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CSn[i][13] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2[9]	J + 2[9]	ns
FA37	$t_{d(oenV-aIV)}$	Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For single write: A = (CSWrOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
with n being the page burst access number
(2) For reading: B = ((ADVRdOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
For writing: B = ((ADVWrOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(3) C = ((OEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(4) D = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
(5) E = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(6) F = ((WEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(7) G = Cycle2CycleDelay × GPMC_FCLK[14]
(8) I = ((OEOffTime + (n - 1) × PageBurstAccessTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(9) J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK[14]
(10) K = ((ADVOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(11) L = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(12) For single read: N = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For single write: N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst read: N = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst write: N = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
(13) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(15) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME,

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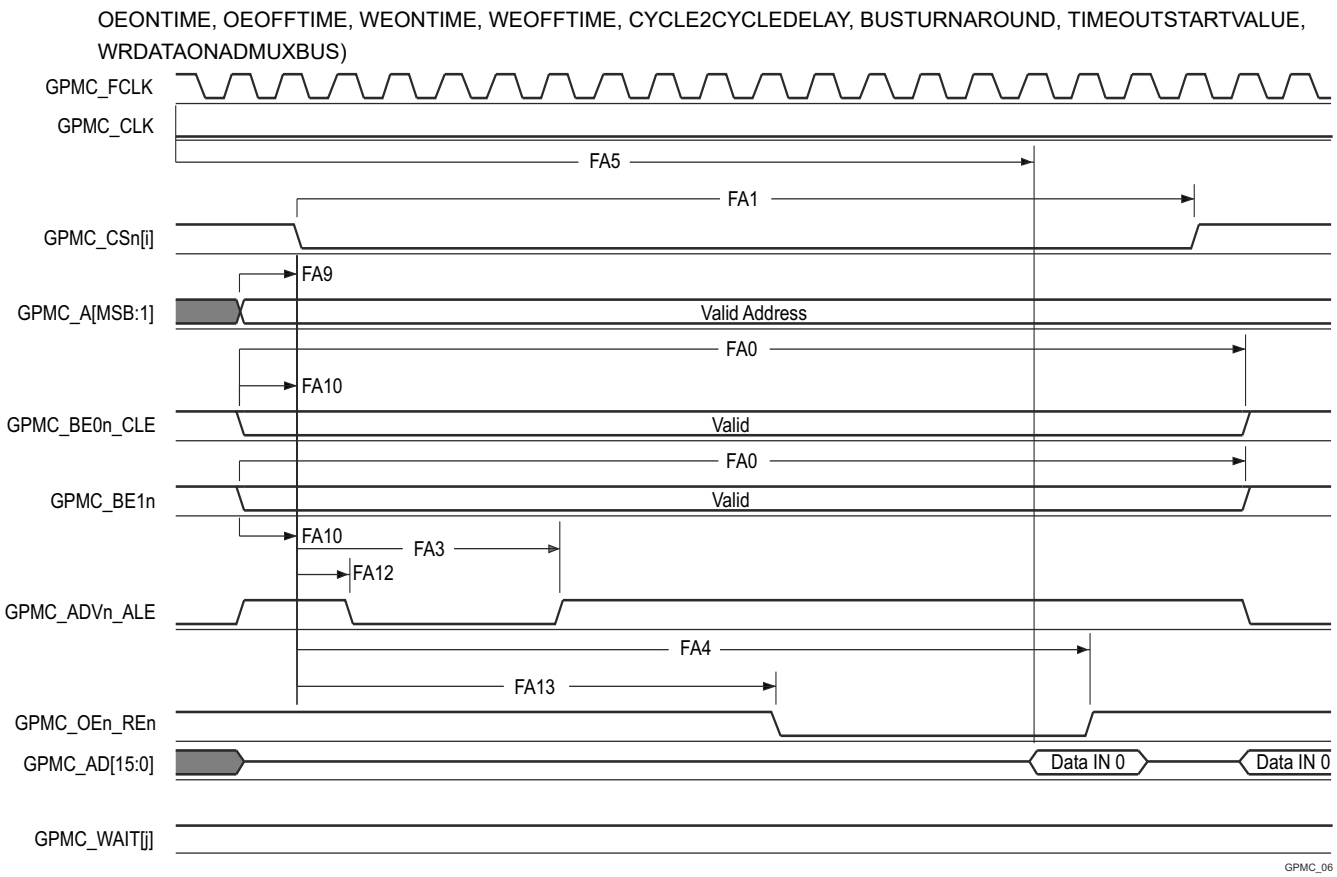

A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], jis equal to 0 or 1.

B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-52. GPMC and NOR Flash — Asynchronous Read — Single Word

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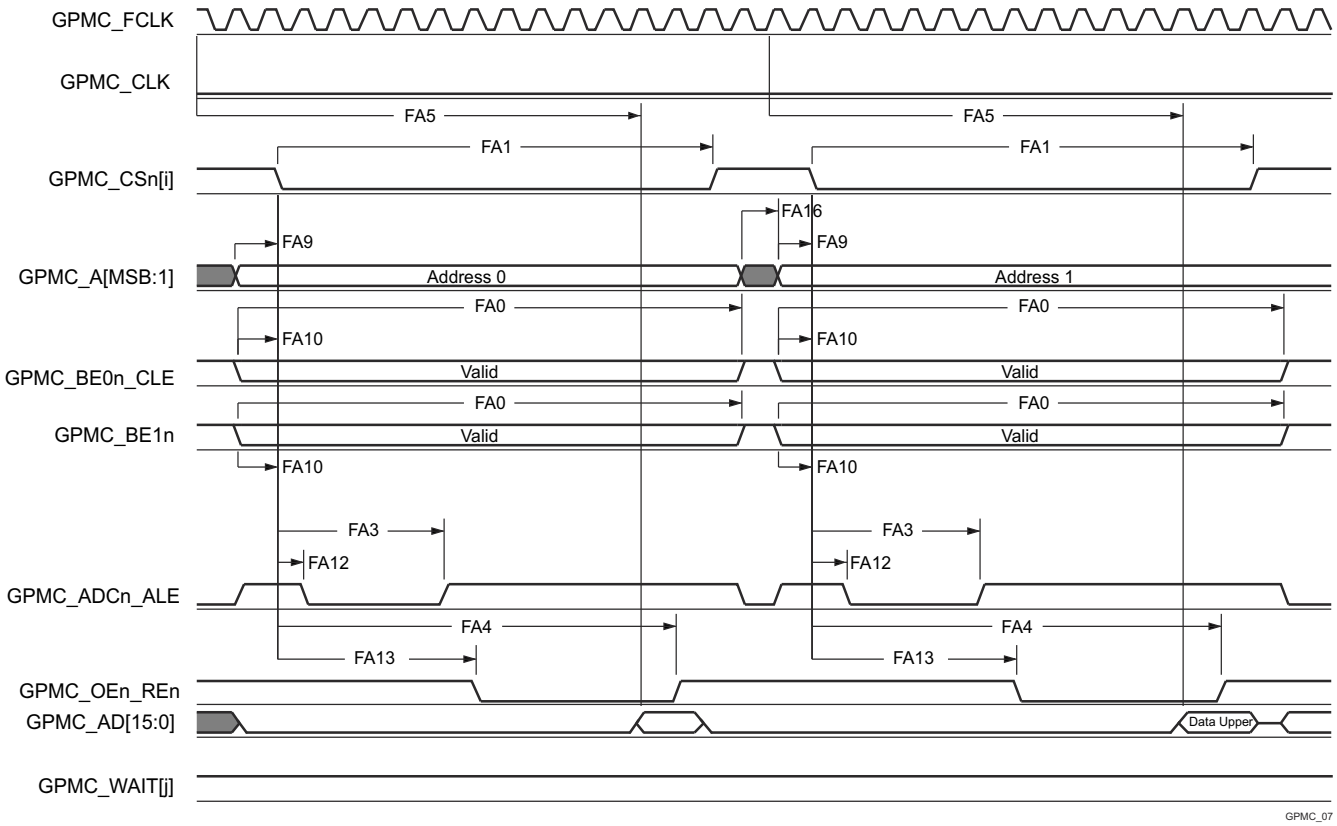

A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-53. GPMC and NOR Flash — Asynchronous Read — 32–Bit

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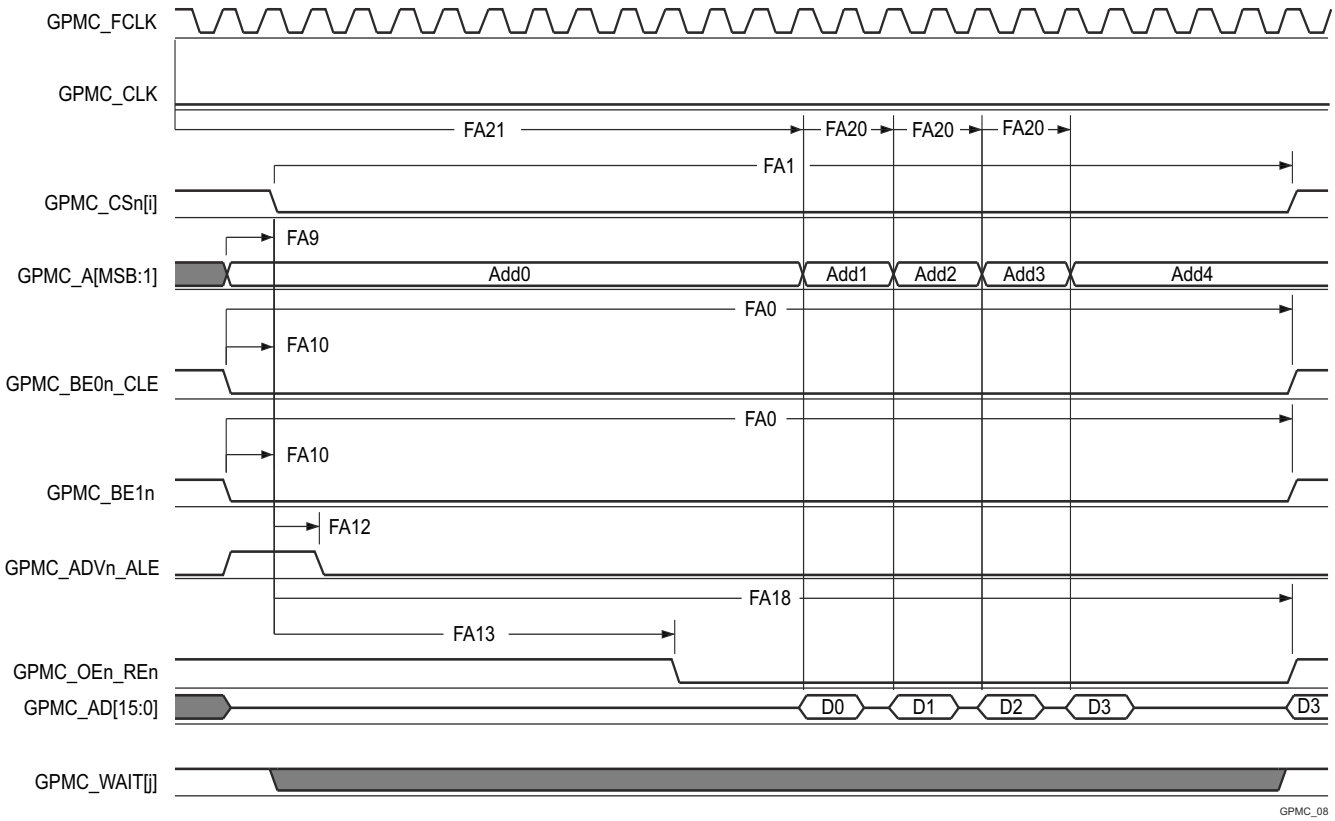

A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.

C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.

D. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-54. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16–Bit

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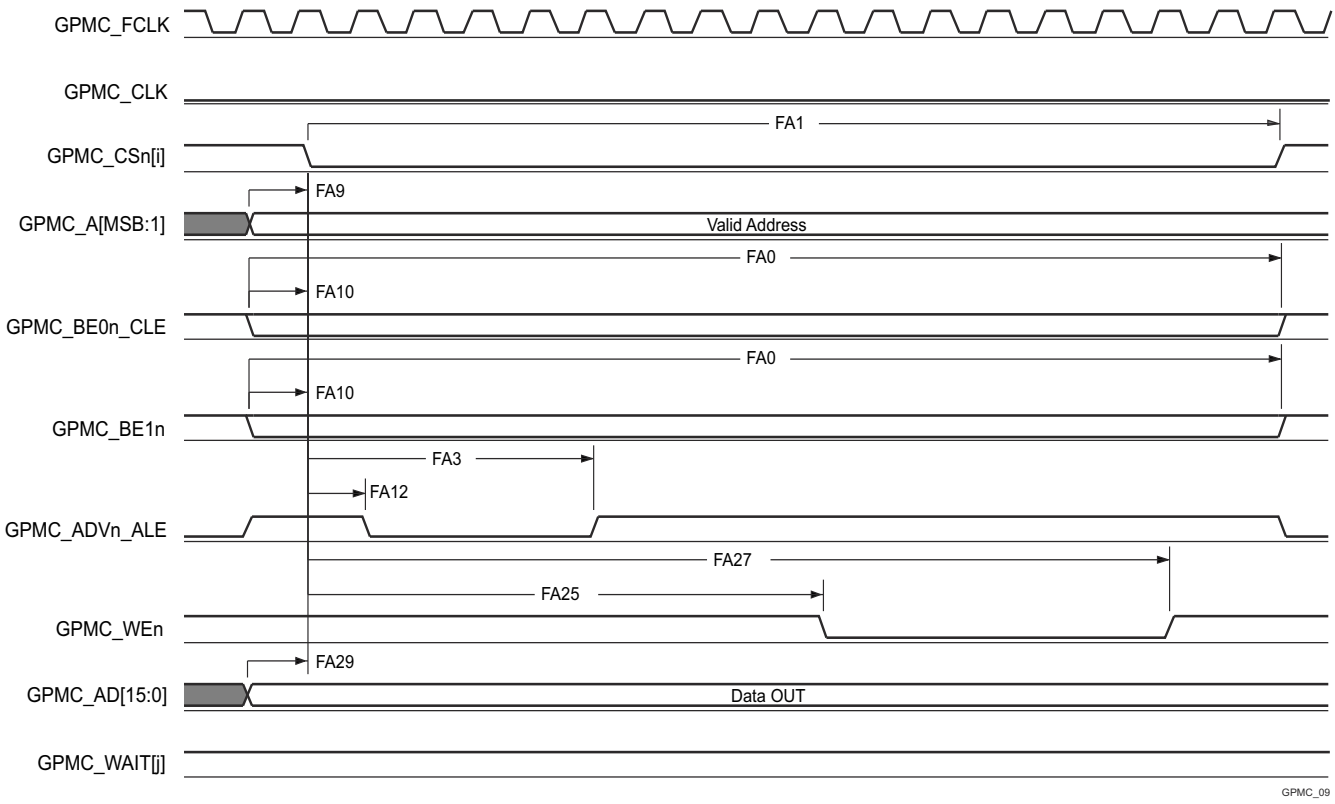

A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-55. GPMC and NOR Flash — Asynchronous Write — Single Word

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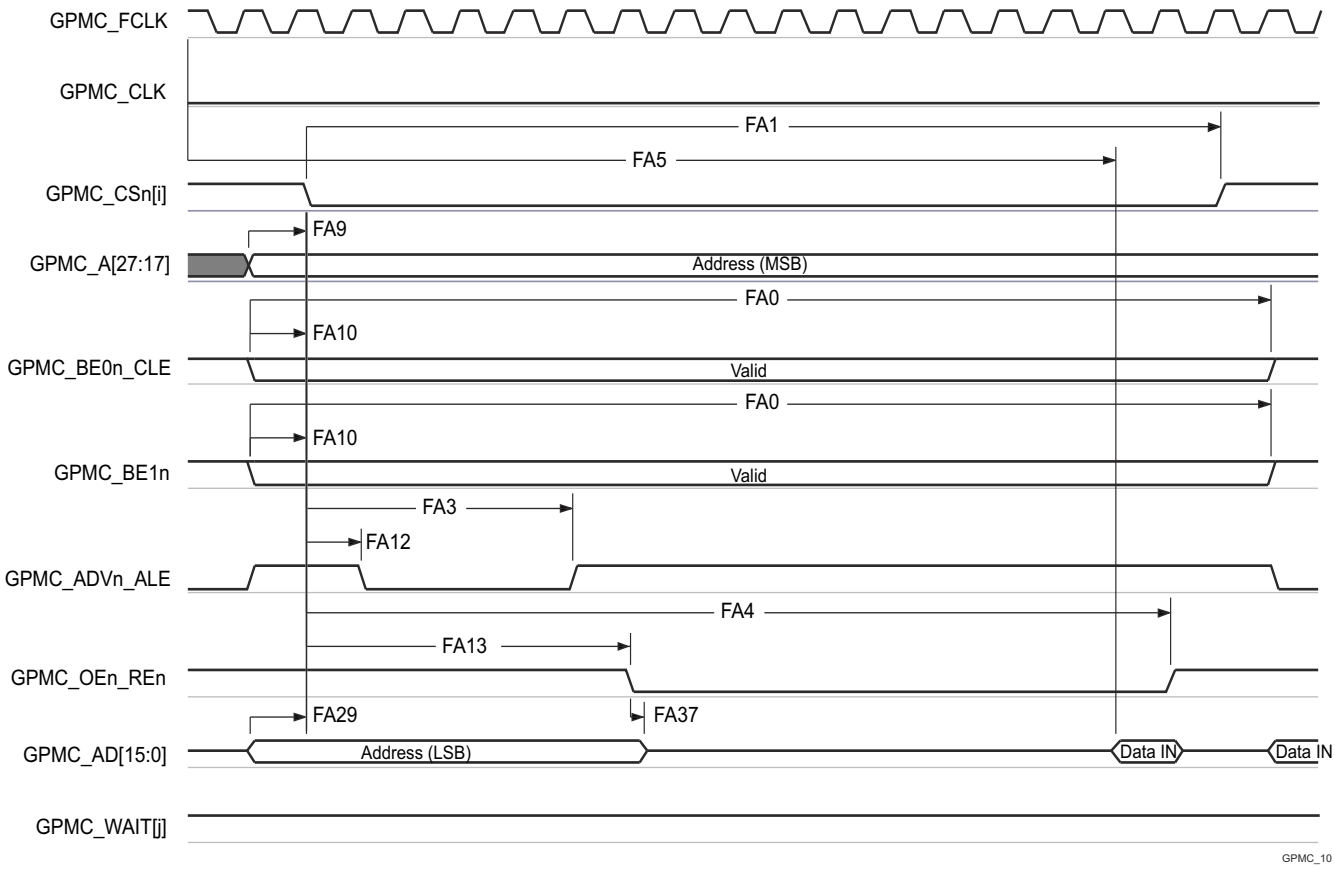

A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-56. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word

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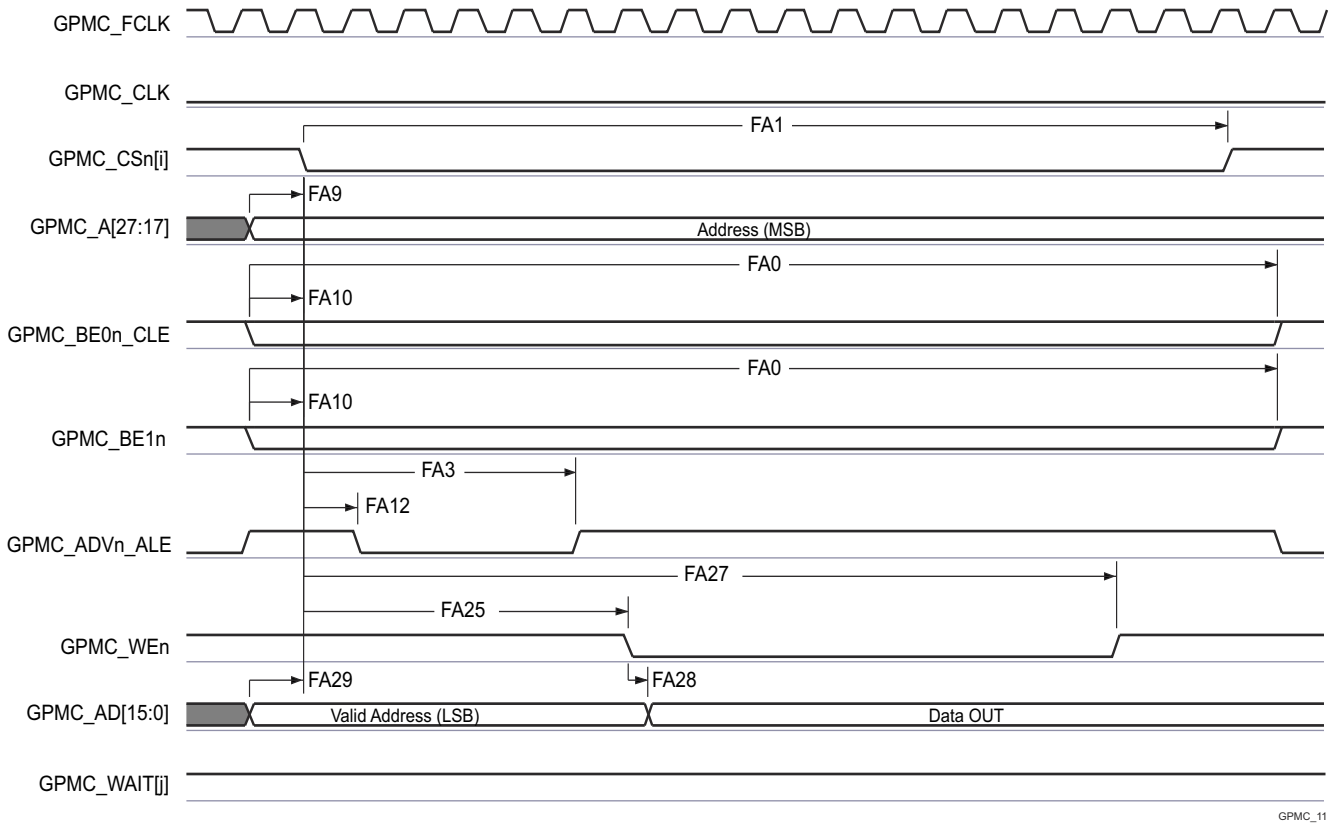

A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-57. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word

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6.9.5.13.3 GPMC and NAND Flash — Asynchronous Mode

Table 6-69 and Table 6-70 present timing requirements and switching characteristics for GPMC and NAND Flash — Asynchronous Mode.

Table 6-69. GPMC and NAND Flash Timing Requirements – Asynchronous Mode

see Figure 6-60

NO.	PARAMETER	DESCRIPTION	MODE (4)	MIN MAX	UNIT
				133MHz	
GNF12 (1)	$t_{acc(d)}$	Access time, input data GPMC_AD[15:0] (3)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J (2)	ns

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
(2) J = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(3)
(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(4) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

Table 6-70. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode

see Figure 6-58, Figure 6-59, Figure 6-60 and Figure 6-61

NO.	PARAMETER		MODE (4)	MIN	MAX	UNIT
GNF0	$t_{w(wenV)}$	Pulse duration, output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	A		ns
GNF1	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i](2) valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2	B + 2	ns
GNF2	$t_{w(cleH-wenV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2	C + 2	ns
GNF3	$t_{w(wenV-dV)}$	Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2	D + 2	ns
GNF4	$t_{w(wenIV-dIV)}$	Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E - 2	E + 2	ns
GNF5	$t_{w(wenIV-cleIV)}$	Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2	F + 2	ns
GNF6	$t_{w(wenIV-CSn[i]V)}$	Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CSn[i](2) invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G - 2	G + 2	ns
GNF7	$t_{w(aleH-wenV)}$	Delay time, output address valid and address latch enable GPMC_ADVn_ALE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2	C + 2	ns

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Table 6-70. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode (continued)

see Figure 6-58, Figure 6-59, Figure 6-60 and Figure 6-61

NO.	PARAMETER		MODE [4]	MIN	MAX	UNIT
GNF8	$t_{w(wenIV-aleIV)}$	Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2	F + 2	ns
GNF9	$t_{c(wen)}$	Cycle time, write	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H	ns
GNF10	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[i][2] valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I - 2	I + 2	ns
GNF13	$t_{w(oenV)}$	Pulse duration, output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		K	ns
GNF14	$t_{c(oen)}$	Cycle time, read	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L		ns
GNF15	$t_{w(oenIV-CSn[i]V)}$	Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CSn[i][2] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	M - 2	M + 2	ns

(1) A = (WEOffTime - WEOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[3]
(2) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(4) For div_by_1_mode:

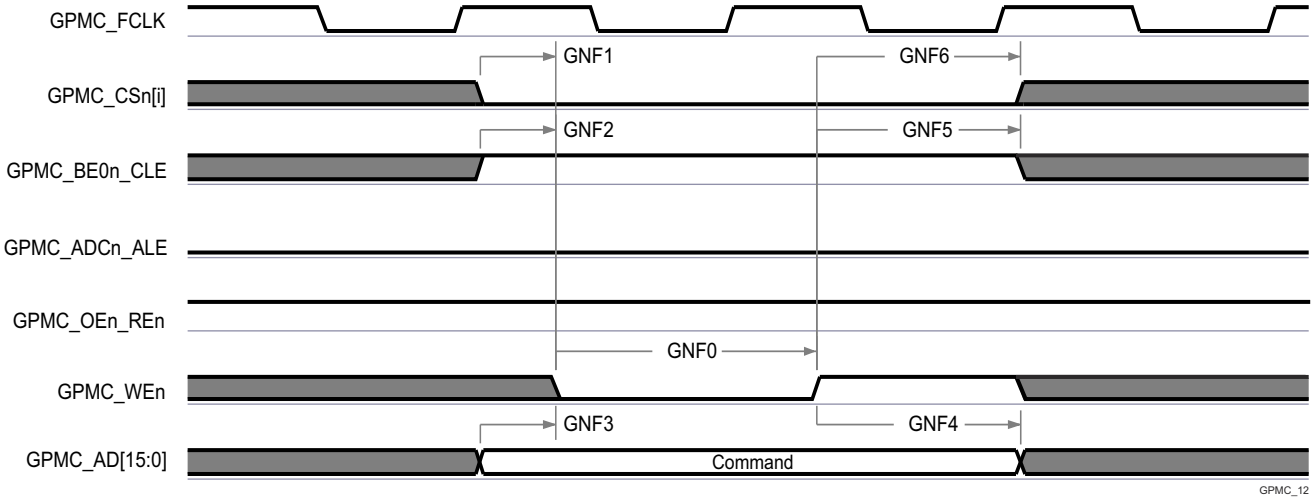
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 6-58. GPMC and NAND Flash — Command Latch Cycle

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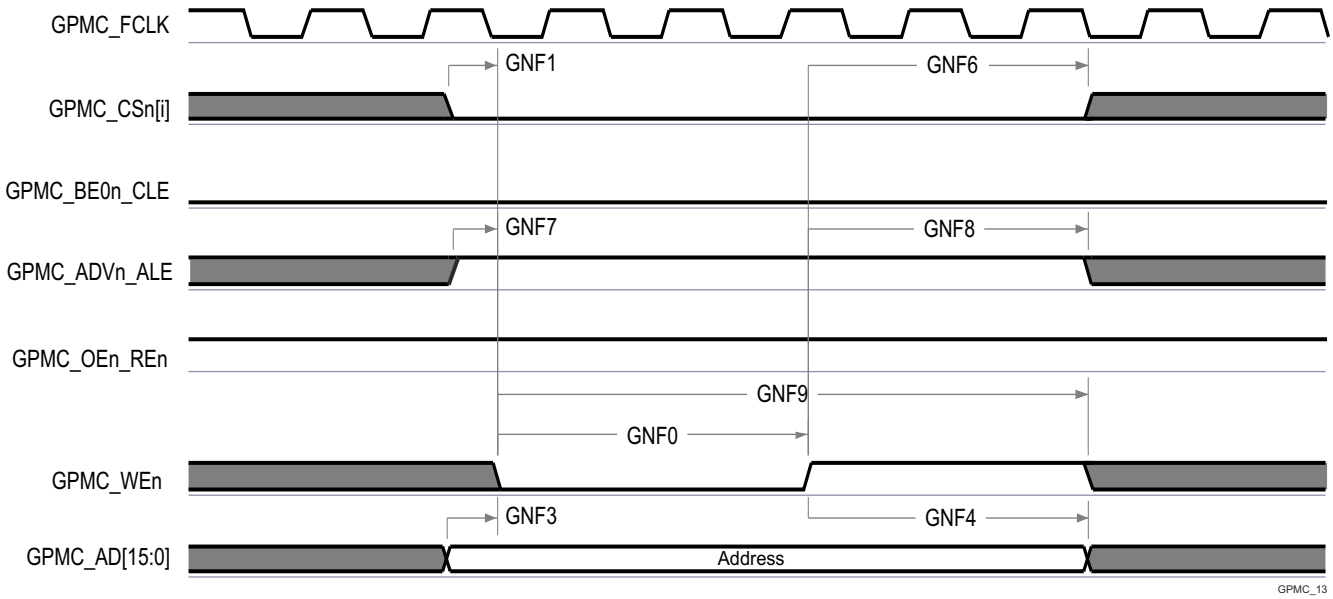
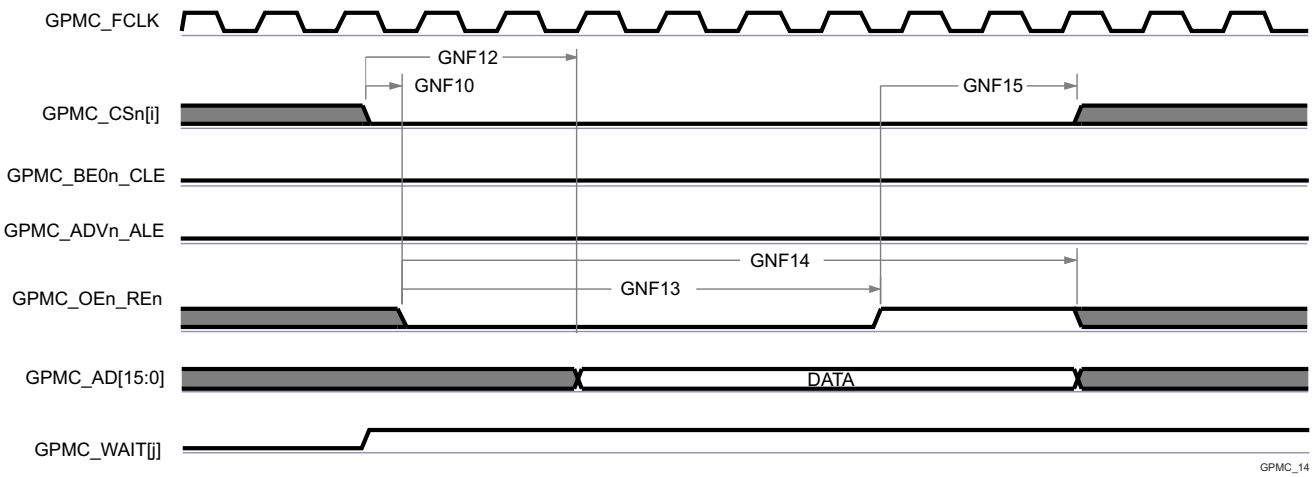


A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 6-59. GPMC and NAND Flash — Address Latch Cycle



A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
B. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
C. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-60. GPMC and NAND Flash — Data Read Cycle

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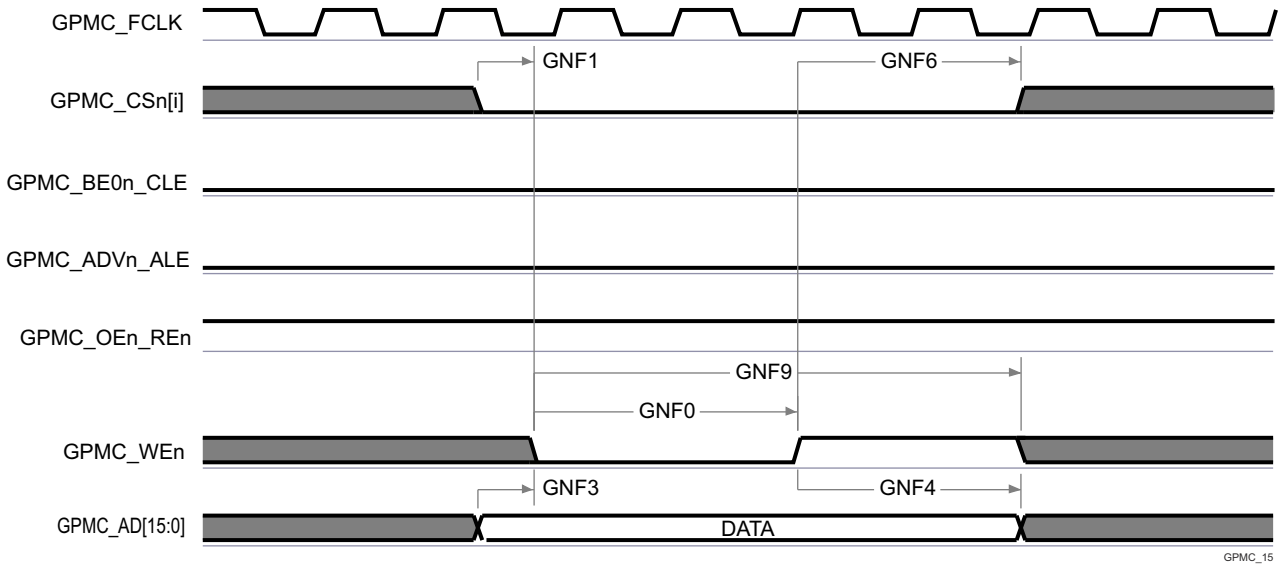

A. `In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 6-61. GPMC and NAND Flash — Data Write Cycle

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6.9.5.14 I2C

The device contains six multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I^{2}C-bus™ specification version 2.1. However, the device IOs are not fully compliant to the I2C electrical specification. The speeds supported and exceptions are described per port below:

- I2C0, I2C1, I2C2, and I2C3
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 1.8V
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 1.8V
      - 3.3V
  - Exceptions:
    - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because they are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.
- MCU_I2C0 and WKUP_I2C0
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 1.8V
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 1.8V
      - 3.3V
    - Hs-mode (up to 3.4Mbits/s)
      - 1.8V
  - Exceptions:
    - The IOs associated with these ports were not design to support Hs-mode while operating at 3.3V. So Hs-mode is limited to 1.8V operation.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.08V/ns (or 8E+7V/s) when operating at 3.3V. This limit is more restrictive than the minimum fall time limits defined in the I2C specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that they do not exceed a slew rate of 0.08V/ns.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.

Note

I2C3 has one or more signals which can be multiplexed to more than one pin. Timing is only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

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6.9.5.15 MCAN

Table 6-71 and Table 6-72 presents timing conditions and switching characteristics for MCAN.

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

Table 6-71. MCAN Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2	15	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	5	20	pF

Table 6-72. MCAN Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MCAN1	$t_{d(MCAN\_TX)}$	Delay time, transmit shift register to MCANn_TX		10	ns
MCAN2	$t_{d(MCAN\_RX)}$	Delay time, MCANn_RX to receive shift register		10	ns

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

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6.9.5.16 MCASP

Note

McASP has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

Table 6-73, Table 6-74, Figure 6-62, Table 6-75, and Figure 6-63 present timing conditions, timing requirements, and switching characteristics for MCASP.

Table 6-73. MCASP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.7	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	10	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	100	1100	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

Table 6-74. MCASP Timing Requirements

see Figure 6-62

NO.			MODE(1)	MIN	MAX	UNIT
ASP1	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X(4)		20		ns
ASP2	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X(4) high or low		0.5P(2) - 1.53		ns
ASP3	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X(4)		20		ns
ASP4	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X(4) high or low		0.5R(3) - 1.53		ns
ASP5	$t_{su(AFSRX-ACLKRX)}$	Setup time, MCASP[x]_AFSR/X(4) input valid before MCASP[x]_ACLKR/X(4)	ACLKR/X int	9.29		ns
			ACLKR/X ext in/out	4		
ASP6	$t_{h(ACLKRX-AFSRX)}$	Hold time, MCASP[x]_AFSR/X(4) input valid after MCASP[x]_ACLKR/X(4)	ACLKR/X int	-1		ns
			ACLKR/X ext in/out	1.6		
ASP7	$t_{su(AXR-ACLKRX)}$	Setup time, MCASP[x]_AXR(4) input valid before MCASP[x]_ACLKR/X(4)	ACLKR/X int	9.29		ns
			ACLKR/X ext in/out	4		
ASP8	$t_{h(ACLKRX-AXR)}$	Hold time, MCASP[x]_AXR(4) input valid after MCASP[x]_ACLKR/X(4)	ACLKR/X int	-1		ns
			ACLKR/X ext in/out	1.6		

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns. For details on AHCLKR/X clock source options, see the McASP Clocks table in the Multichannel Audio Serial Port (MCASP) section of the Module Integration chapter found in the Technical Reference Manual.
(3) R = ACLKR/X period in ns.
(4) x in MCASP[x]_* is 0, 1 or 2

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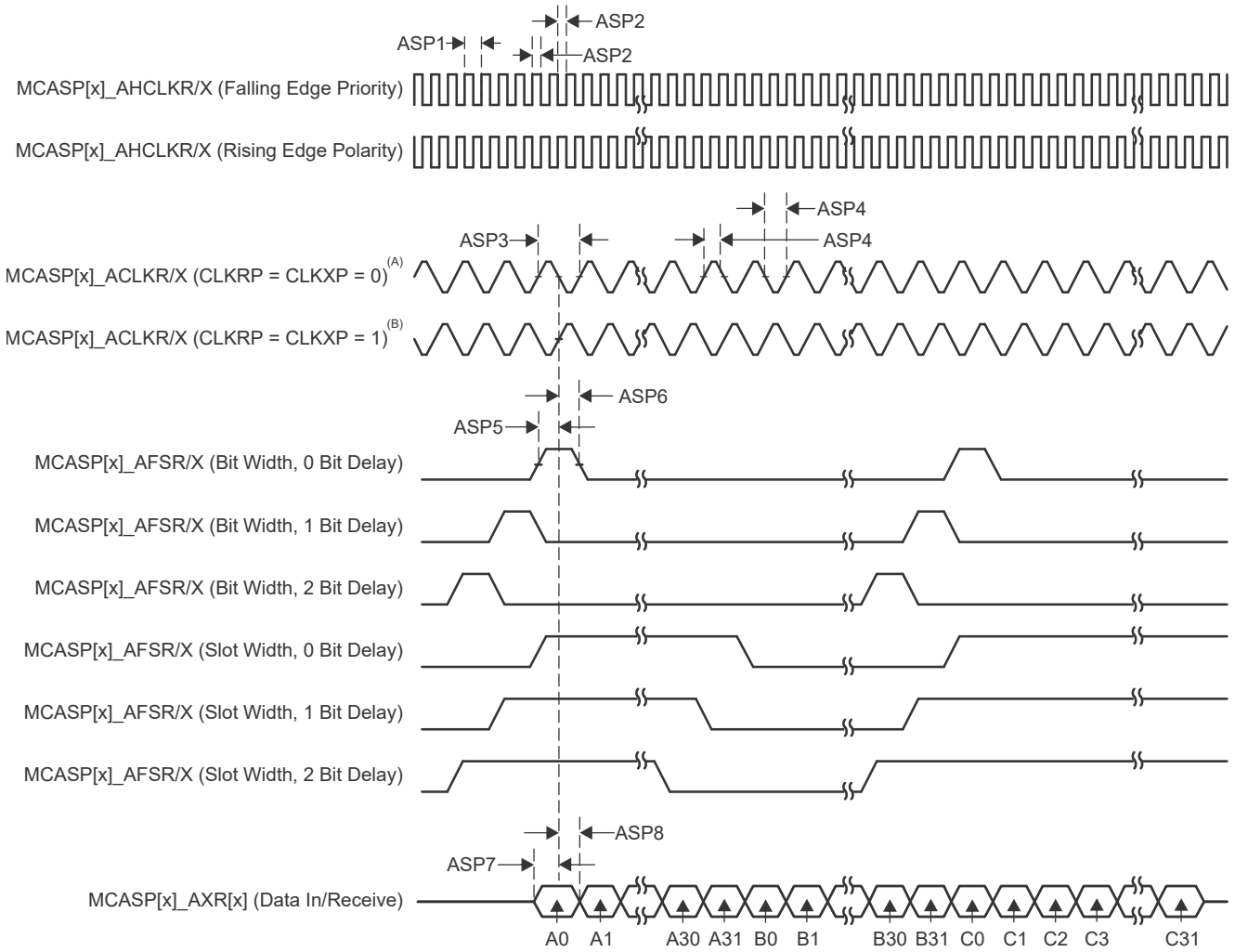

A. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

Figure 6-62. MCASP Timing Requirements

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Table 6-75. MCASP Switching Characteristics

see Figure 6-63

NO.	PARAMETER	DESCRIPTION	MODE(1)	MIN	MAX	UNIT
ASP9	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X(4)		20		ns
ASP10	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X(4) high or low		0.5P(2) - 2		ns
ASP11	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X(4)		20		ns
ASP12	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X(4) high or low		0.5R(3) - 2		ns
ASP13	$t_{d(ACLKRX-AFSRX)}$	Delay time, MCASP[x]_ACLKR/X(4) transmit edge to MCASP[x]_AFSR/X(4) output valid	ACLKR/X int	-1	7.25	ns
			ACLKR/X ext in/out	-15.29	12.84	
ASP14	$t_{d(ACLKX-AXR)}$	Delay time, MCASP[x]_ACLKX(4) transmit edge to MCASP[x]_AXR(4) output valid	ACLKR/X int	-1	7.25	ns
			ACLKR/X ext in/out	-15.29	12.84	
ASP15	$t_{dis(ACLKX-AXR)}$	Disable time, MCASP[x]_ACLKX(4) transmit edge to MCASP[x]_AXR(4) output high impedance	ACLKR/X int	-1	7.25	ns
			ACLKR/X ext in/out	-14.9	14	

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns. For details on AHCLKR/X clock source options, see the McASP Clocks table in the Multichannel Audio Serial Port (MCASP) section of the Module Integration chapter found in the Technical Reference Manual.
(3) R = ACLKR/X period in ns.
(4) x in MCASP[x]_* is 0, 1 or 2

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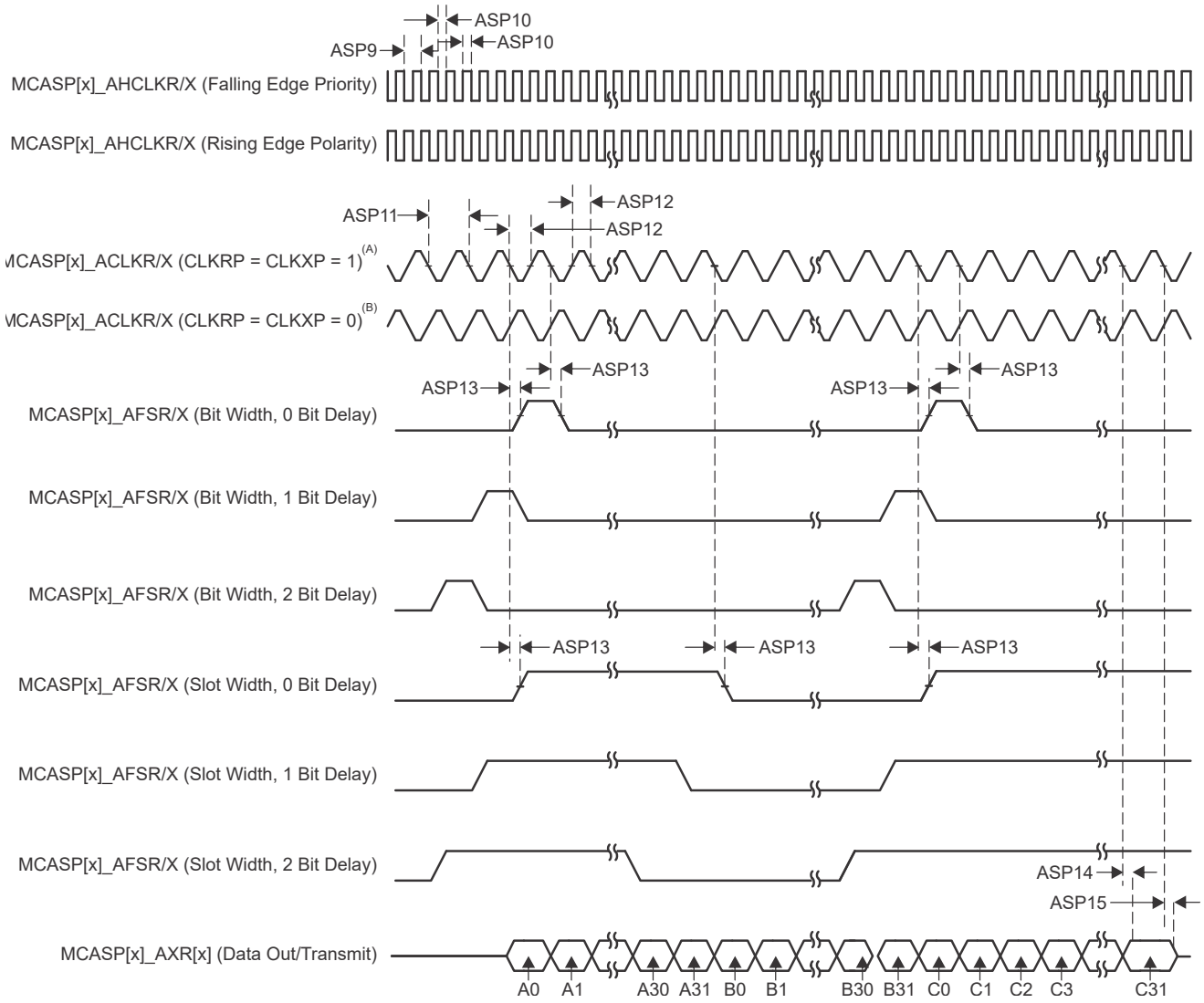

A. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

Figure 6-63. MCASP Switching Characteristics

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

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6.9.5.17 MCSPI

Note

McSPI has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

For more details about features and additional description information on the device Serial Port Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 6-76 presents timing conditions for MCSPI.

Table 6-76. MCSPI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2	8.5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	6	12	pF

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

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6.9.5.17.1 MCSPI — Controller Mode

Table 6-77, Figure 6-64, Table 6-78, and Figure 6-65 present timing requirements and switching characteristics for SPI – Controller Mode.

Table 6-77. MCSPI Timing Requirements – Controller Mode

see Figure 6-64

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SM4	$t_{su(POCI-SPICLK)}$	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	2.8		ns
SM5	$t_{h(SPICLK-POCI)}$	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	3		ns

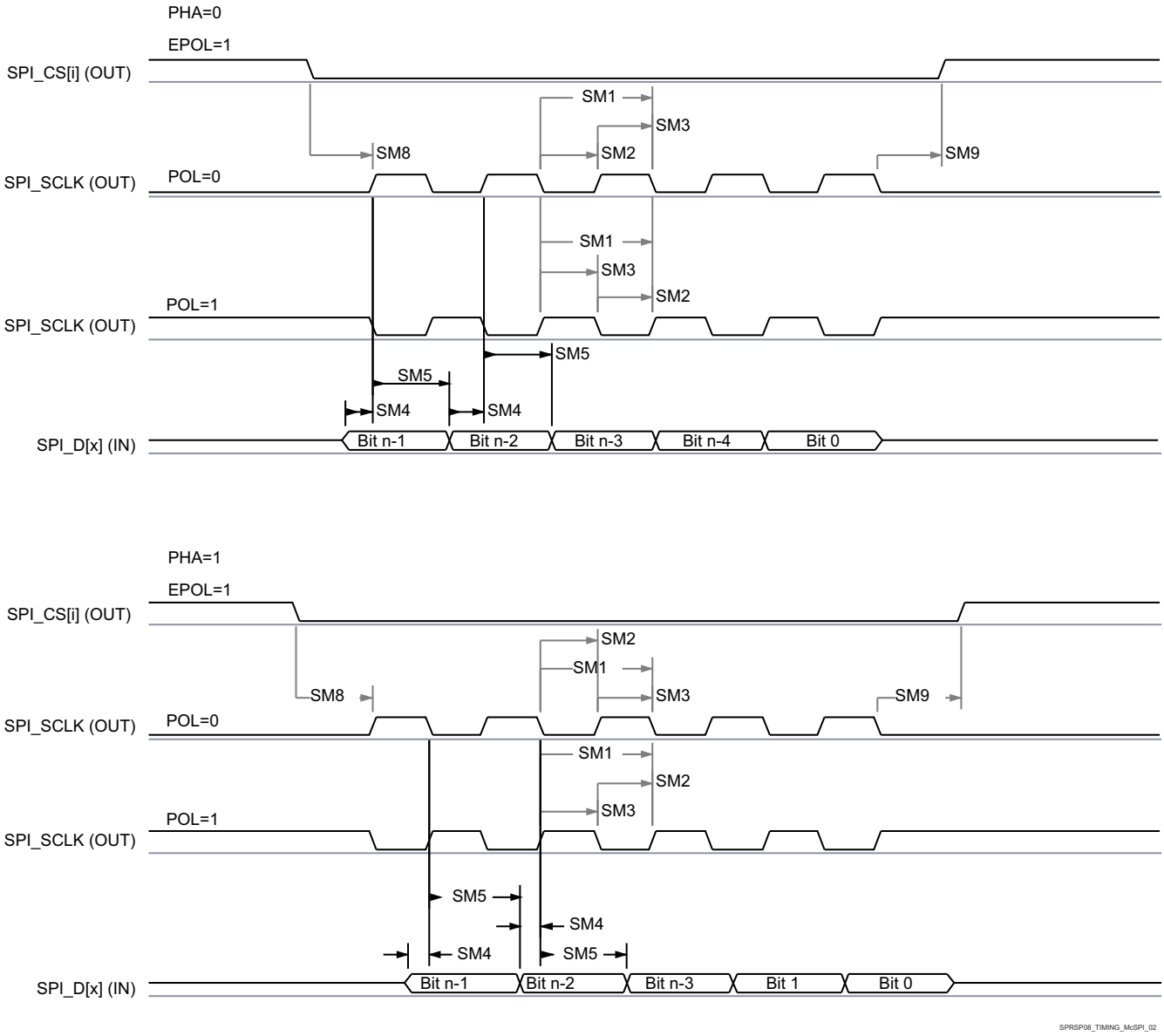

Figure 6-64. SPI Controller Mode Receive Timing

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Table 6-78. MCSPI Switching Characteristics - Controller Mode

see Figure 6-65

NO.	PARAMETER			MIN	MAX	UNIT
SM1	$t_{c(SPICLK)}$	Cycle time, SPIn_CLK		20		ns
SM2	$t_{w(SPICLKL)}$	Pulse duration, SPIn_CLK low		0.5P - 1 (1)		ns
SM3	$t_{w(SPICLKH)}$	Pulse duration, SPIn_CLK high		0.5P - 1 (1)		ns
SM6	$t_{d(SPICLK-PICO)}$	Delay time, SPIn_CLK active edge to SPIn_D[x]		-3	2.5	ns
SM7	$t_{d(CS-PICO)}$	Delay time, SPIn_CSi active edge to SPIn_D[x]		5		ns
SM8	$t_{d(CS-SPICLK)}$	Delay time, SPIn_CSi active to SPIn_CLK first edge	PHA = 0	B - 4 (2)		ns
			PHA = 1	A - 4 (3)		ns
SM9	$t_{d(SPICLK-CS)}$	Delay time, SPIn_CLK last edge to SPIn_CSi inactive	PHA = 0	A - 4 (4)		ns
			PHA = 1	B - 4 (5)		ns

(1) P = SPIn_CLK period in ns.

(2) T_ref is the period of the McSPI functional clock in ns. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.
- When Fratio = 1; B = (TCS(i) + 0.5) * T_ref.
- When Fratio ≥ 2 and even value; B = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; B = ((TCS(i) * Fratio) + ((Fratio + 1) / 2)) * T_ref.

(3) T_ref is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.
- When Fratio = 1; A = (TCS(i) + 1) * T_ref.
- When Fratio ≥ 2 and even value; A = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; A = ((TCS(i) * Fratio) + ((Fratio - 1) / 2)) * T_ref.

(4) T_ref is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.
- When Fratio = 1; A = (TCS(i) + 1) * T_ref.
- When Fratio ≥ 2 and even value; A = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; A = ((TCS(i) * Fratio) + ((Fratio + 1) / 2)) * T_ref.

(5) T_ref is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.
- When Fratio = 1; B = (TCS(i) + 0.5) * T_ref.
- When Fratio ≥ 2 and even value; B = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; B = ((TCS(i) * Fratio) + ((Fratio - 1) / 2)) * T_ref.

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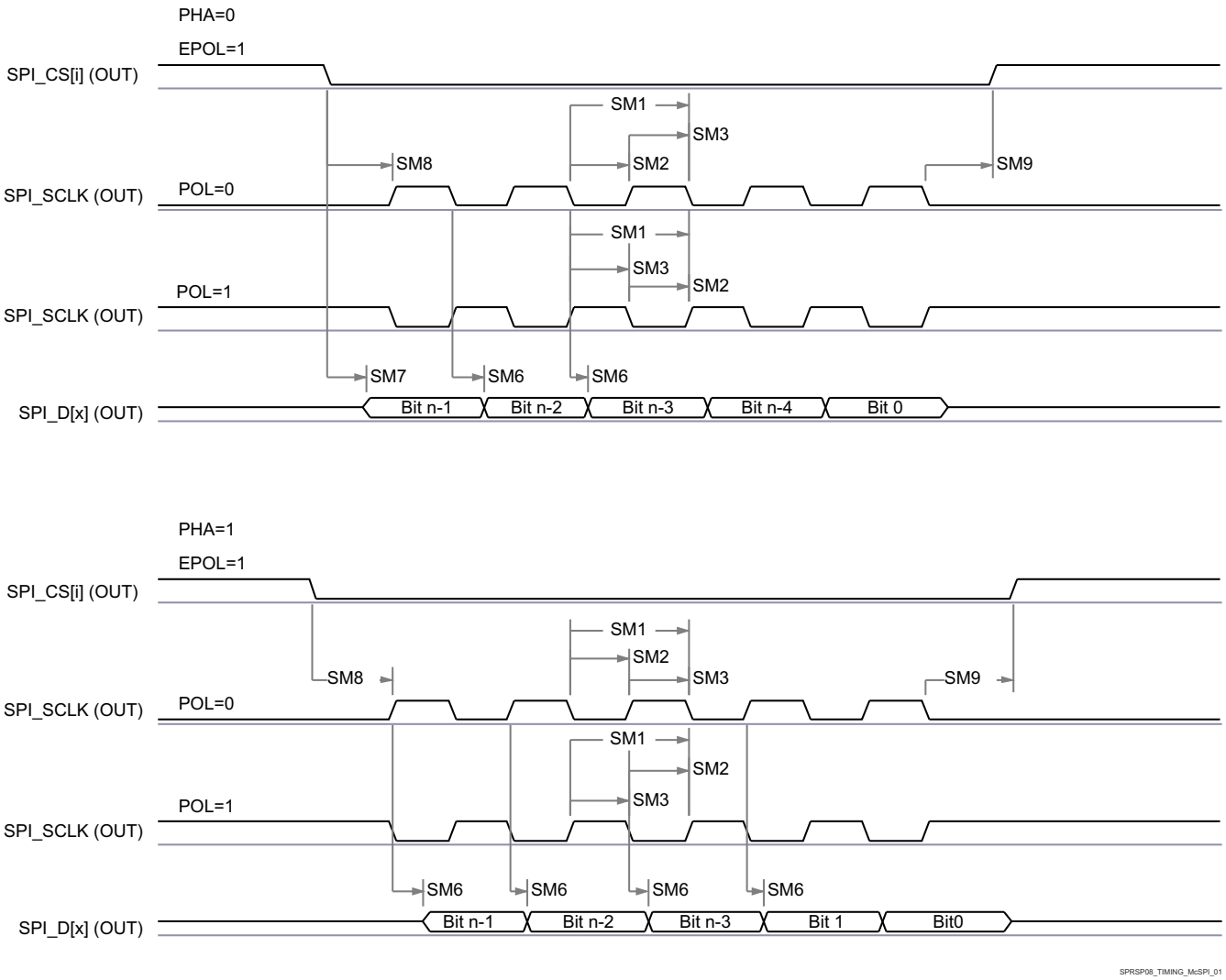

Figure 6-65. SPI Controller Mode Transmit Timing

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6.9.5.17.2 MCSPI — Peripheral Mode

Table 6-79, Figure 6-66, Table 6-80, and Figure 6-67 present timing requirements and switching characteristics for SPI – Peripheral Mode.

Table 6-79. MCSPI Timing Requirements – Peripheral Mode

see Figure 6-66

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS1	$t_{c(SPICLK)}$	Cycle time, SPIn_CLK	20		ns
SS2	$t_{w(SPICLKL)}$	Pulse duration, SPIn_CLK low	0.45P (1)		ns
SS3	$t_{w(SPICLKH)}$	Pulse duration, SPIn_CLK high	0.45P (1)		ns
SS4	$t_{su(PICO-SPICLK)}$	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	5		ns
SS5	$t_{h(SPICLK-PICO)}$	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	5		ns
SS8	$t_{su(CS-SPICLK)}$	Setup time, SPIn_CSi valid before SPIn_CLK first edge	5		ns
SS9	$t_{h(SPICLK-CS)}$	Hold time, SPIn_CSi valid after SPIn_CLK last edge	5		ns

(1) P = SPIn_CLK period in ns.

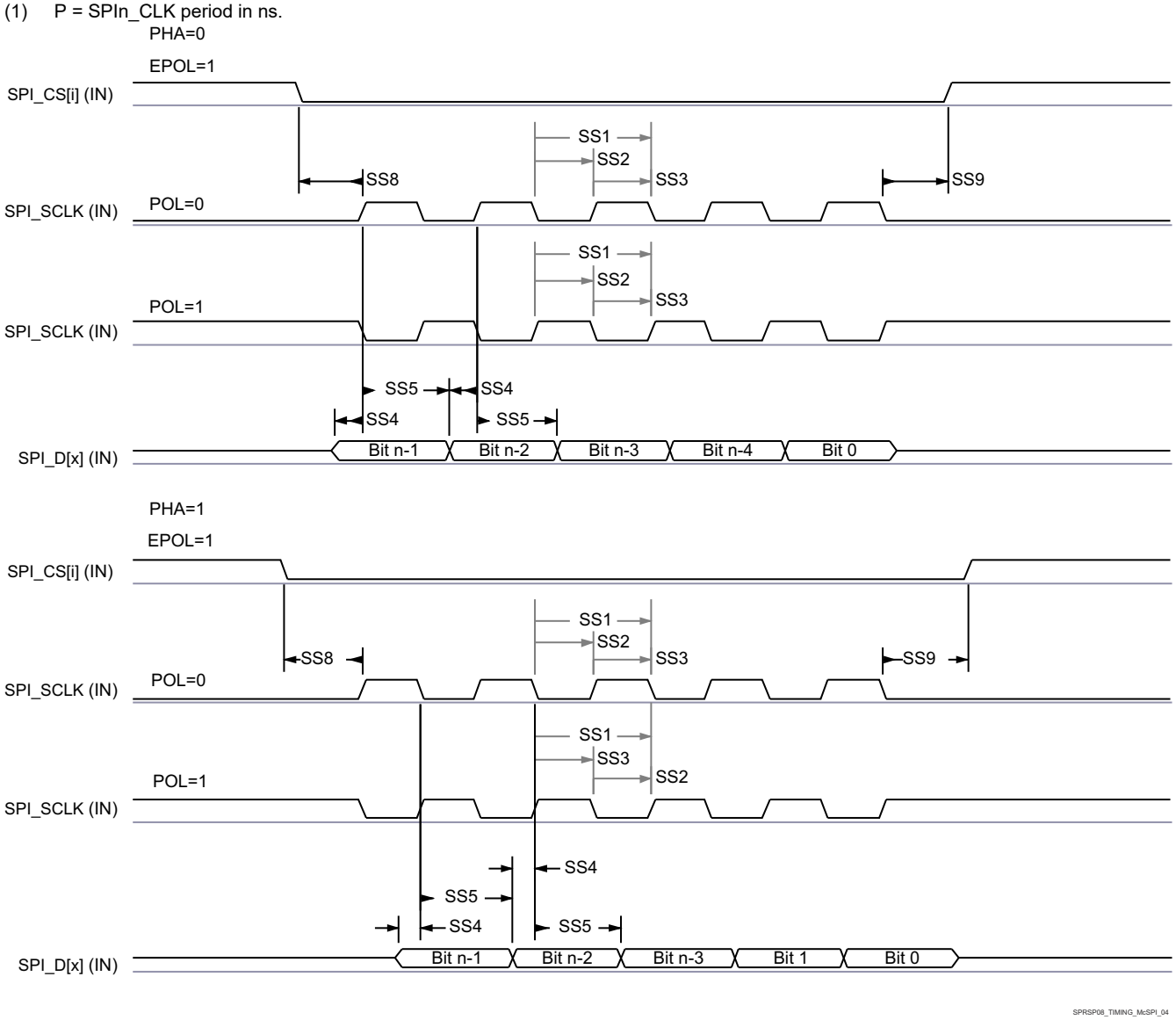

Figure 6-66. SPI Peripheral Mode Receive Timing

Table 6-80. MCSPI Switching Characteristics – Peripheral Mode

see Figure 6-67

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS6	$t_{d(SPICLK-POCI)}$	Delay time, SPIn_CLK active edge to SPIn_D[x]	2	17.12	ns
SS7	$t_{sk(CS-POCI)}$	Delay time, SPIn_CSi active edge to SPIn_D[x]	20.95		ns

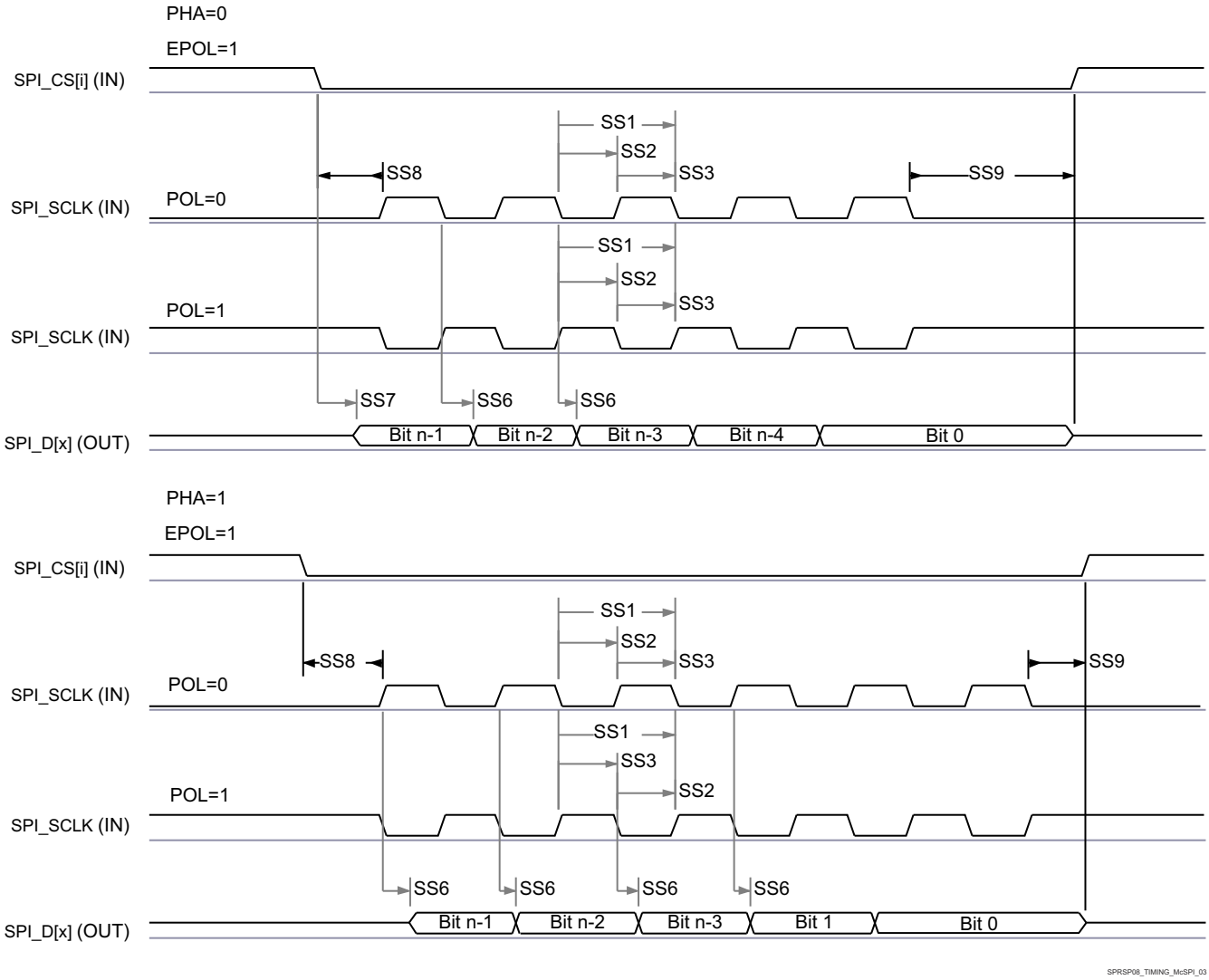

Figure 6-67. SPI Peripheral Mode Transmit Timing

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6.9.5.18 MMCSD

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC), Secure Digital (SD), and Secure Digital IO (SDIO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSD interfaces, see the corresponding MMC0, MMC1, and MMC2 subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

Some operating modes require software configuration of the MMC DLL delay settings, as shown in Table 6-81 and Table 6-99.

The modes which show a value of "Tuning" in the ITAPDLYSEL column of Table 6-81 and Table 6-99 require a tuning algorithm to be used for optimizing input timing. Refer to the MMCSD Programming Guide in the device TRM for more information on the tuning algorithm and configuration of input delays required to optimize input timing.

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

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6.9.5.18.1 MMC0 - eMMC Interface

MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and it supports the following eMMC applications:

- Legacy SDR
- High Speed SDR
- High Speed DDR
- HS200
- HS400

Table 6-81 presents the required DLL software configuration settings for MMC0 timing modes.

Table 6-81. MMC0 DLL Delay Mapping for all Timing Modes

REGISTER NAME		MMCSD0_SS_PHY_CTRL_x_REG								
		x = 4					x = 5			x = 1
BIT FIELD		[31:24]	[20]	[15:12]	[8]	[4:0]	[17:16]	[10:8]	[2:0]	[1]
BIT FIELD NAME		STRBSEL	OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	SELDLYTXCLK SELDLYRXCLK	FRQSEL	CLKBUFSEL	ENDLL
MODE	DESCRIPTION	STROBE DELAY	OUTPUT DELAY ENABLE	OUTPUT DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DLL DELAY CHAIN SELECT	DLL REF FREQUENCY	DELAY BUFFER DURATION	ENABLE DLL
Legacy SDR	8-bit PHY operating 1.8V, 25MHz	0x0	0x1	0x1	0x1	0x10	0x3	NA(1)	0x7	0x0
High Speed SDR	8-bit PHY operating 1.8V, 50MHz	0x0	0x1	0x1	0x1	0xA	0x3	NA(1)	0x7	0x0
High Speed DDR	8-bit PHY operating 1.8V, 50MHz	0x0	0x1	0x6	0x1	0x3	0x0	0x4	NA(1)	0x1
HS200	8-bit PHY operating 1.8V, 200MHz	0x0	0x1	0x8	0x1	Tuning(2)	0x0	0x0	NA(1)	0x1
HS400	8-bit PHY operating 1.8V, 200MHz	0x77	0x1	0x5	0x1	Tuning(2)	0x0	0x0	NA(1)	0x1

(1) NA means Not Applicable
(2) Tuning means this mode requires a tuning algorithm to be used for optimal input timing

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Table 6-82 presents timing conditions for MMC0.

Table 6-82. MMC0 Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	Legacy SDR High Speed SDR	0.3	0.9	V/ns
		High Speed DDR (CMD)	0.3	0.9	V/ns
		High Speed DDR (DAT)	0.45	0.9	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	HS400	1	6	pF
		All other modes	1	12	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	All modes	126	756	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	HS200 HS400		8	ps
		High Speed DDR		20	ps
		All other modes		100	ps

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6.9.5.18.1.1 Legacy SDR Mode

Table 6-83, Figure 6-68, Table 6-84, and Figure 6-69 present timing requirements and switching characteristics for MMC0 – Legacy SDR Mode.

Table 6-83. MMC0 Timing Requirements – Legacy SDR Mode

see Figure 6-68

NO.			IO Operating Voltage	MIN	MAX	UNIT
LSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	1.8V	4.2		ns
			3.3V	2.15		ns
LSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	1.8V	0.87		ns
			3.3V	1.67		ns
LSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	1.8V	4.2		ns
			3.3V	2.15		ns
LSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	1.8V	0.87		ns
			3.3V	1.67		ns

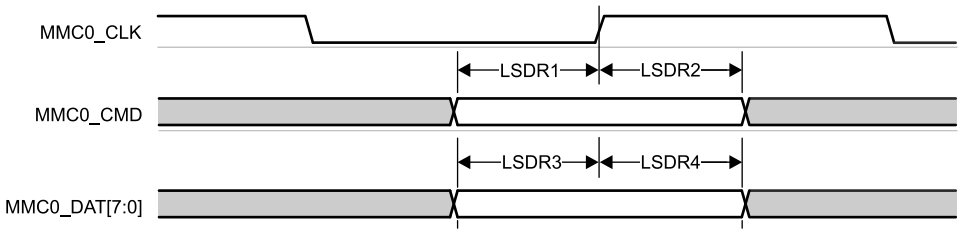

Figure 6-68. MMC0 – Legacy SDR – Receive Mode

Table 6-84. MMC0 Switching Characteristics – Legacy SDR Mode

see Figure 6-69

NO.	PARAMETER		IO Operating Voltage	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK			25	MHz
LSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK		40		ns
LSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high		18.7		ns
LSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low		18.7		ns
LSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	1.8V	-2.1	2.1	ns
			3.3V	-1.8	2.2	ns
LSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	1.8V	-2.1	2.1	ns
			3.3V	-1.8	2.2	ns

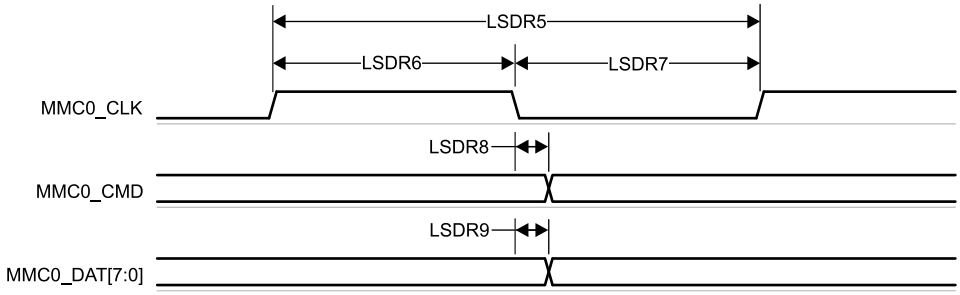

Figure 6-69. MMC0 – Legacy SDR – Transmit Mode

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6.9.5.18.1.2 High Speed SDR Mode

Table 6-85, Figure 6-70, Table 6-86, and Figure 6-71 present timing requirements and switching characteristics for MMC0 – High Speed SDR Mode.

Table 6-85. MMC0 Timing Requirements – High Speed SDR Mode

see Figure 6-70

NO.			IO Operating Voltage	MIN	MAX	UNIT
HSSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	1.8V	2.15		ns
			3.3V	2.24		ns
HSSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	1.8V	1.27		ns
			3.3V	1.66		ns
HSSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	1.8V	2.15		ns
			3.3V	2.24		ns
HSSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	1.8V	1.27		ns
			3.3V	1.66		ns

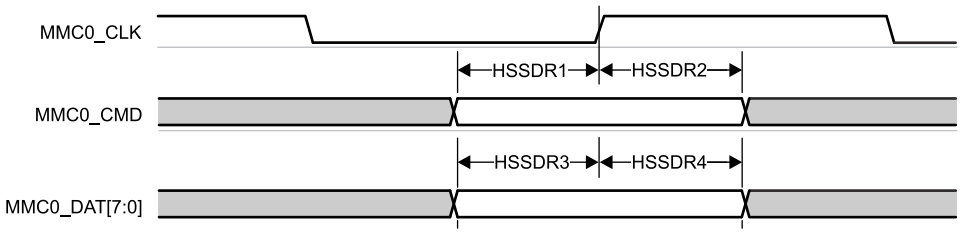

Figure 6-70. MMC0 – High Speed SDR Mode – Receive Mode

Table 6-86. MMC0 Switching Characteristics – High Speed SDR Mode

see Figure 6-71

NO.	PARAMETER		IO Operating Voltage	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK			50	MHz
HSSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK		20		ns
HSSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high		9.2		ns
HSSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low		9.2		ns
HSSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	1.8V	-1.55	3.05	ns
			3.3V	-1.8	2.2	ns
HSSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	1.8V	-1.55	3.05	ns
			3.3V	-1.8	2.2	ns

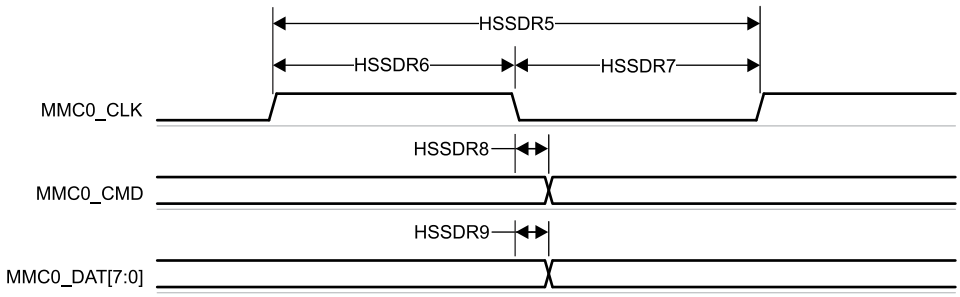

Figure 6-71. MMC0 – High Speed SDR Mode – Transmit Mode

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6.9.5.18.1.3 High Speed DDR Mode

Table 6-87, Figure 6-72, Table 6-88, and Figure 6-73 present timing requirements and switching characteristics for MMC0 – High Speed DDR Mode.

Table 6-87. MMC0 Timing Requirements – High Speed DDR Mode

see Figure 6-72

NO.			MIN	MAX	UNIT
HSDDR1	$t_{su(cmdV-clk)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	1.62		ns
HSDDR2	$t_{h(clk-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	2.52		ns
HSDDR3	$t_{su(dV-clk)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK transition	0.83		ns
HSDDR4	$t_{h(clk-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK transition	1.76		ns

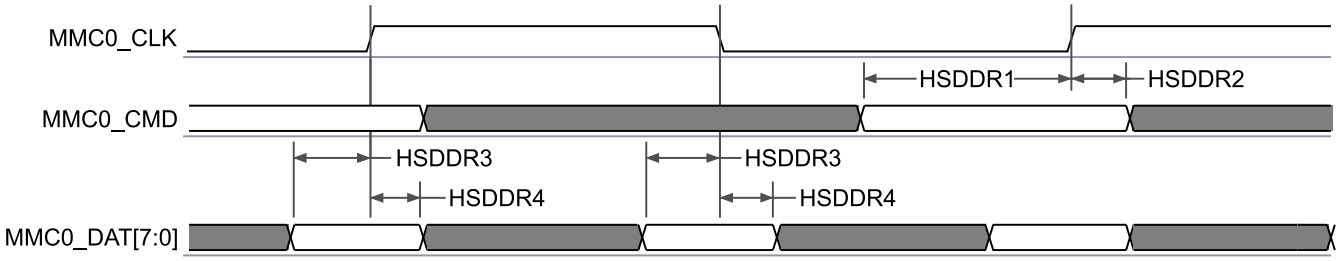

Figure 6-72. MMC0 – High Speed DDR Mode – Receive Mode

Table 6-88. MMC0 Switching Characteristics – High Speed DDR Mode

see Figure 6-73

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
HSDDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
HSDDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
HSDDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
HSDDR8	$t_{d(clk-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	3.31	7.65	ns
HSDDR9	$t_{d(clk-dV)}$	Delay time, MMC0_CLK transition to MMC0_DAT[7:0] transition	2.81	6.94	ns

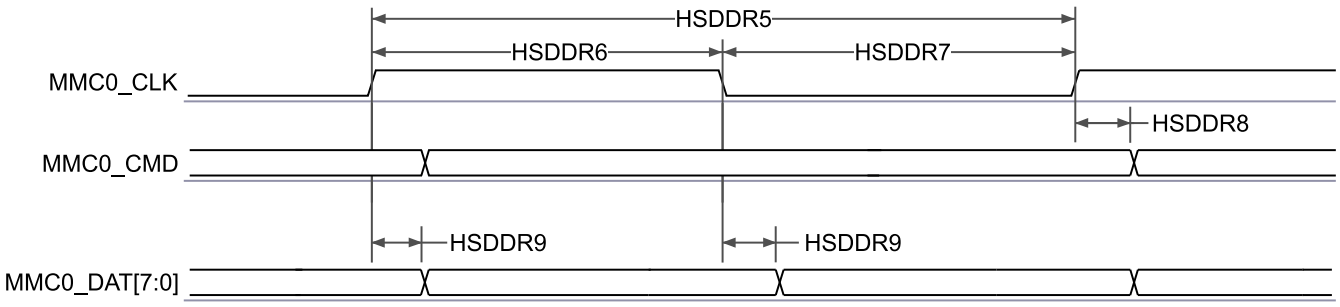

Figure 6-73. MMC0 – High Speed DDR Mode – Transmit Mode

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6.9.5.18.1.4 HS200 Mode

Table 6-89 and Figure 6-74 present switching characteristics for MMC0 – HS200 Mode.

Table 6-89. MMC0 Switching Characteristics – HS200 Mode

see Figure 6-74

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		200	MHz
HS2005	$t_{c(clk)}$	Cycle time, MMC0_CLK	5		ns
HS2006	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	2.12		ns
HS2007	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	2.12		ns
HS2008	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.07	3.21	ns
HS2009	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[7:0] transition	1.07	3.21	ns

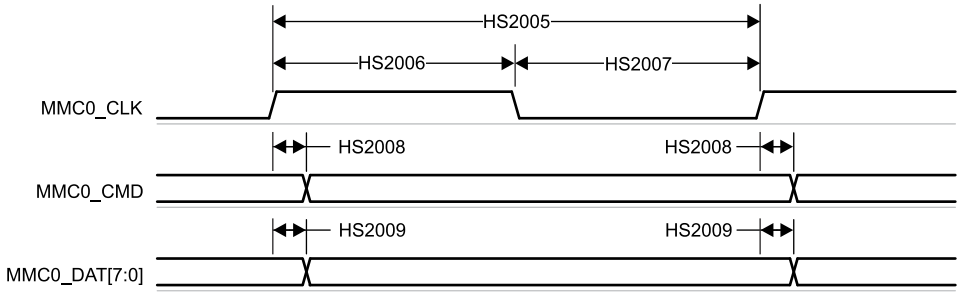

Figure 6-74. MMC0 – HS200 Mode – Transmit Mode

6.9.5.18.1.5 HS400 Mode

Table 6-90, Figure 6-75, Table 6-91, and Figure 6-76 present timing requirements and switching characteristics for MMC0 – HS400 Mode.

Table 6-90. MMC0 Timing Requirements – HS400 Mode

see Figure 6-75

NO.			MIN	MAX	UNIT
HS4000	t_{DSMPW}	Pulse width, MMC0_DS	2.0		ns
HS4001	t_{RQ_DAT}	Input skew, MMC0_DS to MMC0_DAT valid		475	ps
HS4002	t_{RQH_DAT}	Input skew hold, MMC0_DAT invalid to MMC0_DS		475	ps
HS4003	t_{RQ_CMD}	Input skew, MMC0_DS to MMC0_CMD valid		475	ps
HS4004	t_{RQH_CMD}	Input skew hold, MMC0_CMD invalid to MMC0_DS		475	ps

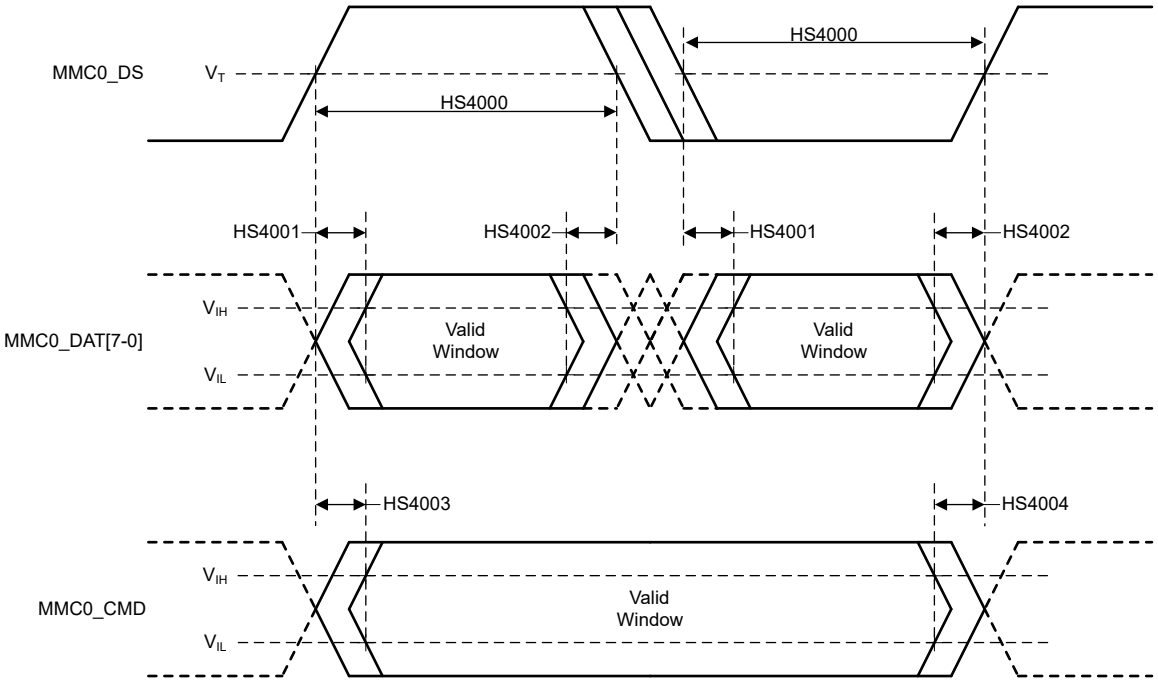

Figure 6-75. MMC0 – HS400 – Receive Mode

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Table 6-91. MMC0 Switching Characteristics – HS400 Mode

see Figure 6-76

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		200	MHz
HS4005	$t_{c(clkH)}$	Cycle time, MMC0_CLK	5		ns
HS4006	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	2.24		ns
HS4007	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	2.24		ns
HS4008	$t_{osu(cmdV-clkH)}$	Output setup time, MMC0_CMD valid to MMC0_CLK rising edge(1)	2.58		ns
HS4009	$t_{osu(dV-clk)}$	Output setup time, MMC0_DAT[7:0] valid to MMC0_CLK rising or falling edge(1)	0.60		ns
HS40010	$t_{oh(clkH-cmdIV)}$	Output hold time, MMC0_CLK rising edge to MMC0_CMD invalid(2)	1.12		ns
HS40011	$t_{oh(clk-dIV)}$	Output hold time, MMC0_CLK rising or falling edge to MMC0_DAT[7:0] invalid(2)	0.85		ns

(1) This parameter defines the output setup time provided to the attached device. This time is relative to the next capture clock edge and already includes the maximum propagation delay mismatch value defined in the *MMC0 Timing Conditions* table. The timing references for this parameter are from mid-supply of the DAT or CMD signal transition to mid-supply of the CLK signal transition. The eMMC standard defines the setup timing references from VIL or VIH of the DAT or CMD signal transition to mid-supply of the CLK signal transition. Therefore, the system designer must consider the impact of the DAT signal slew rate when designing the PCB, and ensure the time it takes for the DAT signal to slew from mid-supply to VIL or VIH does not erode the setup time margin.

(2) This parameter defines the output hold time provided to the attached device. This time is relative to the previous launch clock edge and already includes the maximum propagation delay mismatch value defined in the *MMC0 Timing Conditions* table. The timing references for this parameter are from mid-supply of the CLK signal transition to mid-supply of the DAT or CMD signal transition. The eMMC standard defines the hold timing references from mid-supply of the CLK signal transition to VIL or VIH of the DAT or CMD signal transition. Therefore, the system designer must consider the impact of the DAT signal slew rate when designing the PCB, and ensure the time it takes for the DAT signal to slew from VIL or VIH to mid-supply does not erode the hold time margin.

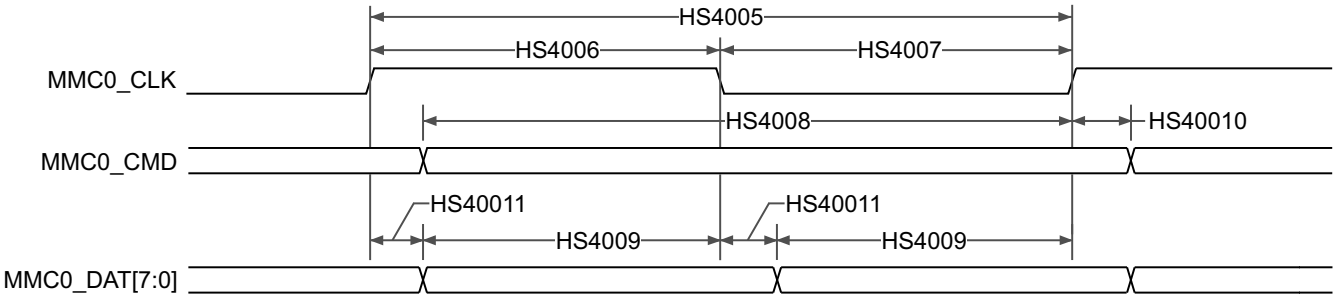

Figure 6-76. eMMC in – HS400 Mode – Transmitter Mode

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6.9.5.18.1.6 UHS–I SDR12 Mode

Table 6-92, Figure 6-77, Table 6-93, and Figure 6-78 present timing requirements and switching characteristics for MMC0 – UHS-I SDR12 Mode.

Table 6-92. Timing Requirements for MMC0 – UHS-I SDR12 Mode

see Figure 6-77

NO.			MIN	MAX	UNIT
SDR121	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	4.2		ns
SDR122	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	0.87		ns
SDR123	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[3:0] valid before MMC0_CLK rising edge	4.2		ns
SDR124	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[3:0] valid after MMC0_CLK rising edge	0.87		ns

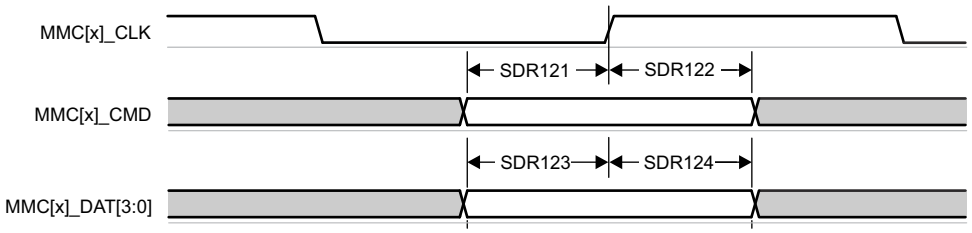

Figure 6-77. MMC0 – UHS-I SDR12 – Receive Mode

Table 6-93. Switching Characteristics for MMC0 – UHS-I SDR12 Mode

see Figure 6-78

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		25	MHz
SDR125	$t_{c(clk)}$	Cycle time, MMC0_CLK	40		ns
SDR126	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	18.7		ns
SDR127	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	18.7		ns
SDR128	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.5	8.6	ns
SDR129	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[3:0] transition	1.5	8.6	ns

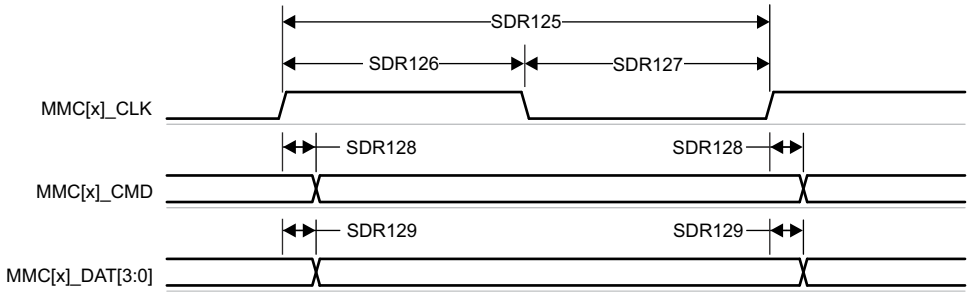

Figure 6-78. MMC0 – UHS-I SDR12 – Transmit Mode

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6.9.5.18.1.7 UHS–I SDR25 Mode

Table 6-94, Figure 6-79, Table 6-95, and Figure 6-80 present timing requirements and switching characteristics for MMC0 – UHS-I SDR25 Mode.

Table 6-94. Timing Requirements for MMC0 – UHS-I SDR25 Mode

see Figure 6-79

NO.			MIN	MAX	UNIT
SDR251	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2.15		ns
SDR252	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	1.27		ns
SDR253	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[3:0] valid before MMC0_CLK rising edge	2.15		ns
SDR254	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[3:0] valid after MMC0_CLK rising edge	1.27		ns

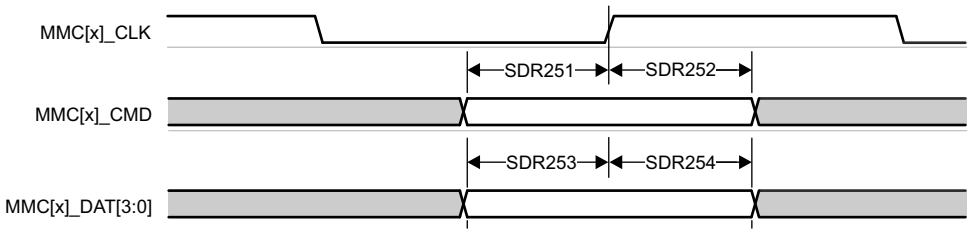

Figure 6-79. MMC0 – UHS-I SDR25 – Receive Mode

Table 6-95. Switching Characteristics for MMC0 – UHS-I SDR25 Mode

see Figure 6-80

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
SDR255	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
SDR256	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
SDR257	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
SDR258	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	2.4	8.1	ns
SDR259	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[3:0] transition	2.4	8.1	ns

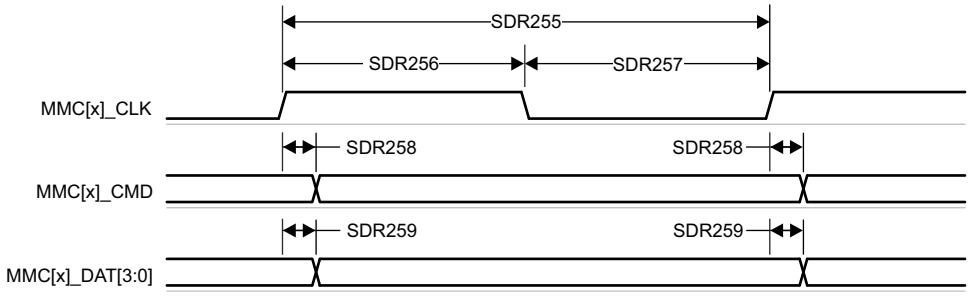

Figure 6-80. MMC0 – UHS-I SDR25 – Transmit Mode

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6.9.5.18.1.8 UHS–I SDR50 Mode

Table 6-96 and Figure 6-81 presents switching characteristics for MMC0 – UHS-I SDR50 Mode.

Table 6-96. Switching Characteristics for MMC0 – UHS-I SDR50 Mode

see Figure 6-81

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		100	MHz
SDR505	$t_{c(clk)}$	Cycle time, MMC0_CLK	10		ns
SDR506	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	4.45		ns
SDR507	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	4.45		ns
SDR508	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.2	6.35	ns
SDR509	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[3:0] transition	1.2	6.35	ns

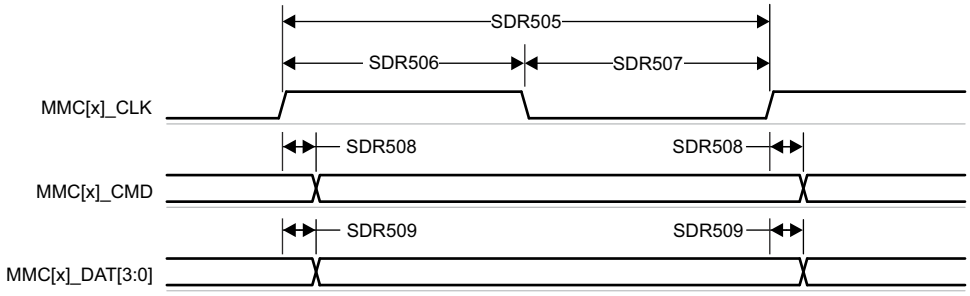

Figure 6-81. MMC0 – UHS-I SDR50 – Transmit Mode

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6.9.5.18.1.9 UHS–I DDR50 Mode

Table 6-97 and Figure 6-82 present switching characteristics for MMC0 – UHS-I DDR50 Mode.

Table 6-97. Switching Characteristics for MMC0 – UHS-I DDR50 Mode

see Figure 6-82

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
DDR505	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
DDR506	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
DDR507	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
DDR508	$t_{d(clk-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.12	6.43	ns
DDR509	$t_{d(clk-dV)}$	Delay time, MMC0_CLK transition to MMC0_DAT[3:0] transition	1.12	6.43	ns

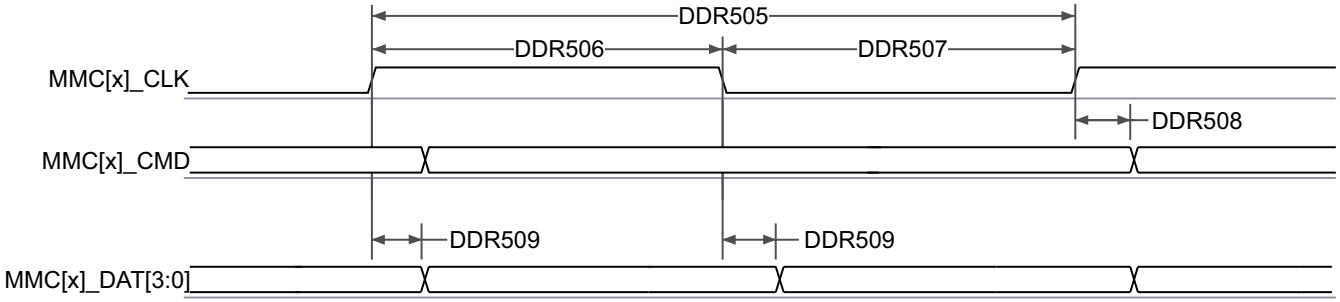

Figure 6-82. MMC0 – UHS-I DDR50 – Transmit Mode

6.9.5.18.1.10 UHS–I SDR104 Mode

Table 6-98 and Figure 6-83 present switching characteristics for MMC0 – UHS-I SDR104 Mode.

Table 6-98. Switching Characteristics for MMC0 – UHS-I SDR104 Mode

see Figure 6-83

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		200	MHz
SDR1045	$t_{c(clk)}$	Cycle time, MMC0_CLK	5		ns
SDR1046	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	2.12		ns
SDR1047	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	2.12		ns
SDR1048	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.07	3.21	ns
SDR1049	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[3:0] transition	1.07	3.21	ns

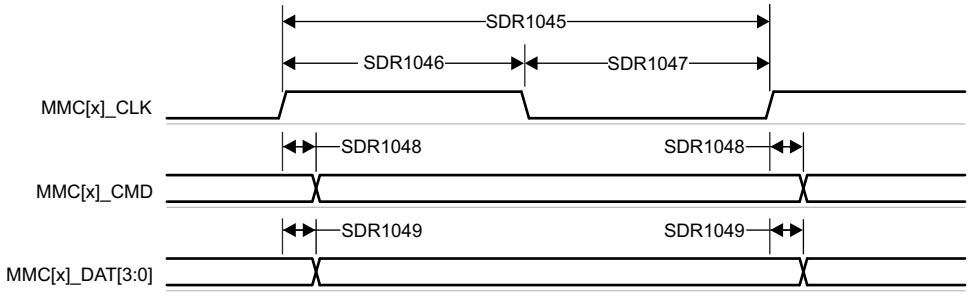

Figure 6-83. MMC0 – UHS-I SDR104 – Transmit Mode

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6.9.5.18.2 MMC1/MMC2 - SD/SDIO Interface

MMC1/MMC2 interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and it supports the following SD Card applications:

- Default speed
- High speed
- UHS–I SDR12
- UHS–I SDR25
- UHS–I SDR50
- UHS–I DDR50
- UHS–I SDR104

Table 6-99 presents the required DLL software configuration settings for MMC1/2 timing modes.

Table 6-99. MMC1/MMC2 DLL Delay Mapping for all Timing Modes

REGISTER NAME		MMCSD1_SS_PHY_CTRL_4_REG/ MMCSD2_SS_PHY_CTRL_4_REG				MMCSD1_SS_PHY_CTRL_5_REG/ MMCSD2_SS_PHY_CTRL_5_REG
BIT FIELD		[20]	[15:12]	[8]	[4:0]	[2:0]
BIT FIELD NAME		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL
MODE	DESCRIPTION	DELAY ENABLE	DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DELAY BUFFER DURATION
Default Speed	4-bit PHY operating 3.3V, 25MHz	0x1	0x0	0x1	0x0	0x7
High Speed	4-bit PHY operating 3.3V, 50MHz	0x1	0x0	0x1	0x0	0x7
UHS-I SDR12	4-bit PHY operating 1.8V, 25MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR25	4-bit PHY operating 1.8V, 50MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR50	4-bit PHY operating 1.8V, 100MHz	0x1	0xC	0x1	Tuning(1)	0x7
UHS-I DDR50	4-bit PHY operating 1.8V, 50MHz	0x1	0x9	0x1	Tuning(1)	0x7
UHS-I SDR104	4-bit PHY operating 1.8V, 200MHz	0x1	0x6	0x1	Tuning(1)	0x7

(1) Tuning means this mode requires a tuning algorithm to be used for optimal input timing

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Table 6-100 presents timing conditions for MMC1.

Table 6-100. MMC1/MMC2 Timing Conditions

PARAMETER			MIN	MAX	UNIT
Input Conditions					
SR_I	Input slew rate	Default Speed High Speed	0.69	2.06	V/ns
		UHS–I SDR12 UHS–I SDR25	0.34	1.34	V/ns
		UHS–I DDR50	1	2	V/ns
Output Conditions					
C_L	Output load capacitance	All modes	1	10	pF
PCB Connectivity Requirements					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	UHS–I DDR50	239	1134	ps
		All other modes	126	1386	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	High Speed UHS–I SDR104		8	ps
		UHS–I DDR50		20	ps
		All other modes		100	ps

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6.9.5.18.2.1 Default Speed Mode

Table 6-101, Figure 6-84, Table 6-102, and Figure 6-85 present timing requirements and switching characteristics for MMC1/MMC2 – Default Speed Mode.

Table 6-101. Timing Requirements for MMC1/MMC2 – Default Speed Mode

see Figure 6-84

NO.			MIN	MAX	UNIT
DS1	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	2.15		ns
DS2	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	1.67		ns
DS3	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	2.15		ns
DS4	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	1.67		ns

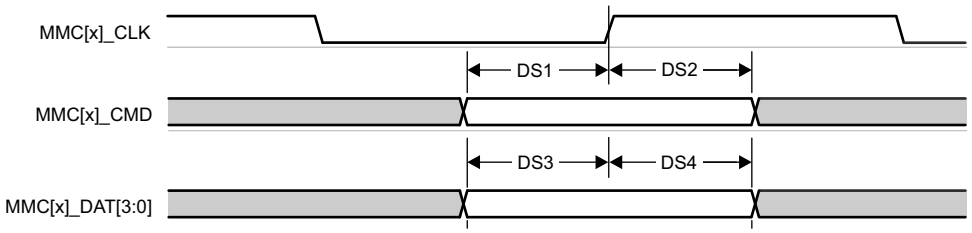

Figure 6-84. MMC1/MMC2 – Default Speed – Receive Mode

Table 6-102. Switching Characteristics for MMC1/MMC2 – Default Speed Mode

see Figure 6-85

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		25	MHz
DS5	$t_{c(clk)}$	Cycle time, MMCx_CLK	40		ns
DS6	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	18.7		ns
DS7	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	18.7		ns
DS8	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK falling edge to MMCx_CMD transition	- 1.8	2.2	ns
DS9	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK falling edge to MMCx_DAT[3:0] transition	- 1.8	2.2	ns

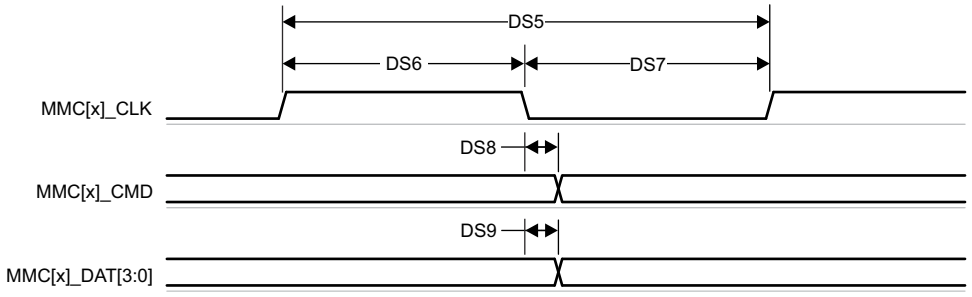

Figure 6-85. MMC1/MMC2 – Default Speed – Transmit Mode

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6.9.5.18.2.2 High Speed Mode

Table 6-103, Figure 6-86, Table 6-104, and Figure 6-87 present timing requirements and switching characteristics for MMC1/MMC2 – High Speed Mode.

Table 6-103. Timing Requirements for MMC1/MMC2 – High Speed Mode

see Figure 6-86

NO.			MIN	MAX	UNIT
HS1	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	2.24		ns
HS2	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	1.66		ns
HS3	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	2.24		ns
HS4	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	1.66		ns

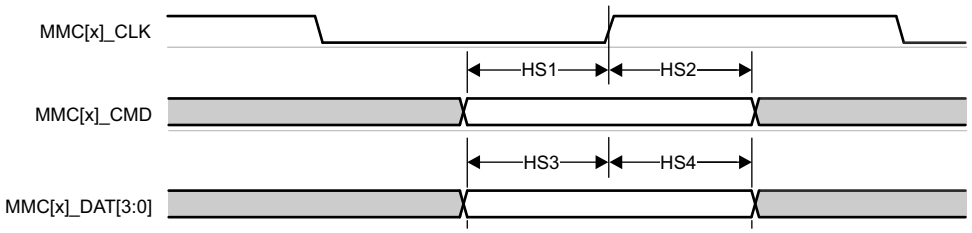

Figure 6-86. MMC1/MMC2 – High Speed – Receive Mode

Table 6-104. Switching Characteristics for MMC1/MMC2 – High Speed Mode

see Figure 6-87

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		50	MHz
HS5	$t_{c(clk)}$	Cycle time. MMCx_CLK	20		ns
HS6	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	9.2		ns
HS7	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	9.2		ns
HS8	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK falling edge to MMCx_CMD transition	- 1.8	2.2	ns
HS9	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK falling edge to MMCx_DAT[3:0] transition	- 1.8	2.2	ns

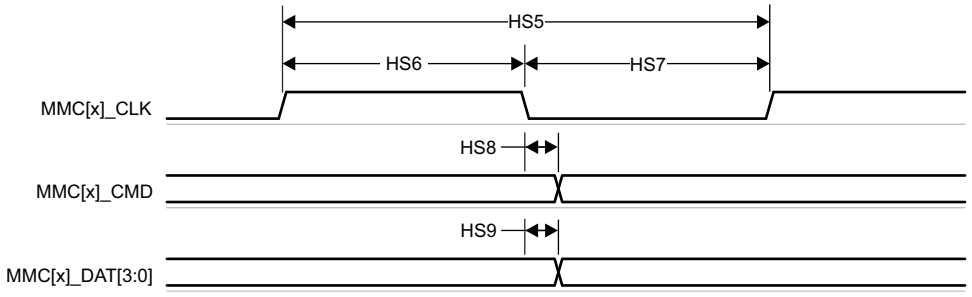

Figure 6-87. MMC1/MMC2 – High Speed – Transmit Mode

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6.9.5.18.2.3 UHS–I SDR12 Mode

Table 6-105, Figure 6-88, Table 6-106, and Figure 6-89 present timing requirements and switching characteristics for MMC1/MMC2 – UHS-I SDR12 Mode.

Table 6-105. Timing Requirements for MMC1/MMC2 – UHS-I SDR12 Mode

see Figure 6-88

NO.			MIN	MAX	UNIT
SDR121	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	4.2		ns
SDR122	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	0.87		ns
SDR123	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	4.2		ns
SDR124	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	0.87		ns

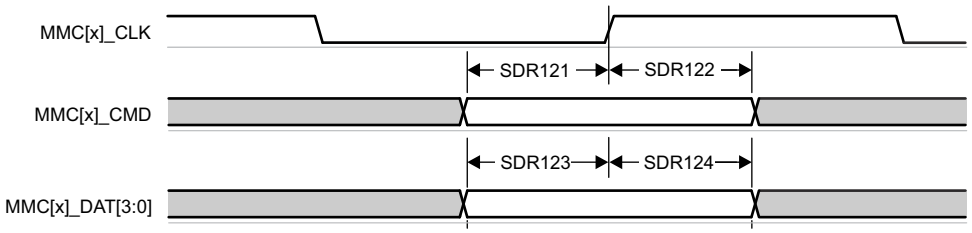

Figure 6-88. MMC1/MMC2 – UHS-I SDR12 – Receive Mode

Table 6-106. Switching Characteristics for MMC1/MMC2 – UHS-I SDR12 Mode

see Figure 6-89

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		25	MHz
SDR125	$t_{c(clk)}$	Cycle time, MMCx_CLK	40		ns
SDR126	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	18.7		ns
SDR127	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	18.7		ns
SDR128	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.5	8.6	ns
SDR129	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	1.5	8.6	ns

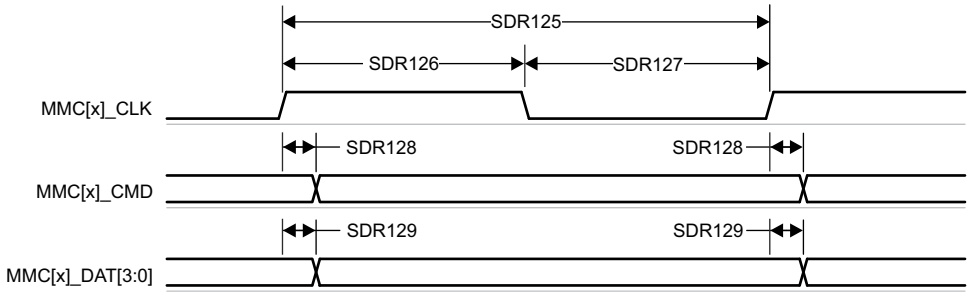

Figure 6-89. MMC1/MMC2 – UHS-I SDR12 – Transmit Mode

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6.9.5.18.2.4 UHS–I SDR25 Mode

Table 6-107, Figure 6-90, Table 6-108, and Figure 6-91 present timing requirements and switching characteristics for MMC1/MMC2 – UHS-I SDR25 Mode.

Table 6-107. Timing Requirements for MMC1/MMC2 – UHS-I SDR25 Mode

see Figure 6-90

NO.			MIN	MAX	UNIT
SDR251	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	2.15		ns
SDR252	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	1.27		ns
SDR253	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	2.15		ns
SDR254	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	1.27		ns

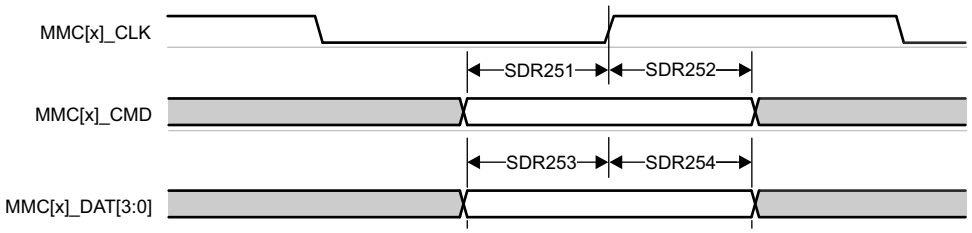

Figure 6-90. MMC1/MMC2 – UHS-I SDR25 – Receive Mode

Table 6-108. Switching Characteristics for MMC1/MMC2 – UHS-I SDR25 Mode

see Figure 6-91

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		50	MHz
SDR255	$t_{c(clk)}$	Cycle time, MMCx_CLK	20		ns
SDR256	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	9.2		ns
SDR257	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	9.2		ns
SDR258	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	2.4	8.1	ns
SDR259	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	2.4	8.1	ns

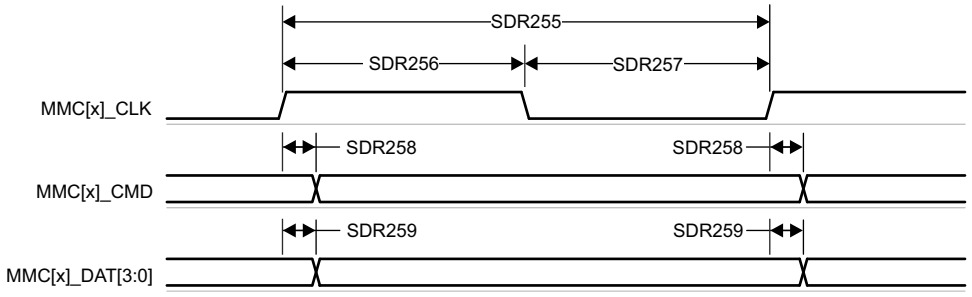

Figure 6-91. MMC1/MMC2 – UHS-I SDR25 – Transmit Mode

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6.9.5.18.2.5 UHS–I SDR50 Mode

Table 6-109 and Figure 6-92 presents switching characteristics for MMC1/MMC2 – UHS-I SDR50 Mode.

Table 6-109. Switching Characteristics for MMC1/MMC2 – UHS-I SDR50 Mode

see Figure 6-92

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		100	MHz
SDR505	$t_{c(clk)}$	Cycle time, MMCx_CLK	10		ns
SDR506	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	4.45		ns
SDR507	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	4.45		ns
SDR508	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.2	6.35	ns
SDR509	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	1.2	6.35	ns

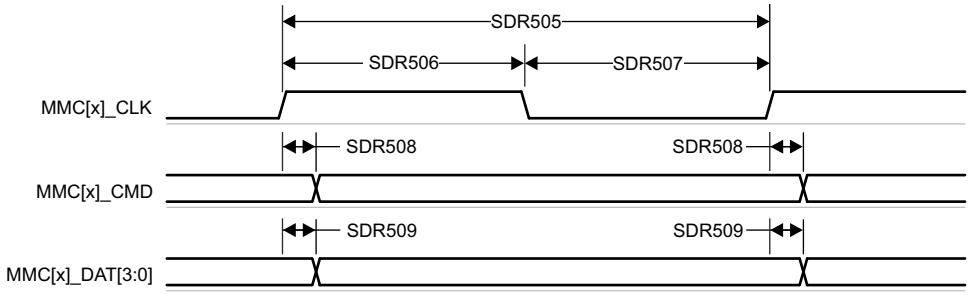

Figure 6-92. MMC1/MMC2 – UHS-I SDR50 – Transmit Mode

6.9.5.18.2.6 UHS–I DDR50 Mode

Table 6-110 and Figure 6-93 present switching characteristics for MMC1/MMC2 – UHS-I DDR50 Mode.

Table 6-110. Switching Characteristics for MMC1/MMC2 – UHS-I DDR50 Mode

see Figure 6-93

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		50	MHz
DDR505	$t_{c(clk)}$	Cycle time, MMCx_CLK	20		ns
DDR506	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	9.2		ns
DDR507	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	9.2		ns
DDR508	$t_{d(clk-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.12	6.43	ns
DDR509	$t_{d(clk-dV)}$	Delay time, MMCx_CLK transition to MMCx_DAT[3:0] transition	1.12	6.43	ns

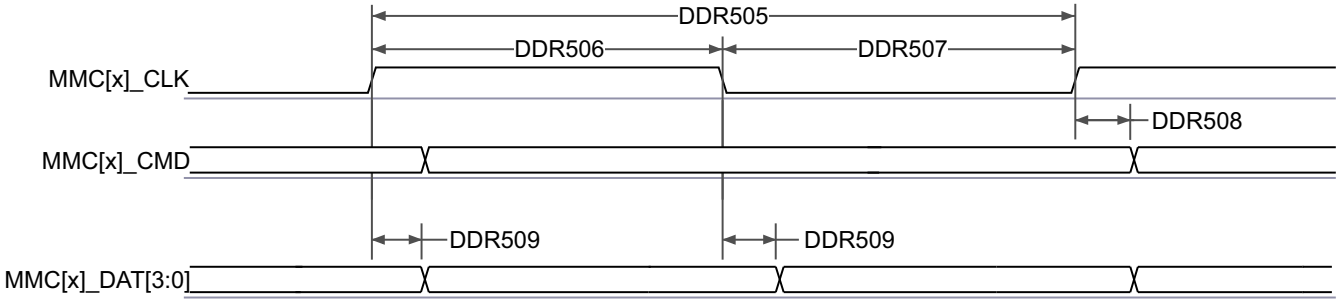

Figure 6-93. MMC1/MMC2 – UHS-I DDR50 – Transmit Mode

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6.9.5.18.2.7 UHS–I SDR104 Mode

Table 6-111 and Figure 6-94 present switching characteristics for MMC1/MMC2 – UHS-I SDR104 Mode.

Table 6-111. Switching Characteristics for MMC1/MMC2 – UHS-I SDR104 Mode

see Figure 6-94

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		200	MHz
SDR1045	$t_{c(clk)}$	Cycle time, MMCx_CLK	5		ns
SDR1046	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	2.12		ns
SDR1047	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	2.12		ns
SDR1048	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.07	3.21	ns
SDR1049	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	1.07	3.21	ns

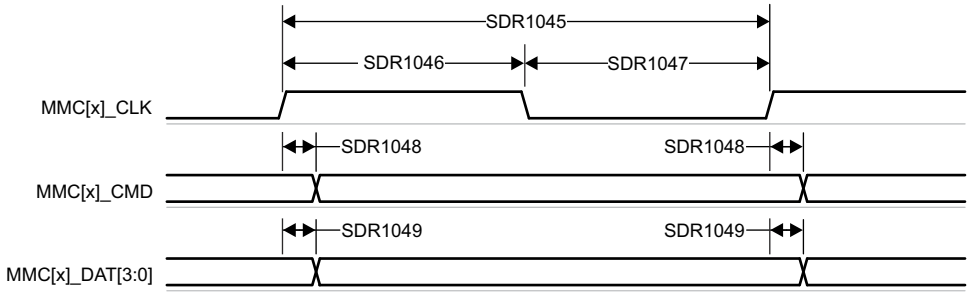

Figure 6-94. MMC1/MMC2 – UHS-I SDR104 – Transmit Mode

6.9.5.19 OSPI

OSPI0 offers two data capture modes, PHY mode and Tap mode.

PHY mode uses an internal reference clock to transmit and receive data via a DLL based PHY, where each reference clock cycle produces a single cycle of OSPI0_CLK for Single Data Rate (SDR) transfers or a half cycle of OSPI0_CLK for Double Data Rate (DDR) transfers. PHY mode supports four clocking topologies for the receive data capture clock. Internal PHY Loopback - uses the internal reference clock as the PHY receive data capture clock. Internal Pad Loopback - uses OSPI0_LBCLKO looped back into the PHY from the OSPI0_LBCLKO pin as the PHY receive data capture clock. External Board Loopback - uses OSPI0_LBCLKO looped back into the PHY from the OSPI0_DQS pin as the PHY receive data capture clock. DQS - uses the DQS output from the attached device as the PHY receive data capture clock. SDR transfers are not supported when using the Internal Pad Loopback and DQS clocking topologies. DDR transfers are not supported when using the Internal PHY Loopback or Internal Pad Loopback clocking topologies.

Tap mode uses an internal reference clock with selectable taps to adjusted data transmit and receive capture delays relative to OSPI0_CLK, which is a divide by 4 of the internal reference clock for SDR transfers or a divide by 8 of the internal reference clock for DDR transfers. Tap mode only supports one clocking topology for the receive data capture clock. No Loopback - uses the internal reference clock as the Tap receive data capture clock. This clocking topology supports a maximum internal reference clock rate of 200MHz, which produces an OSPI0_CLK rate up to 50MHz for SDR mode or 25MHz for DDR mode.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Section 6.9.5.19.1 defines timing requirements and switching characteristics associated with PHY mode and Section 6.9.5.19.2 defines timing requirements and switching characteristics associated with Tap mode.

Table 6-112 presents timing conditions for OSPI0.

Table 6-112. OSPI0 Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		1	6	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	10	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of OSPI0_CLK trace	No Loopback Internal PHY Loopback Internal Pad Loopback		450	ps
	Propagation delay of OSPI0_LBCLKO trace	External Board Loopback	2L(1) - 30	2L(1) + 30	ps
	Propagation delay of OSPI0_DQS trace	DQS	L(1) - 30	L(1) + 30	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch of OSPI0_D[7:0] and OSPI0_CSn[3:0] relative to OSPI0_CLK	All modes		60	ps

(1) L = Propagation delay of OSPI0_CLK trace

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6.9.5.19.1 OSPI0 PHY Mode

6.9.5.19.1.1 OSPI0 With PHY Data Training

Read and write data valid windows will shift due to variation in process, voltage, temperature, and operating frequency. A data training method may be implemented to dynamically configure optimal read and write timing. Implementing data training enables proper operation across temperature with a specific process, voltage, and frequency operating condition, while achieving a higher operating frequency.

Data transmit and receive timing parameters are not defined for the data training use case since they are dynamically adjusted based on the operating condition.

Table 6-113 defines DLL delays required for OSPI0 with Data Training. Table 6-114, Figure 6-95, Figure 6-96, Table 6-115, Figure 6-97, and Figure 6-98 present timing requirements and switching characteristics for OSPI0 with Data Training.

Table 6-113. OSPI0 DLL Delay Mapping for PHY Data Training

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD	(1)
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	(2)

(1) Transmit DLL delay value determined by training software
(2) Receive DLL delay value determined by training software

Table 6-114. OSPI0 Timing Requirements – PHY Data Training

see Figure 6-95, and Figure 6-96

NO.			MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	DDR with DQS	(1)		ns
O16	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	DDR with DQS	(1)		ns
O21	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	SDR with External Board Loopback	(1)		ns
O22	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	SDR with External Board Loopback	(1)		ns
	t_{DVW}	Data valid window (O15 + O16)	1.8V, DDR with DQS	1.6		ns
			3.3V, DDR with DQS	2.2		ns
		Data valid window (O21 + O22)	1.8V, SDR with External Board Loopback	2.3		ns
			3.3V, SDR with External Board Loopback	2.9		ns

(1) Minimum setup and hold time requirements for OSPI0_D[7:0] inputs are not defined when Data Training is used to find the optimum data valid window. The t_{DVW} parameter defines the minimum data invalid window required. This parameter is provided in lieu of minimum setup and minimum hold times, where it must be used to check compatibility with the data valid window provided by an attached device.

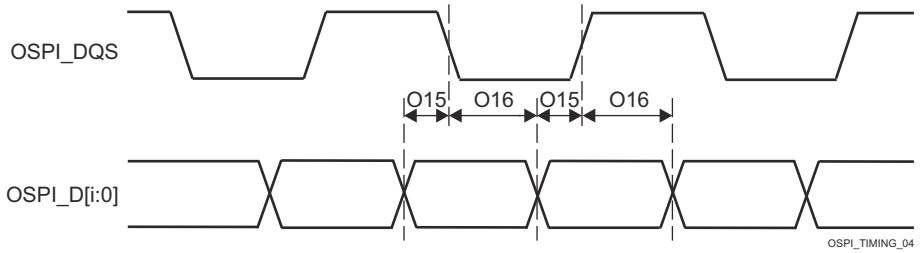

Figure 6-95. OSPI0 Timing Requirements – PHY Data Training, DDR with DQS

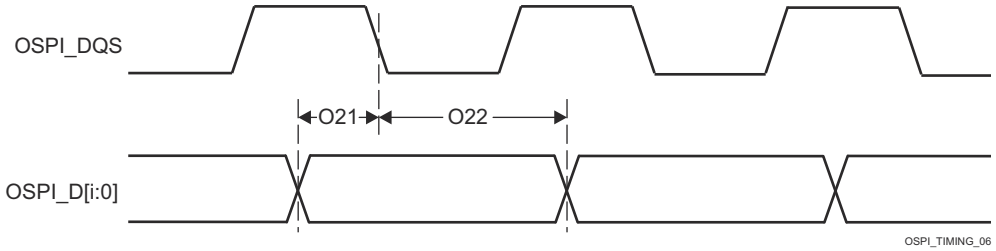

Figure 6-96. OSPI0 Timing Requirements – PHY Data Training, SDR with External Board Loopback

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Table 6-115. OSPI Switching Characteristics – PHY Data Training

See Figure 6-97 and Figure 6-98

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	1.8V, DDR	6.0	10	ns
			3.3V, DDR	7.5	10	ns
O7			1.8V, SDR	6.0	10	ns
			3.3V, SDR	7.5	10	ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low	DDR	((0.475P(1)) - 0.3)		ns
O8			SDR			
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high	DDR	((0.475P(1)) - 0.3)		ns
O9			SDR			
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge	DDR	((0.475P(1)) + (0.975M(2)R(4)) + (0.04TD(5)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + (0.11TD(5)) + 1)	ns
O10			SDR			
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge	DDR	((0.475P(1)) + (0.975N(3)R(4)) - (0.04TD(5)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) - (0.11TD(5)) + 1)	ns
O11			SDR			
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	DDR	(6)	(6)	ns
O12			SDR			
	t_{DIVW}	Data invalid window (O6 Max - Min)	DDR		1.6	ns
		Data invalid window (O12 Max - Min)	SDR			

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns
(5) TD = PHY_CONFIG_TX_DLL_DELAY_FLD
(6) Minimum and maximum delay times for OSPI0_D[7:0] outputs are not defined when Data Training is used to find the optimum data valid window. The t_{DIVW} parameter defines the maximum data invalid window. This parameter is provided in lieu of minimum and maximum delay times, where it must be used to check compatibility with the data valid window requirements of an attached device.

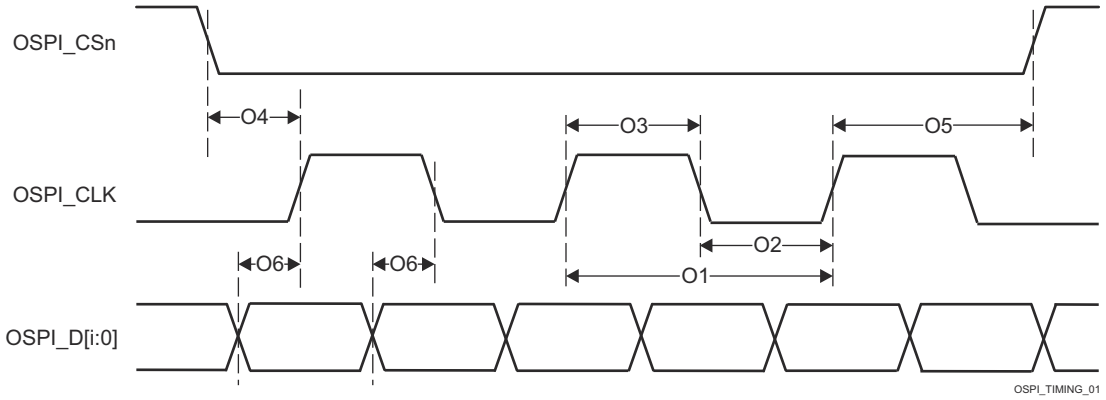

Figure 6-97. OSPI0 Switching Characteristics – PHY DDR Data Training

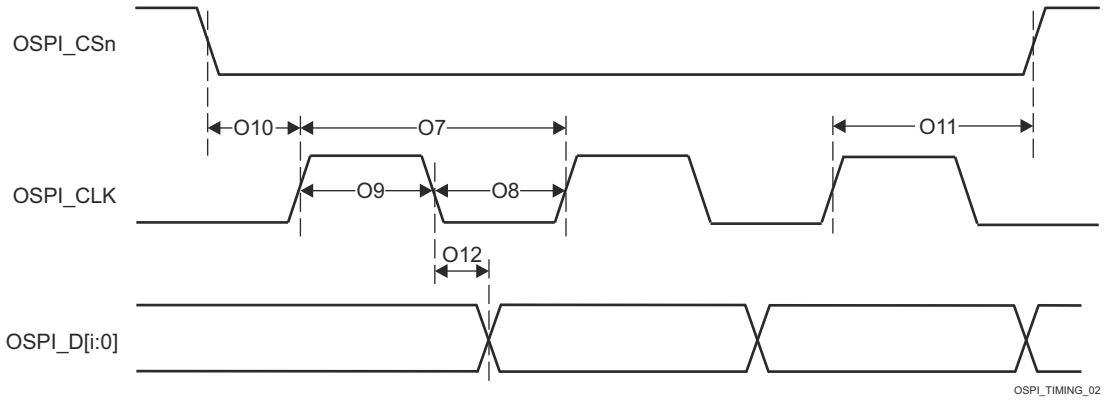

Figure 6-98. OSPI0 Switching Characteristics – PHY SDR Data Training

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6.9.5.19.1.2 OSPI0 Without Data Training

Note

Timing parameters defined in this section are only applicable when data training is not implemented and DLL delays are configured as described in Section 6.9.5.19.1.2.1 and Section 6.9.5.19.1.2.2.

6.9.5.19.1.2.1 OSPI0 PHY SDR Timing

Table 6-116 defines DLL delays required for OSPI0 PHY SDR Mode. Table 6-117, Figure 6-99, Figure 6-100, Table 6-118, and Figure 6-101 present timing requirements and switching characteristics for OSPI0 PHY SDR Mode.

Table 6-116. OSPI0 DLL Delay Mapping for PHY SDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD,	0x0
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

Table 6-117. OSPI0 Timing Requirements – PHY SDR Mode

see Figure 6-99 and Figure 6-100

NO.			MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	1.8V, SDR with Internal PHY Loopback	4.8		ns
			3.3V, SDR with Internal PHY Loopback	5.19		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	1.8V, SDR with Internal PHY Loopback	-0.5		ns
			3.3V, SDR with Internal PHY Loopback	-0.5		ns
O21	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	1.8V, SDR with External Board Loopback	0.6		ns
			3.3V, SDR with External Board Loopback	0.9		ns
O22	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	1.8V, SDR with External Board Loopback	1.7		ns
			3.3V, SDR with External Board Loopback	2.0		ns

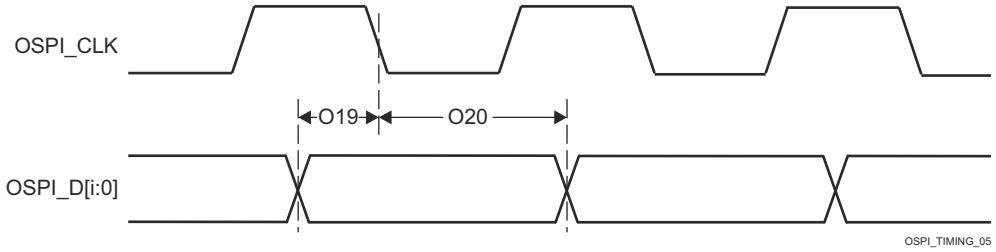

Figure 6-99. OSPI0 Timing Requirements – PHY SDR with Internal PHY Loopback

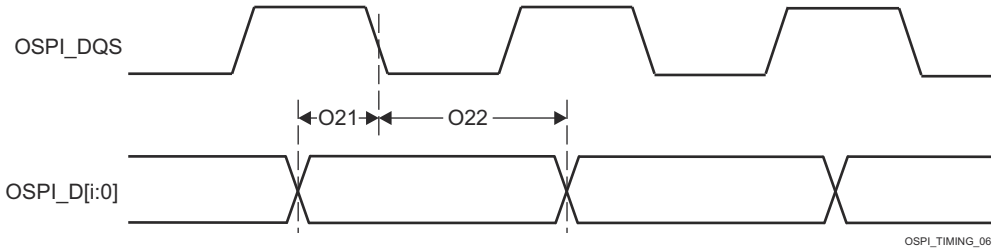

Figure 6-100. OSPI0 Timing Requirements – PHY SDR with External Board Loopback

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Table 6-118. OSPI0 Switching Characteristics – PHY SDR Mode

see Figure 6-101

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	1.8V	7		ns
			3.3V	6.03		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + (0.975M(2)R(4)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + 1)	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) + 1)	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	1.8V	-1.16	1.25	ns
			3.3V	-1.33	1.51	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

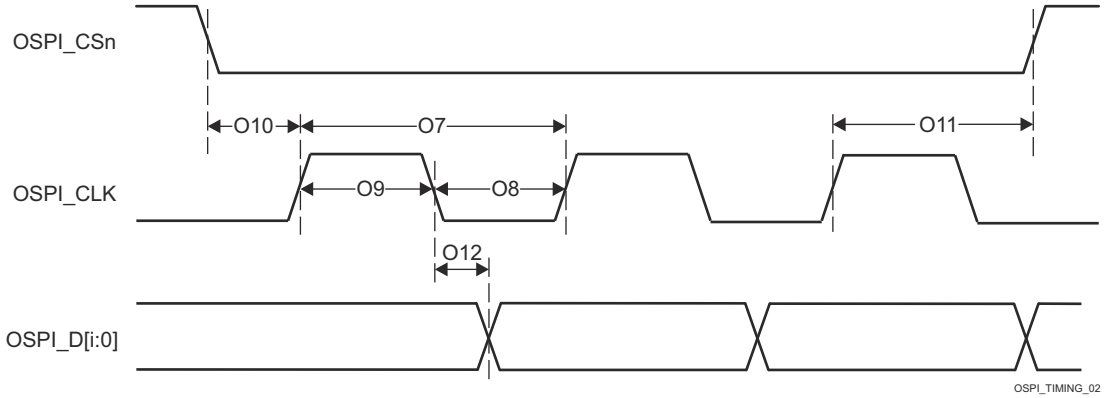

Figure 6-101. OSPI0 Switching Characteristics – PHY SDR

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6.9.5.19.1.2.2 OSPI0 PHY DDR Timing

Table 6-119 defines DLL delays required for OSPI0 PHY DDR Mode. Table 6-120, Figure 6-102, Table 6-121, and Figure 6-103 present timing requirements and switching characteristics for OSPI0 PHY DDR Mode.

Table 6-119. OSPI0 DLL Delay Mapping for PHY DDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
1.8V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x46
3.3V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x43
Receive		
1.8V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x15
3.3V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x3A
All other modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

Table 6-120. OSPI0 Timing Requirements – PHY DDR Mode

see Figure 6-102

NO.			MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	1.8V, DDR with External Board Loopback	0.53		ns
			1.8V, DDR with DQS	-0.46		ns
			3.3V, DDR with External Board Loopback	1.23		ns
			3.3V, DDR with DQS	-0.66		ns
O16	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	1.8V, DDR with External Board Loopback	1.24(1)		ns
			1.8V, DDR with DQS	3.59		ns
			3.3V, DDR with External Board Loopback	1.44(1)		ns
			3.3V, DDR with DQS	7.92		ns

(1) This Hold time requirement is larger than the Hold time provided by a typical OSPI/QSPI/SPI device. Therefore, the trace length between the SoC and attached OSPI/QSPI/SPI device must be sufficiently long enough to ensure that the Hold time is met at the SoC. The length of the SoC's external loopback clock (OSPI0_LBCLKO to OSPI0_DQS) may need to be shortened to compensate.

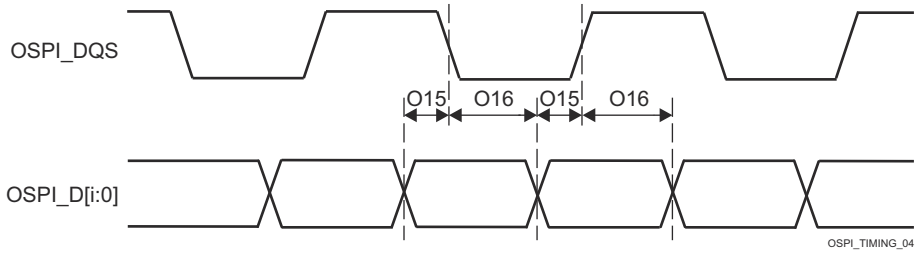

Figure 6-102. OSPI0 Timing Requirements – PHY DDR with External Board Loopback or DQS

Table 6-121. OSPI0 Switching Characteristics – PHY DDR Mode

see Figure 6-103

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		19		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) - (0.975M(2)R(4)))	((0.525P(1)) - (1.025M(2)R(4)) + 7)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 7)	((0.525P(1)) + (1.025N(3)R(4)))	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	1.8V	-7.71	-1.56	ns
			3.3V	-7.71	-1.56	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

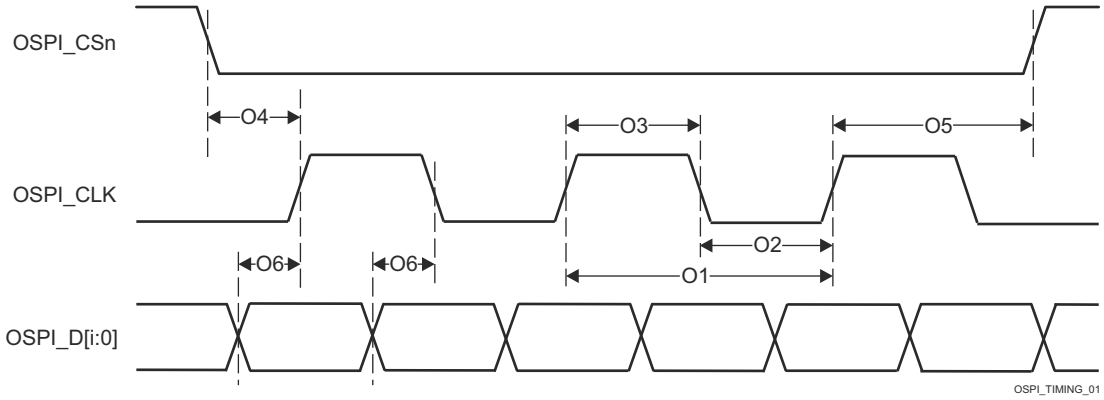

Figure 6-103. OSPI0 Switching Characteristics – PHY DDR

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6.9.5.19.2 OSPI0 Tap Mode

6.9.5.19.2.1 OSPI0 Tap SDR Timing

Table 6-122, Figure 6-104, Table 6-123, and Figure 6-105 present timing requirements and switching characteristics for OSPI0 Tap SDR Mode.

Table 6-122. OSPI0 Timing Requirements – Tap SDR Mode

see Figure 6-104

NO.			MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	(15.4 - (0.975T(1)R(2)))		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	(- 4.3 + (0.975T(1)R(2)))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = reference clock cycle time in ns

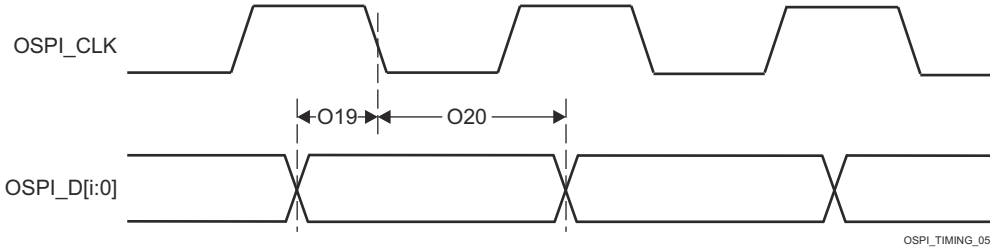

Figure 6-104. OSPI0 Timing Requirements – Tap SDR, No Loopback

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Table 6-123. OSPI0 Switching Characteristics – Tap SDR Mode

see Figure 6-105

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		20		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + (0.975M(2)R(4)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + 1)	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) + 1)	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		- 4.25	7.25	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

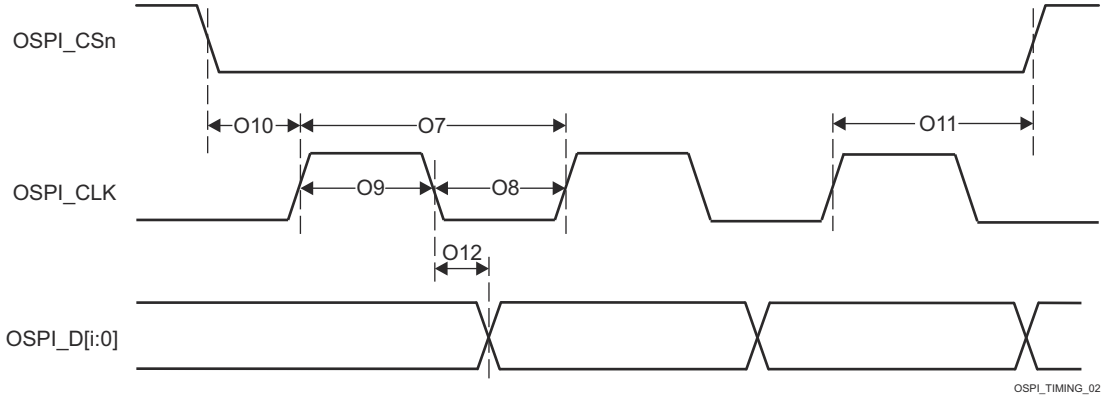

Figure 6-105. OSPI0 Switching Characteristics – Tap SDR, No Loopback

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6.9.5.19.2.2 OSPI0 Tap DDR Timing

Table 6-124, Figure 6-106, Table 6-125, and Figure 6-107 present timing requirements and switching characteristics for OSPI0 Tap DDR Mode.

Table 6-124. OSPI0 Timing Requirements – Tap DDR Mode

see Figure 6-106

NO.			MODE	MIN	MAX	UNIT
O13	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	(17.04 - (0.975T(1)R(2)))		ns
O14	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	(- 3.16 + (0.975T(1)R(2)))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = reference clock cycle time in ns

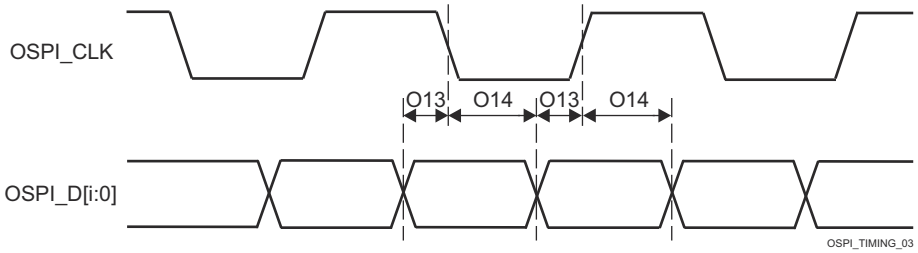

Figure 6-106. OSPI0 Timing Requirements – Tap DDR, No Loopback

Table 6-125. OSPI0 Switching Characteristics – Tap DDR Mode

see Figure 6-107

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		40		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + ((0.975M(2)R(5)) - 1)	((0.525P(1)) + (1.025M(2)R(5)) + 1)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(5)) - 1)	((0.525P(1)) + (1.025N(3)R(5)) + 1)	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		(- 5.04 + (0.975(T(4) + 1)R(5)) - (0.525P(1)))	(3.64 + (1.025(T(4) + 1)R(5)) - (0.475P(1)))	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) T = OSPI_RD_DATA_CAPTURE_REG[DDR_READ_DELAY_FLD]
(5) R = reference clock cycle time in ns

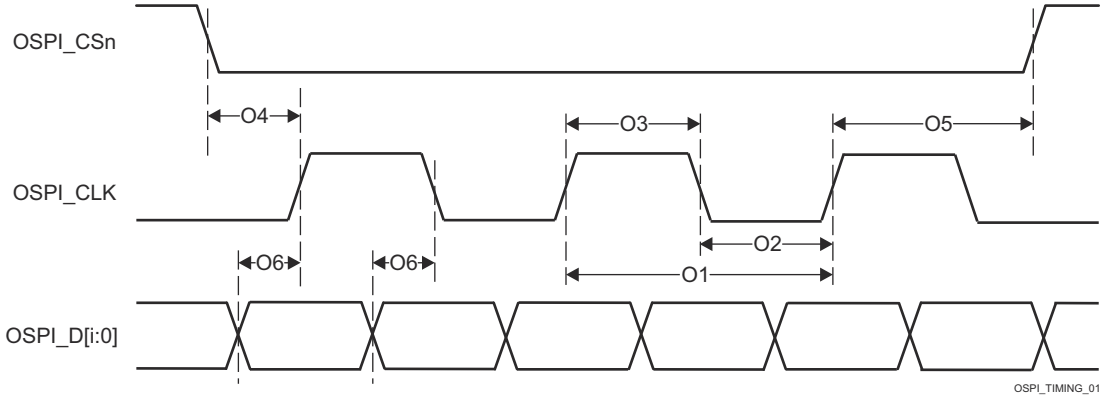

Figure 6-107. OSPI0 Switching Characteristics – Tap DDR, No Loopback

6.9.5.20 PCIe

The PCI-Express Subsystem is compliant with the PCIe® Base Specification, Revision 4.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Peripheral Component Interconnect Express (PCIe), see the *SERDES0 Signal Descriptions* and the corresponding subsection within *Detailed Description*.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter of the device TRM.

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6.9.5.21 Timers

For more details about features and additional description information on the device Timers, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 6-126. Timer Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	10	pF

Table 6-127. Timer Input Timing Requirements

see Figure 6-108

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T1	$t_{w(TINPH)}$	Pulse duration, high	CAPTURE	4P(1)+ 2.5		ns
T2	$t_{w(TINPL)}$	Pulse duration, low	CAPTURE	4P(1)+ 2.5		ns

(1) P = functional clock period in ns.

Table 6-128. Timer Output Switching Characteristics

see Figure 6-108

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T3	$t_{w(TOUTH)}$	Pulse duration, high	PWM	4P(1) - 2.5		ns
T4	$t_{w(TOUTL)}$	Pulse duration, low	PWM	4P(1) - 2.5		ns

(1) P = functional clock period in ns.

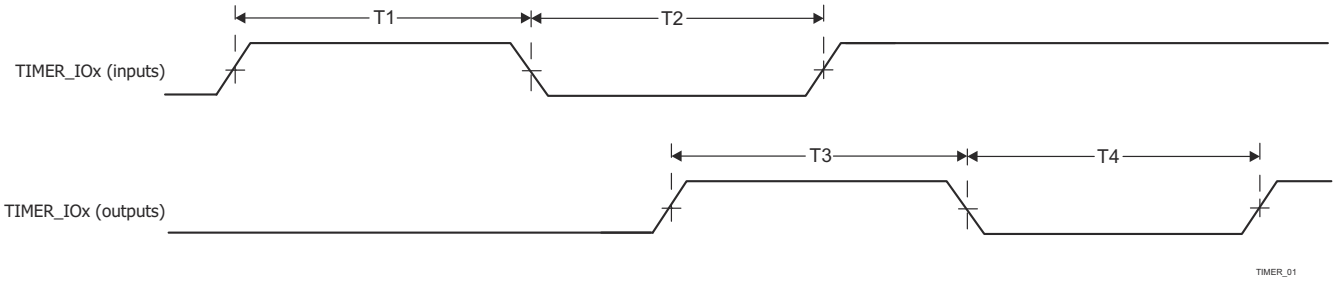

Figure 6-108. Timer Timing Requirements and Switching Characteristics

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

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6.9.5.22 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 6-129. UART Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	30(1)	pF

(1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

Table 6-130. UART Timing Requirements

see Figure 6-109

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{w(RXD)}$	Pulse width, receive data bit high or low	0.95U(1) (2)	1.05U(1) (2)	ns
2	$t_{w(RXDS)}$	Pulse width, receive start bit low	0.95U(1) (2)		ns

(1) U = UART baud time in ns = 1/programmed baud rate.
(2) This value defines the data valid time, where the input voltage is required to be above V_{IH} or below V_{IL}.

Table 6-131. UART Switching Characteristics

see Figure 6-109

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{(baud)}$	Programmable baud rate for Main Domain UARTs		12	Mbps
		Programmable baud rate for MCU and WKUP Domain UARTs		3.7	Mbps
3	$t_{w(TXD)}$	Pulse width, transmit data bit high or low	U(1) - 2	U(1) + 2	ns
4	$t_{w(TXDS)}$	Pulse width, transmit start bit low	U(1) - 2		ns

(1) U = UART baud time in ns = 1/actual baud rate, where the actual baud rate is defined in the UART Baud Rate Settings table of the device TRM.

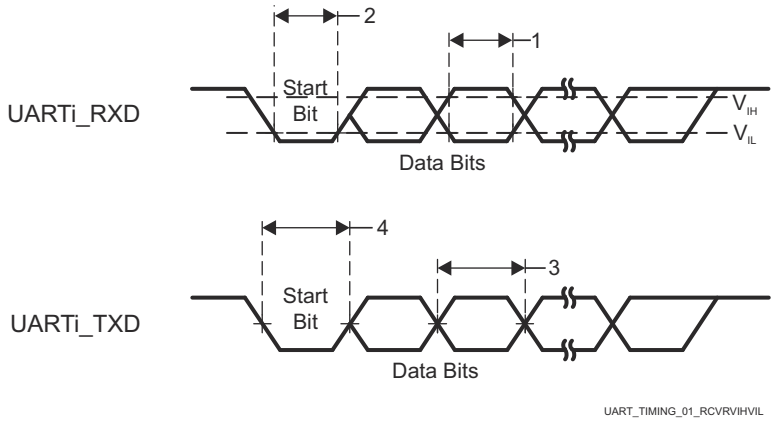

Figure 6-109. UART Timing Requirements and Switching Characteristics

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

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6.9.5.23 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

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7 Detailed Description

7.1 Overview

The TDA4VEN/TDA4AEN (aka, TDA4-Entry) processor family is an extension of the Jacinto™ 7 automotive-grade family of heterogeneous Arm® processors targeted at Advanced Driver Assistance System (ADAS) applications. With embedded Deep Learning (DL), Video, Vision Processing, and 3D Graphics acceleration, display interface and extensive automotive peripheral and networking options, TDA4VEN/TDA4AEN is built for a set of cost and power sensitive automotive applications such as NCAP front camera or entry-level park assistance systems. The cost optimized TDA4VEN/TDA4AEN provides an optimized performance compute for both traditional and deep learning algorithms at industry leading power/performance ratios with a high level of system integration to enable scalability and lower costs for advanced automotive platforms supporting multiple sensor modalities in stand-alone Electronic Control Units (ECUs).

Key features and benefits:

- Focus on innovation and fast development with Linux® and Android™ SDKs accompanied with real-time functional safety and security SDKs.
- Address next wave of HMI designs with new generation of 3D GPU and 4K video acceleration.
- Enhance your design connectivity with an extensive set of automotive and high-speed IOs, including: 4x CAN-FD, 3-port Gigabit Ethernet switch (two external ports) with TSN support, and two USB2.0 ports.
- Supports the latest cybersecurity requirements with the built-in Hardware Security Module (HSM).
- Provides intelligent features, such as: facial recognition and touchless HMI with Arm® Cortex®-A53 CPUs and open-source AI software and tools

The TDA4VEN/TDA4AEN processors comply with the AEC - Q100 automotive standard and support industrial-grade. ASIL-B and SIL-2 functional safety requirements can be addressed using an integrated Arm Cortex-R5F core and dedicated peripherals, which can all be isolated from the rest of the processor.

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8 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Device Connection and Layout Fundamentals

8.1.1 Power Supply

8.1.1.1 Power Distribution Network Implementation Guidance

The Sitara Processor Power Distribution Networks: Implementation and Analysis provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI *only* supports designs that follow the board design guidelines contained in the application report.

8.1.2 External Oscillator

For more information about External Oscillators, see the *Clock Specifications* section.

8.1.3 JTAG, EMU, and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For recommendations on JTAG, EMU, and TRACE routing, see the Emulation and Trace Headers Technical Reference Manual

8.1.4 Unused Pins

For more information about Unused Pins, see *Pin Connectivity Requirements* .

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8.2 Peripheral- and Interface-Specific Design Information

8.2.1 LPDDR4 Board Design and Layout Guidelines

The goal of the Jacinto 7 DDR Board Design and Layout Guidelines is to make the LPDDR4 system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using LPDDR4 memories that follow the guidelines in this document.

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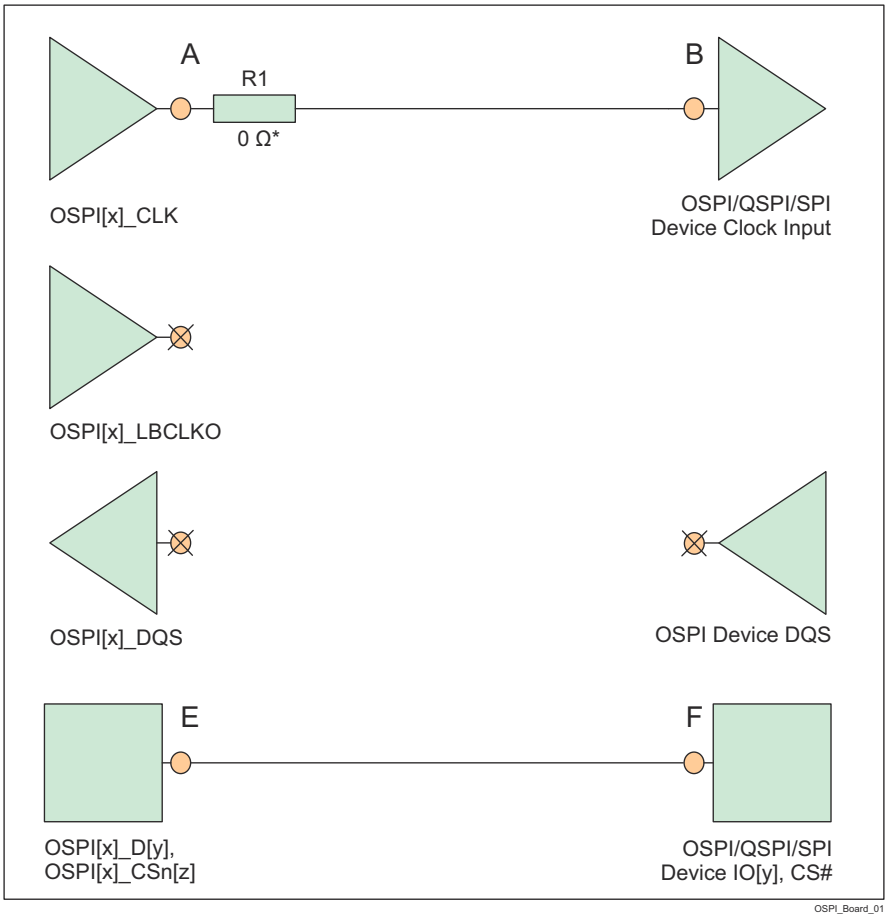
8.2.2 OSPI/QSPI/SPI Board Design and Layout Guidelines

The following section details the PCB routing guidelines that must be observed when connecting OSPI, QSPI, or SPI devices.

8.2.2.1 No Loopback, Internal PHY Loopback, and Internal Pad Loopback

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B) must be ≤ 450ps (~7cm as stripline or ~8cm as microstrip)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50Ω PCB routing is recommended along with series terminations, as shown in Figure 8-1
- Propagation delays and matching:
  - (A to B) ≤ 450ps
  - (E to F, or F to E) = ((A to B) ± 60ps)



* 0Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is placeholder for fine tuning, if needed.

Figure 8-1. OSPI Connectivity Schematic for No Loopback, Internal PHY Loopback, and Internal Pad Loopback

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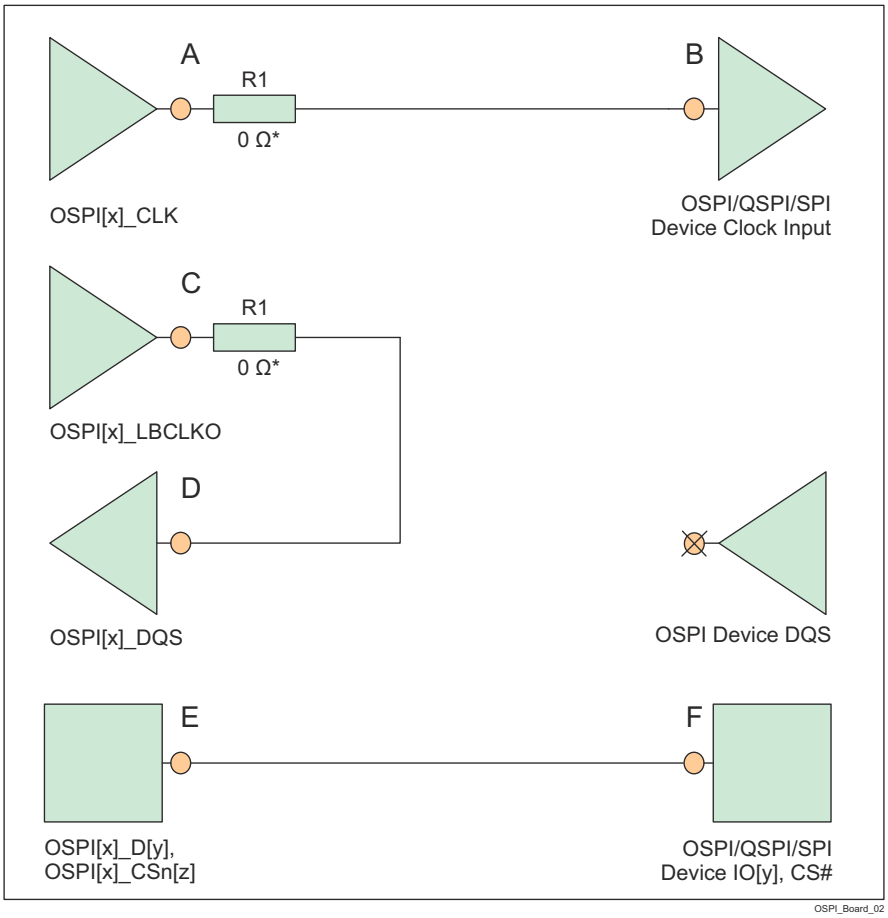
8.2.2.2 External Board Loopback

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The OSPI[x]_LBCLKO output pin must be looped back to the OSPI[x]_DQS input pin
- The signal propagation delay of the OSPI[x]_LBCLKO pin to the OSPI[x]_DQS pin (C to D) must be approximately twice the propagation delay of the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50Ω PCB routing is recommended along with series terminations, as shown in Figure 8-2
- Propagation delays and matching:
  - (C to D) = 2 x ((A to B) ± 30ps), see the exception note below.
  - (E to F, or F to E) = ((A to B) ± 60ps)

Note

The External Board Loopback hold time requirement (defined by parameter number O16 in the *OSPI0 Timing Requirements - PHY DDR Mode* section) may be larger than the hold time provided by a typical OSPI/QSPI/SPI device. In this case, the propagation delay of OPSI[x]_LBCLKO pin to the OSPI[x]_DQS pin (C to D) can be reduced to provide additional hold time.



* 0Ω resistor (R1), located as close as possible to the OSPI[x]_CLK and OSPI[x]_LBCLKO pins, is a placeholder for fine tuning, if needed.

Figure 8-2. OSPI Connectivity Schematic for External Board Loopback

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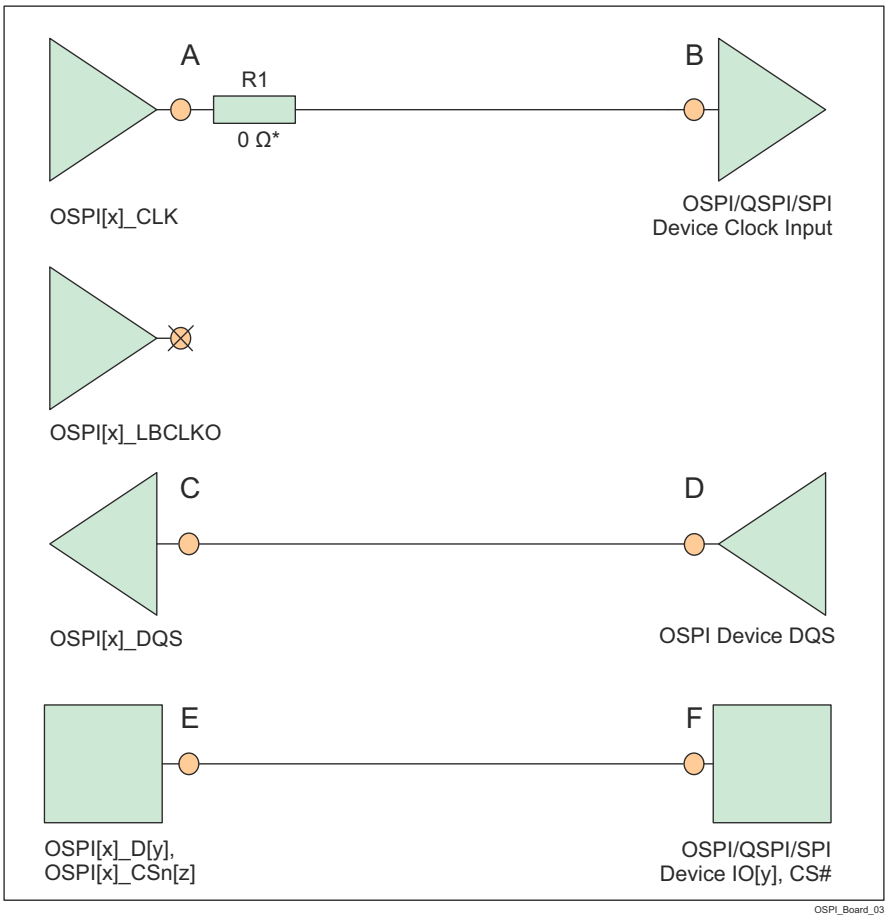
8.2.2.3 DQS (only available in Octal SPI devices)

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The DQS pin of the attached OSPI/QSPI/SPI device must be connected to OSPI[x]_DQS pin
- The signal propagation delay from the attached OSPI/QSPI/SPI device DQS pin to the OSPI[x]_DQS pin (D to C) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50Ω PCB routing is recommended along with series terminations, as shown in Figure 8-3
- Propagation delays and matching:
  - (D to C) = ((A to B) ± 30ps)
  - (E to F, or F to E) = ((A to B) ± 60ps)



* 0Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is a placeholder for fine tuning, if needed.

Figure 8-3. OSPI Connectivity Schematic for DQS

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8.2.3 USB VBUS Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5V for normal operation, and as high as 20V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the Figure 8-4), which limits the voltage applied to the actual device pin (USB0_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of Zener diode at 5V should be less than 100nA.

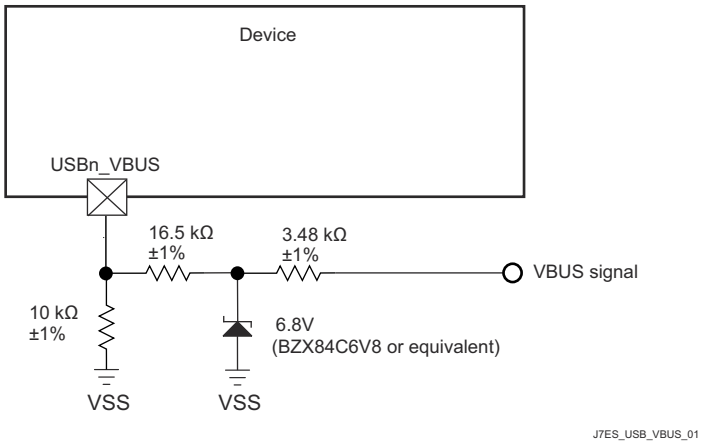

Figure 8-4. USB VBUS Detect Voltage Divider / Clamp Circuit

The USB0_VBUS pin can be considered to be fail-safe because the external circuit in Figure 8-4 limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

8.2.4 System Power Supply Monitor Design Guidelines

The VMON_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system and can be connected to the VMON_VSYS pin via and external resistor divider circuit. This system supply is monitored by comparing the external voltage divider output voltage to an internal voltage reference, where a power fail event is triggered when the voltage applied to VMON_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit.

When designing the resistor divider circuit the designer must understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON_VSYS input threshold which has a nominal value of 0.45V, with a variation of ±3%. Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON_VSYS input leakage current can be in the range of 10nA to 2.5µA when applying 0.45V.

Note

The resistor voltage divider shall be designed such that the output voltage never exceeds the maximum value defined in the *Recommended Operating Conditions* section, during normal operating conditions.

Figure 8-5 presents an example, where the system power supply is nominally 5V and the maximum trigger threshold is 5V - 10%, or 4.5V.

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For this example, the designer must understand which variables effect the maximum trigger threshold when selecting resistor values. A device which has a VMON_VSYS input threshold of 0.45V + 3% needs to be considered when trying to design a voltage divider that doesn't trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but the contribution to the maximum trigger point is not obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON_VSYS pin is 2.5µA. When implementing a resistor divider where R1 = 4.81KΩ and R2 = 40.2KΩ, the result is a maximum trigger threshold of 4.517V.

Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of 0.45V - 3% when the value of R1 is 1% high and the value of R2 is 1% low, and the input leakage current is 10nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.013V.

This example demonstrates a system power supply voltage trip point that ranges from 4.013V to 4.517V. Approximately 250mV of this range is introduced by VMON_VSYS input threshold accuracy of ±3%, approximately 150 mV of this range is introduced by resistor tolerance of ±1%, and approximately 100mV of this range is introduced by loading error when VMON_VSYS input leakage current is 2.5µA.

The resistor values selected in this example produces approximately 100µA of bias current through the resistor divider when the system supply is 4.5V. The 100mV of loading error mentioned above can be reduced to about 10mV by increasing the bias current through the resistor divider to approximately 1mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer must also consider implementing a noise filter on the voltage divider output since VMON_VSYS has minimum hysteresis and a high-bandwidth response to transients. This can be done by installing a capacitor across R1 as shown in Figure 8-5. However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.

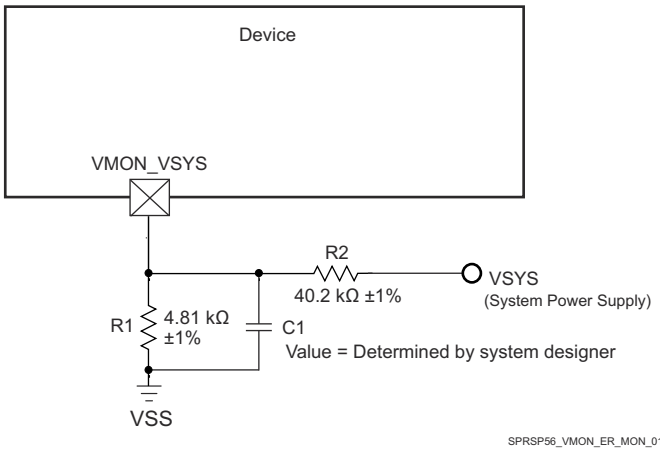

Figure 8-5. System Supply Monitor Voltage Divider Circuit

VMON_1P8_SOC pin provides a way to monitor external 1.8V power supplies. This pin must be connected directly to their respective power source. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

VMON_3P3_SOC pin provides a way to monitor external 3.3V power supplies. This pin must be connected directly to their respective power source. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

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8.2.5 High Speed Differential Signal Routing Guidance

The High Speed Interface Layout Guidelines provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application note.

8.2.6 Thermal Solution Guidance

The Thermal Design Guide for DSP and ARM Application Processors provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application note.

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8.3 Clock Routing Guidelines

8.3.1 Oscillator Routing

When designing the printed-circuit board:

- Place all crystal circuit components as close as possible to the respective device pins.
- Route the crystal circuit traces on the outer layer of the PCB and minimize trace lengths to reduce parasitic capacitance and minimize crosstalk from other signals.
- Place a continuous ground plane on the adjacent layer of the PCB such that it is under all crystal circuit components and crystal circuit traces.
- Route a ground guard around the crystal circuit components to shield it from any adjacent signals routed on the same layer as the crystal circuit traces. Insert multiple vias to stitch down the ground guard such that it does not have any unterminated stubs.
- Route a ground guard between the MCU_OSC0_XI and MCU_OSC0_XO signals to shield the MCU_OSC0_XI signal from the MCU_OSC0_X0 signal. Insert multiple vias to stitch down the ground guard such that it does not have any unterminated stubs.
- Connect all crystal circuit ground connections and ground guard connections directly to the adjacent layer ground plane, and the device VSS ground plane if they are implemented separately on different layers of the PCB.

Note

Implementing a ground guard between the MCU_OSC0_XI and MCU_OSC0_XO signals is critical to minimize shunt capacitance between the two signals. Routing these two signals adjacent to each other without a ground guard between them will effectively reduce the gain of the oscillator amplifier, which reduces its ability to start oscillation.

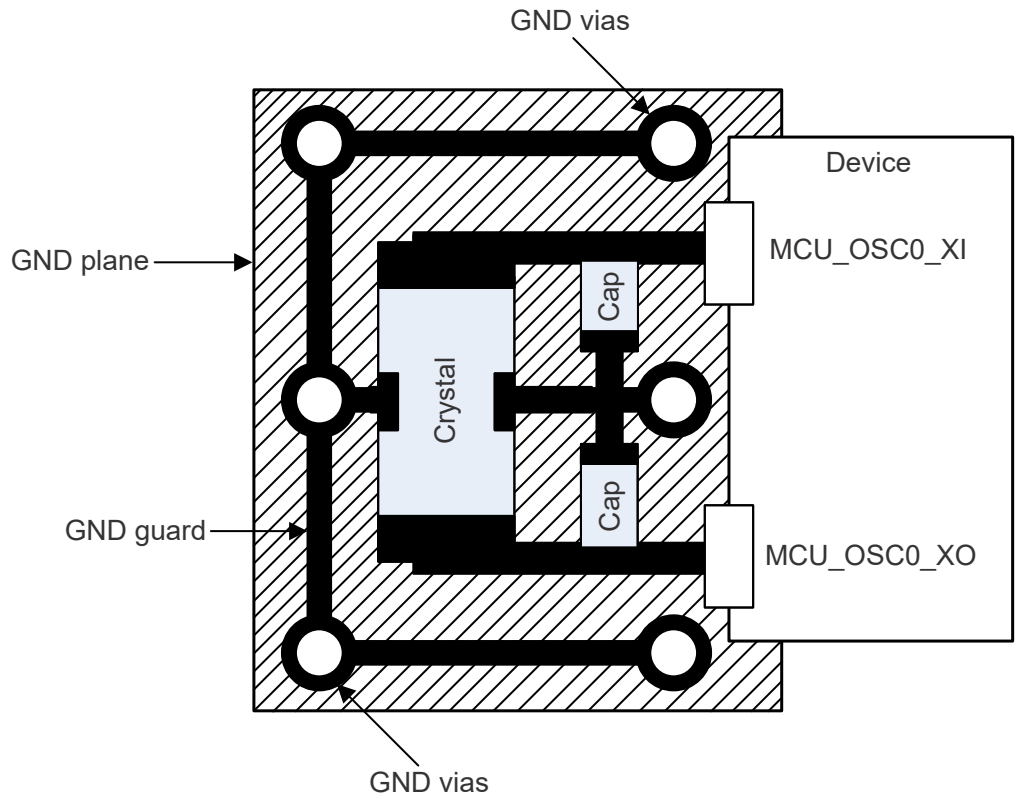

Figure 8-6. MCU_OSC0 PCB requirements

9 Device and Documentation Support

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, TDA4VENxTBD). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of TDA4VEN/TDA4AEN devices in the AMWpackage type, see the Package Option Addendum of this document, the TI website (ti.com), or contact your TI sales representative.

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9.1.1 Standard Package Symbolization

Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

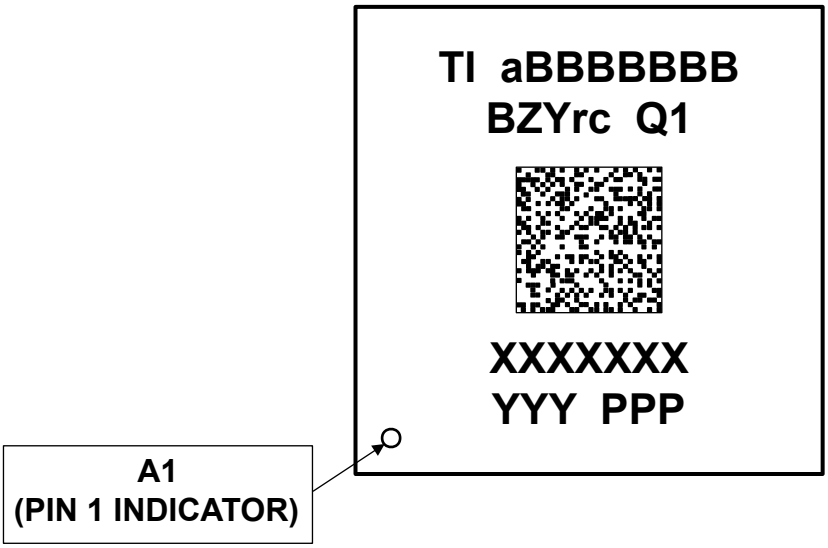

Figure 9-1. Printed Device Reference

9.1.2 Device Naming Convention

Table 9-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUES		DESCRIPTION
		MARKING	ORDERABLE	
x	Device evolution stage(1)	X		Prototype
		P		Preproduction (production test flow, no reliability data)
		BLANK (null)		Production
BBBBBBB**B**	Base production part number	J722S(2)		For more P/N details, see Device Comparison "8=Superset device
		TDA4VEN8		
		TDA4AEN8		
Z	Device Speed Grade	J		See Device Speed Grades table
		K		
Y	Device type	5		High Security capable, Safety capable
r	Device revision	A		SR 1.0
c	Carrier designator (not symbolized on package)	N/A	BLANK	Tray
		N/A	R	Tape and Reel
Q1	Automotive Designator	BLANK		Not automotive qualified. Supports T_J = –40°C to 105°C
		Q1		Meet AEC-Q100 qualification requirements, with exceptions as specified in this document (data sheet). Supports T_J = –40°C to 125°C
	2D Barcode	Varies		Optional 2D barcode, provides additional device information
		Blank		
XXXXXXX	Lot Trace Code (LTC)			
YYY	Production Code, for TI use only			
PPP	Package designator	AMW		AMW FCBGA (18mm × 18mm)
O	Pin one designator			

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Prototype devices are shipped against the following disclaimer:
"This product is still in development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

(2) J722S is the base part number for the preproduction superset device. Software should constrain the features used to match the intended production device.

Note

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

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9.2 Tools and Software

The following Development Tools support development for TI's Embedded Processing platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. The tool includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SysConfig-PinMux Tool The SysConfig-PinMux Tool is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool generates output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements. The **Cloud-based SysConfig-PinMux Tool** is also available.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the TDA4VEN/TDA4AEN devices.

Technical Reference Manual

J722S TDA4VEN TDA4AEN AM67 Processor Silicon Revision 1.0 Technical Reference Manual: Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the TDA4VEN/TDA4AEN family of devices.

Errata

J722S TDA4VEN TDA4AEN AM67 Processor Silicon Revision 1.0 Errata: Describes the known exceptions to the functional specifications for the device.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from March 22, 2024 to September 30, 2024 (from Revision * (March 2024) to Revision A (September 2024)) — **Page**

- **Global:** Changed the document product status from "Advance Information" to "Production Data"..... 1
- (Features): Added "Motion JPEG encode" feature..... 1
- (Features/Media and Data Storage): Updated/Changed the "… eMMC interface up to HS200 speed" to "… up to HS400 speed"..... 1
- (Features): Updated/Changed the CSI2.0 bullet and added sub-bullets..... 1
- (Applications): Add End Equipment (EE) ulinks to the Applications list..... 3
- (Functional Block Diagram): Updated the ulink to the TI Software Development Kits (SDKs)..... 4
- (Functional Block Diagram): Added a "JPEG Encode" block to the Multimedia main block..... 4
- (Device Comparison): Updated the ulink to the TI Software Development Kits (SDKs) in the "To understand what device features are currently supported by TI Software Development Kits. …" Note..... 6
- (Device Comparison): Add the "Motion JPEG Encoder" row to the table..... 6
- (SDIO Electrical Characteristics): Changed VDDSHV5 power rail name, where applicable, used to define the V_{IL}/V_{ILSS}/V_{IH}/V_{IHSS}/V_{OL}/V_{OH} parameter values by referencing a generic power rail name (VDD), and added an associated table note..... 89
- (Recommended Operating Conditions for OTP eFuse Programming): Changed the "VPP Slew Rate" parameter name to "VPP Power-up Slew Rate" to clarify the limit associated with this parameter only applies during power-up..... 92
- (Power-Up Sequencing): Added note to clarify power rails must decay below 300mv before initiating a new power-up sequence..... 97
- (Power-Down Sequencing): Added note to clarify power rails must decay below 300mv before initiating a new power-up sequence..... 100
- (BOOTMODE Timing Requirements): Updated the description for parameters RST23 and RST24..... 103
- (MCU_OSC0 LVCMOS Digital Clock Source): Added the new MCU_OSC0 LVCMOS Digital Clock Source Requirements table..... 115
- (CPSW3G RGMII Timing Conditions): Added operating voltage conditions to the Input Slew Rate parameter to allow a relaxed slew rate when operating at 1.8V..... 127
- (I2C): Changed the maximum slew rate value from 0.8V/ns to 0.08V/ns and added "when operating at 3.3V" to clarify the exception is not applicable to 1.8V operation..... 163
- (MMC0 Timing Requirements – HS400 Mode): Changed the maximum values associated with parameters HS4001, HS4002, HS4003, and HS4004 from 500 to 475..... 182
- (MMC0 Switching Characteristics – HS400 Mode): Replaced the Delay time parameters HS4008 and HS4009 with Output setup and Output hold parameters HS4008, HS4009, HS40010, and HS40011..... 182
- (eMMC in – HS400 Mode – Transmitter Mode): Updated the timing diagram to match the new definitions associated with parameters HS4008, HS4009, HS40010, and HS40011..... 182
- (Device Nomenclature): Updated/Changed the package type (designator) form "AMH" to "AMW" in the orderable part numbers paragraph..... 224

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• (Nomenclature Description): Updated/Changed the table to match the Standard Package Symbolization image.....226

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11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TDA4AEN8J5AAMWRQ1	Active	Production	FCBGA (AMW) | 594	500 | LARGE T&R	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA4AEN 8J5A Q1
TDA4AEN8J5AAMWRQ1.B	Active	Production	FCBGA (AMW) | 594	500 | LARGE T&R	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA4AEN 8J5A Q1
TDA4AEN8K5AAMWRQ1	Active	Production	FCBGA (AMW) | 594	500 | LARGE T&R	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA4AEN 8K5A Q1
TDA4AEN8K5AAMWRQ1.B	Active	Production	FCBGA (AMW) | 594	500 | LARGE T&R	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA4AEN 8K5A Q1
TDA4VEN8J5AAMWRQ1	Active	Production	FCBGA (AMW) | 594	500 | LARGE T&R	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA4VEN 8J5A Q1
TDA4VEN8J5AAMWRQ1.B	Active	Production	FCBGA (AMW) | 594	500 | LARGE T&R	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA4VEN 8J5A Q1
TDA4VEN8K5AAMWRQ1	Active	Production	FCBGA (AMW) | 594	500 | LARGE T&R	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA4VEN 8K5A Q1
TDA4VEN8K5AAMWRQ1.B	Active	Production	FCBGA (AMW) | 594	500 | LARGE T&R	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA4VEN 8K5A Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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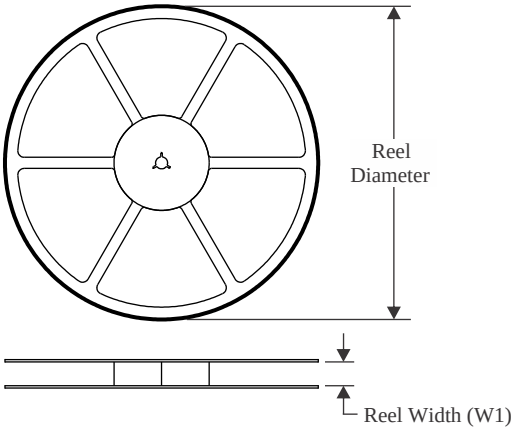
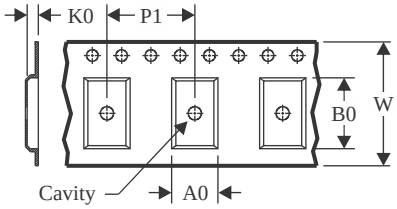
TAPE AND REEL INFORMATION

REEL DIMENSIONS

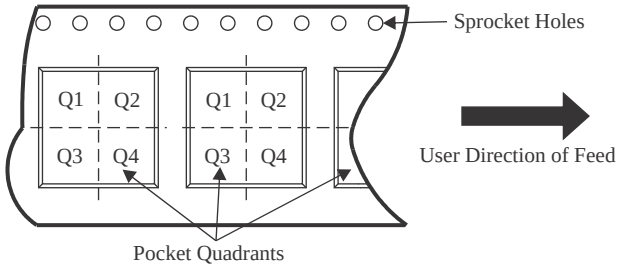


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

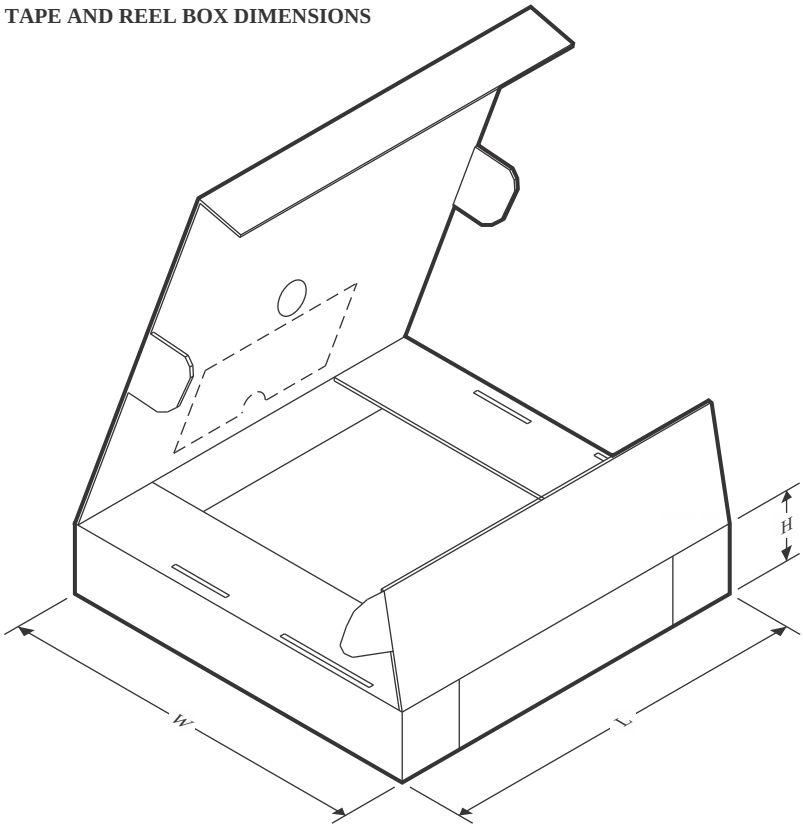
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

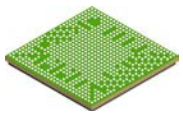
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TDA4AEN8J5AAMWRQ1	FCBGA	AMW	594	500	330.0	32.4	18.35	18.35	3.3	24.0	32.0	Q1
TDA4AEN8K5AAMWRQ1	FCBGA	AMW	594	500	330.0	32.4	18.35	18.35	3.3	24.0	32.0	Q1
TDA4VEN8J5AAMWRQ1	FCBGA	AMW	594	500	330.0	32.4	18.35	18.35	3.3	24.0	32.0	Q1
TDA4VEN8K5AAMWRQ1	FCBGA	AMW	594	500	330.0	32.4	18.35	18.35	3.3	24.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TDA4AEN8J5AAMWRQ1	FCBGA	AMW	594	500	336.6	336.6	41.3
TDA4AEN8K5AAMWRQ1	FCBGA	AMW	594	500	336.6	336.6	41.3
TDA4VEN8J5AAMWRQ1	FCBGA	AMW	594	500	336.6	336.6	41.3
TDA4VEN8K5AAMWRQ1	FCBGA	AMW	594	500	336.6	336.6	41.3

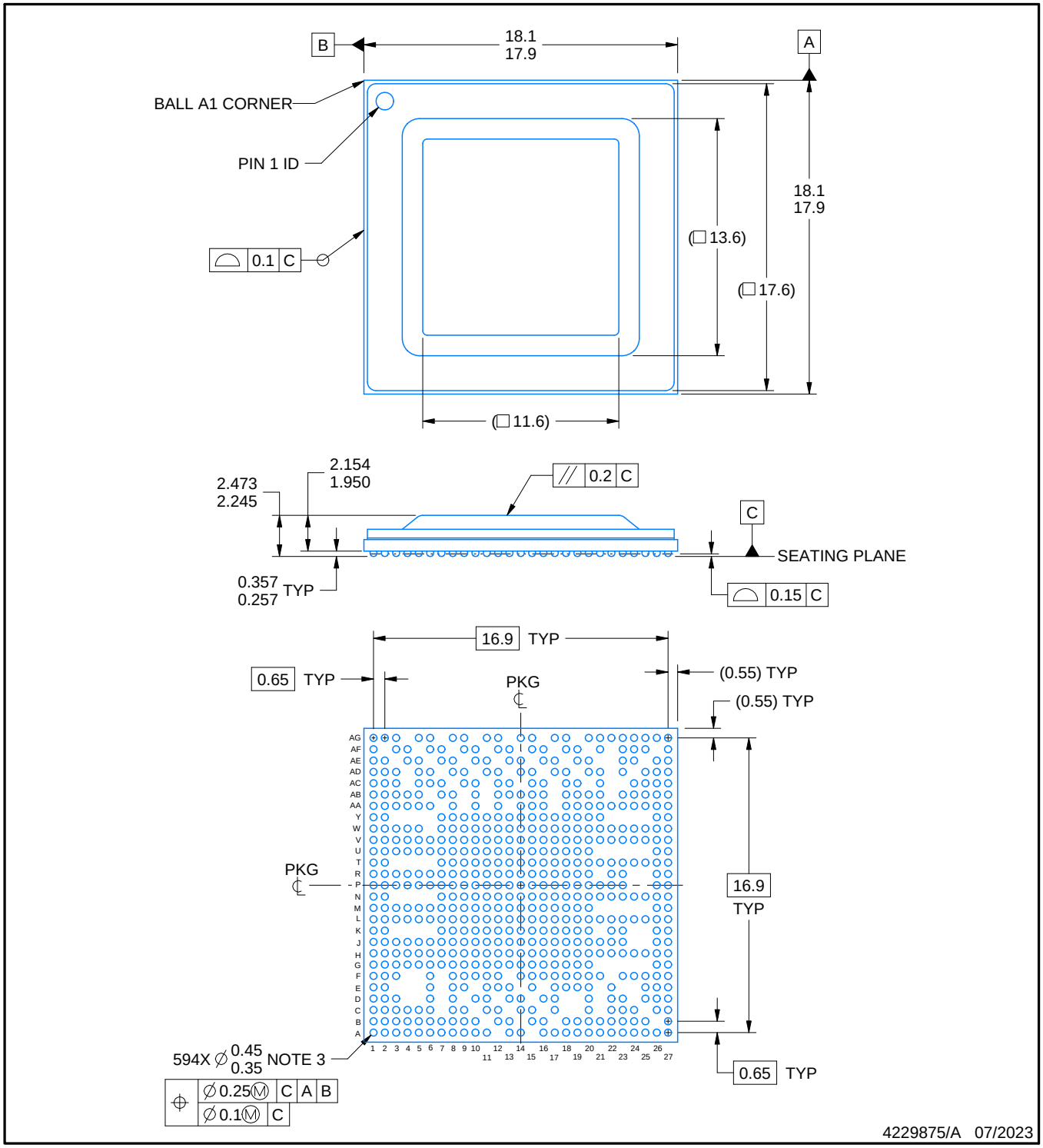


PACKAGE OUTLINE

AMW0594A

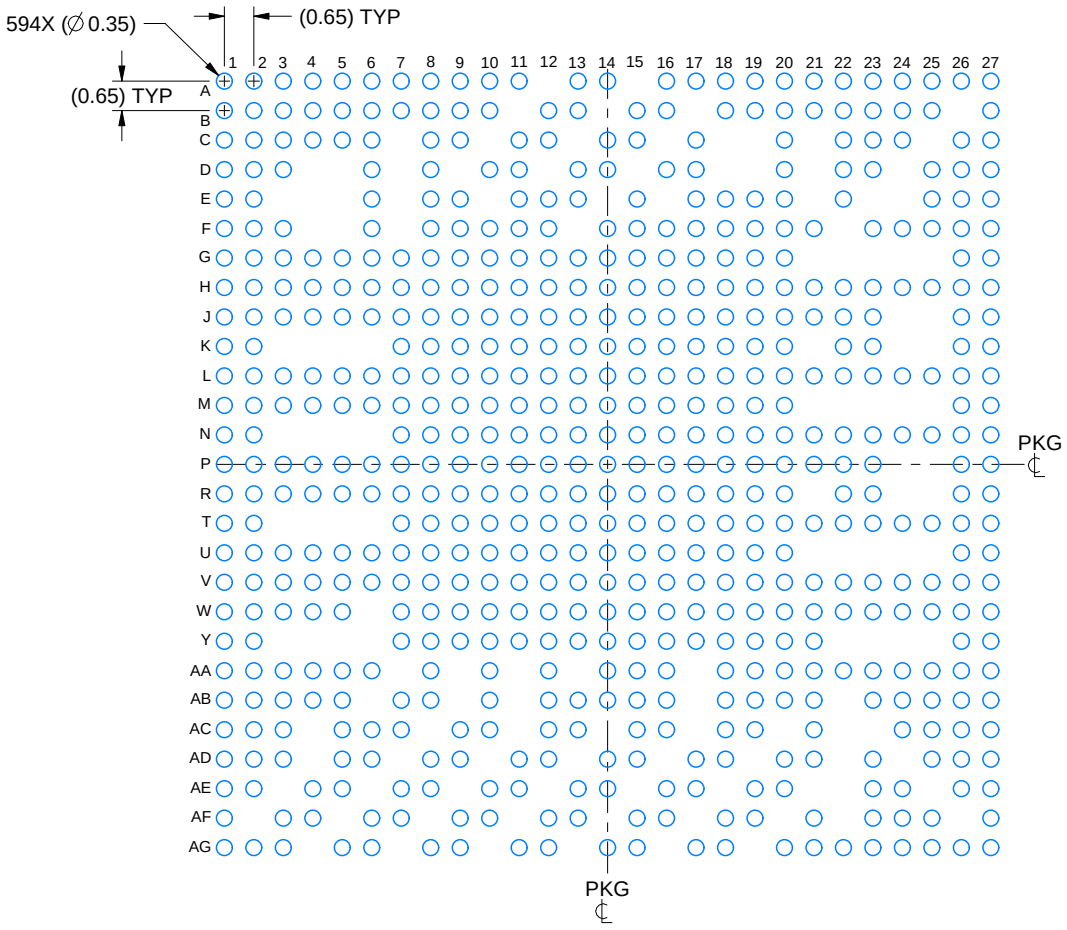
FCBGA - 2.473 mm max height

BALL GRID ARRAY

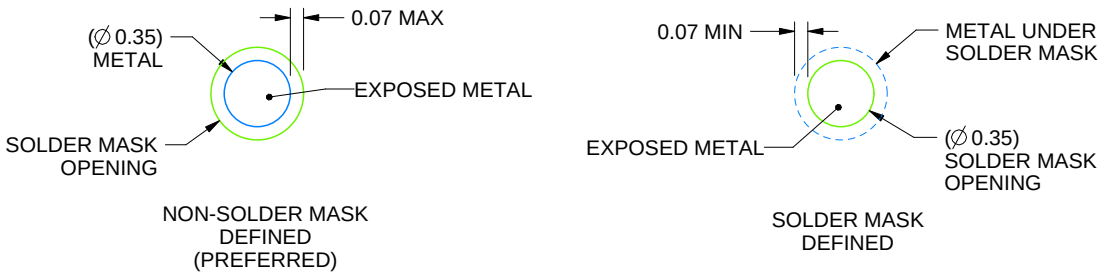


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Ball diameter after reflow. Dimension is measured at the maximum solder ball diameter parallel to primary datum C.



LAND PATTERN EXAMPLE
EXPOSED METAL SNOWN
SCALE:6X

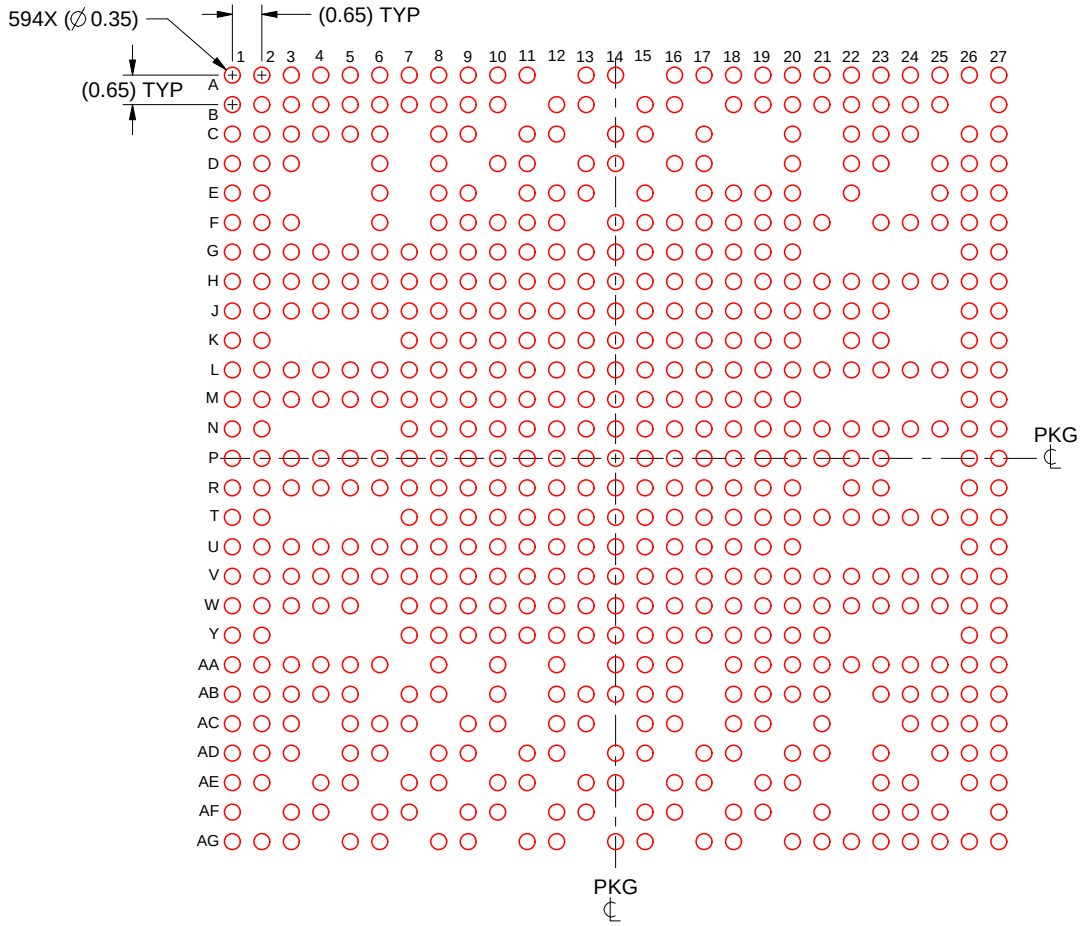


SOLDER MASK DETAILS
NOT TO SCALE

4229875/A 07/2023

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

4229875/A 07/2023

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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