

TCAN857-Q1 Automotive Fault-Protected CAN FD Transceiver with Silent Mode

1 Features

- AEC-Q100 Qualified for automotive applications
 - Human body model (HBM) ESD protection: ±12KV for CANH and CANL pins as per AEC Q100-002
 - Charged-device model (CDM) ESD protection: ±500V as per AEC Q100-011
 - IEC 61000-4-2 Contact discharge: ±8KV (unpowered)
- Compatible with ISO 11898-2:2024 physical layer standard
- **Functional Safety-Capable**
 - Documentation available to aid in functional safety system design
- Support of classical CAN and optimized CAN FD performance at 2Mbps and 5Mbps
 - Short and symmetrical propagation delays for enhanced timing margin
- TCAN857V-Q1 I/O voltage range supports 2.9V to 5.25V
- Support for 12V battery applications
- Receiver common mode input voltage: ±12V
- Protection features:
 - Bus fault protection: ±40V
 - Undervoltage protection
 - TXD-dominant time-out (DTO)
 - Thermal-shutdown protection (TSD)
- Operating modes: Normal and Silent
- Optimized behavior when unpowered
 - Bus and logic pins are high impedance (no load to operating bus or application)
 - Hot-plug capable: power up/down glitch free operation on bus and RXD output
- 8-Pin SOIC, small footprint SOT-23 and leadless VSON-8 package with improved automated optical inspection (AOI) capability

2 Applications

- Automotive and transportation
 - Body control modules
 - Automotive gateway
 - Advanced driver assistance system (ADAS)
 - Infotainment

3 Description

The TCAN857-Q1 is a high speed controller area network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2024 highspeed CAN specification. The transceiver is designed for classical CAN and CAN FD networks up to 5 megabits per second (Mbps).

The transceiver supports two modes of operation; normal mode and silent mode. The transceiver also includes many protection and diagnostic features including thermal shutdown (TSD), TXD-dominant timeout (DTO), and bus fault protection up to ±40V. The device has defined fail-safe behavior in supply under-voltage or floating pin scenarios.

The transceiver features an integrated level shifter on the V_{IO} pin which supplies internal logic-level translation for interfacing the transceiver I/Os directly to 3.3V, or 5V logic level. These transceivers are not only available in industry-standard SOIC-8 and VSON-8 packages, but also have a space-saving small footprint SOT-23 package option.

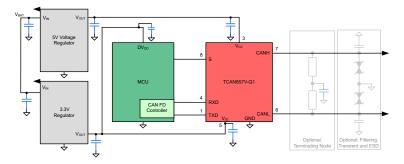
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)
	SOIC (D)	4.9mm x 6mm
TCAN857-Q1	VSON (DRB) (8)	3mm x 3mm
	SOT-23 (DDF) (8)	2.9mm x 2.8mm

- For more information, see Section 11.
- The package size (length × width) is a nominal value and (2)includes pins, where applicable.

Table 3-1. Device Comparison Table

Device Number	Low Voltage I/O Logic Support on Pin 5	Pin 8 Mode Selection					
TCAN857-Q1	No	Silent mode					
TCAN857V-Q1	Yes	Silent mode					



Simplified Schematic



Table of Contents

1 Features	1	7.2 Functional Block Diagram	13
2 Applications		7.3 Feature Description	
3 Description		7.4 Device Functional Modes	
4 Pin Configuration and Functions		8 Application Information Disclaimer	19
5 Specifications	4	8.1 Application Information	
5.1 Absolute Maximum Ratings		8.2 Typical Application	
5.2 ESD Ratings	4	8.3 Power Supply Recommendations	
5.3 ESD Ratings, IEC Specification		8.4 Layout	
5.4 Recommended Operating Conditions	4	9 Device and Documentation Support	
5.5 Thermal Characteristics	4	9.1 Documentation Support	24
5.6 Power Supply Characteristics	<mark>5</mark>	9.2 Receiving Notification of Documentation Update	es <mark>24</mark>
5.7 Dissipation Ratings	<mark>5</mark>	9.3 Support Resources	24
5.8 Electrical Characteristics	<mark>5</mark>	9.4 Trademarks	24
5.9 Switching Characteristics	7	9.5 Electrostatic Discharge Caution	<mark>2</mark> 4
5.10 Typical Characteristics		9.6 Glossary	
6 Parameter Measurement Information		10 Revision History	
7 Detailed Description	13	11 Mechanical, Packaging, and Orderable	
7.1 Overview	13	Information	24



4 Pin Configuration and Functions

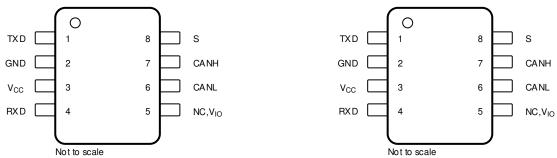


Figure 4-1. DDF Package, 8-Pin SOT (Top View)

Figure 4-2. D Package, 8-Pin SOIC (Top View)

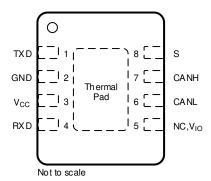


Figure 4-3. DRB Package, 8-Pin VSON (Top View)

Table 4-1. Pin Functions

Pi	ns	Time	Decarintion	
Name	No.	Type	Description	
TXD	1	Digital Input	CAN transmit data input, integrated pull-up	
GND	2	GND	Ground connection	
V _{CC}	3	3 Supply 5V supply voltage		
RXD	4	Digital Output	CAN receive data output, tri-state when powered off	
NC	- 5	_	No connect (not internally connected); devices without V _{IO}	
V _{IO}] 3	Supply	I/O supply voltage	
CANL	6	Bus IO	Low-level CAN bus input/output line	
CANH	7	Bus IO	High-level CAN bus input/output line	
S	8	Digital Input	Silent mode control input, integrated pull-up	
Thermal Pad (VSON only) —		_	Connect the thermal pad to any internal PCB ground plane using multiple vias for optimal thermal performance.	



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.3	6	V
V _{IO}	Supply voltage I/O level shifter	-0.3	6	V
V _{BUS}	CAN Bus I/O voltage (CANH, CANL)	-40	40	V
V _{DIFF}	Max differential voltage range between CANH and CANL	-12	12	V
V _{Logic_Input}	Logic input terminal voltage	-0.3	6	V
V _{RXD}	RXD output terminal voltage range	-0.3	6	V
I _{O(RXD)}	RXD output current	-8	8	mA
TJ	Operating virtual junction temperature range	-40	165	°C
T _{STG}	Storage temperature	-65	150	°C

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
		Human hady model (HPM), per AEC 0400 002(1)	HBM classification level 3A for all pins	±2000	V
V _{ESD}	Electrostatic discharge	discharge Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM classififation global pins CANH	HBM classififation level 3B for global pins CANH & CANL	±12000	V
		Charged-device model (CDM), per AEC Q100-011		±500	V

⁽¹⁾ AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings, IEC Specification

				VALUE	UNIT
V _{ESD}	System level electro-static discharge (ESD) ⁽¹⁾	CAN bus terminals (CANH, CANL) to GND	IEC 61000-4-2 (150pF, 330Ω): Unpowered contact discharge	±8000	V

⁽¹⁾ Tested according to IEC 62228-3 CAN Transcievers (2018), Section 6.4; DIN EN 61000-4.

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{IO}	Supply voltage for I/O level shifter	2.9		5.25	V
I _{OH(RXD)}	RXD terminal high level output current	-2			mA
I _{OL(RXD)}	RXD terminal low level output current			2	mA
TJ	Operational free-air temperature (see thermal characteristics table)	-40		150	°C
T _{SDR}	Thermal shutdown	160			°C
T _{SDF}	Thermal shutdown release			150	°C
T _{SD(HYS)}	Thermal shutdown hysteresis		10		°C

5.5 Thermal Characteristics

THERMAL METRIC	THERMAL METRIC	Paci	UNIT	
	THERWAL WETRIC	D (SOIC)	DRB (VSON)	UNII
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.1	49.9	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	68.3	58.2	°C/W

Product Folder Links: TCAN857-Q1

⁽²⁾ All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

5.5 Thermal Characteristics (continued)

THERMAL	THERMAL METRIC	Paci	UNIT	
METRIC	THERMAL METRIC	D (SOIC)	DRB (VSON)	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	71.6	23.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	1.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.8	23.8	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	_	6.4	°C/W

5.6 Power Supply Characteristics

Over recommended operating conditions with $T_1 = -40^{\circ}$ C to 150°C (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{CC}	Supply current normal mode	Dominant	TXD = 0V, $R_L = 60\Omega$, $C_L = open$			70	mA
I _{CC}	Supply current normal mode	Dominant	TXD = 0V, $R_L = 50\Omega$, $C_L = open$			80	mA
I _{CC}	Supply current normal mode	Dominant with bus fault	TXD = 0V, CANH = CANL = \pm 25V, R _L = open, C _L = open			130	mA
I _{CC}	Supply current normal mode	Recessive	$TXD = V_{CC}$, $R_L = 50\Omega$, $C_L = open$, $RCM = open$			10	mA
I _{CC}	Supply current silent mode		TXD = V_{CC} , $R_L = 50\Omega$, $C_L = open$			3	mA
I _{IO}	I/O supply current normal mode (Devices with V _{IO})	Dominant	RXD floating, TXD = 0V			400	μΑ
I _{IO}	I/O supply current normal mode (Devices with V _{IO})	Recessive	RXD floating, TXD = V _{CC}			150	μΑ
I _{IO}	I/O supply current silent mode (Devices with V _{IO})		RXD floating, TXD = V _{CC}			35	μА
UV _{VCC}	Rising under voltage detecti	Rising under voltage detection on V _{CC} for protected mode			4.2	4.6	V
UV _{VCC}	Falling under voltage detection on V _{CC} for protected mode		3.5	4	4.5	V	
UV _{VIO}	Rising under voltage detection on V _{IO}			2.5	2.9	V	
UV _{VIO}	Falling under voltage detect	ion on V _{IO}		2.1	2.4		V

5.7 Dissipation Ratings

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	V_{CC} = 5 V, V_{IO} = 3.3 V, T_J = 27°C, R_L = 60 Ω , C_{L_RXD} = 15 pF TXD input = 250 kHz 50% duty cycle square wave		90		mW	
FD	Normal mode	$\begin{array}{l} V_{CC}=5.25~\text{V, V}_{IO}=3.3~\text{V, T}_{J}=150^{\circ}\text{C, R}_{L}=60\\ \Omega,~\text{C}_{L_RXD}=15~\text{pF}\\ TXD~\text{input}=2.5~\text{MHz}~50\%~\text{duty cycle square}\\ wave \end{array}$		110		mW

5.8 Electrical Characteristics

Over recommended operating conditions with T_A = -40°C to 125°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT		
Driver Elect	river Electrical Characteristics						
V _{CANH(D)}	Bus output voltage (dominant) CANH	V_{TXD} = 0V, R_L =50 Ω to 65 Ω , C_L = open, R_{CM} = open	2.75	4.5	V		
V _{CANL(D)}	Bus output voltage (dominant) CANL	V_{TXD} = 0V, R_L =50 Ω to 65 Ω , C_L = open, R_{CM} = open	0.5	2.25	V		
V _{CANH(R)} V _{CANL(R)}	Bus output voltage (recessive)	V_{TXD} = VCC1, R_L = open (no load), R_{CM} = open	2	3	V		
V _{SYM}	Driver symmetry (V _{O(CANH)} + V _{O(CANL)})/V _{CC}	R_{TERM} = 60 Ω , C_L = open, C_{SPLIT} = 4.7 nF	0.9	1.1	V/V		

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5.8 Electrical Characteristics (continued)

Over recommended operating conditions with $T_A = -40^{\circ}C$ to $125^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
V _{SYM_DC}	DC output symmetry (V _{CC} - V _{O(CANL)})	R _L = 60 Ω, C _L = open	-400	400	mV
	Differential output voltage	V_{TXD} = 0V, R_L =50 Ω to 65 Ω , C_L = open, R_{CM} = open	1.5	3	V
$V_{DIFF(D)}$	normal mode Dominant	V_{TXD} = 0V, $45\Omega \le R_L \le 70\Omega$, C_L = open	1.4	3.3	V
		V_{TXD} = 0V, R_L = 2240 Ω , C_L = open	1.5	5	V
	Differential output voltage	$V_{TXD} = V_{CC}$, $R_L = 60\Omega$, $C_L = open$	-120	12	mV
$V_{DIFF(R)}$	normal mode Recessive	Normal mode, TXD = V_{CC} , R_L = open, C_L = open	-50	50	mV
I _{CANH(OS)}	Short-circuit steady-state	$-3V \le V_{CANH} \le +18V$, CANL = open, $V_{TXD} = 0V$	-115		mA
I _{CANL(OS)}	output current, Dominant	$-3V \le V_{CANL} \le +18V$, CANH = open, $V_{TXD} = 0V$		115	mA
I _{OS_REC}	Short-circuit steady-state output current; Recessive	-40V ≤ V _{BUS} ≤ +40V _, V _{BUS} = CANH = CANL	- 5	5	mA
Receiver Ele	ctrical Characteristics				
$V_{DIFF_RX(D)}$	Receiver dominant state differential input voltage range, bus biasing active	-12V ≤ V _{CANL} ≤ +12V -12V ≤ V _{CANH} ≤ +12V	0.9	8	V
$V_{DIFF_RX(R)}$	Receiver recessive state differential input voltage range, bus biasing active	-12V ≤ V _{CANL} ≤ +12V -12V ≤ V _{CANH} ≤ +12V	-3	0.5	V
V _{HYS}	Hysteresis voltage for input- threshold, normal mode	-12V ≤ V _{CM} ≤ 12V		80	mV
V _{CM}	Common mode range:		-12	12	V
I _{LKG(IOFF)}	Power-off (unpowered) bus input leakage current	CANH = CANL = 5V		5	μΑ
Cı	Input capacitance to ground (CANH or CANL)	$V_{TXD} = V_{CC}, V_{IO} = V_{CC}$		20	pF
C _{ID}	Differential input capacitance	$TXD = V_{CC}, V_{IO} = V_{CC}$		10	pF
m _R	Input resistance matching: [1 – (R _{IN(CANH)} / R _{IN(CANL)})] × 100%	V _{CANH} = V _{CANL} = 5V	-2%	2%	
TXD Termina	I (CAN Transmit Data Input)			1	
V _{IH}	High-level input voltage	TCAN857-Q1	0.7 × V _{CC}		V
V _{IH}	High-level input voltage	TCAN857V-Q1	0.7 × V _{IO}		V
V _{IL}	Low-level input voltage	TCAN857-Q1		0.3 × V _{CC}	V
V _{IL}	Low-level input voltage	TCAN857V-Q1		0.3 × V _{IO}	V
I _{IH}	High-level input leakage current	$V_{TXD} = V_{CC} = V_{IO} = 5.25V$	-2.5	0 1	μΑ
I _{IL}	Low-level input leakage current	V _{TXD} = 0V, V _{CC} = V _{IO} = 5.25V	-200	-20	μΑ
I _{LKG(OFF)}	Unpowered leakage current	$V_{TXD} = 5.25V, V_{CC} = V_{IO} = 0V$	-1	0 1	μΑ
Cı	Input Capacitance	$V_{IN} = 0.4 \times \sin(2 \times \pi \times 2 \times 10^6 \times t) + 2.5V$		2	pF
RXD Termina	I (CAN Receive Data Output)				
V _{OH}	High-level input voltage	TCAN857-Q;1 I _O = -2mA	0.8 × V _{CC}		V
V _{OH}	High-level input voltage	TCAN857V-Q1; $I_O = -2mA$	0.8 × V _{IO}		V
V _{OL}	Low-level input voltage	TCAN857-Q1; I _O = 2mA		0.2 × V _{CC}	V
V _{OL}	Low-level input voltage	TCAN857V-Q1; I _O = 2mA		0.2 × V _{IO}	V
I _{LKG(OFF)}	Unpowered leakage current	RXD = 5.25V, V _{CC} = V _{IO} = 0V	-1	0 1	μΑ
S Terminal (Silent Mode Input)				
V _{IH}	High-level input voltage	TCAN857-Q1	0.7 × V _{CC}		V
V _{IH}	High-level input voltage	TCAN857V-Q1	0.7 × V _{IO}		V
V _{IL}	Low-level input voltage	TCAN857-Q1		0.3 × V _{CC}	V

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5.8 Electrical Characteristics (continued)

Over recommended operating conditions with T_A = -40°C to 125°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
V _{IL}	Low-level input voltage	TCAN857V-Q1		0.3 × V _{IO}	V
I _{IH}	High-level input leakage current S	V _{CC} = V _{IO} = S = 5.25V	-2	2	μΑ
I _{IL}	Low-level input leakage current S	V _{CC} = V _{IO} = 5.25 V, S = 0V	-20	-2	μΑ
I _{LKG(OFF)}	Unpowered leakage current	S = 5.25V, V _{CC} = V _{IO} = 0V	-1	0 1	μΑ

5.9 Switching Characteristics

Over recommended operating conditions with $T_A = -40^{\circ}C$ to $125^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switch	ing Characteristics					
t _{PROP(LOOP1)}	Total loop delay, driver input (TXD) to	Normal mode, V _{IO} = 3V to 5V, R _L =		100	220	ns
	receiver output (RXD), recessive to dominant Total loop delay, driver input (TXD) to	60Ω , $C_L = 100pF$, $C_{L_RXD} = 15pF$ Normal mode, $V_{IO} = 3V$ to $5V$, $R_L = 100$		110	200	
t _{PROP(LOOP2)}	receiver output (RXD), dominant to recessive	$60Ω$, $C_L = 100pF$, $C_{L_RXD} = 15pF$		110	220	ns
t _{MODE}	Mode change time, from Normal to Silent or from Silent to Normal				45	μs
t _{WK_FILTER}	Filter time for a valid wake-up pattern		0.5		1.8	μs
t _{WK_TIMEOUT}	Bus wake-up timeout value		0.8		6	ms
Driver Switchi	ng Characteristics					
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)			50		ns
t _{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)	$R_L = 60\Omega$, $C_L = 100$ pF, $R_{CM} = 0$ pen		45		ns
t _{sk(p)}	Pulse skew (tpHR - tpLD)	THE COLL, OF TOOP!, I CIM Spoil		4		ns
t _R	Differential output signal rise time			32		ns
t _F	Differential output signal fall time			27		ns
t _{TXD_DTO}	Dominant timeout	$R_L = 60\Omega, C_L = 100pF$	0.8		6.5	ms
Receiver Switch	ching Characteristics					
t _{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)			75		ns
t _{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)	C _{L_RXD} = 15pF		70		ns
t _R	RXD output signal rise time			10		ns
t _F	RXD output signal fall time			10		ns
FD Timing Cha	aracteristics					
$t_{\Delta ext{Bit(Bus)}}$	Transmitted recessive bit width variation: t _{BIT(TXD)} = 500 ns	$R_L = 60\Omega$, $C_L = 100pF$, $C_{L_RXD} = 15pF$ $t_{\Delta Bit(Bus)} = t_{BIT(Bus)} - t_{BIT(TXD)}$	-65		30	ns
$t_{\Delta Bit(Bus)}$	Transmitted recessive bit width variation: t _{BIT(TXD)} = 200 ns	$R_L = 60\Omega$, $C_L = 100pF$, $C_{L_RXD} = 15pF$ $t_{\Delta Bit(Bus)} = t_{BIT(Bus)} - t_{BIT(TXD)}$	-45		10	ns
$t_{\Delta Bit(RXD)}$	Received recessive bit width variation: $t_{BIT(TXD)} = 500 \text{ ns}$	$R_L = 60\Omega$, $C_L = 100pF$, $C_{L,RXD} = 15pF$ $t_{\Delta Bit(Bus)} = t_{BIT(RXD)} - t_{BIT(TXD)}$	-100		50	ns
$t_{\Delta Bit(RXD)}$	Received recessive bit width variation: $t_{BIT(TXD)} = 200 \text{ ns}$	$R_L = 60\Omega$, $C_L = 100pF$, $C_{L,RXD} = 15pF$ $t_{\Delta Bit(Bus)} = t_{BIT(RXD)} - t_{BIT(TXD)}$	-80		20	ns



5.9 Switching Characteristics (continued)

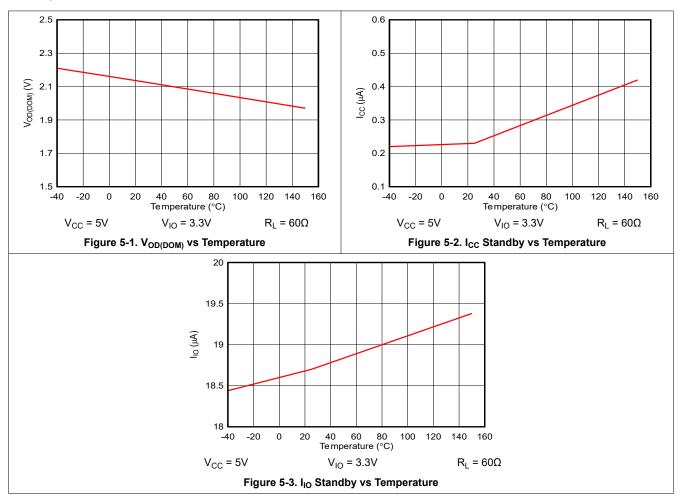
Over recommended operating conditions with T_A = -40°C to 125°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
'AREC		$R_L = 60\Omega$, $C_L = 100pF$, $C_{L_RXD} =$	-65		40	ns
$t_{\Delta REC}$	Receiver timing symmetry with t _{BIT(TXD)} = 200 ns	$\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-45		15	ns

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5.10 Typical Characteristics





6 Parameter Measurement Information

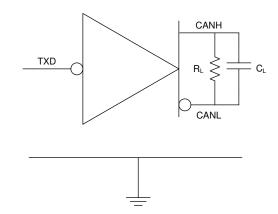


Figure 6-1. I_{CC} Test Circuit

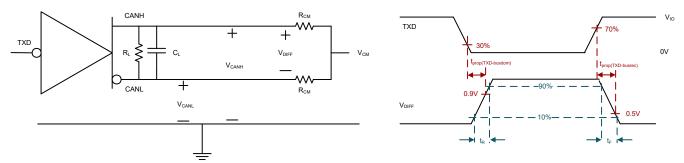


Figure 6-2. Driver Test Circuit and Measurement

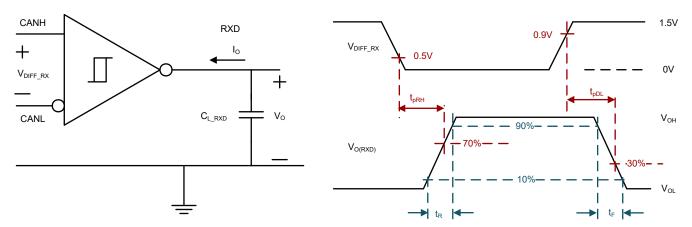


Figure 6-3. Receiver Test Circuit and Measurement

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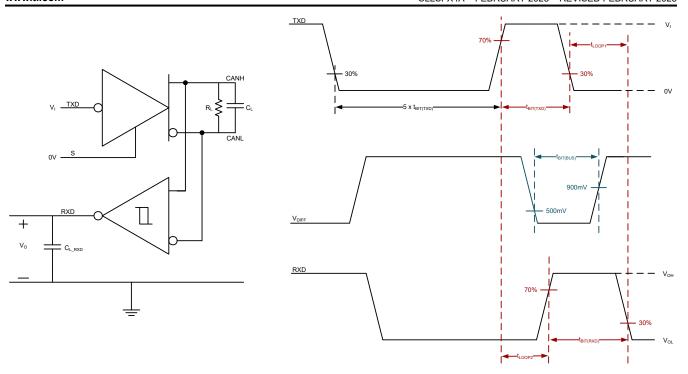


Figure 6-4. Transmitter and Receiver Timing Test Circuit and Measurement

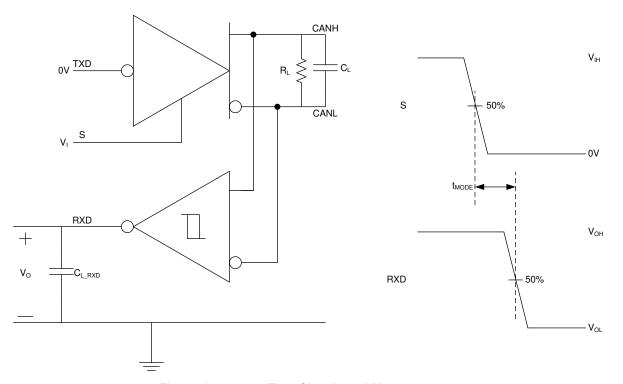


Figure 6-5. t_{MODE} Test Circuit and Measurement



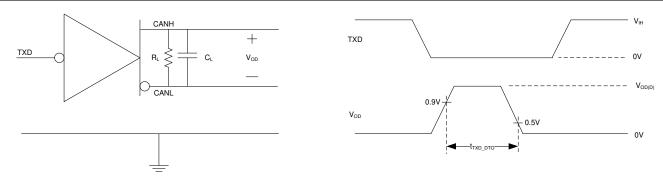


Figure 6-6. TXD Dominant Timeout Test Circuit and Measurement

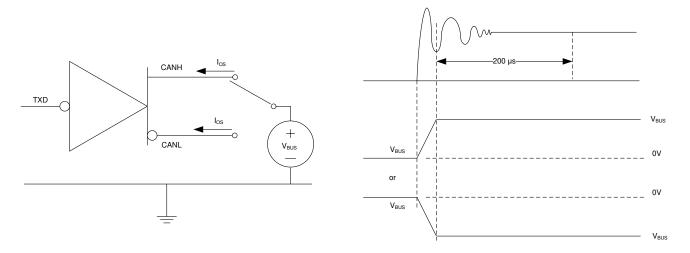


Figure 6-7. Driver Short-Circuit Current Test and Measurement

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7 Detailed Description

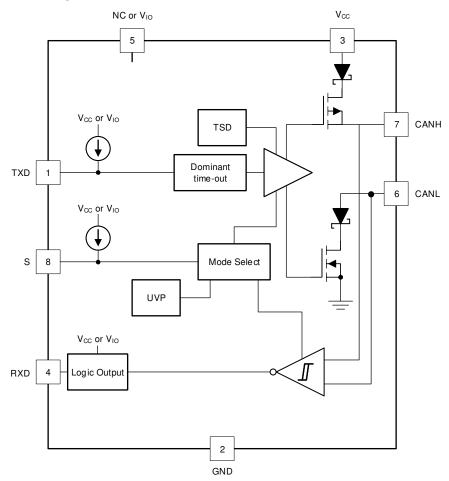
7.1 Overview

The TCAN857(V)-Q1 devices meet or exceed the specifications of the ISO 11898-2:2024 high speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO 11898-2:2024 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceiver provides a number of different protection features providing for stringent automotive system requirements while also supporting CAN FD data rates up to 5Mbps.

The devices support the following CAN standards:

- CAN transceiver physical layer standards:
 - ISO 11898-2:2024 High speed medium access unit
 - ISO 11898-5:2007 High speed medium access unit with low-power mode
 - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125kbps
 - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250kbps
 - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500kbps
 - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 2Mbps
 - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 5Mbps
- Conformance Test requirements:
 - ISO 16845-2 Road vehicles Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

7.2 Functional Block Diagram





7.3 Feature Description

7.3.1 Pin Description

7.3.1.1 TXD

The TXD input is a logic-level signal, referenced to either V_{CC} or V_{IO} from a CAN controller to the transceivers.

7.3.1.2 GND

GND is the ground pin of the transceiver, and must be connected to the PCB ground.

7.3.1.3 V_{CC}

V_{CC} provides the 5V power supply to the CAN transceiver.

7.3.1.4 RXD

The RXD output is a logic-level signal, referenced to either V_{CC} or V_{IO} , from the transceivers to the CAN controller. RXD is only driven once V_{IO} is present.

7.3.1.5 V_{IO}

The V_{IO} pin is the input source for the integrated level shifter which provides the transceiver I/O voltage. Connect the V_{IO} pin to the controller I/O voltage source.

7.3.1.6 CANH and CANL

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transmitter and receiver internally.

7.3.1.7 S (Silent)

The S pin is an input pin used for silent mode control of the transceiver. The S pin can be supplied from either the controller or from a static system voltage source. If normal mode is the only intended mode of operation, then the S pin can be tied directly to system GND using a pull-down resistor. If the silent mode is the only intended mode of operation, then the S pin can be tied directly to a static system voltage source using a pull-up resistor.

7.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 7-1.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ though the high-resistance internal input resistors R_{IN}) of the receiver, and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case, the differential voltage of the bus is greater than the differential voltage of a single driver.

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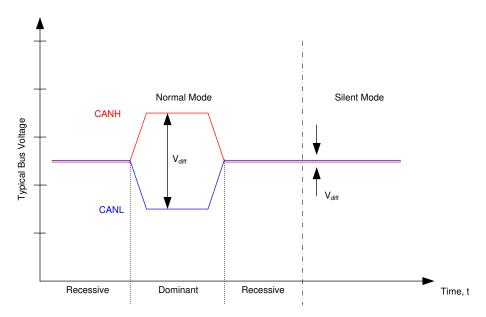


Figure 7-1. Bus States

7.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO} . The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO} , the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin; thus, clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using Equation 1.

Minimum Data Rate = 11 bits /
$$t_{TXD\ DTO}$$
 = 11 bits / $0.8ms$ = 13.75kbps (1)



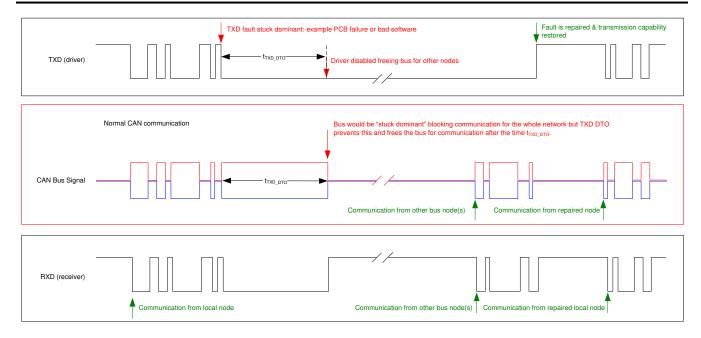


Figure 7-2. Example Timing Diagram for TXD Dominant Timeout

7.3.4 CAN Bus Short-circuit Current Limiting

The device has several protection features that limit the short-circuit current when a CAN bus line is shorted. The features include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state due to a system fault. During CAN communication the bus switches between the dominant and recessive states; thus, the short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design, the average power rating, $I_{OS(AVG)}$, is used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. Making sure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%$$
 Transmit x [(% REC_Bits x $I_{OS(SS)}$ REC) + (% DOM_Bits x $I_{OS(SS)}$ DOM)] + [% Receive x $I_{OS(SS)}$ REC] (2)

Where:

- I_{OS(AVG)} is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- I_{OS(SS)} REC is the recessive steady state short-circuit current
- I_{OS(SS)} DOM is the dominant steady state short-circuit current

This short-circuit current and the possible fault cases of the network is taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

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7.3.5 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shutdown threshold, T_{TSD} , the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD} . The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The device TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

7.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO} , have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

Table 7-1. Undervoltage Lockout - TCAN857(V)-Q1

V _{CC}	DEVICE STATE	BUS	RXD PIN
> UV _{VCC}	Normal	Per TXD	Mirrors bus
< UV _{VCC}	Protected	High impedance Weak pull-down to ground ⁽¹⁾	High impedance

(1) $V_{CC} = GND$, see $I_{LKG(OFF)}$

Table 7-2. V_{IO} Undervoltage Lockout - TCAN857(V)-Q1

V _{cc}	V _{IO}	DEVICE STATE	BUS	RXD PIN
> UV _{VCC}	> UV _{VIO}	Normal	Per TXD	Mirrors bus
< 111/	> 111/	S = V _{IO} : Silent mode		Recessive
< UV _{VCC}	> UV _{VIO}	S = GND: Protected mode	High impedance	Necessive
> UV _{VCC}	< UV _{VIO}	Protected	Weak pull-down to ground ⁽¹⁾	High impedance
< UV _{VCC}	< UV _{VIO}	Protected		High impedance

⁽¹⁾ $V_{CC} = GND$, see $I_{LKG(OFF)}$

Once the undervoltage condition is cleared and t_{MODE} has expired, the device transitions to normal mode. The host controller can again send and receive CAN traffic.

7.3.7 Unpowered Device

The device is designed to be a no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so the device does not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, and do not load other circuits which may remain powered.

7.3.8 Floating pins

The device has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias must not be relied upon by design though, especially in noisy environments, but instead is considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This makes sure the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See Table 7-3 for details on pin bias conditions.

Table 7-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering
S	Pull-up	Weakly biases S towards low-power silent mode to prevent excessive system power

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7.4 Device Functional Modes

7.4.1 Operating Modes

The device has two main operating modes; normal mode and silent mode. Operating mode selection is made by applying a high or low level to the S pin.

Table 7-4. Operating Modes

S	Device Mode	Driver	Receiver	RXD Pin
High	Silent mode	Disabled	Enabled	Mirrors bus state
Low	Normal Mode	Enabled	Enabled	WIITOIS DUS State

7.4.2 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

7.4.3 Silent Mode

In silent mode, the CAN driver is disabled and the high-speed CAN receiver is enabled. CAN communication is unidirectional into the device where the receiver is translating the differential signal from CANH and CANL to a digital output on RXD. The power consumption of the TCAN857(V)-Q1 is reduced in silent mode due to the CAN driver being disabled.

7.4.4 Driver and Receiver Function

The digital input and output levels for the device are CMOS levels with respect to either V_{CC} or V_{IO}.

Table 7-5. Driver Function Table

Device Mode	TXD Input ⁽¹⁾	Bus O	Driven Bus State ⁽²⁾					
Device Mode	TAD IIIput	CANH	CANL	Dilveil Bus State				
Normal	Low	High	Low	Dominant				
Nomai	High or open	High impedance	High impedance	Biased recessive				
Silent	X	High impedance	High impedance	Biased recessive				

- (1) X = irrelevant
- (2) For bus state see Figure 7-1

Table 7-6. Receiver Function Table Normal and Silent Mode

Device Mode	CAN Differential Inputs V _{ID} = V _{CANH} - V _{CANL}	Bus State	RXD Pin
	V _{ID} ≥ 0.9V	Dominant	Low
Normal or Silent	0.5V < V _{ID} < 0.9V	Undefined	Undefined
	V _{ID} ≤ 0.5V	Recessive	High
Any	Open (V _{ID} ≈ 0V)	Open	High

Product Folder Links: TCAN857-Q1



8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application

Figure 8-1 shows a typical configuration for 5V system using the device. The bus termination is shown for illustrative purposes.

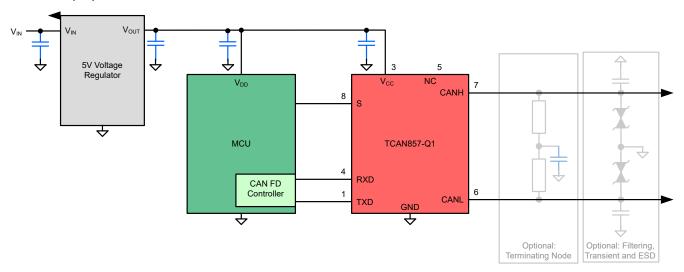


Figure 8-1. Transceiver Application Using 5V I/O Connections



8.2.1 Design Requirements

8.2.1.1 CAN Termination

Termination may be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see Figure 8-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

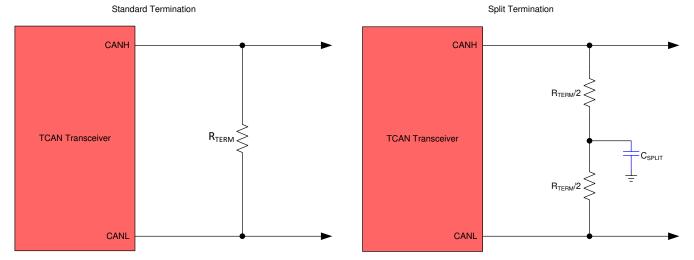


Figure 8-2. CAN Bus Termination Concepts

8.2.2 Detailed Design Procedures

8.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 meters. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN857(V)-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2024 specification the driver differential output is specified with a bus load that can range from 50Ω to 65Ω where the differential output must be greater than 1.5V. The TCAN857(V)-Q1 family is specified to meet the 1.5V requirement down to 50Ω and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance of the transceiver is a minimum of $40k\Omega$. If 100 transceivers are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 52Ω . Therefore, the TCAN857(V)-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity; thus, a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design for a robust network operation.

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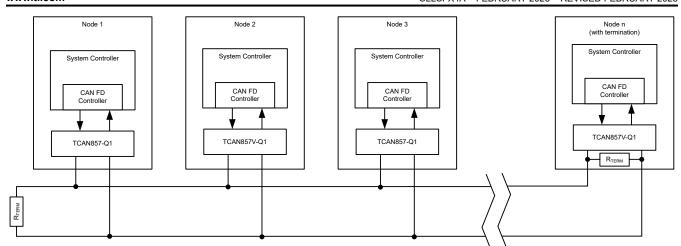


Figure 8-3. Typical CAN Bus

8.2.3 System Examples

Figure 8-4 shows a typical configuration for 3.3V or 5V systems using the TCAN857(V)-Q1. The bus termination is shown for illustrative purposes.

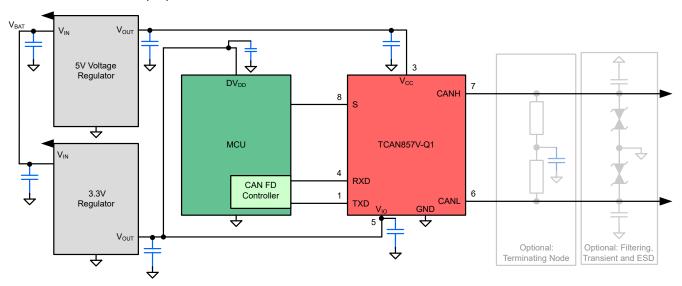


Figure 8-4. Typical Transceiver Application Using 3.3V IO Connections

8.2.4 Application Curve

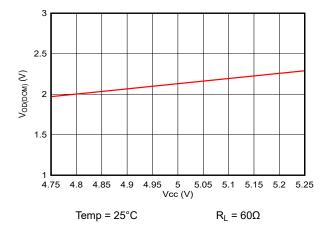


Figure 8-5. $V_{OD(DOM)}$ vs V_{CC}

8.3 Power Supply Recommendations

The TCAN857(V)-Q1 transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.75V and 5.25V. The TCAN857(V)-Q1 implements an I/O level shifting supply input, V_{IO} , designed for a range between 3V and 5.25V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100nF, is placed near the CAN transceiver main V_{CC} supply pin in addition to bypass capacitors. A decoupling capacitor, typically 100nF, is placed near the CAN transceiver V_{IO} supply pin in addition to bypass capacitors.

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8.4 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques can be applied during PCB design.

8.4.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows a optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter 0.1µF capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling 0.1µF capacitors is placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

Note

High frequency current follows the path of least impedance and not the path of least resistance.

This layout example shows how split termination could be implemented on the CAN node. The termination is split into two 60Ω resistors, R4 and R5, with the center or split tap of the termination connected to ground via a 1nF - 100nF capacitor C3. Split termination provides common-mode filtering for the bus. See CAN Termination, CAN Bus Short Circuit Current Limiting, and Equation 2 for information on termination concepts and power ratings needed for the termination resistor(s).

8.4.2 Layout Example

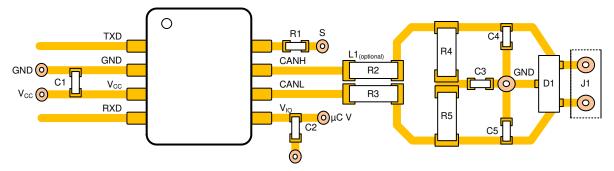


Figure 8-6. Layout Example



9 Device and Documentation Support

9.1 Documentation Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision * (February 2025) to Revision A (February 2025)	Page
•	Initial public release	1
	Updated Typical Characteristics plots	
	Updated Application Curve plots	

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TCAN857DDFRQ1	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857
TCAN857DDFRQ1.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857
TCAN857DRBRQ1	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857
TCAN857DRBRQ1.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857
TCAN857DRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857
TCAN857DRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857
TCAN857VDDFRQ1	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857V
TCAN857VDDFRQ1.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857V
TCAN857VDRBRQ1	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857V
TCAN857VDRBRQ1.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857V
TCAN857VDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857V
TCAN857VDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	T857V

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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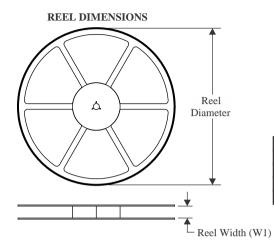
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN857DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN857VDDFRQ1	SOT-23- THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCAN857VDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN857VDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1



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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN857DRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN857VDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCAN857VDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN857VDRQ1	SOIC	D	8	2500	340.5	338.1	20.6

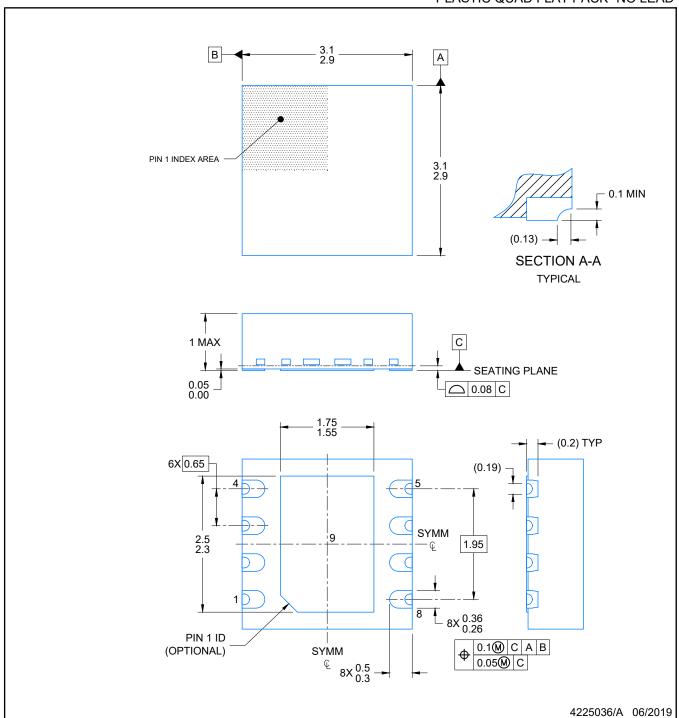


Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4203482/L



PLASTIC QUAD FLAT PACK- NO LEAD

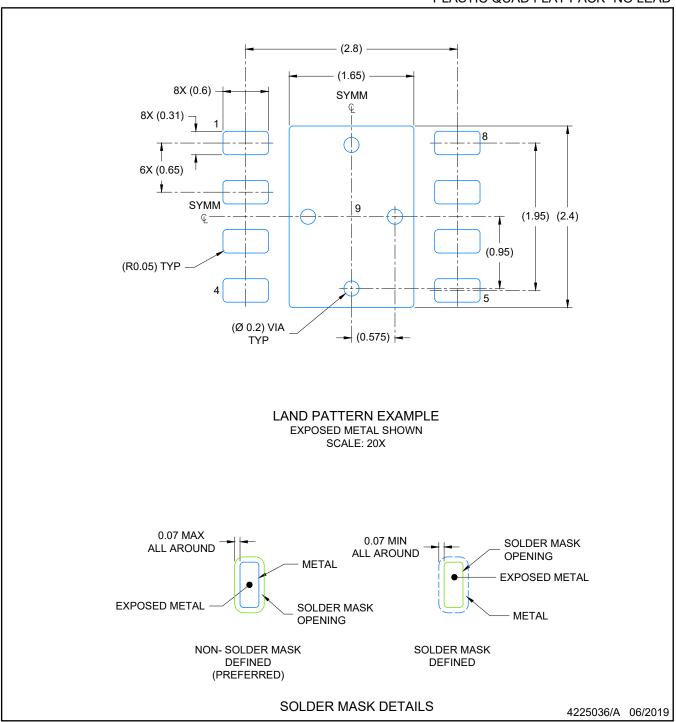


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK- NO LEAD

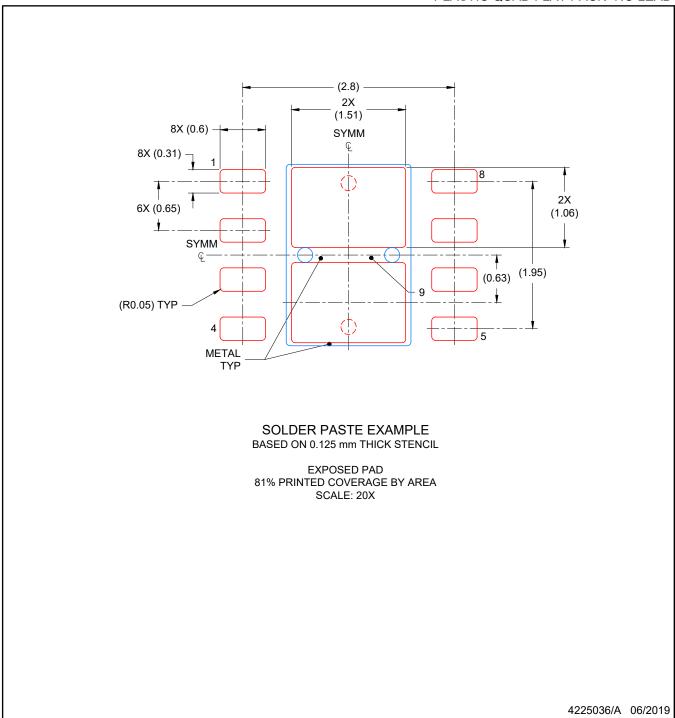


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





PLASTIC SMALL OUTLINE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 7. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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