TCAN843-Q1 Automotive CAN FD Transceiver With Sleep Mode

1 Features

- AEC Q100 Qualified for automotive applications
- Functional Safety-Capable
  - Documentation will be available at release to aid in functional safety system design
- Meets the requirements of ISO 11898-2:2024
- Wide input operational voltage range
- Supports classic CAN and CAN FD up to 5Mbps
- V_{IO} level shifting supports: 3.3V to 5.5V
- Operating modes:
  - Normal mode
  - Silent mode
  - Standby mode
  - Low-power sleep mode
- High-voltage INH output for system power control
- Local wake-up support via the WAKE pin
- Defined behavior when unpowered
  - Bus and IO terminals are high impedance (no load to operating bus or application)
- Protection features:
  - ±40V CAN bus fault tolerant
  - Load dump support on V_{SUP}
  - IEC ESD protection
  - Under-voltage protection
  - Thermal shutdown protection
  - TXD dominant state timeout (TXD DTO)
- Available in 14-pin leaded (SOT and SOIC) packages and leadless (VSON) package with wettable flanks for improved automated optical inspection (AOI) capability

2 Applications

- Body electronics and lighting
- Automotive gateway
- Advanced driver assistance systems (ADAS)
- Infotainment and cluster
- Hybrid, electric & powertrain systems
- Personal transport vehicles - electric bike
- Industrial transportation

3 Description

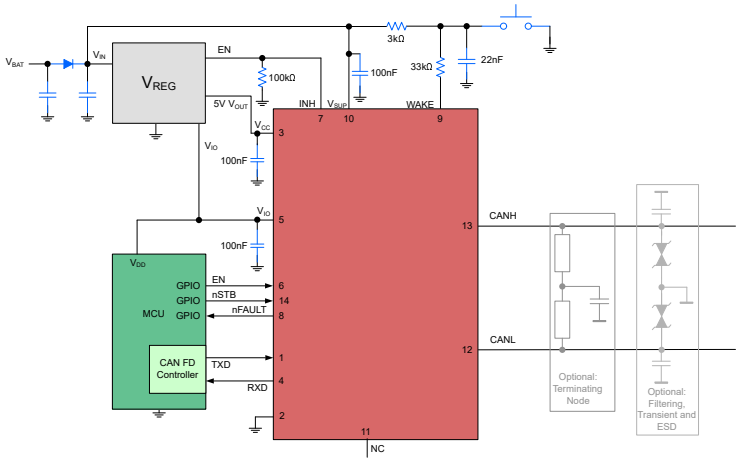
The TCAN843-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2024 high-speed CAN specification. The device supports both classical CAN and CAN FD data rates up to 5 megabits per second (Mbps).

The TCAN843-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a system via the INH output pin. This allows a low-current sleep state in which power is gated to all system components except for the TCAN843-Q1, while monitoring the CAN bus. When a wake-up event is detected, the TCAN843-Q1 initiates system start-up by driving INH high.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAN843-Q1	SOT (DYY)	4.2mm x 2mm
	SOIC (D)	8.65mm x 6mm
	VSON (DMT)	4.5mm x 3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

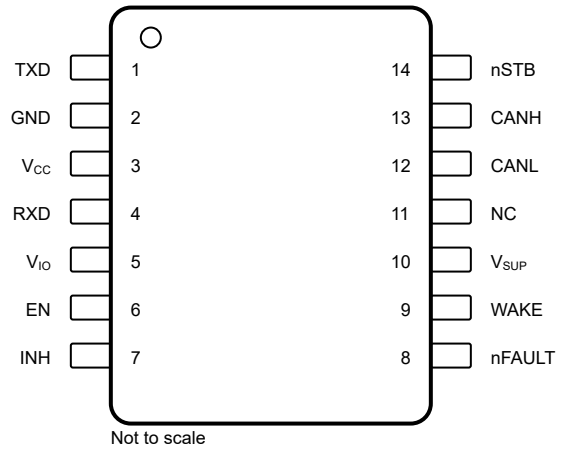

Figure 4-1. D and DYY Packages, 14 Pin (SOIC) and (SOT) (Top View)

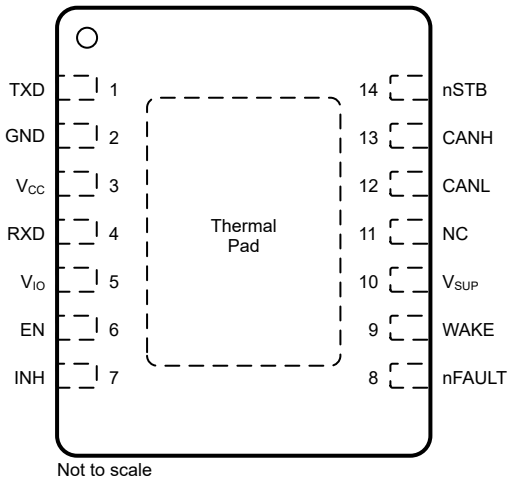

Figure 4-2. DMT Package, 14 Pin (VSON) (Top View)

PINS		TYPE (1)	DESCRIPTION
NAME	NO.		
TXD	1	I	CAN transmit data input, integrated pull-up
GND	2	GND	Ground connection
V_{CC}	3	P	5V transceiver supply
RXD	4	O	CAN receive data output, tri-state when V_{IO} < UV_{IO}
V_{IO}	5	P	I/O supply voltage
EN	6	I	Enable input for mode control, integrated pull-down
INH	7	O	Inhibit pin to control system voltage regulators and supplies, high-voltage
nFAULT	8	O	Fault output, inverted logic
WAKE	9	I	Local WAKE input terminal, high voltage
V_{SUP}	10	P	High-voltage supply from battery
NC	11	NC	No connect, internally not connected
CANL	12	I/O	Low-level CAN bus input/output line
CANH	13	I/O	High-level CAN bus input/output line
nSTB	14	I	Standby mode control input, integrated pull-down
Thermal Pad	—		Connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

(1) I = input, O = output, P = power, GND = ground, NC = not connected

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage(2)	–0.3	40	V
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN bus I/O voltage (CANH, CANL)	–40	40	V
V_{DIFF}	CAN bus differential voltage (V_{DIFF} = V_{CANH} - V_{CANL})	-40	40	V
V_{WAKE}	WAKE input voltage	–40	40 and $V_I \le V_{SUP}$+0.3	V
V_{INH}	INH pin voltage	-0.3	40 and $V_O \le V_{SUP}$+0.3	V
V_{LOGIC}	Logic pin voltage	–0.3	6	V
$I_{O(LOGIC)}$	Logic pin output current		8	mA
$I_{O(INH)}$	Inhibit pin output current		6	mA
$I_{O(WAKE)}$	WAKE pin output current		3	mA
T_J	Junction temperature	–40	165	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Able to support load dumps of up to 40V for 300ms

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	CANH and CANL with respect to GND	±8000	V
			All pins except CANH and CANL with respect to GND	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
V_{ESD}	System level electro-static discharge (ESD)	CAN bus terminals (CANH CANL) to GND	IEC 61000-4-2 (150pF, 330Ω): Unpowered contact discharge	±8000	V

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage	4.5		28	V
V_{IO}	I/O supply voltage	2.9		5.5	V
V_{CC}	CAN transceiver supply voltage	4.5		5.5	V
$I_{OH(DO)}$	Digital output high-level current	–2			mA
$I_{OL(DO)}$	Digital output low-level current			2	mA
$I_{O(INH)}$	Inhibit output current			2	mA
T_J	Operating junction temperature	-40		150	°C

5.4 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_{SDR}	Thermal shutdown	165			°C
T_{SDF}	Thermal shutdown release	155			°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis		10		°C

5.5 Thermal Information

THERMAL METRIC (1)		D (SOIC)	DMT (VSON)	DYY (SOT)	UNIT
		14 PINS	14 PINS	14 PINS	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	87.1	39.7	91.0	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	41.8	41.1	41.7	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	43.7	15.9	25.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.5	0.9	25.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.3	15.9	1.1	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.6	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Power Supply Characteristics

Over recommended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12V, V_{IO} = 3.3V, V_{CC} = 5V and R_L = 60Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage and Current Characteristics						
I_{SUP_NORMAL}	Supply current CAN active	Normal mode, silent mode, go-to-sleep mode			140	µA
I_{SUP_STBY}	Supply current	Standby mode, T_J = –40°C to 85°C			60	µA
I_{SUP_SLEEP}	Supply current	Sleep mode, T_J = –40°C to 85°C		18	30	µA
$UV_{SUP(R)}$	Undervoltage V_{SUP} threshold rising		3.9		4.3	V
$UV_{SUP(F)}$	Undervoltage V_{SUP} threshold falling		3.6		4	V
I_{CC_NORMAL}	Supply current CAN active: dominant	Normal mode TXD = 0V, R_L = 60Ω, C_L = open			70	mA
	V_{CC} supply current normal mode Dominant with bus fault	Normal mode TXD = 0V, R_L = open, C_L = open, CANH = CANL = ±25V			130	mA
	Supply current CAN active: recessive	Normal mode TXD = 0V, R_L = 60Ω, C_L = open			7.5	mA
I_{CC_STBY}	Supply current, Standby mode CAN autonomous: inactive	Standby mode T_J = –40°C to 85°C EN = nSTB = 0V			3.5	µA
I_{CC_SILENT}	Supply current, Silent mode	Silent and go-to-sleep mode TXD = nSTB = V_{IO}, R_L = 60Ω, C_L = open			4	mA
I_{CC_SLEEP}	Supply current, Sleep mode CAN autonomous: inactive	Sleep mode T_J = –40°C to 85°C EN = 0V or V_{IO}, nSTB = 0V			3.2	µA
$UV_{CC(R)}$	Undervoltage V_{CC} threshold rising		4	4.1	4.3	V
$UV_{CC(F)}$	Undervoltage V_{CC} threshold falling		3.8	3.9	4.1	V
$V_{HYS(UVCC)}$	Hysteresis voltage on UV_{CC}		50		300	mV
I_{IO_NORMAL}	I/O supply current	Normal mode RXD floating, TXD = 0V			200	µA
I_{IO_NORMAL}	I/O supply current	Normal mode, silent mode, standby mode, or go-to-sleep mode RXD floating, TXD = V_{IO}			3	µA

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5.6 Power Supply Characteristics (continued)

Over recommended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12V, V_{IO} = 3.3V, V_{CC} = 5V and R_L = 60Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IO_SLEEP}	I/O supply current	Sleep mode T_J = –40°C to 85°C nSTB = 0V			2.5	µA
$UV_{IO(R)}$	Under voltage V_{IO} threshold rising	Ramp up	2.2	2.5	2.8	V
$UV_{IO(F)}$	Under voltage V_{IO} threshold falling	Ramp down	2.1	2.4	2.7	V
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{IO}		40	100	160	mV

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5.7 Electrical Characteristics

Over recommended operating conditions with T_J = –40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12V, V_{IO} = 3.3V, V_{CC} = 5V and R_L = 60Ω

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN Driver Characteristics							
$V_{CANH(D)}$	Dominant output voltage Bus biasing active	CANH	TXD = 0V, 50Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{CANH(R)}$ $V_{CANL(R)}$	Recessive output voltage Bus biasing active		TXD = V_{IO}, R_L = open (no load), R_{CM} = open	2	2.5	3	V
V_{SYM}	Driver symmetry Bus biasing active ($V_{O(CANH)}$ + $V_{O(CANL)}$) / V_{CC}		EN = nSTB= V_{IO}, R_L = 60Ω, C_{SPLIT} = 4.7nF, C_L = Open, R_{CM} = Open, TXD = 250kHz, 1MHz, 2.5MHz	0.9		1.1	V/V
V_{SYM_DC}	DC Driver symmetry Bus biasing active V_{CC} – $V_{O(CANH)}$ – $V_{O(CANL)}$		EN = nSTB= V_{IO}, R_L = 60Ω, C_L = open	-300		300	mV
$V_{DIFF(D)}$	Differential output voltage Bus biasing active Dominant	CANH - CANL	EN = nSTB = V_{IO}, TXD = 0V, 50Ω ≤ R_L ≤ 65Ω, C_L = open	1.5		3	V
		CANH - CANL	EN = nSTB = V_{IO}, TXD = 0V, 45Ω ≤ R_L ≤ 70Ω, CL = open	1.4		3.3	V
		CANH - CANL	EN = nSTB = V_{IO}, TXD = 0V, R_L = 2240Ω, C_L = open	1.5		5	V
$V_{DIFF(R)}$	Differential output voltage Bus biasing active Recessive	CANH - CANL	EN = nSTB = V_{IO}, TXD = V_{IO}, R_L = open, C_L = open	–50		50	mV
$V_{CANH(INACT)}$	Bus output voltage with bus biasing inactive	CANH	nSTB = 0V, TXD = V_{IO}, R_L = open (no load), C_L = open	-0.1		0.1	V
		CANL	nSTB = 0V, TXD = V_{IO}, R_L = open (no load), C_L = open	-0.1		0.1	V
		CANH - CANL	nSTB = 0V, TXD = V_{IO}, R_L = open (no load), C_L = open	-0.2		0.2	V
$I_{CANH(OS)}$	Short-circuit steady-state output current Bus biasing active Dominant		nSTB = V_{IO}, TXD = 0V –3V ≤ $V_{(CANH)}$ ≤ 18V	-100			mA
			nSTB = V_{IO}, TXD = 0V –3V ≤ $V_{(CANL)}$ ≤ 18V			100	mA
I_{OS_REC}	Short-circuit steady-state output current Bus biasing active Recessive		nSTB = V_{IO}, V_{BUS} = CANH = CANL –27V ≤ V_{BUS} ≤ 40V	-3		3	mA
CAN Receiver Characteristics							
$V_{DIFF\_RX(D)}$	Receiver dominant state input voltage range Bus biasing active		nSTB = V_{IO}, –12V ≤ V_{CM} ≤ 12V	0.9		8	V
$V_{DIFF\_RX(R)}$	Receiver recessive state input voltage range Bus biasing active			-3		0.5	V
V_{HYS}	Hysteresis voltage for input threshold Bus biasing active		nSTB = V_{IO}		80		mV
$V_{DIFF\_RX(D\_INACT)}$	Receiver dominant state input voltage range Bus biasing inactive		nSTB = 0V, –12V ≤ V_{CM} ≤ 12V	1.1		9	V
$V_{DIFF\_RX(R\_INACT)}$	Receiver recessive state input voltage range Bus biasing inactive			-4		0.4	V
V_{CM}	Common mode range		nSTB = V_{IO}	–12		12	V
$I_{LKG(IOFF)}$	Power-off (unpowered) input leakage current CANH, CANL pins		V_{SUP} = 0V, CANH = CANL = 5V			5	µA
C_I	Input capacitance to ground (CANH or CANL) (1)					20	pF
C_{ID}	Differential input capacitance (1)					10	pF
R_{DIFF}	Differential input resistance		TXD = V_{CC} = V_{IO} = 5V, nSTB = 5V –2V ≤ V_{CM} ≤ 7V	50		100	kΩ
R_{SE_CANH} R_{SE_CANL}	Input resistance (CANH or CANL)			25		50	kΩ
m_R	Input resistance matching: [1 – $R_{IN(CANH)}$ / $R_{IN(CANL)}$] × 100%		$V_{(CANH)}$ = $V_{(CANL)}$ = 5V	–2		2	%
TXD Characteristics							

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5.7 Electrical Characteristics (continued)

Over recommended operating conditions with T_J = –40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12V, V_{IO} = 3.3V, V_{CC} = 5V and R_L = 60Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	TXD = V_{IO} = 5.5V	-1	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0V, V_{IO} = 5.5V	-115		-2.5	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5V, V_{SUP} = V_{IO} = 0V	–1	0	1	µA
C_I	Input Capacitance	V_{IN} = 0.4 x sin(2 × π × 2 × 10^6 × t) + 2.5V		5	10	pF
RXD Characteristics						
V_{OH}	High-level output voltage	I_O = –2mA	0.8			V_{IO}
V_{OL}	Low-level output voltage	I_O = 2mA			0.2	V_{IO}
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5V, V_{SUP} = V_{IO} = 0V	-1		1	µA
nSTB Characteristics						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	nSTB = V_{IO} = 5.5V	0.5		115	µA
I_{IL}	Low-level input leakage current	nSTB = 0V, V_{IO} = 5.5V	–1		1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	nSTB = 5.5V, V_{IO} = 0V	–1	0	1	µA
nFAULT Characteristics						
V_{OH}	High-level output voltage	I_O = –2mA	0.8			V_{IO}
V_{OL}	Low-level output voltage	I_O = 2mA			0.2	V_{IO}
$I_{LKG(OFF)}$	Unpowered leakage current	nFAULT = 5.5V, V_{IO} = 0V	–1	0	1	µA
EN Characteristics						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	EN = V_{CC} = V_{IO} = 5.5V	0.5		115	µA
I_{IL}	Low-level input leakage current	EN = 0 V, V_{CC} = V_{IO} = 5.5V	-1		1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	EN = 5.5V, V_{CC} = V_{IO} = 0V	-1		1	µA
R_{PD}	Pull-down resistance		50		2000	kΩ
WAKE Characteristics						
V_{IH}	High-level input voltage	Sleep mode	2.6			V
V_{IL}	Low-level input voltage				1.8	V
I_{IH}	High-level input leakage current(2)	WAKE = V_{SUP}			2	µA
		WAKE = 4V	-3			µA
I_{IL}	Low-level input leakage current(2)	WAKE = 1V			3	µA
R_{WAKE}	Pull-up/pull-down resistance(2)			600		kΩ
INH Characteristics						
ΔV_H	High-level voltage drop from VSUP to INH (V_{SUP} - V_{INH})	I_{INH} = –2mA		1	2	V
$I_{LKG(INH)}$	Sleep mode leakage current	INH = 0V	–0.5		0.5	µA

(1) Specified by design and verified via bench characterization
(2) To minimize system level current consumption, the WAKE pin will automatically configure itself based on the applied voltage to either an internal pull-up or pull-down current source. A high-level input results in an internal pull-up and a low-level input results in an internal pull-down.

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5.8 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Characteristics							
t_{PWRUP}	Time required for INH active after $V_{SUP} \geq UV_{SUP(R)}$				310	1000	µs
t_{UV}	Undervoltage filter time V_{CC} and V_{IO} (1)		$V_{CC} \leq UV_{CC}$ or $V_{IO} \leq UV_{IO}$	100		350	ms
t_{UV_det}	Undervoltage detection time for V_{CC} and V_{IO}		$V_{CC} \leq UV_{CC}$ or $V_{IO} \leq UV_{IO}$			30	µs
$t_{UV(RE-ENABLE)}$	Re-enable time after undervoltage event (1)		Time for device to return to normal operation from a UV_{CC} or UV_{IO} undervoltage event			50	µs
Device Characteristics							
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD) Recessive to dominant		R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF V_{IO}=3V - 5.5V			250	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD) Dominant to recessive		R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF V_{IO}=3V - 5.5V			250	ns
$t_{WK(TIMEOUT)}$	Bus wake-up timeout value (1)			0.8		2	ms
$t_{WK(FILTER)}$	Bus time to meet filtered bus requirements for wake-up request (1)			0.5		1.8	µs
t_{FILTER_IO}	Filter time for EN/nSTB(1)			1		5	µs
t_{WAKE_HT}	Hold time for which WAKE pin voltage should be stable after the rising or falling edge on WAKE pin to recognize LWU.			5		50	µs
Mode Change Characteristics							
$t_{INH\_SLP\_STB}$	Time after WUP or LWU event until INH asserted (1)					50	µs
$t_{RXD\_SLP\_STB}$	Time after WUP or LWU event until RXD asserted		Time after WUP or LWU event until RXD asserted			50	µs
t_{MODE1}	Mode change time from leaving the Sleep mode to entering Normal or Silent mode (1)		Time measured from VCC and VIO crossing UV thresholds to entering normal or silent mode.			50	µs
t_{MODE2}	Mode change time between normal, silent and standby mode and from sleep to standby mode (1)		Mode change time between normal, silent and standby mode and from sleep to standby mode			50	µs
$t_{nFAULT\_MODE\_CHANGE}$	nFAULT stabilization time after mode change					20	µs
$t_{GOTOSLEEP}$	Minimum hold time for transition to sleep mode (1)		EN = H and nSTB = L	20		50	µs

(1) Specified by design and verified via bench characterization

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5.9 Switching Characteristics

Over recommended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12V, V_{IO} = 3.3V, V_{CC} = 5V and R_L = 60Ω

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Characteristics								
t_{pHR}	Propagation delay time, high TXD to driver recessive		Propagation delay time, high TXD to driver recessive	R_L = 60Ω, C_L = 100pF, R_{CM} = open		90		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant					75		ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)					25		ns
t_R	Differential output signal rise time					45		ns
t_F	Differential output signal fall time					45		ns
t_{TXDDTO}	Dominant timeout			TXD = 0V, R_L = 60Ω, C_L = open	1.2		3.8	ms
Receiver Characteristics								
t_{pRH}	Propagation delay time, bus recessive input to high RXD			$C_{L(RXD)}$ = 15pF		65		ns
t_{pDL}	Propagation delay time, bus dominant input to RXD low output					60		ns
t_R	Output signal rise time (RXD)					10		ns
t_F	Output signal fall time (RXD)					10		ns
t_{BUSDOM}	Dominant time out			R_L = 60Ω, C_L = open	1.2		3.8	ms
CAN FD Characteristics								
$t_{\Delta BIT(BUS)}$ (1)	Transmitted recessive bit width variation on CAN bus output pins with $t_{BIT(TXD)}$ = 500ns	Transmitted recessive bit width variation on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns		R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(BUS)} = t_{BIT(BUS)} - t_{BIT(TXD)}$	-65		30	ns
$t_{\Delta BIT(BUS)}$ (1)	Transmitted recessive bit width variation on CAN bus output pins with $t_{BIT(TXD)}$ = 200ns	Transmitted recessive bit width variation on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns		R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(BUS)} = t_{BIT(BUS)} - t_{BIT(TXD)}$	-45		10	ns
$t_{\Delta BIT(RXD)}$ (1)	Received recessive bit width variation on RXD output pins with $t_{BIT(TXD)}$ = 500ns	Received recessive bit width variation on RXD output pins with $t_{BIT(TXD)}$ = 500 ns		R_L = 60Ω, C_2 = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(RXD)} = t_{BIT(RXD)} - t_{BIT(TXD)}$	-100		50	ns
$t_{\Delta BIT(RXD)}$ (1)	Received recessive bit width variation on RXD output pins with $t_{BIT(TXD)}$ = 200ns	Received recessive bit width variation on RXD output pins with $t_{BIT(TXD)}$ = 200 ns		R_L = 60Ω, C_2 = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(RXD)} = t_{BIT(RXD)} - t_{BIT(TXD)}$	-80		20	ns
$t_{\Delta REC}$ (1)	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500ns			R_L = 60Ω, C_2 = 100pF, C_{L_RXD} = 15pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	–65		40	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200ns			R_L = 60Ω, C_2 = 100pF, C_{L_RXD} = 15pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	–45		15	ns

(1) The input signal on TXD shall have rise times and fall times (10% to 90%) of less than 10ns

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6 Parameter Measurement Information

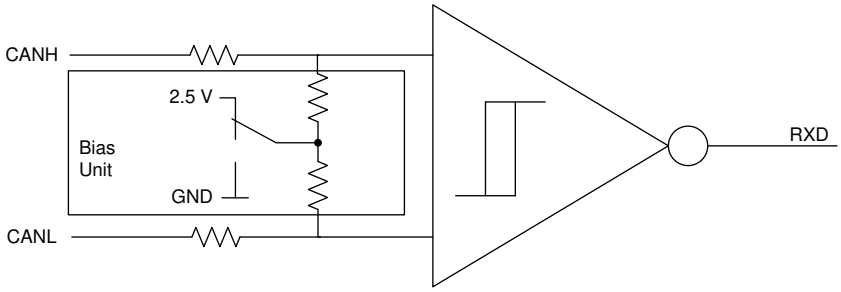

Figure 6-1. Common-Mode Bias Unit and Receiver

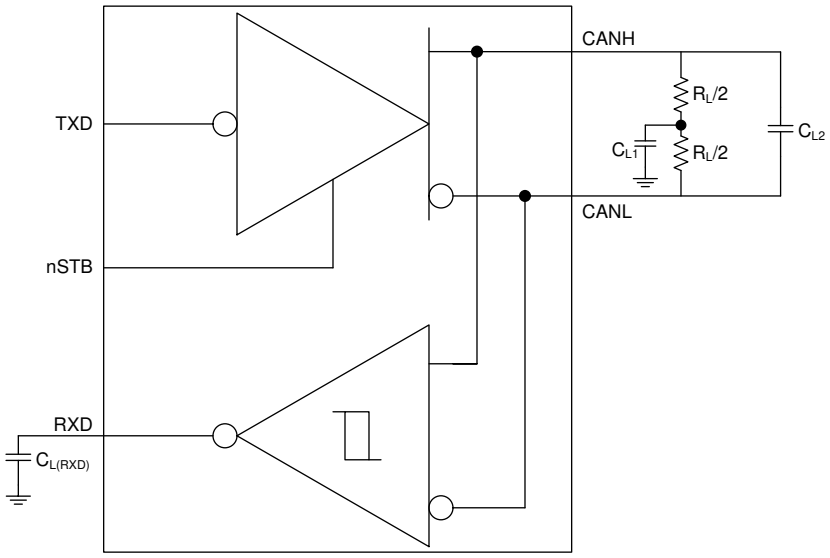

Figure 6-2. Test Circuit

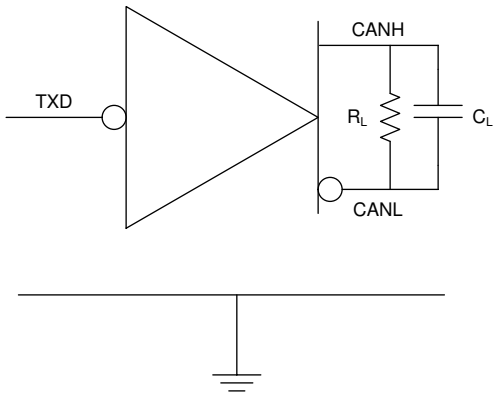

Figure 6-3. Supply Test Circuit

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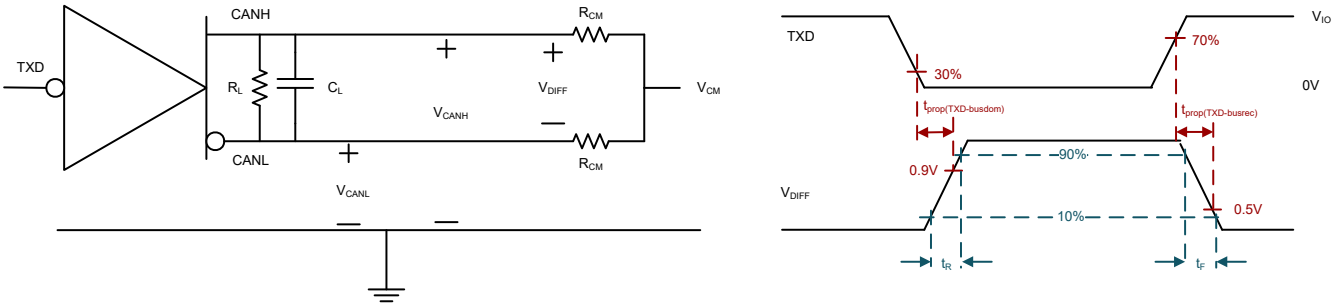

Figure 6-4. Driver Test Circuit and Measurement

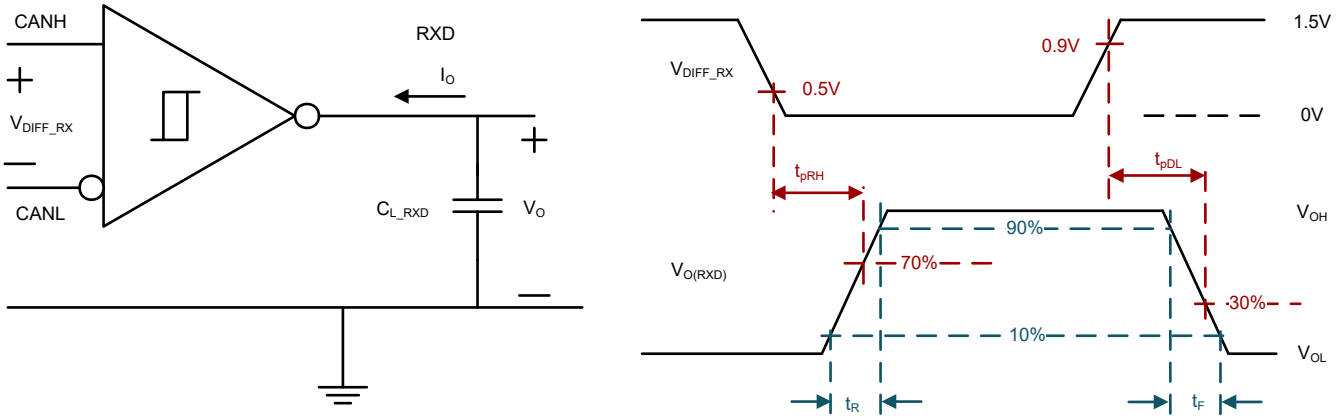

Figure 6-5. Receiver Test Circuit and Measurement

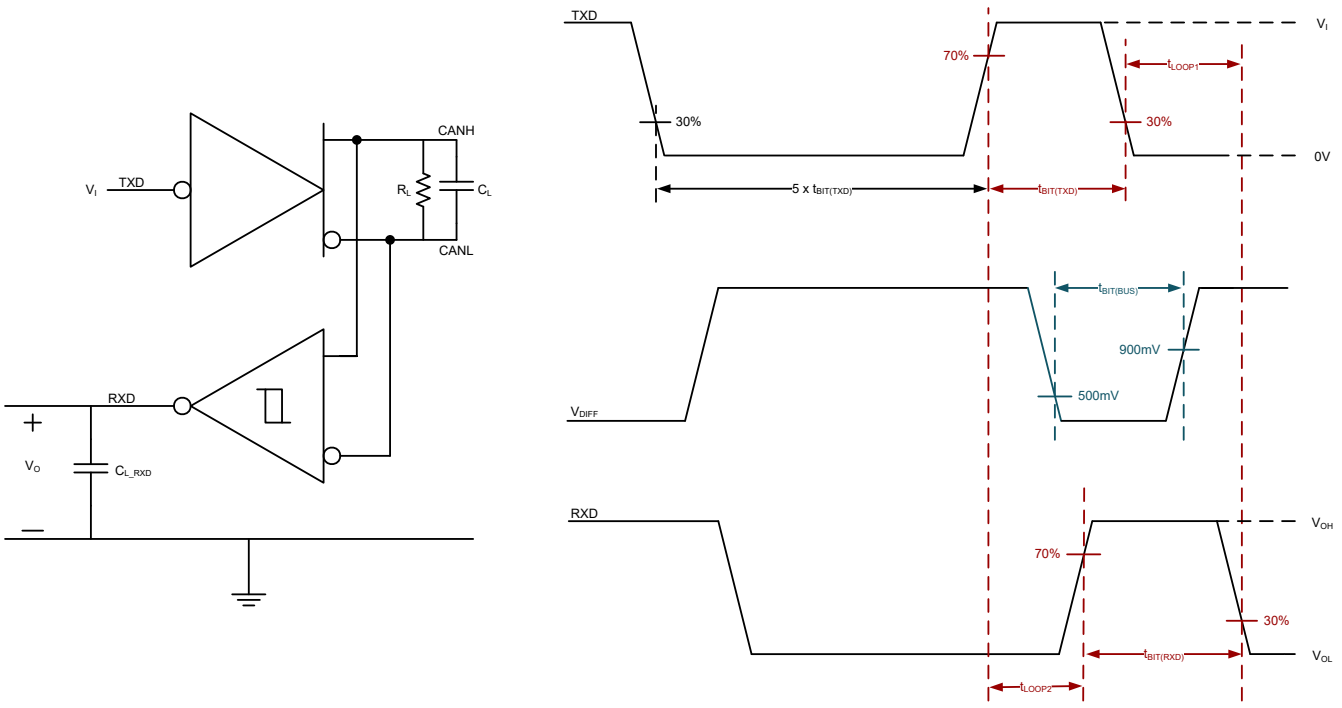

Figure 6-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

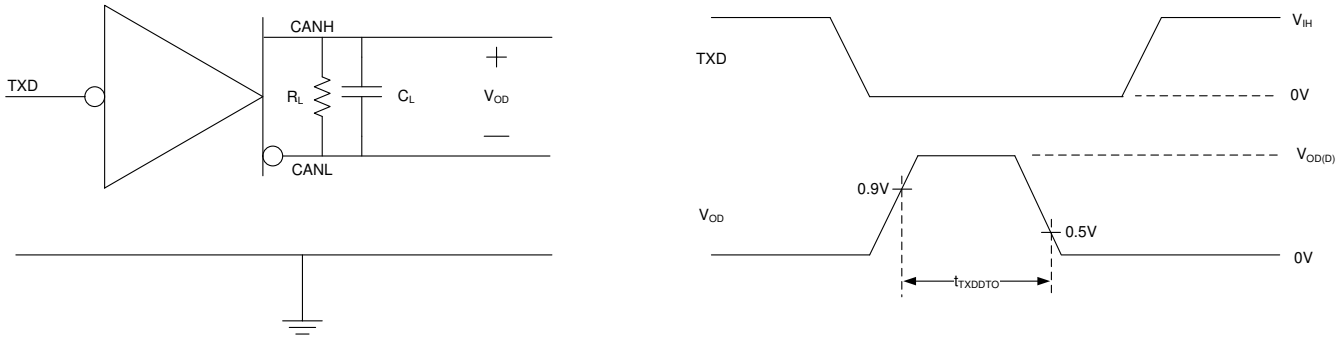

Figure 6-7. TXD Dominant Time Out Test Circuit and Measurement

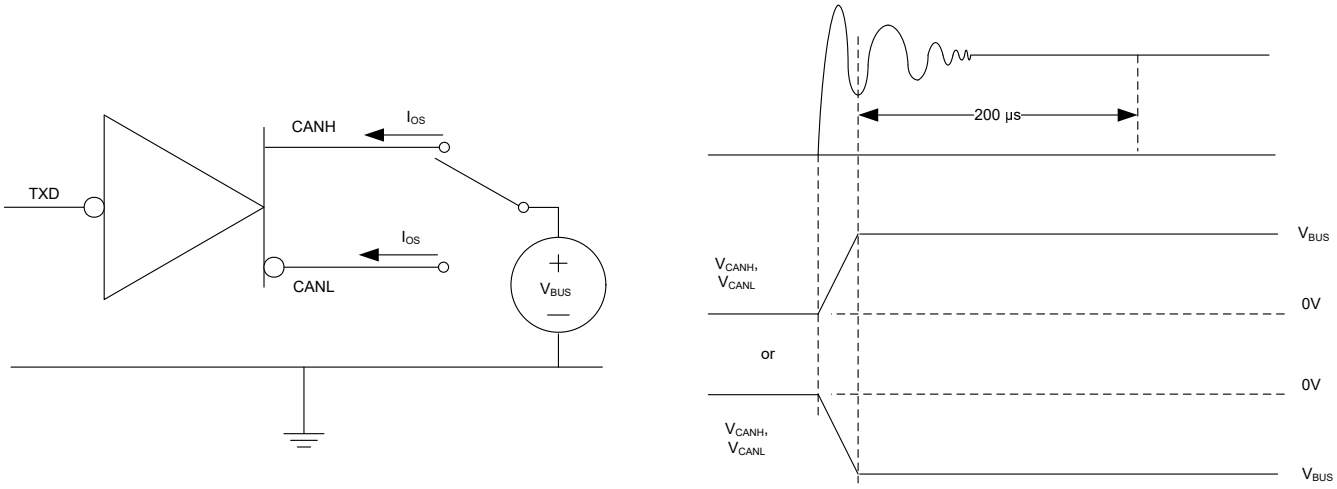

Figure 6-8. Driver Short-Circuit Current Test and Measurement

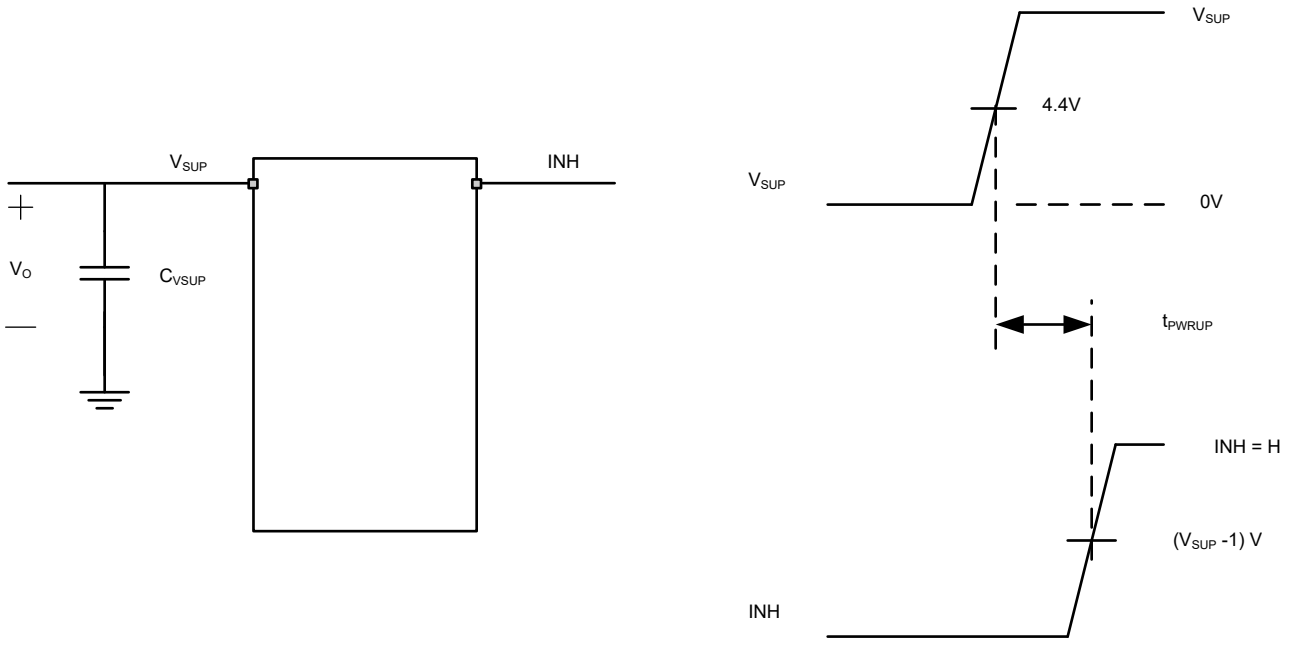

Figure 6-9. Power-Up Timing

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7 Detailed Description

7.1 Overview

The TCAN843-Q1 is a high-speed Controller Area Network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2024 high-speed CAN specification. The TCAN843-Q1 supports both classical CAN and CAN FD networks up to 5 megabits per second (Mbps).

The TCAN843-Q1 supports at least the following CAN and CAN FD standards:

- Physical layer:
  - ISO 11898-2:2024 – High-speed physical medium attachment (PMA) sublayer
  - SAE J2284-1 – High Speed CAN (HSC) for Vehicle Applications at 125kbps
  - SAE J2284-2 – High Speed CAN (HSC) for Vehicle Applications at 250kbps
  - SAE J2284-3 – High Speed CAN (HSC) for Vehicle Applications at 500kbps
  - SAE J2284-4 – High Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 2Mbps
  - SAE J2284-5 – High Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 5Mbps
- Conformance test requirements
  - ISO 16845-2:2018 – High-speed medium access unit – Conformance test plan
  - IOPT.CAN – Interoperability test specification for high-speed CAN transceiver or equivalent devices

The transceiver has three separate supply inputs, V_{SUP}, V_{CC}, and V_{IO}. By using V_{IO}, the TCAN843-Q1 can interface directly to a 3.3V, or 5V controller without the need for a level shifter. The TCAN843-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present in the system via the INH output pin. This enables a low-current sleep state in which power is gated to all system components except for the TCAN843-Q1, which remains in a low-power state while monitoring the CAN bus. When a wake-up pattern is detected on the bus or when a local wake up is requested via the WAKE input, the device initiates node start-up by driving INH high.

The TCAN843-Q1 includes many protection and diagnostic features including undervoltage detection, CAN bus fault detection, battery connection detection, thermal shutdown (TSD), driver dominant timeout (TXD DTO), and bus fault protection up to ±40V.

7.2 Functional Block Diagram

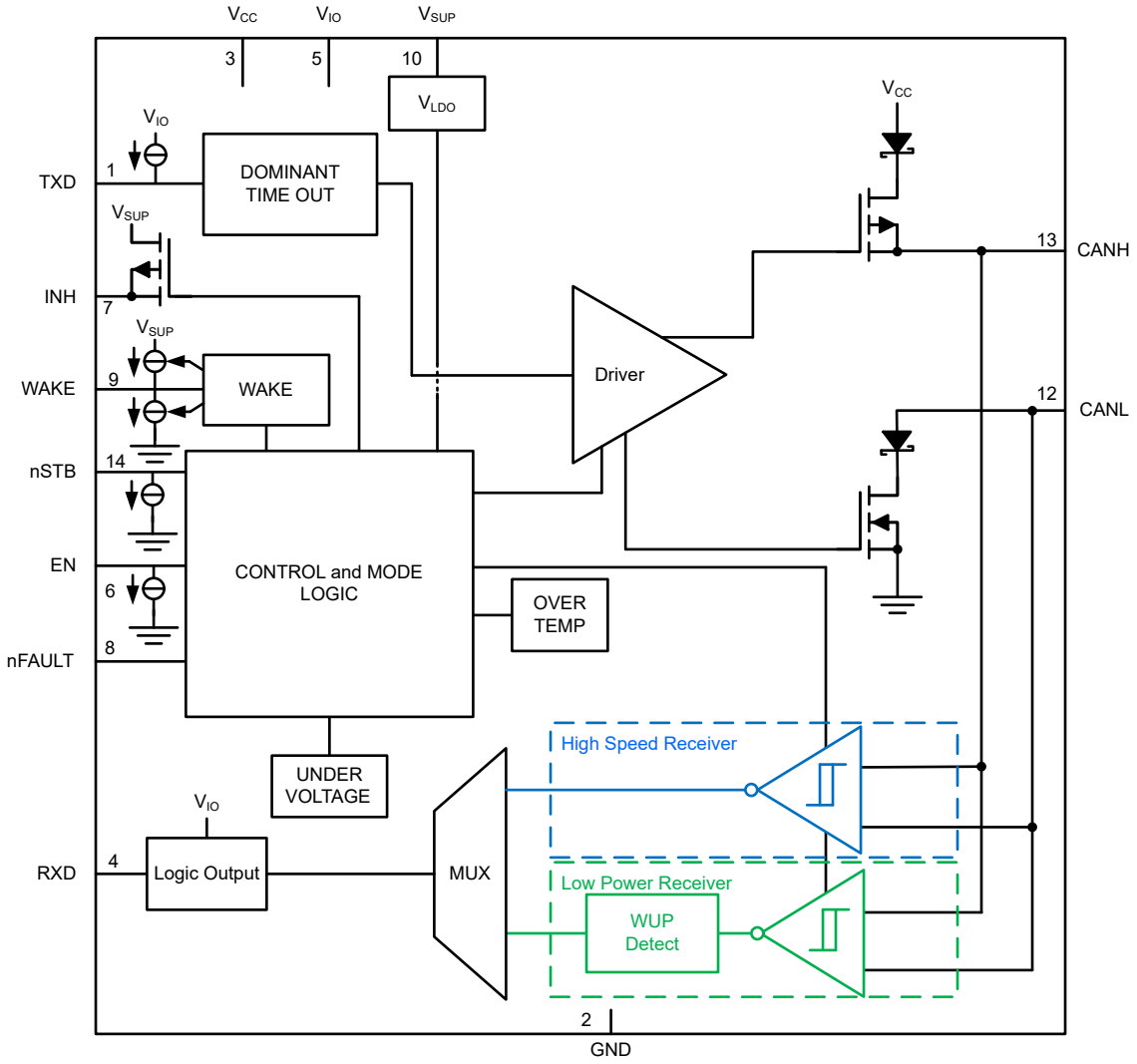

Figure 7-1. TCAN843-Q1 Functional Block Diagram

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7.3 Feature Description

7.3.1 Supply Pins

The TCAN843-Q1 implements three independent supply inputs for regulating different portions of the device.

7.3.1.1 V_{SUP} Pin

This pin is connected to the battery supply. The pin provides the supply to the internal regulators that support the digital core and the low power CAN receiver.

7.3.1.2 V_{CC} Pin

This pin provides the 5V supply voltage for the CAN transceiver.

7.3.1.3 V_{IO} Pin

This pin provides the digital I/O voltage to match the CAN FD controller's I/O voltage. The pin supports I/O voltages from 2.9V to 5.5V providing a wide range of controller support.

7.3.2 Digital Inputs and Outputs

7.3.2.1 TXD Pin

TXD is a logic-level input signal, referenced to V_{IO}, from a CAN FD controller to the TCAN843-Q1. TXD is biased to the V_{IO} level to force a recessive input in case the pin floats.

7.3.2.2 RXD Pin

RXD is a logic-level signal output, referenced to V_{IO}, from the TCAN843-Q1 to a CAN FD controller. The RXD pin is driven to the V_{IO} level as logic-high outputs once a valid V_{IO} is present.

When a power-on or wake-up event takes place, the RXD pin is pulled low.

7.3.2.3 nFAULT Pin

nFAULT is a logic-level output signal, referenced to V_{IO}, from the TCAN843-Q1 to a CAN FD controller. The nFAULT output is driven to the V_{IO} level as logic-high output.

The nFAULT output is used to transmit the TCAN843-Q1 status indicator flags to the CAN FD controller. Please see Table 7-1 for the specific fault scenarios that are indicated externally via the nFAULT pin. The TCAN843-Q1 drives the nFAULT pin high when VIO is present and in the Sleep mode to conserve power because there are no fault scenarios that are indicated externally in the Sleep mode.

7.3.2.4 EN Pin

EN is a logic-level input signal, referenced to V_{IO}, from a CAN FD controller to the TCAN843-Q1. The EN input pin is for mode selection in conjunction with the nSTB pin. EN is internally pulled low to prevent excessive system power and false wake-up events.

7.3.2.5 nSTB Pin

nSTB is a logic-level input signal, referenced to V_{IO}, from a CAN FD controller to the TCAN843-Q1. The nSTB input pin is for mode selection in conjunction with the EN pin. nSTB is internally pulled low to prevent excessive system power and false wake-up events.

7.3.3 GND

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

7.3.4 INH Pin

The INH pin is a high-voltage output. It can be used to control external regulators. These regulators are usually used to support the microprocessor and V_{IO} pin. The INH function is on in all modes except for sleep mode. In sleep mode, the INH pin is turned off, going into a high-impedance state. This allows the node to be placed into the lowest power state while in sleep mode. A 100kΩ load can be added to the INH output for a fast transition time from the driven high state to the low state and to force the pin low when left floating.

This terminal should be considered a high-voltage logic terminal, not a power output. The INH pin should be used to drive the EN terminal of the system power management device, and should not be used as a switch for the power management supply. This terminal is not reverse-battery protected; thus, should not be connected outside the system module.

7.3.5 WAKE Pin

The WAKE pin is a high-voltage reverse-blocked input used for the local wake-up (LWU) function. The WAKE pin is bi-directional edge-triggered and recognizes a local wake-up (LWU) on either a rising or falling edge of WAKE pin transition. The LWU function is explained further in the Local Wake-Up (LWU) via WAKE Input Terminal section.

7.3.6 CAN Bus Pins

These are the CAN high and CAN low, CANH and CANL, differential bus pins. These pins are internally connected to the CAN transceiver and the low-voltage wake receiver.

7.3.7 Faults

7.3.7.1 Internal and External Fault Indicators

The following device status indicator flags are implemented to allow for the MCU to determine the status of the device and the system. In addition to faults, the nFAULT terminal also signals wake-up requests and a “cold” power-up sequence on the V_{SUP} battery terminal so the system can do any diagnostics or cold booting sequence necessary. The RXD terminal indicates wake-up request and the faults are multiplexed (ORed) to the nFAULT output.

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Table 7-1. TCAN843-Q1 Transceiver Status Indicator

EVENT	FLAG NAME	CAUSE	INDICATORS(1)	FLAG IS CLEARED	COMMENT
Power-up	*PWRON*	Power up on V_{SUP} and any return of V_{SUP} after it has been below UV_{SUP}	nFAULT = low upon entering silent mode from standby or sleep mode	After a transition to normal mode	A cold start condition generates a local wake-up WAKERQ, *WAKESR* and a PWRON flag.
Wake-up Request	*WAKERQ* (2)	Wake-up event on CAN bus, state transition on WAKE pin, or initial power up	nFAULT = RXD = low after wake-up upon entering standby mode	After a transition to normal mode or $V_{CC} < UV_{CC(F)}$ or $V_{IO} < UV_{IO(F)}$ for $t \geq t_{UV}$	Wake-up request may only be set from standby, go-to-sleep, or sleep mode. Resets expired timers for UV_{VCC} or UV_{VIO} in sleep mode.
Wake-up Source Recognition(3)	*WAKESR*		Available upon entering normal mode(4) nFAULT = low indicates a local wake-up event from the WAKE pin nFAULT = high indicates a remote wake-up event from the CAN bus	After four recessive-to-dominant edges on TXD in normal mode,(5) leaving normal mode, or $V_{CC} < UV_{CC(F)}$ or $V_{IO} < UV_{IO(F)}$ for $t \geq t_{UV}$	A cold start condition generates a local wake-up WAKERQ, *WAKESR* and a PWRON flag.
Undervoltage	UV_{CC}	$V_{CC} < UV_{CC(F)}$	Not externally indicated	$V_{CC} > UV_{CC(R)}$, or a wake-up request occurs	
	UV_{IO}	$V_{IO} < UV_{IO(F)}$	Not externally indicated	$V_{IO} > UV_{IO(R)}$, or a wake-up request occurs	
	UV_{SUP}	$V_{SUP} < UV_{SUP(F)}$	Not externally indicated	$V_{SUP} > UV_{SUP(R)}$	A V_{SUP} undervoltage event generates a cold start condition once $V_{SUP} > UV_{SUP(R)}$.
Local Faults	*TXDDTO*	TXD dominant time out, dominant (low) signal for $t \geq t_{TXDDTO}$	nFAULT = low upon entering silent mode from normal mode	RXD = low and TXD = high for 4µs, or a mode transition into normal, standby, go-to-sleep, or sleep modes	CAN driver remains disabled until the *TXDDTO* is cleared. CAN receiver remains active during the *TXDDTO* fault.
	TXDRXD	TXD and RXD pins are shorted together for $t \geq t_{TXDDTO}$			CAN driver remains disabled until the *TXDRXD* is cleared. CAN receiver remains active during the *TXDRXD* fault. *TXDRXD* is detected while TXD = RXD = low.
	CANDOM	CAN bus dominant fault, when dominant bus signal received for $t \geq t_{BUSDOM}$		RXD = high, or a transition into normal, standby, go-to-sleep, or sleep modes	CAN driver remains enabled during *CANDOM* fault.
	TSD	Thermal shutdown, $T_J \geq T_{SDR}$		$T_J < T_{SDF}$ and RXD = low and TXD = high for 4µs, or transition into normal, standby, go-to-sleep, or sleep modes	CAN driver remains disabled until the *TSD* event is cleared. CAN receiver remains active during the *TSD* fault.

(1) V_{IO} and V_{SUP} are present
(2) Transitions to go-to-sleep mode is blocked until WAKERQ flag is cleared
(3) Wake-up source recognition reflects the first wake up source. If additional wake-up events occur the source still indicates the original wake-up source
(4) Indicator is only available in normal mode until the flag is cleared
(5) A minimum of 4µs between recessive-to-dominant edges is required to clear the WAKESR flag

7.3.7.1.1 Power-Up (PWRON Flag)

This is an internal and external flag that can be used to control the power-up sequence of the system. When a new battery connection to the transceiver is made the *PWRON* flag is set signifying a cold start condition. The TCAN843-Q1 treats any undervoltage conditions on the V_{SUP}, $V_{SUP} < UV_{SUP(F)}$, as a cold start. Therefore, when the $V_{SUP} > UV_{SUP(R)}$ condition is met the TCAN843-Q1 sets the *PWRON* flag which can be used by the system to enter a routine that is only called upon in cold start situations. The *PWRON* flag is indicated by nFAULT driven low after entering silent mode from either standby mode or sleep mode. This flag is cleared after a transition to normal mode.

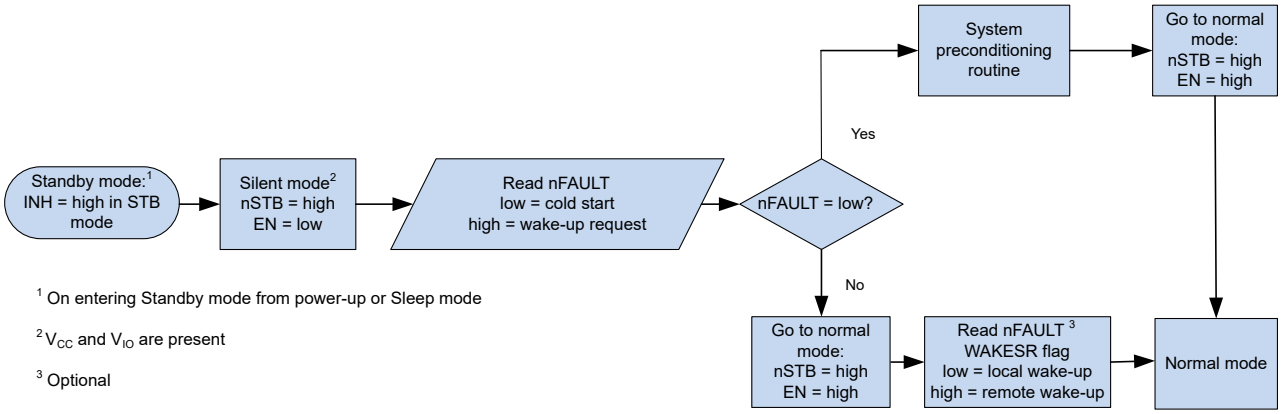

Figure 7-2. Distinguishing between *PWRON* and Wake Request by Entering Silent Mode

7.3.7.1.2 Wake-Up Request (WAKERQ Flag)

This is an internal and external flag that can be set in standby, go-to-sleep, or sleep mode. This flag is set when either a valid local wake-up (LWU) request occurs, or a valid remote wake request occurs, or on power up on V_{SUP}. The setting of this flag clears the t_{UV} timer for the UV_{CC} or UV_{IO} fault detection. This flag is cleared upon entering normal mode or during an undervoltage event on V_{CC} or V_{IO}.

7.3.7.1.3 Undervoltage Faults

The TCAN843-Q1 device implements undervoltage detection circuits on all supply terminals: V_{SUP}, V_{CC}, and V_{IO}. The undervoltage flags are internal indicator flags and are not indicated on the nFAULT output pin.

7.3.7.1.3.1 Undervoltage on V_{SUP}

UV_{SUP} is set when the voltage on V_{SUP} drops below the undervoltage detection voltage threshold, UV_{SUP}. The PWRON and WAKERQ flags are set once $V_{SUP} > UV_{SUP(R)}$.

7.3.7.1.3.2 Undervoltage on V_{CC}

UV_{CC} is set when the voltage on V_{CC} drops below the undervoltage detection voltage threshold, UV_{CC}, for longer than the t_{UV} undervoltage filter time.

7.3.7.1.3.3 Undervoltage on V_{IO}

UV_{IO} is set when the voltage on V_{IO} drops below the undervoltage detection voltage threshold, UV_{IO}, for longer than the t_{UV} undervoltage filter time.

7.3.7.1.4 TXD Dominant State Timeout (TXDDTO Flag)

TXDDTO is an external flag that is set if the TXD pin is held dominant for $t > t_{TXDDTO}$. If a TXD DTO condition exists, the nFAULT pin is driven low upon entering silent mode from normal mode. The TXDDTO flag is cleared when TXD = H and RXD = L in normal mode or upon a transition into normal, standby, go-to-sleep, or sleep modes.

7.3.7.1.5 TXD Shorted to RXD Fault (TXDRXD Flag)

TXDRXD is an external flag that is set if the transceiver detects that the TXD and RXD lines have been shorted together for $t \geq t_{TXDDTO}$. If a TXDRXD condition exists, the nFAULT pin is driven low upon entering silent mode from normal mode and the CAN bus driver is disabled until the TXDRXD fault is cleared. The TXDRXD flag is cleared on the next dominant-to-recessive transition with TXD high and RXD low or upon a transition into normal, standby, go-to-sleep, or sleep modes.

7.3.7.1.6 CAN Bus Dominant Fault (CANDOM Flag)

CANDOM is an external flag that is set if the CAN bus is stuck dominant state for $t > t_{BUSDOM}$. If a CANDOM condition exists, the nFAULT pin is driven low upon entering silent mode from normal mode. The CANDOM

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flag is cleared on the next dominant-to-recessive transition on RXD or upon a transition into normal, standby, go-to-sleep, or sleep modes.

7.3.8 Local Faults

Local faults are detected in both normal mode and silent mode, but are only indicated via the nFAULT pin when the TCAN843-Q1 transitions from normal mode to silent mode. All other mode transitions clear the local fault flag indicators.

7.3.8.1 Thermal Shutdown (*TSD*)

If the junction temperature of the TCAN843-Q1 exceeds the thermal shutdown threshold the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The CAN bus terminals are biased to recessive level during a *TSD* fault and the receiver to RXD path remains operational. The *TSD* fault condition is cleared when the junction temperature, T_J, of the device drops below the thermal shutdown release temperature, T_{SDF}, of the device and a mode change into Normal, standby, or sleep mode is done or a TXD = H & RXD = L is received. If the fault condition that caused the *TSD* fault is still present, the temperature can rise again, and the device enters thermal shutdown again. Prolonged operation with *TSD* fault conditions may affect device reliability. The TSD circuit includes hysteresis to avoid any oscillation of the driver output. During the fault the *TSD* fault condition is indicated to the CAN FD controller via the nFAULT terminal.

7.3.8.2 Undervoltage Lockout (UVLO)

The supply terminals, V_{SUP}, V_{IO} and V_{CC}, are monitored for undervoltage events. If an undervoltage event occurs the TCAN843-Q1 enters a protected state where the bus pins present no load to the CAN bus. This protects the CAN bus and system from unwanted glitches and excessive current draw that could impact communication between other CAN nodes on the CAN bus.

If an undervoltage event occurs on V_{SUP} in any mode, the TCAN843-Q1 CAN transceiver enters the CAN off state.

If an undervoltage event occurs on $V_{CC,}$ the TCAN843-Q1 remains in normal or silent mode but the CAN transceiver changes to the CAN passive state. During a UV_{CC} event, RXD remains high as long as V_{IO} is present and the wake-up circuitry is inactive. The CAN bus is weakly biased to GND. If the undervoltage event persists longer than t_{UV}, the TCAN843-Q1 transitions to sleep mode.

If an undervoltage event occurs on the V_{IO}, the TCAN843-Q1 transitions to standby mode. If the undervoltage event persists longer than t_{UV}, the TCAN843-Q1 transitions to sleep mode.

Once an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically needs 200µs to transition to normal operation.

7.3.8.3 Unpowered Devices

The device is designed to be high-impedance to the CAN bus if it is unpowered. The CANH and CANL pins have low leakage currents when the device is unpowered, so no load is present on the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

The logic terminals also have low leakage currents when the device is unpowered, so there is not a load down other circuits which may remain powered.

7.3.8.4 Floating Terminals

The TCAN843-Q1 has internal pull-ups and pull-downs on critical pins to make sure a known operating behavior if the pins are left floating. See Table 7-2 for the pin fail-safe biasing protection description.

Table 7-2. Pin Fail-safe Biasing

PIN	FAIL-SAFE PROTECTION	VALUE	COMMENT
TXD	Recessive level	60kΩ	Weak pull-up to V_{IO}
EN	Low-power mode		Weak pull-down to GND
nSTB	Low-power mode		Weak pull-down to GND

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This internal bias should not be relied upon by design but rather a fail-safe option. Special care needs to be taken when the transceiver is used with a CAN FD controller that has open-drain outputs. The TCAN843-Q1 implements a weak internal pull-up resistor on the TXD pin. The bit timing requirements for CAN FD data rates require special consideration and the pull-up strength should be considered carefully when using open-drain outputs. An adequate external pull-up resistor must be used to make sure the TXD output of the CAN FD controller maintains proper bit timing input to the CAN device.

7.3.8.5 CAN Bus Short-Circuit Current Limiting

The TCAN843-Q1 has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault.

During CAN communication the bus switches between the dominant and recessive states, thus the short-circuit current may be viewed either as the current during each bus state or as an average current. The average short-circuit current should be used when considering system power for the termination resistors and common-mode choke. The percentage of time that the driver can be dominant is limited by the TXD dominant state timeout and the CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and interframe spacing. These makes sure there is a minimum recessive time on the bus even if the data field contains a high percentage of dominant bits.

The short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using Equation 1.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}] \quad (1)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short-circuit current

The short-circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance and other network components.

7.4 Device Functional Modes

The TCAN843-Q1 has six operating modes: normal, standby, silent, go-to-sleep, sleep, and off mode. Operating mode selection is controlled using the nSTB pin and EN pin in conjunction with supply conditions, temperature conditions, and wake events.

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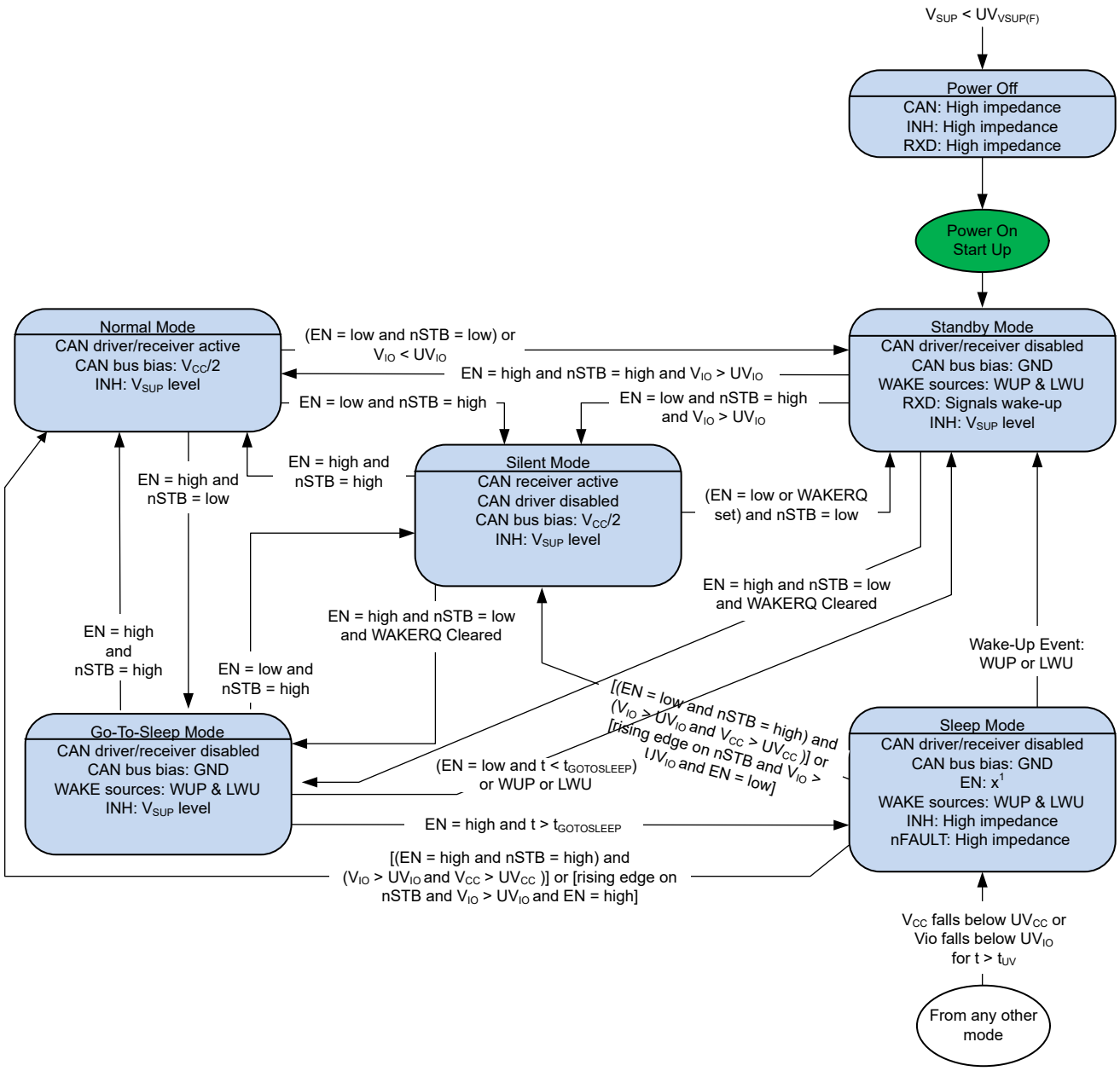

1. The enable pin can be in a logical high or low state while in sleep mode but since it has an internal pull-down, the lowest possible power consumption occurs when the pin is left either floating or pulled low externally.

Figure 7-3. TCAN843-Q1 State Machine

Table 7-3. TCAN843-Q1 Mode Overview

MODE	V_{CC} and V_{IO}	V_{SUP}	EN	nSTB	WAKERQ FLAG	DRIVER	RECEIVER	RXD	INH
Normal	> UV_{CC} and > UV_{IO}	> UV_{SUP}	High	High	X	Enabled	Enabled	Mirrors bus state	On
Silent	> UV_{CC} and > UV_{IO}	> UV_{SUP}	Low	High	X	Disabled	Enabled	Mirrors bus state	On
Standby	> UV_{CC} and > UV_{IO}	> UV_{SUP}	High	Low	Set	Disabled	Low power bus monitor enabled	Low signals wake-up	On
	> UV_{CC} and > UV_{IO}	> UV_{SUP}	Low	Low	X	Disabled	Low power bus monitor enabled	Low signals wake-up	On
	> UV_{CC} and < UV_{IO}	> UV_{SUP}	Low	Low	X	Disabled	Low power bus monitor enabled	High impedance	On
Go-to-sleep(1)	> UV_{CC} and > UV_{IO}	> UV_{SUP}	High	Low	Cleared	Disabled	Low power bus monitor enabled	High or high impedance (no V_{IO})	On(2)

Table 7-3. TCAN843-Q1 Mode Overview (continued)

MODE	V_{CC} and V_{IO}	V_{SUP}	EN	nSTB	WAKERQ FLAG	DRIVER	RECEIVER	RXD	INH
Sleep[3]	> UV_{CC} and > UV_{IO}	> UV_{SUP}	High	Low	Cleared	Disabled	Low power bus monitor enabled	High or high impedance (no V_{IO})	High Impedance
	< UV_{CC} or < UV_{IO}	> UV_{SUP}	X	X	X	Disabled	Low power bus monitor enabled	High or high impedance (no V_{IO})	High impedance
Passive[4]	< UV_{CC} and > UV_{IO}	> UV_{SUP}	X	High	X	Disabled	Disabled	High	On
Protected	X	< UV_{SUP}	X	X	X	Disabled	Disabled	High impedance	High impedance

(1) Go-to-sleep: Transitional mode for EN = H, nSTB = L until $t_{GOTOSLEEP}$ timer has expired. The low-power bus monitor becomes/remains enabled in this state.
(2) The INH pin transitions to high impedance once the $t_{GOTOSLEEP}$ timer has expired and the device transitions to Sleep mode.
(3) Mode change from Go-to-Sleep mode to Sleep mode once $t_{GOTOSLEEP}$ timer has expired.
(4) Passive mode is entered from Normal mode or Silent mode when a UV_{CC} event occurs for t > t_{UV_det}. The device transitions from Passive mode to Sleep mode once the t_{UV} timer has expired.

7.4.1 Operating Mode Description

7.4.1.1 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

Entering normal mode clears both the WAKERQ and the PWRON flags. If Normal mode is entered while TXD is low, the driver is not enabled until TXD becomes high, preventing glitches during state transitions or bus interruptions due to TXD faults.

7.4.1.2 Silent Mode

Silent mode is commonly referred to as listen only and receive only mode. In this mode, the CAN driver is disabled but the receiver is fully operational and CAN communication is unidirectional into the device. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD terminal.

In silent mode, PWRON and Local Failure flags are indicated on the nFAULT pin.

7.4.1.3 Standby Mode

Standby mode is a low-power mode where the driver and receiver are disabled, reducing current consumption. However, this is not the lowest power mode of the device since the INH terminal is on, allowing the rest of the system to resume normal operation.

During standby mode, a wake-up request (*WAKERQ*) is indicated by the RXD terminal being low. The wake-up source is identified via the nFAULT pin after the device is returned to normal mode.

7.4.1.4 Go-To-Sleep Mode

Go-to-sleep mode is the transitional mode of the device from any state to sleep. In this state, the driver and receiver are disabled, reducing the current consumption. The INH pin is active to supply an enable to the V_{IO} controller which allows the rest of the system to operate normally. Upon entering this mode, the low-power bus monitor activates or remains active to monitor for bus wake-up events. If the device is held in this state for t ≥ $t_{GOTOSLEEP}$, the device transitions to sleep mode and the INH turns off transitioning to the high impedance state.

If any wake-up events persist, the TCAN843-Q1 remains in standby mode until the device is switched into normal mode to clear the pending wake-up events.

7.4.1.5 Sleep Mode

Sleep mode is the lowest power mode of the TCAN843-Q1. In sleep mode, the CAN transmitter and the main receiver are switched off, and the transceiver cannot send or receive data. The low power receiver is able to monitor the bus for any activity that validates the wake-up pattern (WUP) requirements, and the WAKE monitoring circuit monitors for state changes on the WAKE terminal for a local wake-up (LWU) event. The INH

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pin is switched off in sleep mode causing any system power supplies controlled by INH to be switched off thus reducing system power consumption.

Sleep mode is exited:

- If a valid wake-up pattern (WUP) is received via the CAN bus pins
- On a local WAKE (LWU) event
- nSTB is high and VCC > UV_{CC} and VIO > UV_{IO} (the device enters Normal or Silent mode depending upon the logic level on the EN pin.

7.4.1.5.1 Remote Wake Request via Wake-Up Pattern (WUP)

The TCAN843-Q1 implements a low-power wake receiver in the standby and sleep mode that uses the multiple filtered dominant wake-up pattern (WUP) defined in the ISO11898-2:2016 standard.

The wake-up pattern (WUP) consists of a filtered dominant bus, then a filtered recessive bus time followed by a second filtered dominant bus time. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive. Other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant. Other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant, the bus monitor recognizes the WUP and drives the RXD terminal low, if a valid V_{IO} is present signaling to the controller the wake-up request. If a valid, V_{IO} is not present when the wake-up pattern is received, the transceiver drives the RXD output pin low once V_{IO} > UV_{IOR}.

The WUP consists of:

- A filtered dominant bus of at least $t_{WK(FILTER)}$ followed by
- A filtered recessive bus time of at least $t_{WK(FILTER)}$ followed by
- A second filtered dominant bus time of at least $t_{WK(FILTER)}$

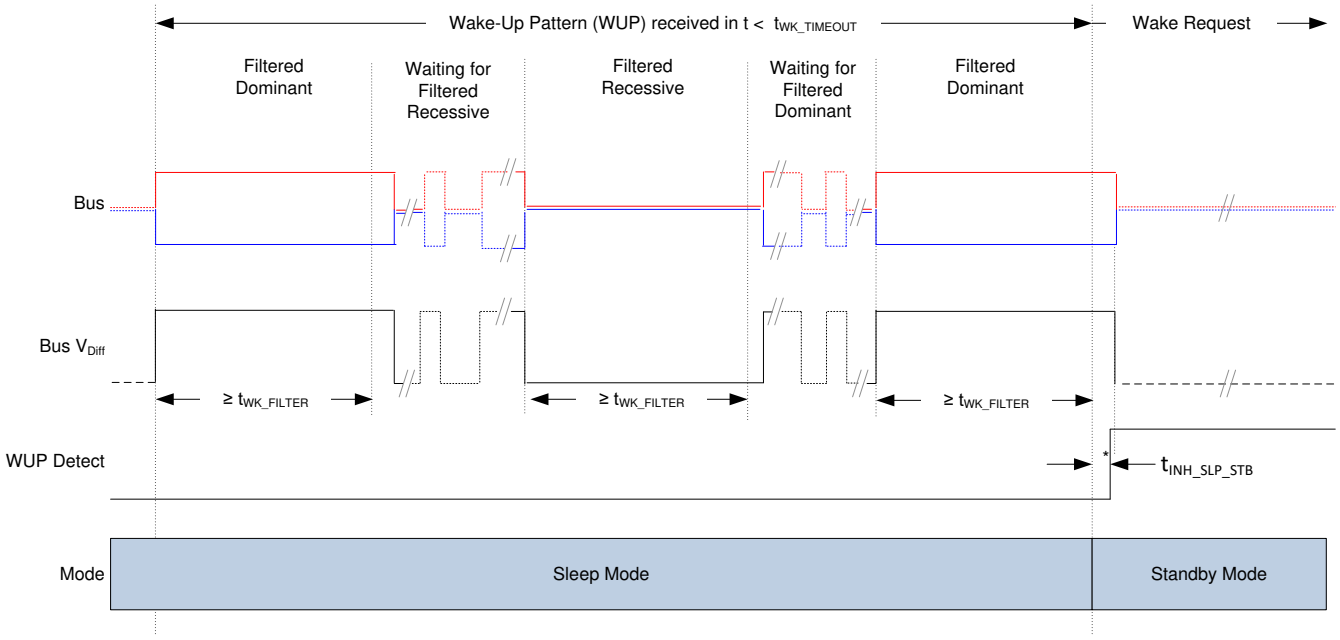
For a dominant or recessive to be considered “filtered,” the bus must be in that state for more than $t_{WK(FILTER)}$ time. Due to variability in the $t_{WK(FILTER)}$ the following scenarios are applicable. Bus state times less than the $t_{WK(FILTER)}$ minimum are never detected as part of a WUP, and thus, no wake request is generated. Bus state times between $t_{WK(FILTER)}$ minimum and $t_{WK(FILTER)}$ maximum may be detected as part of a WUP and a wake request may be generated. Bus state times more than $t_{WK(FILTER)}$ maximum is always detected as part of a WUP, and thus, a wake request is always generated. See Figure 7-4 for the timing diagram of the WUP.

The pattern and $t_{WK(FILTER)}$ time used for the WUP and wake request prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a wake request.

ISO11898-2:2024 has two sets of times for a short and long wake-up filter times. The $t_{WK(FILTER)}$ timing for the TCAN843-Q1 has been picked to be within the min and max values of both filter ranges. This timing has been chosen such that a single bit time at 500kbps, or two back to back bit times at 1Mbps trigger the filter in either bus state.

For an additional layer of robustness and to prevent false wake-ups, the transceiver implements the $t_{WK(TIMEOUT)}$ timer. For a remote wake-up event to successfully occur, the entire wake-up pattern must be received within the timeout value. If the full wake-up pattern is not received before the $t_{WK(TIMEOUT)}$ expires then the internal logic is reset and the transceiver remains in sleep mode without waking up. The full pattern must then be transmitted again within the $t_{WK(TIMEOUT)}$ window. See Figure 7-4.

A recessive bus of at least $t_{WK(FILTER)}$ must separate the next WUP pattern if the CAN bus is dominant when the $t_{WK(TIMEOUT)}$ expires.



*The RXD pin is only driven once V_{IO} is present.

Figure 7-4. Wake-Up Pattern (WUP)

7.4.1.5.2 Local Wake-Up (LWU) by WAKE Input Terminal

The WAKE terminal is a bi-directional high-voltage reverse-battery protected input which can be used for local wake-up (LWU) requests through a voltage transition. A LWU event is triggered on either a low-to-high or high-to-low transition due to the bi-directional input thresholds. The WAKE pin could be used with a switch to V_{SUP} or to ground. If the terminal is unused, the terminal should be pulled to V_{SUP} or ground to avoid unwanted parasitic wake-up events.

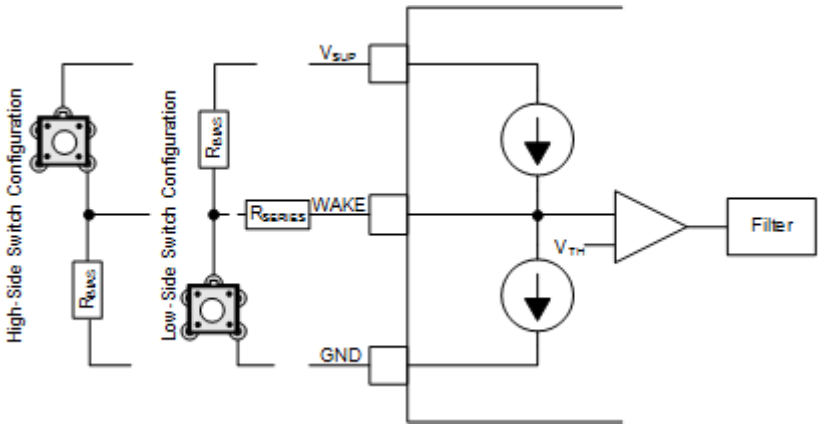


Figure 7-5. WAKE Circuit Example

Figure 7-5 shows two possible configurations for the WAKE pin, a low-side and high-side switch configuration. The objective of the series resistor, R_{SERIES}, is to protect the WAKE input of the device from over current conditions that may occur in the event of a ground shift or ground loss. The minimum value of R_{SERIES} can be calculated using the maximum supply voltage, V_{SUPMAX}, and the maximum allowable current of the WAKE pin, $I_{IO(WAKE)}$. R_{SERIES} is calculated using:

$$R_{SERIES} = V_{SUPMAX} / I_{IO(WAKE)} \quad (2)$$

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With absolute maximum voltage, V_{SUPMAX}, of 45V and maximum allowable $I_{IO(WAKE)}$ of 3mA, the minimum required R_{SERIES} value is 15kΩ.

The R_{BIAS} resistor is used to set the static voltage level of the WAKE input when the switch is released. When the switch is in use in a high-side switch configuration, the R_{BIAS} resistor in combination with the R_{SERIES} resistor sets the WAKE pin voltage above the V_{IH} threshold. The maximum value of R_{BIAS} can be calculated using the maximum supply voltage, V_{SUPMAX}, the maximum WAKE threshold voltage V_{IH}, the maximum WAKE input current I_{IH} and the series resistor value R_{SERIES}. R_{BIAS} is calculated using:

$$R_{BIAS} < ((V_{SUPMAX} - V_{IH}) / I_{IH}) - R_{SERIES} \quad (3)$$

With V_{SUPMAX} of 40V, V_{IH} of 39V at I_{IH} of 3µA, the R_{BIAS} resistor value must be less than 330kΩ. The recommendation is to use R_{Series} less than 50kΩ to provide better margin for the WAKE pin voltage to rise above V_{IH} when the switch is released.

The LWU circuitry is active in sleep and standby mode.

The WAKE circuitry is switched off in normal and silent mode.

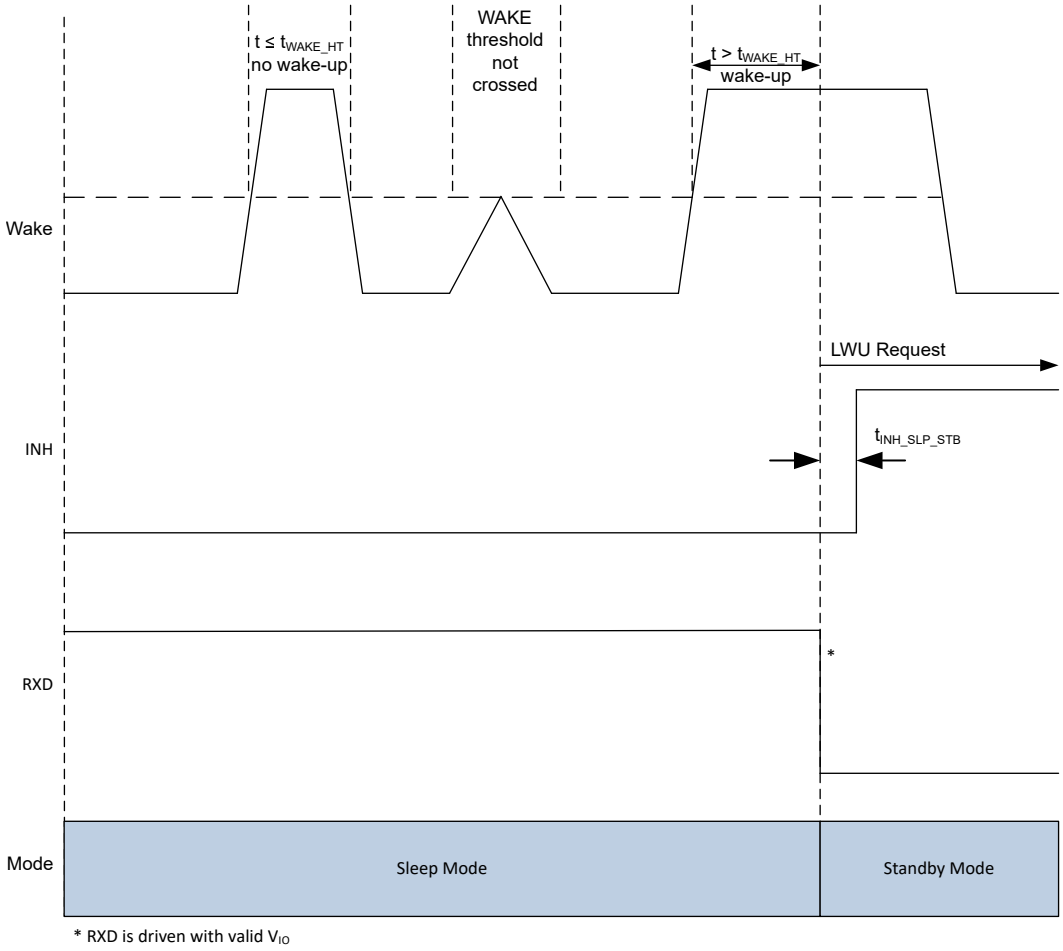

Figure 7-6. LWU Request Rising Edge

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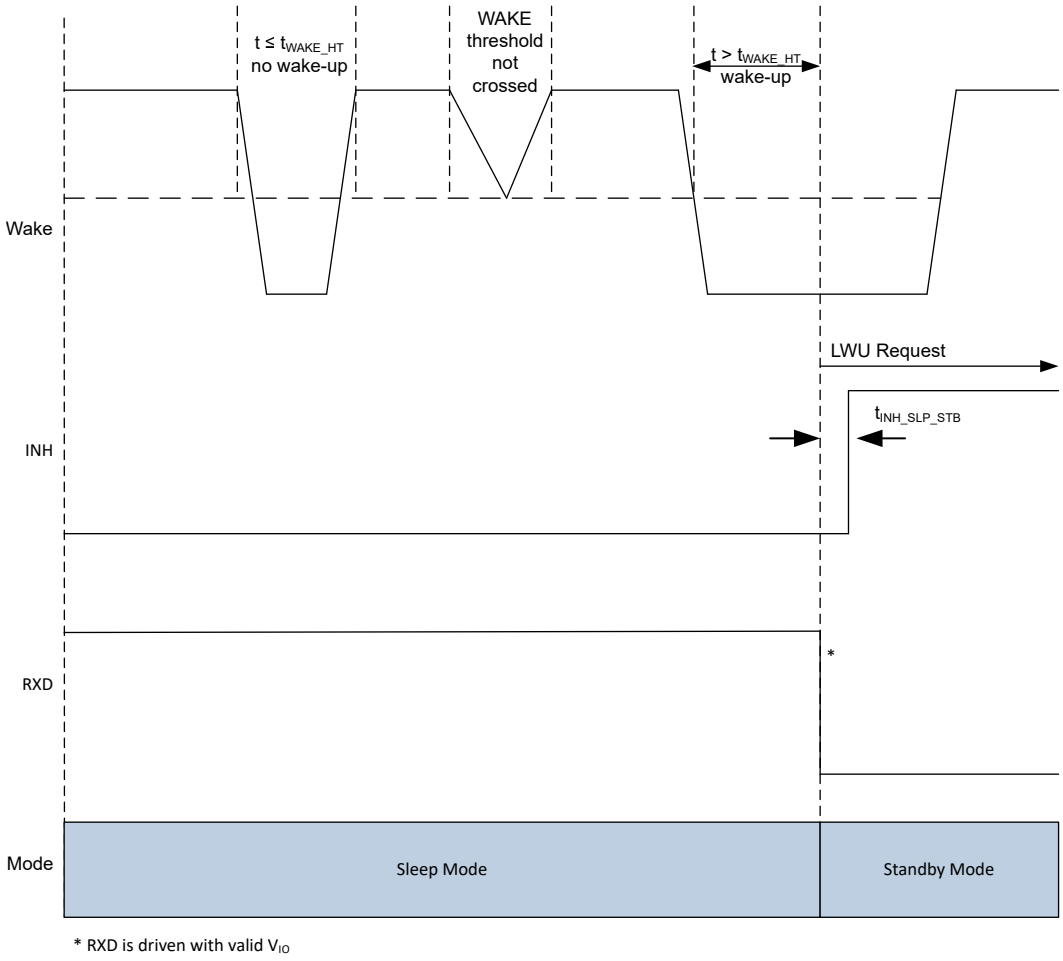

Figure 7-7. LWU Request Falling Edge

7.4.2 CAN Transceiver

7.4.2.1 CAN Transceiver Operation

The TCAN843-Q1 supports the ISO 11898-2:2024 CAN physical layer standard normal bus biasing scheme. Normal bus biasing means that the CAN bus is biased when the transceiver is in Normal mode or Silent mode. In other modes, the CAN pins are either high-impedance or weakly biased to GND.

7.4.2.1.1 Driver and Receiver Function Tables

Table 7-4. Driver Function Table

DEVICE MODE	TXD INPUTS(1)	BUS OUTPUTS		DRIVEN BUS STATE(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or Open	High impedance	High impedance	$V_{CC}/2$
Silent	x	High impedance	High impedance	$V_{CC}/2$
Standby	x	High impedance	High impedance	Weak bias to GND
Sleep	x	High impedance	High impedance	Weak bias to GND

(1) x = irrelevant
(2) For bus states and typical bus voltages see Figure 7-8

Table 7-5. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} – V_{CANL}$	BUS STATE	RXD TERMINAL
Normal / Silent	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Indeterminate	Indeterminate
	$V_{ID} \leq 0.5V$	Recessive	High
	Open ($V_{ID} \approx 0V$)	Open	High
Standby	$V_{ID} \geq 1.15V$	Dominant	High Low if wake-up event persists
	$0.4V < V_{ID} < 1.15V$	Indeterminate	
	$V_{ID} \leq 0.4$	Recessive	
	Open ($V_{ID} \approx 0V$)	Open	
Sleep / Go-to-sleep(1)	$V_{ID} \geq 1.15V$	Dominant	High Tri-state if V_{IO} or V_{SUP} are not present
	$0.4V < V_{ID} < 1.15V$	Indeterminate	
	$V_{ID} \leq 0.4V$	Recessive	
	Open ($V_{ID} \approx 0V$)	Open	

(1) Low power wake-up receiver is active

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7.4.2.1.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 7-8.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to one half of the CAN transceiver supply voltage via the high resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the CAN bus is greater than the differential voltage of a single CAN driver. The TCAN843-Q1 CAN transceiver implements low-power standby modes which enable a third bus state where the bus pins are biased to ground via the high-resistance internal resistors of the receiver.

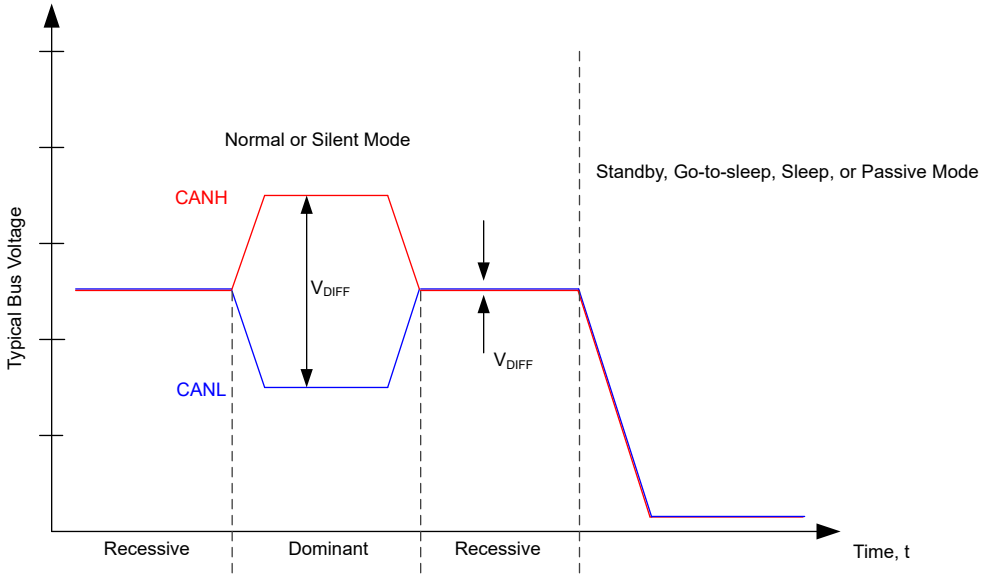

Figure 7-8. Bus States

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8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TCAN843-Q1 transceiver is typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. These types of applications usually also include power management technology that allows for power to be gated to the application via an enable (EN) or inhibit (INH) pin. A single 5V regulator can be used to drive both V_{CC} and V_{IO}, or independent 5V and 3.3V regulators can be used to drive V_{CC} and V_{IO} separately as shown in Figure 8-1. The bus termination is shown for illustrative purposes.

8.1.1 Typical Application

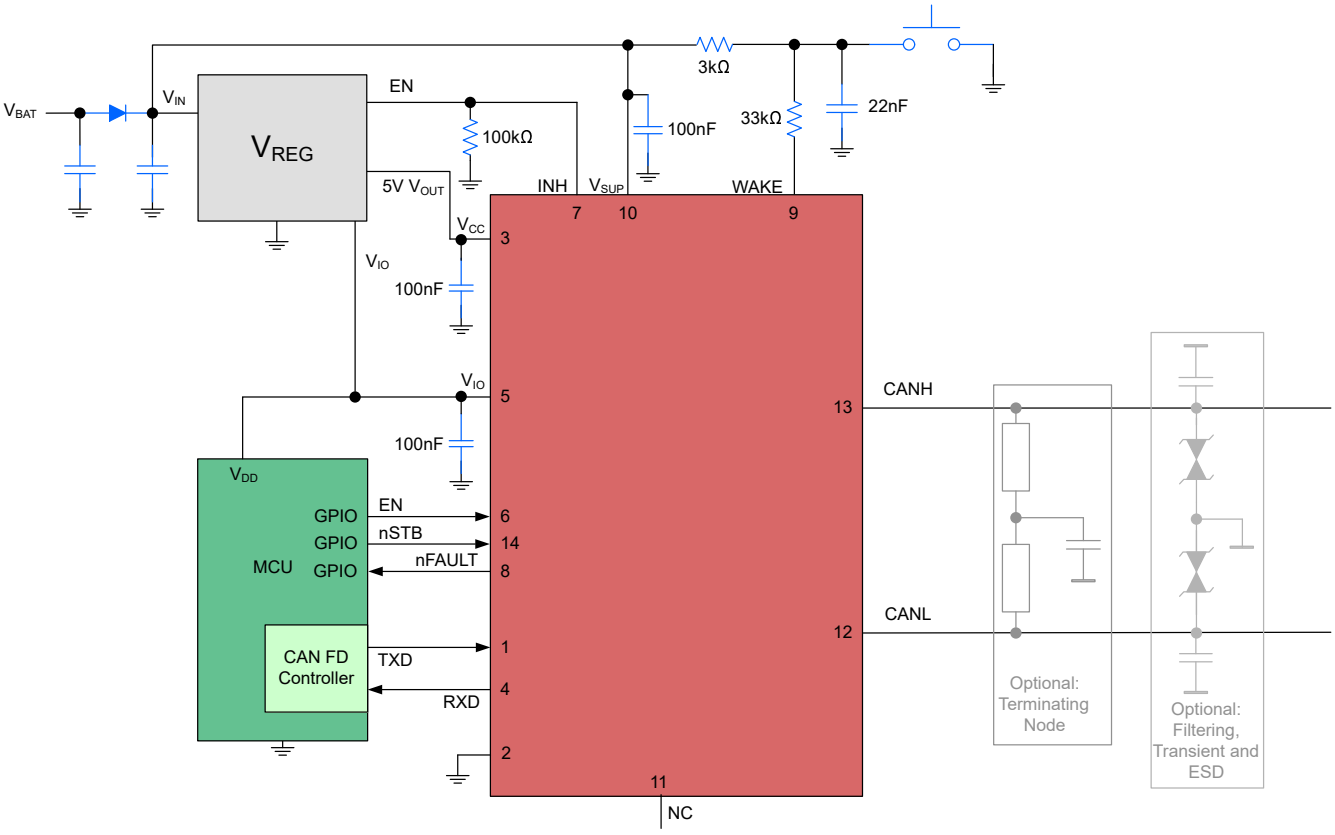

Figure 8-1. Typical Application

8.1.2 Design Requirements

8.1.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN843-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898-2:2024 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAEJ2284, SAEJ1939, and NMEA200.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2024 specification the differential output driver is specified with a bus load that can range from 50Ω to 65Ω where the differential output must be greater than 1.5V. The TCAN843-Q1 is specified to meet the 1.5V requirement down to 50Ω and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance, R_{ID}, of the TCAN843-Q1 is a minimum of 50kΩ. If 100 TCAN843-Q1 transceivers are in parallel on a bus, this is equivalent to a 500Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 54Ω. Therefore, the TCAN843-Q1 theoretically supports over 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of its key strengths allowing for these system level network extensions and additional standards to build on the original ISO11898-2 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design for a robust network operation.

8.1.3 Detailed Design Procedure

8.1.3.1 CAN Termination

Termination may be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see Figure 8-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

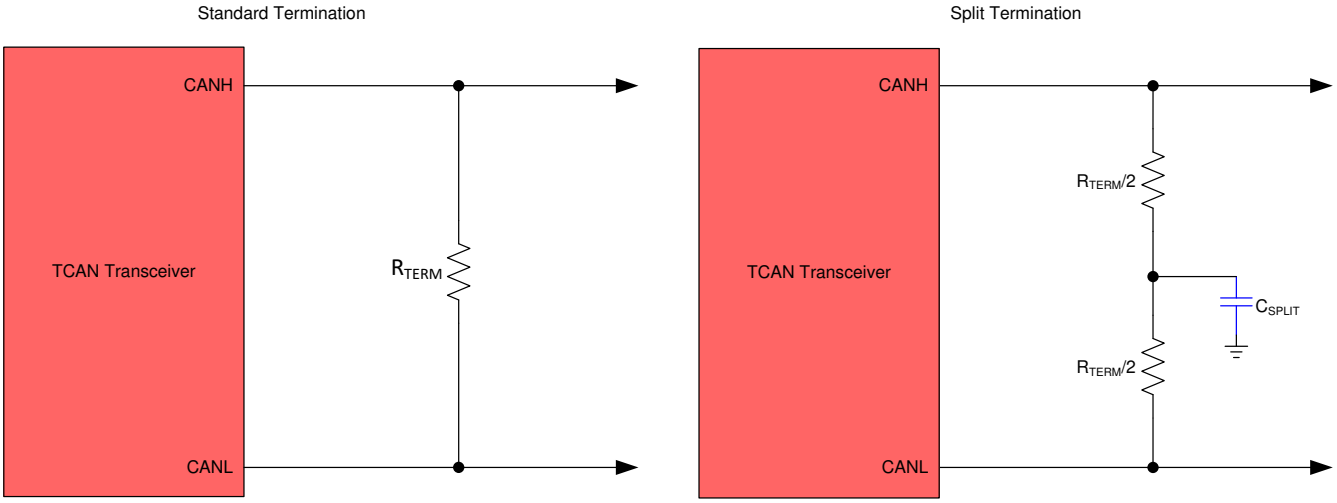

Figure 8-2. CAN Bus Termination Concepts

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8.1.4 Application Curves

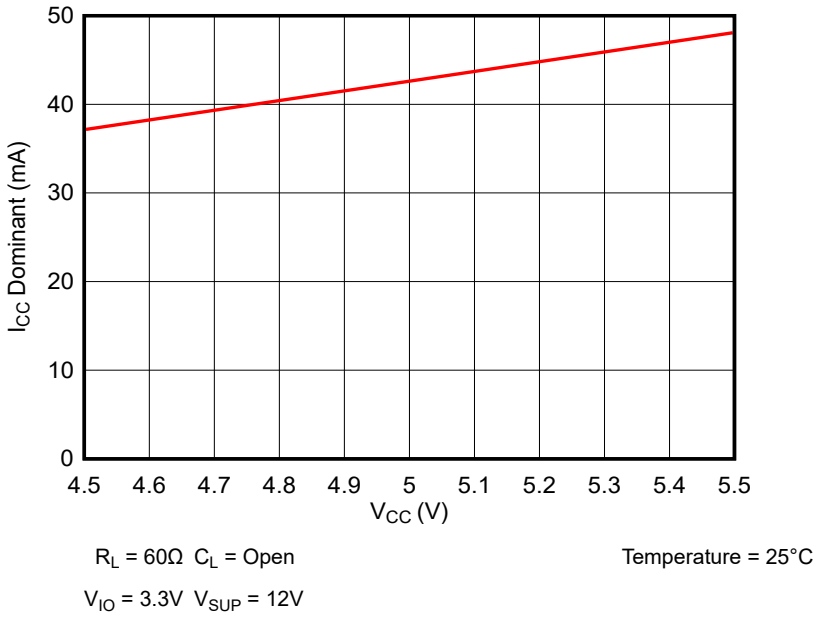

Figure 8-3. I_{CC} Dominant over I_{CC} Supply Voltage

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8.2 Power Supply Recommendations

The TCAN843-Q1 is designed to operate off of three supply rails; V_{SUP}, V_{CC}, and V_{IO}. V_{SUP} is a high-voltage supply pin designed to connect to the V_{BAT} rail, V_{CC} is a low-voltage supply pin with an input voltage range from 4.5V to 5.5V that supports the CAN transceiver and V_{IO} is a low-voltage supply pin with an input voltage range from 2.95V to 5.5V that provides the I/O voltage to match the system controller. For a reliable operation, a 100nF decoupling capacitor should be placed as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the output of switched-mode power supplies, and also helps to compensate for the resistance and inductance of the PCB power planes.

8.3 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

8.3.1 Layout Guidelines

The layout example provides information on components around the device. Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. Transient voltage suppression (TVS) device can be added for extra protection, shown as D1. The production solution can be either a bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C6 and C7. A series common-mode choke (CMC) is placed on the CANH and CANL lines between the device and connector J1.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance. Note that high-frequency currents follow the path of least impedance and not the path of least resistance. Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver, examples are C1 on V_{CC}, C2 on V_{IO} , and C3 and C4 on the V_{SUP} supply.
- V_{IO} pin of the transceiver is connected to the microcontroller IO supply voltage (µC V).
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R3 and R4, with the center or split tap of the termination connected to ground via capacitor C5. Split termination provides common-mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to make sure the terminating node is not removed from the bus; thus, also removing the termination.
- INH, pin 7, can have a 100kΩ resistor (R1) to ground.
- WAKE, pin 9, can recognize either a rising or a falling edge of a wake signal and is usually connected to an external switch. The pin should be configured as shown with C8 which is a 22nF capacitor to GND where R5 is 33kΩ and R6 is 3kΩ.

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8.3.2 Layout Example

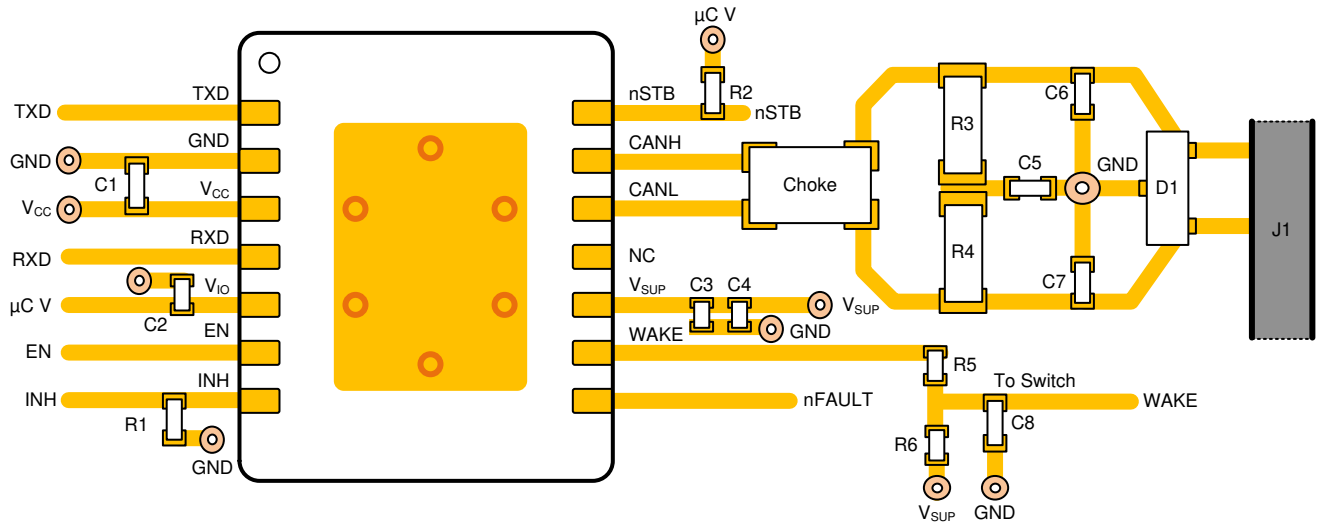

Figure 8-4. Example Layout

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9 Device and Documentation Support

9.1 Documentation Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

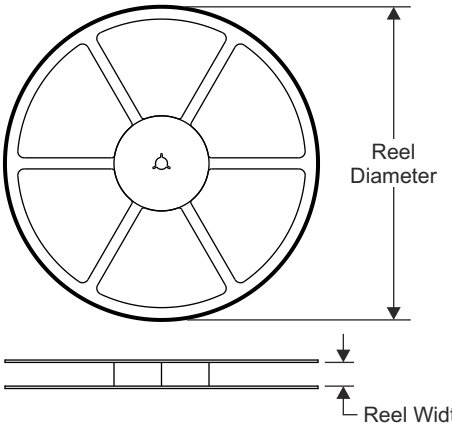
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

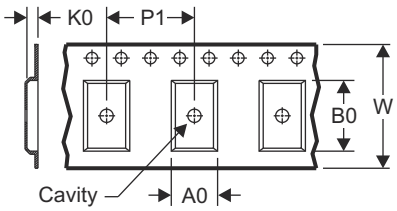
11.1 Package Option Addendum

11.1.1 Tape and Reel Information

REEL DIMENSIONS

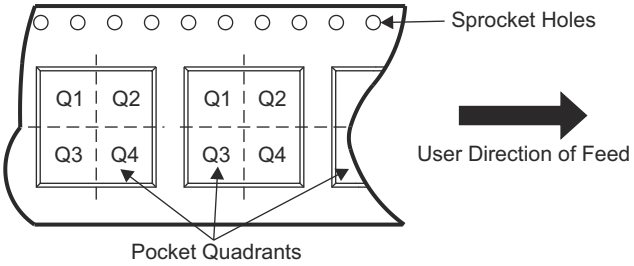


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DEVICE	PACKAGE TYPE	PACKAGE DRAWING	PINS	SPQ	REEL DIAMTER (mm)	REEL WIDTH W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN1 QUADRANT
TCAN843DYYQ1	SOT	DYY	14	250	177.8	12.4	3.56	4.5	1.3	8.0	12.0	Q1Q1
TCAN843DQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN843NMTQ1	VSON	DMT	14	3000	180.0	12.4	3.2	47.0	1.15	8.0	12.0	Q1

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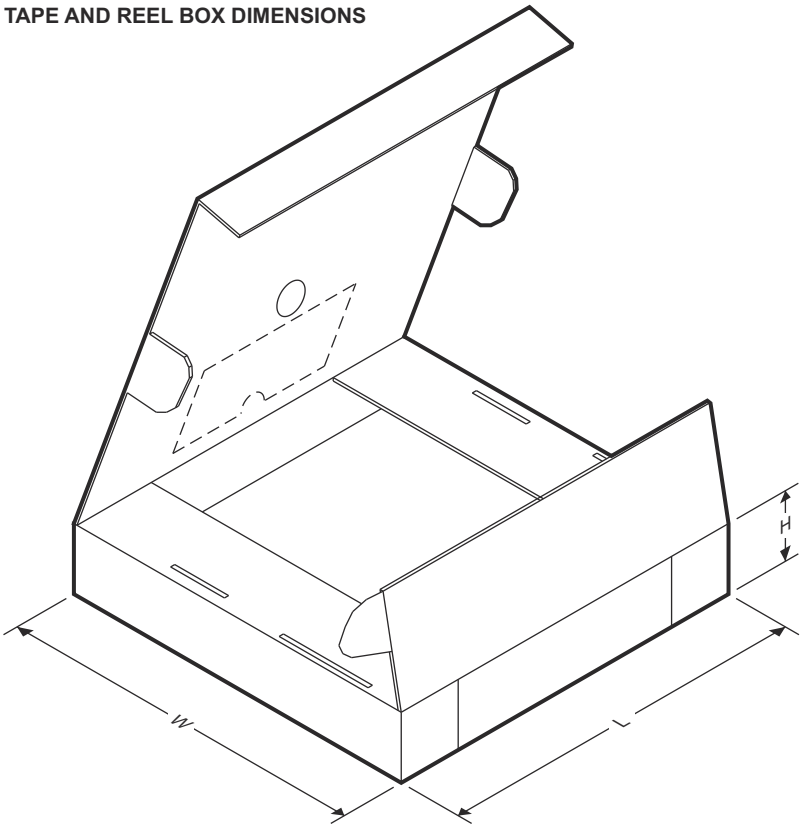
TAPE AND REEL BOX DIMENSIONS



DEVICE	PACKAGE TYPE	PACKAGE DRAWING	PINS	SPQ	LENGTH (mm)	WIDTH (mm)	HEIGHT (mm)
TCAN843DYYQ1	SOT	DYY	14	250	208.0	191.0	35.0
TCAN843DQ1	SOIC	D	14	2500	333.2	345.9	28.6
TCAN843DMTQ1	VSON	DMT	14	3000	370.4	355.0	55.0

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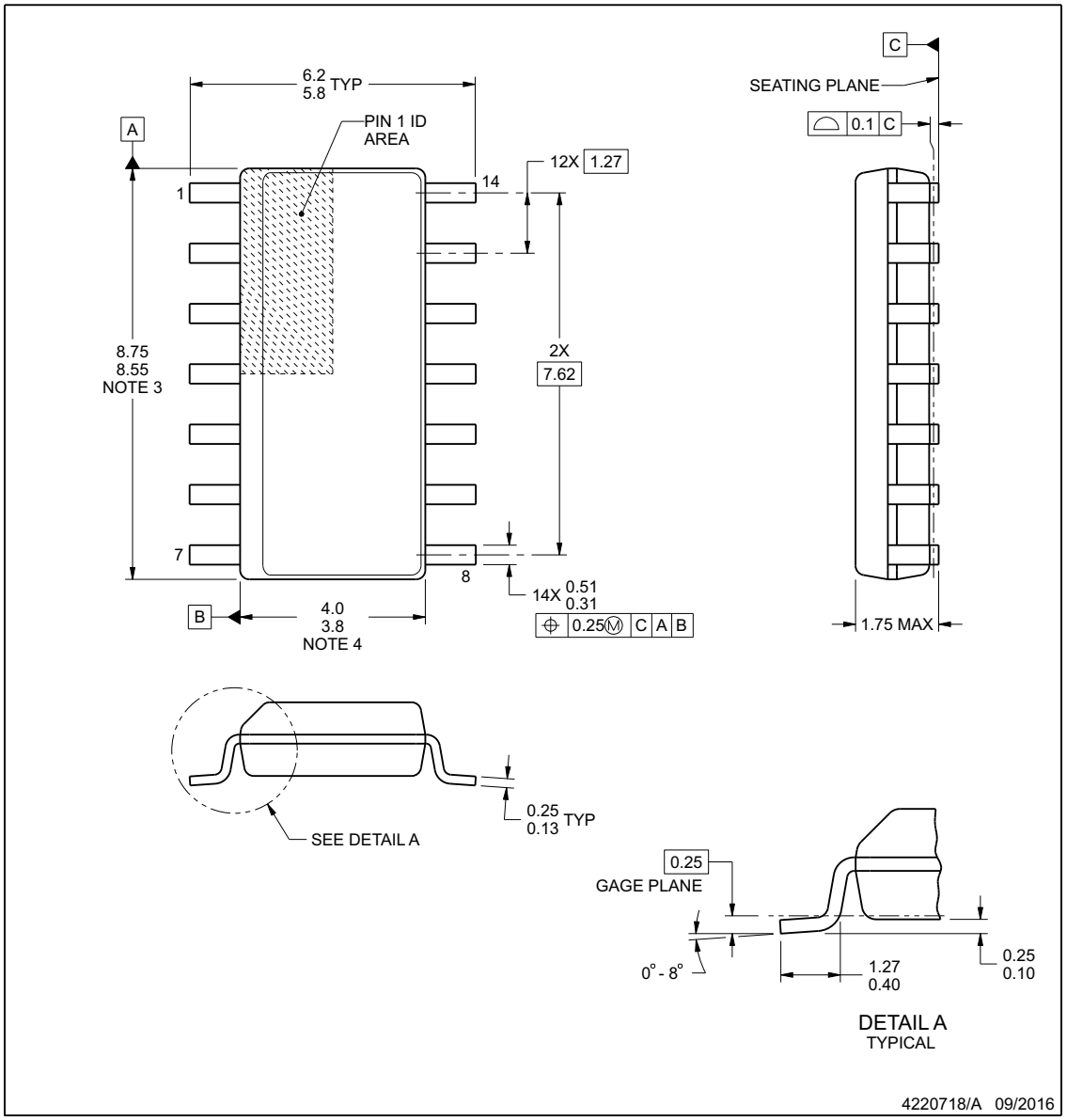
PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

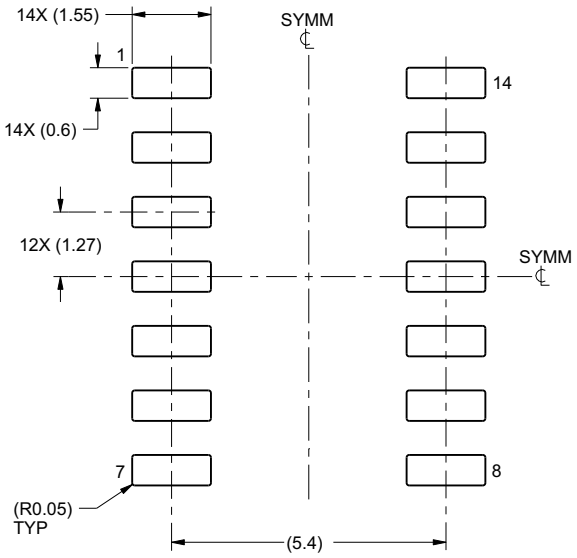
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

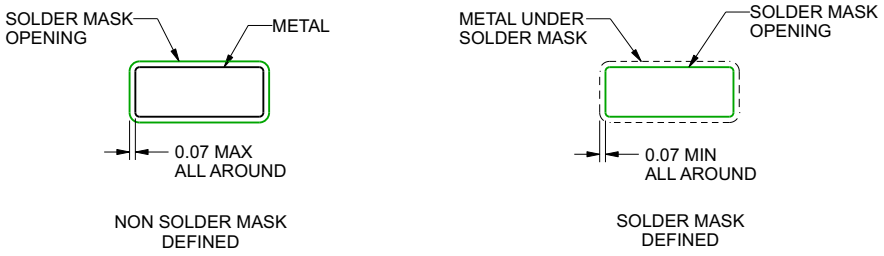
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

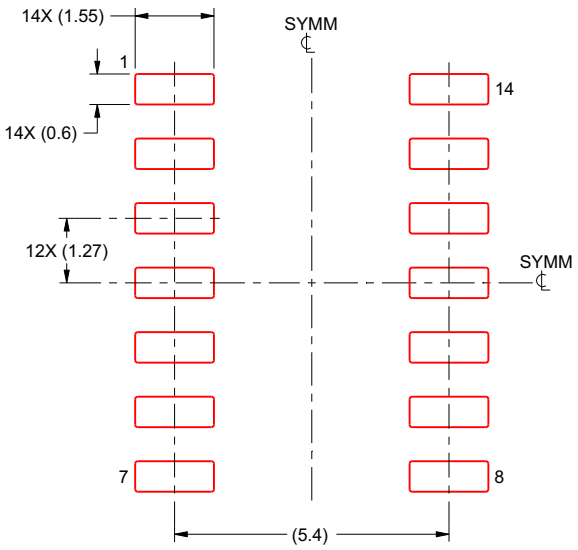
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

D0014A — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

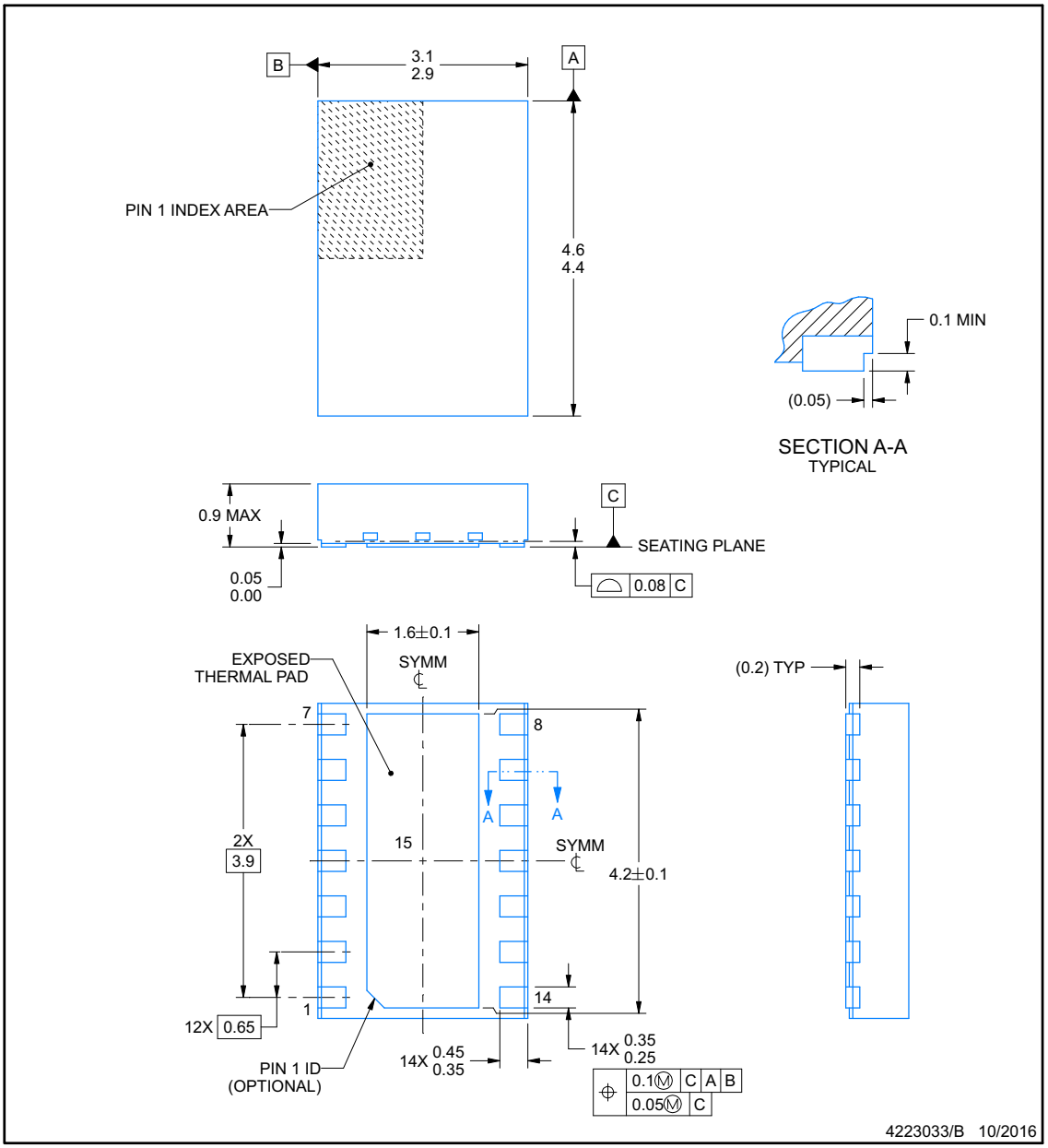
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DMT0014A

VSON - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

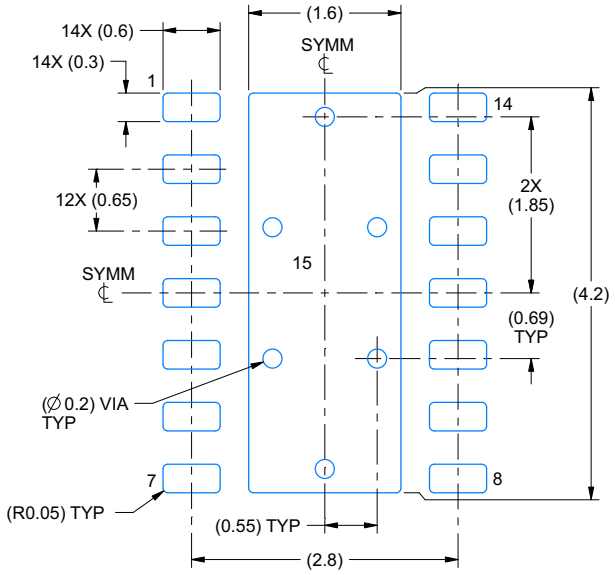
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

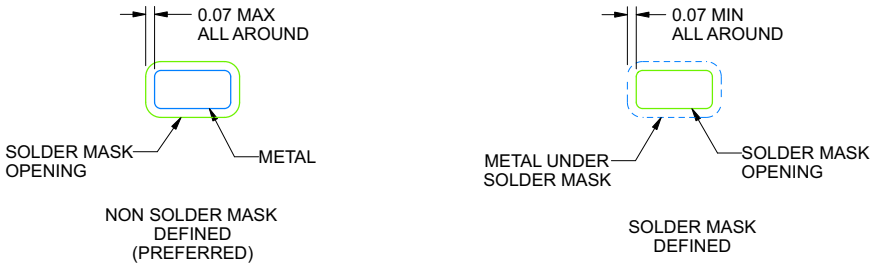
DMT0014A

VSON - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4223033/B 10/2016

NOTES: (continued)

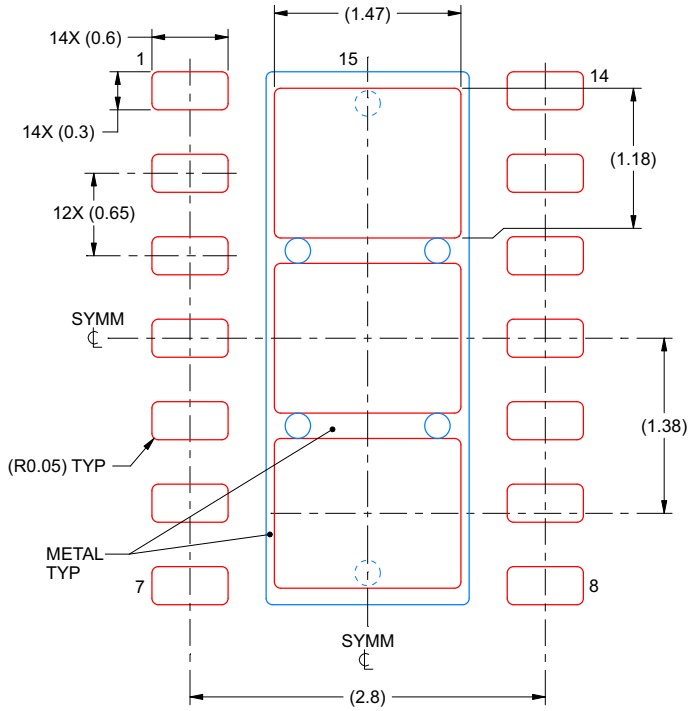
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DMT0014A

VSON - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4223033/B 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

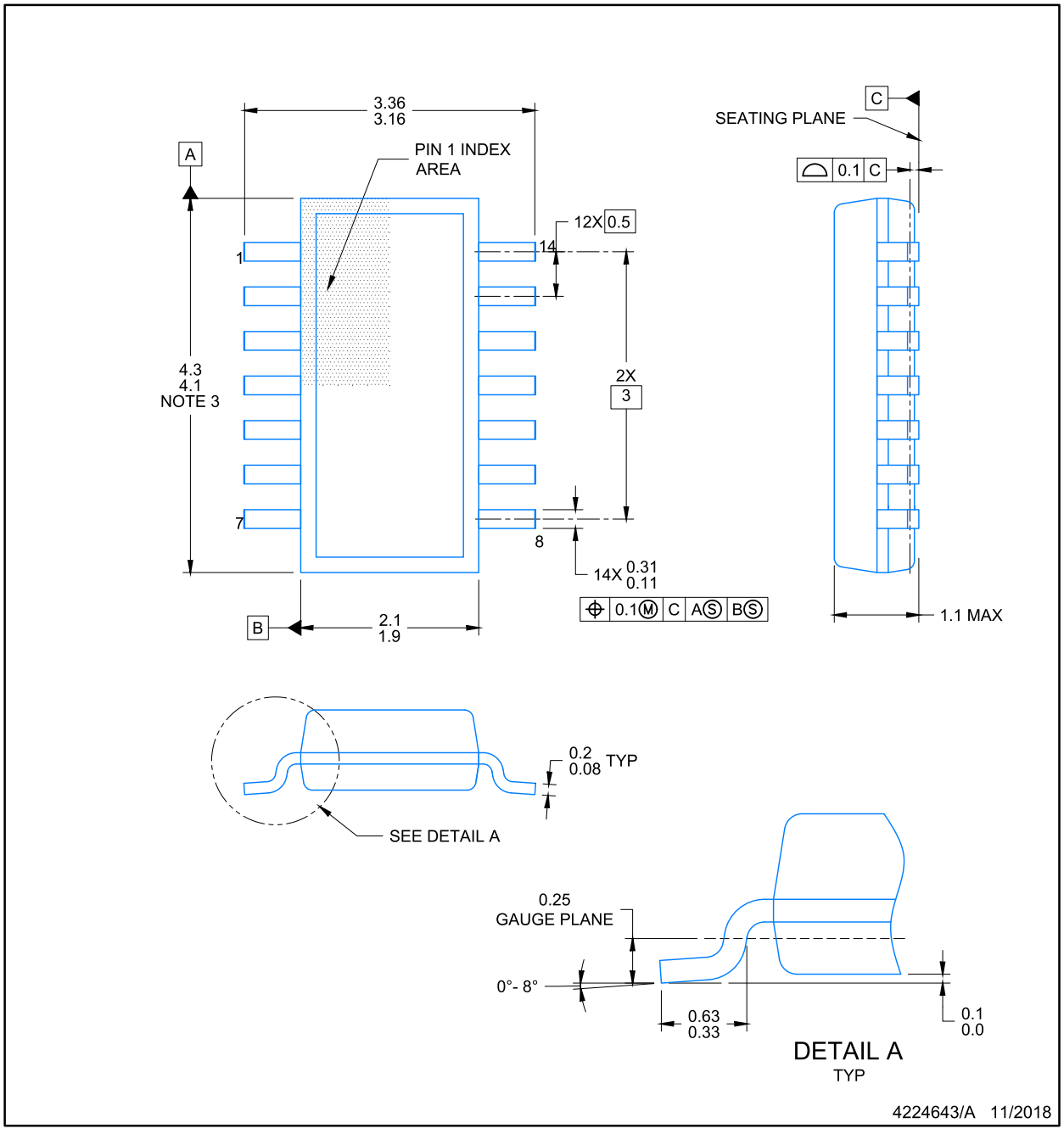
ADVANCE INFORMATION

ADVANCE INFORMATION

PACKAGE OUTLINE

DYY0014A — SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

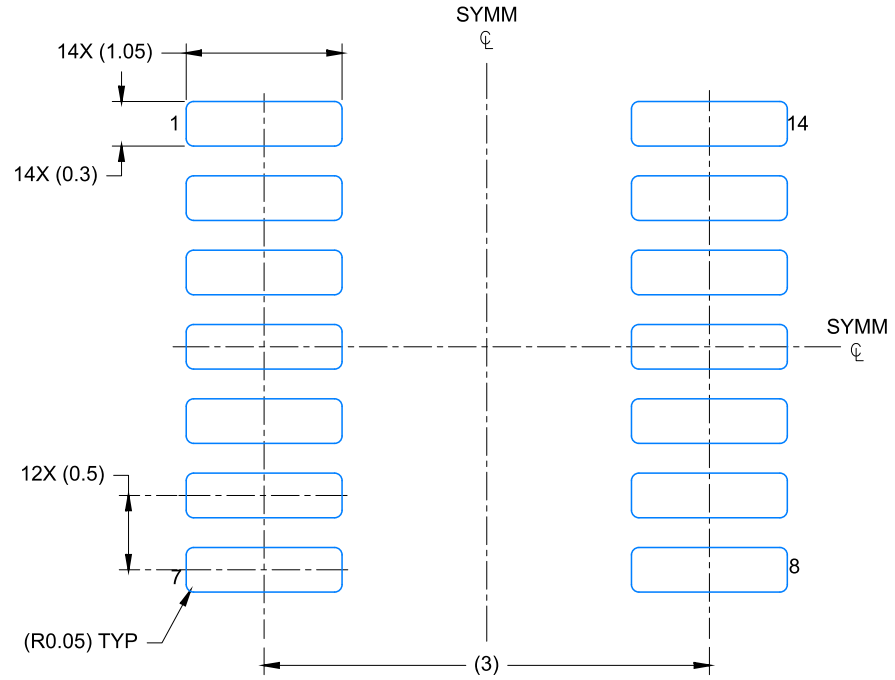
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

EXAMPLE BOARD LAYOUT

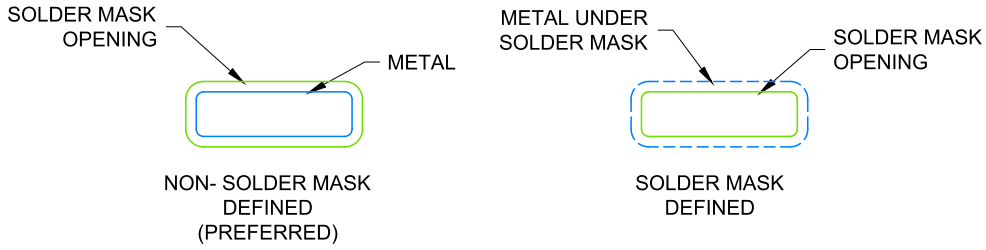
DYY0014A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224643/A 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

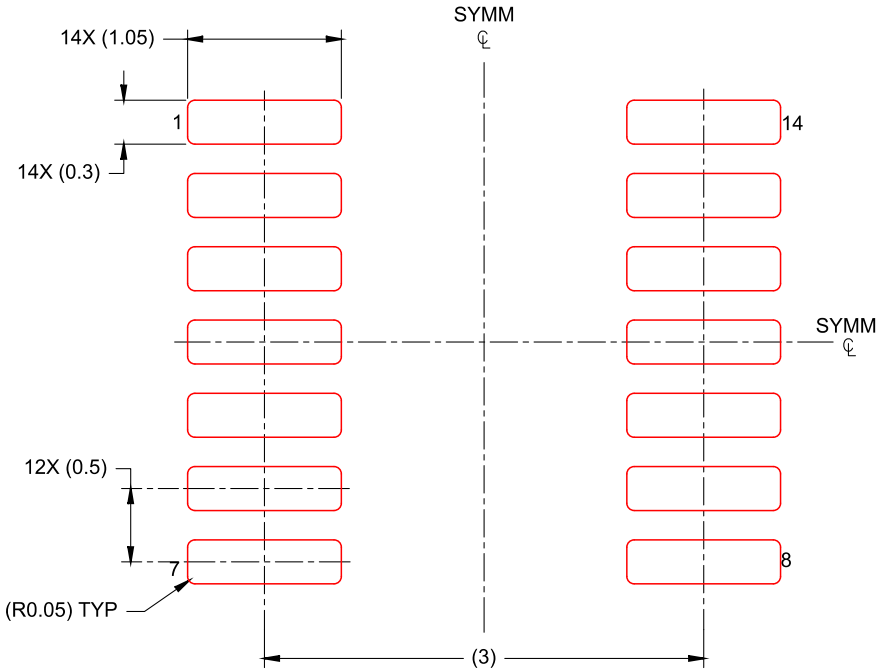
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DYY0014A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/A 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTCAN843DMTRQ1	Active	Preproduction	VSON (DMT) | 14	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
PTCAN843DRQ1	Active	Preproduction	SOIC (D) | 14	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
PTCAN843DYYRQ1	Active	Preproduction	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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