TCAN340x-Q1 3.3V Automotive CAN FD Transceivers with Standby Mode and ±58V bus Standoff

1 Features

- AEC-Q100 Qualified for automotive applications
- 3.3V Single supply operation
  - Eliminates the 5V regulator saving BOM cost and reducing PCB space
- Excellent EMC operation in homogeneous and heterogeneous networks
- Compatible with the requirements of ISO 11898-2:2016 physical layer standard
- Functional Safety-Capable
  - Documentation available to aid in functional safety system design
- Support of classical CAN and optimized CAN FD performance at 2, 5, and 8Mbps
  - Short and symmetrical propagation delays for enhanced timing margin
- TCANC3403-Q1: I/O voltage range supports: 1.7V to 3.6V
- Receiver common mode input voltage: ±30V
- Protection features:
  - Bus fault protection: ±58V
  - ISO 10605 ESD on bus pins: ±8kV
  - Undervoltage protection
  - TXD-dominant time-out (DTO)
  - Thermal-shutdown protection (TSD)
- Operating modes:
  - Normal mode
  - Low power standby mode supporting remote wake-up request
  - Ultra-low power shutdown mode: TCANC3404-Q1 only
- Optimized behavior when unpowered
  - Bus and logic pins are high impedance (no load to operating bus or application)
  - Hot-plug capable: power up or down glitch-free operation on bus and RXD output
- 8-Pin SOIC, small footprint SOT-23 and lead less VSON-8 package with wettable flanks for automated optical inspection (AOI)

2 Applications

- Automotive and transportation
  - Body control modules
  - Automotive gateway
  - Advanced driver assistance system (ADAS)
  - Infotainment

3 Description

The TCANC3403-Q1 and TCANC3404-Q1 are 3.3V controller area network (CAN) FD transceivers that are compatible with the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification.

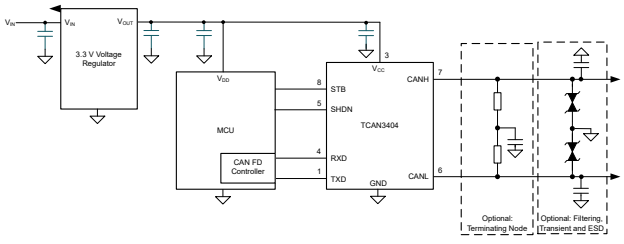
The transceivers have certified electromagnetic compatibility (EMC) operation for use with classical CAN and CAN FD networks up to 5 megabits per second (Mbps). Up to 8Mbps operation in simpler networks is possible with these devices. The TCANC3403-Q1 includes an internal logic level translation through the V_{IO} pin, allowing the direct interface of the transceiver I/Os to 1.8V, 2.5V, or 3.3V logic levels. The TCANC3404-Q1 has shutdown feature where all blocks are powered off and device enters ultra-low power consumption mode. The transceivers support a low-power standby mode, and a wake over CAN which is compliant to the ISO 11898-2:2016 defined wake-up pattern (WUP).

The transceivers include thermal-shutdown (TSD), TXD-dominant time-out (DTO) and supply undervoltage detection. The devices have defined fail-safe behavior in supply undervoltage or floating pin scenarios. These devices are available in industry-standard SOIC-8, the VSON-8, and a space-saving small footprint SOT-23 packages.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCANC3403-Q1 TCANC3404-Q1	SOIC (D)	4.9mm x 6mm
	VSON (DRB)	3mm x 3mm
	SOT-23 (DDF)	2.9mm x 2.8mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

4 Device Comparison

Part Number	Pin 5	Pin 8
TCAN3404-Q1	Ultra-low power shutdown mode	Low Power Standby Mode with Remote Wake
TCAN3403-Q1	Low voltage I/O support	

5 Pin Configuration and Functions

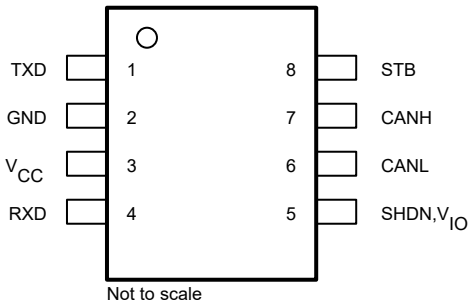


Figure 5-1. DDF Package, 8-Pin SOT-23 (Top View)

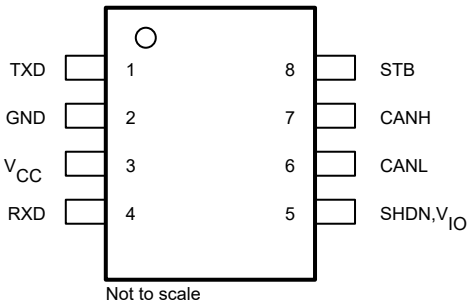


Figure 5-2. D Package, 8-Pin SOIC (Top View)

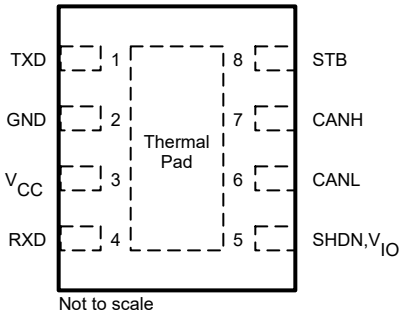


Figure 5-3. DRB Package, 8-Pin VSON (Top View)

Table 5-1. Pin Functions

PINS		TYPE[1]	DESCRIPTION
NAME	NO.		
TXD	1	Digital Input	CAN transmit data input; integrated pull-up
GND	2	G	Ground connection
V_{CC}	3	Supply	3.3V supply voltage
RXD	4	Digital Output	CAN receive data output, tri-stated when device powered off
SHDN	5	Digital Input	Device in ultra-low power shutdown mode if pin is high; integrated pull-down (TCAN3404-Q1 only)
V_{IO}		Supply	I/O supply voltage (TCAN3403-Q1 only)
CANL	6	Bus I/O	Low-level CAN bus input/output line
CANH	7	Bus I/O	High-level CAN bus input/output line
STB	8	Digital Input	Standby input for mode control; integrated pull-up
Thermal Pad (VSON only)		—	Connect the thermal pad to any internal PCB ground plane using multiple vias for optimal thermal performance.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter (only for TCAN3403)	–0.3	6	V
V_{BUS}	CAN bus I/O voltage range on CANH and CANL	–58	58	V
V_{DIFF}	Max differential voltage between CANH and CANL V_{DIFF} = (CANH - CANL)	–58	58	V
V_{Logic_Input}	Logic pin input voltage (TXD, STB, SHDN)	–0.3	6	V
V_{RXD}	Logic output voltage range (RXD)	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Junction temperature	–40	165	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pins	±4000	V
			HBM classification level 3B for global pins CANH and CANL with respect to GND	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings, IEC Transients

				VALUE	UNIT
V_{ESD}	System level electrostatic discharge	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10605 Powered contact discharge	±8000	V
			SAE J2962-2 per ISO 10605 Powered air discharge	±15000	V
			IEC 62228-3 per ISO 10605	±8000	V
V_{Tran}	ISO 7637-2 Transient immunity(1)	CAN bus terminals (CANH, CANL) to GND	Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	Direct capacitor coupling, SAE J2962-2 per ISO 7637-3(2)	CAN bus terminals (CANH, CANL) to GND	DCC slow transient pulse	±30	V

(1) Tested according to IEC 62228-3:2019 CAN Transceivers, Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011)
(2) Tested according to SAE J2962-2

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IO}	Supply voltage for I/O level shifter (only for TCAN3403)	1.7		3.6	V

6.4 Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
$I_{OH(RXD)}$	RXD terminal high-level output current	–2			mA
$I_{OL(RXD)}$	RXD terminal low-level output current			2	mA
$I_{OH(RXD)}$	RXD terminal high-level output current (only for TCAN3403)	–1.5			mA
$I_{OL(RXD)}$	RXD terminal low-level output current (only for TCAN3403)			1.5	mA
T_J	Junction temperature	–40		150	°C

6.5 Thermal Characteristics

THERMAL METRIC[1]		TCAN3403/3404-Q1			UNIT
		D (SOIC)	DDF (SOT)	DRB (VSON)	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	114.4	122.9	50.9	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	49.0	51.7	55.8	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	58.0	45.7	23.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.0	1.3	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	57.1	45.4	23.2	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	7.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Supply Characteristics

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 3.3 V; V_{IO} = 3.3 V for TCAN3403 , Device ambient maintained at 27°C) unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current normal mode	Dominant	TXD = 0 V, STB = 0 V R_L = 60 Ω, C_L = open See Figure 7-1		42	55	mA
		Dominant	TXD = 0 V, STB = 0 V R_L = 50 Ω, C_L = open See Figure 7-1		50	60	mA
		Recessive	TXD = V_{CC}, STB = 0 V R_L = 50 Ω, C_L = open See Figure 7-1		7	8.2	mA
I_{CC}	Supply current normal mode	Dominant with bus fault	TXD = 0 V, STB = 0 V CANH = CANL = ±25 V R_L = open, C_L = open See Figure 7-1			130	mA
	Supply current standby mode (TCAN3403)		TXD = STB = V_{IO}, R_L = 50 Ω, C_L = open , T_J <= 85 °C, See Figure 7-1		1	2	µA
			TXD = STB = V_{IO}, R_L = 50 Ω, C_L = open , T_J <= 125 °C, See Figure 7-1		1	3	
			TXD = STB = V_{IO}, R_L = 50 Ω, C_L = open, T_J <= 150 °C, See Figure 7-1		1	4	
	Supply current standby mode (TCAN3404)		TXD = STB = V_{CC}, R_L = 50 Ω, C_L = open, T_J <= 85 °C, See Figure 7-1		10	15	µA
			TXD = STB = V_{CC}, R_L = 50 Ω, C_L = open, T_J <= 125 °C, See Figure 7-1		10	16	
			TXD = STB = V_{CC}, R_L = 50 Ω, C_L = open, T_J <= 150 °C, See Figure 7-1		10	17	

6.6 Supply Characteristics (continued)

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 3.3 V; V_{IO} = 3.3 V for TCAN3403 , Device ambient maintained at 27°C) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IO} (only for TCAN3403)	I/O supply current normal mode	Dominant	TXD = 0 V, STB = 0 V R_L = 60 Ω, C_L = open RXD floating		125	300	µA
		recessive	TXD = V_{IO}, STB = 0 V R_L = 60 Ω, C_L = open RXD floating		19	48	
	I/O supply current standby mode		TXD = V_{IO}, STB = V_{IO} R_L = 60 Ω, C_L = open RXD floating, T_J <= 85 °C		9	13	
			TXD = V_{IO}, STB = V_{IO} R_L = 60 Ω, C_L = open RXD floating, T_J <= 125 °C		9	14	
			TXD = V_{IO}, STB = V_{IO} R_L = 60 Ω, C_L = open RXD floating, T_J <= 150 °C		9	15	
I_{CC}	Supply current (V_{CC} pin current), shutdown mode (TCAN3404)		SHDN = V_{CC}, RXD floating, TXD = V_{CC}, T_J <= 85 °C			2	µA
			SHDN = V_{CC}, RXD floating, TXD = V_{CC}, T_J <= 150 °C			5	
$UV_{CC(R)}$	Undervoltage detection V_{CC} rising		Ramp up		2.75	2.9	V
$UV_{CC(F)}$	Undervoltage detection on V_{CC} falling		Ramp down	2.5	2.65		
$V_{HYS(UVCC)}$	Hysteresis voltage on UV_{CC}				120		mV
$UV_{IO(R)}$	Undervoltage detection V_{IO} rising (TCAN3403)		Ramp up		1.6	1.65	V
$UV_{IO(F)}$	Undervoltage detection on V_{IO} falling (TCAN3403)		Ramp down	1.4	1.5		
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{IO}				50		mV

6.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 3.3 V, T_J = 27°C, R_L = 60Ω, C_{L_RXD} = 15 pF TXD input = 250 kHz 50% duty cycle square wave		50		mW
		V_{CC} = 3.6 V, T_J = 150°C, R_L = 50Ω, C_{L_RXD} = 15 pF TXD input = 2.5 MHz 50% duty cycle square wave		60		mW
T_{TSD}	Thermal shutdown temperature			192		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			10		

6.8 Electrical Characteristics

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 3.3 V, V_{IO} = 3.3 V for TCAN3403 , Device ambient maintained at 27°C) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(DOM)}$	Dominant output voltage normal mode	CANH	TXD = 0 V, STB, SHDN = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open See Figure 7-2 and Figure 8-3	2.25		V_{CC}	V
		CANL		0.5		1.25	V
$V_{O(REC)}$	Recessive output voltage normal mode	CANH and CANL	TXD = V_{IO} or V_{CC}, STB, SHDN = 0 V R_L = open (no load), C_L = open See Figure 7-2 and Figure 8-3	1.5	1.9	2.25	V

6.8 Electrical Characteristics (continued)

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 3.3 V, V_{IO} = 3.3 V for TCAN3403 , Device ambient maintained at 27°C) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SYM}	Driver symmetry {($V_{O(CANH)}$ + $V_{O(CANL)}$)/($V_{O(REC\_CANH)}$ + $V_{O(REC\_CANL)}$)}		TXD = 250 kHz, 1 MHz, 2.5 MHz, STB, SHDN = 0 V R_L = 60, C_{SPLIT} = 4.7 nF, C_L = open See Figure 7-2 and Figure 9-2	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry ($CANH_{REC}$ + $CANL_{REC}$ - $CANH_{DOM}$ - $CANL_{DOM}$)		STB, SHDN = 0 V R_L = 60 Ω, C_L = open See Figure 7-2 and Figure 8-3	–400		400	mV
$V_{OD(DOM)}$	Differential output voltage normal mode Dominant	CANH - CANL	TXD = 0 V, STB. SHDN = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open See Figure 7-2 and Figure 8-3	1.5		3	V
			TXD = 0 V, STB, SHDN = 0 V 45 Ω ≤ R_L ≤ 70 Ω, C_L = open See Figure 7-2 and Figure 8-3	1.4		3	V
		CANH - CANL	TXD = 0 V, STB, SHDN = 0 V R_L = 2240 Ω, C_L = open See Figure 7-2 and Figure 8-3	1.5		3.4	V
$V_{OD(REC)}$	Differential output voltage normal mode Recessive	CANH - CANL	TXD = V_{IO} or V_{CC}, STB, SHDN = 0 V R_L = 60 Ω, C_L = open See Figure 7-2 and Figure 8-3	–120		12	mV
		CANH - CANL	TXD = V_{IO} or V_{CC}, STB, SHDN = 0 V R_L = open, C_L = open See Figure 7-2 and Figure 8-3	–50		50	mV
$V_{O(STB)}$	Bus output voltage standby mode	CANH	TXD = STB = V_{IO} or V_{CC}, R_L = open , C_L = open See Figure 7-2 and Figure 8-3	-0.1		0.1	V
		CANL		-0.1		0.1	V
		CANH - CANL		-0.2		0.2	V
$I_{OS(DOM)}$	Short-circuit bus output current, dominant, normal mode		See Figure 7-7 and Figure 8-3, $V_{(CANH)}$ = -15 V to 40 V, CANL = open, TXD = 0 V	–115		115	mA
			See Figure 7-7 and Figure 8-3 , $V_{(CAN\_L)}$ = -15 V to 40 V, CANH = open, TXD = 0 V	–115		115	mA
$I_{OS(REC)}$	Short-circuit steady-state output current, recessive, normal mode		See Figure 7-7 and Figure 8-3 , $V_{(CANH)}$ = -27 V to 32 V, CANL = open, STB=0, TXD = V_{IO} or V_{CC},	–7		7	mA
			See Figure 7-7 and Figure 8-3 , $V_{(CANL)}$ = -27 V to 32 V, CANH = open, STB = 0, TXD = V_{IO} or V_{CC},	–7		7	mA
Receiver Electrical Characteristics							
V_{IT}	Input threshold voltage normal mode		See Figure 7-3 and Table 8-6 -30 V ≤ V_{CM} ≤ 30 V, STB, SHDN= 0 V	500		900	mV
$V_{IT(STB)}$	Input threshold standby mode, TCAN3404		See Figure 7-3 and Table 8-6 -30 V ≤ V_{CM} ≤ 30 V, SHDN= 0 V, STB= V_{CC}	400		1150	mV
	Input threshold standby mode, TCAN3403		See Figure 7-3 and Table 8-6 V_{IO} = 3 V to 3.6 V, -30 V ≤ V_{CM} ≤ 30 V, STB= V_{IO}	400		1150	mV
			See Figure 7-3 and Table 8-6 V_{IO} = 1.7 V to 1.9 V, 2.25 V to 2.75 V, -12 V ≤ V_{CM} ≤ 12 V, STB= V_{IO}	400		1150	mV
V_{DOM}	Normal mode dominant state differential input voltage range		See Figure 7-3 and Table 8-6 -30 V ≤ V_{CM} ≤ 30 V, STB, SHDN= 0 V	0.9		9	V
V_{REC}	Normal mode recessive state differential input voltage range		See Figure 7-3 and Table 8-6 -30 V ≤ V_{CM} ≤ 30 V, STB, SHDN= 0 V	-4		0.5	V
$V_{DOM(STB)}$	Standby mode dominant state differential input voltage range		See Figure 7-3 and Table 8-6 SHDN= 0 V, STB = V_{IO}, -30 V ≤ V_{CM} ≤ 30 V	1.15		9	V
$V_{REC(STB)}$	Standby mode recessive state differential input voltage range		See Figure 7-3 and Table 8-6 SHDN = 0 V, STB = V_{IO}, -30 V ≤ V_{CM} ≤ 30 V	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold normal mode		See Figure 7-3 and Table 8-6 -30 V ≤ V_{CM} ≤ 30 V, STB, SHDN= 0 V		50		mV

6.8 Electrical Characteristics (continued)

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 3.3 V, V_{IO} = 3.3 V for TCAN3403 , Device ambient maintained at 27°C) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CM}	Common mode range normal and standby modes	See Figure 7-3 and Table 8-6	–30		30	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			5	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{IO},			40	pF
C_{ID}	Differential input capacitance				20	pF
R_{ID}	Differential input resistance	TXD = V_{IO}, STB = 0 V -30 V ≤ V_{CM} ≤ 30 V	25		50	kΩ
R_{IN}	Single ended input resistance (CANH or CANL)		13		25	kΩ
$R_{IN(M)}$	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5 V	–3		3	%
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage	TCAN3404	0.7 V_{CC}			V
V_{IH}	High-level input voltage	TCAN3403	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	TCAN3404			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	TCAN3403			0.3 V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 3.6 V	–2.5	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0 V, V_{CC} = V_{IO} = 3.6 V	–200	-100	–20	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 3.6 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA
C_I	Input capacitance			4		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level output voltage	TCAN3404 See Figure 7-3 , I_O = –2 mA	0.8 V_{CC}			V
V_{OH}	High-level output voltage	See Figure 7-3 , I_O = –1.5 mA, TCAN3403	0.8 V_{IO}			V
V_{OL}	Low-level output voltage	TCAN3404 See Figure 7-3 , I_O = 2 mA			0.2 V_{CC}	V
V_{OL}	Low-level output voltage	TCAN3403 See Figure 7-3 , I_O = 1.5 mA			0.2 V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 3.6 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA
STB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage	TCAN3404	0.7 V_{CC}			V
V_{IH}	High-level input voltage	TCAN3403	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	TCAN3404			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	TCAN3403			0.3 V_{IO}	V
I_{IH}	High-level input leakage current	V_{CC} = V_{IO} = STB = 3.6 V	–2		2	µA
I_{IL}	Low-level input leakage current	V_{CC} = V_{IO} = 3.6 V, STB = 0 V	–20		–2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 3.6V, V_{CC}= V_{IO} = 0 V	–1	0	1	µA
SHDN Terminal (Shutdown mode input)						
V_{IH}	High-level input voltage	TCAN3404	0.7 V_{CC}			V
V_{IL}	Low-level input voltage	TCAN3404			0.3 V_{CC}	V
I_{IH}	High-level input leakage current	V_{CC} = V_{IO} = SHDN = 3.6 V	2		5.5	µA
I_{IL}	Low-level input leakage current	V_{CC} = V_{IO} = 3.6 V, SHDN = 0 V	–2		2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	SHDN = 3.6 V, V_{CC}= V_{IO} = 0 V	–1	0	1	µA

6.9 Switching Characteristics

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 3.3 V, V_{IO} = 3.3 V for TCAN3403 , Device ambient maintained at 27°C) unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics					

6.9 Switching Characteristics (continued)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 3.3 V, V_{IO} = 3.3 V for TCAN3403 , Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See Figure 7-4, normal mode, V_{CC} = V_{IO} = 3 V to 3.6 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF TCAN3404, TCAN3403		95	180	ns
		See Figure 7-4 , normal mode, V_{CC} = 3 to 3.6 V, V_{IO} = 2.25 V to 2.75 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF TCAN3403		102	190	ns
		See Figure 7-4 , normal mode, V_{CC} = 3 to 3.6 V, V_{IO} = 1.71 V to 1.89 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF TCAN3403		115	210	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	See Figure 7-4 , normal mode, V_{CC} = V_{IO} = 3 V to 3.6 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF TCAN3404, TCAN3403		120	180	ns
		See Figure 7-4 , normal mode, V_{CC} = 3 to 3.6 V, V_{IO} = 2.25 V to 2.75 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF TCAN3403		125	190	ns
		See Figure 7-4 , normal mode, V_{CC} = 3 to 3.6 V, V_{IO} = 1.71 V to 1.89 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF TCAN3403		140	210	ns
t_{MODE}	Mode change time, from normal to standby or from standby to normal	See Figure8-5 in TCAN1044A datasheet See Figure 7-5			30	µs
t_{SHDN1}	Mode change time from normal mode to shutdown mode	With TXD = High, Time from SHDN pin (low to high edge 50%) to CANH going from recessive level Vo(rec) to 0.5V			40	µs
t_{SHDN2}	Mode change time from shutdown mode to normal mode	With TXD high, time from SHDN pin (high to low edge 50%) to CANH going from 0.5V to Vo(rec)			200	µs
t_{WK_FILTER}	Filter time for a valid wake-up pattern	See Figure 8-5	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value		0.8		6	ms
Tstartup	Time duration after V_{CC} or V_{IO} hass cleared UV+, and device can resume normal operation				1.5	ms
$T_{filter(STB)}$	Filter on STB pin to filter out any glitches		0.5	1	2	µs
$T_{filter(SHDN)}$	Filter on SHDN pin to filter out any glitches		0.5	1	2	µs
Driver Switching Characteristics						
$t_{prop(TxD-busrec)}$	Propagation delay time, low-to-high TXD edge to driver recessive (dominant to recessive)	See Figure 7-2 , STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{CC} = V_{IO} = 3 V to 3.6 V TCAN3404, TCAN3403		65	100	ns
		See Figure 7-2 ,STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{CC} = 3 to 3.6 V, V_{IO} = 2.25 V to 2.75 V TCAN3403		67	110	ns
		See Figure 7-2 ,STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{CC} = 3 to 3.6 V, V_{IO} = 1.71 V to 1.89 V TCAN3403		71	110	ns

6.9 Switching Characteristics (continued)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 3.3 V, V_{IO} = 3.3 V for TCAN3403 , Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{prop(TxD-busdom)}$	Propagation delay time, high-to-low TXD edge to driver dominant (recessive to dominant)	See Figure 7-2 , STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{CC} = V_{IO} = 3 V to 3.6 V TCAN3404, TCAN3403		46	100	ns
		See Figure 7-2 ,STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{CC} = 3 to 3.6 V, V_{IO} = 2.25 V to 2.75 V TCAN3403		48	110	ns
		See Figure 7-2 ,STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{CC} = 3 to 3.6 V, V_{IO} = 1.71 V to 1.89 V TCAN3403		53	110	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{prop(TxD-busrec)} - t_{prop(TxD-busdom)} \rvert$)	, STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF, See Figure 7-2		18	28	ns
t_R	Differential output signal rise time	See Figure 7-2 , STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF		32	57	ns
t_F	Differential output signal fall time			30	50	ns
t_{TXD_DTO}	Dominant timeout	See Figure 7-6 , STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF	1.2		4.0	ms
Receiver Switching Characteristics						
$t_{prop(busrec-RXD)}$	Propagation delay time, bus recessive input to RXD high output (dominant to recessive)	See Figure 7-3 , STB, SHDN = 0 V, $C_{L(RXD)}$ = 15 pF, V_{CC} = V_{IO} = 3 V to 3.6 V TCAN3404, TCAN3403		55	90	ns
		See Figure 7-3 , STB, SHDN = 0 V, $C_{L(RXD)}$ = 15 pF, V_{CC} = 3 to 3.6 V, V_{IO} = 2.25 V to 2.75 V TCAN3403		60	90	ns
		See Figure 7-3 , STB, SHDN = 0 V, $C_{L(RXD)}$ = 15 pF, V_{CC} = 3 to 3.6 V, V_{IO} = 1.71 V to 1.89 V TCAN3403		70	102	ns
$t_{prop(busdom-RXD)}$	Propagation delay time, bus dominant input to RXD low output (recessive to dominant)	See Figure 7-3 , STB, SHDN = 0 V, $C_{L(RXD)}$ = 15 pF, V_{CC} = V_{IO} = 3 V to 3.6 V TCAN3404, TCAN3403		45	90	ns
		See Figure 7-3 , STB, SHDN = 0 V, $C_{L(RXD)}$ = 15 pF, V_{CC} = 3 to 3.6 V, V_{IO} = 2.25 V to 2.75 V TCAN3403		51	90	ns
		See Figure 7-3 , STB, SHDN = 0 V, $C_{L(RXD)}$ = 15 pF, V_{CC} = 3 to 3.6 V, V_{IO} = 1.71 V to 1.89 V TCAN3403		60	100	ns
t_R	RXD output signal rise time	See Figure 7-3 , STB, SHDN = 0 V $C_{L(RXD)}$ = 15 pF		10	25	ns
t_F	RXD output signal fall time			10	28	ns
FD Timing Characteristics						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	See Figure 7-4 , STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	450		525	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns		160		205	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 125 ns(1)		85		130	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns	See Figure 7-4 , STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	410		540	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns		130		210	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 125 ns(1)		75		135	ns

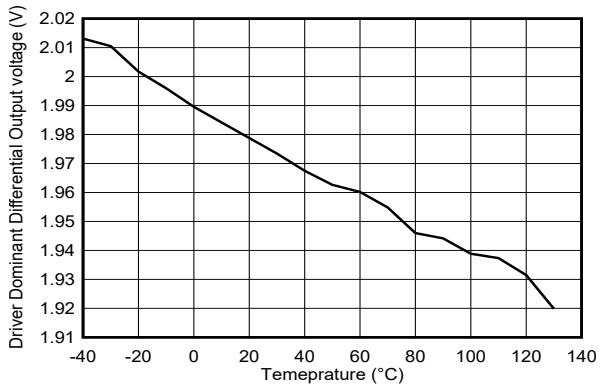
6.9 Switching Characteristics (continued)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 3.3 V, V_{IO} = 3.3 V for TCAN3403 , Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns	See Figure 7-4 , STB, SHDN = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-50		20	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns		-40		10	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 125 ns(1)		-40		10	ns

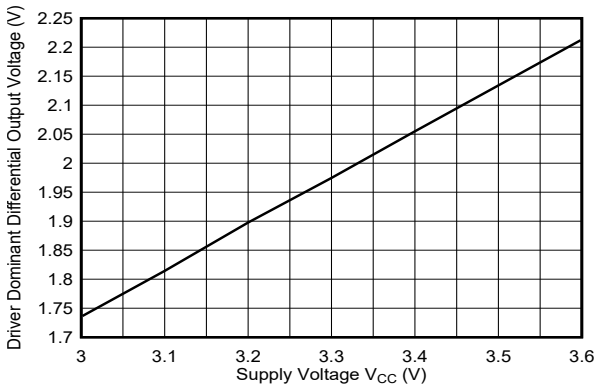
(1) Min/Max limits based on characterization.

6.10 Typical Characteristics



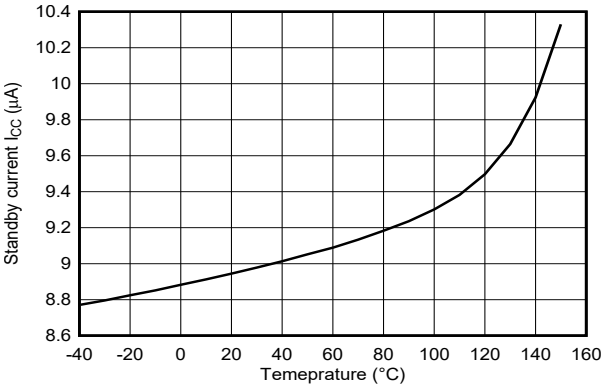
STB = GND V_{CC} = 3.3V R_L = 60Ω

Figure 6-1. $V_{OD(DOM)}$ vs Temperature



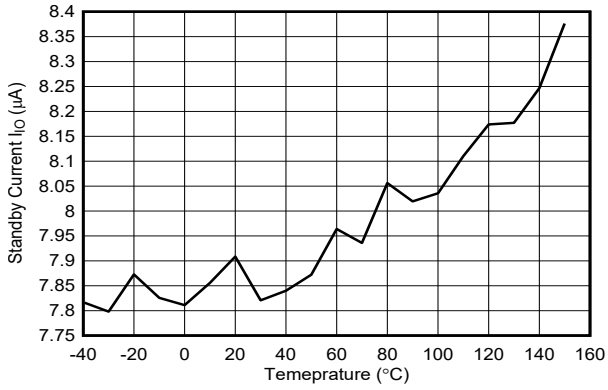
Temp = 25°C STB = GND R_L = 60Ω

Figure 6-2. $V_{OD(DOM)}$ vs V_{CC}



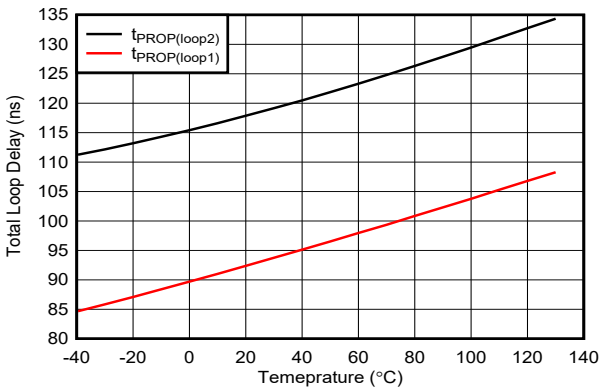
V_{CC} = 3.3V STB = V_{CC}

Figure 6-3. I_{CC} Standby vs Temperature



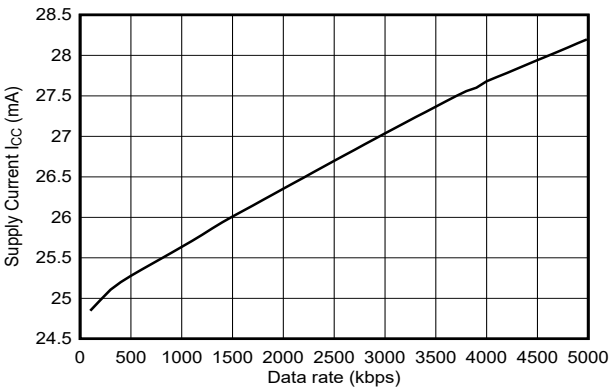
V_{CC} = 3.3V V_{IO} = 3.3V STB = V_{IO}

Figure 6-4. I_{IO} Standby vs Temperature



V_{CC} = V_{IO} = 3.3V C_L = 100pF R_L = 60Ω

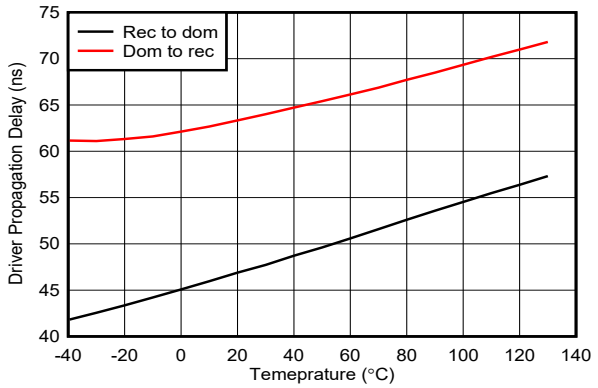
Figure 6-5. Total Loop Delay vs Temperature



V_{CC} = 3.3V R_L = 60Ω

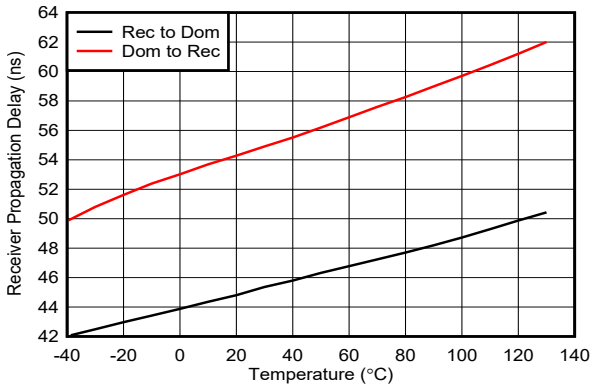
Figure 6-6. I_{CC} vs Data Rate

6.10 Typical Characteristics (continued)



V_{CC} = V_{IO} = 3.3V C_L = 100pF R_L = 60Ω

Figure 6-7. Driver Propagation Delay vs Temperature



V_{CC} = V_{IO} = 3.3V C_L = 100pF R_L = 60Ω

Figure 6-8. Receiver Propagation Delay vs Temperature

7 Parameter Measurement Information

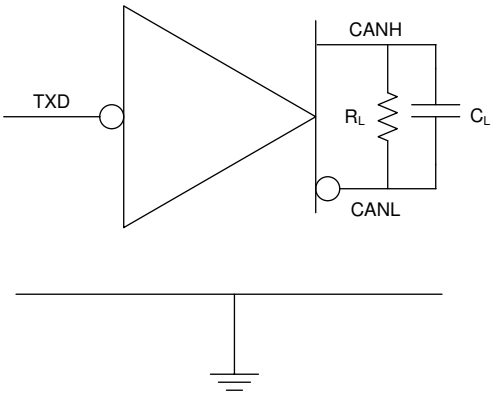


Figure 7-1. I_{CC} Test Circuit

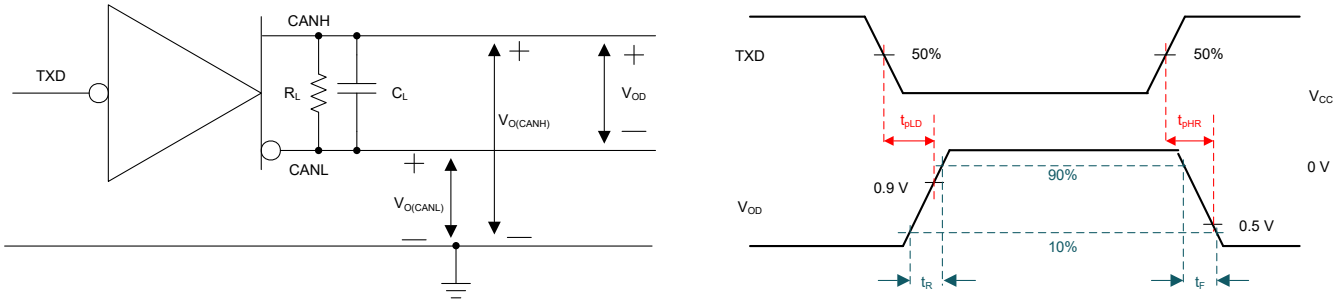


Figure 7-2. Driver Test Circuit and Measurement

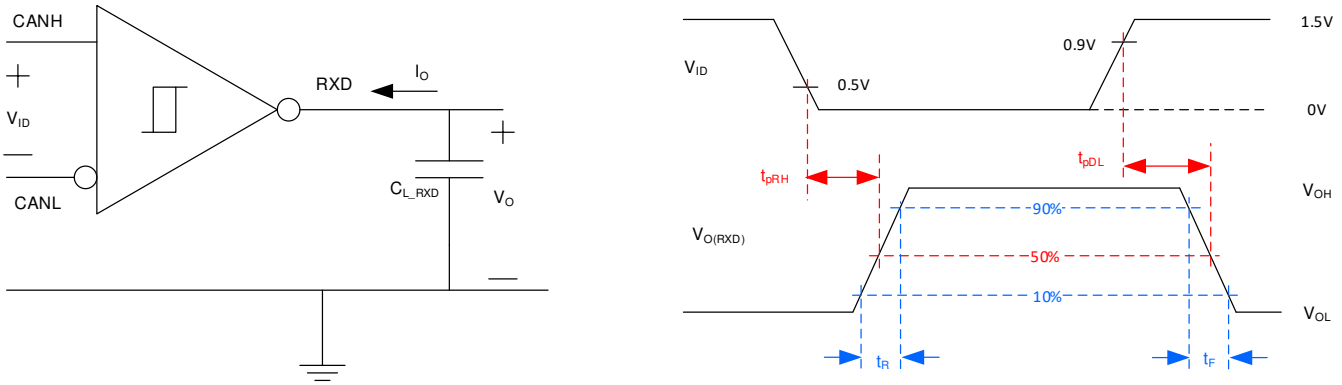


Figure 7-3. Receiver Test Circuit and Measurement

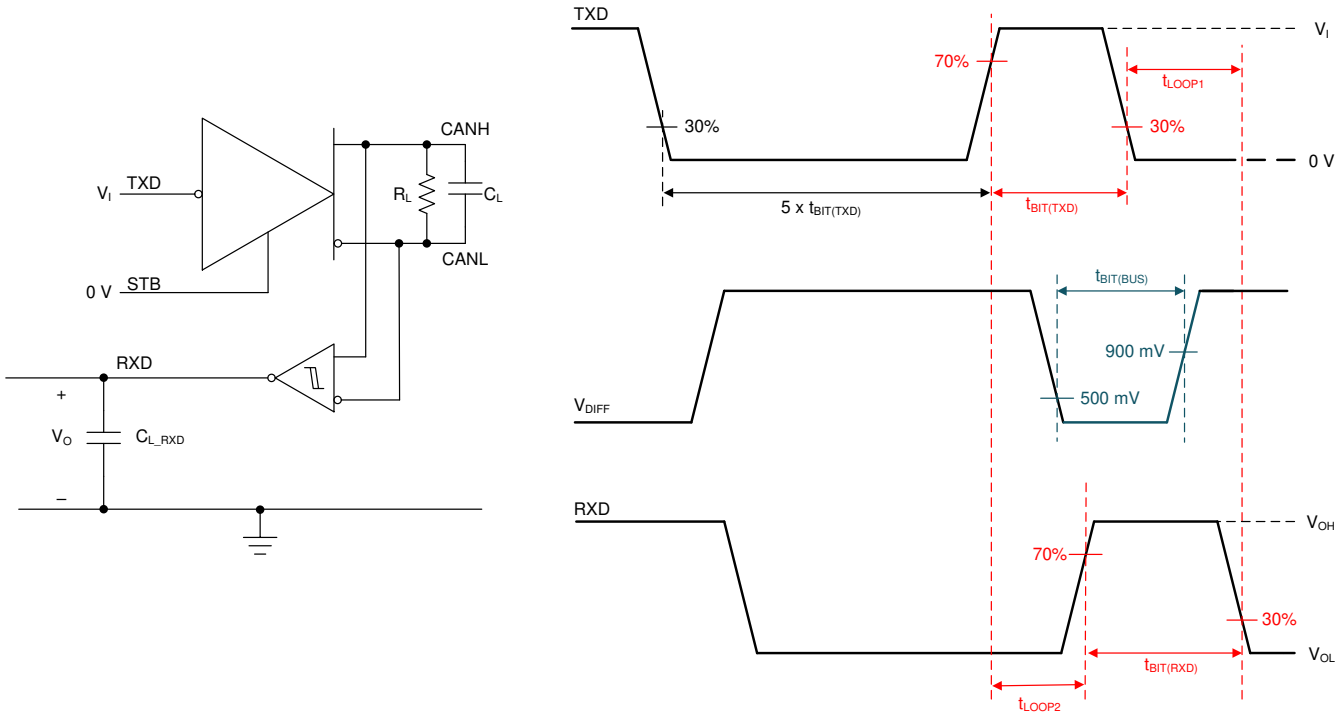


Figure 7-4. Transmitter and Receiver Timing Test Circuit and Measurement

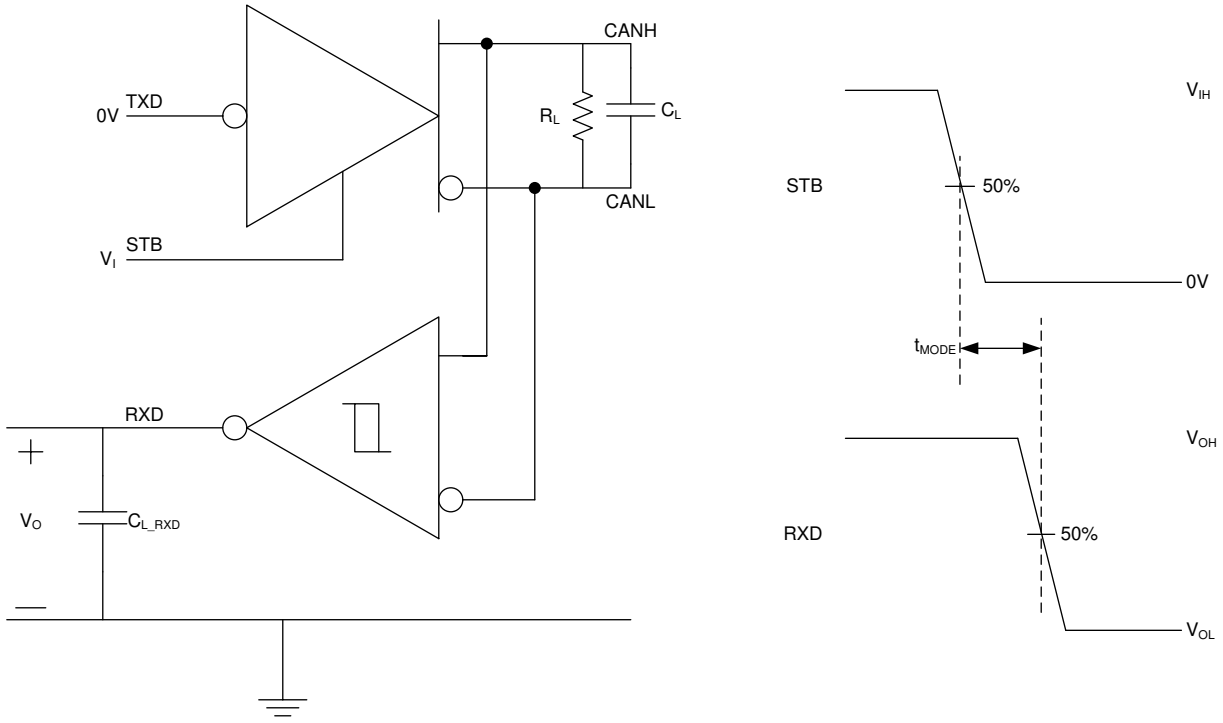


Figure 7-5. t_{MODE} Test Circuit and Measurement

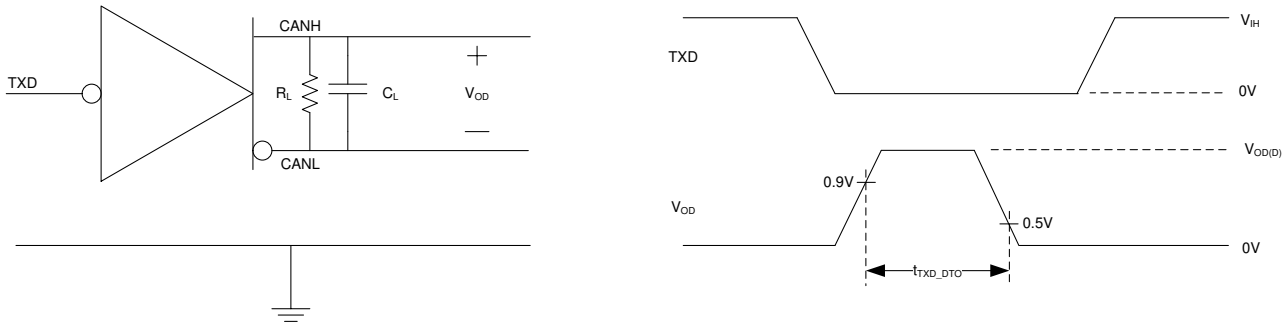


Figure 7-6. TXD Dominant Timeout Test Circuit and Measurement

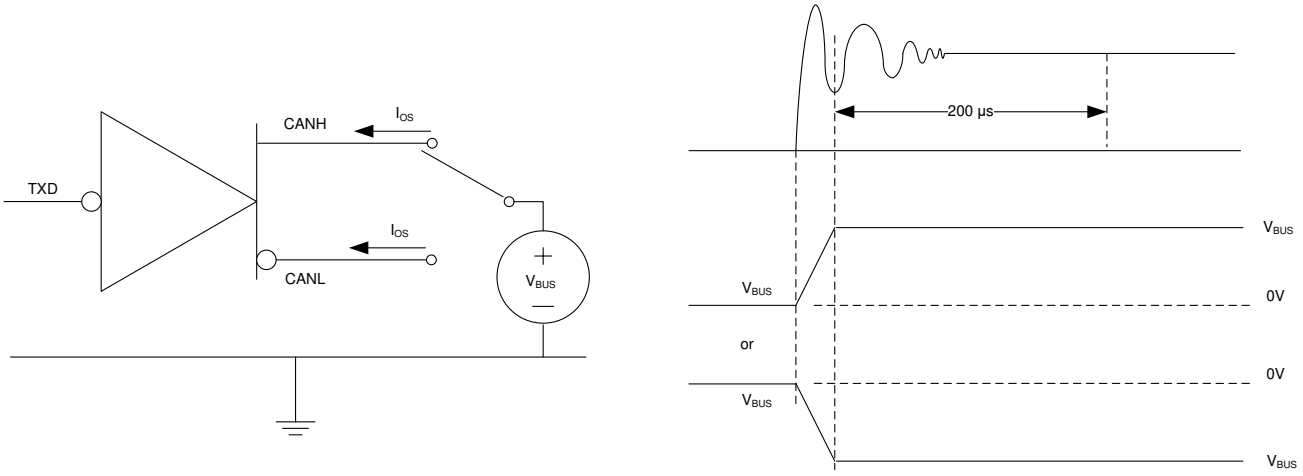


Figure 7-7. Driver Short-Circuit Current Test and Measurement

8 Detailed Description

8.1 Overview

The TCANC340x-Q1 devices are automotive EMC compliant 3.3V CAN FD transceivers. The devices are data rate agnostic making them backward compatible for supporting classical CAN applications while also supporting CAN FD networks up to 8Mbps. These devices have standby mode support which puts the transceiver in low current consumption mode. Upon receiving valid wake-up pattern on CAN bus, the device signals to the micro-controller through the RXD pin. The MCU can then place the device in normal mode using STB pin.

TCANC3404-Q1 supports ultra-low power shutdown mode where most of the internal blocks are disabled. This feature is optimized for battery-powered applications. TCANC3403-Q1 supports V_{IO} pin for low voltage logic level interface. The device can be interfaced to 1.8V, 2.5V or 3.3V micro controllers.

8.2 Functional Block Diagram

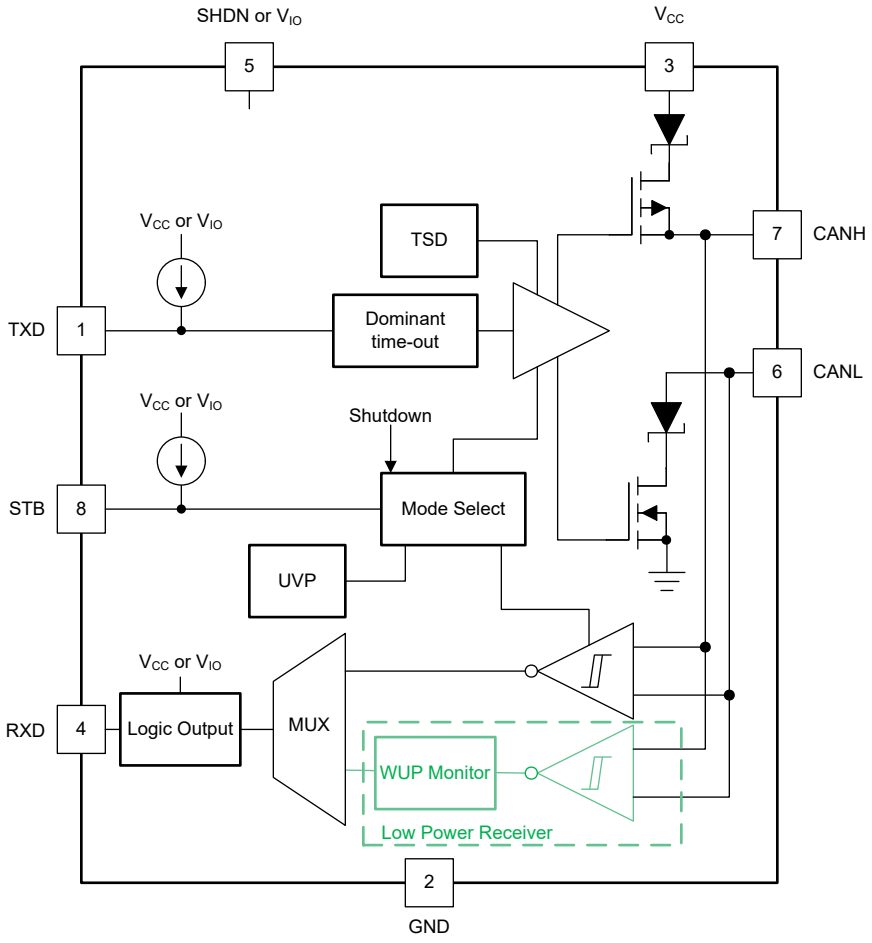


Figure 8-1. Block Diagram

8.3 Feature Description

8.3.1 Pin Description

8.3.1.1 TXD

The TXD input is a logic-level signal from a CAN controller to the transceiver. It is referenced to V_{CC} for TCAN3404-Q1 or to V_{IO} for TCAN3403-Q1 device.

8.3.1.2 GND

GND is the ground pin of the transceiver. The pin must be connected to the PCB ground.

8.3.1.3 V_{CC}

V_{CC} provides the 3.3 V power supply to the CAN transceiver.

8.3.1.4 RXD

The RXD output is a logic-level signal from the CAN transceiver to the CAN controller. It is referenced to V_{CC} for TCAN3404-Q1 and V_{IO} for TCAN3403-Q1. For TCAN3403-Q1, this pin is only driven once V_{IO} is present.

When a CAN bus wakeup event takes place, RXD is driven low

8.3.1.5 V_{IO} (TCAN3403-Q1 only)

The V_{IO} pin provides the digital I/O voltage to match the CAN controller voltage thus avoiding the requirement for a level shifter. It supports voltages from 1.7V to 3.6V providing a wide range of controller support.

8.3.1.6 CANH and CANL

The CANH and CANL pins are the CAN high and CAN low differential bus pins. These pins are internally connected to the CAN transmitter, receiver and the low-power wake-up receiver.

8.3.1.7 STB (Standby)

The STB pin is an input pin used for mode control of the transceiver. The STB pin can be supplied from either the system processor or from a static system voltage source. STB pin has default pull-up resistor on-chip. So if the pin is left floating or pulled high externally, device is in standby mode. If normal mode is the only intended mode of operation, the STB pin can be tied directly to GND.

8.3.1.8 SHDN (Shutdown)

The SHDN pin is only applicable to TCAN3404-Q1 and is used to put the device in ultra-low power mode. SHDN pin has an internal pull-down resistor on-chip, so if the pin is left floating, the device is in normal mode or standby mode depending on the state of STB pin. Pulling SHDN pin high externally puts the device in shutdown. All blocks (including low power wakeup receiver) are disabled in this mode. SHDN pin has higher priority compared to STB pin.

8.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 8-2 and Figure 8-3.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to roughly $V_{CC}/2$ via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCANC340x-Q1 transceivers implement a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 8-2 and Figure 8-3.

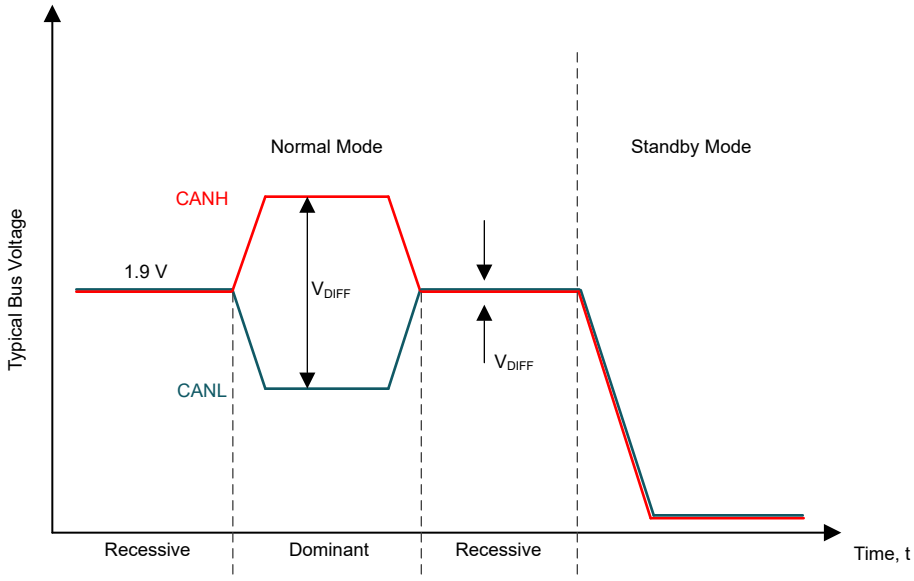
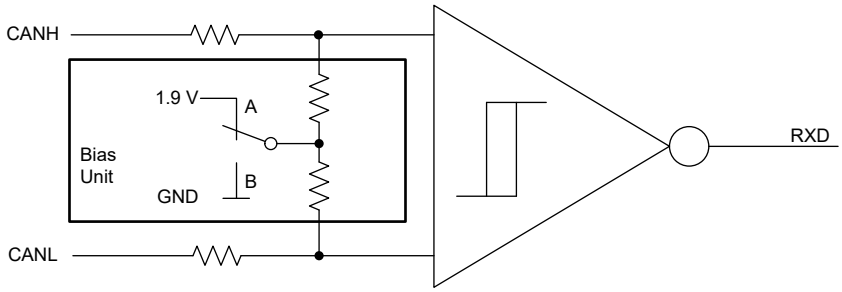


Figure 8-2. Bus States



A - Normal Mode B - Standby Mode

Figure 8-3. Simplified Recessive Common Mode Bias Unit and Receiver

8.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin; thus, clearing the dominant time out. The receiver remains active and biased to approximately 1.9V and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using Equation 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2\text{ms} = 9.2\text{kbps} \quad (1)$$

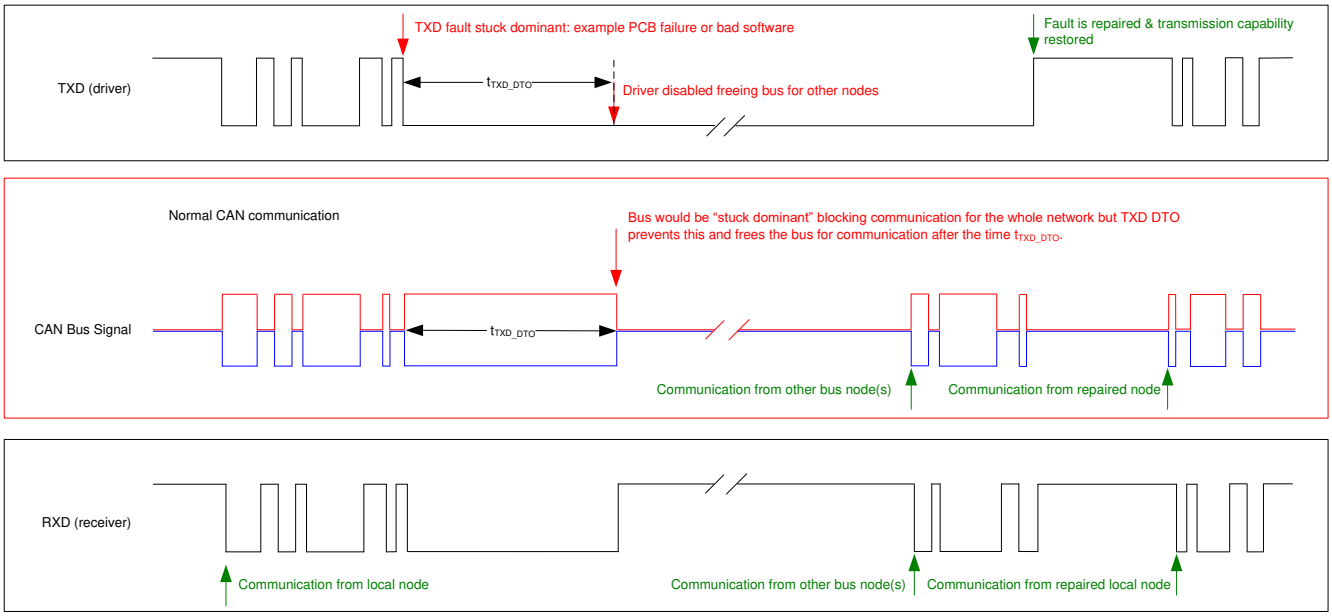


Figure 8-4. Example Timing Diagram for TXD Dominant Timeout

8.3.4 CAN Bus short-circuit current limiting

The devices have several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common-mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. making sure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and the respective short-circuit currents. The average short-circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%\ \text{Transmit} \times [(\%\ \text{REC\_Bits} \times I_{OS(SS)\_REC}) + (\%\ \text{DOM\_Bits} \times I_{OS(SS)\_DOM})] + [\%\ \text{Receive} \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short-circuit current

This short circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

8.3.5 Thermal Shutdown (TSD)

If the junction temperature of the devices exceed the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to approximately 1.9V

during a TSD fault and the receiver to RXD path remains operational. The TCANC340x-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

8.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

Table 8-1. Undervoltage Lockout - TCAN3404-Q1

V_{CC}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	Normal if STB = GND and SHDN = GND	Per TXD	Mirrors bus
> UV_{VCC}	Standby mode if STB = High and SHDN = GND	Weak biased to GND	V_{CC}, Remote wake request See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode
> UV_{VCC}	Shutdown mode if SHDN = High	Weak biased to GND	V_{CC}
< UV_{VCC}	Protected	High impedance	High impedance

Table 8-2. Undervoltage Lockout - TCAN3403-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	STB = High: Standby Mode	Weak biased to GND	V_{IO}: Remote wake request See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode
		STB =Low: Protected Mode	High impedance	Recessive
> UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance
< UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance

Once the undervoltage condition is cleared, and t_{MODE} or t_{SHDN2} has expired, the TCANC340x-Q1 transitions to normal mode and the host controller can again send and receive CAN traffic.

8.3.7 Unpowered Device

For unpowered condition, the TCANC340x-Q1 is designed to be a passive or no load to the CAN bus. This is because the bus pins were designed to have low leakage currents to not load the bus. This design consideration is critical if some nodes of the network are unpowered while the rest of the network remains operational.

For unpowered scenario, the logic pins also have low leakage currents. The pins do not load other circuits which may remain powered.

8.3.8 Floating pins

The TCANC340x-Q1 devices have internal pull-up/pull-down resistors on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This makes sure the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See Table 8-3 for details on pin bias conditions.

Table 8-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD towards recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB towards low-power standby mode to prevent excessive system power

Table 8-3. Pin Bias (continued)

Pin	Pull-up or Pull-down	Comment
SHDN	Pull-down	Weakly biases SHDN towards normal mode to allow normal communication. SHDN pin has higher priority than STB for TCAN3404.

8.4 Device Functional Modes

8.4.1 Operating Modes

The TCAN340x-Q1 has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB pin. TCAN3404-Q1 has a third mode: shutdown activated through SHDN pin. Pulling SHDN pin high disables most internal blocks and puts the device in lowest power consumption mode.

Table 8-4. Operating Modes for STB pin

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

8.4.2 Normal Mode

This is the normal operating mode of the TCAN340x-Q1. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

8.4.3 Standby Mode

This is the low-power mode of the TCAN340x-Q1. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD as shown in Figure 8-5. The local CAN protocol controller should monitor RXD for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB pin low. The CAN bus pins are weakly pulled to GND in this mode; see Figure 8-2 and Figure 8-3.

For TCAN3403-Q1 in standby mode, only the V_{IO} supply is required; therefore, the V_{CC} may be switched off for additional system level current savings.

8.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN340x-Q1 devices support a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the device.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than

$t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP; therefore, a wake request is always generated. See Figure 8-5 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake-up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500kbps, or two back-to-back bit times at 1Mbps triggers the filter in either bus state. Any CAN frame at 500kbps or less would contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in the current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 8-5 for the timing diagram of the wake-up pattern with wake timeout feature.

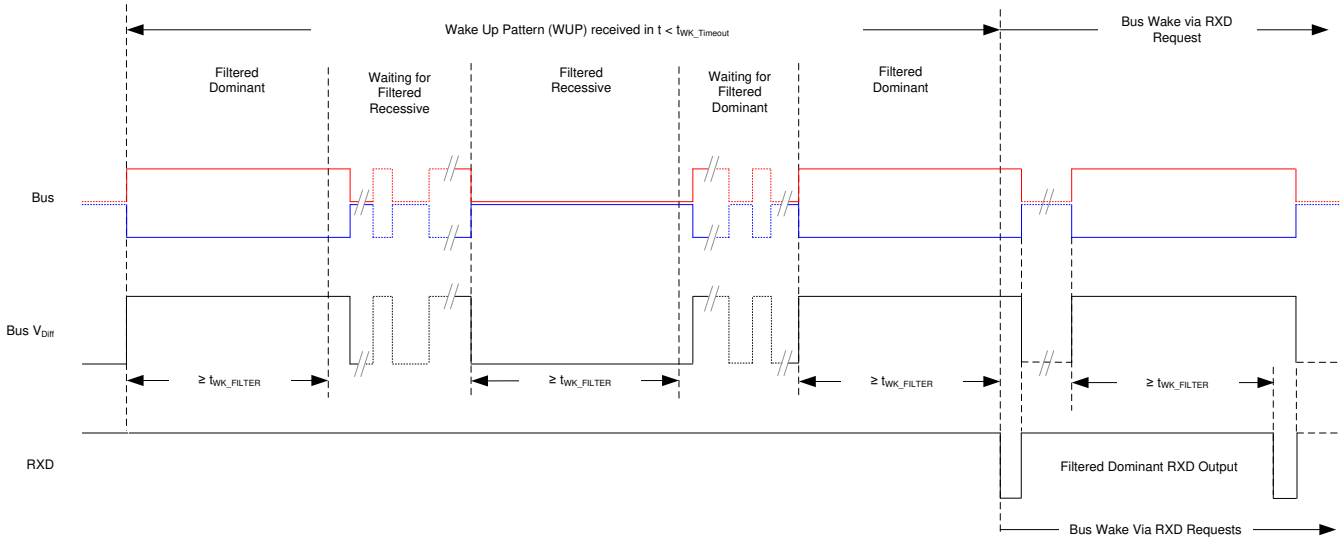


Figure 8-5. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$

8.4.4 Shutdown Mode

This is the lowest power state of TCAN3404-Q1. All internal blocks including CAN driver, main receiver and low power wake-up receiver are switched off and bi-directional CAN communication is not possible. Wakeup over CAN bus is also not possible in this mode. CAN bus pins are weakly biased towards GND and RXD is high in this state,

8.4.5 Driver and Receiver Function

The TCAN340x-Q1 logic I/Os support CMOS levels with respect to either V_{CC} for 3.3V systems (TCAN3404-Q1) or V_{IO} (TCAN3403-Q1) for compatibility with MCUs that support 1.8V, 2.5V, or 3.3V systems.

Table 8-5. Driver Function Table

Device Mode	TXD Input(1)	Bus Outputs		Driven Bus State(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Standby	X	High impedance	High impedance	Biased to ground
Shutdown	X	High impedance	High impedance	Biased to ground

(1) X = irrelevant
(2) For bus state and bias see Figure 8-2 and Figure 8-3

Table 8-6. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} – V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	High
Standby	$V_{ID} \geq 1.15V$	Dominant	High Low if a remote wake event occurred See Figure 8-5
	$0.4V < V_{ID} < 1.15V$	Undefined	
	$V_{ID} \leq 0.4V$	Recessive	
Any	Open ($V_{ID} \approx 0V$)	Open	High

9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

The TCANC340x-Q1 transceiver can be used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. Figure 9-1 shows a typical configuration for 3.3V controller applications. The bus termination is shown for illustrative purposes.

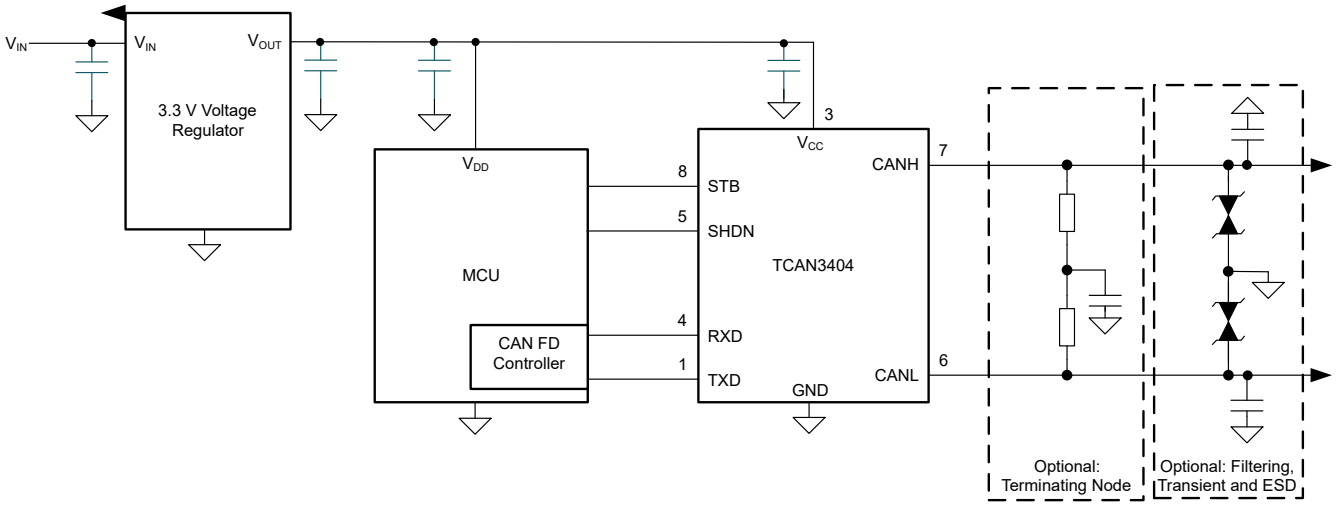


Figure 9-1. Transceiver Application Using 3.3V I/O Connections

9.2.1 Design Requirements

9.2.1.1 CAN Termination

Termination may be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination can be used, see Figure 9-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

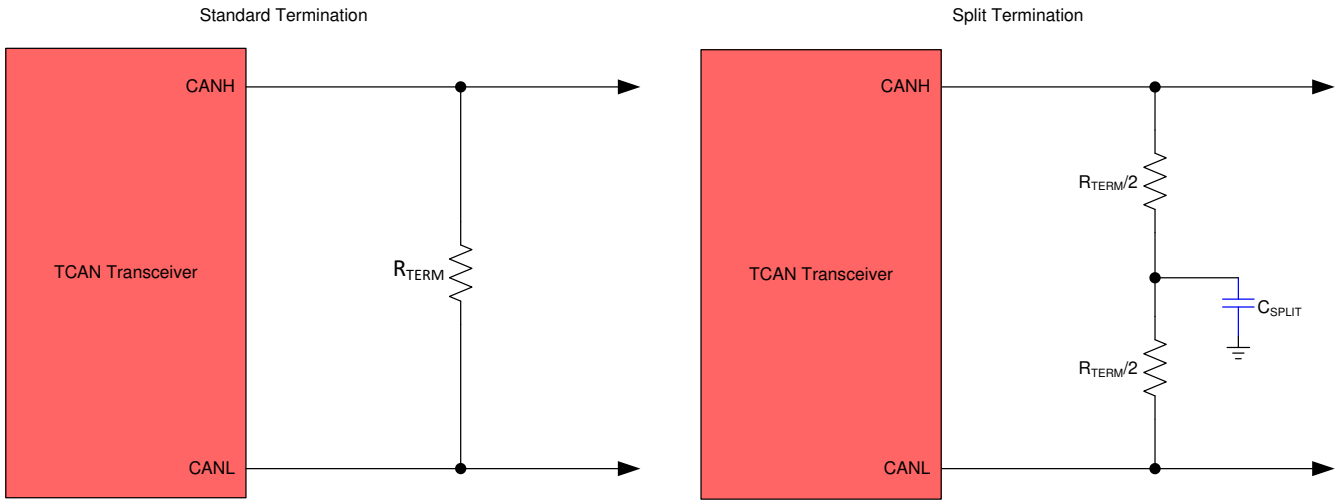


Figure 9-2. CAN Bus Termination Concepts

9.2.2 Detailed Design Procedures

9.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN340x-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. There are many system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification, the driver differential output is specified with a bus load that can range from 50Ω to 65Ω where the differential output must be greater than 1.5V. The TCANC340x-Q1 family is specified to meet the 1.5V requirement down to 50Ω and is specified to meet 1.4V differential output at 45-Ω bus load. The differential input resistance of the TCANC340x-Q1 is a minimum of 22kΩ. If 55 TCANC340x-Q1 transceivers are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60-Ω bus termination which gives a total bus load of approximately 52Ω. Therefore, the TCAN340x-Q1 family theoretically supports over 50 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets, and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design for robust network operation.

See the application report SLLA270: Controller Area Network Physical layer requirements. This document discusses in detail all system design physical layer parameters.

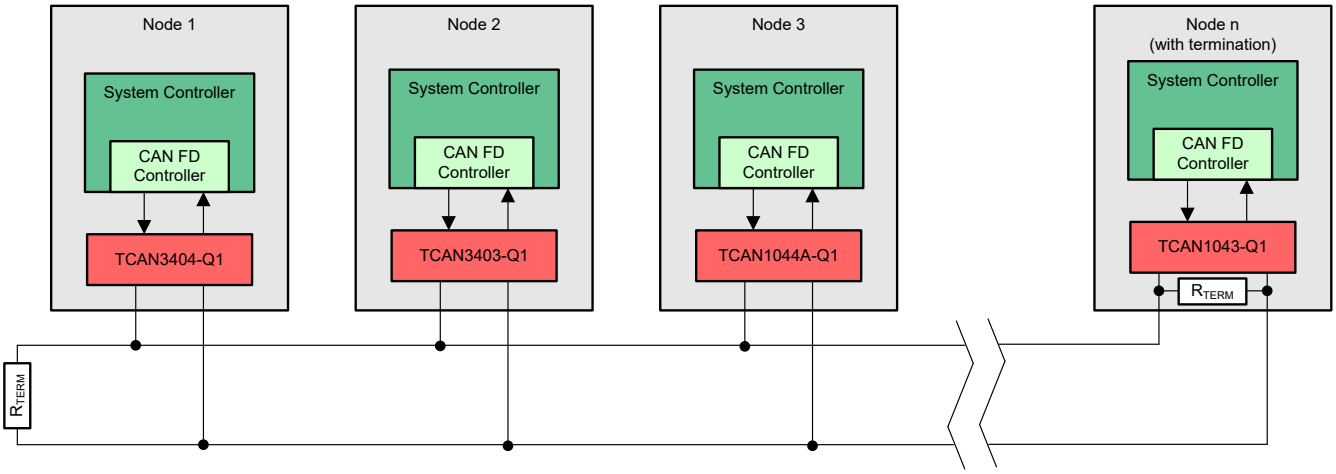
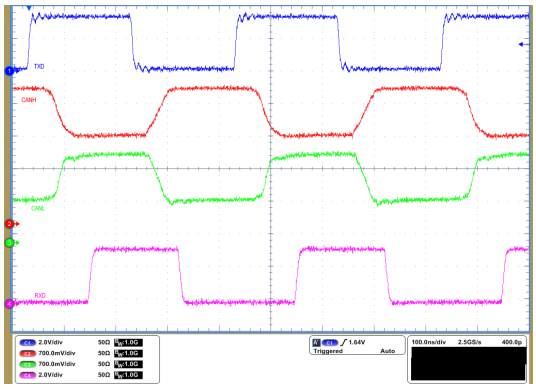


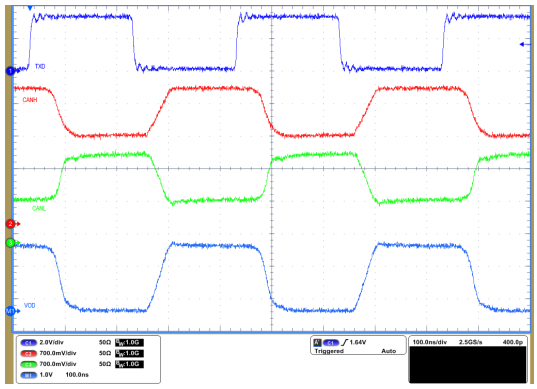
Figure 9-3. Typical CAN Bus

9.2.3 Application Curves



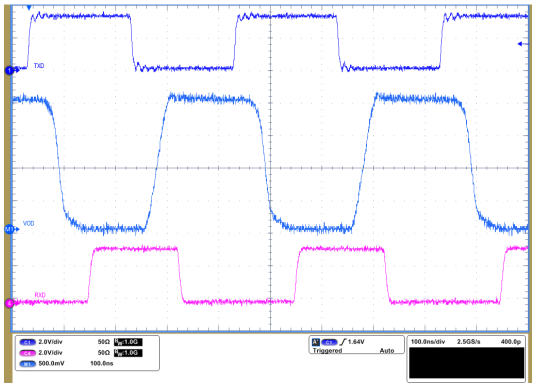
V_{CC} = 3.3V V_{IO} = 3.3V R_L = 60Ω

Figure 9-4. TXD_CANH_CANL_RXD waveforms for 60Ω load at 5Mbps toggling



V_{CC} = 3.3V V_{IO} = 3.3V R_L = 60Ω

Figure 9-5. TXD_CANH_CANL_Vod waveforms for 60Ω load at 5Mbps toggling



V_{CC} = 3.3V V_{IO} = 3.3V R_L = 60Ω

Figure 9-6. TXD_Vod_RXD waveforms for 60Ω load at 5Mbps toggling

9.3 System Examples

The TCANC340x-Q1 CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 1.8V or 2.5V application is shown in Figure 9-7. The bus termination is shown for illustrative purposes.

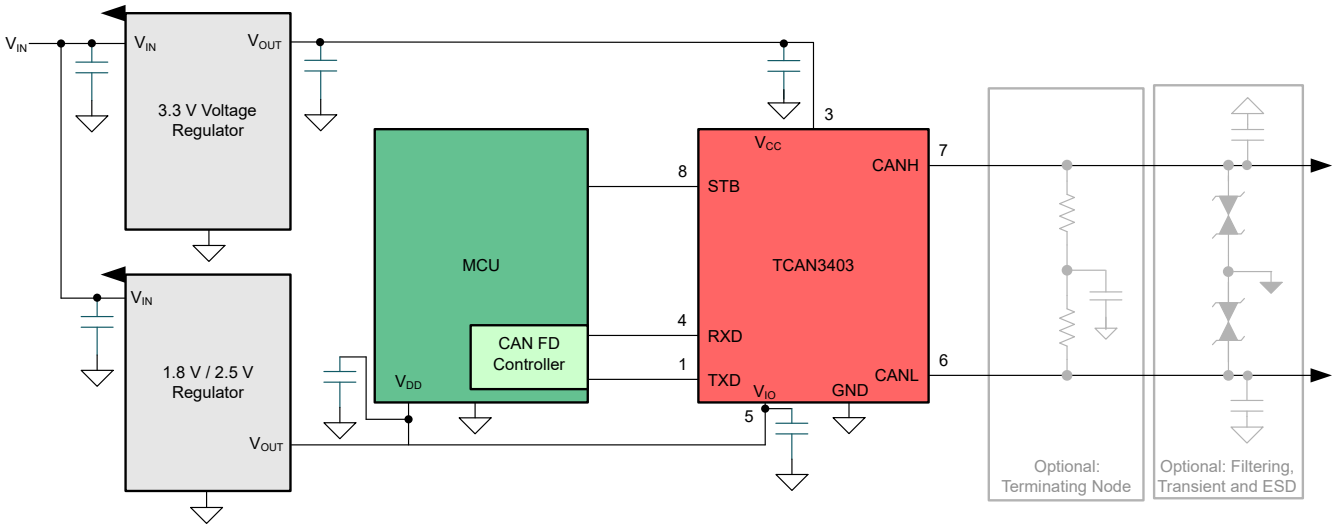


Figure 9-7. Typical Transceiver Application Using 1.8V, 2.5V I/O Connections

9.3.1 ISO 11898-2 Compatibility of TCAN340x-Q1 Family of 3.3V CAN Transceivers

9.3.1.1 Introduction

Many users value the low power consumption of operating their CAN transceivers from a 3.3V supply. However, some are concerned about the interoperability with 5V supplied transceivers on the same bus. This section tries to address those concerns.

9.3.1.2 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single ended logic level output signal.

The CAN driver creates the differential voltage between CANH and CANL in the dominant state. The dominant differential output of the TCANC340x-Q1 is greater than 1.5V and less than 3V across a 60Ω load as defined by the ISO 11898-2 standard. These are the same limiting values for 5V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state when less than 500mV of differential voltage exists on the bus, and a dominant state when more than 900mV of differential voltage exists on the bus. The CAN receiver must do this with common-mode input voltages from –12V to 12V. The TCANC340x-Q1 device receivers meet and exceed these receiver input specifications.

9.3.1.3 Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. The TCAN340x-Q1 family has the recessive bias voltage set to 1.9V. This is intentional to match the common mode of recessive output with the common mode of dominant output signal from TCAN340x-Q1. Furthermore, TCAN340x-Q1 has special design techniques for optimum EMC performance in a heterogeneous bus consisting of TCAN340x-Q1 and 5V CAN transceivers.

9.3.1.4 Interoperability of 3.3V CAN in 5V CAN Systems

The 3.3V supplied TCAN340x-Q1 family of CAN transceivers are fully compatible with 5V CAN transceivers. The minimum differential output voltage is the same, and the receivers have the same input threshold specifications. The only difference is in the recessive common mode output voltage which is little lower for 3.3V CAN transceiver than 5V supplied transceiver. But this does not impact regular functionality. Furthermore, special design techniques in TCAN340x-Q1 provide optimum EMC performance in heterogeneous network consisting of TCAN340x-Q1 and 5V supplied CAN transceivers on same CAN bus.

9.4 Power Supply Recommendations

The TCAN3404-Q1 transceiver is designed to operate with a main V_{CC} input voltage supply range between 3V and 3.6V.

The TCAN3403-Q1 implements an I/O level shifting supply input, V_{IO}, designed for a range between 1.8V and 3.6V.

Both the V_{CC} and V_{IO} inputs must be well regulated. In addition to the power supply filtering, a decoupling capacitance, typically 100nF, should be placed near the CAN transceiver main V_{CC} and V_{IO} supply pins.

9.5 Layout

Robust and reliable CAN node designs may require special layout techniques depending on the application and design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

9.5.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows a optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

Note

High-frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R2 and R3, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. See CAN Termination, CAN Bus short-circuit limiting, and Equation 2 for information on termination concepts and power ratings needed for the termination resistor(s).

9.5.2 Layout Example

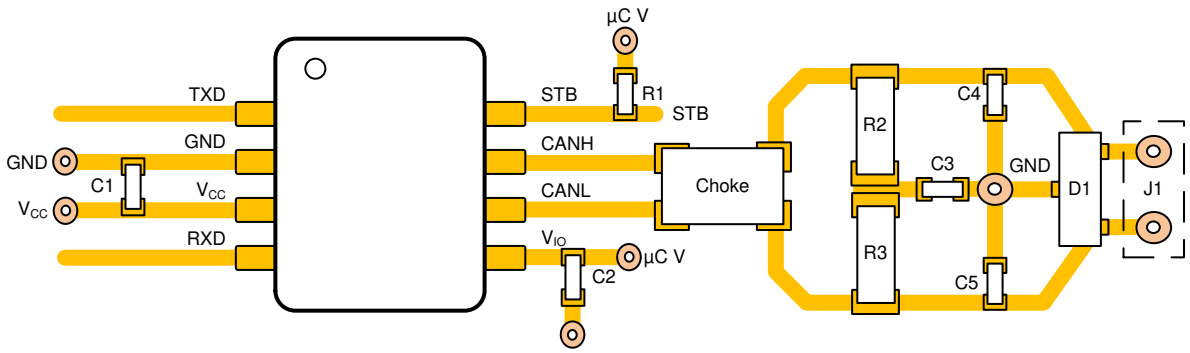


Figure 9-8. Layout Example

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2022) to Revision A (June 2024)	Page
• Changed the document status from *Advanced Information* to *Production* data	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN3403DDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2THF
TCAN3403DDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2THF
TCAN3403DRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	3403
TCAN3403DRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	3403
TCAN3403DRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	3403
TCAN3403DRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	3403
TCAN3404DDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2TIF
TCAN3404DDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2TIF
TCAN3404DRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	3404
TCAN3404DRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	3404
TCAN3404DRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	3404
TCAN3404DRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	3404

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

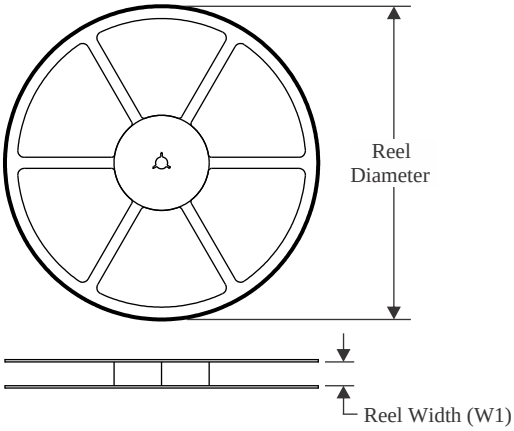
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

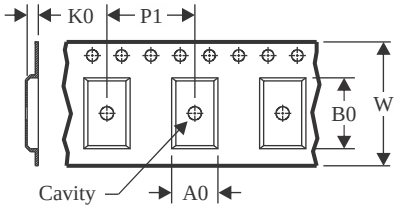
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

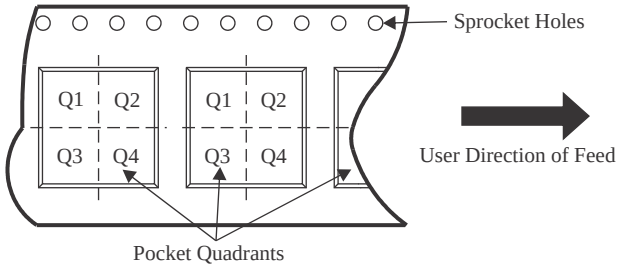


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

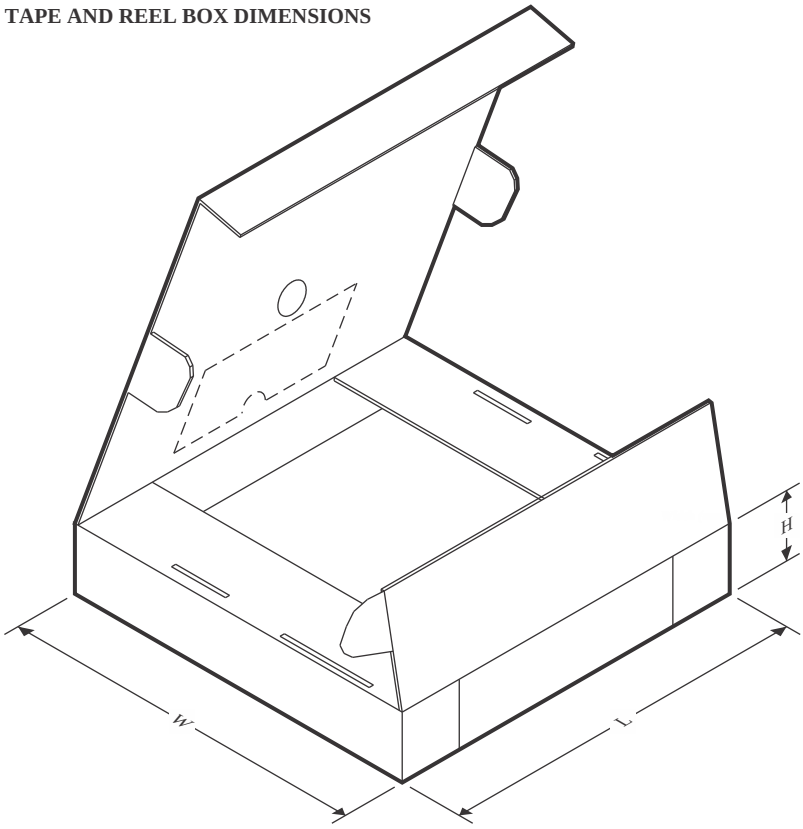
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN3403DDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCAN3403DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN3403DRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCAN3404DDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCAN3404DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN3404DRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

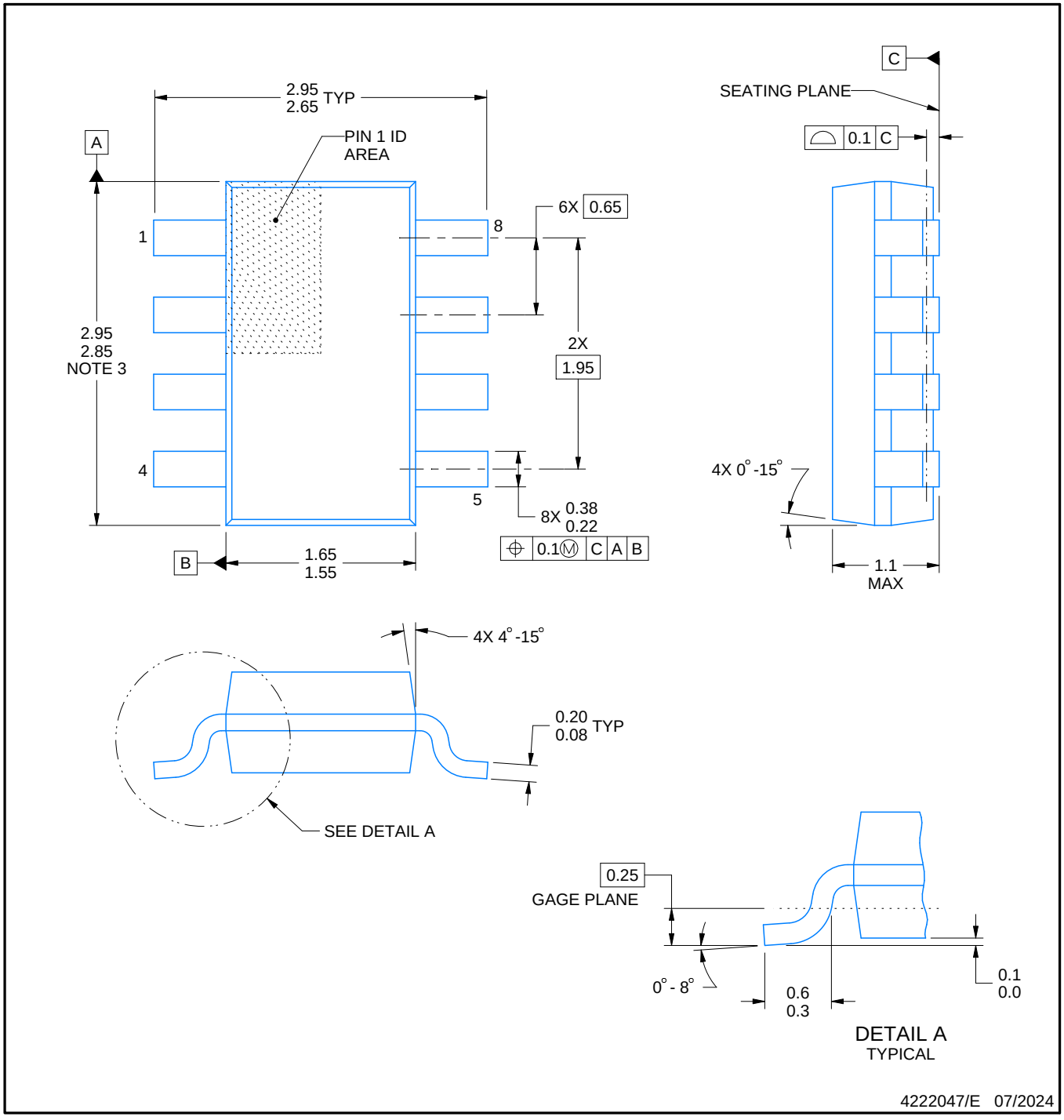
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN3403DDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCAN3403DRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN3403DRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TCAN3404DDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCAN3404DRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN3404DRQ1	SOIC	D	8	2500	340.5	338.1	20.6

PACKAGE OUTLINE

DDF0008A

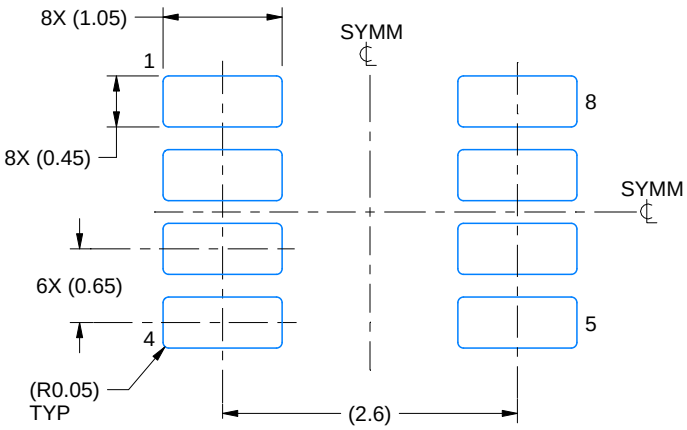
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

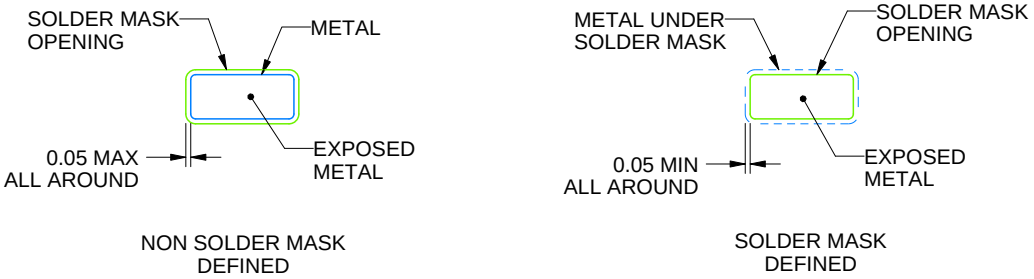


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

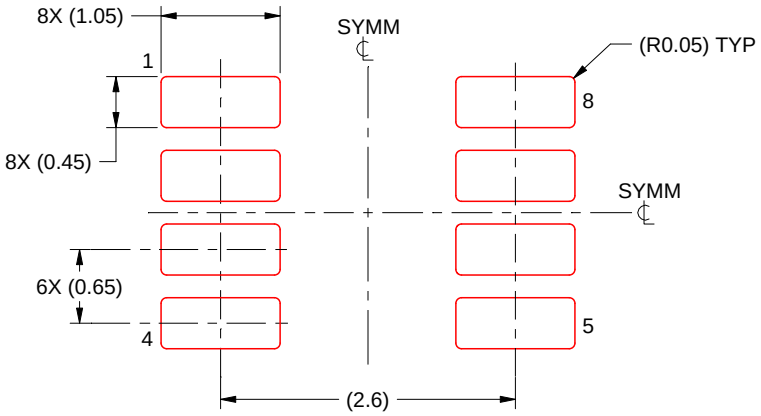
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

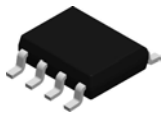


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

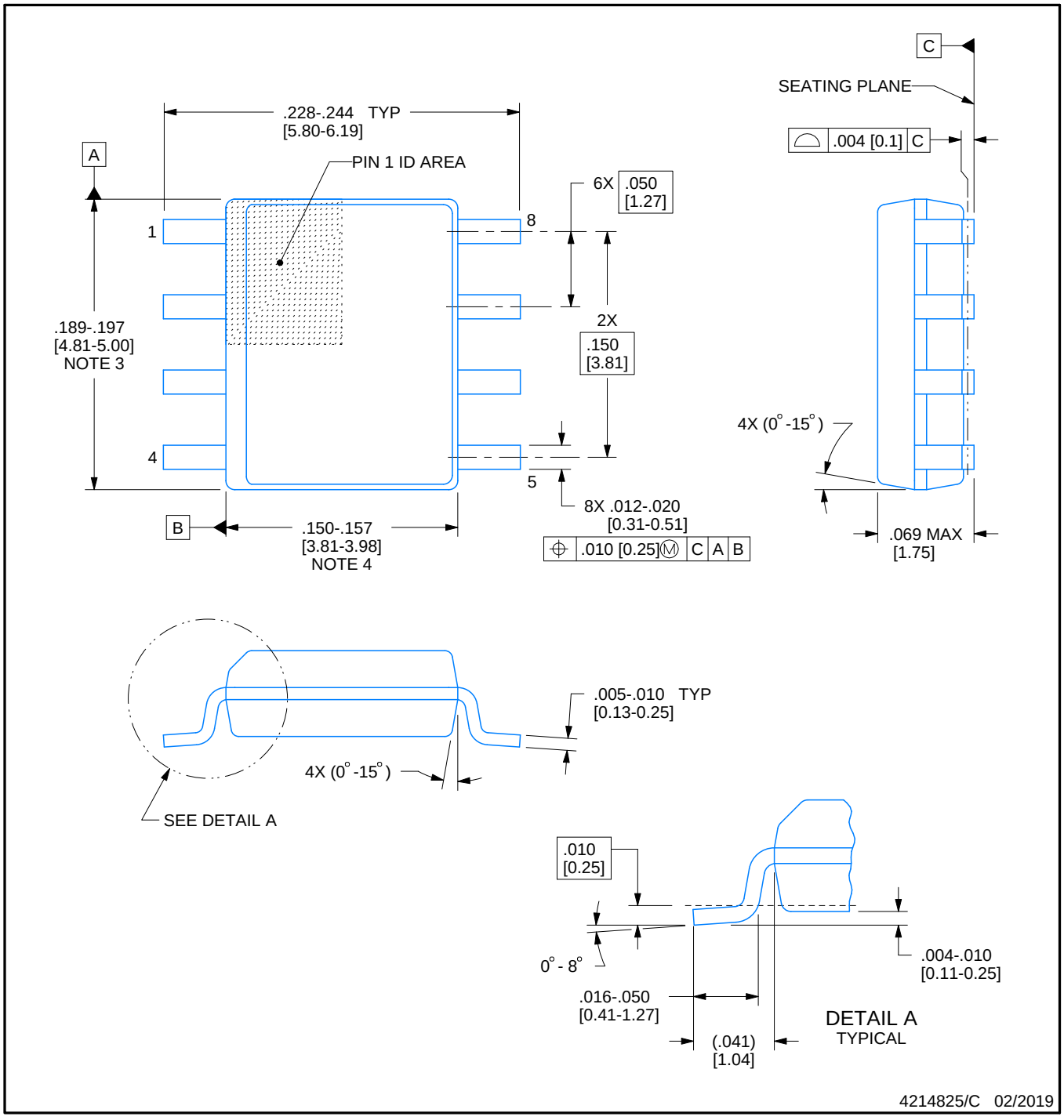


PACKAGE OUTLINE

D0008A

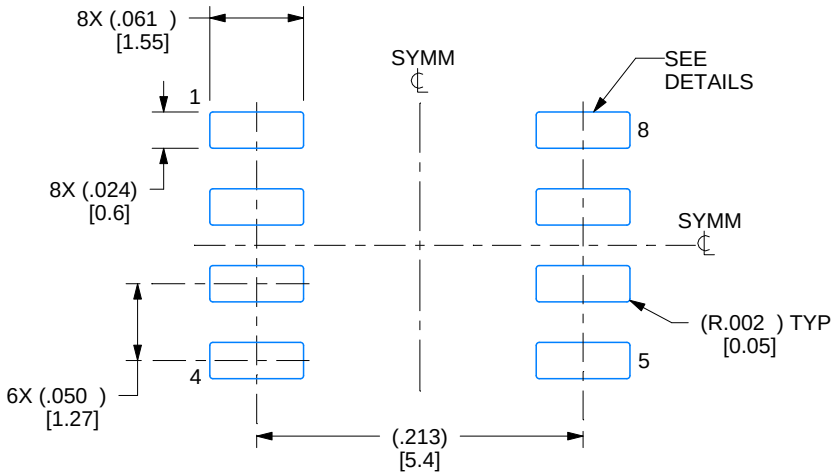
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

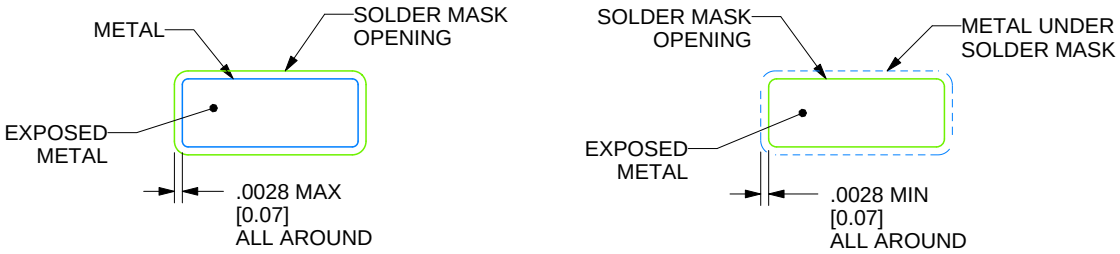


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

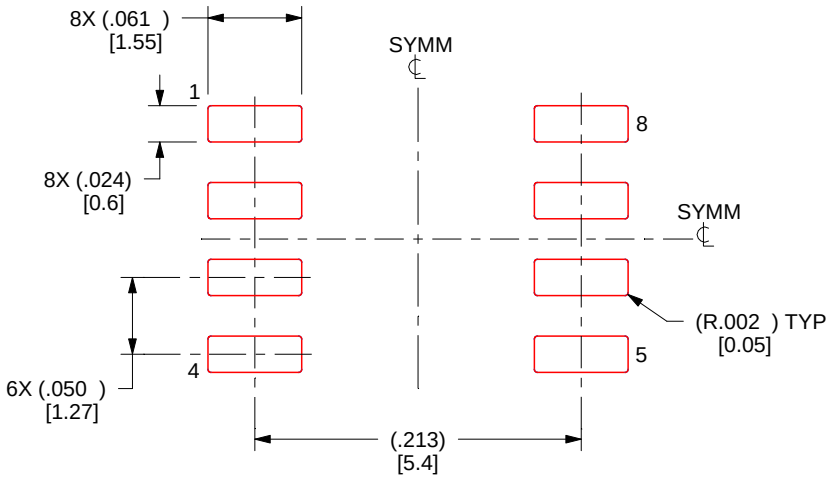
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

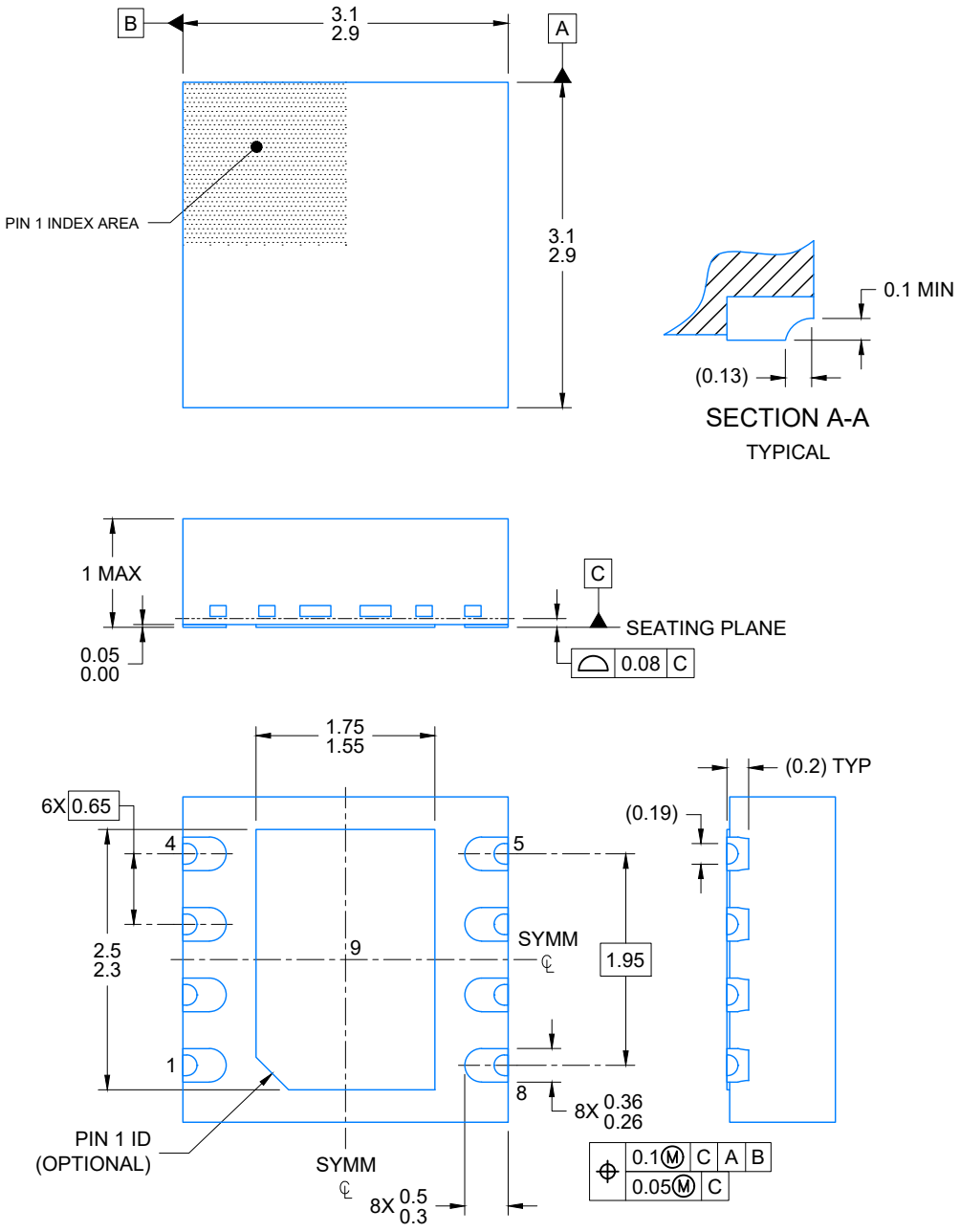
4203482/L

PACKAGE OUTLINE

DRB0008J

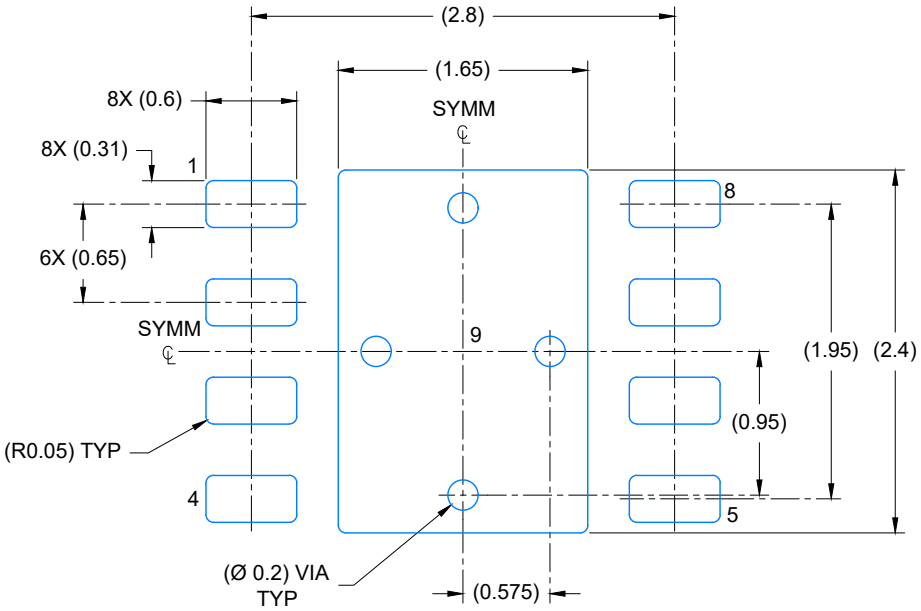
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

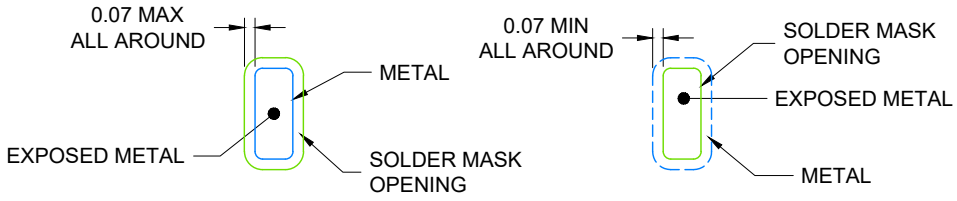


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

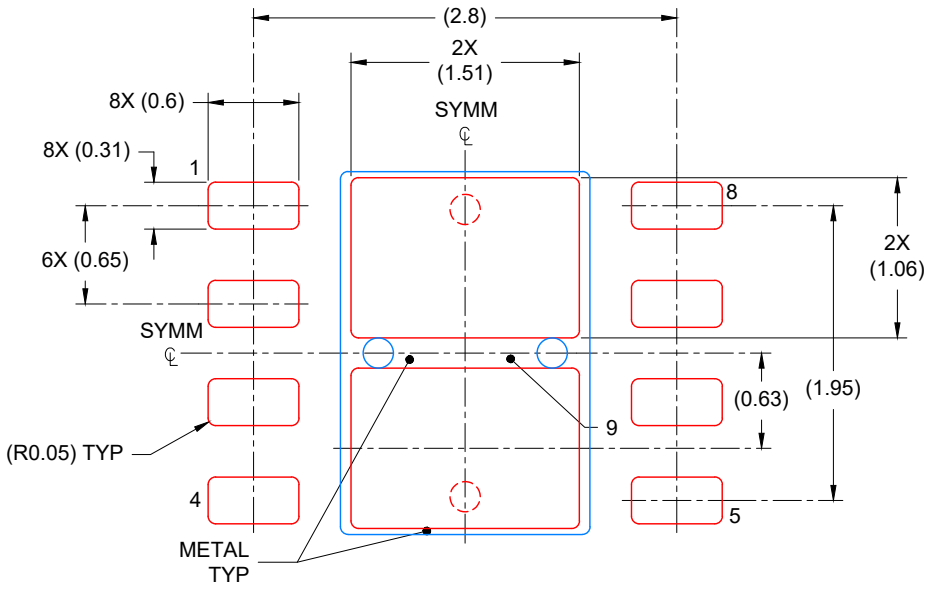
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265