TCAN157x-Q1 Automotive Enhanced CAN FD SIC Transceiver with Partial Networking

1 Features

- AEC-Q100 (Grade 1): Qualified for automotive applications
- Meets requirements for ISO 11898-2:2024 Annex A standard for CAN with Signal Improvement Capability for 2Mbps and 5Mbps communication
- CAN FD communication rates up to 8Mbps
- Supports selective wake or partial networking while transmitting and receiving error-free classic CAN or CAN FD data
- Functional Safety Quality-Managed: TCAN1576-Q1
- Functional Safety-Capable: TCAN1575-Q1
- The TCAN157x-Q1 supports nominal processor IO voltages from 1.8V to 5V
- Wide operating range:
  - ±58V Bus fault protection
  - ±12V Common mode
- TCAN1576-Q1 supports:
  - Watchdog: Timeout, Window and Q&A
  - Bus fault diagnostics and reporting
  - Programmable INH/LIMP pin
- 14-Pin SOIC, VSON and SOT23 packages
  - VSON package with improved automated optical inspection (AOI) capability

2 Applications

- Body electronics and lighting
- Automotive infotainment and cluster
- Hybrid, electric and powertrain systems
- Industrial transportation

3 Description

The TCAN157x-Q1 are enhanced high-speed, CAN FD SIC transceivers that meet the physical layer requirements of the ISO 11898-2:2024 (Annex A) for a high-speed CAN SIC specification supporting data rates up to 8Mbps. The devices are configured using SPI for access to full functionality. They support nominal processor IO voltages from 1.8V to 5V using the corresponding voltage on V_{IO}, allowing the use of lower power processors.

These transceivers support selective wake (being able to wake-up based on WUF identification). The feature enables systems to implement partial networking and operate with a reduced number of nodes in an active state while the remaining nodes are in a low-power sleep mode. The transceivers and selective wake function meet the specifications of the ISO 11898-2:2024 standard.

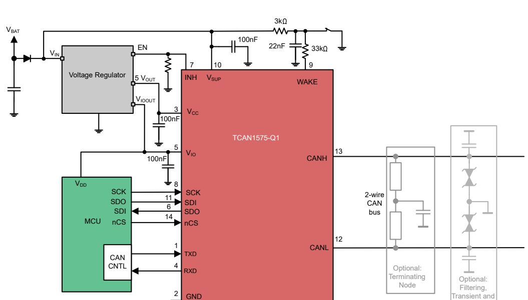
The TCAN1576-Q1 is a full-featured device supporting watchdog and advanced bus diagnostics. For ease of debug, the advanced bus fault diagnostics and communication feature is used to determine specific bus faults.

The TCAN157x-Q1 are register compatible within the family and with TCAN1145-Q1 and TCAN1146-Q1 CAN FD Partial Networking transceivers. The TCAN157x-Q1 provides system designers the flexibility to implement features without hardware modifications, and with minimal software changes. The TCAN1576-Q1 inhibit (INH) pin is used to either enable node power or to be configured as a limp home pin when a watchdog error takes place.

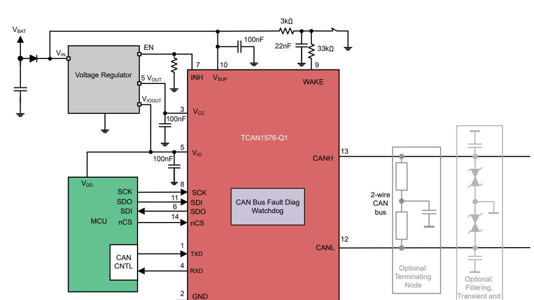
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAN1575-Q1 TCAN1576-Q1	SOIC (D, 14)	8.65mm x 3.9mm
	VSON (DMT, 14)	4.5mm x 3mm
	SOT23 (DYY, 14)	4.2mm x 2mm

(1) For more information, see Section 13.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematics



Simplified Schematics

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4 Device Comparison Table

Device Number	CAN FD SIC Transceiver	Selective Wake	Watchdog	Bus Fault Diagnostics	Limp Home Capable	SOIC	VSON	SOT
TCAN1575D-Q1	X	X				X		
TCAN1575DMT-Q1	X	X					X	
TCAN1575DYY-Q1	X	X						X
TCAN1576D-Q1	X	X	X	X	X	X		
TCAN1576DMT-Q1	X	X	X	X	X		X	
TCAN1576DYY-Q1	X	X	X	X	X			X

5 Pin Configuration and Functions

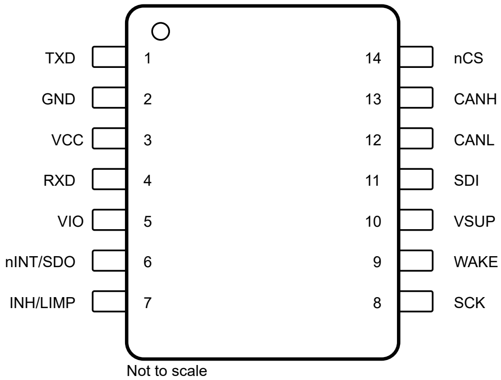


Figure 5-1. D Package, 14 Pin (SOIC), Top View

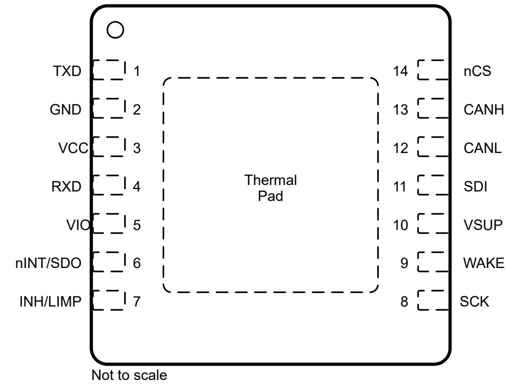


Figure 5-2. DMT Package, 14 Pin (VSON), Top View

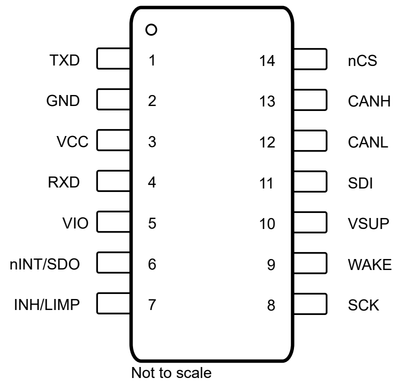


Figure 5-3. DYY Package, 14 Pin (SOT-23), Top View

Table 5-1. Pin Functions

PIN		TYPE[2]	DESCRIPTION
NO.	NAME		
1	TXD	DI	CAN transmit data input (low for dominant and high for recessive bus states)
2	GND	GND	Ground connection[1]
3	V_{CC}	P	5V CAN bus supply voltage
4	RXD	DO	CAN receive data output (low for dominant and high for recessive bus states)
5	VIO	P	Digital I/O voltage supply
6	nINT/SDO	DO	Serial data output when nCS is low and nINT when nCS is high
7	INH/LIMP	HVO	Defaults to Inhibit pin to control system voltage regulators and supplies. TCAN1576-Q1 can configure this pin for a LIMP home function
8	SCK	DI	SPI clock input
9	WAKE	HVI	Local wake input terminal
10	VSUP	HVP	High-voltage supply from the battery
11	SDI	DI	Serial data input
12	CANL	BI/O	Low level CAN bus I/O line
13	CANH	BI/O	High level CAN bus I/O line
14	nCS	DI	Chip select (active low)

(1) GND pin is soldered to GND, and the recommendation is the pad for DMT package is soldered to the ground plane for thermal relief
(2) DI = digital input, DO = digital output, HVI = high voltage input, HVO = high voltage output, HVP = high voltage power, P = power, BI/O = bus input/output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{SUP}	Device Supply voltage	–0.3	42	V
V_{CC}	CAN Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN bus I/O voltage (CANH, CANL)	–58	58	V
V_{DIFF}	CAN bus differential voltage (V_{DIFF} = V_{CANH} - V_{CANL})	–58	58	V
V_{WAKE}	WAKE input voltage	–18	42	V
V_{INH}	INH pin voltage	–0.3	42 and VO ≤ VSUP+0.3	V
V_{LOGIC}	Logic pin voltage (RXD, TXD, SPI)	–0.3	6	V
$I_{O(LOGIC)}$	Logic pin output current (RXD, SDO)		4	mA
$I_{O(INH/LIMP)}$	Inhibit/ILIMP pin output current		6	mA
$I_{O(WAKE)}$	WAKE pin output current		3	mA
T_J	Junction temperature	–40	165	°C
T_{stg}	Storage temperature	–65	150	°C

(1) *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) Classification Level H2, V_{SUP}, CANL/H, and WAKE, per AEC Q100-002[(1)]		±8000	V
		Human body model (HBM) Classification Level 3A, all other pins, per AEC Q100-002[(1)]		±4000	
		Charged device model (CDM) Classification Level C5, per AEC Q100-011	Corner pins (1, 7, 8, and 14)	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage	4.5		28	V
V_{IO}	I/O supply voltage	1.71		5.5	V
V_{CC}	CAN transceiver supply voltage	4.75		5.25	V
$I_{OH(DO)}$	Digital output high level current	–2			mA
$I_{OL(DO)}$	Digital output low level current			2	mA
$I_{O(INH/LIMP)}$	Inhibit/LIMP pin current			1	mA
T_J	Junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TCAN157x-Q1			UNIT
		D (SOIC)	DMT (VSON)	DYY(SOT-23)	
		14-PINS	14-PINS	14-PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	82.6	37.5	91.8	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		TCAN157x-Q1 D (SOIC) 14-PINS	TCAN157x-Q1 DMT (VSON) 14-PINS	TCAN157x-Q1 DYY(SOT-23) 14-PINS	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.3	37.8	33.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.4	13.9	30.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.6	0.7	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	38.9	13.9	30.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	4.7	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Supply Characteristics

parameters valid across –40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY FROM BATTERY						
I_{SUP}	Battery supply current	Sleep mode: selective wake off, 4.5V ≤ V_{SUP} ≤ 28V		20	35	µA
		Standby mode: selective wake off, 4.5V ≤ V_{SUP} ≤ 28V		60	95	µA
		Additional current when CAN bus is listening and bias is connected to 2.5V.		15	40	µA
		Additional current from WAKE pin		1	2	µA
		Normal mode		1	1.5	mA
		Additional current when selective wake is enabled and bus active		400	550	µA
$V_{SUP(PU)R}$	Supply on detection	V_{SUP} rising	1.9		3.9	V
$V_{SUP(PU)F}$	Supply off detection	V_{SUP} falling	1.8		3.5	V
UV_{SUPR}	Supply under voltage recovery	V_{SUP} rising	3.75		4.4	V
UV_{SUPF}	Supply under voltage detection	V_{SUP} falling	3.4		4.25	V
SUPPLY FROM V_{CC}						
I_{CC}	Supply current	Normal mode: Recessive, V_{TXD} = V_{IO}		3	5	mA
		Normal mode: Dominant, V_{TXD} = 0 V, R_L = 60Ω and C_L = open, typical bus load			60	mA
		Normal mode: Dominant, V_{TXD} = 0 V, R_L = 50Ω and C_L = open, high bus load			70	mA
		Normal mode: Dominant with bus fault, V_{TXD} = 0V, CANH = - 25V, R_L and C_L = open			110	mA
		Standby mode: selective wake off, V_{TXD} = V_{IO}, R_L = 50Ω, C_L = open		3.5	8	µA
		Sleep mode		2.5	5	µA
UV_{CCR}	Supply under voltage recovery	V_{CC} rising		4.2	4.5	V
UV_{CCF}	Supply under voltage detection	V_{CC} falling	3.5	4		V
SUPPLY FROM V_{IO}						
I_{IO}	I/O supply current from V_{IO}	Sleep mode: V_{TXD} = V_{IO} where 1.71V < VIO < 5.5V			10	µA
I_{IO}	I/O supply current from V_{IO}	Standby mode: V_{TXD} = V_{IO}			10	µA
		Normal mode: recessive			10	µA
		Normal mode: dominant			40	µA
UV_{IOR}	Supply under voltage recovery	V_{IO} rising		1.4	1.65	V
UV_{IOF}	Supply under voltage detection	V_{IO} falling	1	1.25		V

6.6 Electrical Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃, 4.75V ≤ V_{CC} ≤ 5.25V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN DRIVER ELECTRICAL CHARACTERISTICS						
$V_{O(D)}$	Bus output voltage (dominant) CANH	See Receiver Test Circuit and Measurement V_{TXD} = 0V, R_L =45Ω to 65Ω, C_L = open, R_{CM} = open	3		4.26	V
	Bus output voltage (dominant) CANL		0.75		2.01	V
$V_{O(R)}$	Bus output voltage (recessive) for CANH and CANL	See Bus States (Physical Bit Representation) and Receiver Test Circuit and Measurement V_{TXD} = V_{IO}, R_L = open (no load), R_{CM} = open	2	2.5	3	V
$V_{(DIFF)}$	Differential voltage		–42		42	V
$V_{OD(R)}$	Terminated bus output voltage (recessive) for CANH and CANL	V_{TXD} = V_{IO}, 45Ω ≤ R_L ≤ 65Ω, Split termination capacatance 4.7nF	2.256		2.756	V
$V_{OD(D)}$	Differential output voltage (dominant); extended bus load	See Bus States (Physical Bit Representation) and Receiver Test Circuit and Measurement, V_{TXD} = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open	1.5		3	V
		See Bus States (Physical Bit Representation) and Receiver Test Circuit and Measurement, V_{TXD} = 0V, 45Ω ≤ R_L ≤ 70Ω, C_L = open, R_{CM} = open	1.5		3.3	V
		See Bus States (Physical Bit Representation) and Receiver Test Circuit and Measurement, V_{TXD} = 0V, R_L = 2.24kΩ, C_L = open, R_{CM} = open	1.5		5	V
$V_{OD(R)}$	Differential output voltage (recessive)	See Bus States (Physical Bit Representation) and Receiver Test Circuit and Measurement, V_{TXD} = V_{IO}, R_L = 60Ω, C_L = open, R_{CM} = open	–120		12	mV
		See Bus States (Physical Bit Representation) and Receiver Test Circuit and Measurement, V_{TXD} = V_{IO}, R_L = open (no load), C_L = open, R_{CM} = open	–50		50	mV
$V_{O(INACT)}$	Bus output voltage on CANH with bus biasing inactive (STBY)	See Bus States (Physical Bit Representation) and Receiver Test Circuit and Measurement, V_{TXD} = V_{IO}, R_L = open, C_L = open, R_{CM} = open	–0.1		0.1	V
	Bus output voltage on CANL with bus biasing inactive (STBY)		–0.1		0.1	V
	Bus output voltage on CANH - CANL (recessive) with bus biasing inactive (STBY)		–0.2		0.2	V
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{REC}	See Bus States (Physical Bit Representation) and Receiver Test Circuit and Measurement, 45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open, C_1 = 4.7nF, TXD = 250kHz, 1MHz, 2.5MHz	0.95		1.05	V/V
V_{SYM_DC}	Output symmetry (dominant or recessive) (V_{CC} – $V_{O(CANH)}$ – $V_{O(CANL)}$) with a frequency that corresponds to the highest bit rate for which the HS-PMA implementation is intended, <1 MHz or <2 Mbit/s	See Bus States (Physical Bit Representation) and Receiver Test Circuit and Measurement, 45Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open, C_1 = 4.7nF	–300		300	mV
I_{OS_DOM}	Short-circuit steady-state output current, dominant See Figure 9-1 and Figure 9-8	–3.0V ≤ V_{CANH} ≤ +18.0V, CANL = open, V_{TXD} = 0V	–115			mA
		–3.0V ≤ V_{CANL} ≤ +18.0 , CANH = open, V_{TXD} = 0V			115	mA
I_{OS_REC}	Short-circuit steady-state output current, recessive. See Figure 9-1 and Figure 9-8	–27V ≤ V_{BUS} ≤ +42V, V_{BUS} = CANH = CANL	–5		5	mA
$R_{SE\_ACT\_REC}$	Single ended SIC impedance (CANH to common mode bias and CANL to common mode bias) during active recessive drive phase	TXD= 0V, 2V ≤ $V_{O(D)}$ ≤ VCC - 2V if –12V ≤ $V_{O(D)}$ ≤ 12V Use Delta V/ Delta I method(same as used for $R_{SE\_PAS\_REC}$/$R_{DIFF\_PAS\_REC}$ in RX section), no load on bus	37.5		66.5	Ω
$R_{DIFF\_ACT\_REC}$	Differential input resistance in active recessive drive phase (CANH to CANL)	2V ≤ $V_{O(D)}$ ≤ VCC - 2V Duration from TXD= From low-to-high edge to elapse of active recessive drive period (t_{REC_START}), Use Delta V/ Delta I method(same as used for $R_{SE\_PAS\_REC}$/ $R_{DIFF\_PAS\_REC}$ in RX section), no load on bus	75		133	Ω

6.6 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃, 4.75V ≤ V_{CC} ≤ 5.25V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN RECEIVER ELECTRICAL CHARACTERISTICS						
V_{ITDOM}	Receiver dominant state differential input voltage range, bus biasing active	–12V ≤ V_{CANL} ≤ +12V –12V ≤ V_{CANH} ≤ +12V; See Receiver Test Circuit and Measurement and Receiver Function Table Normal and Standby Modes	0.9		8	V
V_{ITREC}	Receiver recessive state differential input voltage range, bus biasing active		–3		0.5	V
V_{HYS}	Hysteresis voltage for input-threshold, normal and selective wake modes			120		mV
V_{DIFF_DOM}	Receiver dominant state differential input voltage range, bus biasing in-active	12V ≤ V_{CANL} ≤ +12V –12V ≤ V_{CANH} ≤ +12V; See Receiver Test Circuit and Measurement and Receiver Function Table Normal and Standby Modes	1.15		8	V
V_{DIFF_REC}	Receiver recessive state differential input voltage range, bus biasing in-active		–3		0.4	V
V_{CM}	Common mode range: normal and standby mode		–12		12	V
$I_{IOFF(LKG)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5V, V_{CC} = V_{IO} = V_{sup} to GND via 0Ω and 47kΩ resistor	–5		5	µA
C_I	Input capacitance to ground (CANH or CANL) [(1)]				40	pF
C_{ID}	Differential input capacitance[(1)]				20	pF
$R_{DIFF\_PAS\_REC}$	Differential input resistance during passive recessive phase	V_{TXD} = V_{IO}, normal mode: –2V ≤ V_{CANH} ≤ +7V; –2V ≤ V_{CANL} ≤ +7V	12		100	kΩ
$R_{SE\_CANH/L}$	Single ended Input resistance during passive recessive phase (CANH or CANL)	–2V ≤ V_{CANH} ≤ +7V –2V ≤ V_{CANL} ≤ +7V	6		50	kΩ
$R_{IN(M)}$	Input resistance matching: [2 x ($R_{IN(CANH}$ - $RI_{NCANL)}$)/(R_{CANH}+$R_{INCANL)}$)]	V_{CANH} = V_{CANL} = 5V	–1		1	%
INH OUTPUT TERMINAL (HIGH VOLTAGE OUTPUT)						
ΔV_H	High-level voltage drop from V_{SUP} to INH	I_{INH} = –6mA		0.5	1	V
R_{pd}	Pull-down resistor	Sleep Mode	7	10	13	MΩ
WAKE INPUT TERMINAL						
V_{IH}	High-level input voltage	Selective wake-up or standby mode, WAKE pin enabled	4			V
V_{IL}	Low-level input voltage	Selective wake-up or standby mode, WAKE pin enabled			2	V
I_{IL}	Low-level input current	WAKE = 1V		1	2	µA
SDI, SCK, nCS, TXD INPUT TERMINALS						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	1.71V ≤ V_{IO} ≤ 5.5V	–1		1	µA
I_{IL}	Low-level input leakage current	Inputs = 0V, 1.71V ≤ V_{IO} ≤ 5.5V	–30		–2	µA
C_{IN}	Input capacitance	at 20MHz	2		15	pF
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.5V, V_{IO} = V_{SUP} = 0V	–1	0	1	µA
Rpu	Pull-up resistor		250	350	450	kΩ
RXD, SDO OUTPUT TERMINALS						
V_{OH}	High level output voltage	I_{OH} = -1.5mA; V_{IO} = 1.71 V	0.8			V_{IO}
		I_{OH} = -2mA; V_{IO} ≥ 2.5 V	0.8			
V_{OL}	Low level output voltage	I_{OL} = 2mA			0.2	V_{IO}
$I_{LKG(OFF)}$	Unpowered leakage current - SDO pin	V_{nCS} = V_{IO}; V_O = 0V to V_{IO}	–5		5	µA
$R_{RXD(PU)}$	RXD pin pull-up resistance	Active during UV_{SUP} and POR conditions and when in Sleep mode	40	60	80	kΩ
$I_{LKG(RXD)}$	RXD current when V_{IO} present and $R_{RXD(PU)}$ enabled	V_{RXD} = V_{IO}; V_O = 0V to V_{IO}	–1		1	µA
		V_{RXD} = GND; Active during UV_{SUP} and POR conditions and when in Sleep mode	–140		–20	µA
THERMAL SHUTDOWN						
T_{SDR}	Thermal shut down		175			°C

6.6 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃, 4.75V ≤ V_{CC} ≤ 5.25V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SDF}	Thermal shut down release		160			°C
T_{SDW}	Thermal shut down warning		150			°C
T_{SDHYS}	Thermal shut down hysteresis			10		°C

(1) Test according to ISO 11898-2:2024

6.7 Timing Requirements

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY					
t_{PWRUP}	Time from V_{SUP} exceeding 4.4V until INH active; see Power Up Timing		2	4	ms
t_{UVFLTR}	Under voltage detection delay time	3		50	µs
t_{UVSLP}	Time from an UV_{CC} and/or UV_{IO} event to clear before transitioning to sleep or failsafe mode	200		400	ms
MODE CHANGE					
$t_{MODE\_STBY\_NOM}$	The time it takes for the part to transition to normal mode from standby mode after receiving this command via SPI; see Section 7			70	µs
$t_{MODE\_NOM\_SLP}$	The time it takes for the part to transition to sleep mode from normal mode after receiving this command via SPI; see Normal to Sleep Timing			200	µs
$t_{MODE\_SLP\_STBY}$	Time from UV_{CC} and UV_{IO} clearing after INH turns on to RXD pin pulling low; (3) see Sleep to Standby Timing			100	µs
$t_{MODE\_NOM\_STBY}$	The time it takes for the part to transition to standby mode from normal mode after receiving this command via SPI; see Normal to Standby Timing			70	µs
$t_{INH\_SLP\_STBY}$	WUP, LWU or WUF event until INH asserted; see Sleep to Standby Timing			100	µs
$t_{INH\_NOM\_SLP}$	SPI write to go to sleep from normal mode and INH turns off; see Normal to Sleep Timing			50	µs
DEVICE TIMING					
t_{WAKE}	Wake up time from a wake edge on WAKE; standby, selective wake or sleep mode; See Local Wake Up – Rising Edge and Local Wake Up – Falling Edge	40			µs
$t_{WAKE\_INVALID}$	WAKE pin pulses shorter than this will be filtered out; See Local Wake Up – Rising Edge and Local Wake Up – Falling Edge			10	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value; see Wake Up Pattern (WUP) and Bus Wake via RXD Request (BWRR)	0.5		2	ms
t_{WK_FILTER}	Bus time to meet filtered bus requirements for wake-up request; 4.75V ≤ VCC ≤ 5.25V; see Wake Up Pattern (WUP) and Bus Wake via RXD Request (BWRR)	0.5		0.95	µs
$t_{WK\_WIDTH\_MIN}$ (4)	Minimum WAKE Pin pulse width Register (1) (2) 11h[3:2] = 00b; see WAKE Pin Pulse Behavior	10			ms
	Minimum WAKE Pin pulse width Register (1) (2) 11h[3:2] = 01b; see WAKE Pin Pulse Behavior	20			ms
	Minimum WAKE Pin pulse width Register (1) (2) 11h[3:2] = 10b; see WAKE Pin Pulse Behavior	40			ms
	Minimum WAKE Pin pulse width Register (1) (2) 11h[3:2] = 11b; see WAKE Pin Pulse Behavior	80			ms
$t_{WK\_WIDTH\_INVALID}$	Maximum WAKE Pin pulse width that is considered invalid (1) (2) Register 11h[3:2] = 00b; see WAKE Pin Pulse Behavior			5	ms
	Maximum WAKE Pin pulse width that is considered invalid (1) (2) Register 11h[3:2] = 01b; see WAKE Pin Pulse Behavior			10	ms
	Maximum WAKE Pin pulse width that is considered invalid (1) (2) Register 11h[3:2] = 10b; see WAKE Pin Pulse Behavior			20	ms
	Maximum WAKE Pin pulse width that is considered invalid (1) (2) Register 11h[3:2] = 11b; see WAKE Pin Pulse Behavior			40	ms

6.7 Timing Requirements (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$t_{WK\_WIDTH\_MAX}$	Maximum WAKE Pin pulse window [(1)] Register 11h[1:0] = 00b; see WAKE Pin Pulse Behavior	750		950	ms
	Maximum WAKE Pin pulse window [(1)] Register 11h[1:0] = 01b; see WAKE Pin Pulse Behavior	1000		1250	ms
	Maximum WAKE Pin pulse window [(1)] Register 11h[1:0] = 10b; see WAKE Pin Pulse Behavior	1500		1875	ms
	Maximum WAKE Pin pulse window [(1)] Register 11h[1:0] = 11b; see WAKE Pin Pulse Behavior	2000		2500	ms
$t_{SILENCE}$	Timeout for bus inactivity. Timer is reset and restarted when bus changes from dominant to recessive or vice versa.	0.6		1.2	s
$t_{INACTIVE}$	Sleep Wake Error (SWE) timer	3.75		5	min
t_{Bias}	Time from the start of a dominant-recessive-dominant sequence. Each phase 6 µs until Vsym ≥ 0.1; see Test Signal Definition for Bias Reaction Time Measurement			250	µs
t_{TXD_DTO}	Dominant time out, R_L = 60Ω, C_L = open; see TXD Dominant Time Out Test Circuit and Measurement	1		5	ms
t_{TOGGLE}	RXD pin toggle timing when programmed after a WUP; see Wake Up Pattern (WUP) and Bus Wake via RXD Request (BWRR)	5	10	15	µs

(1) This parameter is valid only when register 11h[7:6] = 11b
(2) This is the minimum pulse width for a WAKE pin input that device will detect as a good pulse. Values between the min $t_{WK\_WIDTH\_MIN}$ and max $t_{WK\_WIDTH\_INVALID}$ are indeterminate and may or may not be considered valid. This parameter works with $t_{WK\_WIDTH\_MIN}$ to determine if a WAKE input pulse is valid
(3) Dependent upon V_{CC} and V_{IO} being above UV_{CC} and UV_{IO} after INH turns on node power.
(4) $t_{WK\_WIDTH\_INVALID}$ sets this value by using register 11h[3:2]

6.8 Switching Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN TRANSCEIVER SWITCHING CHARACTERISTICS						
$t_{prop(TxD-busdom)}$	Propagation delay time, high-to-low TXD edge to bus dominant (recessive to dominant)	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, R_{CM} = open; see Receiver Test Circuit and Measurement; The input signal on TXD shall have rising times (10% to 90%) and fall times (90% to 10%) of less than 10ns			80	ns
$t_{prop(TxD-busrec)}$	Propagation delay time, low-to-high TXD edge to bus recessive (dominant to recessive)				80	ns
$t_{sk(p)}$	Pulse skew (|$t_{pHR} - t_{pLD}$|)			10	40	ns
$t_{R/F}$	Differential output signal rise time		5	55	75	ns
$t_{prop(busdom-RxD)}$	Propagation delay time, bus dominant input to RxD low output	$C_{L(RXD)}$ = 15pF; see Receiver Test Circuit and Measurement; The input signal on TXD shall have rising times (10% to 90%) and fall times (90% to 10%) of less than 10ns			110	ns
$t_{prop(busrec-RxD)}$	Propagation delay time, bus to recessive input to RXD high output				110	ns
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD) dominant to recessive	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF See Transmitter and Receiver Timing Behavior Test Circuit and Measurement		100	190	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD) recessive to dominant	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF See Transmitter and Receiver Timing Behavior Test Circuit and Measurement		110	190	ns
CAN FD BIT TIMING						
$t_{BIT(BUS)}$ [(1)]	2Mbps Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500ns	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ See Transmitter and Receiver Timing Behavior Test Circuit and Measurement	490		510	ns
	5Mbps Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200ns		190		210	
$t_{BIT(BUS)}$ [(1)]	8Mbps Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 125ns[(2)]	R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ See Transmitter and Receiver Timing Behavior Test Circuit and Measurement	115		135	ns

6.8 Switching Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BIT(RXD)}$ (1)	2Mbps Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500ns	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$ See Transmitter and Receiver Timing Behavior Test Circuit and Measurement	470		520	ns
	5Mbps Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200ns		170		220	
$t_{BIT(RXD)}$ (1)	8Mbps Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 125ns(2)	R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$ See Transmitter and Receiver Timing Behavior Test Circuit and Measurement	95		145	ns
Δt_{REC} (1)	2Mbps Receiver timing symmetry with $t_{BIT(TXD)}$ = 500ns	45Ω ≤ R_L ≤ 65Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$ See Transmitter and Receiver Timing Behavior Test Circuit and Measurement	–20		15	ns
	5Mbps Receiver timing symmetry with $t_{BIT(TXD)}$ = 200ns		–20		15	
Δt_{REC} (1)	8Mbps Receiver timing symmetry with $t_{BIT(TXD)}$ = 125ns(2)	R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$ See Transmitter and Receiver Timing Behavior Test Circuit and Measurement	–20		15	ns
SIGNAL IMPROVEMENT CHARACTERISTICS						
$t_{PAS\_REC\_START}$	Signal improvement start time of passive recessive phase	Measured from rising TXD edge with < 5ns slope at 50% threshold, to the end of the signal improvement phase; $R_{DIFF\_PAS\_REC}$ ≥ MIN $R_{DIFF\_ACT\_REC}$; $R_{SE\_CANH/L}$ ≥ MIN $R_{SE\_SIC\_REC}$ See Transmitter and Receiver Timing Behavior Test Circuit and Measurement			530	ns
$t_{ACT\_REC\_START}$	Start time of active signal improvement phase	Measured from rising TXD edge with < 5ns slope at 50% threshold,			120	ns
$t_{ACT\_REC\_END}$	End time of active signal improvement phase	Measured from rising TXD edge with < 5ns slope at 50% threshold,	355			ns
SPI SWITCHING CHARACTERISTICS						
f_{SCK}	SCK, SPI clock frequency	Normal, standby, listen and failsafe modes			4	MHz
		Sleep mode: If V_{IO} is present			10	kHz
t_{SCK}	SCK, SPI clock period	Normal, standby, listen and failsafe modes; see SPI AC Characteristic Read	250			ns
		Sleep mode: If If V_{IO} is present; See SPI AC Characteristic Read	1			µs
t_{RSCK}	SCK rise time	See SPI AC Characteristic Write			40	ns
t_{FSCK}	SCK fall time	See SPI AC Characteristic Write			40	ns
t_{SCKH}	SCK, SPI clock high	Normal, standby, listen and failsafe modes; see SPI AC Characteristic Read	125			ns
		Sleep mode: If V_{IO} is present; See SPI AC Characteristic Read	500			ns
t_{SCKL}	SCK, SPI clock low	Normal, standby, listen and failsafe modes; see SPI AC Characteristic Read	125			ns
		Sleep mode: If V_{IO} is present	500			ns
t_{CSS}	Chip select setup time	See SPI AC Characteristic Write	100			ns
t_{CSH}	Chip select hold time	See SPI AC Characteristic Write	100			ns
t_{CSD}	Chip select disable time	See SPI AC Characteristic Write	50			ns
t_{SISU}	Data in setup time	Normal, standby, listen and failsafe modes; see SPI AC Characteristic Write	50			ns
		Sleep mode: If V_{IO} is present; see SPI AC Characteristic Write	200			ns
t_{SIH}	Data in hold time	Normal, standby, listen and failsafe modes; see SPI AC Characteristic Write	50			ns
		Sleep mode: If V_{IO} is present; see SPI AC Characteristic Write	200			ns

6.8 Switching Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SOV}	Data out valid	Normal, standby, listen and failsafe modes; see SPI AC Characteristic Read			80	ns
		Sleep mode: If V_{IO} is present; see SPI AC Characteristic Read			200	ns
t_{RSO}	Data out rise time	See SPI AC Characteristic Read			40	ns
t_{FSO}	Data out fall time	See SPI AC Characteristic Read			40	ns

(1) The input signal on TXD shall have rise times and fall times (10% to 90%) of less than 10 ns
(2) ISO 11898-2 parameter, bench verified

6.9 Typical Characteristics

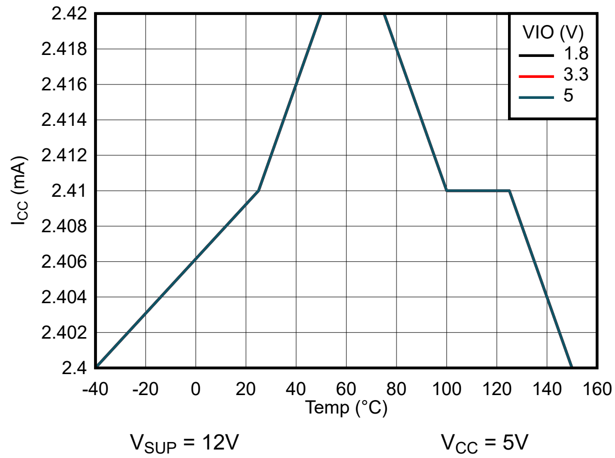


Figure 6-1. Normal Mode Recessive I_{CC} vs Temperature

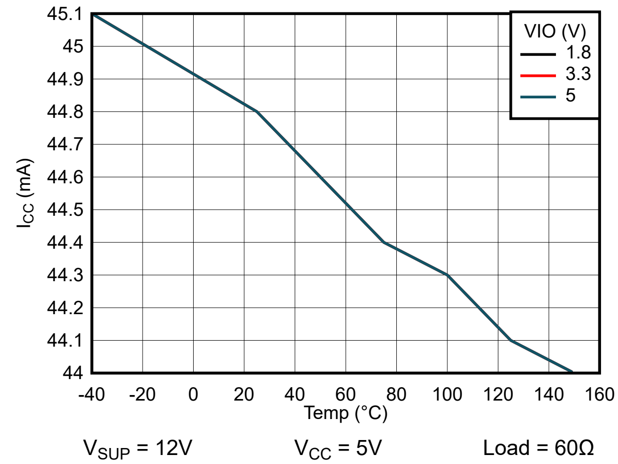


Figure 6-2. Normal Mode Dominant I_{CC} vs Temperature

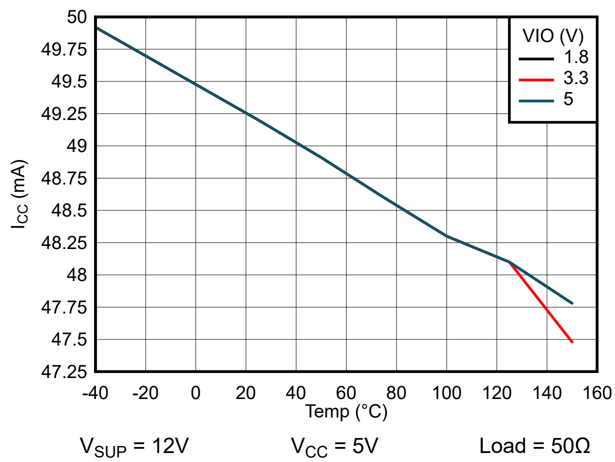


Figure 6-3. Normal Mode Dominant I_{CC} vs Temperature

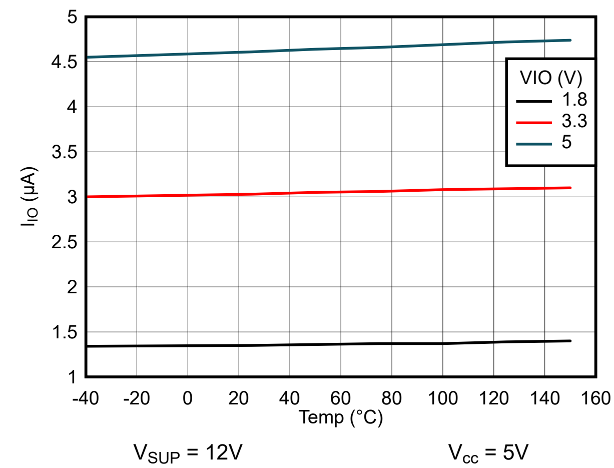


Figure 6-4. Normal Mode Recessive I_{IO} vs Temperature

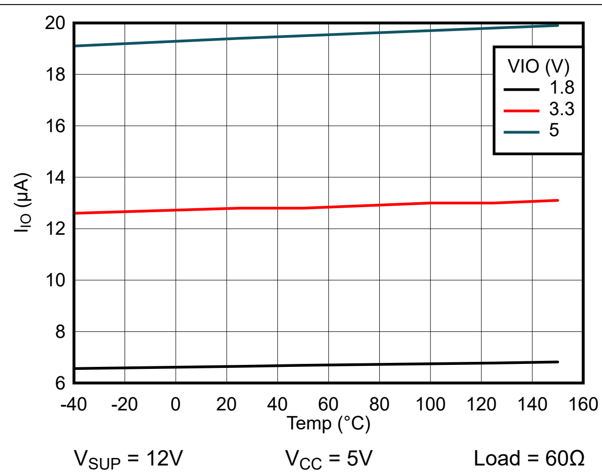


Figure 6-5. Normal Mode Dominant: I_{IO} vs Temperature

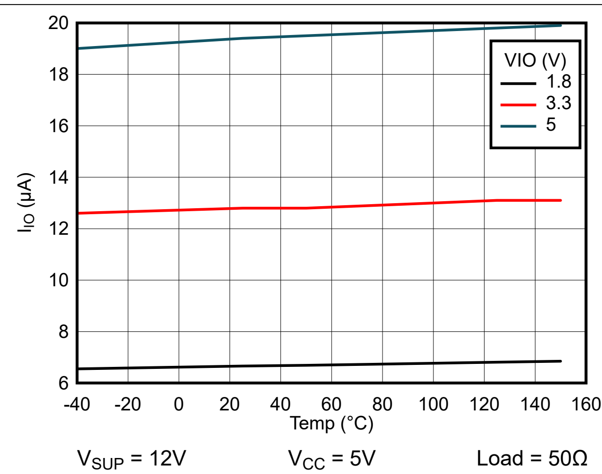
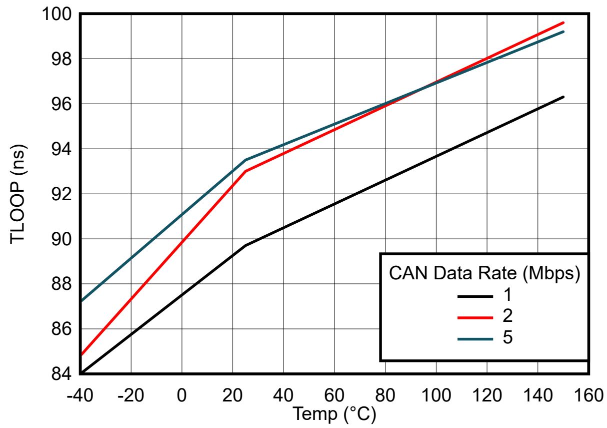


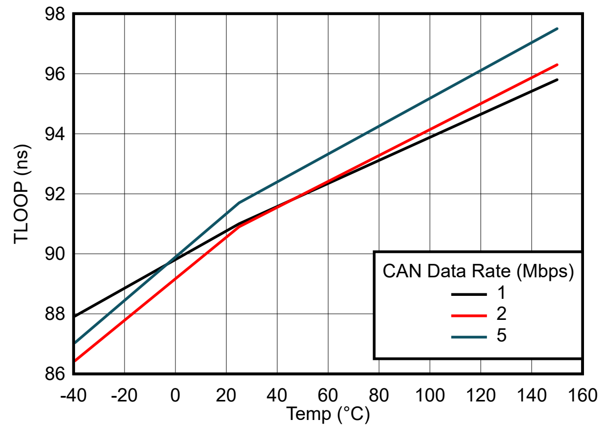
Figure 6-6. Normal Mode Dominant: I_{IO} vs Temperature

6.9 Typical Characteristics (continued)



V_{SUP} = 12V V_{CC} = 5V Load = 60Ω

Figure 6-7. t_{LOOP} vs Temperature



V_{SUP} = 12V V_{CC} = 5V Load = 50Ω

Figure 6-8. t_{LOOP} vs Temperature

7 Parameter Measurement Information

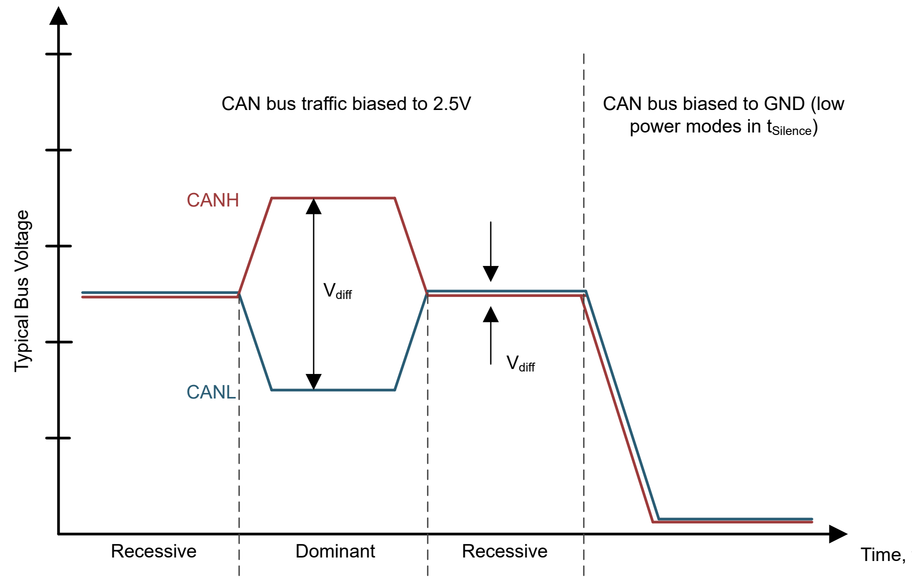


Figure 7-1. Bus States (Physical Bit Representation)

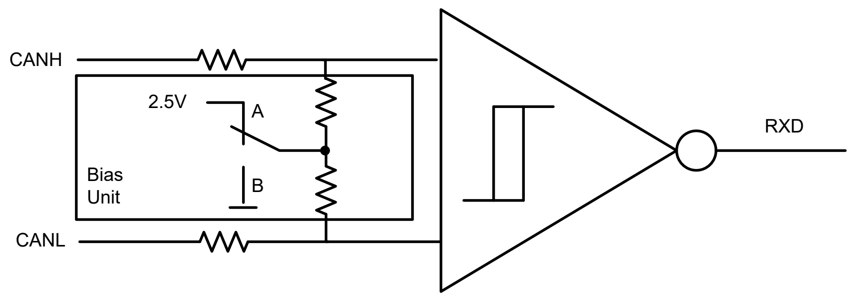


Figure 7-2. Simplified Recessive Common Mode Bias Unit and Receiver

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Note

A: Normal and Listen modes or all other modes not in $t_{Silence}$

B: All modes except Normal and Listen modes, in $t_{Silence}$

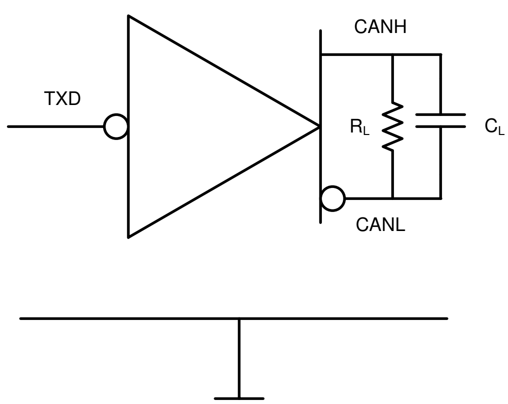

Figure 7-3. Supply Test Circuit

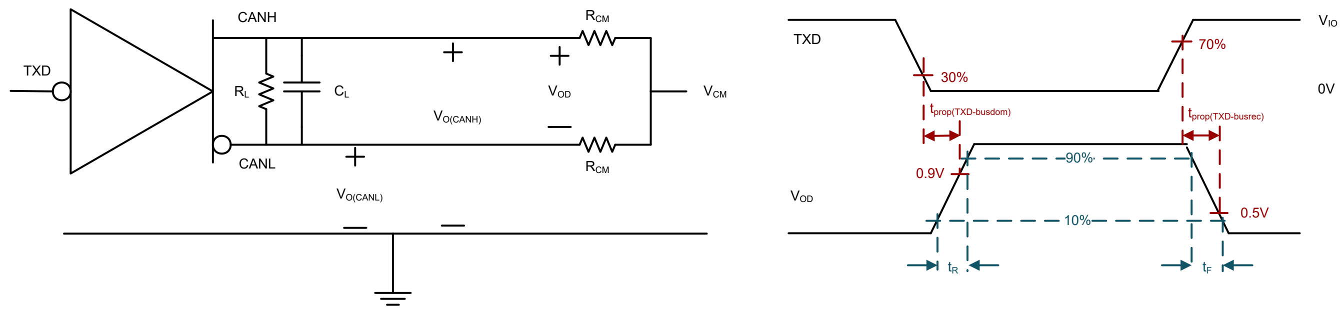

Figure 7-4. Driver Test Circuit and Measurement

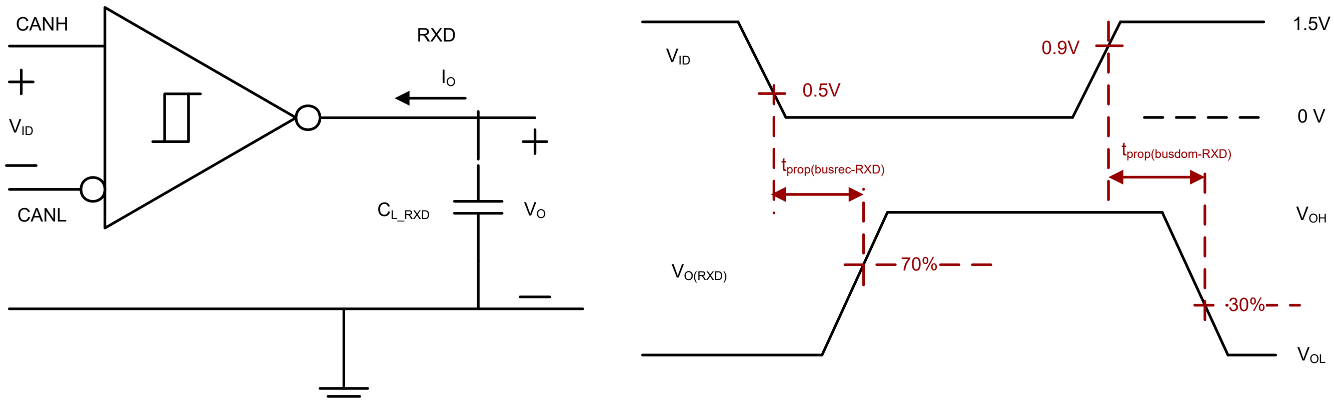

Figure 7-5. Receiver Test Circuit and Measurement

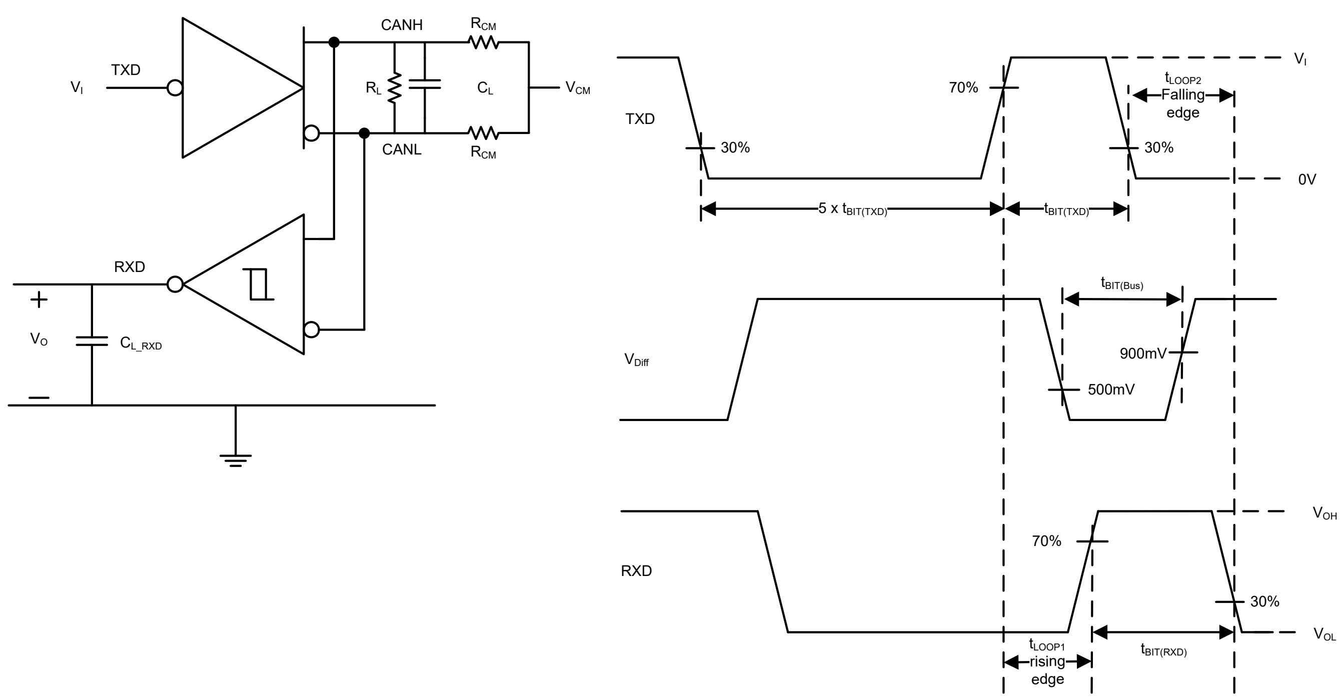

Figure 7-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

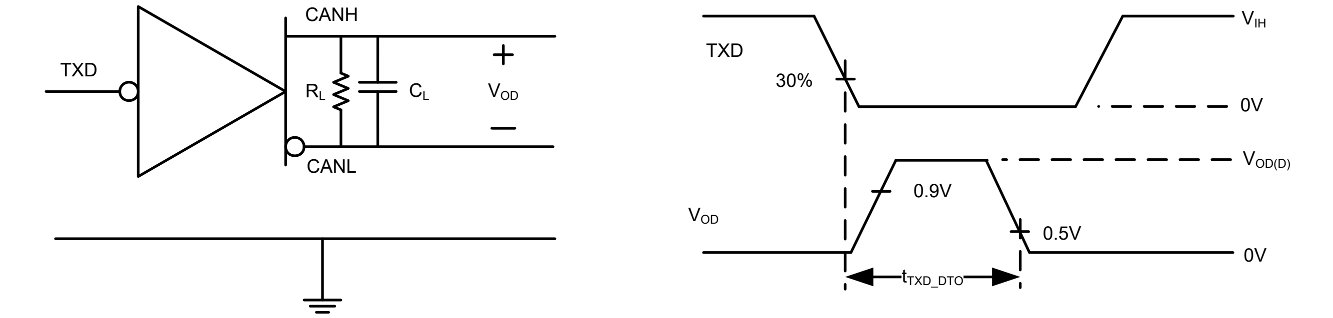

Figure 7-7. TXD Dominant Time Out Test Circuit and Measurement

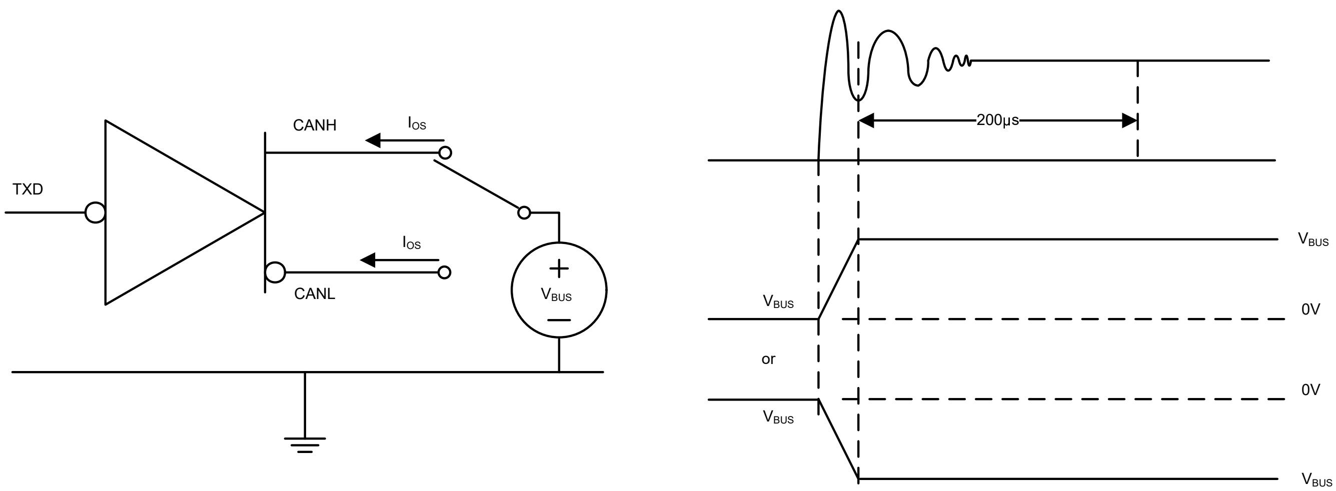

Figure 7-8. Driver Short-Circuit Current Test and Measurement

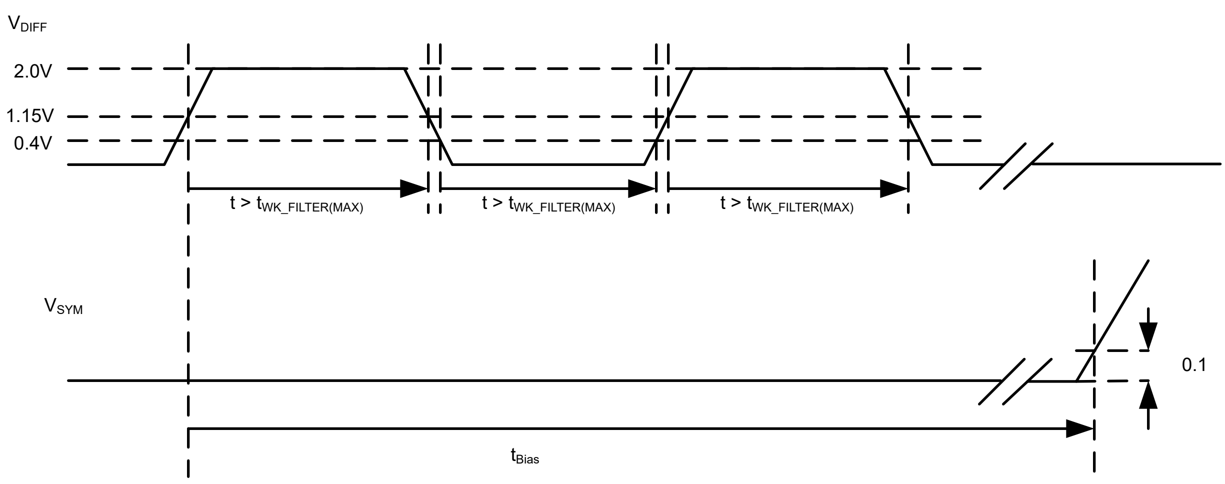

Figure 7-9. Test Signal Definition for Bias Reaction Time Measurement

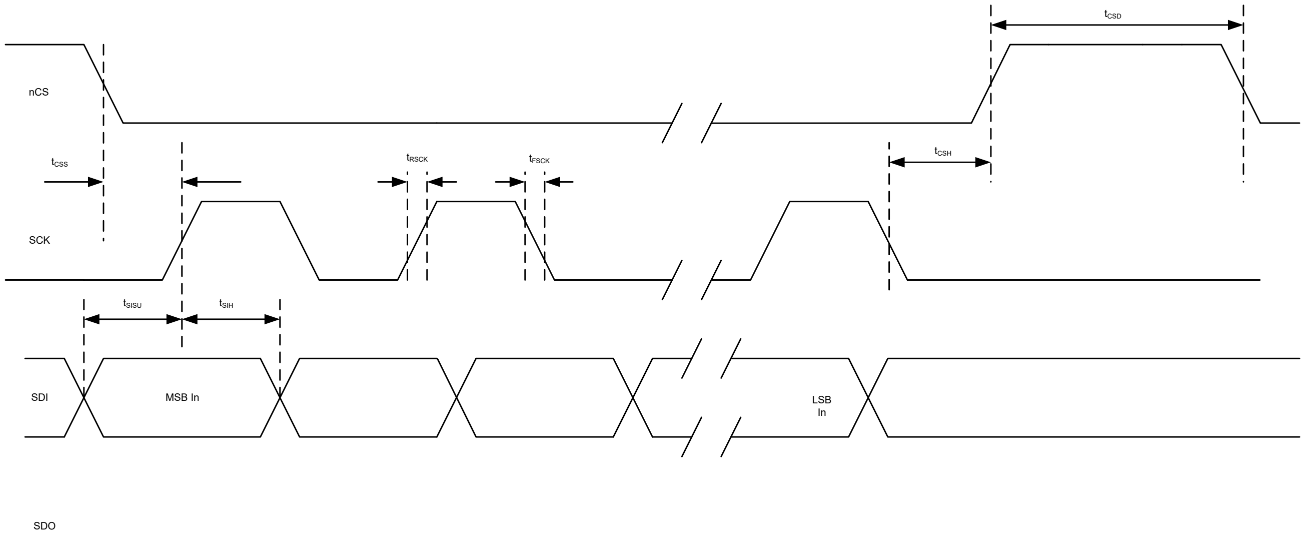

Figure 7-10. SPI AC Characteristic Write

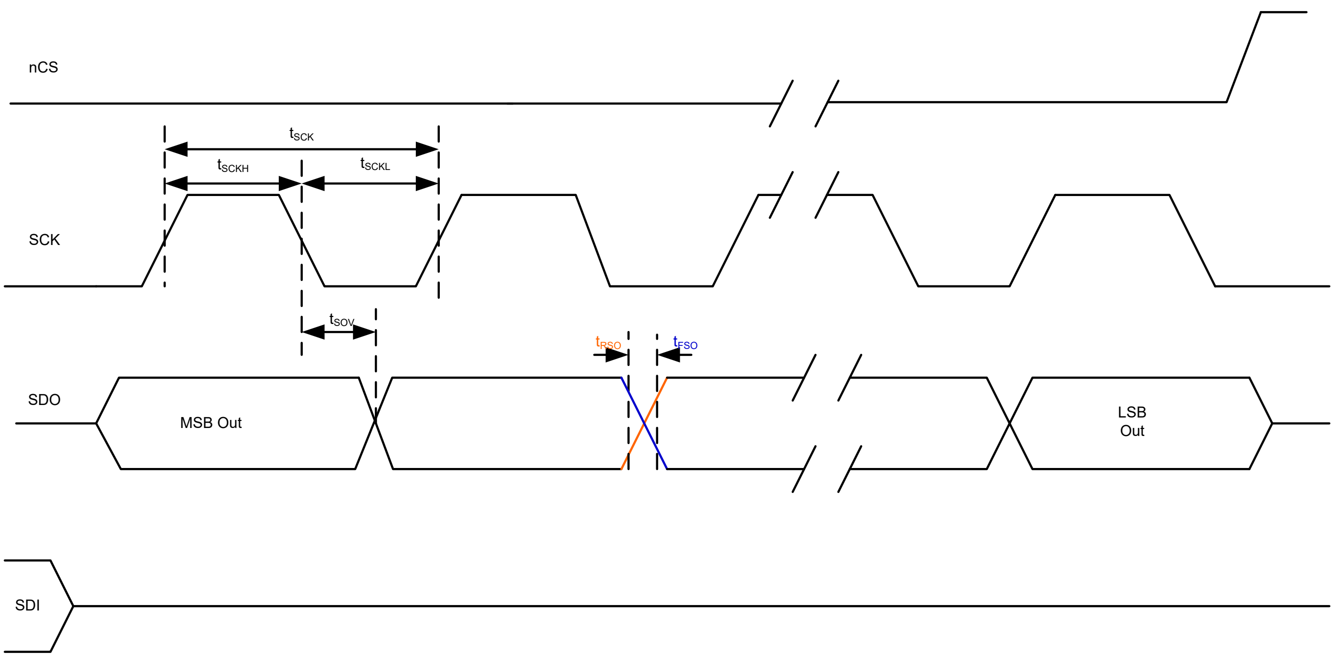

Figure 7-11. SPI AC Characteristic Read

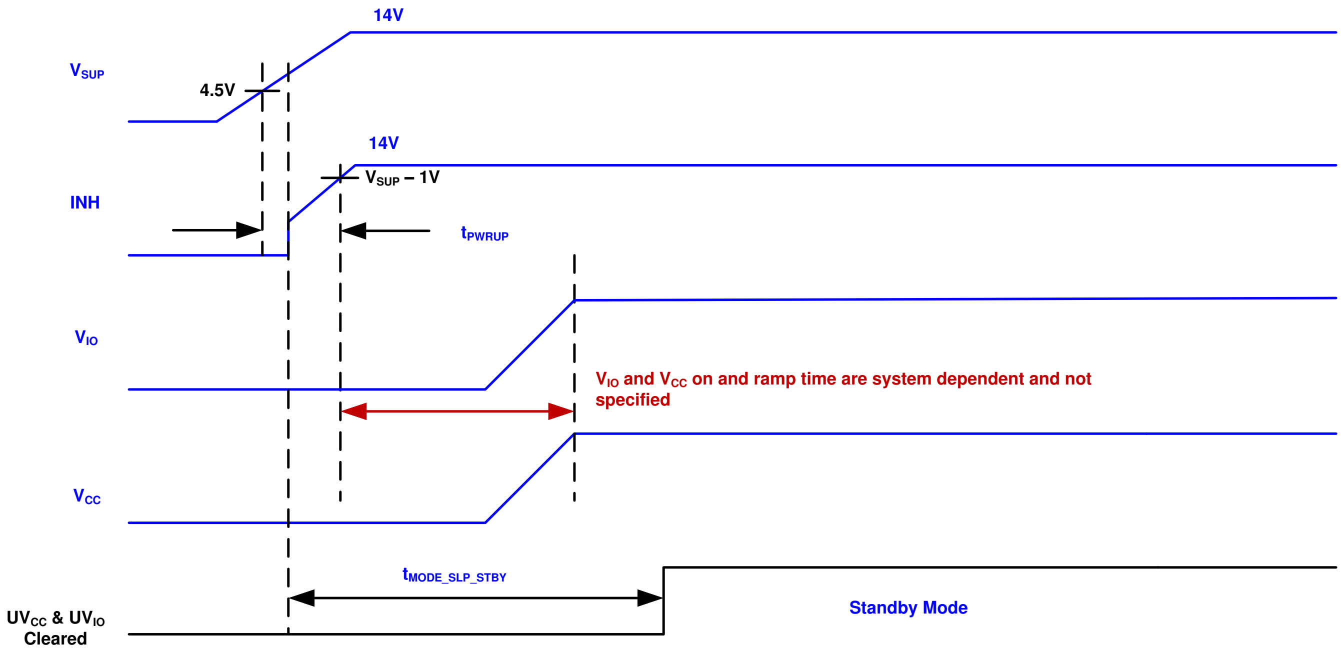

Figure 7-12. Power Up Timing

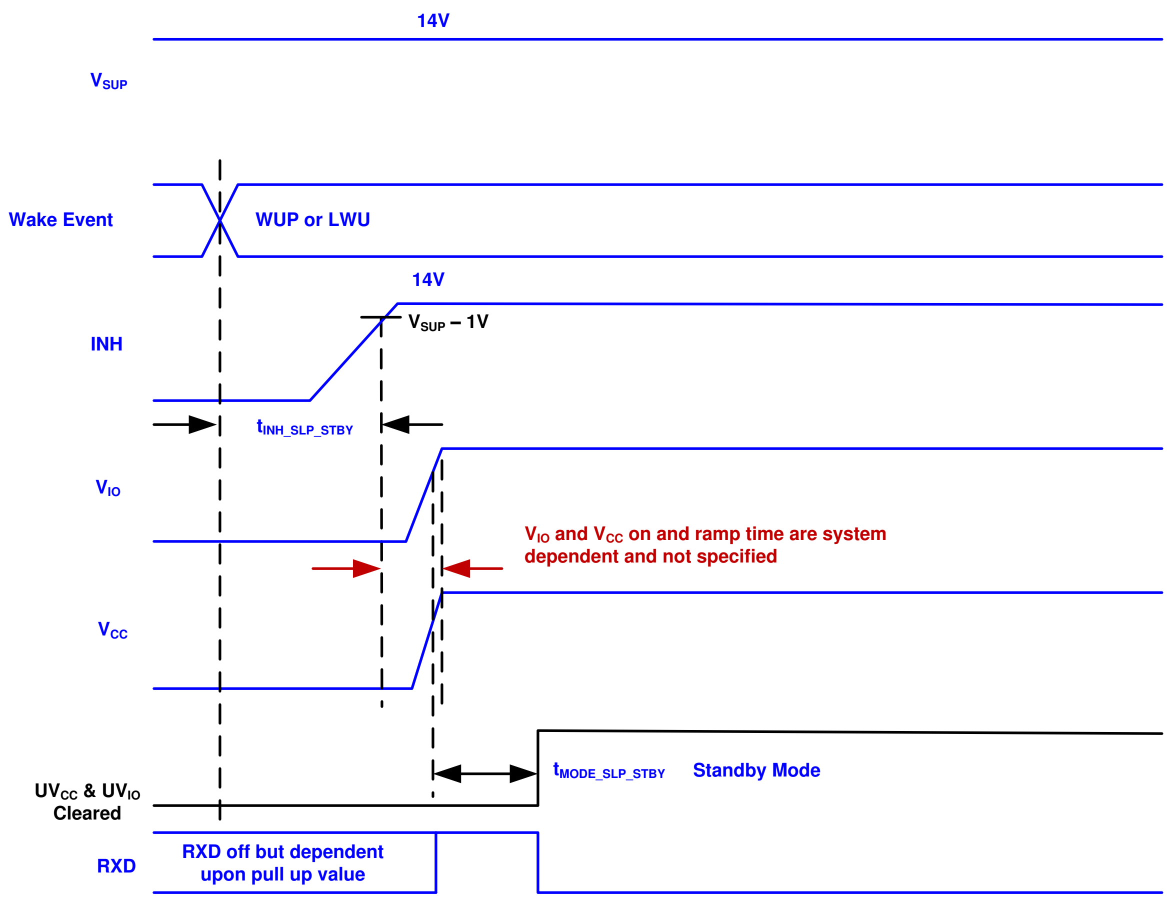

Figure 7-13. Sleep to Standby Timing

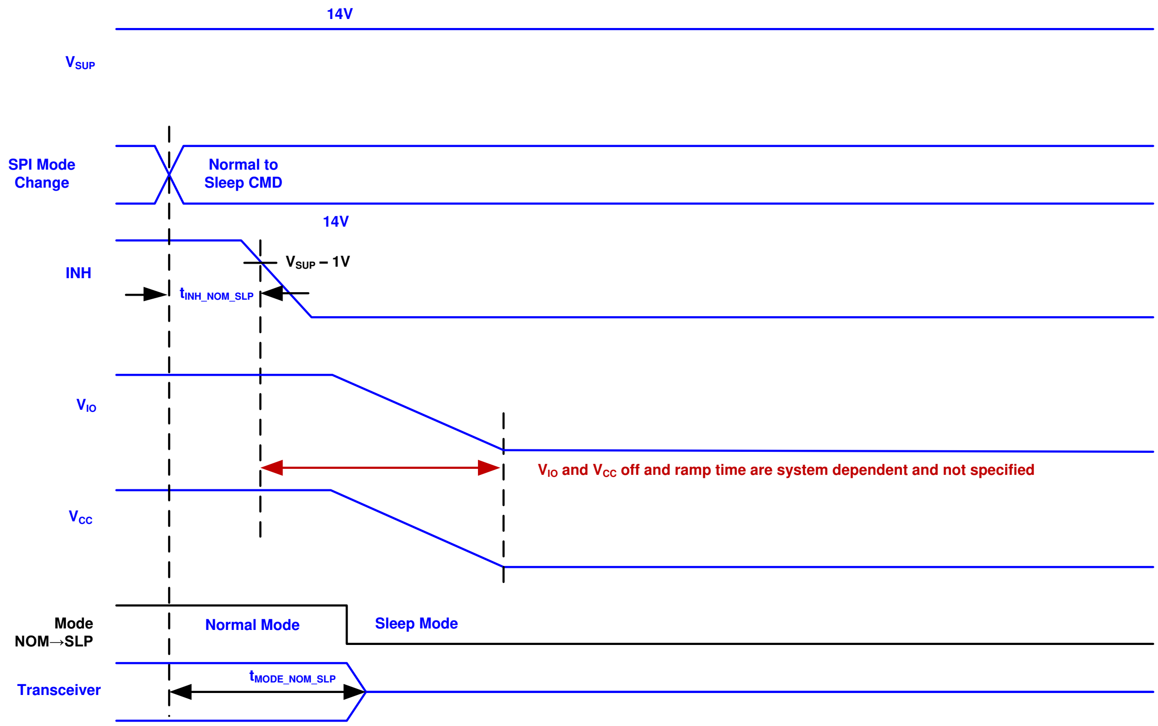

Figure 7-14. Normal to Sleep Timing

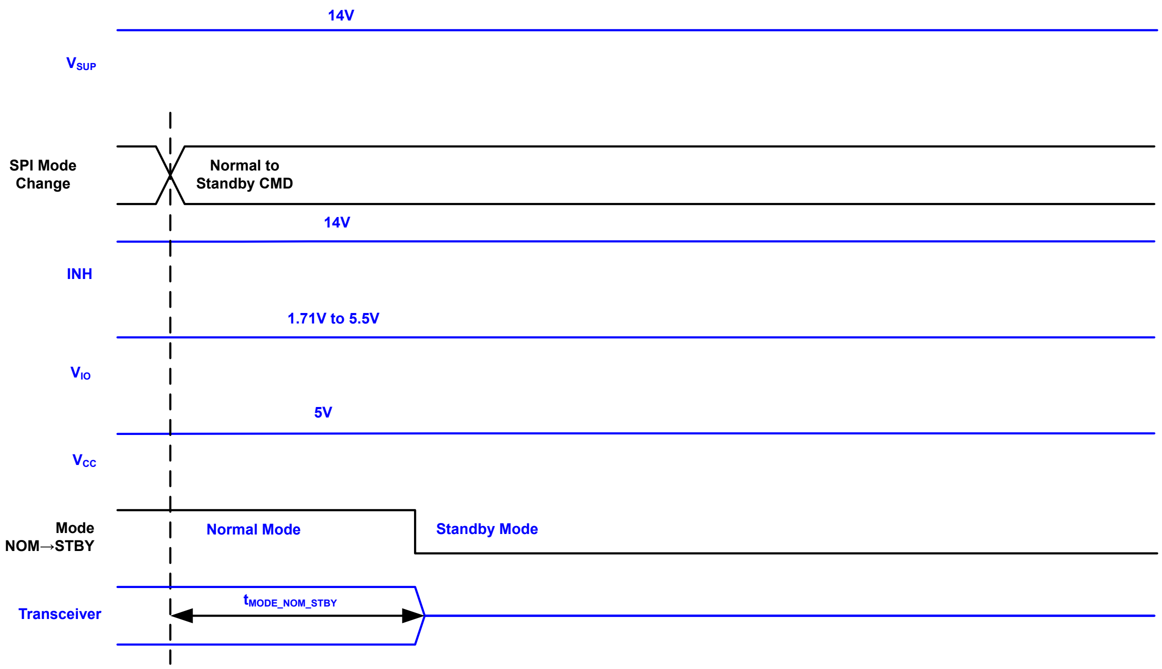

Figure 7-15. Normal to Standby Timing

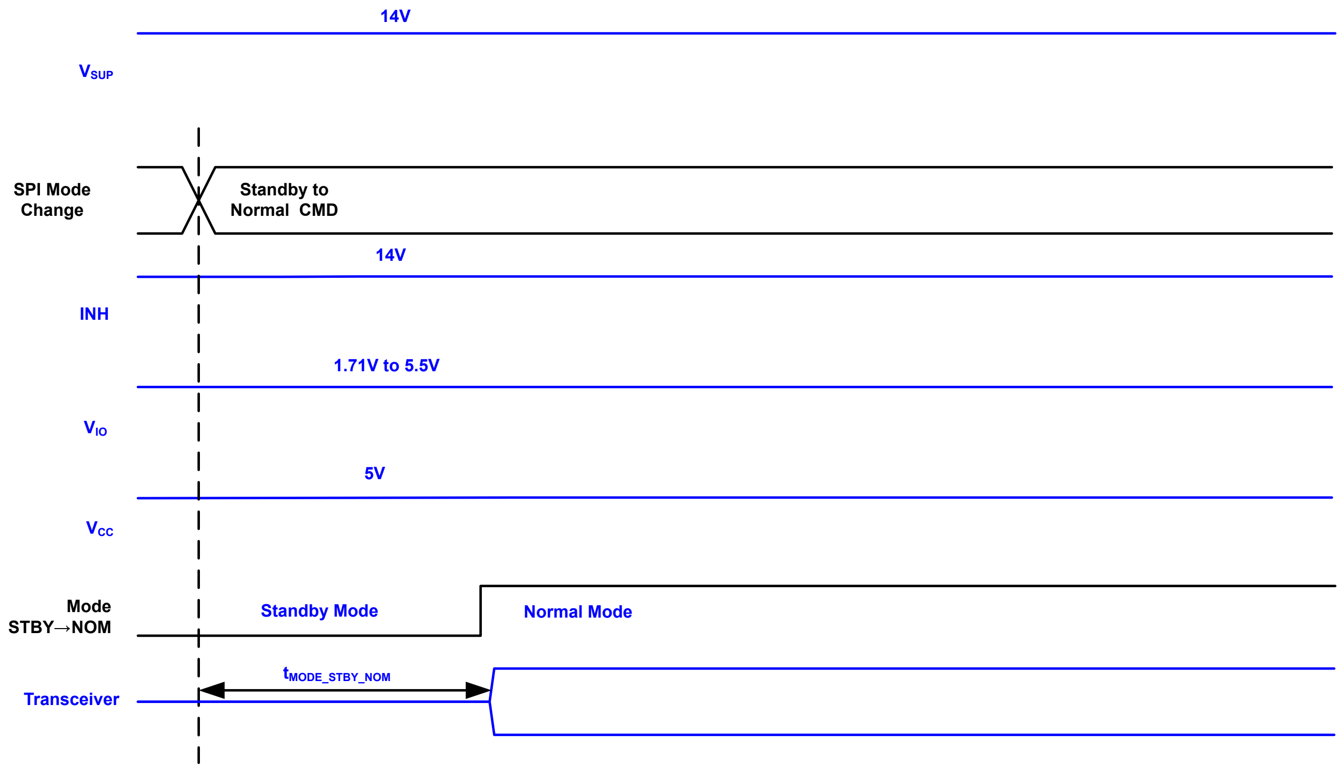

Figure 7-16. Standby to Normal Timing

Note

The blue signals are input or output of the TCAN157x-Q1. Black signals are internal to the TCAN157x-Q1. The colors are provided for timing diagrams Figure 7-12, Figure 7-13, Figure 7-14, Figure 7-15, and Figure 7-16.

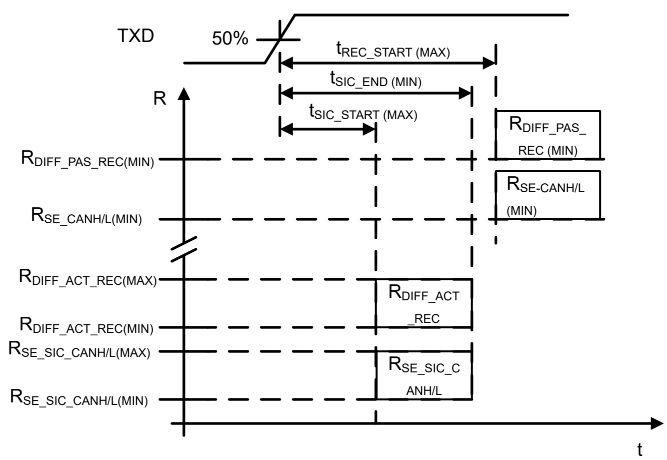

Figure 7-17. Resistance Value During Active Recessive Phase for Signal Improvement Capability

8 Detailed Description

8.1 Overview

The TCAN1576-Q1 is a CAN FD signal improvement capable (SIC) transceiver supporting data rates up to 8Mbps. Meeting the physical layer requirements of the ISO 11898-2:2024 Annex A for high-speed CAN specification or Signal Improvement (SIC) specification for up to 5Mbps. The devices support selective wake up on dedicated CAN-frames. The devices can also wakeup remotely using a CAN bus that is implementing the ISO 11898-2:2024 Annex A for the Wake Up Pattern (WUP). The TCAN1576-Q1 supports 1.8V, 3.3V and 5V processors using V_{IO} pin. The processor interface is through the SPI, RXD and TXD terminals. The devices have a Serial Peripheral Interface (SPI) that connects to a local microprocessor for configuration. SPI supports clock rates up to 4MHz. To provide flexibility for system design, configure the serial data output (SDO) pin as an interrupt output pin when the chip select pin is high.

The TCAN1576-Q1 provides a CAN FD transceiver function. The function is a differential transmit capability to the bus and differential receive capability from the bus. The device includes many protection features which provides device and CAN network robustness.

The CAN bus has two logical states during operation: recessive and dominant (see Figure 7-1 and Figure 7-2).

Recessive bus state is when the bus is biased to a common mode of about 2.5V through the high-resistance internal input resistors of the receiver of each node on the bus across the termination resistors. Recessive is equivalent to logic high and is typically a differential voltage on the bus of almost 0V. Recessive state is also the idle state.

Dominant bus state is when the bus is driven differentially by one or more drivers. Current is induced to flow through the termination resistors and generate a differential voltage on the bus. Dominant is equivalent to logic low and is a differential voltage on the bus greater than the minimum threshold for a CAN dominant. A dominant state overwrites the recessive state.

During arbitration, multiple CAN nodes can transmit a dominant bit at the same time. In this case, the differential voltage of the bus is greater than the differential voltage of a single driver.

Transceivers have a third bus state where the bus terminals are weakly biased to ground through the high resistance internal resistors of the receiver. See Figure 7-1 and Figure 7-2.

The TCAN1576-Q1 provides many enhanced features that are listed in the Feature Description. The enhanced features, advanced bus fault detection, fail-safe, and watchdog, provide a processor interrupt, which is described in each specific subsections.

8.2 Functional Block Diagram

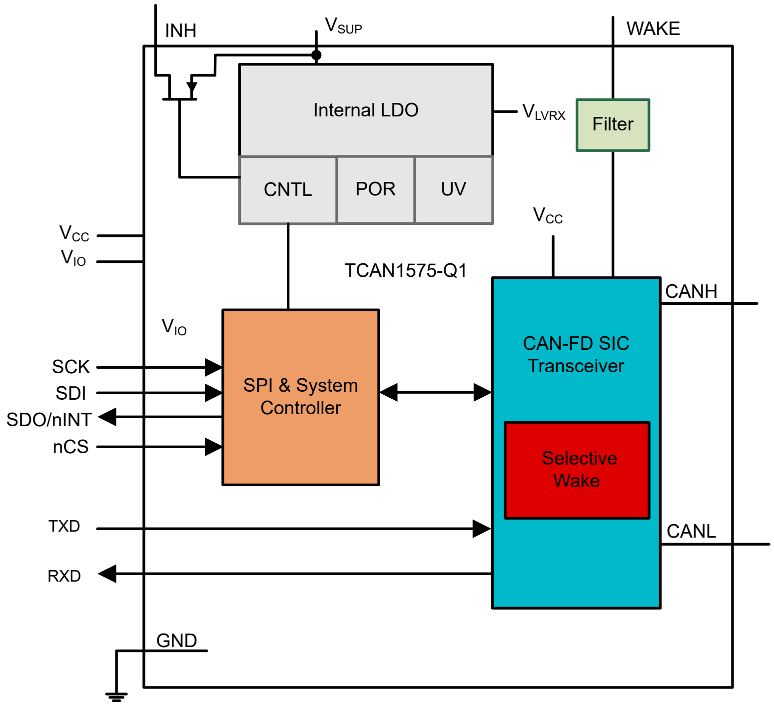

Figure 8-1. TCAN1575-Q1 Functional Block Diagram

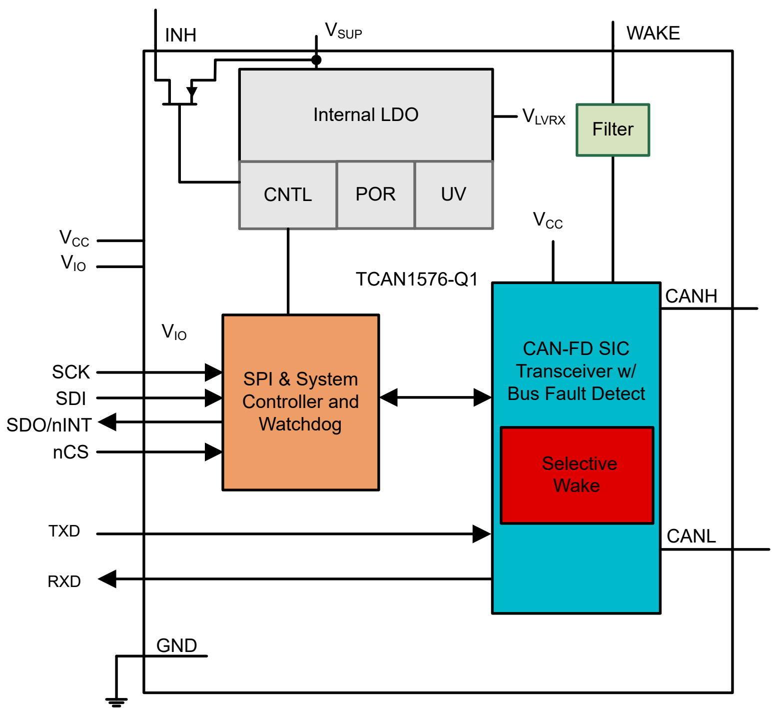

Figure 8-2. TCAN1576-Q1 Functional Block Diagram

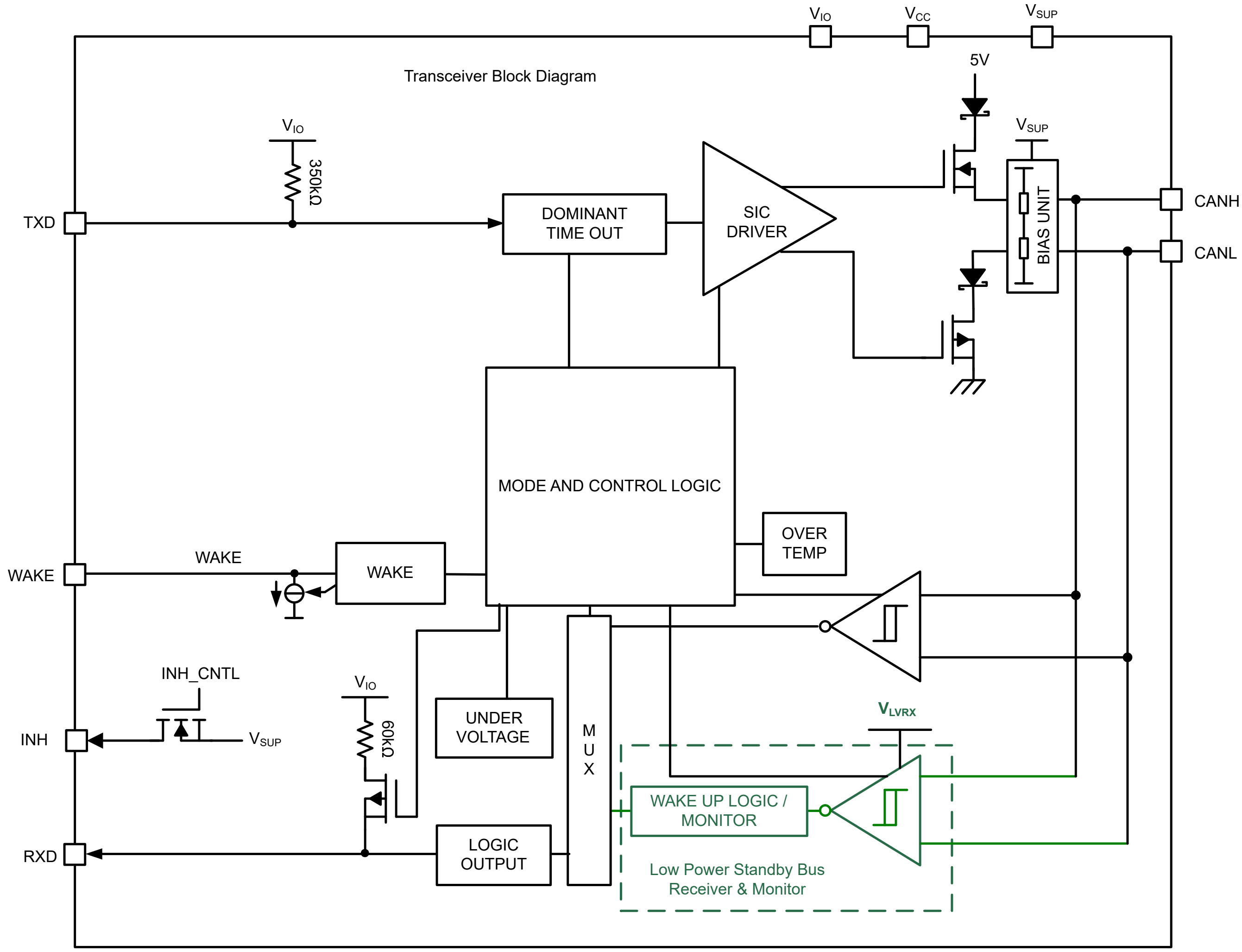

Figure 8-3. TCAN1575-Q1 CAN Transceiver Block Diagram

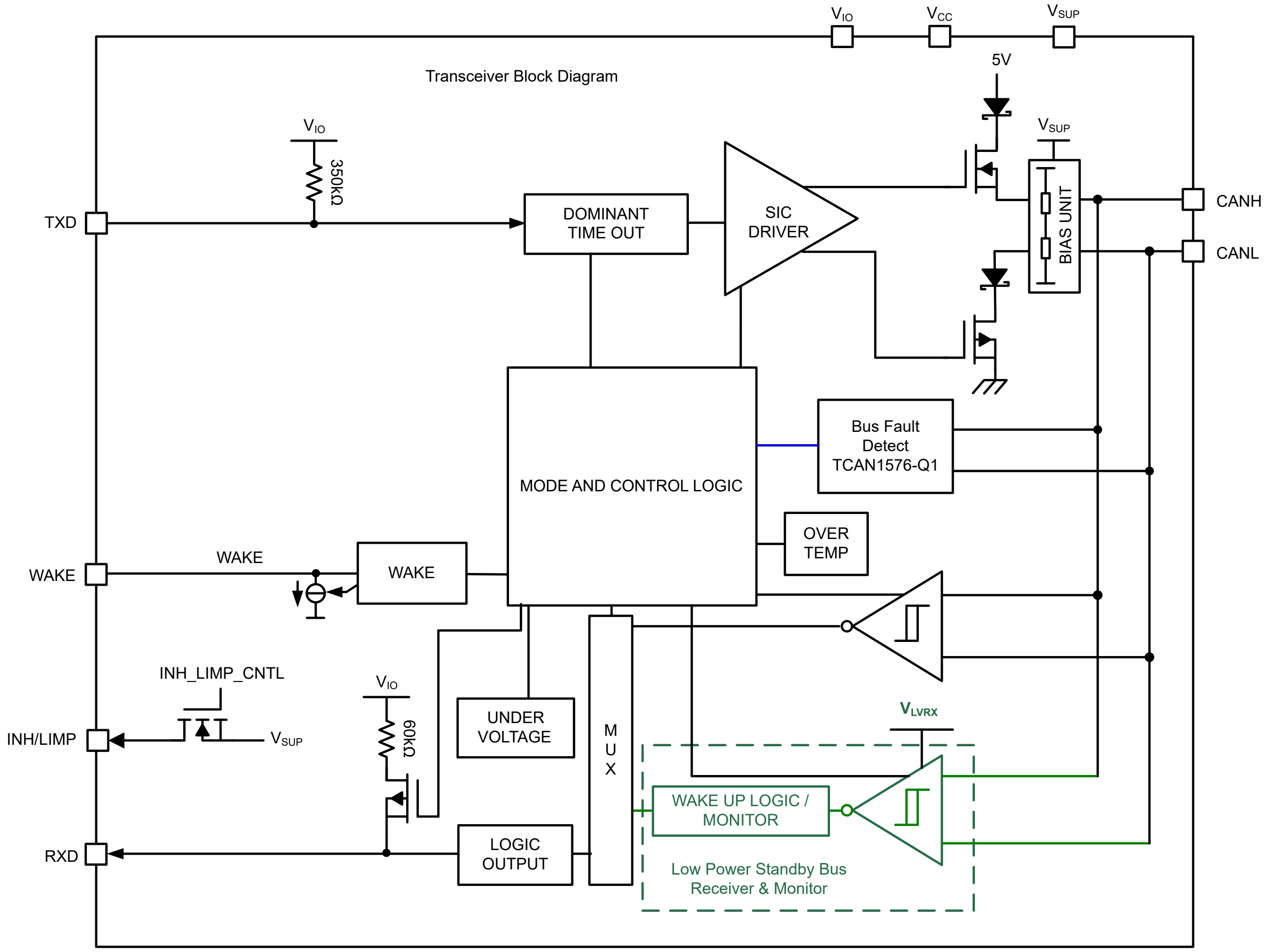

Figure 8-4. TCAN1576-Q1 CAN Transceiver Block Diagram

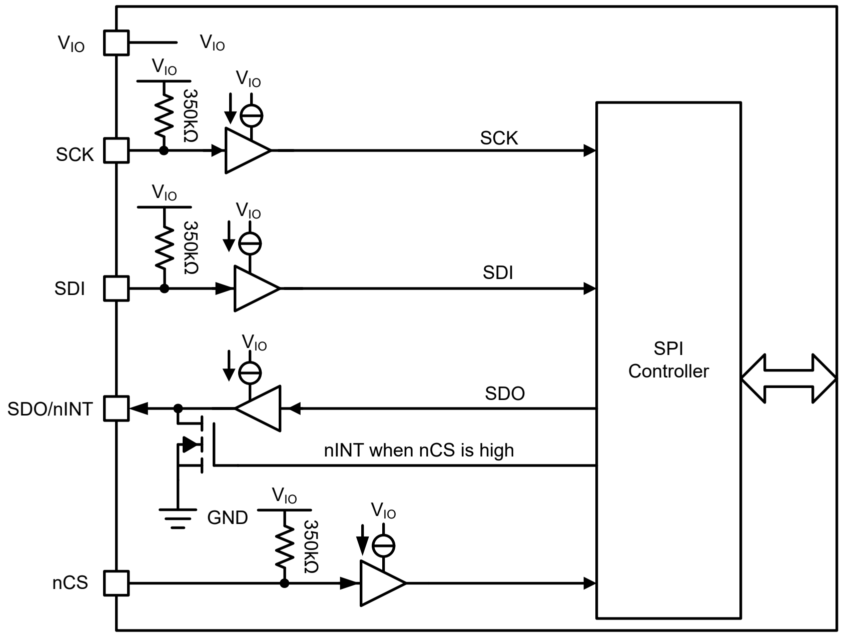

Figure 8-5. TCAN157x-Q1 SPI and Digital IO Block Diagram

8.3 Feature Description

8.3.1 V_{SUP} Pin

The V_{SUP} pin connects to the battery supply. The pin provides the supply to the internal regulators that support the digital core and low-power CAN receiver.

8.3.2 V_{IO} Pin

The V_{IO} pin provides the digital IO voltage to match the microprocessor IO voltage; thus, avoiding the requirements for a level shifter. V_{IO} supports SPI pins. The TCAN157x-Q1 family supports processors with 1.8V, 3.3V and 5V input/output which provide the widest range of controller support.

8.3.3 V_{CC} Pin

The V_{CC} pin provides 5V to the internal CAN transceiver.

8.3.4 GND Pin

The GND pin is for ground. The recommendation is the DMT package thermal pad be connected to the GND plane for heat dissipation, but is not required.

8.3.5 INH/LIMP Pin

The INH pin is a high-voltage output pin that provides voltage from the V_{SUP} minus a diode drop to enable an external high voltage regulator. These regulators are usually used to support the microprocessor and V_{IO} pin. The INH function is on in all modes except for sleep mode. In sleep mode, the INH pin is turned off, going into a high Z state. Allowing the node to be placed into the lowest power state while in sleep mode. If the INH function is not required, disable the function by setting register 8'h1A[6] = 1b using the SPI interface. The TCAN1576-Q1 can configure the pin as a LIMP home pin by setting register 8'h1A[5] = 1b. When configured as the LIMP pin, it is connected to external circuitry for a limp home mode. If a watchdog fault occurs, exceeding the programmed watchdog error counter, the device turns on the LIMP pin. If fail-safe mode is enabled, the LIMP pin turns on when entering the mode. Once on, the LIMP pin is on until the programmed watchdog error-free behavior requirement is met according to LIMP_SEL_RESET at register 8'h1A[3:2]. Writing a 1b to 8'h1A[1], LIMP_RESET, turns off the LIMP pin.

Note

The INH/LIMP pin is considered a "high voltage logic" terminal, not a power output. Thus, the pin is used to drive the EN pin of the systems power management device, and not used as a switch for power management supply. The terminal is not reverse battery protected, and must not be connected outside of the system module.

8.3.6 WAKE Pin

WAKE pin is used for a local wake up (LWU). This function is explained further in Section 8.4.4.2 section. The pin is defaulted to bidirectional edge trigger, meaning the pin recognizes a local wake up (LWU) on either a rising or falling edge of WAKE pin transition. This default value is changed through a SPI command that either configures the value as a rising edge only, a falling edge only, a pulse of specific width, and timing or a filtered rising or falling edge. This is done by using register 8'h11[7:0]. The pin requires a 22nF capacitor to ground between the two resistors.

8.3.7 TXD Pin

The TXD pin is an input from the processor for the CAN bus.

8.3.8 RXD Pin

The RXD pin is the output to the processor from the CAN bus. When a wake event takes place, this pin is pulled low by default. Change the wake-up action to pulse by setting register 8'h12[2] = 1b, RXD_WK_CONFIG. Upon power up, the RXD pin is pulled low as the device has entered standby mode once $V_{IO} \geq UV_{IO}$ and $V_{CC} \geq UV_{CC}$. To remove the $V_{CC} \geq UV_{CC}$ requirement, VCC_DIS register 8''h4B[0] = 1b. The RXD pin has an internal 60kΩ pull-up to V_{IO} that is active when $V_{SUP} \leq UV_{SUP}$, POR or when the device is in sleep mode.

8.3.9 SDO or nINT Interrupt Pin

The nINT shares the pin with the SPI serial data output (SDO) function and is defaulted as SDO only. If the pin is used as nINT, register 8'h29[0] must to be set to 1b, SDO_CONFIG. When configured to support nINT, the pin functions as an interrupt output when the nCS pin is high and by default is pulled low for a global interrupt, 8'h50[7:0]. When nCS is low, the device is using the SPI ports, and the pin is the serial data output from the TCAN1576-Q1. Figure 8-6 and Figure 8-7 show an example high level system and timing diagram when using the nINT feature.

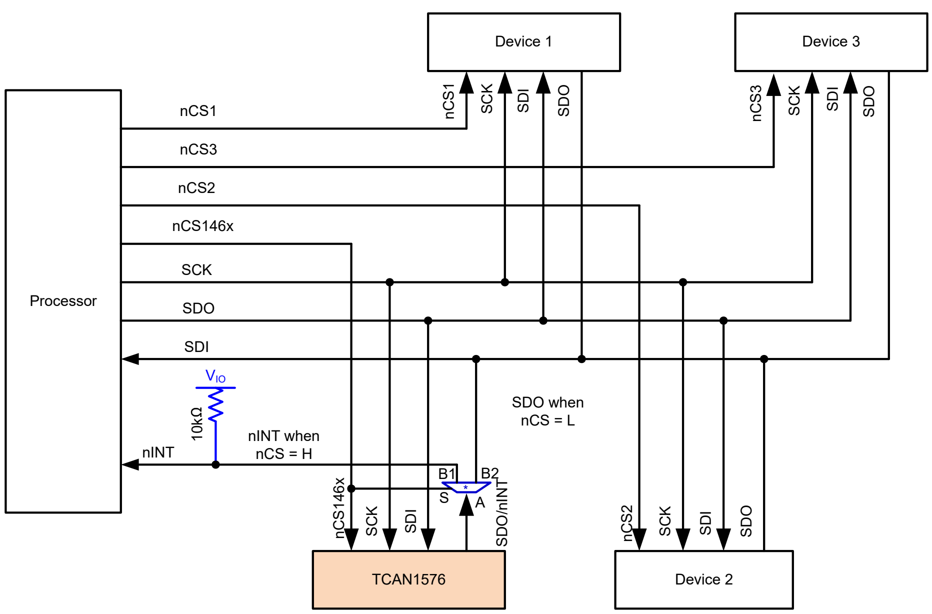

Figure 8-6. Example System Using nINT Feature

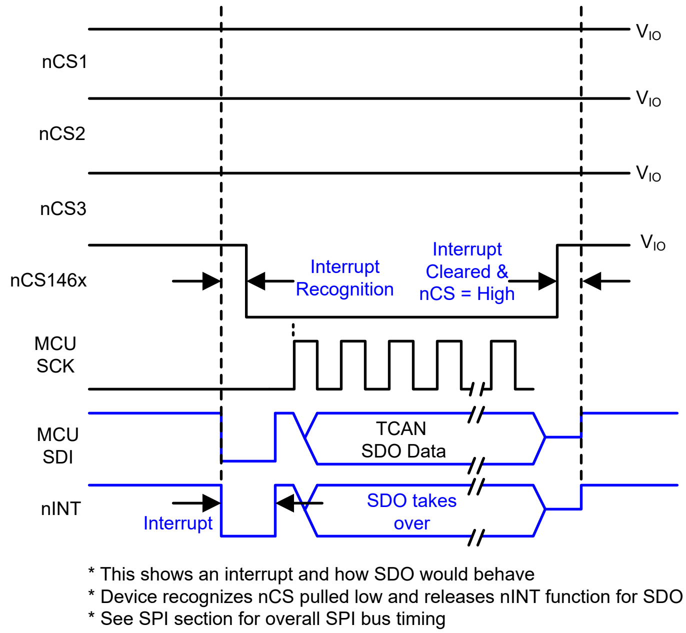

Figure 8-7. nINT Timing Diagram

Note

- Using the nINT feature, a point-to-point architecture for the SPI bus is recommended, but not required.
- To prevent an interrupt from corrupting the SDO line while using the nINT feature in a multidrop system, the recommendation is to first disable the nINT feature before communicating with another device on the SPI bus, and then re-enable the feature after communication has stopped.
- The nINT is the logical OR of all faults in registers 8'h50 to 8'h54 that are not masked.

8.3.10 nCS Pin

The nCS pin is the SPI chip-select pin. When pulled low and a clock is present, the device is written to or read from.

8.3.11 SCK

The SCK pin is the SPI serial input clock to the TCAN1576-Q1. The max clock rate is 4MHz. If VIO is present in sleep mode, SPI access can take place but at a reduced rate. If at least a 10µs delay is used between pulling nCS low, and the start of a read or write, the max SPI rate is used.

8.3.12 SDI

When nCS is low, the pin is the SPI serial data input pin used for programming the device or requesting data.

8.3.13 CANH and CANL Bus Pins

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver. The functionality of the bus pins is explained throughout the document. The CAN WUP receiver is used to wake the device from sleep mode with a CAN wake up pattern, see Section 8.4.4.1. If the system does not need to wake from the CAN bus, CAN wake is disabled by setting register 8'h1B[0] = 1b, see Figure 8-8. CAN bus biasing follows ISO 11898-2:2024 requirements, see CAN Bus Biasing.

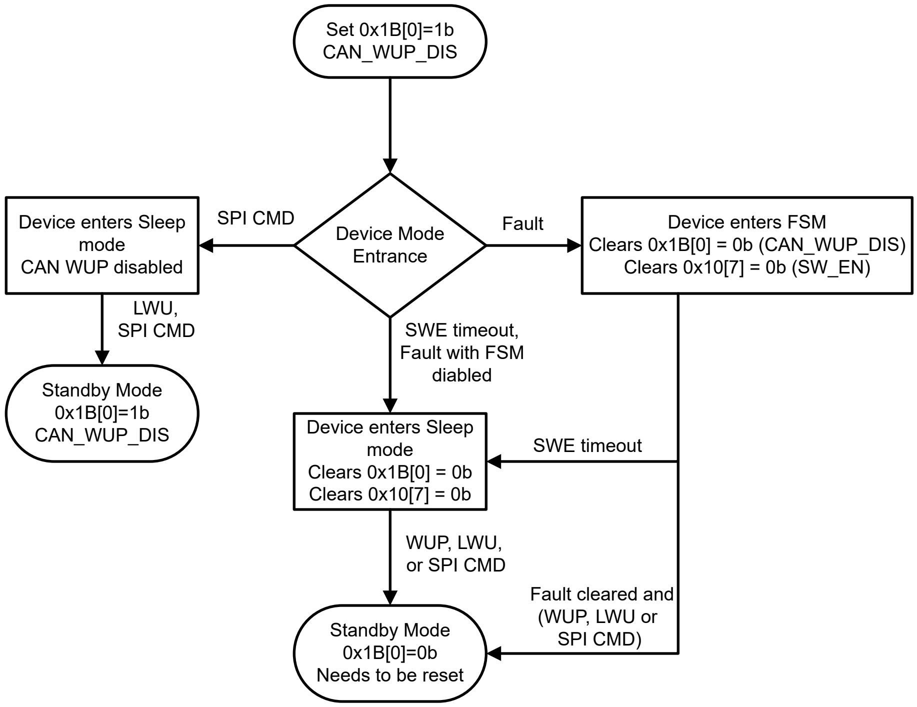

Figure 8-8. CAN Bus Wake Up Pattern Disable

Note

SWE timeout reference is valid when SWE_EN = 1b

8.3.14 CAN FD SIC Transceiver

Signal improvement is an additional capability added to CAN FD transceiver that enhances the maximum data rate achievable in complex star topologies by minimizing signal ringing. Signal ringing is the result of reflections caused by impedance mismatch at various points in a CAN network due to the nodes that act as stubs. An example of a complex network is shown in Figure 8-9.

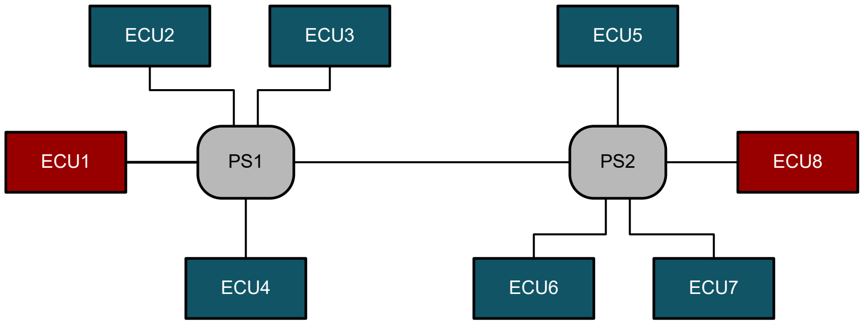

Figure 8-9. CAN FD Signal Improvement Topology

Recessive-to-dominant signal edge is usually clean as the bus is strongly driven by the transmitter. Transmitter output impedance of CAN transceiver is approximately 50Ω and matches to the network characteristic impedance. For a regular CAN FD transceiver, dominant-to-recessive edge is when the driver output impedance goes to approximately 60kΩ and the signal reflected back experiences impedance mismatch which causes ringing. The TCAN157x-Q1 resolves this issue by TX-based Signal Improvement Capability (SIC). The TCAN157x-Q1 continues to drive the bus recessive strongly until t_{REC_START} so that reflections die down and the recessive bit is clean at the sampling point. In the active recessive phase, the transmitter output impedance is low (approximately 100Ω). After this phase is over and device goes to passive recessive phase, driver output impedance goes to high-Z. This phenomenon is explained using Figure 7-17.

8.4 Device Functional Modes

The TCAN1576-Q1 has several operating modes: normal, standby, listen, sleep, and fail-safe mode, and two protected modes. The first four mode selections are made by the SPI register, 8h10[2:0]. Fail-safe mode, if enabled, is entered due to various fault conditions. The protected modes are modified standby modes used to protect the device or bus when fail-safe mode is disabled. The TCAN1576-Q1 automatically goes from sleep to standby mode when receiving a WUP or LWU event. When selective wake is enabled, the device looks for a wake-up frame (WUF) after receiving a WUP. If a WUF is not received the device transitions back to sleep mode. See Table 8-1 for the various modes and what parts of the device are active during each mode.

The TCAN1576-Q1 state diagram figure, see Figure 8-10, Figure 8-11.

Table 8-1. Mode Overview

Block	Normal	Standby	Listen	Sleep	Fail-safe	UV_{IO} Protected (Fail-safe Disabled)	TSD Protected (Fail-safe Disabled)
nINT (If Enabled)	On	On	On	Off	Fault Determines	Off	On
INH	On	On	On	Off	On	On	On
LIMP (If Enabled): TCAN1576-Q1	On if WD fail or Previous mode's state until cleared	On if WD fail or Previous mode's state until cleared	Previous mode's state until cleared	Previous mode's state until cleared	On	Previous mode's state until cleared	Previous mode's state until cleared
WAKE	Off	On	Off	On	See Note	Off	Off
SPI	On	On	On	On if VIO present	Fault Determines	Off	On
Watchdog (if enabled): TCAN1576-Q1	On	On	Off	Off	Off	Off	Off
Low Power CAN RX	Off	On	Off	On	On	On	On
CAN Transmitter	On	Off	Off	Off	Off	Off	Off
CAN Receiver	On	Off	On	Off	Off	Off	Off

Note

Fail-safe mode has several blocks that state Fault Determines. The following provides an explanation.

- nINT and SPI are active if the fault condition is UV_{CC} or TSD. These blocks are off if the fault condition is UV_{IO}.
- INH (default) in fail-safe mode is on, so the processor has power and can read which fault has occurred. When using the fail-safe counter after programmed number of wake up and go back to fail-safe cycles, INH is programmed to turn off and then on.
- The low-power CAN (WUP) receiver is powered off of V_{SUP}. A UV_{SUP} event causes this receiver to be off.
- Once the fail-safe counter limit has been reached and if register 8’h17[6:4] = 100b, FS_CNTR_ACT, the device enters sleep mode and does not respond to the wake request. A hard reset (power cycle) is required to bring the device back to normal operation.
- In fail-safe mode, the SWE timer (if enabled) starts and wake events are ignored until the fault is cleared. Once fault is cleared the WAKE pin is active.
  - If enabled and the SWE timer times out, the device enters Sleep mode. This happens even if faults are cleared, and if no wake event has taken place, or the device has not had SPI communication like changing modes.
- During an UV_{CC} event the CAN transmitter and receiver are off and low-power CAN receiver is on.

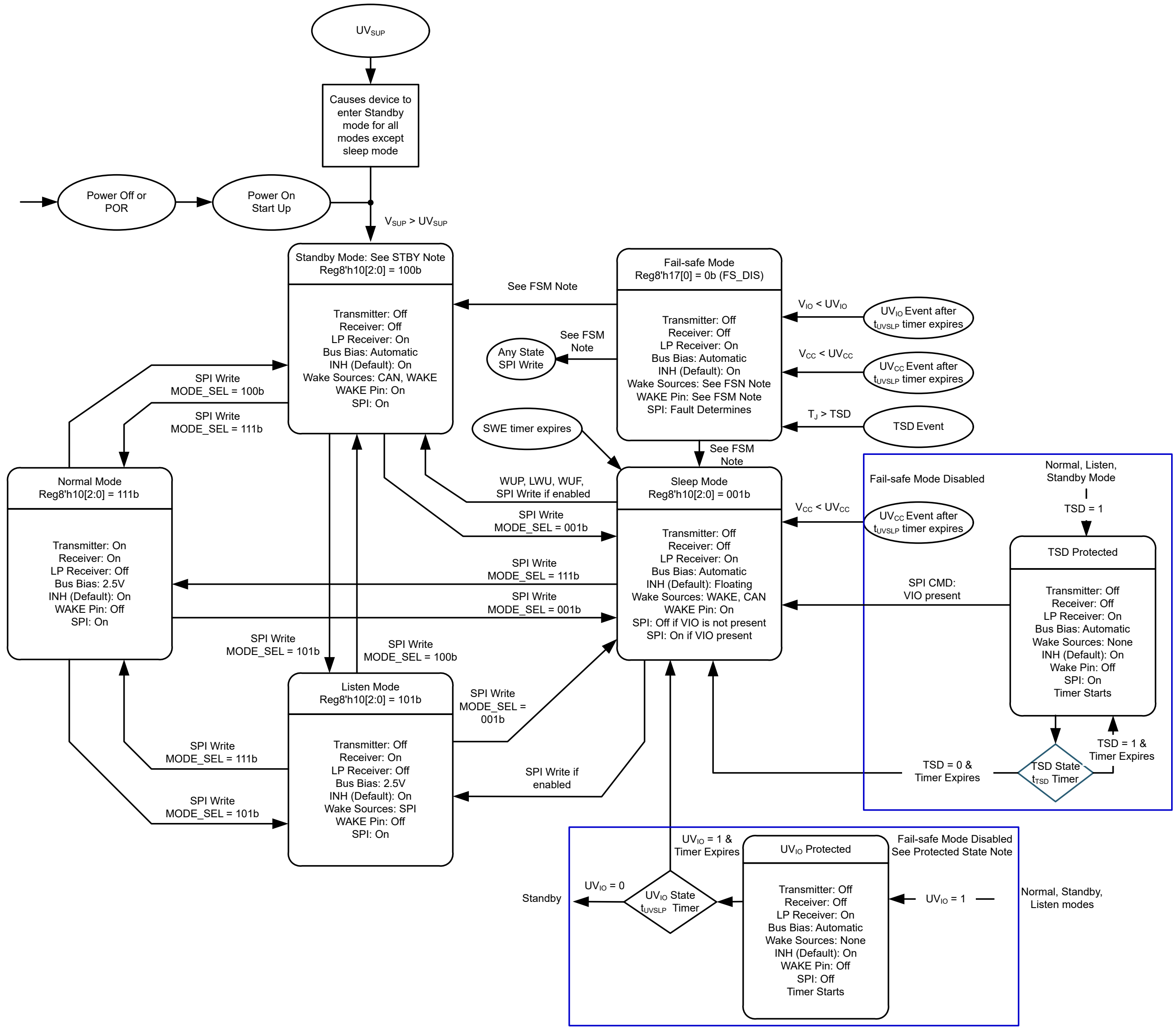

Figure 8-10. TCAN1575-Q1 Device State Diagram

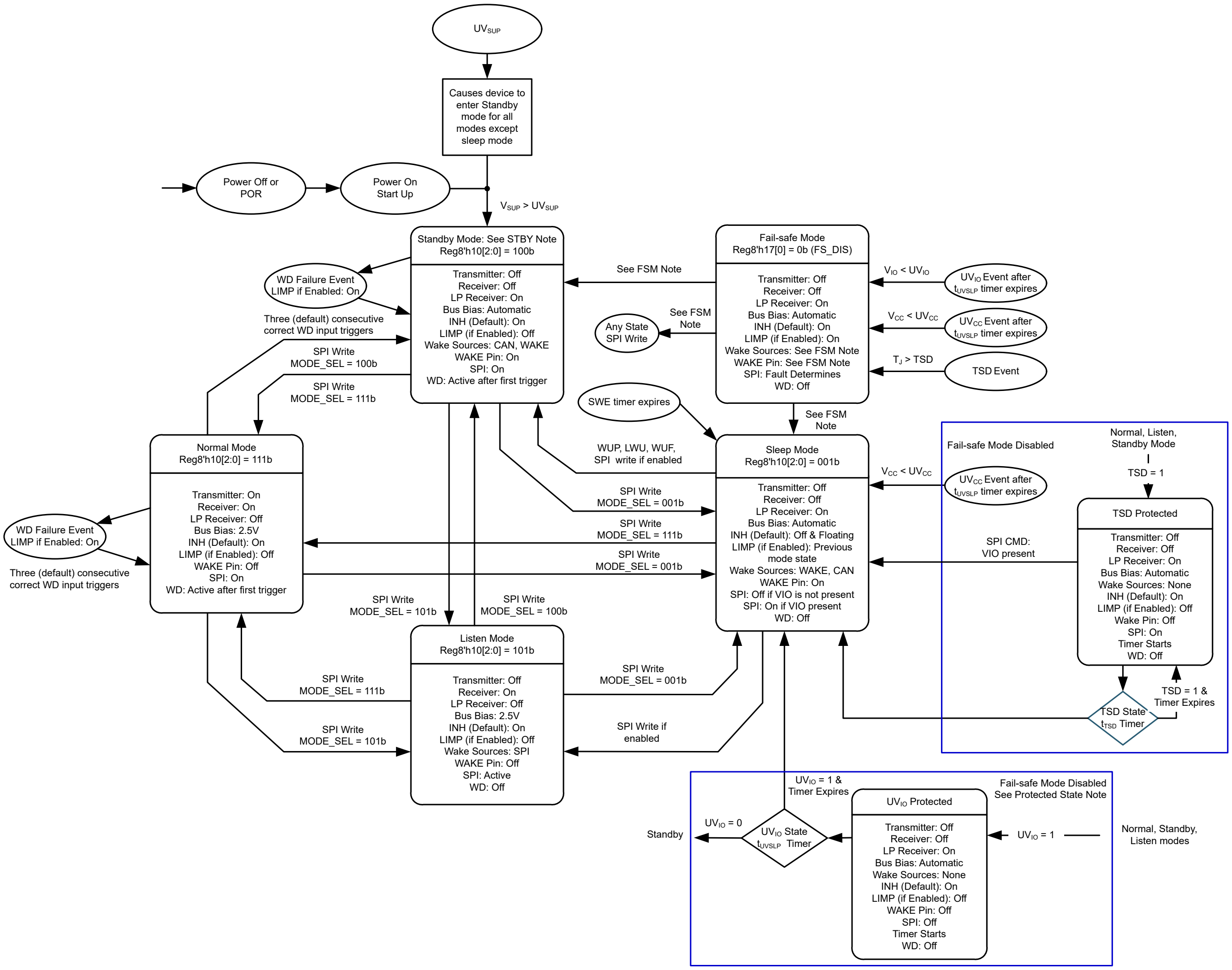

Figure 8-11. TCAN1576-Q1 Device State Diagram

Note

Notes for all Three Device State Diagrams

- Standby Mode Note (STBY Note)
  - When entering from Sleep mode, Fail-safe mode, or from a power up case, the SWE timer starts.
  - A mode change or clearing interrupts must take place prior to the SWE timer expiring.
- Fail-Safe Mode Notes (FSM Note)
  - To come out of Fail-Safe Mode the fault must be cleared.
    - A wake event must take place and enters Standby or
    - A SPI write can change to any state as long as faults are cleared.
  - If enabled, the SWE timer starts upon entering Fail-safe mode.
    - If the SWE timer times out the device enters Sleep mode.
    - The device still enters Sleep mode if SWE timer times out and faults clear if no wake event takes place.
- Protected State Notes
  - UVIO Protected status happens when the IO voltage rail that is aligned to the device is removed. Causing a mismatch between the device and the processor if the timer times out and UVIO = 1 the device goes to sleep.
  - If a Thermal Shutdown and UVIO event take place at the same time the device enters sleep mode.
- A UV_{SUP} enters UV_{SUP} mode and once V_{SUP} > UV_{SUPR} the device enters standby mode except for when this takes place in sleep mode. In sleep mode the device returns to sleep mode.

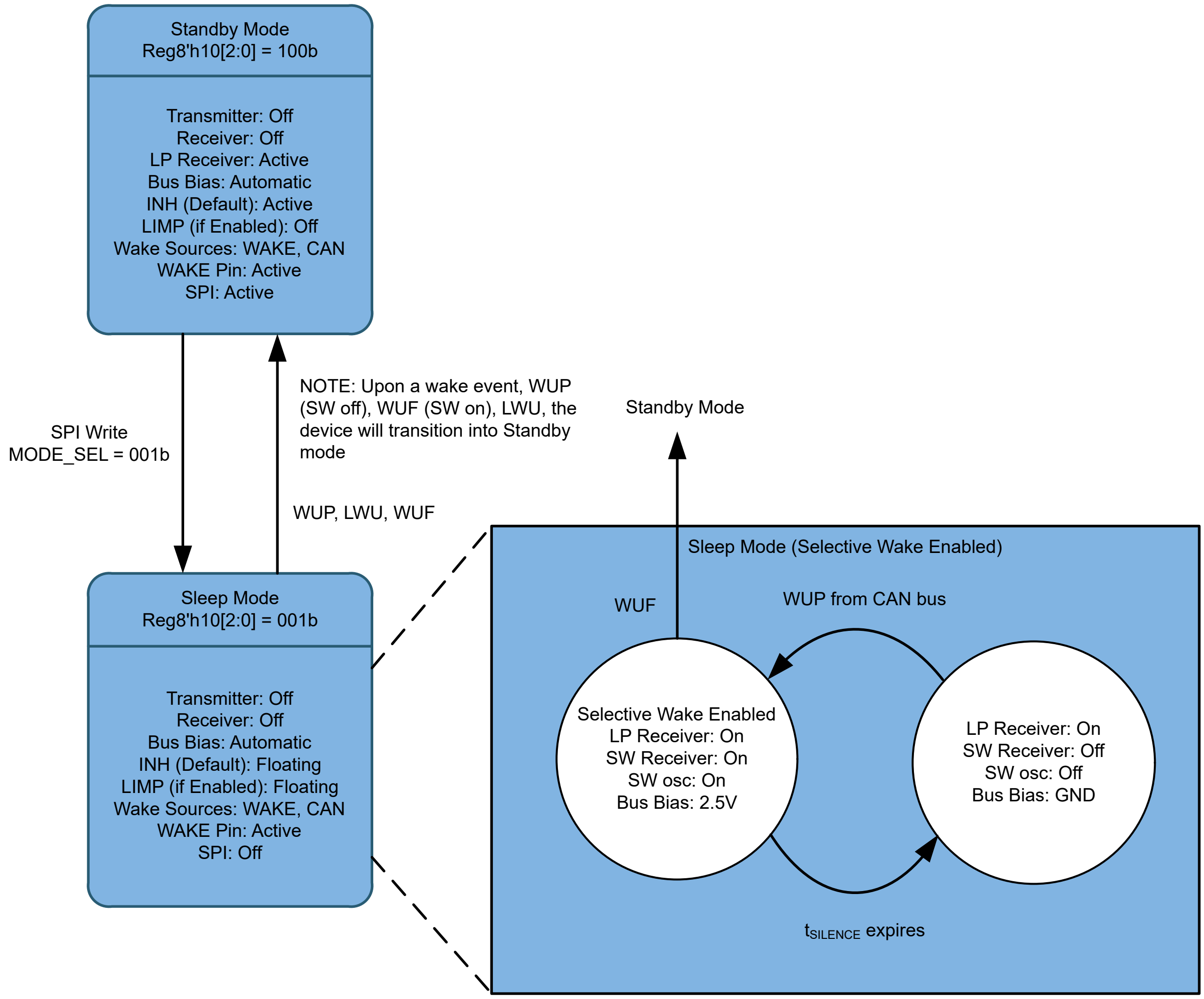

Figure 8-12. Selective Wake Enabled Sleep Mode

Note

For the state diagrams by default, SPI is off in sleep mode. If V_{IO} is present SPI works in sleep mode but at a reduced data rate, which includes selective wake sub state as shown in Figure 8-12.

8.4.1 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD signal from the CAN FD controller to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD signal to the CAN FD controller. Normal mode is enabled or disabled through SPI.

When fail-safe mode and the SWE timer are enabled, a SPI command to enter normal mode turns off the SWE timer. Clearing interrupts is recommended while in standby mode. There are two cases that cause the SWE timer, when enabled, to start while in normal mode.

- CANSLNT_SWE_DIS = 0b which starts the SWE timer after CANSLNT interrupt is set. CANSLNT interrupt needs to be cleared to stop the timer.
- CANSLNT_SWE_DIS = 1b (default) which starts the SWE timer when no bus activity is present for longer than $t_{SILENCE}$. Bus activity clears $t_{SILENCE}$ timer reset the SWE timer.

When the SWE timer times out, the device enters sleep mode.

Note

The SWE timer is disabled by default

8.4.2 Standby Mode

In standby mode, the bus transmitter does not send data nor does the normal mode receiver accept data. There are several blocks that are active in this mode. The low-power CAN receiver is actively monitoring the bus for the wake-up pattern (WUP). The WAKE pin monitor is active. SPI is active, so that the microprocessor can read and write registers in the memory for status and configuration. The INH pin is active to supply an enable to the V_{IO} controller if this function is used. The device goes from sleep mode to standby mode automatically upon a bus WUP event, WUF event or a local wake up from the WAKE pin. If V_{IO} is present, the device can wake up from a SPI mode change command.

Upon a wake event from sleep mode the TCAN1576-Q1 enters standby mode. If enabled, this transition starts the SWE timer, $t_{INACTIVE}$, that requires the processor to either reset the interrupt flags or configure the device to normal or listen modes. This feature makes sure the node is in the lowest power mode if the processor does not come up properly. This automatic mode change also takes place when the device has been put into sleep mode and receives a wake event, WUP, WUF or LWU. To enable this feature for sleep events, register 8'h1C[7] (SWE_EN) must be set to 1b.

The following provides the description on how selective wake interacts between sleep and standby modes.

- At power up, the device is in standby. Clear all Wake flags (PWRON, WUP/LWU), configure the Selective Wake registers, and then set selective wake config (SWCFG = 1b) and selective wake enable (SW_EN = 1b).
- When SWCFG = 1 and the device is placed into sleep mode the low-power WUP receiver is active and waiting for a WUP.
- Once a WUP is received, the WUF receiver is active.
- The device receives the wake-up frame and determines if the node has been requested to wake up.
  - If the WUF is a valid match, the device wakes up the node entering standby mode.
  - If the WUF is not a valid match, the device stays in sleep mode.
- A wake interrupt occurs from any type, WUF (CANINT), FRAME_OVF or LWU (if enabled), the device enters standby mode.

Note

When in standby mode, the RXD pin is released back to high when the PWRON, LWU, CANINT and FRAME_OVF interrupts have been cleared.

8.4.3 Listen Only Mode

In this mode, the CAN transmitter is disabled with only the receiver enabled. Data on the CAN bus is seen on the RXD pin but anything on the TXD does not reach the CAN bus. All other functionality is the same as Normal Mode. When fail-safe mode and SWE timer are enabled, the same behavior as provided in normal mode is present in listen only mode.

8.4.4 Sleep Mode

Sleep mode is similar to the standby mode except the SPI interface and INH typically are disabled. As the low-power CAN receiver is powered off of V_{SUP} the implementer can turn off V_{IO}. If V_{IO} is present in sleep mode, SPI access can take place but at a reduced rate. If at least a 10µs delay is used between pulling nCS low and the start of a read or write, the max SPI rate is used. If V_{IO} is off, the SPI interface is turned off and the only ways to exit sleep mode is by a wake-up event or power cycle. A sleep mode status flag is provided to determine if the device entered sleep mode through normal operation or if a fault caused the mode change. Register 8'h52[7] provides the status. If a fault causes the device to enter sleep mode, this flag is set to a one.

Note

Difference between Sleep and Standby Mode

- Sleep mode reduces whole node power by shutting off INH to the VREG enable pin, and thus, shutting off power to the node.
- Standby mode reduces TCAN1576-Q1 power from Normal mode but has higher power than Sleep mode, as INH is enabled, turning on node processors VREG.

When fail-safe mode is disabled, 8'h17[0]=0b; a fault that transitions the device to sleep mode clears CAN_SUP_DIS and SW_EN bits and will need to be reset if used.

8.4.4.1 Bus Wake via RXD Request (BWRR) in Sleep Mode

The TCAN1576-Q1 supports low-power sleep and standby modes and uses a wake up from the CAN bus mechanism called bus wake through RXD Request (BWRR). Once this pattern is received, the TCAN1576-Q1 automatically switches to standby mode from sleep mode and inserts an interrupt onto the nINT pin, if enabled, to indicate to a host microprocessor that the bus is active. The processor wakes up and services the TCAN1576-Q1. The low-power receiver and bus monitor are enabled in sleep mode to allow for RXD Wake Requests through the CAN bus. A wake-up request is output to the RXD (driven low) as shown in Figure 8-13. The external CAN FD controller monitors RXD for transitions (high to low) and reactivates the device to normal mode based on the RXD Wake Request. The CAN bus terminals are weakly pulled to GND during this mode, prior to BWRR if $t_{SILENCE}$ is expired (see Figure 7-2).

This device uses the wake-up pattern (WUP) from ISO 11898-2: 2024 Annex A to qualify bus traffic into a request to wake the host microprocessor. The bus wake request is signaled to the integrated CAN FD controller by a falling edge and low on the RXD terminal (BWRR).

The wake-up pattern (WUP) consists of

- A filtered dominant bus of at least t_{WK_FILTER} followed by
- A filtered recessive bus time of at least t_{WK_FILTER} followed by
- A second filtered dominant bus time of at least t_{WK_FILTER} followed by
- A second filtered recessive bus time of at least t_{WK_FILTER}

Once the WUP is detected, the device starts issuing wake up requests (BWRR) on the RXD pin. The behavior of this pin is determined by register 8h'12[2]. If 8h'12[2] = 0b the RXD pin is pulled low once the WUP pattern has been received that meets the dominant, recessive, dominant, recessive filtered times and $V_{IO} \geq UV_{IO}$ and $V_{CC} \geq UV_{CC}$. For cases where V_{IO} is present or requiring $V_{CC} \geq UV_{CC}$ not needed, the $V_{CC} \geq UV_{CC}$ requirement is disabled by setting VCC_DIS at 8'h4B[0] = 1b. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a second filtered dominant, other bus traffic does not reset the bus monitor. Once the second filtered dominant is received, the bus monitor is now waiting on a second filtered recessive, other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered recessive, the bus monitor recognizes the WUP and transitions to BWRR output.

For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER}, the following scenarios are applicable.

- Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP; thus, no BWRR is generated.
- Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ is detected as part of a WUP and a BWRR may be generated.
- Bus state times more than $t_{WK\_FILTER(MAX)}$ is always detected as part of a WUP; thus, a BWRR is always generated.

See Figure 8-13 for the timing diagram of the WUP.

The pattern and t_{WK_FILTER} time used for the WUP and BWRR prevents noise and a bus stuck dominant fault from causing false wake requests while allowing any CAN or CAN FD message to initiate a BWRR. If the device is switched to normal mode or an under voltage event occurs on V_{CC}, the BWRR is lost. The WUP pattern must take place within the $t_{WK\_TIMEOUT}$ time; otherwise, the device is in a state waiting for the next recessive and then a valid WUP pattern.

If 8h'12[2] = 1b, the RXD pin toggles low to high to low for t_{TOGGLE} = 10µs until the device is put into normal or listen mode. BWRR is active in standby mode upon power up and once coming out of sleep mode or certain fail-safe mode conditions. If a SPI write puts the device into standby mode, the RXD pin is high until a wake event takes place. The RXD pin then behaves as if waking up from sleep mode.

Note

If the CAN bus wake up capability is not needed, the capability is disabled by setting CAN_WUP_DIS 8'h1B[0] = 1b.

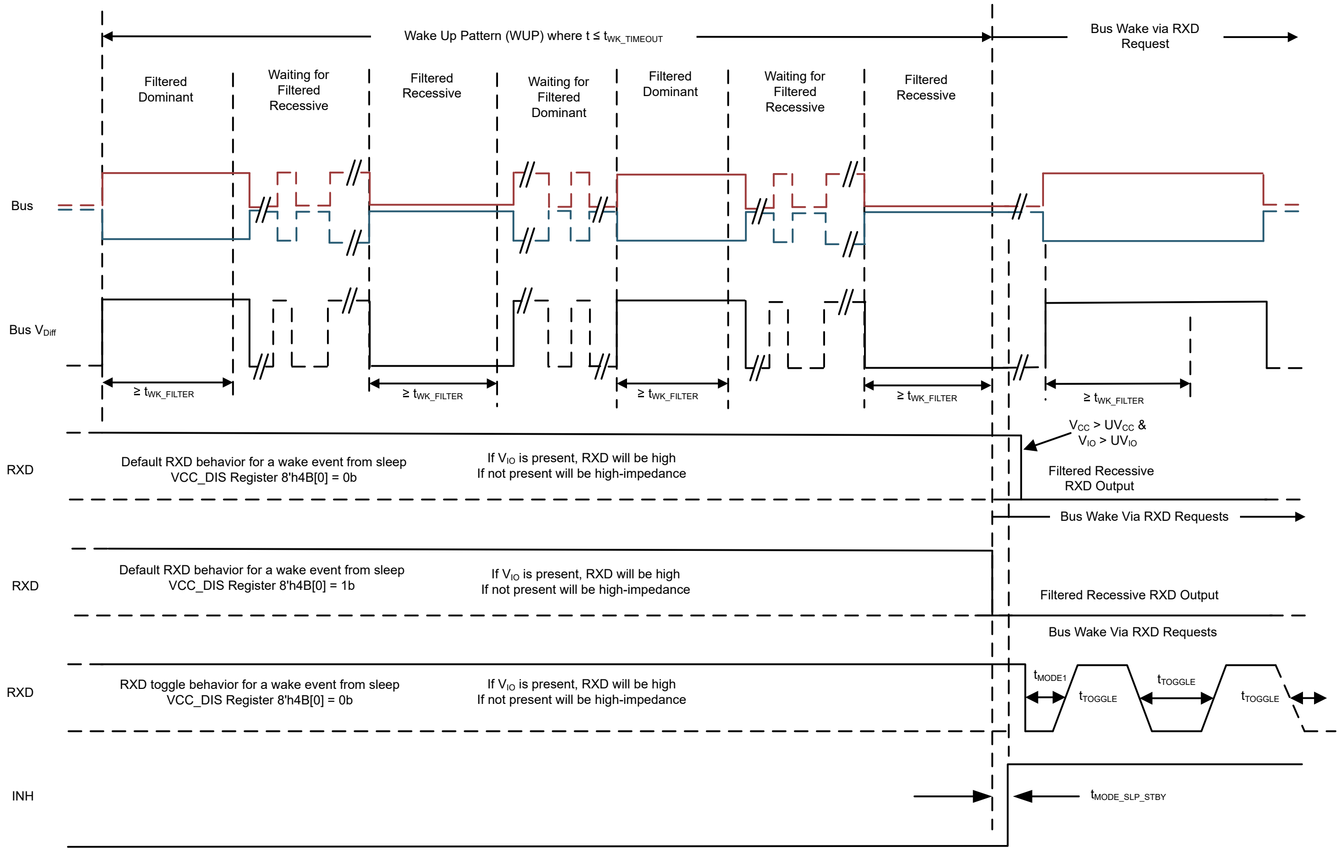

Figure 8-13. Wake Up Pattern (WUP) and Bus Wake via RXD Request (BWRR)

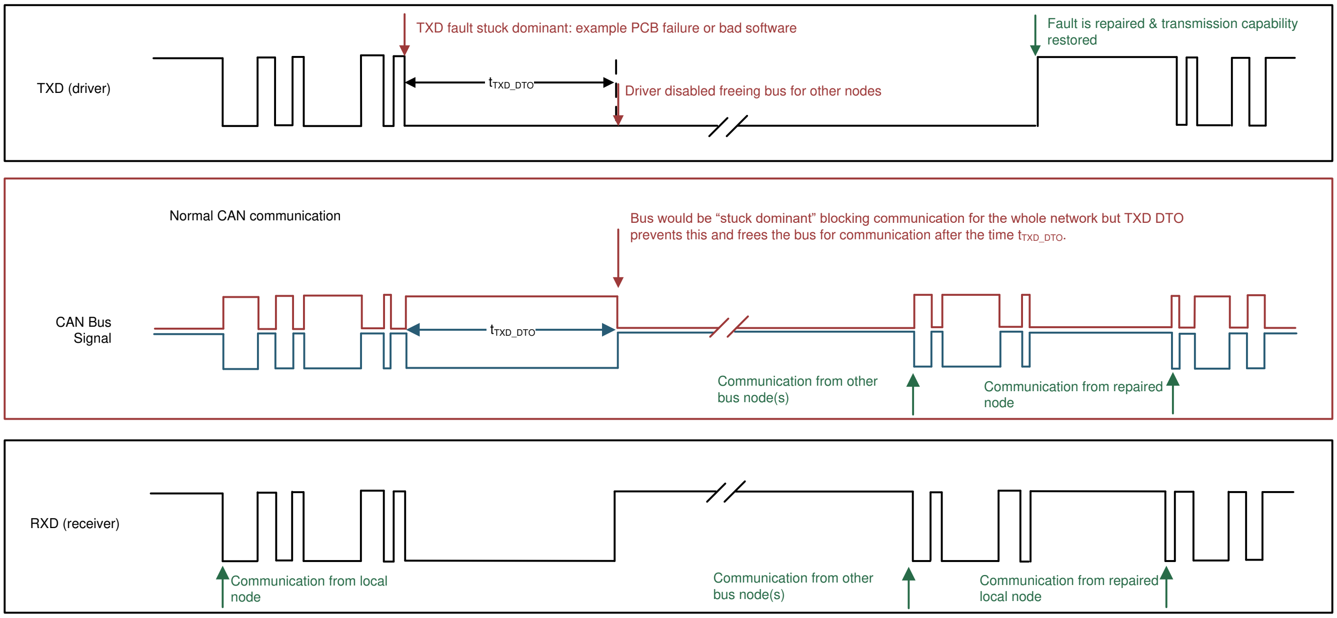

Figure 8-14. Example timing diagram with TXD DTO

8.4.4.2 Local Wake Up (LWU) via WAKE Input Terminal

The WAKE terminal is a ground biased input terminal that can support high voltage wake inputs used for local wake up (LWU) request via a voltage transition. The terminal triggers a LWU event on either a low to high or high to low transition as it has bidirectional input thresholds. This terminal may be used with a switch to V_{SUP} or ground. If the terminal is not used, pull the terminal to ground to avoid unwanted parasitic wake up events.

The WAKE terminal defaults to bidirectional input, but is configured for rising edge and falling edge transitions (see Figure 8-15 and Figure 8-16), by using WAKE_CONFIG register 11h[7:6]. Once the device enters sleep mode, the WAKE terminal voltage level must be at either a low state or high state for t_{WAKE} before a state transition for a WAKE input is determined.

There are two other wake methods that are used with the WAKE pin, a pulse wake and a filtered wake. For the pulsed wake input, a pulse on the WAKE pin must be within a specified time to be considered valid. A pulse width less than $t_{WAKE\_INVALID}$ is filtered out for both the pulse and filtered wake configurations. For the pulse configuration, the pulse must be between $t_{WK\_WIDTH\_MIN}$ and $t_{WK\_WIDTH\_MAX}$, see Figure 8-17. This figure provides three examples of pulses, and whether the device wakes or not. $t_{WK\_WIDTH\_MIN}$ is determined by the value for $t_{WK\_WIDTH\_INVALID}$ which is set by register 11h[3:2]. There are two regions where a pulse may or may not be detected. By using register 1Bh[1], WAKE_WIDTH_MAX_DIS, the pulse mode is configured as a filtered wake input. Writing a 1b to this bit disables $t_{WK\_WIDTH\_MAX}$, and the WAKE input is based upon the configuration of register 11h[3:2] which selects a $t_{WK\_WIDTH\_INVALID}$ and $t_{WK\_WIDTH\_MIN}$ value. A WAKE input of less than $t_{WK\_WIDTH\_INVALID}$ is filtered out, and if longer than $t_{WK\_WIDTH\_MIN}$, INH turns on, and the device enters standby mode. The region between the two may or may not be recognized, see Figure 8-18. Register 12h[7] determines the direction of the pulse or filter edge that is recognized. The status of the WAKE pin is determined from register 11h[5:4]. When a WAKE pin change takes place, the device registers this as a rising edge or falling edge. This is latched until a 00b is written to the bits.

The LWU circuitry is active in sleep mode, standby mode and transition state of going to sleep. If a valid LWU event occurs the device transitions to standby mode. The LWU circuitry is not active in normal mode. A constant high level on WAKE has an internal pull up to V_{SUP}, and a constant low level on WAKE has an internal pull down to GND. On power up, this looks like a LWU event, and is flagged as such.

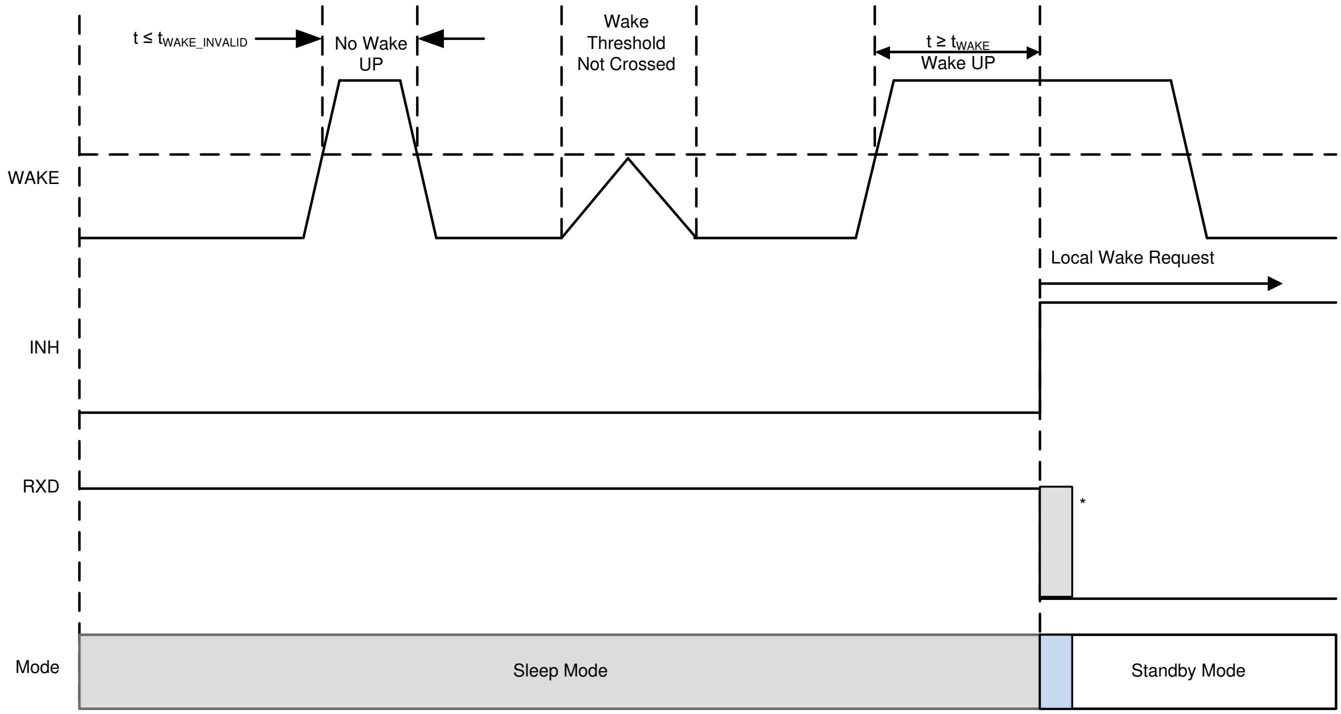

Figure 8-15. Local Wake Up – Rising Edge

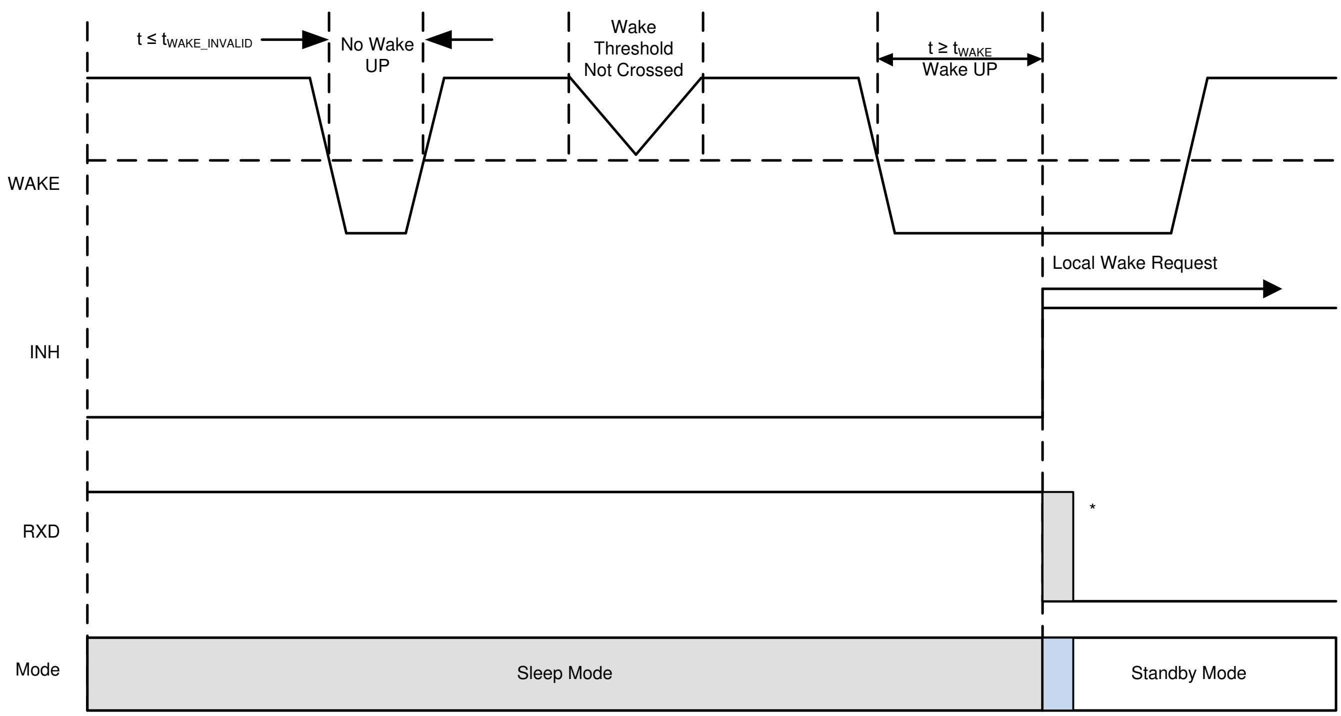

Figure 8-16. Local Wake Up – Falling Edge

Note

When either a rising or falling edge is selected for the WAKE pin the state prior to the edge requires a t_{WAKE} period of time.

- If a rising edge is selected and the device goes to sleep with WAKE high, a low of at least t_{WAKE} must be present prior to the rising edge wake event
- If a falling edge is selected and the device goes to sleep with WAKE low, a high of at least t_{WAKE} must be present prior to the falling edge wake event
- This requirement is not necessary for a bidirectional edge (default)
- Figure 8-15 and Figure 8-16 provide examples of a rising or falling edge WAKE input. t_{WAKE} is based upon the time it takes from a valid WUP to INH turning on. RXD is pulled low once V_{IO} > UV_{IO} and V_{CC} > UV_{CC} and standby mode is entered.

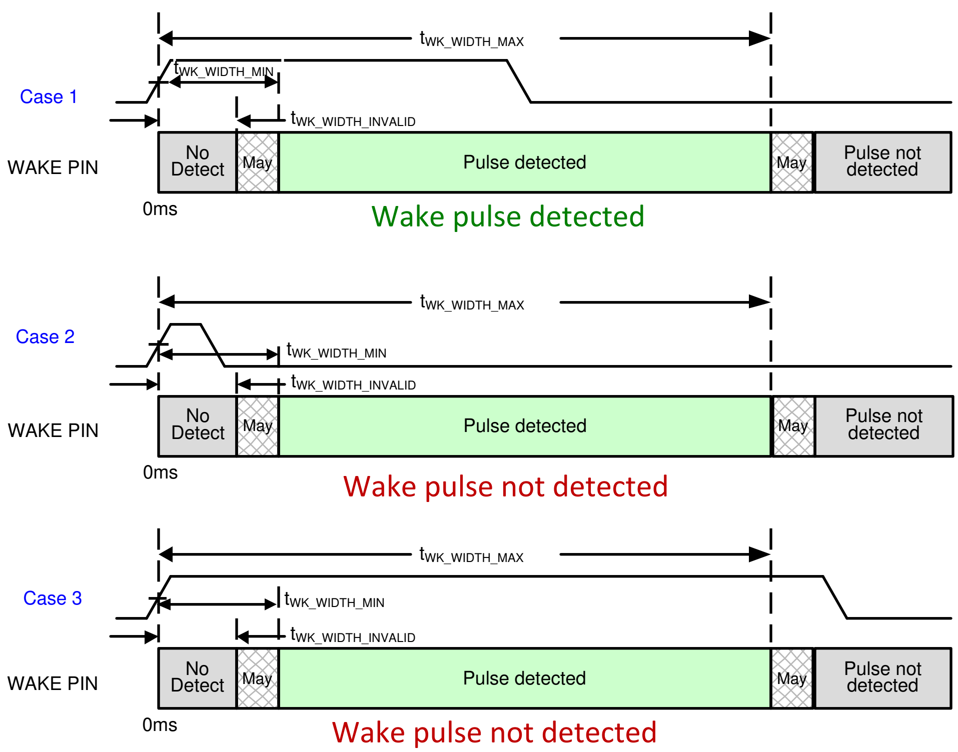

Figure 8-17. WAKE Pin Pulse Behavior

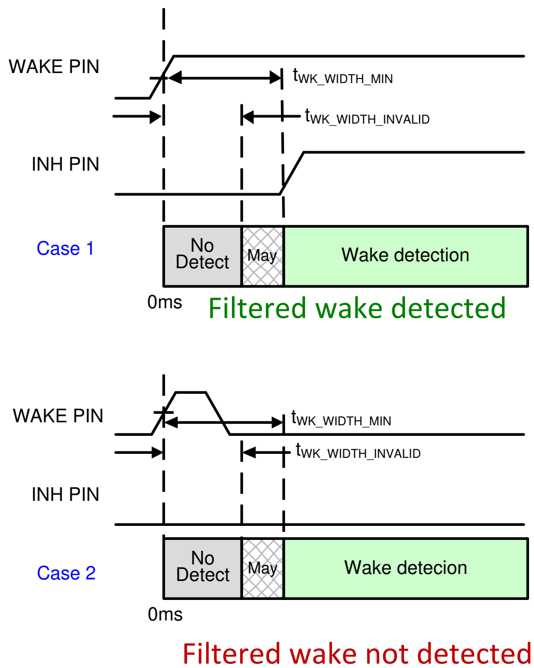

Figure 8-18. WAKE Pin Filtered Behavior

8.4.5 Selective Wake-up

The devices support selective wake-up according to ISO 11898-2:2024.

8.4.5.1 Selective Wake Mode

This is the medium level of power saving mode of the device. The WUF receiver is turned on and connected internally to the frame detection logic which is looking for a Wake-Up Frame (WUF) as outlined in the Frame Detection section of the data sheet. The CAN bus data is not put on the RXD pin in this state. The device is supplied by the V_{SUP} supply coming from the system battery.

The valid wakes up sources in selective wake mode are:

- Wake-Up Frame (WUF)
- WAKE pin local wake up (LWU). Event on WAKE pin must match the programmed requirements for WAKE pin in register 8'h11[7:6]
- Frame Overflow (FRAME_OVF)
- SPI command to another state

If a WUF and/or LWU event occurs, the wake request for the corresponding wake-event flag (WUF and/or LWU) is set. At this point, an interrupt is provided to the MCU using the nINT pin (if enabled) and by pulling down the RXD pin.

To enter selective wake mode, the following conditions must be met:

- Selective Wake Configured (SWCFG) flag is set
  - All Selective Wake registers must be written followed by a read to be sure all registers are programmed correctly for the proper frame detection and selective wake configuration. Once configured, the SWCFG bit needs to be set to 1b.
- Selective Wake Error (SWERR) flag is cleared
- Set Selective Wake Enable (SW_EN) = 1b, register 8'h10[7] = 1b

Note

If a fault condition or FRAME_OVF forces the device into sleep mode, fail-safe mode disabled, or into fail-safe mode SW_EN is disabled turning off selective wake function.

Note

For selective wake to work properly, a WUP signal is required, therefore the recommendation is that the CAN_WUP_DIS set to 0b in the DEVICE_CONFIG2 register in Section 10.1.17 before sending the device to sleep mode.

8.4.5.2 Frame Detection

The frame detection logic is what enables processing of serial data, or CAN frames, from the CAN bus. The device has selective wake control registers to set up the device to look for a programmed match using either the CAN ID (11 bit or 29 bit), or the CAN ID plus the data frame including data masking. If the detected CAN frame received from the bus matches the configured requirements in the frame detection logic and is called Wake-Up Frame (WUF).

Before frame detection is enabled or used, the data needed for validation, or match, of the WUF needs to be correctly configured in the device registers. Once the device has been correctly configured to allow frame detection, or selective wake function the SWCFG (Selective Wake Configuration) must be set to load the parameters for WUF for the device. If a valid WUF is detected, the CANINT flag indicates this and includes selective wake-up.

When frame detection is enabled and the bus is biased to 2.5V from a valid WUP, several other actions take place as the logic is decoding the CAN frames the device receives on the bus. These actions include detecting errors, counting, and the indicating the reception of a CAN frame through the CAN_SYNC and CAN_SYNC_FD flags.

If a Frame Overflow (FRAME_OVF) occurs while in frame-detection mode, selective wake is disabled, clearing the SW_EN bit.

When Frame Detection is enabled, transitioning from a mode where the receiver bias is not on, up to four CAN frames for 500kbps and slower data rates and up to eight CAN frames for greater than 500kbps is ignored by the device until the frame detection is stabilized.

The procedure to correctly configure the device to use frame detection and selective wake up is:

- Write all control registers for frame detection (selective wake), Selective Wake Config 1-4 (Registers 8'h44 through 8'h47), and ID and ID mask (Registers 8'h30 and 8'h40).
- Recommend reading all Selective Wake registers, allowing the software to confirm the device was written and thus configured properly.
- Set Selective Wake Configured (SWCFG) bit to 1b, register 8'4F[7] = 1b.
- Set Selective Wake Enable = 1b, register 8'h10[7] = 1b.

If a SWERR interrupt then occurs from the Frame Overflow flag, the Frame Overflow interrupt needs to be cleared, and then the SWCFG bit must be set again to 1b.

8.4.5.3 Wake-Up Frame (WUF) Validation

When the following conditions are all met, the received frame shall be valid as a wake-up Frame (WUF):

- The received frame is a classical CAN data frame when DLC (Data Length Code) matching is not disabled. The frame can also be a remote frame when DLC matching is disabled.
- The ID (as defined in ISO 11898-1:2024, 8.4.2.2) of the received classical CAN frame is exactly matching a configured ID in the relevant bit positions. The relevant bit positions are given by an ID-mask illustrated in WUF DLC Validation
- The DLC (as defined in ISO 11898-1:2024, 8.4.2.4) of the received classical CAN data frame is exactly matching a configured DLC. See the mechanism illustrated in Figure 8-20. Optionally, this DLC matching condition is disabled by configuration in the implementation.
- When the DLC is greater than 0 and DLC matching is enabled, the data field (as defined in ISO 11898-1:2024, 8.4.2.5) of the received frame has at least one bit set in a bit position which corresponds to a set bit in the configured data mask. See the mechanism illustrated in WUF DLC Validation.
- A correct cyclic redundancy check (CRC) has been received, including a recessive CRC delimiter, and no error (according to ISO 11898-1:2024, 10.11) is detected prior to the acknowledgment (ACK) Slot.

8.4.5.4 WUF ID Validation

The ID of the received frame matches the configured ID in all required bit positions. The relevant bit positions are determined by the configured ID in 8'h30 through 8'h33 and the programmed ID mask in 8'h34 through 8'h38. Classic Base Frame Format (CBFF) 11-bit Base ID and Classic Extended Frame Format (CEFF) 29-bit Extended ID and ID masks are supported. All masked ID bits except "do not care" must match exactly the configured ID bits for a WUF validation. If the masked ID bits are configured as "do not care" then both "1" and "0" are accepted in the ID. In the ID mask register a 1 represents “do not care”.

Figure 8-19 shows an example for valid WUF ID and corresponding ID Mask register

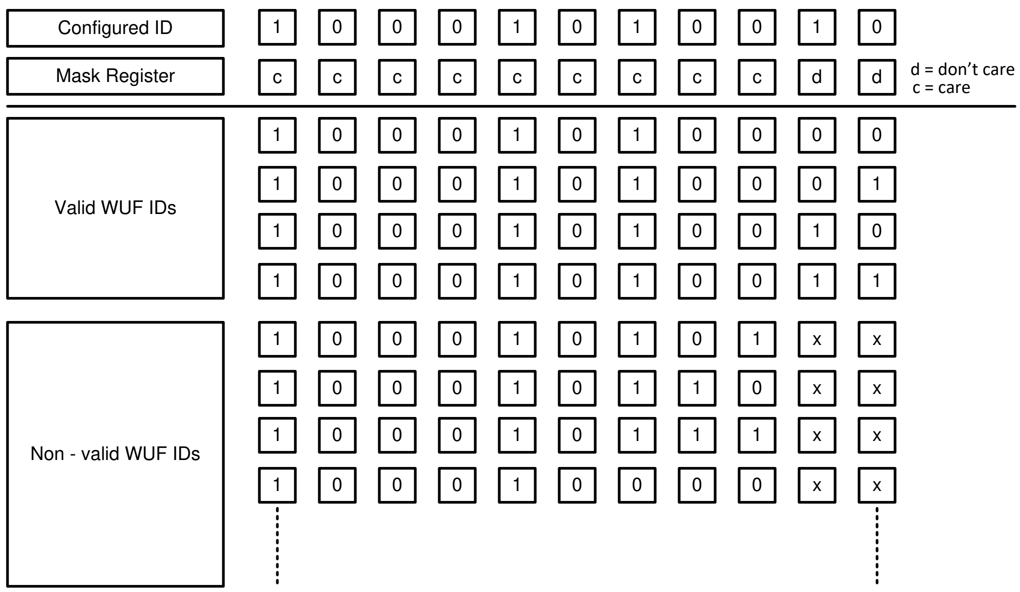

Figure 8-19. ID and ID Mask Example for WUF

8.4.5.5 WUF DLC Validation

The DLC (Data Length Code) of the received frame must match exactly the configured DLC if the data mask bit is set. The DLC is configured in 8'h38[4:1]. The data mask bit is set in 8'h38[0]. While the FD DLC are included in this table, selective wake only works for classic CAN frames, so CAN FD codes aren't used in WUF validation.

Table 8-2. DLC

Frames	Data Length Code				Number of Data Bytes
	DLC3	DLC2	DLC1	DLC0	
Classical Frames & FD Frames	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
Classical Frames	1	0 or 1	0 or 1	0 or 1	8

Table 8-2. DLC (continued)

Frames	Data Length Code				Number of Data Bytes
	DLC3	DLC2	DLC1	DLC0	
FD Frames	1	0	0	1	12
	1	0	1	0	16
	1	0	1	1	20
	1	1	0	0	24
	1	1	0	1	32
	1	1	1	0	48
	1	1	1	1	64

8.4.5.6 WUF Data Validation

When the data mask is enabled through the data mask bit, the data of the received frame must match the configured data where at least one logic high (1) bit within the data field of the received frame matches a logic high (1) of the data field within the configured data. The relevant bit positions are determined by the configured Data in 8'h39 through 8'h40 and enabled by data mask enable in 8'h38[0]. An example of a matching and non-matching data is shown in Figure 8-20

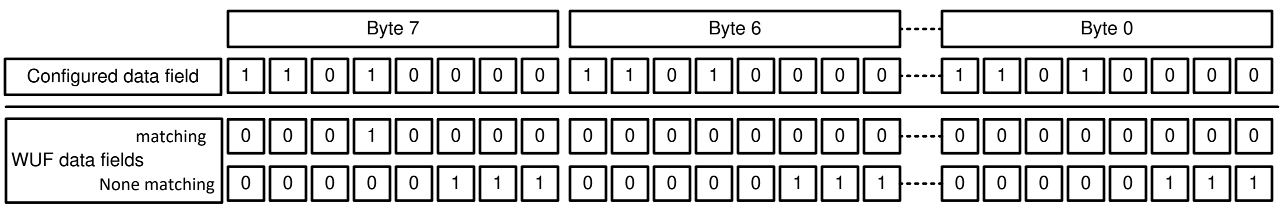

Figure 8-20. Data Field Validation for WUF Example

The selective wake data validation makes sure the last byte sent on the bus is interpreted as data mask byte 0. This means for 8 bytes of data, the first byte sent is interpreted as data mask byte 7. For a DLC of 3, the last byte sent on the bus is interpreted as data mask byte 0 and the first byte sent is interpreted as data mask byte 2. The following are a few examples of which bytes are used for various bytes sent and received.

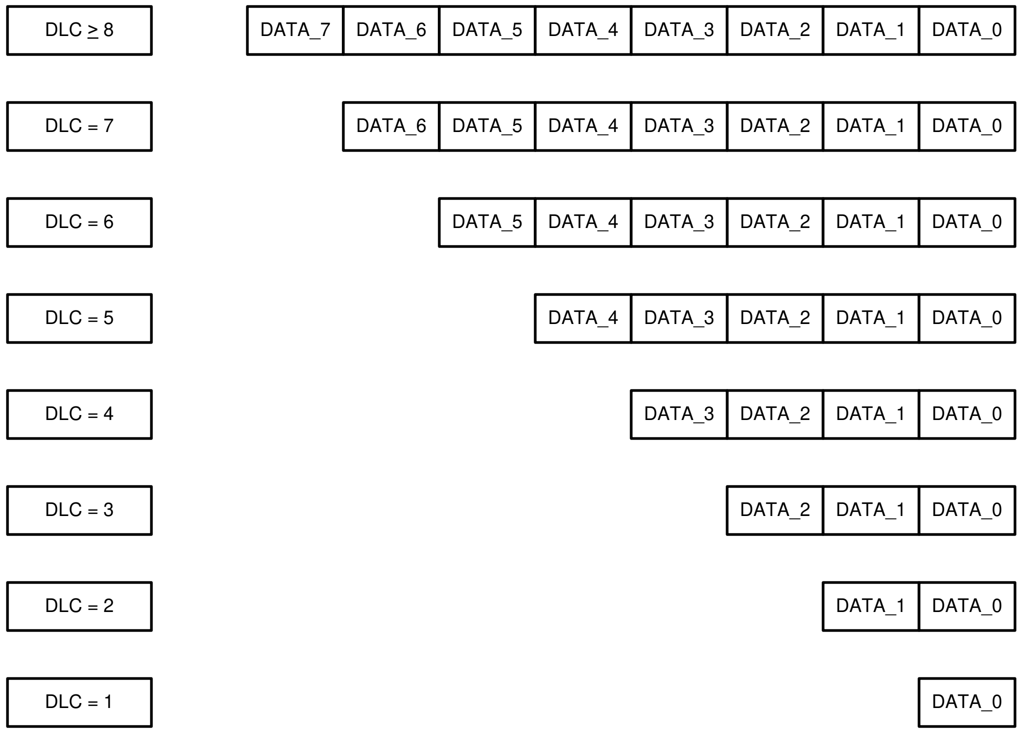

Figure 8-21. Data register mask values for different DLC values

8.4.5.7 Frame error counter

Upon activation of the selective wake up function and upon the expiration of $t_{SILENCE}$, the CAN frame error counter is set to zero. This error counter determines the CAN frame errors detected by the device. The error counter is at 8'h45 and is called FRAME_CNTx.

The initial counter value is zero and is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. If the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame has no impact on the frame error counter (no increment or decrement). If a valid classical CAN frame has been received and the counter is not zero, the counter shall be decremented by one. Dominant bits between the CRC delimiter and the end of the intermission field do not increase the frame error counter.

On each increment or decrement of the error counter, the decoder unit waits for nBits_idle recessive bits before considering a dominant bit as a start of frame (SOF). See Figure 8-22 for the position of the mandatory start of frame detection when classic CAN frame was received and in case of error scenario.

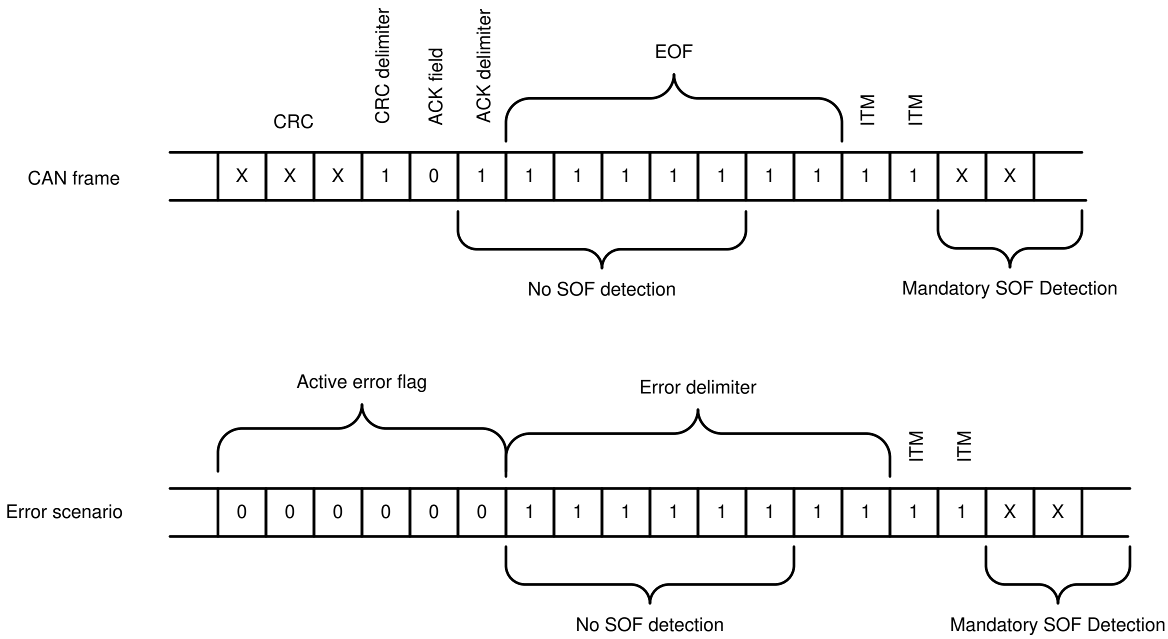

Figure 8-22. Mandatory SOF Detection after Classic CAN Frames and Error Scenarios

The default value for the frame error counter threshold is 31, so that on the 32nd error, the frame overflow flag (FRAME_OVF) is set.

When the WUP is sent, the CAN bus will bias to a recessive level, activating the WUF receiver. Up to four (or eight when bit rate > 500kbps) consecutive classic CAN data and/or remote frames that start after the bias reaction time, t_{Bias}, has elapsed or ignored. There is no error counter increase or failure, or judged as erroneous (error counter increases even in case of no error).

Received frames in CEFF with non-nominal reserved bits (SRR, r0) do not lead to an increase of the error counter.

The frame error counter is compared to the frame error counter threshold, FRAME_CNT_THRESHOLD in 8'h46. If the counter overflows the threshold, the frame error overflow flag, FRAME_OVF, is set. The default value for the frame error counter threshold is 31 so that on the 32nd error the overflow flag is set. However, if the application requires a different frame error count overflow threshold, program the required value into the FRAME_CNT_THRESHOLD register.

The counter is reset by the following: disabling the frame detection, CANSLNT flag set, and setting register 8'h46 = 1b.

The description for the errors detected:

- **Stuff bit error:** A stuff bit error is detected when the 6th consecutive bit of the same state (level) is received. CAN message coding has had a stuff bit at this bit position in the data stream.
- **CRC error:** The CRC sequence consists of the result of the CRC calculation by the transmitting node. This device calculates the CRC with the same polynomial as the transmitting node. A CRC error is detected if the calculated result is not the same as the result received in the CRC sequence.
- **CRC delimiter error:** The CRC delimiter error is detected when a bit of the wrong state (logic low / dominant) is received in the CRC delimiter bit position which is defined as logic high (recessive).

8.4.5.8 CAN FD Frame Tolerance

After receiving a FD Format indicator (FDF) followed by a dominant res bit, the decoder unit waits for n_{Bits_idle} recessive bits before considering a further dominant bit as a SOF as per Figure 8-22. Table 8-3 defines n_{Bits_idle}.

Table 8-3. Number of Recessive Bits Prior to Next SOF

Parameter	Notation	Value	
		Min	Max
Number of recessive bits before a new SOF is accepted	n_{Bits_idle}	6	10

There are two bitfilter options available to support different combinations of arbitration and data phase bit rates. Register 8'h47[4] is where the $p_{Bitfilter}$ option is selected.

- Bitfilter 1: A data phase bit rate ≤ four times the arbitration rate or 2Mbps whichever is lower shall be supported
- Bitfilter 2: A data phase bit rate ≤ ten times the arbitration rate or 5Mbps whichever is lower shall be supported

Dominant signals ≤ the minimum pBitfilter, see Table 8-4, of the arbitration bit time in duration is not considered valid and does not restart the recessive bit counter. Dominant signals ≥ the maximum of pBitfilter of the arbitration bit time duration restart the recessive bit counter.

Table 8-4. Number of Recessive Bits Prior to Next SOF

Parameter	Notation	Value	
		Min	Max
CAN FD data phase bitfilter 1	pBitfilter1	5.00%	17.50%
CAN FD data phase bitfilter 2	pBitfilter2	2.50%	8.75%

8.4.6 Fail-safe Features

The TCAN1576-Q1 has fail-safe features used to reduce node power consumption for a node system issue. Separating into two operation modes, sleep and fail-safe.

8.4.6.1 Sleep Mode via Sleep Wake Error

The sleep wake error (SWE) timer is a timer used to determine if specific external and internal functions are working and is disabled by default. Figure 8-23 provides an overview of when SWE timer is on and starts or off when fail-safe mode is enabled. This feature is enabled by setting 8'h1C[7] SWE_EN to 1b.

If enabled, when the device wakes up from a CAN bus WUP or a local wake standby mode is entered. Once in standby mode, the $t_{SILENCE}$ and $t_{INACTIVE}$ timers start. If $t_{INACTIVE}$ expires, the device re-enters sleep mode. When the device receives a CANINT, LWU or FRAME_OVF such that the device leaves sleep mode and enters standby mode, the processor has until $t_{INACTIVE}$ expires to clear the flags and place the device into normal mode. If this does not happen, the device enters sleep mode. When in standby, normal or listen mode and $t_{SILENCE}$ (SWE_EN=1b) or CANSLNT (SWE_DIS=0b) persists for $t_{INACTIVE}$, the device enters sleep mode. Examples of events that can create this are the processor is no longer working and not able to exercise the SPI bus, a go to sleep command comes in and the processor is not able to receive the command or is not able to respond.

Note

If the INH/LIMP pin for the TCAN1576-Q1 is configured as a LIMP pin, the $t_{INACTIVE}$ expiration causes the LIMP pin to assert and stay on until turned off by the processor.

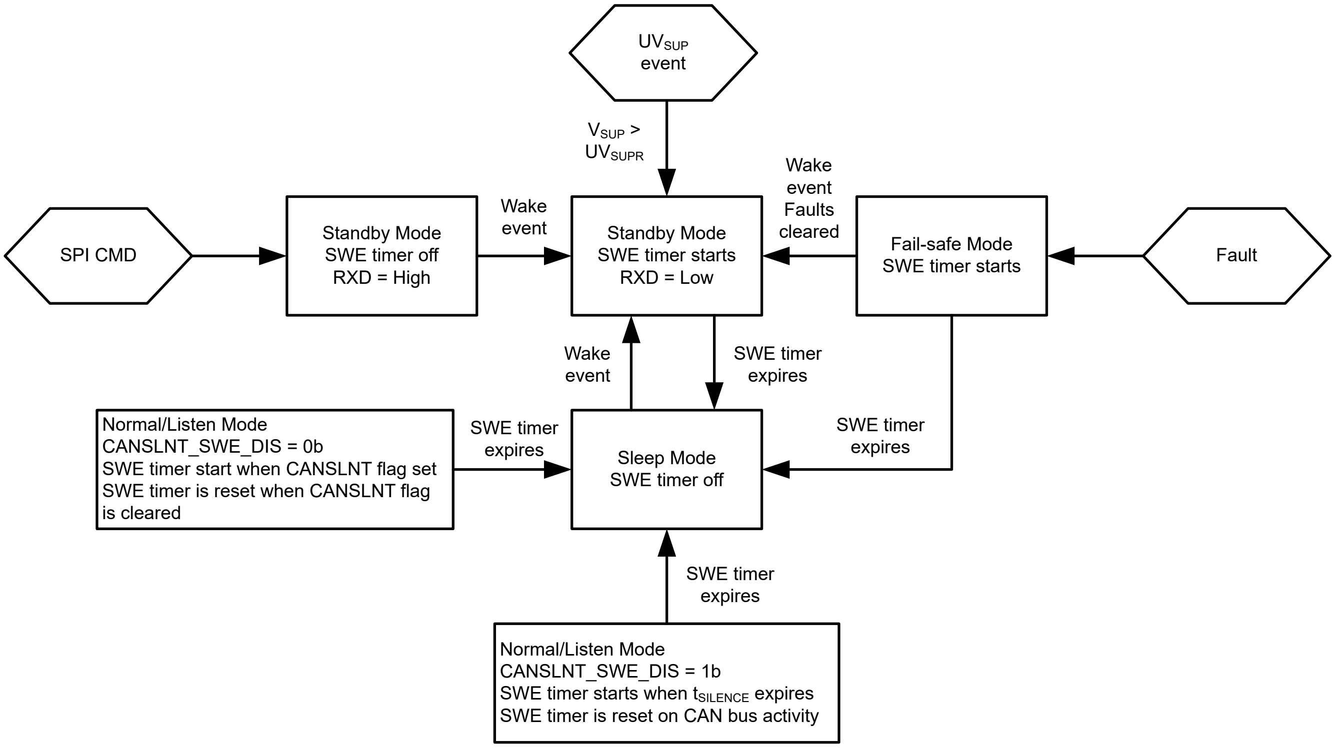

Figure 8-23. Sleep Wake Error (SWE) Timer if Enabled

8.4.6.2 Fail-safe Mode

Fail-safe mode is a low-power mode that different faults can cause the device to enter. Once in this mode, the SWE timer starts, if enabled. This provides a window of time to clear the faults and receive a wake event. If the faults are not cleared or a wake event doesn't take place prior to $t_{INACTIVE}$ the device enters sleep mode to reduce power consumption. The fault must be cleared before a wake event is recognized for the device to enter the correct operating mode. This mode is default on and is disabled by setting register 8'h17[0] = 1b. A fail-safe mode counter is available so that, after a set number of events in a row, the device performs the programmed action, which can include going to sleep. A WUP or LWU event does not wake the device. A power-on reset is required. The counter is default disabled and is enabled at 8'h17[7]. The counter expiration action is at 8'h17[6:4]. The number of events before action is programmed is set at 8'h18[7:4] with a value up to 15 events. 8'h18[3:0] runs the up and down fail-safe event counter that is read and cleared.

If fail-safe mode is entered, a global interrupt is issued at 8'h53[5], and the reason for entering fail-safe mode is provided by register 8'h17[3:1].

Note

- Fail-safe counter counts each event. The term "in a row" means each event that happens without the counter being cleared and does not mean within a specified time.
- The fail-safe counter needs to be cleared after each time the device enters fail-safe mode to avoid unwanted actions.
- Entering fail-safe mode clears CAN_WUP_DIS and SW_EN bits and need to be reset if used.

8.4.7 Protection Features

The TCAN1576-Q1 has several protection features that are described as follows.

8.4.7.1 Driver and Receiver Function

The TXD and RXD pins are input and output between the processor and the CAN physical layer transceiver. The digital logic input and output levels for these devices are TTL levels for compatibility with protocol controllers having 1.8V, 3.3V or 5V logic or I/O. Table 8-5 and Table 8-6 provides the states of the CAN driver and CAN receiver in each mode.

Table 8-5. Driver Function Table

DEVICE MODE	TXD INPUT	BUS OUTPUTS		DRIVEN BUS STATE
		CANH	CANL	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Biased Recessive
Standby	X	Z	Z	Weak Pull to GND
Listen	X	Z	Z	Biased to ~ 2.5V
Sleep	X	Z	Z	Weak Pull to GND

Table 8-6. Receiver Function Table Normal and Standby Modes

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD TERMINAL
Normal/Listen	$V_{ID} \geq 0.9V$	Dominant	L
	$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	H
Standby/Sleep	$V_{ID} \geq 1.15V$	Dominant	See Figure 8-13
	$0.4V < V_{ID} < 1.15V$	Undefined	
	$V_{ID} \leq 0.4V$	Recessive	
Any	Open ($V_{ID} \approx 0V$)	Open	H

8.4.7.2 Floating Terminals

There are internal pull ups on critical terminals to place the device into known states if the terminal floats. See Table 8-7 for details on terminal bias conditions.

Table 8-7. Terminal Bias

TERMINAL	PULL UP or PULL DOWN	COMMENT
SCK	Pull up	Weakly biases input
SDI	Pull up	Weakly biases input
nCS	Pull up	Weakly biases input so the device is not selected
RXD	Pull up	Active when CAN transceiver is off.
TXD	Pull up	Weakly biases input

Note

The internal bias is not be relied upon as only termination, especially in noisy environments, but is considered a fail-safe protection. Special care needs to be taken when the device is used with MCUs using open drain outputs.

8.4.7.3 TXD Dominant Time Out (DTO)

The TCAN1576-Q1 supports dominant state time out. This is an internal function based upon the TXD path. The TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant (LOW) longer than the time out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen on TXD terminal, thus, clearing the time out constant of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal (HIGH) is seen on TXD terminal;

thus, clearing the dominant time out. The receiver remains active and the RXD terminal reflects the activity on the CAN bus and the bus terminals is biased to recessive level during a TXD DTO fault. The feature is disabled by using register 8'h10[6] = 1b, DTO_DIS.

Note

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame.

8.4.7.4 CAN Bus Short Circuit Current Limiting

These devices have several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive). The device has TXD dominant time out which prevents permanently having the higher short circuit current of dominant state for a system fault. During CAN communication the bus switches between dominant and recessive states; thus, the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings, the average short circuit current is used. The percentage dominant is limited by the TXD dominant time out and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and inter frame space. This provides a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

Note

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using Equation 1.

$$I_{OS(AVG)} = \%Transmit \text{ x } [(\%REC\_Bits \text{ x } IOS(SS)\_REC) + (\%DOM\_Bits \text{ x } IOS(SS)\_DOM)] + [\%Receive \text{ x } IOS(SS)\_REC] \quad (1)$$

Where

- $I_{OS(AVG)}$ is the average short circuit current.
- %Transmit is the percentage the node is transmitting CAN messages.
- %Receive is the percentage the node is receiving CAN messages.
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages.
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages.
- IOS(SS)_REC is the recessive steady state short circuit current and IOS(SS)_DOM is the dominant steady state short circuit current.

Note

The short circuit current and possible fault cases of the network is taken into consideration when sizing the power ratings of the termination resistance, other network components, and the power supply used to generate V_{SUP}.

8.4.7.5 Thermal Shutdown

The TCAN1576-Q1 has two trigger points for thermal events. The first is a thermal shutdown warning. Once the temperature exceeds this limit, an interrupt is issued. The second is the actual thermal shutdown (TSD) event. This is a device preservation event. If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN transceiver and CAN transceiver circuitry, thus blocking the signal to bus transmission path. A thermal shut down interrupt flag is set, and an interrupt is inserted so that the microprocessor is informed. If this event happens, other interrupt flags may be set as an example a bus fault where the CAN bus is shorted to V_{BAT}. When this happens, the digital core and SPI interface is still active. After a time of ≈ 300ms the device checks the temperature of the junction. Thermal shutdown timer, t_{TSD}, starts when

TSD fault event starts and exit to sleep mode when TSD fault is not present when TSD timer is expired. While in thermal shut down protected mode, a SPI write to change the device to either Normal or Standby mode is ignored while writes to change to sleep mode are accepted.

If the TSD event takes place and fail-safe mode is enabled, the same process takes place with and instead off thermal shut down protected stated it enters fail-safe mode.

Note

If a thermal shut down event happens while the device is experiencing a V_{IO} under voltage event, the device enters sleep mode if fail-safe mode is disabled.

8.4.7.6 Under-Voltage Lockout (UVLO) and Unpowered Device

There are three under-voltage events monitored in the TCAN1576-Q1, V_{SUP}, V_{IO} and V_{CC}. The three supply terminals are input sources for the TCAN1576-Q1 and have under-voltage detection circuitry which places the device in a protected state if an under-voltage fault occurs, UV_{SUP}, UV_{CC} and UV_{IO}. This protects the bus during an under-voltage event on these terminals. If V_{SUP} experiences an under-voltage event while in standby mode, the device loses the source needed to keep the internal regulators active. Causing the device to go into a state where communication between the microprocessor and the TCAN1576-Q1 is disabled. The TCAN1576-Q1 is not able to receive information from the bus; and thus, does not pass any signals from the bus, including any Bus Wake via the BWRR signals to the microprocessor. See Table 8-9. For under-voltage events, there is a filter time, t_{UVFLTR}, that the even must last longer than for the t_{UVSLP} timer to start. Once the t_{UVSLP} timer expires and the under-voltage condition is still present, the device enters sleep mode or fail-safe mode if enabled.

8.4.7.6.1 UV_{SUP}, UV_{CC}

If UV_{SUP} decreases to below UV_{SUPF}, the device is in standby mode for any case except for when the device is in sleep mode. When in sleep mode, a UV_{SUP} event does not cause the device to transition to standby mode. A UV_{SUP} event causes the INH pin to turn off. When V_{SUP} is greater than UV_{SUP}, INH turns on and the SWE timer starts if enabled. If V_{SUP} decreases below $V_{SUP(PU)F}$, the TCAN1576-Q1 shuts everything down as the POR level has been reached. When V_{SUP} returns, the device comes up as an initial power on. All registers are cleared and the device has to be reconfigured. If an under-voltage event takes place on the V_{CC} pin, the device starts t_{UVSLP} timer to determine if this is a real event. If after the timer times out, the device enters fail-safe or sleep mode depending upon device set up. See Figure 8-24. The TCAN1576-Q1 also provides voltage over protection on the V_{CC} input. Once detected, the device enters fail-safe or sleep mode depending upon device set up. See Table 8-8 for the relationship between V_{SUP} and V_{CC}.

Table 8-8. UV_{SUP}, UV_{CC}

V_{SUP}	V_{CC}	DEVICE STATE	BUS	RXD
> UV_{SUP}	> UV_{CC}	Normal	Per TXD	Mirrors Bus
> UV_{SUP}	< UV_{CC}	Fail-safe or Sleep	High Impedance	High (Recessive)
< UV_{SUP}	NA	Power off	High Impedance	High Impedance

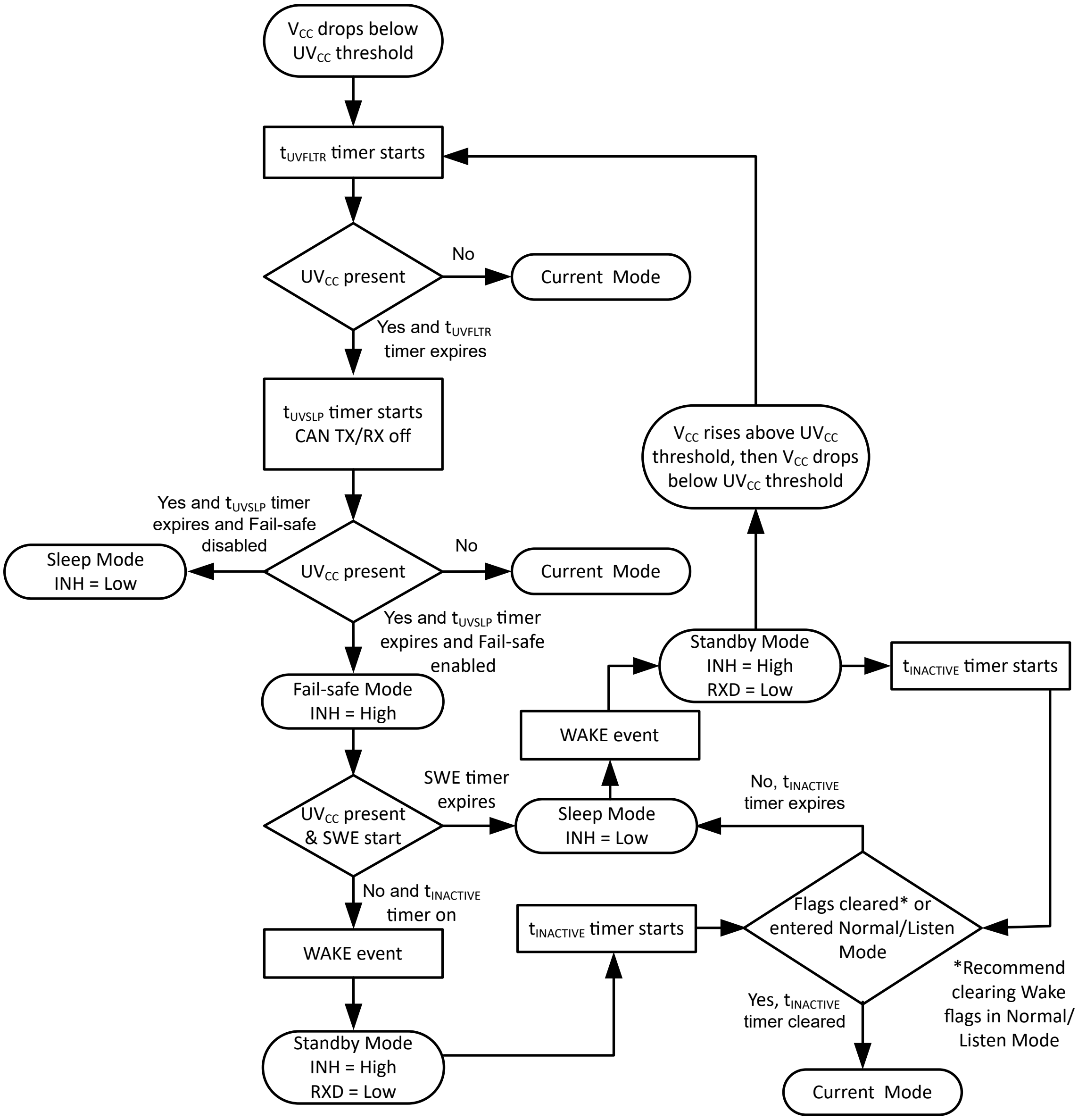

Figure 8-24. UV_{CC} State Diagram

Note

SWE timer and $t_{INACTIVE}$ branches are valid if 8'h1C[7] SWE_EN = 1b

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8.4.7.6.2 UV_{IO}

If V_{IO} drops below UV_{IO} under-voltage detection several functions are disabled. The transceiver switches off and disengages from the bus until V_{IO} has recovered. When UV_{IO} triggers, the t_{UV} timer starts. If the timer times out and the UV_{IO} is still there, the device enters sleep mode. See Figure 8-10, Figure 8-11. Once in sleep mode, a wake event is required to place the TCAN1576-Q1 into standby mode and enable the INH pin. As registers are cleared in sleep mode, the UV_{IO} interrupt flag is lost. If the UV_{IO} event is still in place, the cycle repeats. If during a thermal shut down event a UV_{IO} event happens, the device automatically enters sleep mode. See Figure 8-25 on how UV_{IO} behaves.

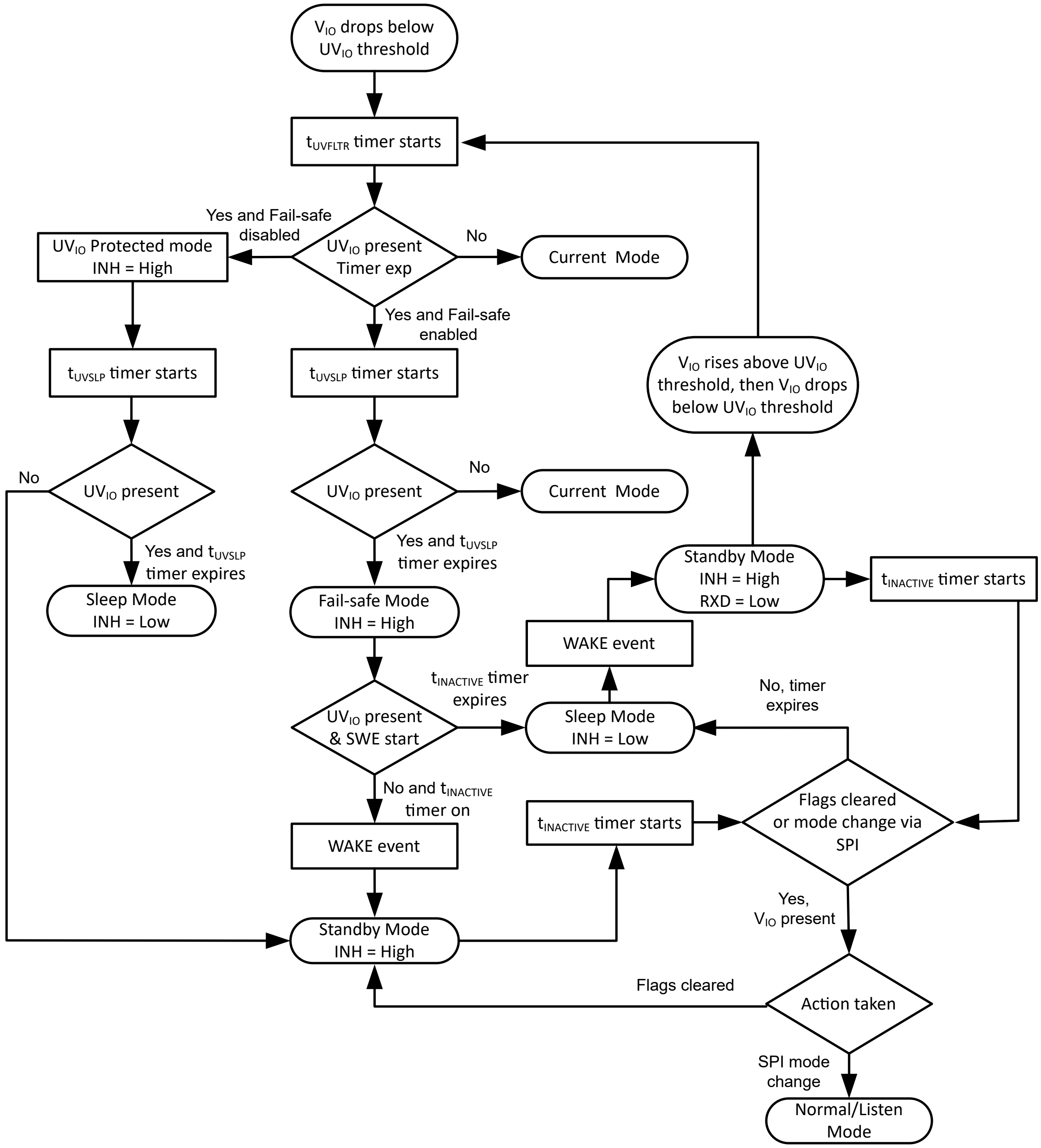


Figure 8-25. UV$_{IO}$ State Diagram

Note

SWE timer and $t_{INACTIVE}$ branches are valid if 8'h1C[7] SWE_EN = 1b

The device is designed to be *passive* or *no load* to the CAN bus if the device is unpowered. The bus terminals (CANH, CANL) have low leakage currents when the device is unpowered not loading the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational. Logic terminals also have low leakage currents when the device is unpowered, which avoids loading other circuits which can remain powered.

The UVLO circuit monitors both rising and falling edge of a power rail when ramping and declining.

8.4.7.6.2.1 Fault Behavior

During a UV_{IO}, UV_{CC} or TSD fault the TCAN1576-Q1 automatically does the following to keep the digital core in a known state.

Table 8-9. Under Voltage Lockout I and O Level Shifting Devices

V_{SUP}	V_{IO}	V_{CC}	DEVICE STATE	BUS	RXD
> UV_{SUP}	> UV_{IO}	> UV_{CC}	Normal	Per TXD	Mirrors Bus
> UV_{SUP}	> UV_{IO}	< UV_{CC}	Fail-safe or Sleep	High Impedance	High (Recessive)
< UV_{SUP}	> UV_{IO}	NA	Power Off	High Impedance	High (Recessive)
> UV_{SUP}	< UV_{IO}	> UV_{CC}	Fail-safe or UV_{IO} Protected → Sleep	High Impedance	High Impedance
> UV_{SUP}	< UV_{IO}	< UV_{CC}	Fail-safe or Sleep	High Impedance	High Impedance
< UV_{SUP}	< UV_{IO}	NA	Power Off	High Impedance	High Impedance

Note

Once an under-voltage condition and interrupt flags are cleared and the V_{SUP} supply has returned to valid level the device typically needs t_{MODE_x} to transition to normal operation. The host processor does not attempt to send or receive messages until this transition time has expired. If V_{SUP} has an under-voltage event, the device goes into a protected mode which disables the wake-up receiver and places the RXD output into a high impedance state.

8.4.7.7 Watchdog (TCAN1576-Q1)

The TCAN1576-Q1 has an integrated watchdog function that supports three watchdog types: a window watchdog, a timeout watchdog, and a question and answer (Q&A) watchdog. These are highly configurable using the SPI pins for programming. This function is default disabled. When enabled, the watchdog timer does not start until the first input trigger event to register 8'h15 when in normal and standby (when enabled) operational modes. The watchdog timer is off in sleep mode. When in sleep mode, the watchdog is disabled and requires the first watchdog trigger to start again once entering one of the allowed modes of operation. This is the same behavior when entering Fail-safe mode.

The INH pin is used as a node reset by turning off the node power and turning it back on after 300ms. There are two programmable configuration for this function. This feature is enabled by configuring the WD_ACT bits in the WD_CONFIG1 register 8'h13[1:0], see Figure 8-26. The INH pin is programmed as a LIMP function which provides a limp home capability when connected to external circuitry. Otherwise, the nINT reflects a watchdog failure and any specific programmed action. When in sleep mode, the LIMP pin is normally off, but if entered while on, the pin stays on. The LIMP pin turn off method is programmed by using DEVICE_CONFIG1 register 8'h1A[3:2], LIMP_SEL_RESET. When the error counter reaches the watchdog trigger event level, the LIMP pin turns on connecting V_{SUP} to the pin as described in the LIMP pin section. The watchdog flow chart Figure 8-27 provide the general flow for all three watchdog configurations and general behavior when LIMP pin is enabled instead of INH.

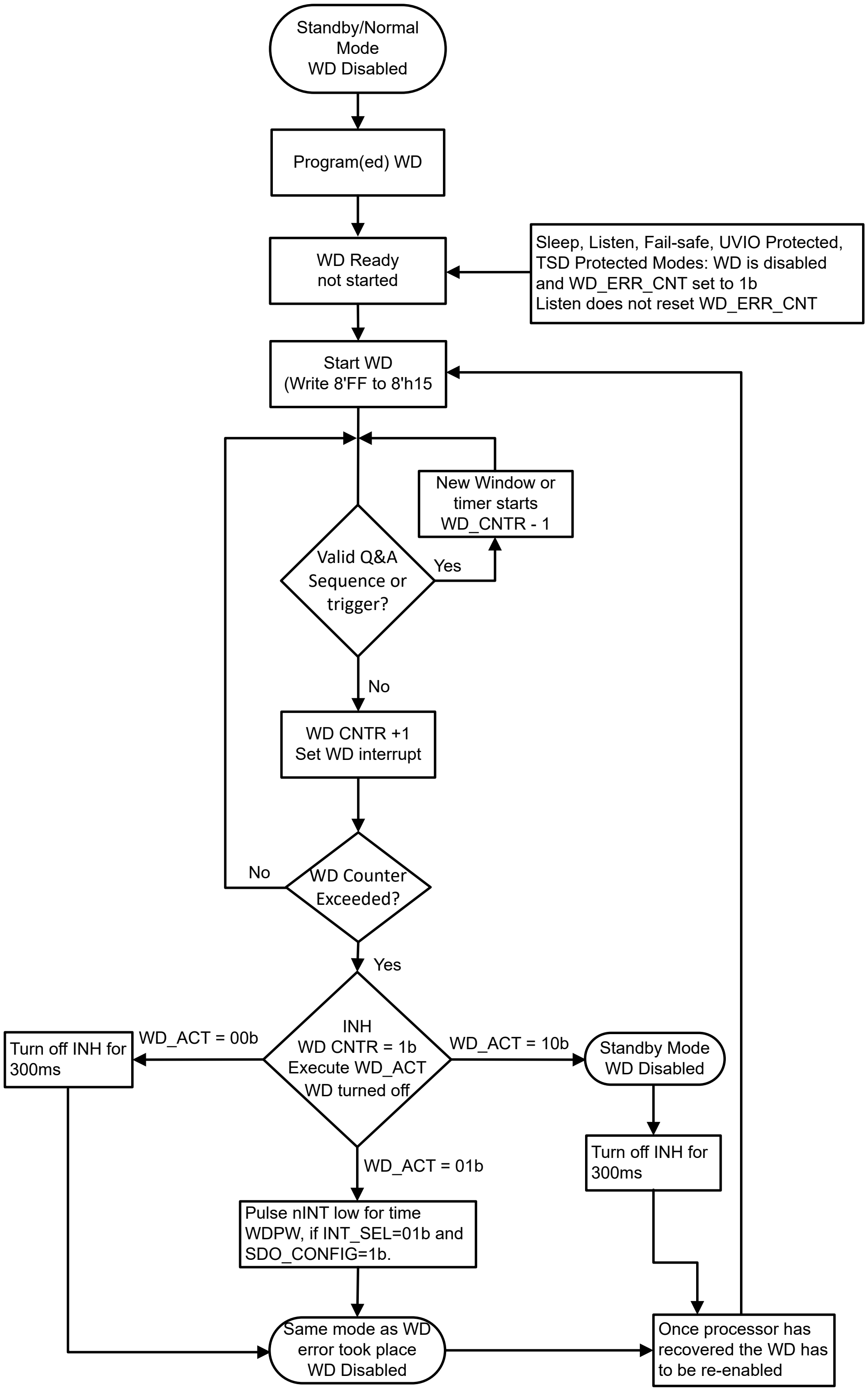


Figure 8-26. Watchdog Flow Chart INH Pin

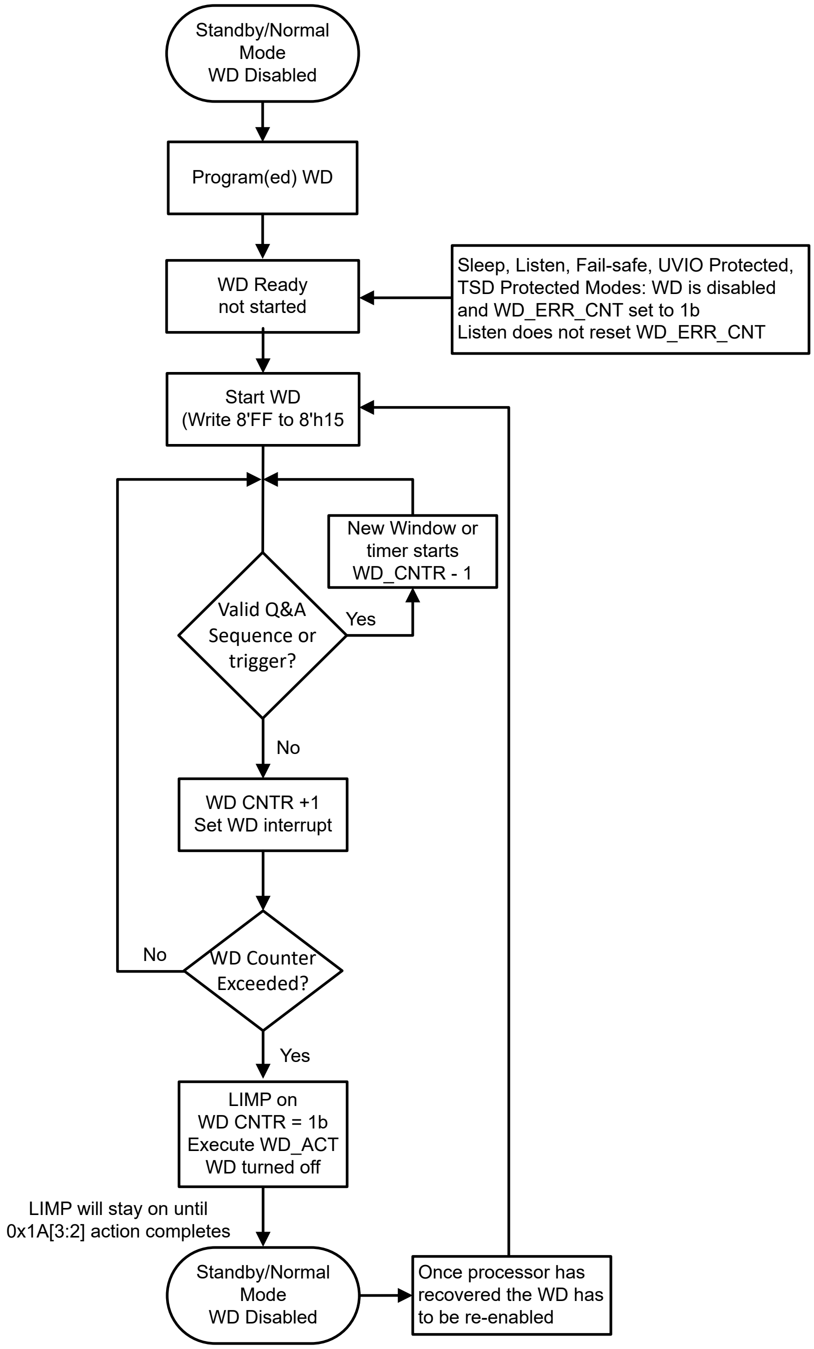


Figure 8-27. Watchdog Flow Chart LIMP Pin

8.4.7.7.1 Watchdog Error Counter

The TCAN1576-Q1 has a watchdog error counter. The counter is an up down counter that increments for every missed window or incorrect input watchdog trigger event. For every correct input trigger, the counter decrements, but does not drop below zero. The default trigger for this counter is set to trigger a watchdog error event. The counter changes to the fifth or ninth error. The error counter is read at register 8'h13[3:2].

8.4.7.7.2 Watchdog SPI Control Programming

The watchdog is configured and controlled using registers 8’h13 through 8’h15. These registers are provided in table Table 8-10. The TCAN1576-Q1 watchdog is set as a timeout, window or question and answer (Q&A) watchdog by setting 8’h13[7:6] to the method of choice. The time-out and window watchdog timer is based upon registers 8’h13[5:4] WD prescaler and 8’h14[7:5] WD timer and is in ms. See Table Table 8-10 for the achievable times. If using smaller time windows, the suggestion is to use the Timeout version of the watchdog. This is for times between 4ms and 64ms.

Table 8-10. Watchdog Window and Timeout Timer Configuration (ms)

WD_TIMER (ms)	8'h13[5:4] WD_PRE			
8'h14[7:5]	00	**01 (default)**	10	11
000 (default)	4	**8**	12	16
001	32	64	96	128
010	128	256	384	512
011	256	384	512	768
100	512	1024	1536	2048
101	2048	4096	6144	8192
110	10240	20240	RSVD	RSVD
1111	RSVD	RSVD	RSVD	RSVD

Note

If timing parameters are changed while the watchdog is running, the WD stops until after the first input trigger event after the new parameters have been programmed. At which time, WD runs based upon the new timing parameters.

8.4.7.7.2.1 Watchdog Configuration Registers Lock and Unlock

To avoid inadvertent watchdog configuration changes, the TCAN1576-Q1 implements a mechanism for locking and unlocking watchdog configuration registers. This impacts registers 8'h13, 8'h14, 8'h16 and 8'h2D. These registers can only be programmed in standby mode. The WD trigger write to 8'h15 automatically locks these registers. Once these registers are locked, an SPI write to them is treated as a WD failure. To unlock these registers, the device must transition into standby mode from normal or listen mode (see Figure 8-28). Unlocking is good for one write to each of the registers.

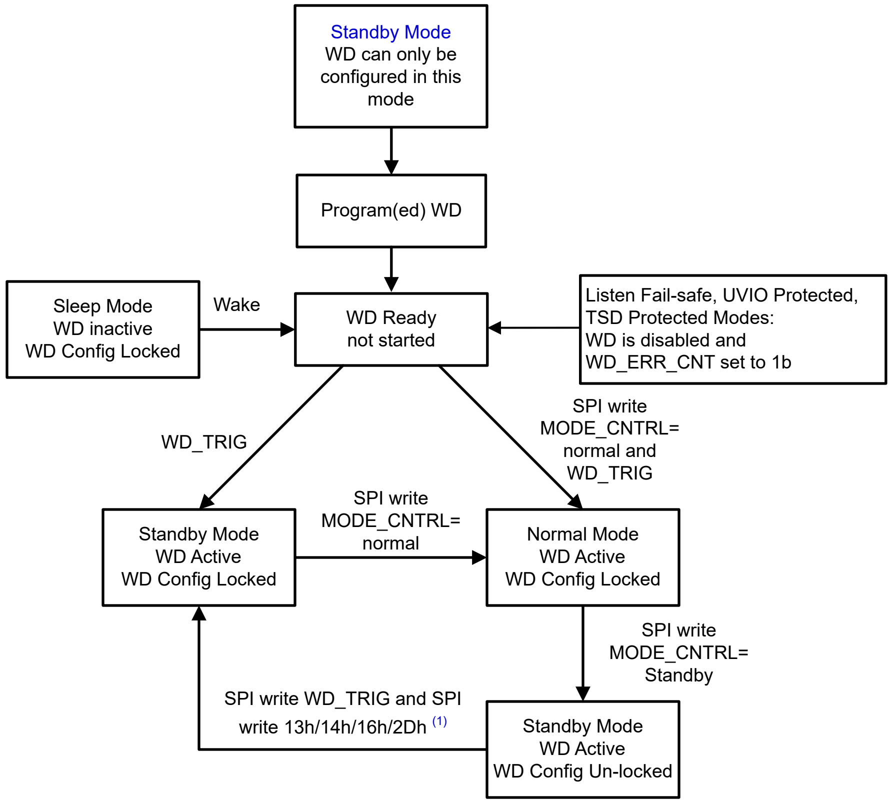


Figure 8-28. Watchdog Lock and Unlock Flow Chart

Note

(1) Registers 8'h13, 8'h14, 8'h16, and 8'h2D are allowed one write each after entering standby mode before being relocked.

8.4.7.7.3 Watchdog Timing

The TCAN1576-Q1 provides three methods for setting up the watchdog. If more frequent, < 64ms, input trigger events are desired the suggestion is to use the Timeout timer as this is an event within the time event and not specific to an open window.

When using the window watchdog, it is important to understand the closed and open window aspects. The TCAN1576-Q1 are set up with a 50%/50% open and closed window and is based on an internal oscillator with a ± 10% accuracy range. To determine when to provide the input trigger, this variance needs to be considered. Using the 60ms nominal total window provides a closed and open window that are each 30ms. Taking the ± 10% internal oscillator into account means the total window is 54ms, t_{WINDOW}, MIN or 66ms, t_{WINDOW} MAX. The closed and open window would then be 27ms, T_{WDOUT} MIN, or 33ms, T_{WDOUT} MIN. From the 54ms total window and 33ms closed window the total open window is 21ms. The trigger event needs to happen at the 43.5ms ± 10.5ms, safe trigger area. The same method is used for the other window values. Figure 8-29 provides the above information graphically. Once the WD trigger is written, the current Window is terminated and a new Closed Window is started.

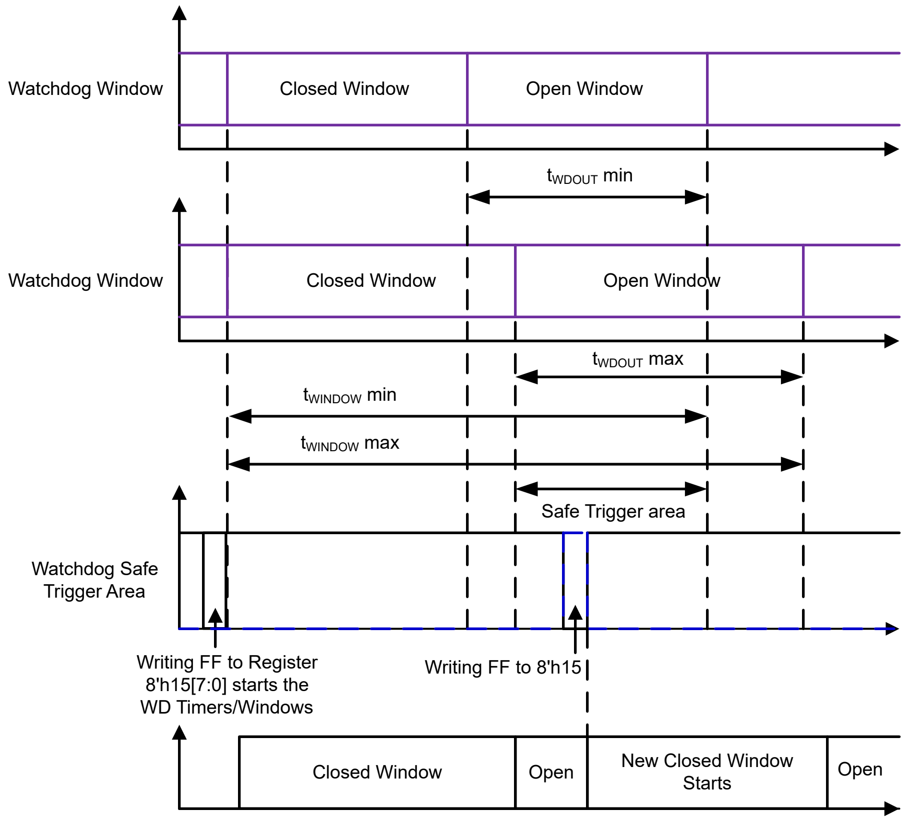


Figure 8-29. Window Watchdog Timing Diagram

8.4.7.7.4 Question and Answer Watchdog

The TCAN1576-Q1 includes a question and answer watchdog selectable from SPI. Device defaults to disabled.

Question and Answer WD Example explains the WD initialization events.

8.4.7.7.4.1 WD Question and Answer Basic Information

A Question and Answer (Q&A) watchdog is a type of watchdog where instead of simply resetting the watchdo through a SPI write, the MCU must read a ‘question’ from the TCAN1576-Q1, do math based on the question and then write the computed answers back to the TCAN1576-Q1. The correct answer is a 4-byte response. Each byte must be written in order and with the correct timing to have a correct answer.

There are two watchdog windows, referred to as WD Response Window #1 and WD Response Window #2 (Figure 8-31 WD Q&A Windows as example). The size of each window is 50% of the total watchdog window time, $t_{WD\_RESP\_WIN1}$ + $t_{WD\_RESP\_WIN2}$, which is selected from the WD_TIMER and WD_PRE register bits.

Each watchdog question and answer is a full watchdog cycle. The general process is that the MCU reads the question during WD Response Window #1. The CPU must perform a mathematical function on the question, resulting in 4 bytes of answers. 3 of the 4 answer bytes must be written to the answer register within the WD Response Window #1, in the correct order. The last answer must be written to the answer register after the first response window, inside of WD Response Window #2. If all 4 answer bytes were correct and in the correct order, then the response is considered good, the error counter is decremented and a new question is generated, starting the cycle over again. Once the fourth answer is written into WD Response Window #2, that window is terminated and a new WD Response Window #1 is started. The General Question & Answer timing diagram Figure 8-30 provides information on how the response windows may align. Response Window 1 is associated to Closed Window in the window WD timing diagram and Response Window 2 is associated to the Open Window with all the same rules and timing information.

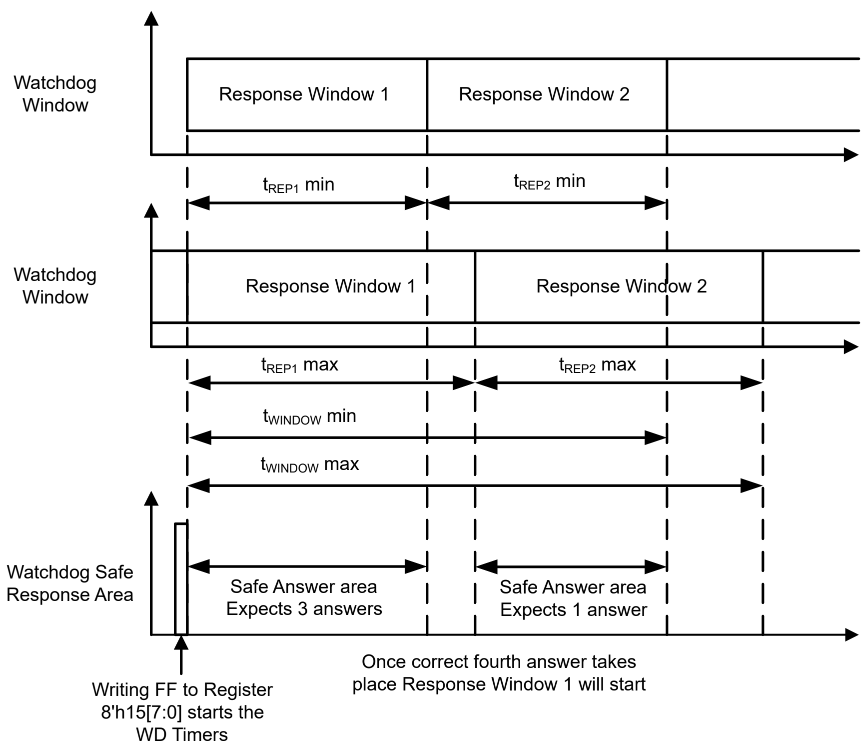
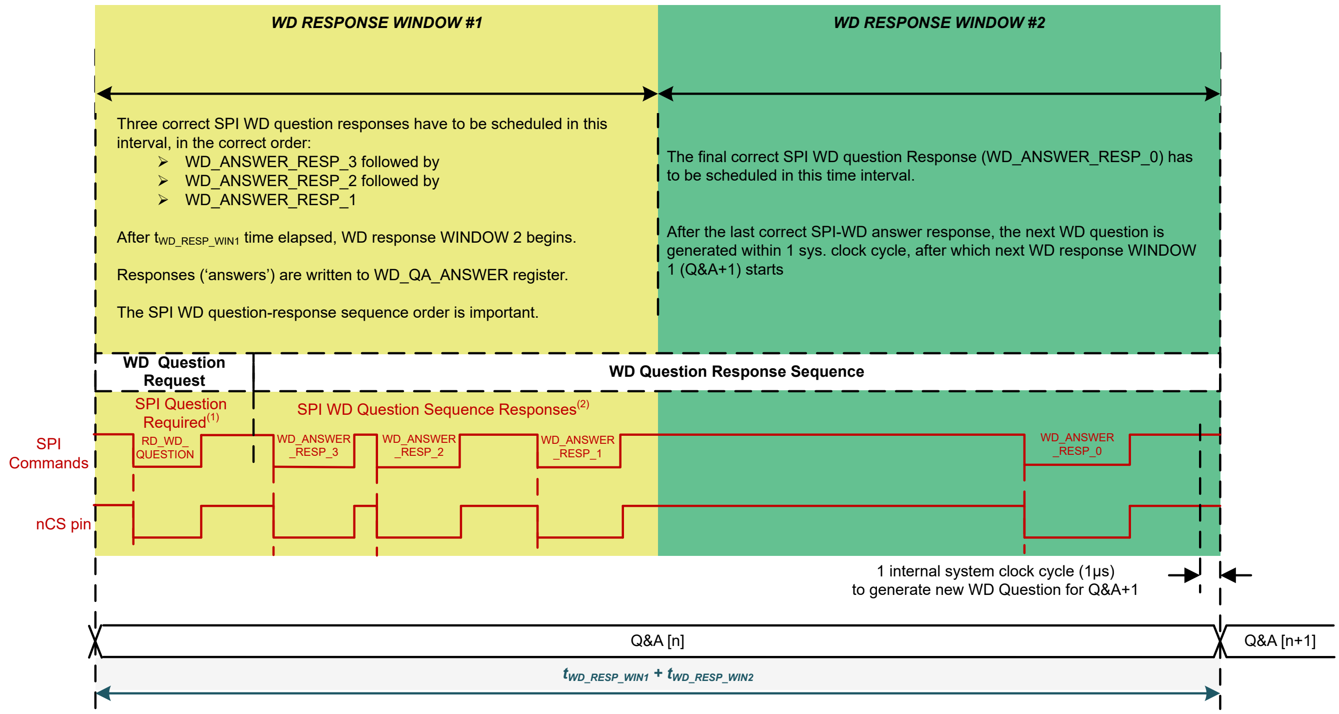


Figure 8-30. General Question & Answer Timing Diagram

If anything is incorrect or missed, the response is considered bad and the watchdog question does not change. In addition, an error counter is incremented. Once this error counter exceeds the threshold (defined in the

WD_ERR_CNT_SET register field), the watchdog failure action is performed. Examples of actions are an interrupt, or reset toggle, and so on.



A. The MCU is not required to request the WD question. The MCU can start with correct answers, WD_ANSWER_RESP_x bytes anywhere within RESPONSE WINDOW 1. The new WD question is always generated within one system clock cycle after the final WD_ANSWER_RESP_0 answer during the previous WD Q&A sequence run.

B. The MCU can schedule other SPI commands between the WD_ANSWER_RESP_x responses (even a command requesting the WD question) without any impact to the WD function as long as the WD_ANSWER_RESP_[3:1] bytes are provided within the RESPONSE WINDOW 1 and WD_ANSWER_RESP_0 is provided within the RESPONSE WINDOW 2.

Figure 8-31. WD Q&A Sequence Run

8.4.7.7.4.2 Question and Answer Register and Settings

There are several registers used to configure the watchdog registers, see Table 8-11.

Table 8-11. List of Watchdog Related Registers

Register Address	Register Name	Description
0x13	WD_CONFIG_1	Watchdog configuration and action in event of a failure
0x14	WD_CONFIG_2	Sets the time of the window, and shows current error counter value
0x15	WD_INPUT_TRIG	Register to reset or start the watchdog
0x16	WD_RST_PULSE	Sets error counter threshold
0x2D	WD_QA_CONFIG	Configuration related to the QA configuration
0x2E	WD_QA_ANSWER	Register for writing the calculated answers
0x2F	WD_QA_QUESTION	Reading the current QA question

The WD_CONFIG_1 and WD_CONFIG_2 registers mainly deal with setting up the watchdog window time length. Refer to *Timeout, Window, and Q&A Watchdog Timer Configuration (ms)* to see the options for window sizes and the required values for the WD_TIMER values and WD_PRE values. Take note that each of the 2 response windows are half of the selected value. Due to the need for several bytes of SPI to be used for each watchdog QA event, windows greater than 64ms are recommended when using the QA watchdog functionality.

There are also different actions that are performed when the watchdog error counter exceeds the error counter threshold.

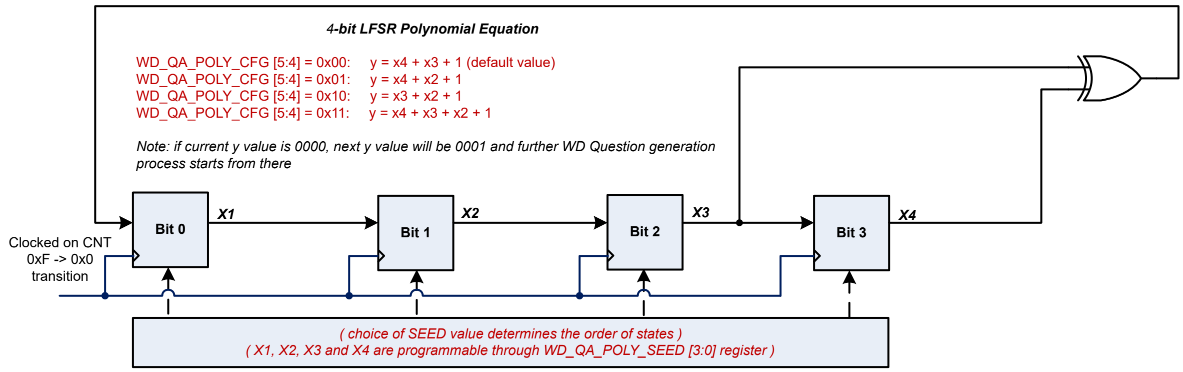
8.4.7.7.4.3 WD Question and Answer Value Generation

The 4-bit WD question, WD_QA_QUESTION[3:0], is generated by 4-bit Markov chain process. A Markov chain is a stochastic process with Markov property, which means that state changes are probabilistic, and the future state depends only on the current state. The valid and complete WD answer sequence for each WD Q&A mode is as follows:

- In WD Q&A multi-answer mode:
  1. Three correct SPI WD answers are received during RESPONSE WINDOW 1.
  2. One correct SPI WD answer is received during RESPONSE WINDOW 2.
  3. In addition to the previously listed timing, the sequence of four responses shall be correct.

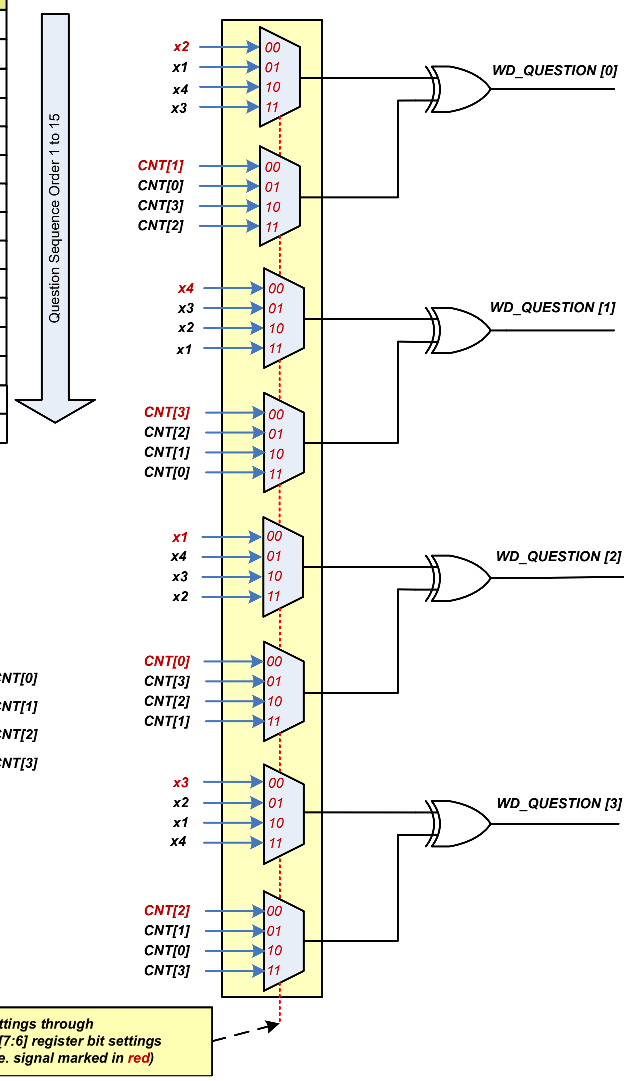
The WD question value is latched in the WD_QUESTION bits of the WD_QA_QUESTION register and is read out at any time.

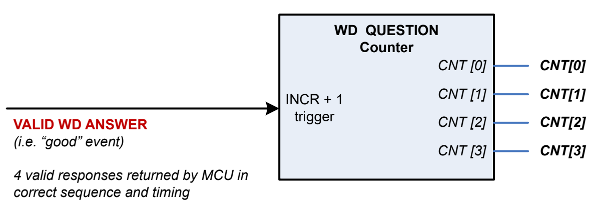
The Markov chain process is clocked by the 4-bit Question counter at the transition from 1111b to 0000b. This includes the condition of a correct answer (correct answer value and correct timing response). The logic combination of the 4-bit questions WD_QA_QUESTION [3:0] generation is given in Figure 8-32. The question counter is reset to default value of 0000b and the Markov chain is re-initialized to programmed register value when a watchdog fail puts the device into standby mode.



	X1	X2	X3	X4
Seed	1	0	1	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	1	0	0	0
8	0	1	0	0
9	0	0	1	0
10	1	0	0	1
11	1	1	0	0
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	1	0	1	0

Default QUESTION sequence order with default WD_QA_POLY_SEED and WD_QA_POLY_CFG values





A.
- Register 8'h2D[3:0] WD_QA_POLY_SEED maps as bit 3 = X1, bit 2 = X2. bit 1 = X3 and bit 0 = X4.
- If the current *y* value is 0000b, the next *y* value is 0001b. The next watchdog question generation process starts from that value. Any changes to WD_QA_CONFIG register in Standby mode will re-initialize the Markov chain to the current register value. The question counter is not affected.

Figure 8-32. Watchdog Question Generation

8.4.7.7.4.3.1 Answer Comparison

The 2-bit, watchdog-answer counter, WD_ANSW_CNT[1:0], counts the number of received answer-bytes and controls the generation of the reference answer-byte as shown in Figure 8-33. At the start of each watchdog sequence, the default value of the WD_ANSW_CNT[1:0] counter is 11b to indicate that the watchdog expects the MCU to write the correct Answer-3 in WD_QA_ANSWER[7:0].

The device sets the WD_QA_ERR status bit as soon as one answer byte is not correct. The device clears this status bit only if the MCU writes a ‘1b’ to this bit.

8.4.7.7.4.3.2 Sequence of the 2-bit Watchdog Answer Counter

The sequence of the 2-bit, watchdog answer counter is as follows for each counter value:

- WD_ANSW_CNT[1:0] = 11b:
  1. The watchdog calculates the reference Answer-3.
  2. A write access occurs. The MCU writes the Answer-3 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-3 with the Answer-3 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 10b and sets the WD_QA_ERR status bit to 1 if the Answer-3 byte was incorrect.
- WD_ANSW_CNT[1:0] = 10b:
  1. The watchdog calculates the reference Answer-2.
  2. A write access occurs. The MCU writes the Answer-2 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-2 with the Answer-2 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 01b and sets the WD_QA_ERR status bit to 1 if the Answer-2 byte was incorrect.
- WD_ANSW_CNT[1:0] = 01b:
  1. The watchdog calculates the reference Answer-1.
  2. A write access occurs. The MCU writes the Answer-1 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-1 with the Answer-1 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 00b and sets the WD_QA_ERR status bit to 1 if the Answer-1 byte was incorrect.
- WD_ANSW_CNT[1:0] = 00b:
  1. The watchdog calculates the reference Answer-0.
  2. A write access occurs. The MCU writes the Answer-0 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-0 with the Answer-0 byte in WD_QA_ANSWER[7:0].
  4. The watchdog sets the WD_QA_ERR status bit to 1 if the Answer-0 byte was incorrect.
  5. The watchdog starts a new watchdog sequence and sets the WD_ANSW_CNT[1:0] to 11b.

The MCU needs to clear the bit by writing a '1' to the WD_QA_ERR bit.,

Table 8-12. Set of WD Questions and Corresponding WD Answers Using Default Setting

QUESTION IN WD_QA_QUESTION REGISTER	WD ANSWER BYTES (EACH BYTE TO BE WRITTEN INTO WD_QA_ANSWER REGISTER)			
	WD_ANSWER_RESP_3	WD_ANSWER_RESP_2	WD_ANSWER_RESP_1	WD_ANSWER_RESP_0
WD_QUESTION	WD_ANSW_CNT[1:0] 11b	WD_ANSW_CNT[1:0] 10b	WD_ANSW_CNT[1:0] 01b	WD_ANSW_CNT[1:0] 00b
0x0	FF	0F	F0	00
0x1	B0	40	BF	4F
0x2	E9	19	E6	16
0x3	A6	56	A9	59
0x4	75	85	7A	8A
0x5	3A	CA	35	C5
0x6	63	93	6C	9C
0x7	2C	DC	23	D3
0x8	D2	22	DD	2D
0x9	9D	6D	92	62
0xA	C4	34	CB	3B
0xB	8B	7B	84	74
0xC	58	A8	57	A7
0xD	17	E7	18	E8
0xE	4E	BE	41	B1
0xF	01	F1	0E	FE

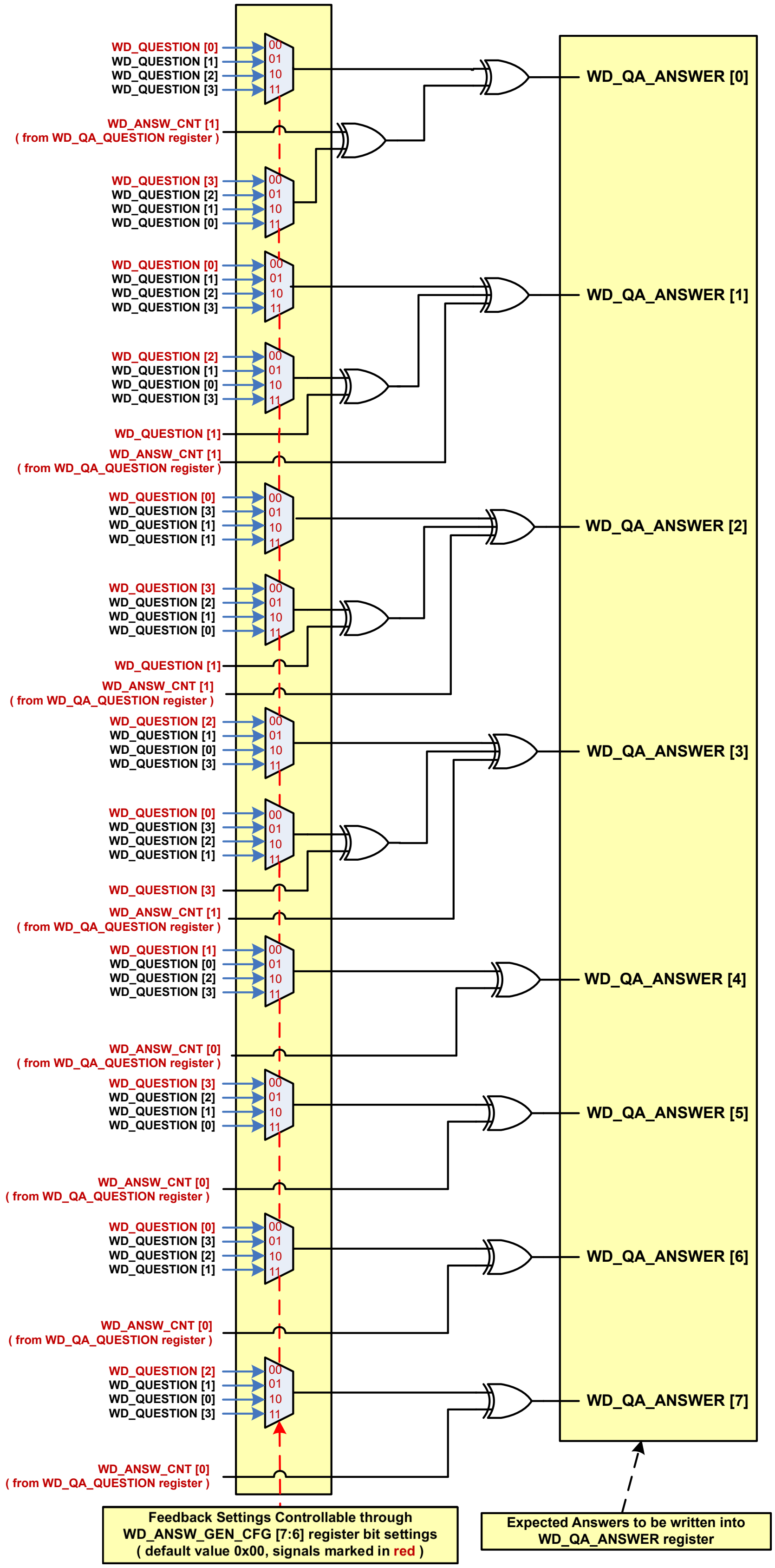


Figure 8-33. WD Expected Answer Generation

Table 8-13. Correct and Incorrect WD Q&A Sequence Run Scenarios

NUMBER OF WD ANSWERS		ACTION	WD_QA_ERR (in WD_QA_QUESTION Register)[1]	COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2			
0 answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	No answer
0 answer	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
0 answer	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
0 answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in RESPONSE WINDOW 1 and 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 CORRECT answer			
2 CORRECT answers	1 CORRECT answer			
0 answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in RESPONSE WINDOW 1 and 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 INCORRECT answer			
2 CORRECT answers	1 INCORRECT answer			
0 answer	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in WIN1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 CORRECT answers			
2 CORRECT answer	2 CORRECT answers			
0 answer	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 INCORRECT answers			
2 CORRECT answers	2 INCORRECT answers			
0 answer	3 CORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 CORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	
2 INCORRECT answers	1 CORRECT answer			
0 answer	3 INCORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 INCORRECT answers			
2 INCORRECT answers	1 INCORRECT answer			
0 answer	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 CORRECT answers		1b	
2 INCORRECT answers	2 CORRECT answers			
0 answer	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 INCORRECT answers			
2 INCORRECT answers	2 INCORRECT answers			
3 CORRECT answers	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question	1b	Less than 4 CORRECT ANSWERS in RESPONSE WINDOW 1 and more than 0 ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
2 CORRECT answers	0 answer		1b	
1 CORRECT answer	0 answer			
3 CORRECT answers	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Decrement WD failure counter -New WD cycle starts with a new WD question	0b	CORRECT SEQUENCE
3 CORRECT answers	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
3 INCORRECT answers	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received < 4
3 INCORRECT answers	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4

Table 8-13. Correct and Incorrect WD Q&A Sequence Run Scenarios (continued)

NUMBER OF WD ANSWERS		ACTION	WD_QA_ERR (in WD_QA_QUESTION Register)(1)	COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2			
3 INCORRECT answers	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
4 CORRECT answers	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	
3 CORRECT answers + 1 INCORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	4 CORRECT or INCORRECT ANSWERS in RESPONSE WINDOW 1
2 CORRECT answers + 2 INCORRECT answers	Not applicable			
1 CORRECT answer + 3 INCORRECT answers	Not applicable			

(1) WD_QA_ERR is the logical OR of all QA watchdog errors

8.4.7.7.4.4 Question and Answer WD Example

For this example, see the single sequence with the following configuration settings.

Table 8-14. WD Function Initialization

Item	Value	Description
Watchdog window size	1024ms	Window size of 1024ms
Answer Generation Option	0 (default)	Answer generation configuration
Question Polynomial	0 (default)	Polynomial used to generate the question
Question polynomial seed	A (default)	Polynomial seed used to generate questions
WD Error Counter Limit	15	On the 15th fail event, do the watchdog action

8.4.7.7.4.4.1 Example Configuration for Desired Behavior

Table 8-15 configures the part for the example behavior. Most of the settings are power on defaults.

Table 8-15. Example Register Configuration Writes

Step	Register	Data
1	WD_CONFIG_1 (0x13)	[W] 0b11011101 / 0xDD
2	WD_CONFIG_2 (0x14)	[W] 0b10000000 / 0x80
3	WD_RST_PULSE (0x16)	[W] 0b00000111 / 0x07
4	WDT_QA_CONFIG (0x2D)	[W] 0b00001010 / 0x0A

8.4.7.7.4.4.2 Example of Performing a Question and Answer Sequence

The normal sequence summary is as follows:

1. Read the question
2. Calculate the 4 answer bytes
3. Send 3 of them within the first response window
4. Wait and send the last byte in the second response window

See Table 8-16 for an example of the first loop sequence.

Table 8-16. Example First Loop

Step	Register	Data	Description
1	WD_INPUT_TRIG (ox15)	[W] 0xFF	Start the watchdog, also keep a timer internally to flag when response window 1 ends and window 2 starts.
2	WD_QA_QUESTION (0x2F)	[R] 0x3C	Read the question. Question is 0x3C
3	WD_QA_ANSWER (0x2E)	[W] 0x58	Write answer 3 (See Table 8-12 Example answers to questions with default settings to see answers)
4	WD_QA_ANSWER (0x2E)	[W] 0xA8	Write answer 2
5	WD_QA_ANSWER (0x2E)	[W] 0x57	Write answer 1
6	WD_QA_ANSWER (0x2E)	[W] 0xA7	Write answer 0 once window 2 has started

At this point, the user can read the WD_QA_QUSTION[6] (0x2F) register to determine if WD_QA_ERR is set.

8.4.8 Bus Fault Detection and Communication (TCAN1576-Q1)

The TCAN1576-Q1 provide advanced bus fault detection. The device can determine certain fault conditions and set a status/interrupt flag so the MCU can understand what the fault is. Detection takes place and is recorded if the fault is present during four dominant to recessive transitions with each dominant bit being ≥ 2µs. As with any bus architecture where termination resistors are at each end not every fault is specified to the lowest level, meaning exact location. The fault detection circuitry is monitoring the CANH and CANL pins (currents) to determine if there is a short to battery, short to ground, short to each other or opens. From a system perspective, the location of the device can impact what fault is detected. See Figure 8-34 as an example of node locations and how the nodes can impact the ability to determine the actual fault location. Figure 8-35 through Figure 8-39 show the various bus faults based upon the three node configuration. Table 8-17 shows what is detected and by which device.

Bus fault detection is a system-level situation. If the fault is occurring at the ECU, then the general communication of the bus is compromised. For complete coverage of a node, a system level diagnostic step for each node and the ability to communicate this back to a central point is needed.

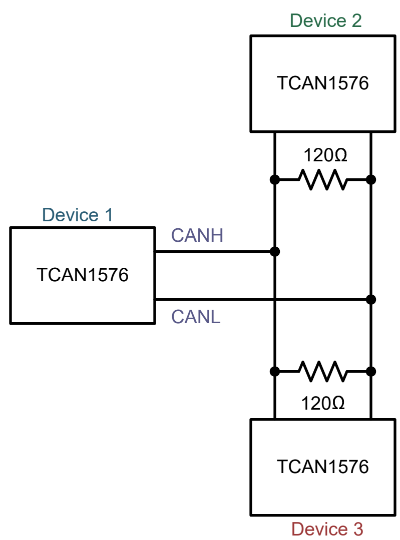


Figure 8-34. Three-Node Example

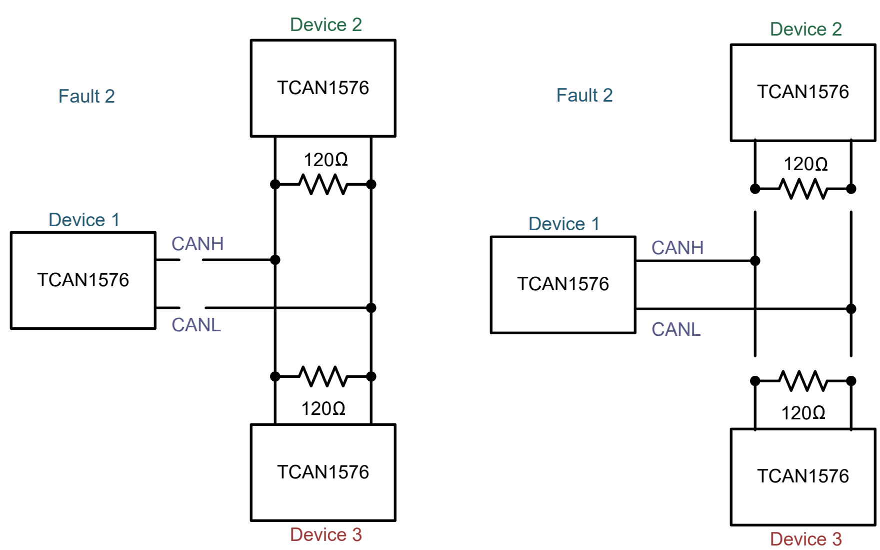


Figure 8-35. Open Fault 2 Examples

- Fault 2 is any case where no termination is seen

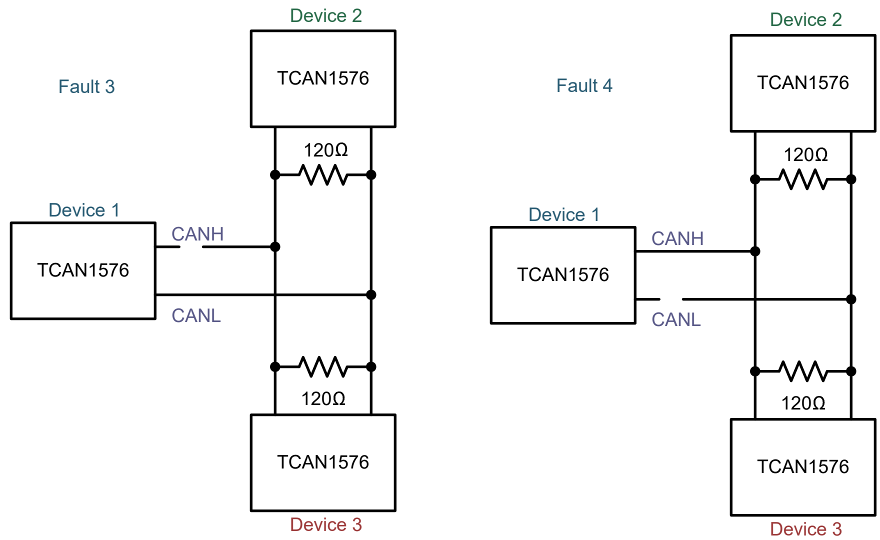


Figure 8-36. Open Fault 3 and 4 Examples

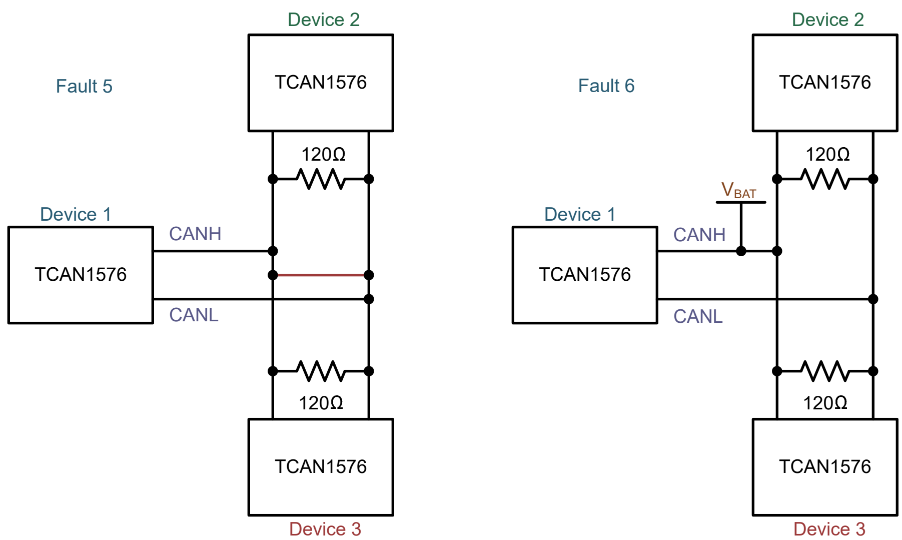


Figure 8-37. Fault 5 and 6 Examples

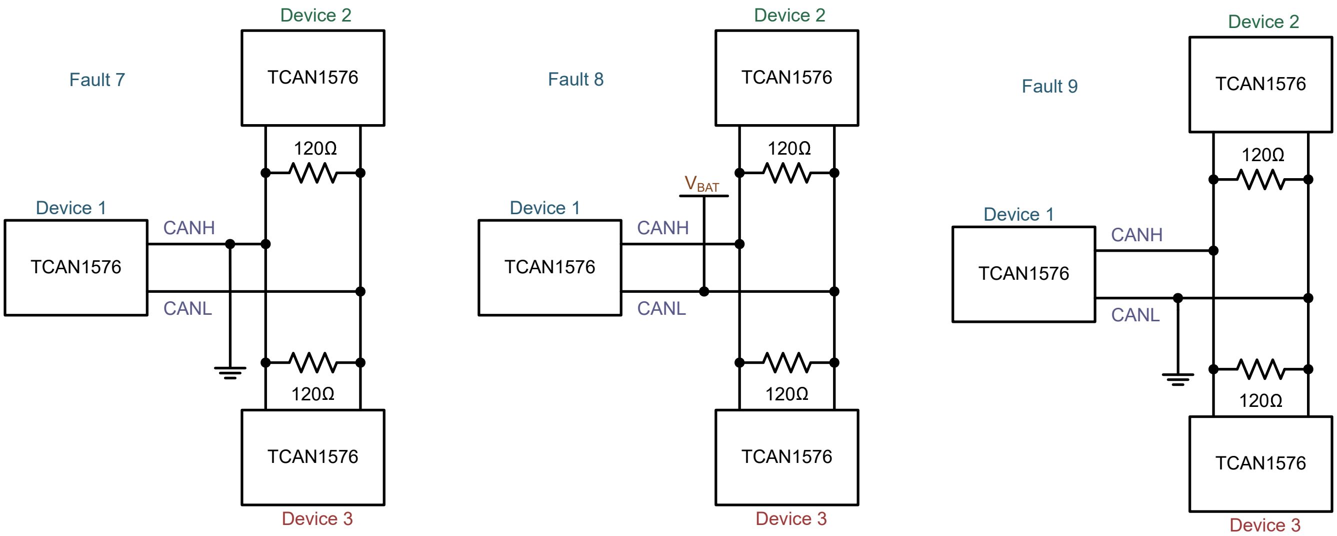


Figure 8-38. Fault 7, 8 and 9 Examples

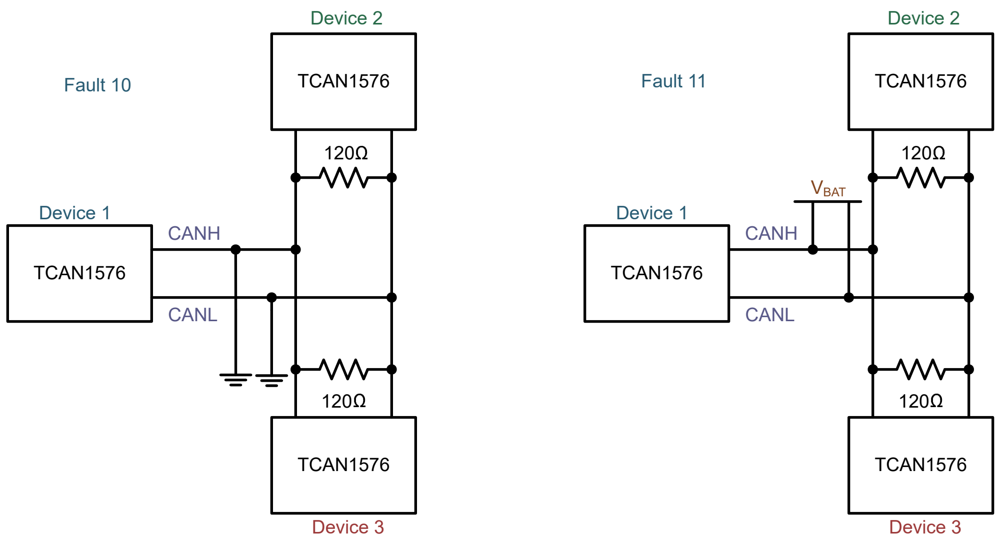


Figure 8-39. Fault 10 and 11 Examples

Table 8-17. Bus Fault Pin State and Detection Table

Fault #	CANH	CANL	Fault Detected
2	Open	Open	Depending upon open location the device detects this as no termination.
3	Open	Normal	Yes, but cannot tell the difference between Fault 3 and Faults 2 and 4; Device 2 and Device 3 does not see this fault
4	Normal	Open	Yes, but cannot tell the difference between Fault 4 and Faults 2 and 3; Device 2 and Device 3 does not see this fault
5	Shorted to CANL	Shorted to CANH	Yes, but not location
6	Shorted to V_{bat}	Normal	Yes, but not location
7	Shorted to GND	Normal	Yes, but cannot tell the difference between this and Fault 10
8	Normal	Shorted to V_{bat}	Yes, but cannot tell the difference between this and Fault 11
9	Normal	Shorted to GND	Yes, but not location
10	Shorted to GND	Shorted to GND	Yes, but cannot tell the difference between this and Fault 7
11	Shorted to V_{bat}	Shorted to V_{bat}	Yes, but cannot tell the difference between this and Fault 8

Table 8-18. Bus Fault Interrupt Flags Mapping to Fault Detection Number

Address	BIT(S)	DEFAULT	FLAG	DESCRIPTION	FAULT DETECTED	ACCESS
8'h54	7	1'b0	RSVD	Reserved		
	6	1'b0	RSVD	Reserved		
	5	1'b0	CANHCANL	CANH and CANL Shorted Together	Fault 5	R/WC
	4	1'b0	CANHBAT	CANH Shorted to V_{BAT}	Fault 6	R/WC
	3	1'b0	CANLGND	CANL Shorted to GND	Fault 9	R/WC
	2	1'b0	CANBUSOPEN	CAN Bus Open (One of three possible places)	Faults 2, 3 and 4	R/WC
	1	1'b0	CANBUSGND	CANH Shorted to GND or Both CANH & CANL Shorted to GND	Faults 7 and 10	R/WC
	0	1'b0	CANBUSBAT	CANL Shorted to V_{BAT} or Both CANH & CANL Shorted to V_{BAT}	Faults 8 and 11	R/WC

8.5 Programming

The TCAN1576-Q1 uses 7-bit addressing with a read/write bit followed by one to three bytes of data.

8.5.1 SPI Communication

The Serial Peripheral Interface (SPI) uses a standard configuration. Physically, the digital interface pins are nCS (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out) and SCK (Serial Clock). Each SPI transaction is a 16, 24 or 32 bits containing an address and read/write command bit followed by one to three data bytes. Supporting two and three data bytes is accomplished using burst read and write where the address is automatically incremented for the data along with the same number of clock cycles per bit. The data shifted out on the SDO pin for the transaction always starts with the Global Status Register (byte).

The SPI data input data on SDI is sampled on the low to high edge of the clock (SCK). The SPI output data on SDO is changed on the high to low edge of the clock (SCK).

When programming the device in sleep mode, care must be taken to understand what the output is. An example is the device is programmed with fail-safe mode off and one of the fault conditions that puts the device in sleep mode takes place, like an UV_{CC}. While in sleep mode, fail-safe mode is enabled. the device stays in sleep mode and does not switch to fail-safe mode.

8.5.1.1 Chip Select Not (nCS):

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the Serial Data Output (SDO) pin of the device is high impedance allowing an SPI bus to be designed. When nCS is low the SDO driver is activated and communication may be started. The nCS pin is held low for a SPI transaction. A special feature on this device allows the SDO pin to immediately show the Global Fault Flag on a falling edge of nCS.

8.5.1.2 SPI Clock Input (SCK):

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The SPI Data Input is sampled on the rising edge of SCK and the SPI Data Output is changed on the falling edge of the SCK. See Figure 8-40.

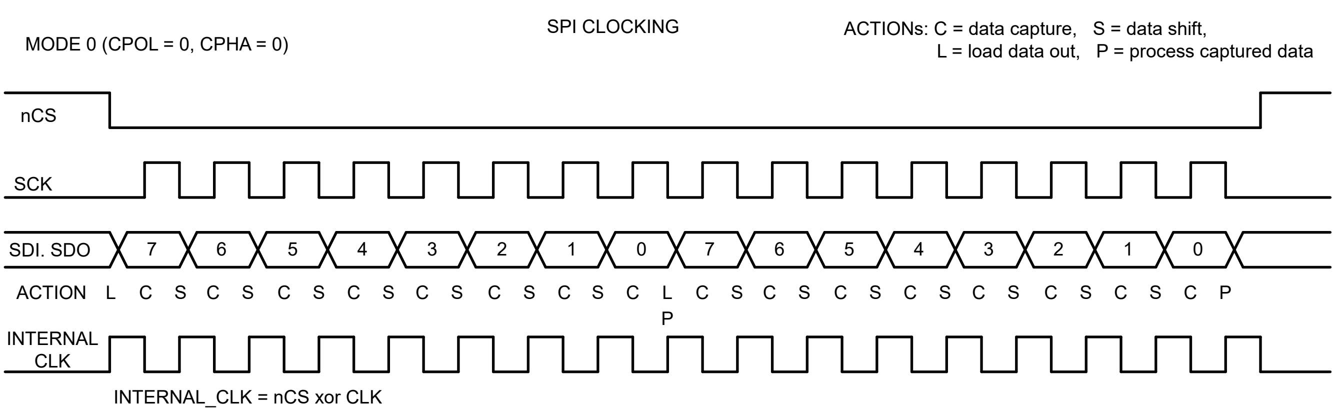


Figure 8-40. SPI Clocking

8.5.1.3 SPI Serial Data Input (SDI):

The SDI pin is used to let the device know which address is being read from or written to. During a write, the number of clock cycles determines how many data bytes up to three are loaded into sequential addresses. The minimum number of clock cycles for a write is 16 supporting the initial address and write command followed by one byte of data as seen in Figure 8-41. The TCAN1576-Q1 supports burst read and write. Figure 8-42 shows an example of a 32-bit write which includes the initial 7-bit address, write bit and three data bytes. This all requires 32 clock cycles. Once the SPI is enabled by a low on nCS, the SDI samples the input data on each rising edge of the SPI clock (SCK). The data is shifted into an appropriately-sized shift register and after the correct number of clock cycles the shift register is full and the SPI transaction is complete. For a write command code, the new data is written into the addressed register only after the exact number of clock cycles have been shifted in by SCK and the nCS has a rising edge to deselect the device. For a burst write if there are 31 clock cycles of SCK (1 clock cycle less than the full 3 byte write), the third byte write won't happen while the first two bytes write is executed. If the correct number of clock cycles and data are not shifted in during one SPI transaction (nCS low), the SPIERR flag is set.

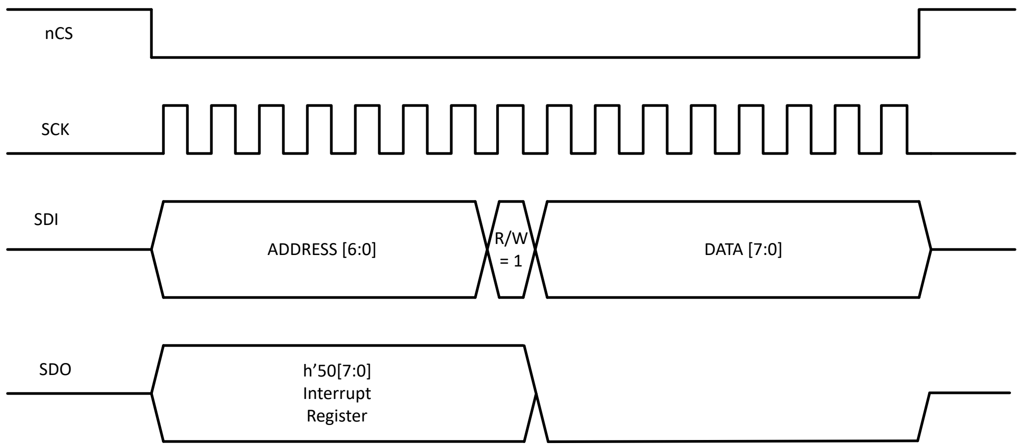


Figure 8-41. SPI Write

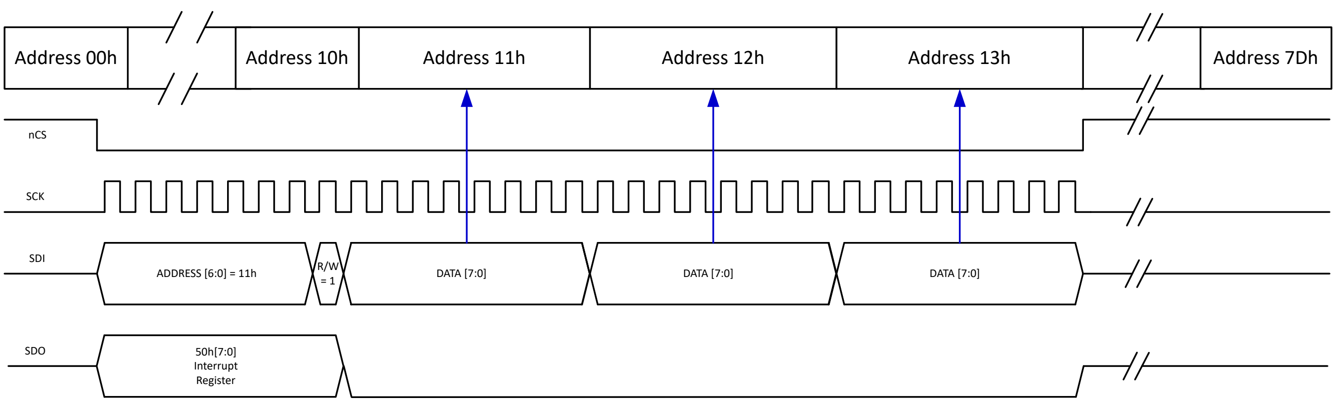


Figure 8-42. 32-bit SPI Burst Write

8.5.1.4 SPI Serial Data Output (SDO):

This pin is high impedance until the SPI output is enabled through nCS. Once the SPI is enabled by a low on nCS, the SDO is immediately driven high or low showing the global interrupt register 8'h50, bit 7. The Global Interrupt register, INT_GLOBAL, is the first byte to be shifted out. The SDO pin provides data out from the device to the processor. For a write command, this is the only data that is provided on the SDO pin. For a read command, the one to three bytes of data from successive address is provided on the SDO line. Figure 8-43 and Figure 8-44 shows examples of a single address read and of a three sequential address read using the 32-bit burst read. The 32-bit burst read shows the global interrupt register followed by the three requested data bytes.

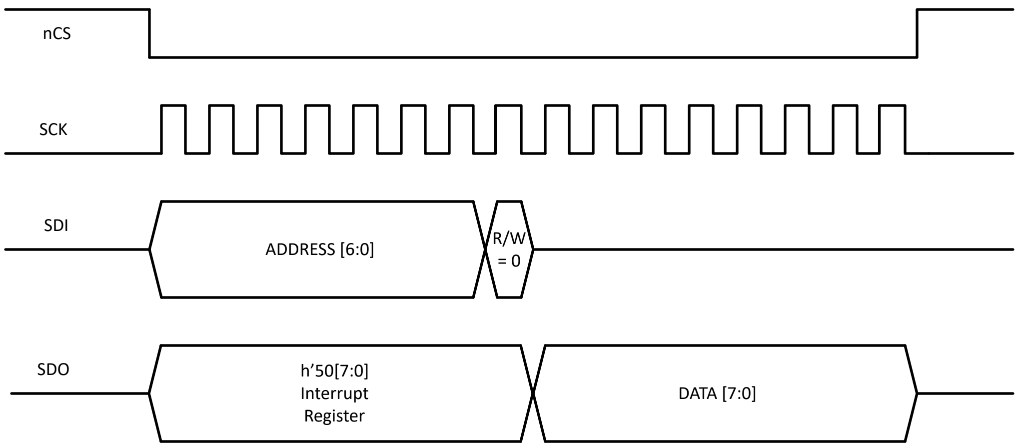


Figure 8-43. SPI Read

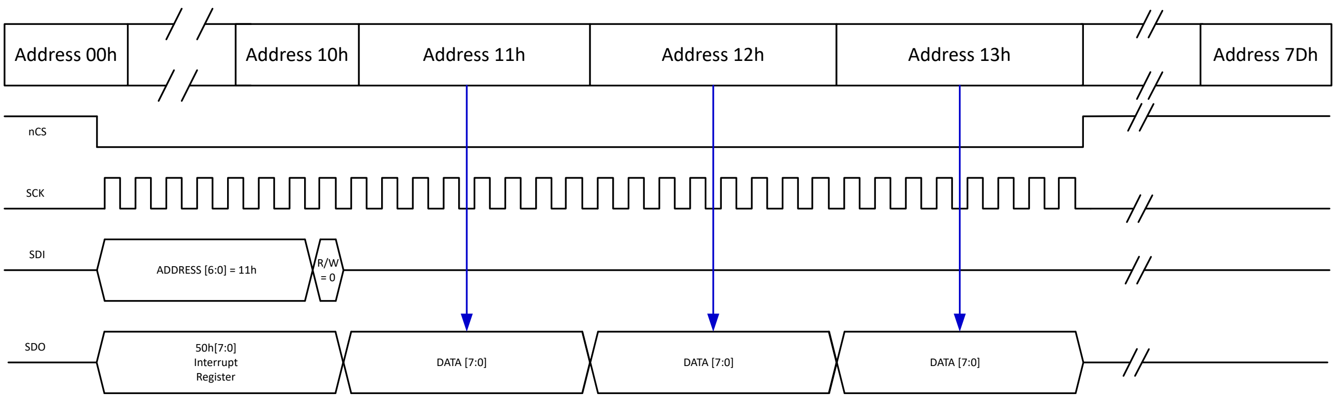


Figure 8-44. 32-bit SPI Burst Read

Note

If a read happens faster than 2μs after a write, the global fault flag status may not reflect any status change that the write may have initiated.

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9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Signal Improvement Capable (SIC)

The TCAN157x-Q1 family is a group of CAN SIC transceivers that are designed to meet the signal improvement capable requirements of the ISO 11898-2:2024 CAN standard to suppress bus ringing in large or complex CAN networks. Signal Improvement Capable (SIC) was started as a CIA standard and is included in the main section of the standard called set C and outlines SIC operation to be consistent with the design methodology used in existing CAN FD networks. Including continued use of 60Ω as a nominal differential load (two 120Ω termination resistor in parallel) as well as the wake up pattern (WUP) consisting of a dominant-recessive-dominant pattern. This implementation of the CAN standard is designed to provide CAN networks with ringing suppression while having minimal impact on other design considerations of the network such as termination type, value, placement and operation such as use of the standard WUP.

ISO 11898-2:2024 CAN standard includes new CAN physical layer call CAN XL with SIC mode capability in Annex A. Annex A introduces a more stringent SIC transceiver that can work with standard CAN and CAN XL and is known as SIC mode. Annex A defines specifications primarily addressing the use of CAN XL. CAN XL also uses CAN SIC in the implementation, but defines tighter specifications to the SIC portion of the driver than standalone CAN SIC transceivers. This includes specifying driver behavior across a 50Ω nominal load to accommodate the 100Ω characteristic impedance and termination values used in CAN XL system. The TCAN157x-Q1 is used in systems using CAN SIC node, this device also specifies behavior across the set C extended load range.

Annex A defines a revision to the standard CAN bus wake up pattern, WUP, to include a second filter period appearing as dominant-recessive-dominant-recessive-dominant. The TCAN157x-Q1 implements this new WUP but works in set C applications.

9.1.2 CAN Termination

The ISO 11898-2:2024 Annex A standard specifies the interconnection to be a single twisted pair cable (shielded or unshielded) with 100Ω characteristic impedance (ZO). The device also works in a traditional 120Ω environment that Set C of the standard covers.

9.1.2.1 Termination

Resistors equal to the characteristic impedance of the line are to be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus are to be kept as short as possible to minimize signal reflections. Termination must be carefully placed so that removal from the bus is not possible.

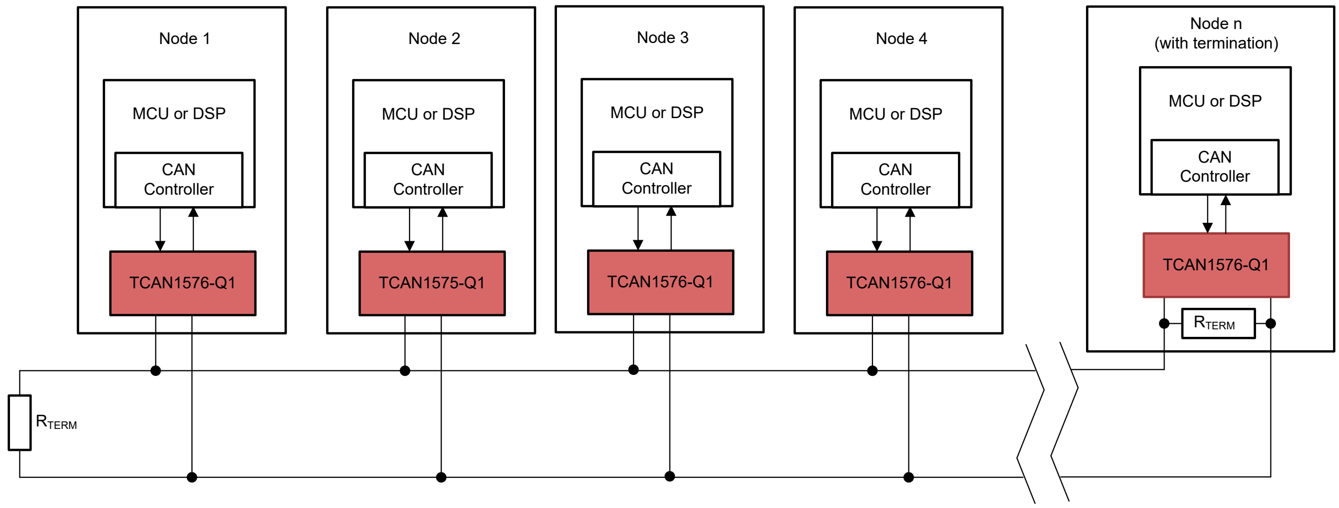


Figure 9-1. Typical CAN Bus

Termination is a single 100Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then "split termination" is used, see Figure 9-2. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltage levels at the start and end of message transmissions.

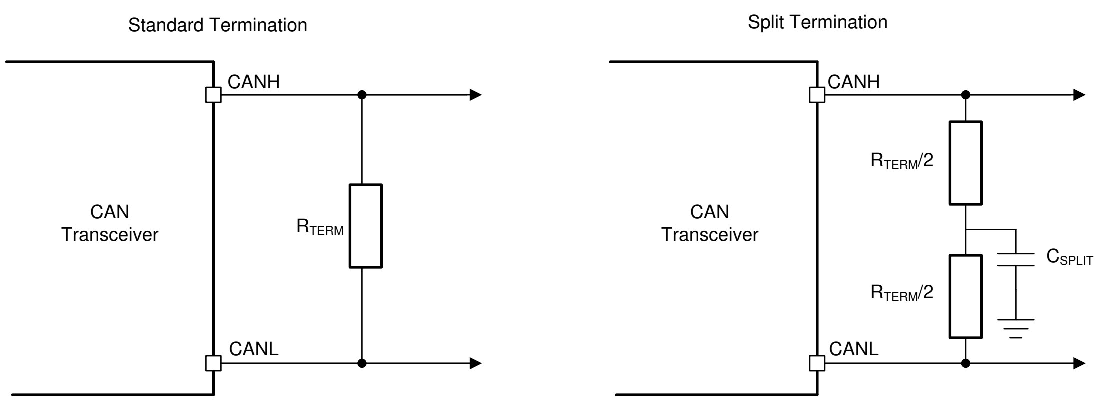


Figure 9-2. CAN Bus Termination Concepts

9.1.2.2 CAN Bus Biasing

Bus biasing is normal biasing, active in normal mode and inactive in low-power mode. Automatic voltage biasing is where the bus is active in normal mode but is controlled by the voltage between CANH and CANL in lower power modes. See Figure 9-3 for the state diagram on how the TCAN1576-Q1 performs automatic biasing.

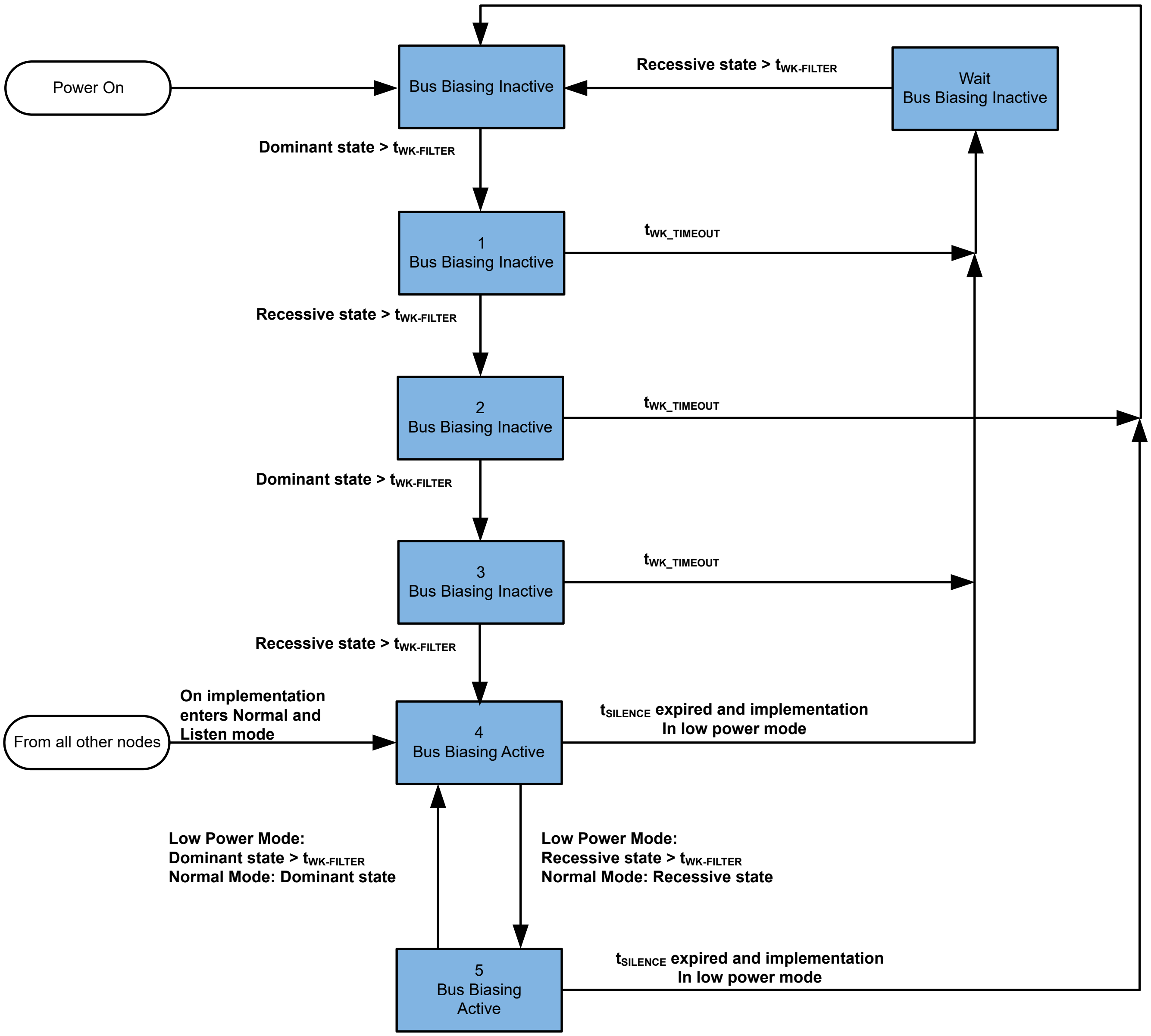


Figure 9-3. Automatic bus biasing state diagram

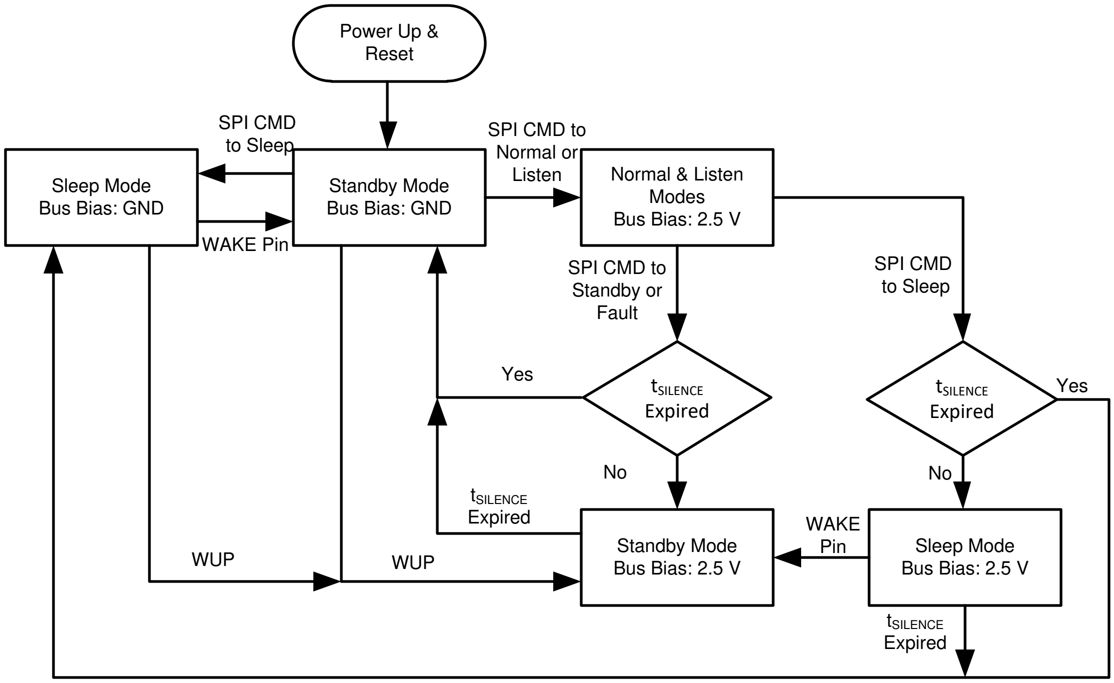


Figure 9-4. Bus biasing by Mode

Note

Fail-safe, TSD and VIO protected modes follow automatic bus biasing similar to Standby mode.

9.2 Typical Application

The TCAN1576-Q1 is typically used as the CAN FD transceiver in applications where the host microprocessor or FPGA supporting a CAN controller does not have an integrated CAN transceiver. Below is a typical application configuration for 3.3V microprocessor applications. The TCAN1576-Q1 works with 1.8V, 3.3V and 5V microprocessors when using the V_{IO} pin from the microprocessor voltage regulator. The bus termination is shown for illustrative purposes.

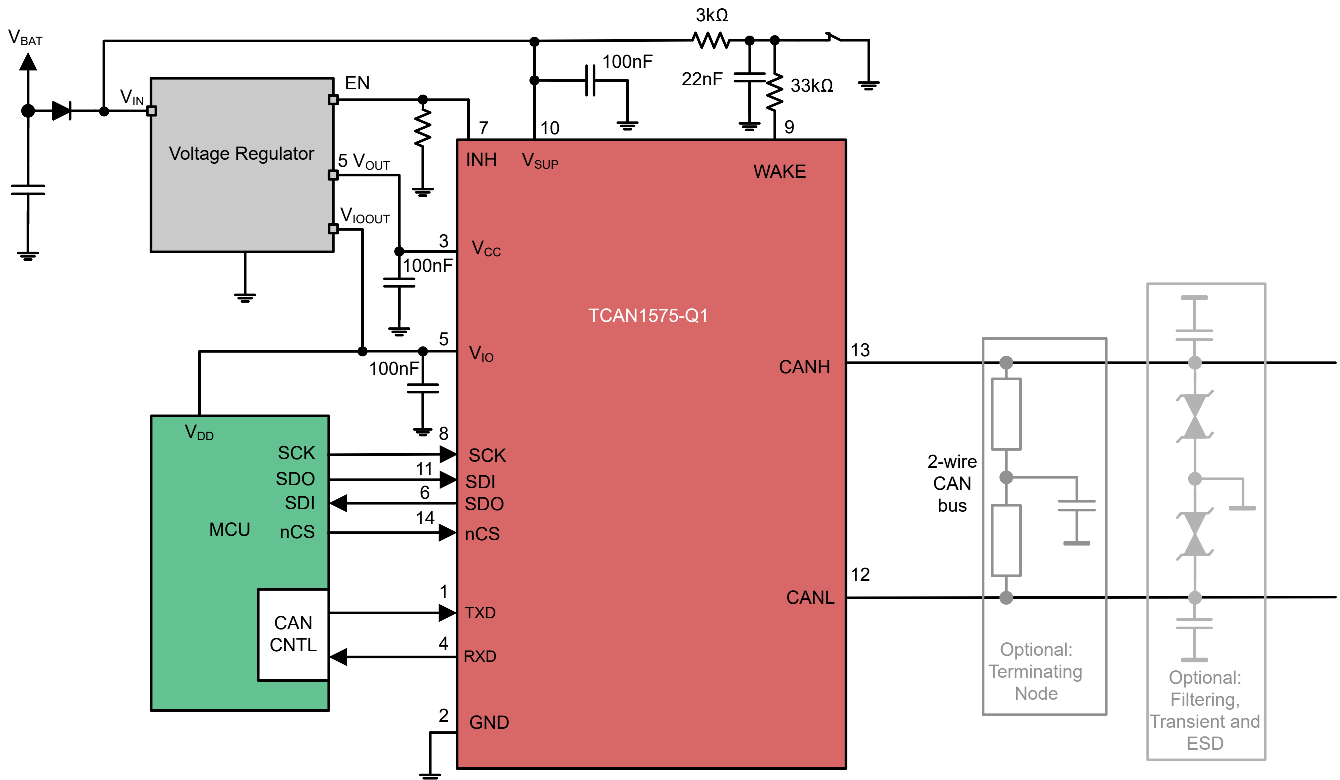


Figure 9-5. Typical CAN Application for TCAN1575-Q1

Note: Add decoupling capacitors as needed.

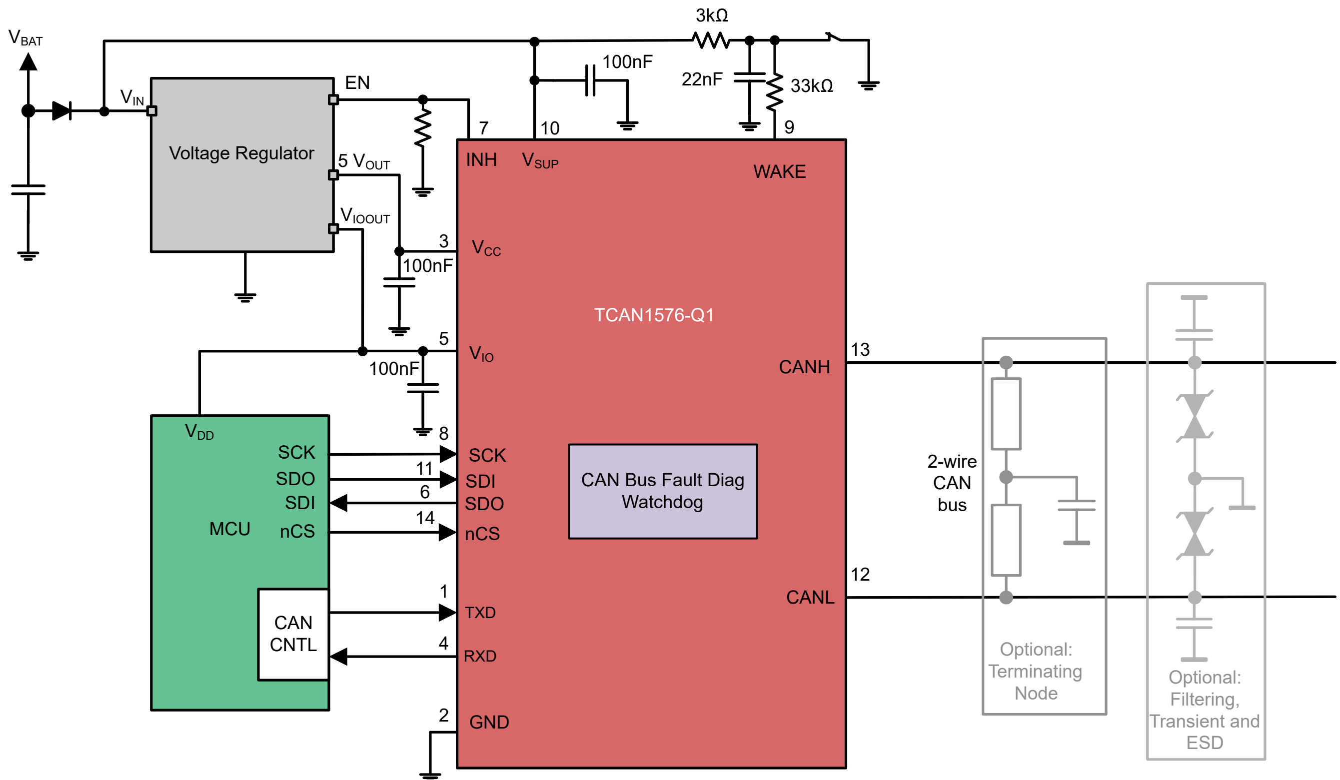


Figure 9-6. Typical CAN Application for TCAN1576-Q1

9.2.1 Design Requirements

The ISO 11898-2:2016 Standard specifies a maximum bus length of 40m and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the TCAN1576-Q1. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2:2016. There are system-level trade-offs for data rate, cable length, and parasitic loading of the bus. The TCAN1576-Q1 is specified to meet the 1.5V requirement with a 50Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the TCAN1576-Q1 is a minimum of 30kΩ. If 100 the TCAN1576-Q1 are in parallel on a bus, this is equivalent to a 300Ω differential load worst case. That transceiver load of 300Ω in parallel with the 60Ω gives an equivalent loading of 50Ω. Therefore, the TCAN1576-Q1 can supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO 11898-2:2016 standard of 40m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate. This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2:2016 CAN standard. In using this flexibility comes the responsibility of good network design and balancing these tradeoffs.

9.2.2 Detailed Design Procedure

The ISO 11898-2:2024 Annex A standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 100Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line is used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus are kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network. Termination may be a single 100Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

9.2.2.1 Brownout

Figure 9-7 shows the behavior of the INH pin during a brownout event. Brownout is when V_{SUP} is ≤ UV_{SUP} but > POR state. The RXD pin has an internal pull-up resister that is active during this event and will pull up the RXD pin output to the voltage level of V_{IO}.

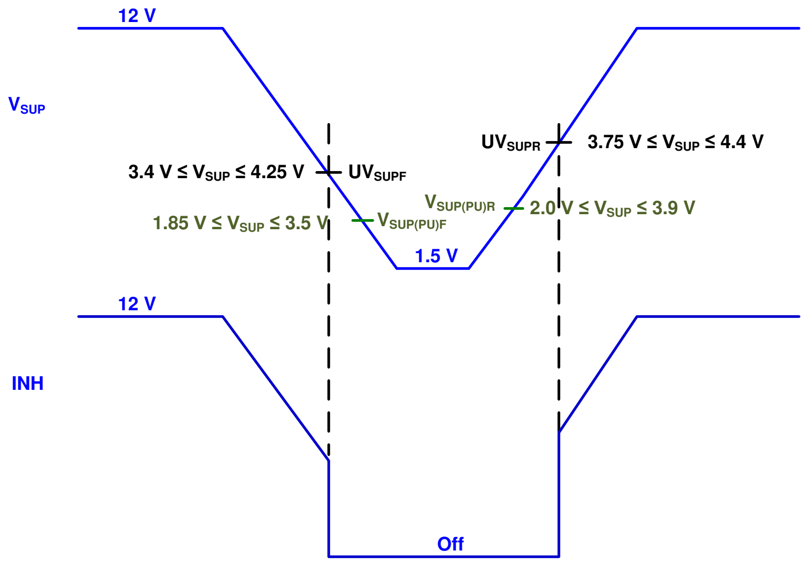
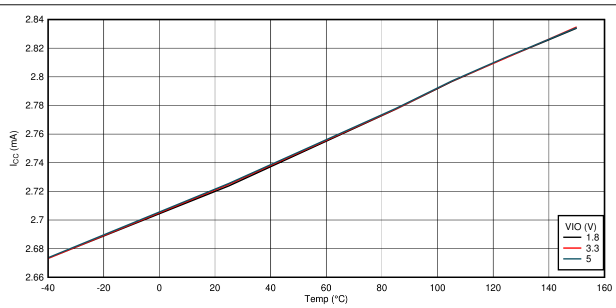


Figure 9-7. INH Behavior During Brownout

Note

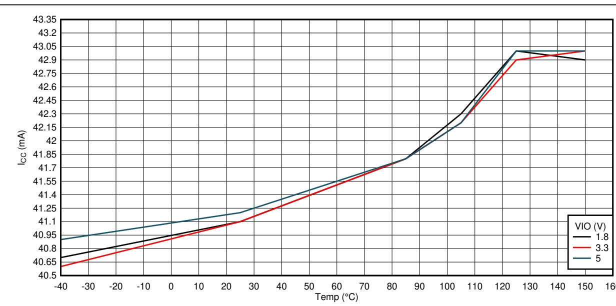
When the TCAN1576-Q1 has a UV_{SUP} event, the CAN bus is biased to ground.

9.2.3 Application Curves



V_{SUP} = 12V V_{CC} = 5V

Figure 9-8. Normal Mode: I_{CC} vs Temperature Recessive



V_{SUP} = 12V V_{CC} = 5V

Figure 9-9. Normal Mode: I_{CC} vs Temperature Dominant

9.3 Power Supply Recommendations

The TCAN1576-Q1 is designed to operate off of the battery Vbat and a 5V V_{CC} supporting the CAN transceiver and low voltage CAN receiver. To support a wide range of microprocessors, SPI is powered off of the V_{IO} pin which supports levels 1.8V, 3.3V and 5V. A bulk capacitance, typically 10µF, is placed near the V_{SUP} supply with a 100nF cap place near the V_{SUP} terminal. A bulk capacitance, typically 1µF, is placed near the CAN transceiver V_{IO} supply terminal in addition to bulk capacitors near the V_{IO} source.

9.4 Layout

Robust and reliable bus node design often requires the use of external transient protection device to protect against EFT and surge transients that occur in industrial environments. Because ESD and transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high-frequency layout techniques must be applied during PCB design. The family comes with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes are used. TVS diodes and bus filtering capacitors are placed as close to the on-board connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

9.4.1 Layout Guidelines

Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. The layout example provides information on components around the device. Transient voltage suppression (TVS) device is added for extra protection, shown as D1. The production solution is either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C10 and C11. A series common mode choke (CMC) is placed on the CANH and CANL lines between TCAN1576-Q1 and connector J1.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance.

Note

A high-frequency current follows the path of least impedance and not the path of least resistance.

Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

- Bypass and bulk capacitors are placed as close as possible to the supply terminals of transceiver, examples are C1 V_{CC} and C2 on V_{IO} , pins and C4 and C5 on the V_{SUP} supply.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R4 and R5, with the center or split tap of the termination connected to ground via capacitor C6. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to be sure the terminating node is not removed from the bus; thus, removing the termination.
- As terminal 6 (SDO/nINT) is an open drain, when working as nINT, an external resistor to V_{IO} is required. These can have a value between 2kΩ and 10kΩ.
- Terminal 7(INH) can have a 100kΩ resistor to ground if not used.
- Terminal 9 (WAKE) is a bi-directional wake up that is usually connected to an external switch. The terminal is configured as shown with C3 which is a 22nF capacitor to GND where R2 is 33kΩ and R3 is 3kΩ.
- Terminal 14 is the nCS pin.

9.4.2 Layout Example

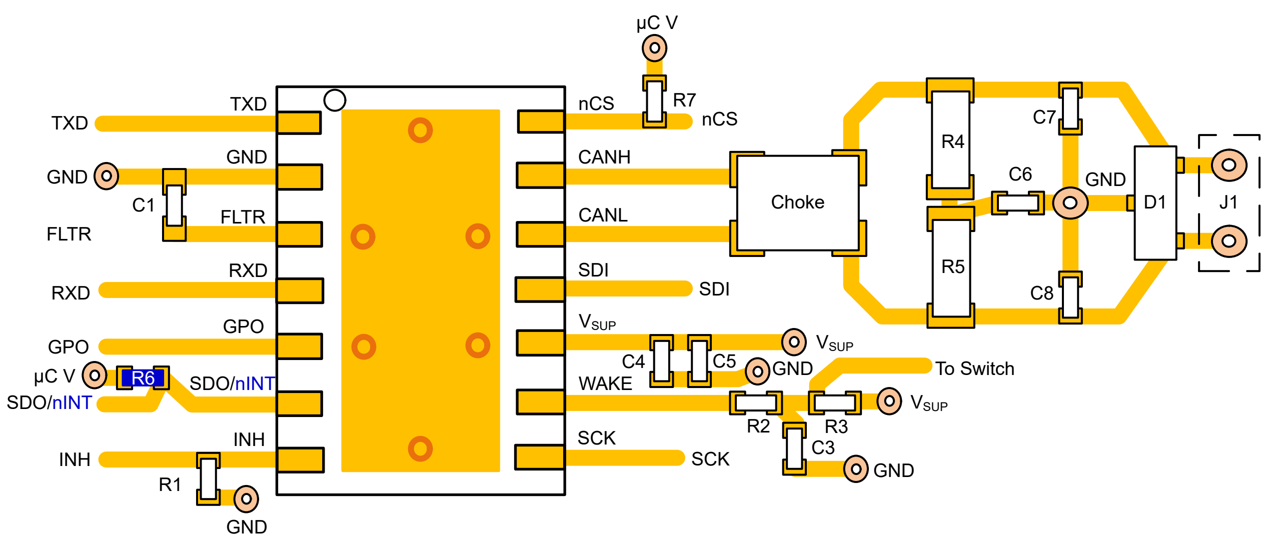


Figure 9-10. Example Layout

10 Registers

10.1 Register Maps

The TCAN1576-Q1 has a comprehensive register set with 7-bit addressing.

Table 10-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 10-1 is considered as reserved locations and the register contents are not be modified.

Table 10-1. Device Registers

Address	Acronym	Register Name	Section
0h + formula	DEVICE_ID_y	Device Part Number	Section 10.1.1
8h	REV_ID_MAJOR	Major Revision	Section 10.1.2
9h	REV_ID_MINOR	Minor Revision	Section 10.1.3
Ah + formula	SPI_RSVD_x	SPI reserved registers	Section 10.1.4
Fh	Scratch_Pad_SPI	Read and Write Test Register SPI	Section 10.1.5
10h	MODE_CNTRL	Mode configurations	Section 10.1.6
11h	WAKE_PIN_CONFIG	WAKE pin configuration	Section 10.1.7
12h	PIN_CONFIG	Pin configuration	Section 10.1.8
13h	WD_CONFIG_1(1)	Watchdog configuration 1	Section 10.1.9
14h	WD_CONFIG_2(1)	Watchdog configuration 2	Section 10.1.10
15h	WD_INPUT_TRIG(1)	Watchdog input trigger	Section 10.1.11
16h	WD_RST_PULSE(1)	Watchdog output pulse width	Section 10.1.12
17h	FSM_CONFIG	Fail safe mode configuration	Section 10.1.13
18h	FSM_CNTR	Fail safe mode counter	Section 10.1.14
19h	DEVICE_RST	Device reset	Section 10.1.15
1Ah	DEVICE_CONFIG1	Device configuration	Section 10.1.16
1Bh	DEVICE_CONFIG2	Device configuration	Section 10.1.17
1Ch	SWE_EN	Sleep wake error timer enable	Section 10.1.18
29h	SDO_CONFIG	Enables SDO to also support the nINT function	Section 10.1.19
2Dh	WD_QA_CONFIG (1)	Q and A Watchdog configuration	Section 10.1.20
2Eh	WD_QA_ANSWER(1)	Q and A Watchdog answer	Section 10.1.21
2Fh	WD_QA_QUESTION (1)	Q and A Watchdog question	Section 10.1.22
30h	SW_ID1	Selective wake ID 1	Section 10.1.23
31h	SW_ID2	Selective wake ID 2	Section 10.1.24
32h	SW_ID3	Selective wake ID 3	Section 10.1.25
33h	SW_ID4	Selective wake ID 4	Section 10.1.26
34h	SW_ID_MASK1	Selective wake ID mask 1	Section 10.1.27
35h	SW_ID_MASK2	Selective wake ID mask 2	Section 10.1.28
36h	SW_ID_MASK3	Selective wake ID mask 3	Section 10.1.29
37h	SW_ID_MASK4	Selective wake ID mask 4	Section 10.1.30
38h	SW_ID_MASK_DLC	ID Mask, DLC and Data mask enable	Section 10.1.31
39h + formula	DATA_y	CAN data byte 7 through 0	Section 10.1.32
41h + formula	SW_RSVD_y	SW_RSVD0 through SW_RSVD4	Section 10.1.33
44h	SW_CONFIG_1	CAN and CAN FD DR and behavior	Section 10.1.34
45h	SW_CONFIG_2	Frame counter	Section 10.1.35
46h	SW_CONFIG_3	Frame counter threshold	Section 10.1.36
47h	SW_CONFIG_4	Mode configuration	Section 10.1.37

Table 10-1. Device Registers (continued)

Address	Acronym	Register Name	Section
48h + formula	SW_CONFIG_RSVD_y	SW_CONFIG_RSVD_0 through SW_CONFIG_RSVD_2	Section 10.1.38
4Bh	DEVICE_CONFIGx	Device configuration	Section 10.1.39
50h	INT_GLOBAL	Global Interrupts	Section 10.1.40
51h	INT_1	Interrupts	Section 10.1.41
52h	INT_2	Interrupts	Section 10.1.42
53h	INT_3	Interrupts	Section 10.1.43
54h	INT_CANBUS(1)	CAN Bus fault interrupts	Section 10.1.44
55h	INT_GLOBAL_ENABLE	Interrupt enable for INT_GLOBAL	Section 10.1.45
56h	INT_ENABLE_1	Interrupt enable for INT_1	Section 10.1.46
57h	INT_ENABLE_2	Interrupt enable for INT_2	Section 10.1.47
58h	INT_ENABLE_3	Interrupt enable for INT_3	Section 10.1.48
59h	INT_ENABLE_CANBUS(1)	Interrupt enable for INT_CANBUS	Section 10.1.49
5Ah + formula	INT_RSVD_y	Interrupt Reserved Register INT_RSVD0 through INT_RSVD5	Section 10.1.50

(1) TCAN1576-Q1

Complex bit access types are encoded to fit into small table cells. Table 10-2 shows the codes that are used for access types in this section.

Table 10-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	H R	Set or cleared by hardware Read
Write Type		
H	H	Set or cleared by hardware
W	W	Write
W1C	1C W	1 to clear Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

10.1.1 DEVICE_ID_y Register (Address = 0h + formula) [reset = value]

DEVICE_ID_y is shown in Figure 10-1 and described in Table 10-3.

Return to Summary Table.

Device Part Number - reset value described in description field.

Offset = 0h + y; where y = 0h to 7h

Figure 10-1. DEVICE_ID_y Register

7	6	5	4	3	2	1	0
DEVICE_ID							
R-value							

Table 10-3. DEVICE_ID_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID	R	value	The DEVICE_ID[1:8] registers determine the part number of the device. The reset values and value of each DEVICE_ID register are listed for the corresponding register address Address 00h = 54h Address 01h = 43h Address 02h = 41h Address 03h = 4Eh Address 04h = 31h Address 05h = 34h Address 06h = 36h Address 07h = 35h for TCAN1575-Q1 Address 07h = 39h for TCAN1576-Q1

10.1.2 REV_ID_MAJOR Register (Address = 8h) [reset = 00h]

REV_ID_MAJOR is shown in Figure 10-2 and described in Table 10-4.

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Major Revision

Figure 10-2. REV_ID_MAJOR Register

7	6	5	4	3	2	1	0
Major_Revision							
R-00h							

Table 10-4. REV_ID_MAJOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Major_Revision	R	00h	Major die revision

10.1.3 REV_ID_MINOR Register (Address = 9h) [reset = 01h]

REV_ID_MINOR is shown in Figure 10-3 and described in Table 10-5.

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Minor Revision

Figure 10-3. REV_ID_MINOR Register

7	6	5	4	3	2	1	0
Minor_Revision							
R-01h							

Table 10-5. REV_ID_MINOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Minor_Revision	R	01h	Minor die revision

10.1.4 SPI_RSVD_x Register (Address = Ah + formula) [reset = 00h]

SPI_RSVD_x is shown in Figure 10-4 and described in Table 10-6.

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Configuration Reserved Bits Ah to Eh

Offset = Ah + x; where x = 0h to 4h

Figure 10-4. SPI_RSVD_x Register

7	6	5	4	3	2	1	0
SPI_RSVD_x							
R-00h							

Table 10-6. SPI_RSVD_x Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SPI_RSVD_x	R	0b	SPI reserved registers 0 - 4

10.1.5 Scratch_Pad_SPI Register (Address = Fh) [reset = 00h]

Scratch_Pad_SPI is shown in Figure 10-5 and described in Table 10-7.

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Read and Write Test Register SPI

Figure 10-5. Scratch_Pad_SPI Register

7	6	5	4	3	2	1	0
Scratch_Pad							
R/W-00h							

Table 10-7. Scratch_Pad_SPI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Scratch_Pad	R/W	00h	Read and Write Test Register SPI

10.1.6 MODE_CNTRL Register (Address = 10h) [reset = 04h]

MODE_CNTRL is shown in Figure 10-6 and described in Table 10-8.

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Mode select and feature enable and disable register

Figure 10-6. MODE_CNTRL Register

7	6	5	4	3	2	1	0
SW_EN	DTO_DIS	FD_EN	RSVD		MODE_SEL		
R/W-0b	R/W-0b	R/W-0b	R-00b		R/W-100b		

Table 10-8. MODE_CNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_EN	R/W	0b	Selective wake enable 0b = Disabled 1b = Enabled
6	DTO_DIS	R/W	0b	Disables dominant time out function 0b = Enabled 1b = Disabled

Table 10-8. MODE_CNTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FD_EN	R/W	0b	CAN bus fault detection enable for TCAN1576-Q1 otherwise reserved 0b = Disabled 1b = Enabled
4-3	RSVD	R	00b	Reserved
2-0	MODE_SEL	R/W	100b	Mode of operation select 001b = Sleep 100b = Standby 101b = Listen 111b = Normal **Note** NOTE: The current mode is read back and all other values are reserved

10.1.7 WAKE_PIN_CONFIG Register (Address = 11h) [reset = 4h]

WAKE_PIN_CONFIG is shown in Figure 10-7 and described in Table 10-9.

Return to Summary Table.

Register to configure the behavior of the WAKE pin.

Figure 10-7. WAKE_PIN_CONFIG Register

7	6	5	4	3	2	1	0
WAKE_CONFIG		WAKE_STAT		WAKE_WIDTH_INVALID		WAKE_WIDTH_MAX	
R/W-00b		R/W0C/H-00b		R/W-01b		R/W-00b	

Table 10-9. WAKE_PIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WAKE_CONFIG	R/W	00b	Wake pin configuration: Note: Pulse requires more programming 00b = Bi-directional - either edge 01b = Rising edge 10b = Falling edge 11b = Pulse
5-4	WAKE_STAT	R/W0C/H	00b	Status of the WAKE pin 00b = No change 01b = Rising edge 10b = Falling edge 11b = Pulse **Note** The status of the WAKE pin is displayed here after a state change. 00 must be written to these bits to clear the change. For Filtered WAKE Rising or falling edge is displayed depending upon selected method from register 12h[7]
3-2	WAKE_WIDTH_INVALID	R/W	01b	Pulses less than or equal to these pulses are considered invalid 00b = 5ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 10ms 01b = 10ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 20ms 10b = 20ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 40ms 11b = 40ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 80ms

Table 10-9. WAKE_PIN_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	WAKE_WIDTH_MAX	R/W	00b	Maximum WAKE pin input pulse width to be considered valid. 00b = 750ms 01b = 1000ms 10b = 1500ms 11b = 2000ms

10.1.8 PIN_CONFIG Register (Address = 12h) [reset = 00h]

PIN_CONFIG is shown in Figure 10-8 and described in Table 10-10.

Return to Summary Table.

Device configuration register

Figure 10-8. PIN_CONFIG Register

7	6	5	4	3	2	1	0
WAKE_PULSE_CONFIG	RSVD		nINT_SEL		RXD_WK_CONFIG	RSVD	
R/W-0b	R-00b		R/W-00b		R/W-0b	R-00b	

Table 10-10. PIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE_PULSE_CONFIG	R/W	0b	Set WAKE pin expected pulse/filtered direction 0b = Low –> High –> Low (Pulse), Low –> High (Filtered) 1b = High –> Low –> High (Pulse), High –> Low (Filtered)
6-5	RSVD	R	00b	Reserved
4-3	nINT_SEL	R/W	00b	nINT configuration selection: active low 00b = Global Interrupt 01b = Watchdog failure output 10b = Bus Fault Interrupt 11b = Wake Request
2	RXD_WK_CONFIG	R/W	0b	Configures RXD pin behavior from a wake event 0b = Pulled low 1b = Toggle
1-0	RSVD	R	00b	Reserved

10.1.9 WD_CONFIG_1 Register (Address = 13h) [reset = 15h]

WD_CONFIG_1 is shown in Figure 10-9 and described in Table 10-11.

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Watchdog configuration setup 1 for TCAN1576-Q1

Figure 10-9. WD_CONFIG_1 Register

7	6	5	4	3	2	1	0
WD_CONFIG		WD_PRE		WD_ERR_CNT_SET		WD_ACT	
R/W-00b		R/W-01b		R/W-01b		R/W-01b	

Table 10-11. WD_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CONFIG	R/W	00b	Watchdog configuration 00b = Disabled 01b = Timeout 10b = Window 11b = Q&A

Table 10-11. WD_CONFIG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	WD_PRE	R/W	01b	Watchdog prescaler 00b = Factor 1 01b = Factor 2 10b = Factor 3 11b = Factor 4
3-2	WD_ERR_CNT_SET	R/W	01b	Sets the watchdog event error counter that upon overflow the watchdog output triggers 00b = Immediate trigger on each WD event 01b = Triggers on the fifth error event 10b = Triggers on the ninth error event 11b = Triggers on the 15th error event
1-0	WD_ACT	R/W	01b	Watchdog output trigger event action 00b = Turns off INH for 300ms and sets WD interrupt 01b = Sets WD interrupt 10b = Turns off INH for 300ms and sets WD interrupt and transition to standby mode 11b = Reserved

Note

For WD_ACT, if 01b is selected and nINT_SEL = 01b (8'h12[4:3] and SDO_CONFIG = 1b (8'h29[0]), the nINT pin is be pulsed low for time WDPW, 8'h16[3:0].

10.1.10 WD_CONFIG_2 Register (Address = 14h) [reset = 02h]

WD_CONFIG_2 is shown in Figure 10-10 and described in Table 10-12.

Return to Summary Table.

Watchdog configuration setup 2 for TCAN1576-Q1

Figure 10-10. WD_CONFIG_2 Register

7	6	5	4	3	2	1	0
WD_TIMER			WD_ERR_CNT				RSVD
R/W-000b			RH-0001b				R-0b

Table 10-12. WD_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	WD_TIMER	R/W	000b	Sets window or timeout times based upon the WD_PRE setting See WD_TIMER table
4-1	WD_ERR_CNT	RH	0001b	Watchdog error counter Running count of errors up to 15 errors
0	RSVD	R	0b	Reserved

10.1.11 WD_INPUT_TRIG Register (Address = 15h) [reset = 00h]

WD_INPUT_TRIG is shown in Figure 10-11 and described in Table 10-13.

Return to Summary Table.

Writing FFh resets WD timer if accomplished at appropriate time for TCAN1576-Q1

Figure 10-11. WD_INPUT_TRIG Register

7	6	5	4	3	2	1	0
WD_INPUT							
W1C-00h							

Table 10-13. WD_INPUT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_INPUT	R/W1C	00h	Write FFh to trigger WD

10.1.12 WD_RST_PULSE Register (Address = 16h) [reset = 07h]

WD_RST_PULSE is shown in Figure 10-12 and described in Table 10-14.

Return to Summary Table.

Selects the pulse width of the WD trigger event if nINT is selected for this function for TCAN1576-Q1.

Figure 10-12. WD_RST_PULSE Register

7	6	5	4	3	2	1	0
RESERVED				WDPW			
R-0000b				R/W-0111b			

Table 10-14. WD_RST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved
3-0	WDPW	R/W	0111b	Window WD reset pulse width (ms) when selected 0001b = 3.6 - 5 0010b = 10 - 12.5 0100b = 40 - 50 0111b = 150 - 190 1000b = 1 - 1.5 1011b = 20 - 25 1101b = 60 - 75 1110b = 100 - 125

10.1.13 FSM_CONFIG Register (Address = 17h) [reset = 00h]

FSM_CONFIG is shown in Figure 10-13 and described in Table 10-15.

Return to Summary Table.

Configures the fail-safe mode.

Figure 10-13. FSM_CONFIG Register

7	6	5	4	3	2	1	0
FS_CNTR_EN	FS_CNTR_ACT			FS_STAT			FS_DIS
R/W-0b	R/W-000b			RH-000b			R/W-0b

Table 10-15. FSM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FS_CNTR_EN	R/W	0b	Enabled fails-afe mode counter 0b = Disabled 1b = Enabled
6-4	FS_CNTR_ACT	R/W	000b	Action if fails-afe counter exceeds programmed value 000b = No action 001b = Pull INH low for 1s 010b = Perform soft reset 011b = Perform hard reset - POR 100b = Stop responding to wake events and go to sleep until power cycle reset 101b = Reserved 110b = Reserved 111b = Reserved **Note** • When selecting 001b, if enabled, the SWE timer starts after the action has taken place. • When selecting 010b and 011b, the SWE timer must be re-enabled if used.

Table 10-15. FSM_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-1	FS_STAT	RH	000b	Reason for entering fail-safe mode 000b = Not in FS mode 001b = Thermal shut down event 010b = Reserved 011b = UV_{CC} All other combinations are reserved **Note** These values are held until cleared by writing 0h to FSM_CNTR_STAT
0	FS_DIS	R/W	0b	Fails-safe disable: Excludes power up fail safe 0b = Enabled 1b = Disabled

10.1.14 FSM_CNTR Register (Address = 18h) [reset = 00h]

FSM_CNTR is shown in Figure 10-14 and described in Table 10-16.

Return to Summary Table.

Set Fail-safe counter and status.

Figure 10-14. FSM_CNTR Register

7	6	5	4	3	2	1	0
FSM_CNTR_SET				FSM_CNTR_STAT			
R/W-0h				RH-0h			

Table 10-16. FSM_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_SET	R/W	0h	Sets the number of times FS mode enters before action taken. Value is one less than the number of times FS mode is entered. Range is 0-15, representing entering fail-safe mode 1-16 times
3-0	FSM_CNTR_STAT	RH	0h	Reads back the number of time FSM has been entered in a row up to 15. Cleared by writing 0h.

10.1.15 DEVICE_RST Register (Address = 19h) [reset = 00h]

DEVICE_RST is shown in Figure 10-15 and described in Table 10-17.

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Forces a soft or hard reset.

Figure 10-15. DEVICE_RST Register

7	6	5	4	3	2	1	0
RESERVED						SF_RST	HD_RST
R-000000b						R/W1C-0b	R/W1C-0b

Table 10-17. DEVICE_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	00000b	Reserved
1	SF_RST	R/W1C	0b	Soft Reset: Writing a 1b causes a soft reset. Device registers return to default values while keeping INH on.

Table 10-17. DEVICE_RST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HD_RST	R/W1C	0b	Hard Reset: Forces a power on reset when writing a 1b. **Note** NOTE: This will set the PWRON interrupt flag.

10.1.16 DEVICE_CONFIG1 Register (Address = 1Ah) [reset = 00h]

DEVICE_CONFIG1 is shown in Figure 10-16 and described in Table 10-18

Return to Summary Table.

Enables SPI to work in sleep mode if VIO is available.

LIMP pin only active for TCAN1576-Q1 otherwise reserved for TCAN1575-Q1.

Figure 10-16. DEVICE_CONFIG1 Register

7	6	5	4	3	2	1	0
RSVD	INH_DIS	INH_LIMP_SEL	LIMP_DIS	LIMP_SEL_RESET		LIMP_RESET	RSVD
R-0b	R/W-0b	R/W - 0b	R/W - 0b	R/W - 00b		R/W1C - 0b	R - 0b

Table 10-18. DEVICE_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6	INH_DIS	R/W	0b	INH pin disable 0b = Enabled 1b = Disabled
5	INH_LIMP_SEL	R/W	0b	Pin function select 0b = INH 1b = LIMP
4	LIMP_DIS	R/W	0b	LIMP pin disable if LIMP function selected 0b = Enabled 1b = Disabled
3-2	LIMP_SEL_RESET	R/W	00b	Selects the method to reset/turnoff the LIMP pin 00b = On third successful WD input trigger the error counter receives 01b = First correct WD input trigger 10b = WD input trigger not used 11b = Reserved
1	LIMP_RESET	R/W1C	0b	LIMP reset/turn off: Writing a one to this location resets the LIMP pin to off state and bit automatically clears
0	RSVD	R	0b	Reserved

10.1.17 DEVICE_CONFIG2 Register (Address = 1Bh) [reset = 0h]

DEVICE_CONFIG2 is shown in Figure 10-17 and described in Table 10-19.

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Disables the $t_{WK\_WIDTH\_MAX}$ from WAKE pin pulse configuration and makes the WAKE pin a filtered WAKE pin based off of $t_{WK\_WIDTH\_INVALID}$ and $t_{WK\_WIDTH\_MIN}$

Masks the CAN bus wake up (WUP) capability with CAN_WUP_DIS

Figure 10-17. DEVICE_CONFIG2 Register

7	6	5	4	3	2	1	0
RESERVED						WAKE_WIDTH_MAX_DIS	CAN_WUP_DIS

Figure 10-17. DEVICE_CONFIG2 Register (continued)

R-00000b	R/W-0b	R/W-0b

Table 10-19. DEVICE_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	00000b	Reserved
1	WAKE_WIDTH_MAX_DIS	R/W	0b	WAKE pulse maximum width disable. Disables $t_{WK\_WIDTH\_MAX}$ and puts the device into WAKE filtered configuration. 0b = Enabled 1b = Disabled
0	CAN_WUP_DIS	R/W	0b	Masks the CAN bus wake up (WUP) capability to avoid unwanted wake up due to glitches on the CAN bus. 0b = WUP enabled 1b = WUP disabled

10.1.18 SWE_EN Register (Address 1Ch) [reset = 04h]

SWE_EN is shown in Figure 10-18 and described in Table 10-20.

Return to Summary Table.

Enable the sleep wake error timer. Does not enable the timer for power on.

Figure 10-18. SWE_EN Register

7	6	5	4	3	2	1	0
SWE_EN	RESERVED				CANSLNT_SWE_DIS	RESERVED	
R/W-0b	R-0000b				R/W-1b	R-00b	

Table 10-20. SWE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWE_EN	R/W	0b	Sleep wake error enable: NOTE: This enables the SWE timer when coming out of sleep mode on a wake event. If this is enabled a SPI read or write must take place within the SWE timer window or the device goes back to sleep. 0b = Disabled 1b = Enabled
6-3	RSVD	R	0000b	Reserved
2	CANSLNT_SWE_DIS	R/W	1b	SWE timer is disabled from the CANSLNT flag and based only on $t_{Silence}$ 0b = Enabled 1b = Disabled
1-0	RSVD	R	00b	Reserved

10.1.19 SDO_CONFIG Register (Address = 29h) [reset = 00h]

SDO_CONFIG is shown in Figure 10-19 and described in Table 10-21.

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Configures SDO pin as SDO only or allows the pin to also behave like an interrupt pin, nINT.

Figure 10-19. SDO_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED							SDO_CONFIG
R-0000000b							R/W-0b

Table 10-21. SDO_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved

Table 10-21. SDO_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SDO_CONFIG	R/W	0b	SDO pin configuration: NOTE: When configured as SDO and nINT the pin behaves as SDO when nCS is low and behaves as nINT when nCS is high 0b = SDO only 1b = SDO and nINT

10.1.20 WD_QA_CONFIG Register (Address = 2Dh) [reset = 00h]

WD_QA_CONFIG is shown in Figure 10-20 and described in Table 10-22.

Return to Summary Table.

Q&A watchdog configuration bits for TCAN1576-Q1 only

Figure 10-20. WD_QA_CONFIG Register

7	6	5	4	3	2	1	0
WD_ANSW_GEN_CFG		WD_Q&A_POLY_CFG		WD_Q&A_POLY_SEED			
R/W-00b		R/W-00b		R/W-0000b			

Table 10-22. WD_QA_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_ANSW_GEN_CFG	R/W	00b	WD answer generation configuration
5-4	WD_Q&A_POLY_CFG	R/W	00b	WD Q&A polynomial configuration
3-0	WD_Q&A_POLY_SEED	R/W	0000b	WD Q&A polynomial seed value loaded when device is in the RESET state

Note

Upon power up, WD_Q&A_POLY_SEED will read back 0000b but the actual seed value is 1010b. Once written to the read back value and actual value is the same.

10.1.21 WD_QA_ANSWER Register (Address = 2Eh) [reset = 00h]

WD_QA_ANSWER is shown in Figure 10-21 and described in Table 10-23.

Return to Summary Table.

Q&A watchdog answer bits for TCAN1576-Q1 only

Figure 10-21. WD_QA_ANSWER Register

7	6	5	4	3	2	1	0
WD_QA_ANSWER							
R-00h							

Table 10-23. WD_QA_ANSWER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_QA_ANSWER	R/W	00h	MCU watchdog Q&A answer response byte

10.1.22 WD_QA_QUESTION Register (Address = 2Fh) [reset = 3Ch]

WD_QA_QUESTION is shown in Figure 10-22 and described in Table 10-24.

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Q&A watchdog question bits for TCAN1576-Q1 only

Figure 10-22. WD_QA_QUESTION Register

7	6	5	4	3	2	1	0
RSVD	QA_ANSW_ERR	WD_ANSW_CNT		WD_QUESTION			
R-0b	W1C-0b	R-11b		R-1100b			

Table 10-24. WD_QA_QUESTION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6	QA_ANSW_ERR	W1C	0b	Watchdog Q&A answer error flag
5-4	WD_ANSW_CNT	R	11b	Current state of received Watchdog Q&A error counter
3-0	WD_QUESTION	R	1100b	Current watchdog question value

10.1.23 SW_ID1 Register (Address = 30h) [reset = 00h]

SW_ID1 is shown in Figure 10-23 and described in Table 10-25.

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Extended ID bits 17:10

Figure 10-23. SW_ID1 Register

7	6	5	4	3	2	1	0
EXT_ID_17:10							
R/W-00h							

Table 10-25. SW_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_17:10	R/W	00h	Extended ID bits 17:10

10.1.24 SW_ID2 Register (Address = 31h) [reset = 00h]

SW_ID2 is shown in Figure 10-24 and described in Table 10-26.

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Extended ID bits 9:2

Figure 10-24. SW_ID2 Register

7	6	5	4	3	2	1	0
EXT_ID_9:2							
R/W-00h							

Table 10-26. SW_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_9:2	R/W	00h	Extended ID bits 9:2

10.1.25 SW_ID3 Register (Address = 32h) [reset = 00h]

SW_ID3 is shown in Figure 10-25 and described in Table 10-27.

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Extended ID bits 1:0, Extended ID Field, ID[10:6] and Extended ID[28:24]

Figure 10-25. SW_ID3 Register

7	6	5	4	3	2	1	0
EXT_ID_1:0		IDE	ID_10:6__EXT_ID_28:24				
R/W-00b		R/W-0b	R/W-00000b				

Table 10-27. SW_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	EXT_ID_1:0	R/W	00b	Extended ID bits 1:0
5	IDE	R/W	0b	Extended ID field 0b = Standard ID (11-bits) 1b = Extended ID (29-bits)
4-0	ID_10:6__EXT_ID_28:24	R/W	00000b	ID[10:6] and Extended ID[28:24]

10.1.26 SW_ID4 Register (Address = 33h) [reset = 00h]

SW_ID4 is shown in Figure 10-26 and described in Table 10-28.

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ID[5:0] and Extended ID[23:18]

Figure 10-26. SW_ID4 Register

7	6	5	4	3	2	1	0
ID_5:0__EXT_ID_23:18						RESERVED	
R/W-000000b						R-00b	

Table 10-28. SW_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	ID_5:0__EXT_ID_23:18	R/W	000000b	ID[5:0] and Extended ID[23:18]
1-0	RESERVED	R	00b	Reserved

10.1.27 SW_ID_MASK1 Register (Address = 34h) [reset = 00h]

SW_ID_MASK1 is shown in Figure 10-27 and described in Table 10-29.

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Extended ID Mask 17:16

Figure 10-27. SW_ID_MASK1 Register

7	6	5	4	3	2	1	0
RESERVED						EXT_ID_MASK_17:16	
R-000000b						R/W-00b	

Table 10-29. SW_ID_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved
1-0	EXT_ID_MASK_17:16	R/W	00b	Extended ID Mask 17:16

10.1.28 SW_ID_MASK2 Register (Address = 35h) [reset = 00h]

SW_ID_MASK2 is shown in Figure 10-28 and described in Table 10-30.

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Extended ID Mask 15:8

Figure 10-28. SW_ID_MASK2 Register

7	6	5	4	3	2	1	0
EXT_ID_MASK_15:8							
R/W-00h							

Table 10-30. SW_ID_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_MASK_15:8	R/W	00h	Extended ID Mask 15:8

10.1.29 SW_ID_MASK3 Register (Address = 36h) [reset = 00h]

SW_ID_MASK3 is shown in Figure 10-29 and described in Table 10-31.

Return to Summary Table.

Extended ID Mask 7:0

Figure 10-29. SW_ID_MASK3 Register

7	6	5	4	3	2	1	0
EXT_ID_MASK_7:0							
R/W-00h							

Table 10-31. SW_ID_MASK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_MASK_7:0	R/W	00h	Extended ID Mask 7:0

10.1.30 SW_ID_MASK4 Register (Address = 37h) [reset = 00h]

SW_ID_MASK4 is shown in Figure 10-30 and described in Table 10-32.

Return to Summary Table.

ID Mask 10:3 and Extended ID Mask 28:21 (Base ID)

Figure 10-30. SW_ID_MASK4 Register

7	6	5	4	3	2	1	0
ID_MASK_10:3__EXT_ID_MASK_28:21							
R/W-00h							

Table 10-32. SW_ID_MASK4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ID_MASK_10:3__EXT_ID_MASK_28:21	R/W	00h	ID Mask 10:3 and Extended ID Mask 28:21 (Base ID)

10.1.31 SW_ID_MASK_DLC Register (Address = 38h) [reset = 00h]

SW_ID_MASK_DLC is shown in Figure 10-31 and described in Table 10-33.

Return to Summary Table.

ID Mask 2:0 and Extended ID Mask 20:18 (Base ID), DLC[3:0], Data mask enable

Figure 10-31. SW_ID_MASK_DLC Register

7	6	5	4	3	2	1	0
SW_ID_MASK_5			DLC				DATA_MASK_EN
R/W-000b			R/W-0000b				R/W-0b

Table 10-33. SW_ID_MASK_DLC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	SW_ID_MASK_5	R/W	000b	ID Mask 2:0 and Extended ID Mask 20:18 (Base ID)
4-1	DLC	R/W	0000b	DLC[3:0]
0	DATA_MASK_EN	R/W	0b	Data mask enable 0b = DLC field and Data field are not compared and assumed valid. Remote frames are allowed. 1b = DLC field must match DLC[3:0] register and data field bytes are compared with DATAx registers for a matching 1. Remote frames are ignored

10.1.32 DATA_y Register (Address = 39h + formula) [reset = 00h]

DATA_y is shown in Figure 10-32 and described in Table 10-34.

Return to Summary Table.

Register address 39h through 40h

Offset = 39h + (y x 1h); where y = 0h to 7h

Figure 10-32. DATA_y Register

7	6	5	4	3	2	1	0
DATAx							
R/W-00h							

Table 10-34. DATA_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATAx	R/W	00h	CAN data byte x

10.1.33 SW_RSVD_y Register (Address = 41h + formula) [reset = 00h]

SW_RSVD_y is shown in Figure 10-33 and described in Table 10-35.

Return to Summary Table.

Register address 41h through 43F

Offset = 41h + (y x 1h); where y = 0h to 2h

Figure 10-33. SW_RSVD_y Register

7	6	5	4	3	2	1	0
RSVD							
R-00h							

Table 10-35. SW_RSVD_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	00h	Reserved

10.1.34 SW_CONFIG_1 Register (Address = 44h) [reset = 50h]

SW_CONFIG_1 is shown in Figure 10-34 and described in Table 10-36.

Return to Summary Table.

CAN and CAN FD DR and Behavior

Figure 10-34. SW_CONFIG_1 Register

7	6	5	4	3	2	1	0
SW_FD_PASSIVE	CAN_DR			FD_DR		RSVD	
R/W-0b	R/W-101b			R/W-00b		R-00b	

Table 10-36. SW_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_FD_PASSIVE	R/W	0b	Selective Wake FD Passive: this bit modifies the behavior of the error counter when CAN with flexible data rate frames are seen. 0b = CAN with flexible data rate frame is counted as an error frame 1b = CAN with flexible data rate frame are ignored (passive)
6-4	CAN_DR	R/W	101b	CAN bus data rate 000b = 50 Kbps 001b = 100 Kbps 010b = 125 Kbps 011b = 250 Kbps 100b = Reserved 101b = 500 Kbps 110b = Reserved 111b = 1 Mbps
3-2	FD_DR	R/W	00b	CAN bus FD data rate ratio verses CAN data rate 00b = CAN FD <= 4x CAN data rate 01b = CAN FD => 5x and <= 10x CAN data rate 10b = Reserved 11b = Reserved
1-0	RSVD	R	0b	Reserved

10.1.35 SW_CONFIG_2 Register (Address = 45h) [reset = 00h]

SW_CONFIG_2 is shown in Figure 10-35 and described in Table 10-37.

Return to Summary Table

Frame Error Counter: this error counter is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. If the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame has no impact on the frame error counter (no increment or decrement). If the frame counter reaches FRAME_CNT_THRESHOLD[7:0] value, the next increment overflows the counter, set FRAME_OVF flag. The counter is reset by the following: enabling the frame detection or $t_{SILENCE}$ detection.

Figure 10-35. SW_CONFIG_2 Register

7	6	5	4	3	2	1	0
FRAME_CNTx							
RH-00h							

Table 10-37. SW_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FRAME_CNTx	RH	00h	Frame Error Counter: this error counter is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. In case the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame will have no impact on the frame error counter (no increment or decrement). If the frame counter reaches FRAME_CNT_THRESHOLD[7:0] value the next increment will overflow the counter, set FRAME_OVF flag. The counter is reset by the following: enabling the frame detection or $t_{SILENCE}$ detection.

10.1.36 SW_CONFIG_3 Register (Address = 46h) [reset = 1Fh]

SW_CONFIG_3 is shown in Figure 10-36 and described in Table 10-38.

Return to Summary Table.

Frame Error Counter Threshold: these bits set the point at which the error counter reaches the maximum set value and on the next error frame overflows and sets the FRAME_OVF flag. Default is 31 so the 32nd error sets the overflow flag

Figure 10-36. SW_CONFIG_3 Register

7	6	5	4	3	2	1	0
FRAME_CNT_THRESHOLD							
R/W-1Fh							

Table 10-38. SW_CONFIG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FRAME_CNT_THRESHOLD	R/W	1Fh	Frame Error Counter Threshold: these bits set the point at which the error counter reaches the maximum value and on the next error frame causes an overflow and sets the FRAME_OVF flag. Default is 31 so the 32nd error, the overflow flag sets.

10.1.37 SW_CONFIG_4 Register (Address = 47h) [reset = 00h]

SW_CONFIG_4 is shown in Figure 10-37 and described in Table 10-39.

Return to Summary Table.

Figure 10-37. SW_CONFIG_4 Register

7	6	5	4	3	2	1	0
SWCFG	CAN_SYNC_FD	CAN_SYNC	RSVD				
RH/W-0b	RH-0b	RH-0b	R-00000b				

Table 10-39. SW_CONFIG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWCFG	RH/W	0b	Selective wake configuration complete 0b = SW registers not configured 1b = SW registers configured Note: Make this the last step in configuring and turning on selective wake. **Note** NOTE: Writing to any of these wake configuration registers (8'h30-8'h44, 8'h46) clears the SWCFG bit.
6	CAN_SYNC_FD	RH	0b	Device is properly decoding CAN FD frames if frame detection is enabled. This flag is updated after every received frame. By polling this flag, the system can determine if the device is properly decoding CAN FD frames, up to but not including the Data Field. This flag is self-clearing.
5	CAN_SYNC	RH	0b	Synchronized to CAN data: this flag indicates if the device is properly decoding CAN frames if frame detection is enabled. This flag is updated after every received frame. By polling this flag the system can determine if the device is properly decoding CAN frames. This flag is self-clearing.
4-0	RSVD	R	00000b	Reserved

10.1.38 SW_CONFIG_RSVD_y Register (Address = 48h + formula) [reset = 00h]

SW_CONFIG_RSVD_y is shown in Figure 10-38 and described in Table 10-40.

Return to Summary Table.

Register address 48h through 4Ah

Offset = 48h + (y x 1h); where y = 0h to 2h

Figure 10-38. SW_CONFIG_RSVD_y Register

7	6	5	4	3	2	1	0
RSVD							
R-00h							

Table 10-40. SW_CONFIG_RSVD_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	00h	Reserved

10.1.39 DEVICE_CONFIGx Register (Address = 4Bh) [reset = 0h]

DEVICE_CONFIGx is shown in Figure 10-39 and described in Table 10-41.

Return to Summary Table.

Disables the V_{CC} requirement on RXD toggling LOW during wake. WAKE event on RXD powered by VIO only.

Figure 10-39. DEVICE_CONFIGx Register

7	6	5	4	3	2	1	0
RESERVED							VCC_DIS
R-00000b							R/W-0b

Table 10-41. DEVICE_CONFIGx Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	00000b	Reserved
0	VCC_DIS	R/W	0b	Disables the VCC requirement on RXD toggling LOW during WAKE. 0b =VCC requirement enabled 1b = VCC requirement disabled

10.1.40 INT_GLOBAL Register (Address = 50h) [reset = 00h]

INT_GLOBAL is shown in Figure 10-40 and described in Table 10-42.

Return to Summary Table.

Logical OR of all to certain interrupts

Figure 10-40. INT_GLOBAL Register

7	6	5	4	3	2	1	0
GLOBALERR	INT_1	INT_2	INT_3	INT_CANBUS	RSVD		
RH-0b	RH-0b	RH-0b	RH-0b	RH-0b	R-000b		

Table 10-42. INT_GLOBAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBALERR	RH	0b	Logical OR of all interrupts
6	INT_1	RH	0b	Logical OR of INT_1 register
5	INT_2	RH	1b	Logical OR of INT_2 register
4	INT_3	RH	0b	Logical OR of INT_3 register
3	INT_CANBUS	RH	0b	Logical OR of INT_CANBUS register
2-0	RSVD	R	0000b	Reserved

10.1.41 INT_1 Register (Address = 51h) [reset = 00h]

INT_1 is shown in Figure 10-41 and described in Table 10-43.

Return to Summary Table.

Interrupts are dependent on device. All interrupts are for TCAN1576-Q1. Selective wake interrupts are for TCAN157x-Q1.

Figure 10-41. INT_1 Register

7	6	5	4	3	2	1	0
WD	CANINT	LWU	WKERR	FRAME_OVF	CANSLNT	CANTO	CANDOM
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-43. INT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD	R/W1C	0b	Watchdog event interrupt. **Note** This interrupt bit is set for every watchdog error event and does not rely upon the Watchdog error counter
6	CANINT	R/W1C	0b	CAN bus wake up interrupt
5	LWU	R/W1C	0b	Local wake up
4	WKERR	R/W1C	0b	Wake error bit is set when the SWE timer has expired and the state machine has returned to Sleep mode
3	FRAME_OVF	R/W1C	0b	Frame error counter overflow
2	CANSLNT	R/W1C	0b	CAN bus inactive for $t_{SILENCE}$
1	CANTO	R/W1C	0b	CAN bus inactive for $t_{SILENCE}$ while Selective Wake is enabled and in Sleep mode
0	CANDOM	R/W1C	0b	CAN bus stuck dominant

10.1.42 INT_2 Register (Address = 52h) [reset = 40h]

INT_2 is shown in Figure 10-42 and described in Table 10-44.

Return to Summary Table.

Interrupts All interrupts are for TCAN1576-Q1. Selective wake interrupts are for TCAN157x-Q1

Figure 10-42. INT_2 Register

7	6	5	4	3	2	1	0
SMS	PWRON	RSVD	UVSUP	UVIO	UVCC	TSD	TSDW
R/W1C-0b	R/W1C-1b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-44. INT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SMS	R/W1C	0b	Sleep mode status flag. Only sets when sleep mode is entered by a WKERR, UVIO timeout or UVIO + TSD fault
6	PWRON	R/W1C	1b	Power on
5	RSVD	R-0b	0b	Reserved
4	UVSUP	R/W1C	0b	V_{SUP} under voltage
3	UVIO	R/W1C	0b	V_{IO} under voltage
2	UVCC	R/W1C	0b	V_{CC} under voltage
1	TSD	R/W1C	0b	Thermal Shutdown
0	TSDW	R/W1C	0b	Thermal Shutdown Warning

10.1.43 INT_3 Register (Address 53h) [reset = 00h]

INT_3 is shown in Figure 10-43 and described in Table 10-45.

Return to Summary Table.

All interrupts are for TCAN1576-Q1. Selective wake interrupts are for TCAN157x-Q1.

The CRC_EEPROM interrupt is set when the internal EEPROM used for trimming has a CRC error. Upon power up, the device loads an internal register from the EEPROM and performs a CRC check. If an error is present after eight attempts of loading valid data, the CRC_EEPROM interrupt is set. This interrupt indicates an error that can impact device performance. The process is repeated when the device leaves sleep mode or fail-safe mode due to a wake event. The device performs a CRC check on the internal registers loaded from the EEPROM. If there is an error, the device reloads the registers from the EEPROM. If there is a CRC error, the device attempts to load the internal registers up to eight times. After the eighth attempt, the CRC_EEPROM interrupt flag is set. This indicates an error that can impact the device performance.

Figure 10-43. INT_3 Register

7	6	5	4	3	2	1	0
SPIERR	SWERR	FSM	RSVD				CRC_EEPROM
R/W1C-0b	RH-0b	R/W1C-0b	R-0000b				R/W1C-0b

Table 10-45. INT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR	R/W1C	0b	Sets when SPI status bit sets
6	SWERR	RH	0b	Logical OR of (SW_EN=1 and NOT(SWCFG)) and FRAME_OVF. Selective Wake may not be enabled while SWERR is set
5	FSM	R/W1C	0b	Entered fail-safe mode. Cleared while in fail-safe mode.
4-1	RSVD	R	0000b	Reserved
0	CRC_EEPROM	R/W1C	0b	EEPROM CRC error

10.1.44 INT_CANBUS Register (Address = 54h) [reset = 00h]

INT_CANBUS is shown in Figure 10-44 and described in Table 10-46.

Return to Summary Table.

CAN bus faults that include shorts and opens for TCAN1576-Q1

Figure 10-44. INT_CANBUS Register

7	6	5	4	3	2	1	0
RSVD	RSVD	CANHCANL	CANHBAT	CANLGND	CANBUSOPEN	CANBUSGND	CANBUSBAT
R-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 10-46. INT_CANBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	RESERVED	R	0b	Reserved
5	CANHCANL	R/W1C	0b	CANH and CANL shorted together
4	CANHBAT	R/W1C	0b	CANH shorted to Vbat
3	CANLGND	R/W1C	0b	CANL shorted to GND
2	CANBUSOPEN	R/W1C	0b	CAN bus open
1	CANBUSGND	R/W1C	0b	CAN bus shorted to GND or CANH shorted to GND
0	CANBUSBAT	R/W1C	0b	CAN bus shorted to Vbat or CANL shorted to Vbat

10.1.45 INT_GLOBAL_ENABLE (Address = 55h) [reset = 00h]

INT_GLOBAL_ENABLE is shown in Figure 10-45 and described in Table 10-47.

Return to Summary Table.

Interrupt mask for Global interrupts

Figure 10-45. INT_GLOBAL_ENABLE Register

7	6	5	4	3	2	1	0
RSVD							
R-00h							

Table 10-47. INT_GLOBAL_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	00h	Reserved

10.1.46 INT_ENABLE_1 Register (Address = 56h) [reset = FFh]

INT_ENABLE_1 is shown in Figure 10-46 and described in Table 10-48.

Return to Summary Table.

Interrupt masks for INT_1; All interrupt masks are for TCAN1576-Q1. Selective wake interrupt masks are for TCAN157x-Q1

Figure 10-46. INT_ENABLE_1 Register

7	6	5	4	3	2	1	0
WD_ENABLE	CANINT_ENABLE	LWU_ENABLE	WKERR_ENABLE	FRAME_OVF_ENABLE	CANSLNT_ENABLE	CANTO_ENABLE	CANDOM_ENABLE
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 10-48. INT_ENABLE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_ENABLE	R/W	1b	Watchdog event interrupt enable
6	CANINT_ENABLE	R/W	1b	CAN bus wake up interrupt enable
5	LWU_ENABLE	R/W	1b	Local wake up enable
4	WKERR_ENABLE	R/W	1b	Wake error enable
3	FRAME_OVF_ENABLE	R/W	1b	Frame error counter overflow enable
2	CANSLNT_ENABLE	R/W	1b	CAN silent enable
1	CANTO_ENABLE	R/W	1b	CAN timeout enable
0	CANDOM_ENABLE	R/W	1b	CAN bus stuck dominant enable

10.1.47 INT_ENABLE_2 Register (Address = 57h) [reset = 1Fh]

INT_ENABLE_2 is shown in Figure 10-47 and described in Table 10-49.

Return to Summary Table.

Interrupt masks for INT_2

Figure 10-47. INT_ENABLE_2 Register

7	6	5	4	3	2	1	0
RSVD			UVSUP_ENABLE	UVIO_ENABLE	UVCC_ENABLE	TSD_ENABLE	TSDW_ENABLE
R-000b			R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 10-49. INT_ENABLE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Reserved
4	UVSUP_ENABLE	R/W	1b	V_{SUP} under voltage enable
3	UVIO_ENABLE	R/W	1b	V_{IO} under voltage enable
2	UVCC_ENABLE	R/W	1b	V_{CC} under voltage enable
1	TSD_ENABLE	R/W	1b	Thermal shutdown enable
0	TSDW_ENABLE	R/W	1b	Thermal shutdown warning enable

10.1.48 INT_ENABLE_3 Register (Address = 58h) [reset = 0h]

INT_ENABLE_3 is shown in Figure 10-48 and described in Table 10-50.

Return to Summary Table.

Interrupt masks for INT_3

Figure 10-48. INT_ENABLE_3 Register

7	6	5	4	3	2	1	0
SPIERR_ENABLE	SWERR_ENABLE	FSM_ENABLE	RSVD				
R/W-1b	R/W-0b	R/W-1b	R-00000b				

Table 10-50. INT_ENABLE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR_ENABLE	R/W	1b	SPI error interrupt enable
6	SWERR_ENABLE	R/W	0b	Selective wake error enable
5	FSM_ENABLE	R/W	1b	Fail-safe mode enable
4-0	RSVD	R	00000b	Reserved

10.1.49 INT_ENABLE_CANBUS Register (Address = 59h) [reset = 7Fh]

INT_ENABLE_CANBUS is shown in INT_ENABLE_CANBUS Register and described in INT_ENABLE_CANBUS Register Field Descriptions.

Return to Summary Table.

Interrupt masks for INT_CANBUS

Figure 10-49. INT_ENABLE_CANBUS Register

7	6	5	4	3	2	1	0
RSVD	RSVD	CANHCANL_ENABLE	CANHBAT_ENABLE	CANLGND_ENABLE	CANBUSOPEN_ENABLE	CANBUSGND_ENABLE	CANBUSBAT_ENABLE
R-0b	R-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 10-51. INT_ENABLE_CANBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	RESERVED	R	1b	Reserved
5	CANHCANL_ENABLE	R/W	1b	CANH and CANL shorted together enable
4	CANHBAT_ENABLE	R/W	1b	CANH shorted to Vbat enable
3	CANLGND_ENABLE	R/W	1b	CANL shorted to GND enable
2	CANBUSOPEN_ENABLE	R/W	1b	CAN bus open enable
1	CANBUSGND_ENABLE	R/W	1b	CAN bus shorted to GND enable
0	CANBUSBAT_ENABLE	R/W	1b	CAN bus shorted to Vbat enable

10.1.50 INT_RSVD_y Register (Address = 5Ah + formula) [reset = 00h]

INT_RSVD_y is shown in Figure 10-50 and described in Table 10-52.

Return to Summary Table.

Register address 58h through 5Fh

Offset = 58h + (y x 1h); where y = 0h to 7h

Figure 10-50. INT_RSVD_y Register

7	6	5	4	3	2	1	0
RSVD							
R-00h							

Table 10-52. INT_RSVD_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	00h	Reserved

11 Device and Documentation Support

This device will conform to the following CAN standards. The core of what is needed is covered within this system specification, however reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed. However, for a full understanding of CAN including the protocol these additional sources will be very helpful as the scope of CAN protocol in detail is outside the scope of this physical layer (transceiver) specification.

11.1 Documentation Support

11.1.1 CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2016: High speed medium access unit with low power mode (super sets -2 standard electrically in several specs and adds the original wake up capability via the bus in low power mode)
- ISO 8802-3: CSMA/CD – referenced for collision detection from ISO11898-2
- CAN FD 1.0 Spec and Papers
- Bosch “Configuration of CAN Bit Timing”, Paper from 6th International CAN Conference (ICC), 1999. This is repeated a lot in the DCAN IP CAN Controller spec copied into this system spec.
- GMW3122: GM requirements for HS CAN
- SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
- SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps
- Bosch M_CAN Controller Area Network Revision 3.2.1.1 (3/24/2016)

11.1.2 EMC Requirements:

- SAE J2962-2: Communication Transceivers Qualification Requirements - CAN
- HW Requirements for CAN, LIN,FR V1.3: German OEM requirements for HS CAN

11.1.3 Conformance Test Requirements:

- HS_TRX_Test_Spec_V_1_0: GIFT / ICT CAN test requirements for High Speed Physical Layer

11.1.4 Related Documentation

- “A Comprehensible Guide to Controller Area Network”, Wilfried Voss, Copperhill Media Corporation
- “CAN System Engineering: From Theory to Practical Applications”, 2nd Edition, 2013; Dr. Wolfhard Lawrenz, Springer.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2025) to Revision B (August 2025)	Page
• First release of the Production data sheet	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1575DMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	TCAN 1575
TCAN1575DRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1575
TCAN1576DMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	TCAN 1576
TCAN1576DRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1576

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

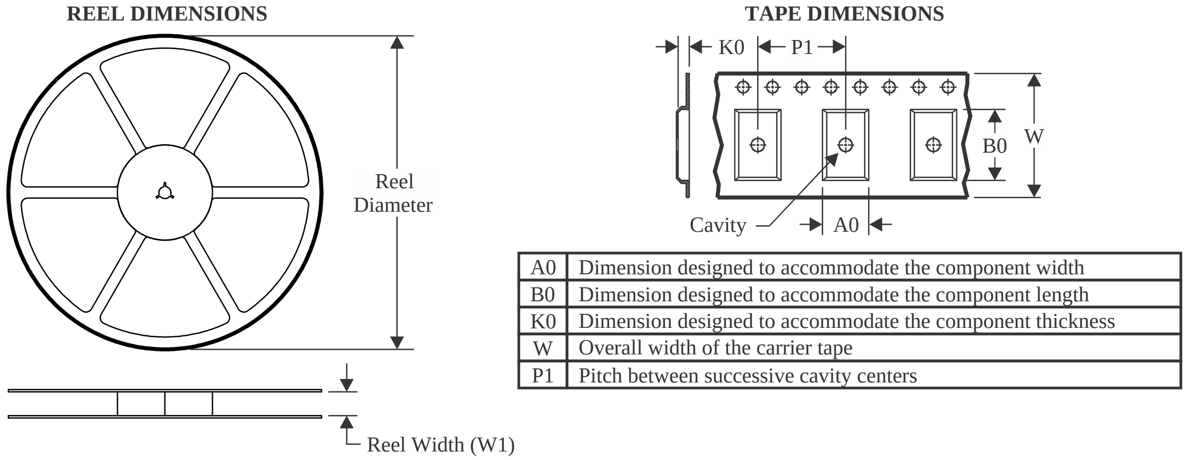
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

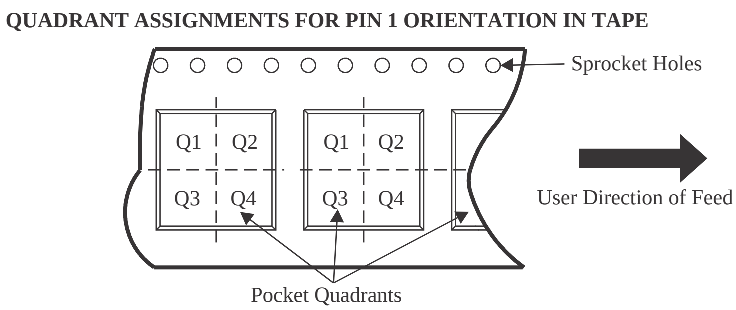
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



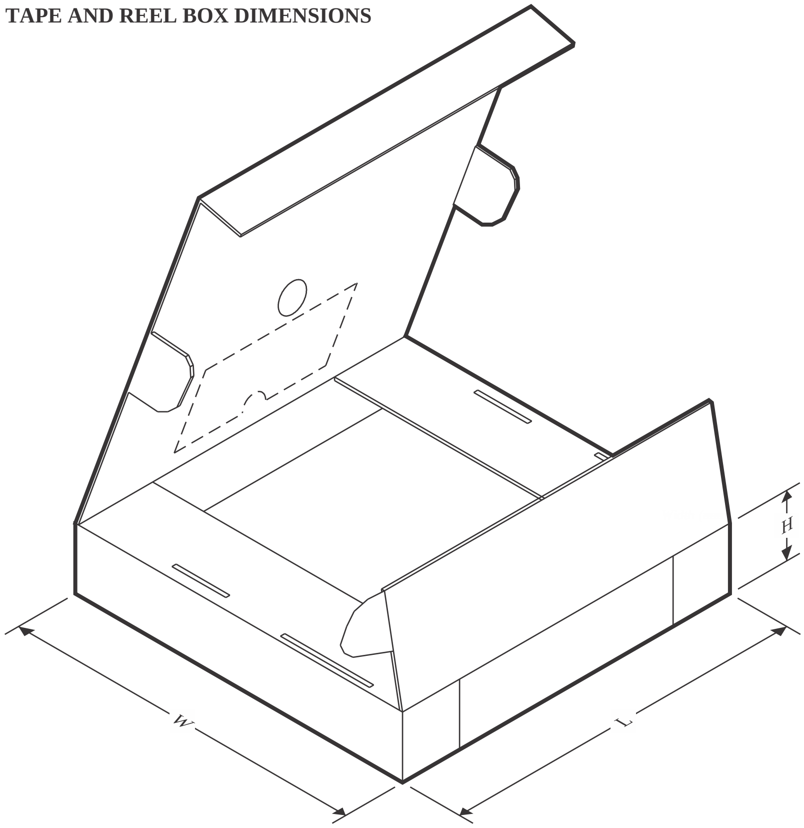
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

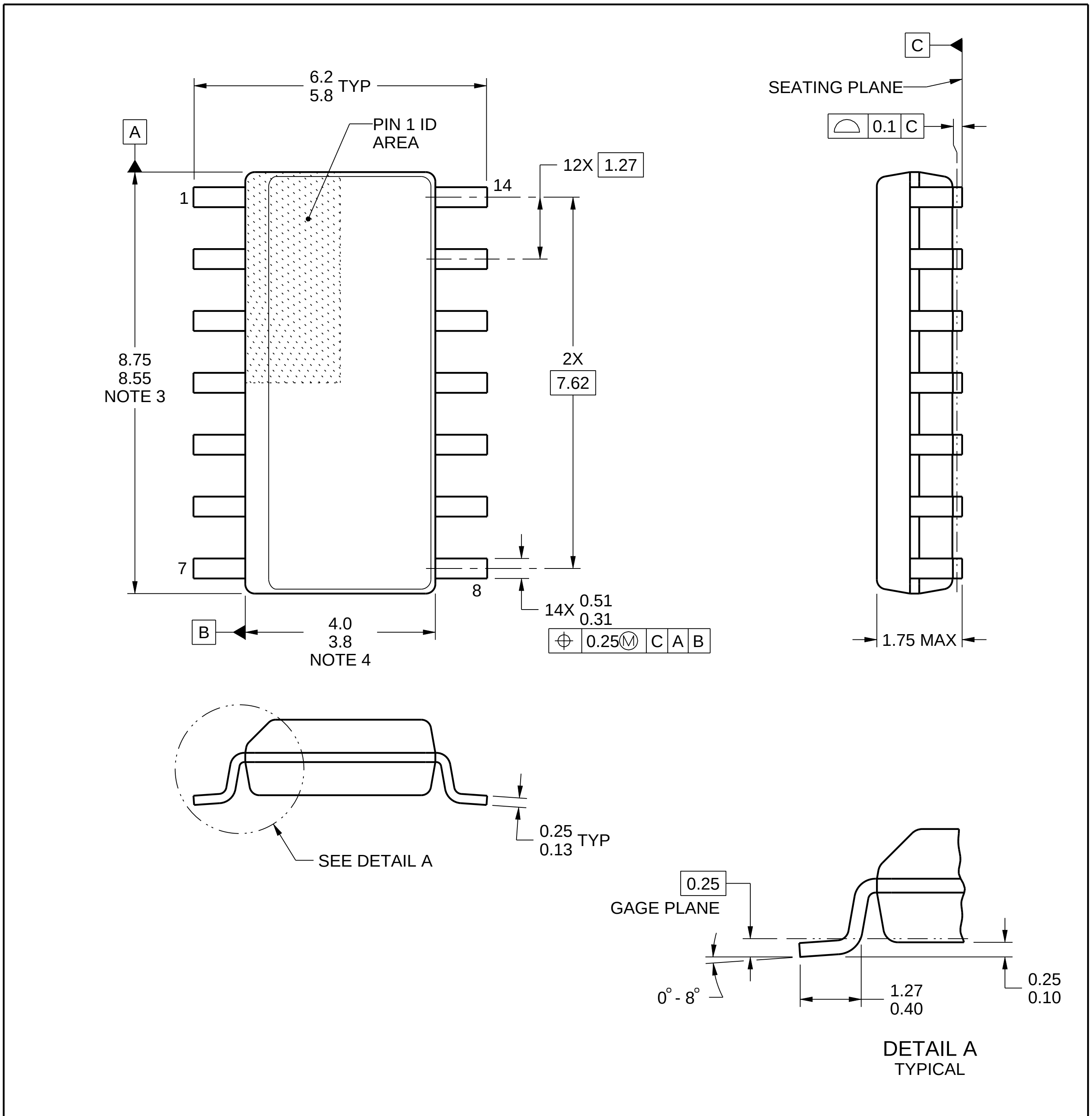
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1575DMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1575DRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1576DMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1576DRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

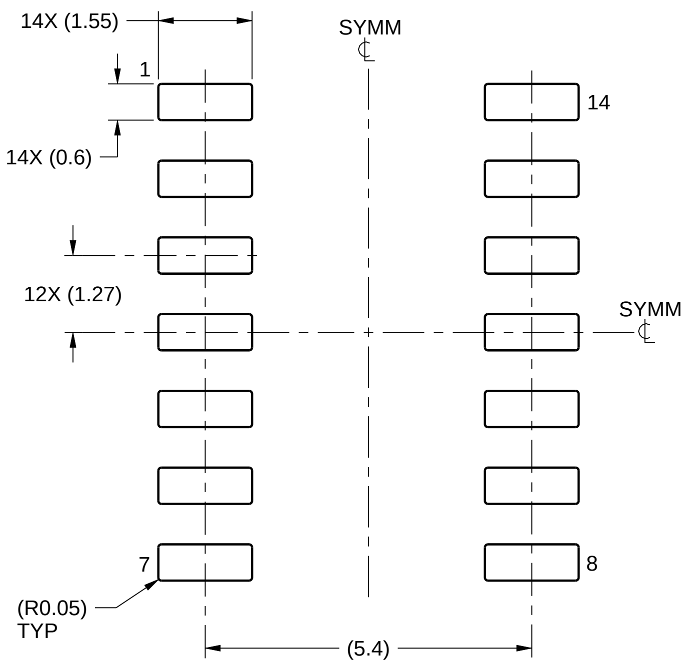
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1575DMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1575DRQ1	SOIC	D	14	2500	340.5	336.1	32.0
TCAN1576DMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1576DRQ1	SOIC	D	14	2500	340.5	336.1	32.0



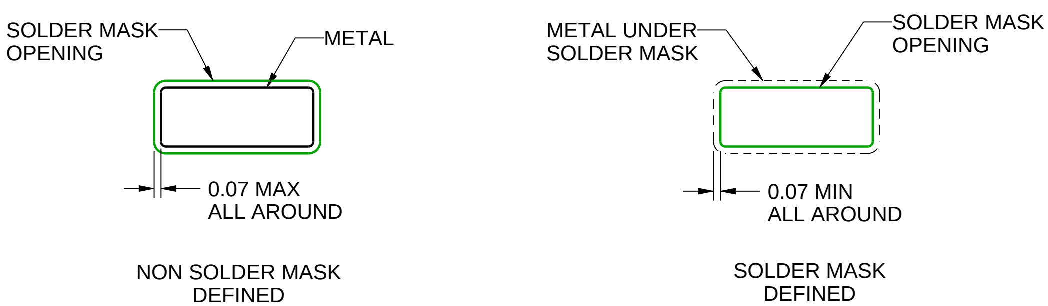
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

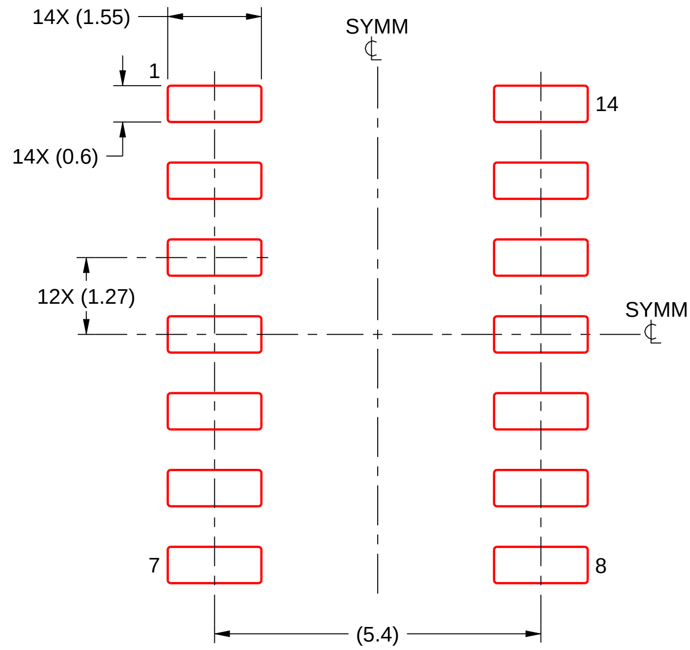


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



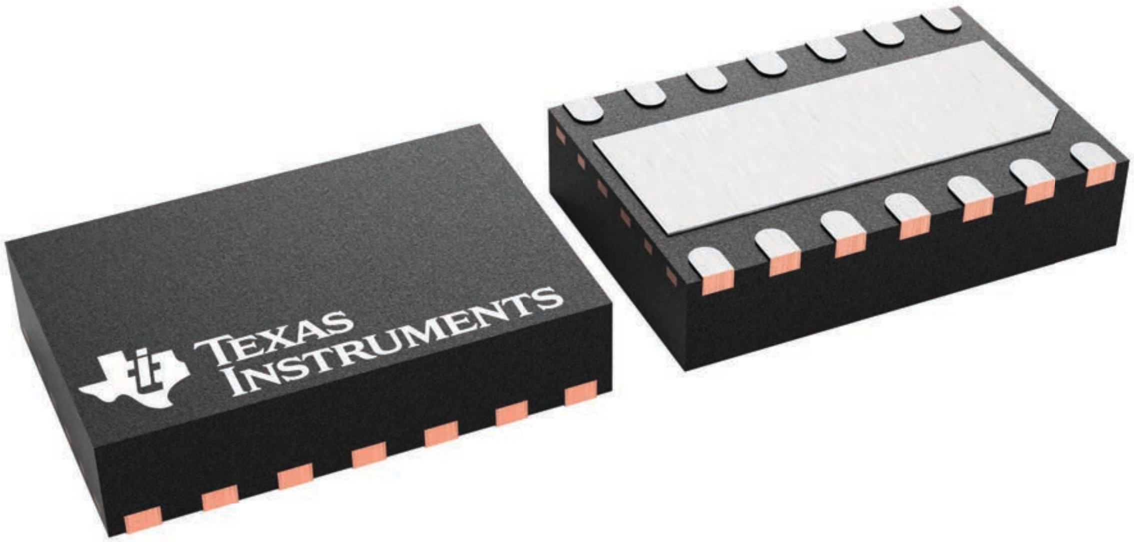
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

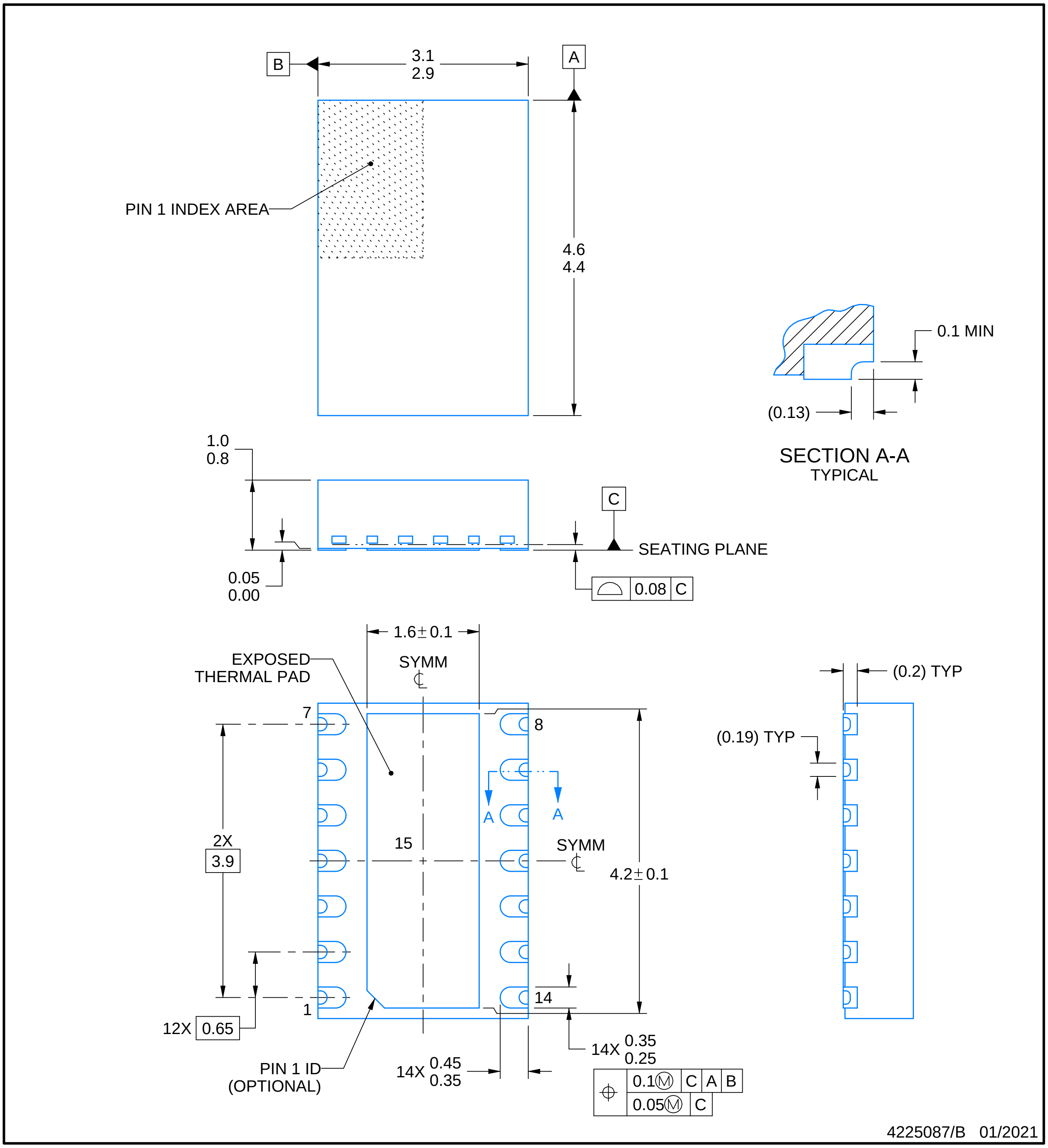


4225088/A

PACKAGE OUTLINE

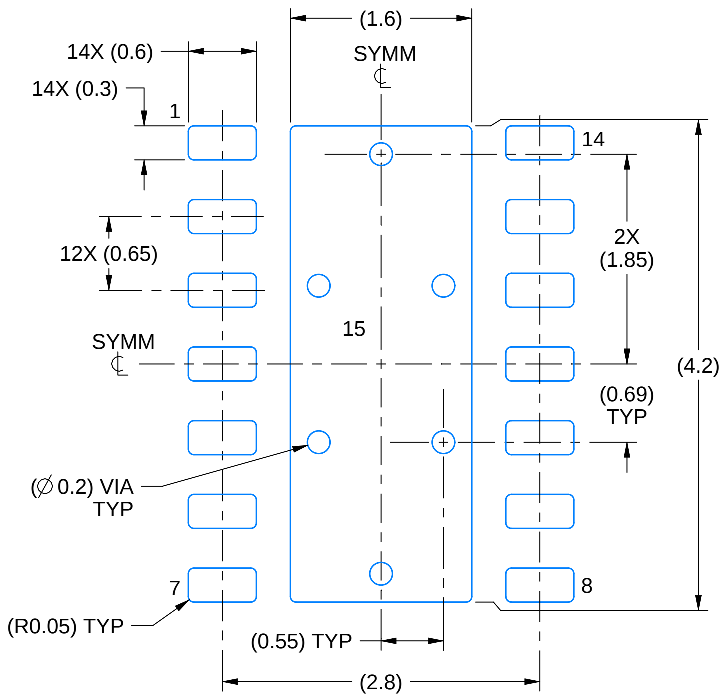
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

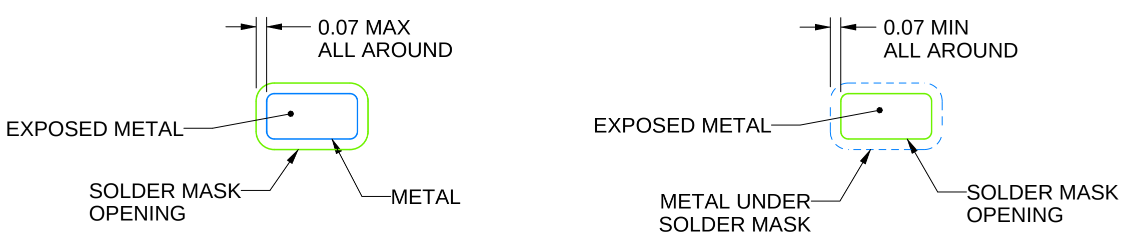


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

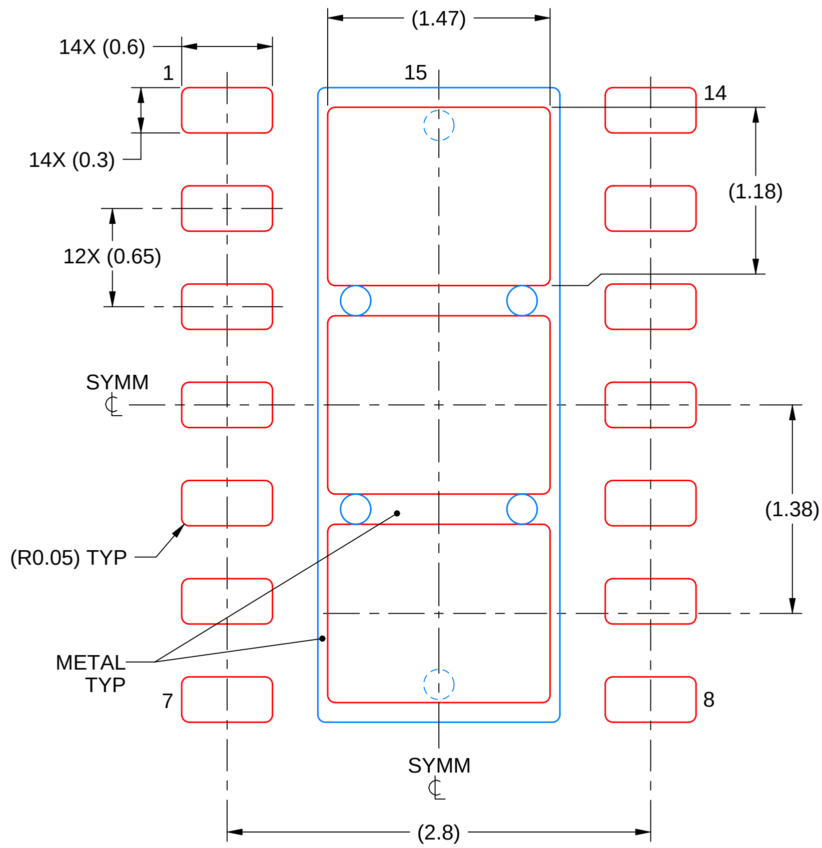
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225087/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/B 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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